MICROCOMPUTER SYSTEM BUSES

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The paper reviews some most popular microcomputer common buses which appeared together with the generation of 16-bit devices. Bus specifications considerably differ from each other, since most of them are primarily suited to a certain microprocessor family. The paper describes the most important functional characteristics of the following microcomputer buses: S-100, VERSAbus, Multibus, TM 990 bus and ZBI bus. A brief summary of connector types and card dimensions for each bus is given as well.

MIKRORAČUNALNIŠKA VODILA. Članek podaja pregled mikroračunalniških vodil, ki so nastala vzporedno z generacijo 16-bitnih mikroprocesorjev. Vodila se med seboj precej razlikujejo, saj so v večini primerov "pisana na kožo" ene od mikroprocesorskih familij. Članek predstavlja mikroračunalniška sistemska vodila: S-100, VERSAbus, Multibus, TM 990 bus in ZBI bus z ozirom na njihove najpomembnejše funkcionalne karakteristike. Za vsako vodilo so opisani tudi tipi konektorjev in dimenzije kartic.

I. INTRODUCTION

One of the most important features of microcomputer system design is the implementation of the system bus. A common bus is a composition of unidirectional or bidirectional lines which transfer information and electrical power between the various components of a microcomputer system. These lines are characterised from a functional point of view (e.g. address lines, data lines,...), as well as from an electrical point of view (e.g. open collector line, three state line,...).

There are two basic types of functional elements that connect to the bus: masters and slaves. A bus master is any module having the ability to control the bus. It is capable to address bus slaves by generating proper control and address signals. A bus master has the capability to transfer messages to or from the addressed slave. A bus slave decodes the address lines and acts upon the command signals from the masters.
The overall behaviour of the events on the bus is defined by the bus protocol.

The last but not least important feature of the bus are its mechanical specifications (e.g. connector types, board size etc.). The bus structure is important to the users when they intend to upgrade their systems by, say, commercially available memory boards or peripherals.

II. MICROCOMPUTER BUS PROPOSALS

In the area of 8-bit microcomputers almost as many different backplane packaging and functional specifications were proposed as there were microprocessor manufacturers. Obviously, some of them gained more popularity than others (SBC 80, EXORcisor, Z-80 bus, PRO-LOG, to cite just a few of them). Still none is the favorit. As the 16-bit devices began to appear on the

market the same story happened again though with a considerably smaller number of bus proposals. Intel Multibus, Motorola VERSAbus, TM 990 bus and ZILOG ZBI bus are widely proclaimed but they all tend to be specific to the computer they were designed for. In some cases, the design of the bus is constrained by the fact that compatibility with preceding members of the microprocessor family is provided. VERSAbus and ZBI bus are here outstanding exceptions. They still provide means for supporting 8-bit microprocessors but their upper limit is 32 rather than 16-bit data transfer.

Despite differences in internal CPU architecture, bus protocol of any microprocessor system exerts similar master - slave relations. For example, communication with memory and peripherals requires similar signals and timing relationship. Consequently, a universal bus structure which is independant of actual microprocessor type should be possible to define. The S-100 bus resulted from the effords to create such "universal" bus. With its specification openly published by the IEEE it could meet most requirements for the present microcomputer systems and it had been adopted by many manufacturers. Yet, a drawback is that it had been originally designed for 8-bit data and 16-bit address lines. Its proposed exetention to 16-bit data lines has not been widely accepted.

In October 1980, the IEEE Computer Society proposed the 796 Bus Standard which is actually only a slight modification of the Multibus and is stated to be "a cooperative industry effort toward establishing a standard for a large number of manufacturers and users of microcomputer modules".

The purpose of this paper is not to make an assessment of advantages and disadvantages of the contenders for the title of "industry standard". Instead, most common features of microprocessor bus proposals are reviewed to acquaint the reader with their basic design.

III. ADDRESS AND DATA LINES

All the above mentioned buses provide means for 8 and 16-bit data transfer, but still considerable differences exist in the way to accomplish this. Likawise, the number of address lines differs from each other resulting in different addressing capabilities.
The data bus of the S-100 bus consists of 16 lines which are grouped as two unidirectional 8-bit buses for byte transfer and as a single bidirectional bus for 16-bit word format. The address bus consists of 16 lines for standard memory addressing (64 k locations), or of 24 lines for extended memory addressing (16 M locations).

The Multibus provides 16 bit data bus and 20 bit address bus. The implementation of the 8 and 16-bit data transfer employs a special Swap Byte Buffer which must be included in any 16-bit master or slave in order tc maintain compatibility with previous 8-bit masters and slaves. The 20 address lines allow a maximum of 1 M bytes of memory to be accessed.

The VERSAbus provides 16 bit data and 24 bit address lines which can both be expanded to 32 lines using the second connector.

The TM 990 data bus consists of 16 lines. The 20 address lines are comprised of 16 basic and 4 extended address lines. Up to 1 M bytes can be addressed by means of the memory mapping technique.

The most significant difference between the ZBI bus and other buses is in the way of the transfer of data and address information. The ZBI bus uses a multiplexed bus structure with 32 data or address lines. This gives a smaller number of bus interconnections, at the expense of a slight increase in the complexity of the circuits connected by the bus. 32 lines provide means to accomodate future 32-bit microprocessors and offer wide addressing capability.

IV. BUS ARBITRATION

All 16-bit microprocessors are designed to allow multiprocessing. They have facilities to handle bus control which can accomodate several bus masters on the same system, each taking control of the bus for its own data transfer.

The S-100 bus arbitration system uses 4 bus lines for arbitrating among 16 temporary masters. In general, one permanent master may exist in the system and it has the highest arbitration priority. Each temporary master has a unique priority number which it asserts on the arbitration bus at an appropriate time. A temporary master can get the control of the bus from the permanent master only for an arbitrary number of bus cycles. Then it must return the control to the

permanent master. The parallel priority resolution is implemented by means of additional logic stored on each master board interfacing to the arbitration lines.
There are another 4 lines on the bus to disable the line drivers of the permanent master making together 8 control lines for the DMA arbitration.

In cases where the existence of the permanent master in the system may prove to be inefficient, a dummy master may replace it. The dummy master merely passes the control of the bus from one temporary master to another. It is especially suitable when a number of processors co-exist in a single system.

The Multibus offers two bus exchange priority techniques: serial and parallel. Serial priority resolution is accomplished with a daisy - chain technique. A relatively small number of masters can be accomodated in this way. Due to the present time hardware limitations only up to 3 masters can be accomodated in a system with bus clock period of 100 ns.
In the parallel technique, the priority is resolved by means of a priority resolution circuit. This circuit must be externally supplied and its position in the system is not strictly determined by the bus standard. If the parallel technique is used a practical limit of 16 masters in a system is stated.

The VERSAbus provides 5 level bus arbitration. Each level can be implemented as a daisy - chain to increase the number of bus masters. The priority is first resolved among the five levels and then within the elements of the daisy - chain of the level which gained the priority.

In the TM 990 bus specification the arbitration scheme is limited to a single daisy- chain like the Multibus serial resolution.

Similarly, the ZBI bus employs a serial daisy - chain resolution technique and four control lines to enable multiple processors to share the bus. While in the previously mentioned bus specificatoins a DMA module uses the same arbitration scheme as other processor modules in the system, the ZBI bus makes a distinction: it provides separate daisy - chain for the DMA arbitration.

V. INTERRUPT REQUEST SCHEME

The interrupt request scheme in the S-100 bus is comprised of an 8-level maskable vectored interrupt system and a non - maskable interrupt which is an optional control input to the bus masters. The eight interrupt request lines are inputs to a bus slave or an interrupt controller which masks and prioritizes the requests. As a result it outputs the interrupt request to the permanent master.

The Multibus can support bus vectored and non-bus vectored interrupts at the same time. Bus vectored interrupts are generated by the slave Priority Interrupt Controllers which transfer the vector address to the bus master. The non-bus vectored interrupts are handled on the bus master. A bus slave that requests the interrupt does not convey interrupt vector address on the bus, it is generated by the interrupt controller on the master.
Eight interrupt request lines enable 8-level priority interrupts.

To handle interrupts the VERSAbus provides a 7-level priority control. The 7 interrupt request lines are of the wire-ORed configuration so that each level can be expanded by a daisy - chain. The VERSAbus accomodates bus vectored interrupts.

15 general purpose vectored interrupts are defined in the TM 990 bus each having its own priority level. The interrupts are maskable by the primary master.

Interrupts on the ZBI signal lines can be implemented as maskable or non-maskable, vectored or non-vectored depending on how the CPU is configured. 9 interrupt lines organized into 3 independed groups exist on the bus each having its unique priority level.

VI. MISCELLANEOUS FUNCTIONS

A number of signals and their functions have not been described not to go too much into detailes. Nevertheless, let us review just a few interesting features. The decision, if they are worth mentioning is left to the reader.

The ZBI bus and the VERSAbus include parity check bits for data and address lines, while in general, each bus includes at least one generalized error line that indicates that the current operation is producing an error.

For the case of power failure, control signals are provided that indicate that the power is going to fail enabling the system to enter the power fail sequence. The system may store important data in memory which is powered by the standby power supply.

To enhance the system's integrity, clock signal lines are accompanied by their own signal-ground lines on the backplane.

	NUMBER OF CONNECTORS	CONNECTOR DESCRIPTION	CARD DIMENSIONS (in inches)
S-100	1	(50/100 pin) board edge connecter	5.125x10
VERSAbus	2	P1: (70/140 pin) board edge c. P2: (60/120 pin) board edge c.	9.25x6.5 (reduced size) or 9.25x14.5
Multibus	2	P1: (43/86 pin) board edge c. P2: (30/60 pin) board edge c.	12.00x6.75
TM 990	1	(50/100 pin) board edge c.	11x7.5
ZBI bus	2	P1: (32/32/32 pin) wirewrap c. P2: (32/32/32 pin) wirewrap c.	6.3x3.9 (Eurocard) or 6.3x9.2 (Double Euroc.)

Table 1

VII. MECHANICAL SPECIFICATIONS

Table 1. summarizes some most important mechanical specifications concerning the physical design of a bus backplane and the dimensions of the printed circuit boards that plug into the bus interface. Some remarks are necessary:

Signals of the VERSAbus P1 connector allow the implementation of a complete 16-bit device on a reduced size board. The P2 connector provides extension to service future 32-bit devices. P1 connector of the Multibus is the primary connector and P2 is an auxiliary connector. The ZBI system signals are all gathered together on the P1 connector, the P2 connector is reserved entirely for the user application.

VIII. CONCLUSION

Standardization of the microcomputer bus is an important element to be considered when microcomputer systems are designed. A number of bus standards have been proposed in the past. Each microprocessor maker was solving problems from his own point of view which resulted also in the different bus specifications.
This may be the reason why the IEEE works on a processor - independant standard P896 referred as the "future bus". The future bus, if it becomes the IEEE standard, will operate at rates over 10 MHz, the arbitration scheme will handle up to 64 masters in a sofisticated arbitration protocol, the interrupt control will handle 1024 priority levels.
Another bus design is reported from Intel. Developing the new 32-bit microprocessor iAPX 432, new bus interconnection concepts are announced. The last word has not been said yet.

IX. LITERATURE

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