VERTICAL SILICON-ON-NOTHING FET: SUBTHRESHOLD SLOPE CALCULATION USING COMPACT CAPACITANCE MODEL

B. Sviličić[1], V. Jovanović[2], T. Suligoj[3]

[1]Faculty of Maritime Studies, University of Rijeka, Rijeka, Croatia
[2]ECTM-DIMES, Delft University of Technology, The Netherlands
[3]Faculty of Electrical Engineering and Computing, University of Zagreb, Croatia

Key words: Silicon-on-Nothing, fully-depleted MOSFET, vertical SONFET, subthreshold slope, compact model

Abstract: The subthreshold slope model of the Vertical Silicon-on-Nothing FET, extracted from the compact capacitance model, has been developed. For short-channel effects modeling the voltage-doping transformation is used. The analytical model is verified by comparison to the two-dimensional numerical device simulator, MEDICI, over a wide range of different device structures. Good agreement is obtained for channel lengths down to 50 nm.

Vertikalni SONFET: modeliranje podpragovne tokovne karakteristike

Kjučne besede: SONFET, vertikalni SONFET, naklon podpragovne tokovne karakteristike, modeliranje

Izvleček: Razvili smo model podpragovne tokovne karakteristike vertikalnega tranzistorja SONFET (Silicon-on-nothing FET). Analitični model smo preverili s primerjavo rezultatov dobljenih z dvodimenzionalno simulacijo s programom MEDICI. Dobili smo dobro ujemanje izračunanih in izmerjenih vrednosti za dolžine kanala navzdol do 50nm.

1 Introduction

The scaling of conventional CMOS is approaching technological limits /1/, and the need for replacement device architecture is growing. A possible alternative is the Silicon-on-Nothing (SON) technology /2/, where the epitaxial process is used for the formation of the sacrificial SiGe layer and top Si layer for the active device part. The sacrificial SiGe region is later removed below transistor channel and replaced by an insulating material, resulting in quasi-SOI structure in the active region. However, the SON MOSFET (SONFET) transistors are processed on bulk Si wafers with reverse biased source and drain junctions to the substrate. This eliminates one of the major advantages of standard SOI technologies, which is the reduction of parasitic capacitances. The SON technology can also be transferred to SOI substrate, but with considerable increase in process complexity.

The Vertical Fully-Depleted SONFET (VFD SONFET) is developed as a further evolution of the lateral SONFET /3, 4, 5/. The channel length of the vertical SONFET is defined by the molecular-beam epitaxy (MBE), allowing the channel-length reduction into the sub-30 nm region without the need for high-resolution lithography. Furthermore, standard bulk region underneath the buried oxide is eliminated (Fig. 1.). The absence of the transistor bulk is a unique property of the VFD SONFET, not present in either bulk or SOI CMOS.

The subthreshold slope value is one of the key issues for deep-submicrometer devices, with the target value of 60 mV/dec at temperature of 300 K. In this paper, we give an analytical solution for the VFD SONFET subthreshold slope based on the compact capacitive model in subthreshold region. The voltage-doping transformation (VDT) is used for short-channel effects modeling and the solutions are verified in comparison to the results of two-dimensional device simulator.

2 Modelling

2.1 Capacitive model in subthreshold region

The analytical solution for subthreshold slope is based on the capacitive model in subthreshold region (Fig. 2.). The compact capacitive component model for the VFD SONFET operating in accumulation, depletion and inversion condition is presented in /6/.

Intrinsic capacities include the capacitance of the depleted silicon body $C_{Si,d}$, gate oxide capacitance $C_{GOX}=k_{GOX}L_{eff}/t_{GOX}$, and buried oxide capacitance C_{BOX}:

$$C_{BOX} = \frac{2k_{BOX}}{\pi} \ln\left(1+\frac{L_{eff}}{2\,d_{BOX}}\right) \quad (1)$$

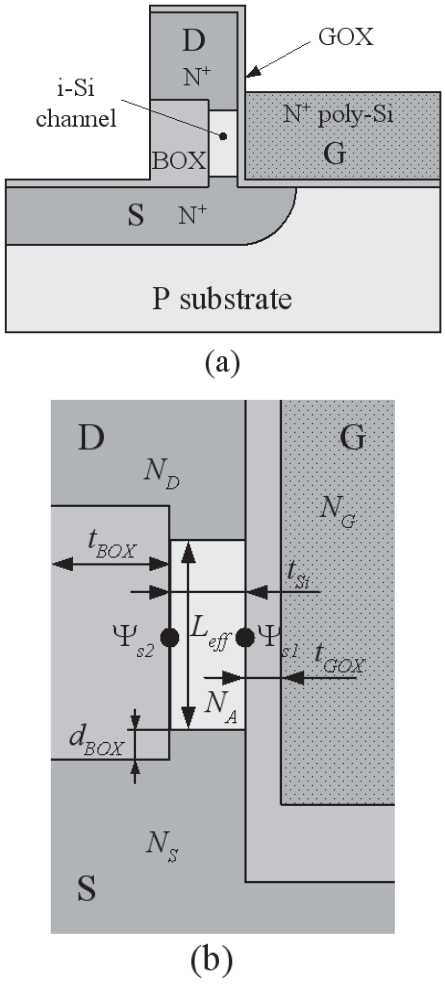

Fig. 1. (a) VFD SONFET structure cross-section, (b) VFD SONFET structure close-up.

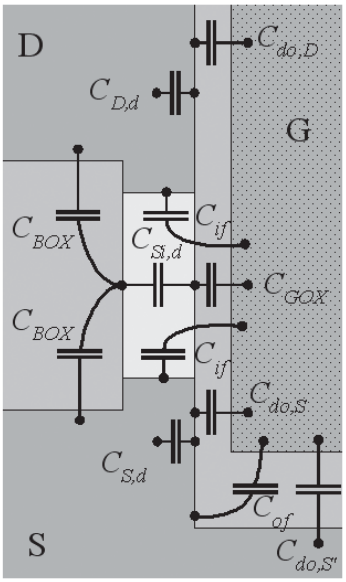

Fig. 2. Capacitive model of the VFD SONFET in the subthreshold region.

The buried oxide capacitance C_{BOX} of the VFD SONFET has specific, two-dimensional properties and its analytical relation is given with an approximation by perpendicular planes. For the effective channel lengths that are $t_{BOX} < L_{eff}/2$ analytical relation is given:

$$C_{BOX}\Big|_{t_{BOX}<\frac{L_{eff}}{2}} = \frac{2k_{BOX}}{\pi}\ln\left(1+\frac{t_{BOX}}{d_{BOX}}\right) \quad (2)$$

Overlap, fringe and source/drain depletion capacitances are also included in Fig. 2, but do not have significant influence on the subthreshold slope. Equivalent capacitive circuit of the VFD SONFET in the subthreshold region is shown on the Fig. 3.

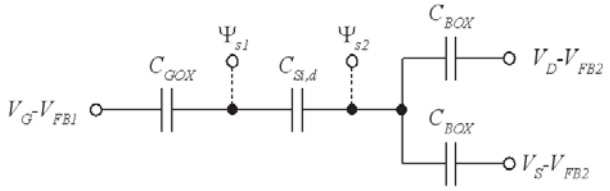

Fig. 3. Equivalent capacitive circuit of the VFD SONFET in the subthreshold region.

Applying the Ohms law at each node, we calculate the relation between the front-gate surface potential ψ_{S1} (interface gate-oxide/Si-film) and the back-gate surface potential ψ_{S2} (interface Si-Film/BOX) /Fig. 1 (b)/:

$$\Psi_{s1}\left(C_{GOX}+C_{Si,d}\right)= C_{GOX}\left(V_G - V_{FB1} + \frac{Q_{Si,d}}{2C_{GOX}}\right)+ C_{Si,d}\Psi_{s2} \quad (3)$$

$$\Psi_{s2}\left(2C_{BOX}+C_{Si,d}\right)= \\ = C_{BOX}\left(\left(V_D - V_{FB2}\right)+\left(V_S - V_{FB2}\right)+\frac{Q_{Si,d}}{2C_{BOX}}\right)+ C_{Si,d}\Psi_{s1} \quad (4)$$

where $Q_{Si,d}=-qN_At_{Si}$ is the depletion charge, $V_{FB1}=V_T\ln(N_GN_A/n_i^2)$ is the top-gate flat-band voltage, $V_{FB2}=V_T\ln(N_{S\text{-}D}N_A/n_i^2)$ is the back-gate flat-band voltage, and V_D and V_S are drain and source voltages, respectively. With source voltage being zero (V_S=0), the following relations can be used: $V_D+V_S=V_D=V_D-V_S=V_{DS}$. From the equivalent capacitive circuit, the analytical solution for the gate voltage V_G is extracted:

$$V_G = V_{FB1} + \Psi_{s1}\left(1+\frac{C_{Si,d}\,2C_{BOX}}{C_{GOX}\left(C_{Si,d}+2C_{BOX}\right)}\right)+ \\ + \frac{qN_At_{Si}}{C_{GOX}}\cdot\left(\frac{1}{C_{Si,d}}+\frac{1}{C_{BOX}}\right)\cdot\left(\frac{C_{Si,d}C_{BOX}}{\left(C_{Si,d}+2C_{BOX}\right)}\right)- \\ - V_{DS}\frac{C_{Si,d}C_{BOX}}{C_{GOX}\left(C_{Si,d}+2C_{BOX}\right)}+2V_{FB2}\frac{C_{Si,d}C_{BOX}}{C_{GOX}\left(C_{Si,d}+2C_{BOX}\right)} \quad (5)$$

2.2 Two-Dimensional Effects: Voltage Doping Transformation

An elegant and compact solution for two-dimensional model is offered by the concept of Voltage-Doping Transformation (VDT) /7/. VDT enables to account for 2D-effects into

quasi 1D-analysis of the VFD SONFET. According to this concept, the influence of the lateral field initiated by the junctions is equivalent to a reduction in the effective channel area doping. The effective doping in channel area:

$$N_A^* = N_A - \frac{\varepsilon_{Si} 2V_{DS}^*}{qL_{ef}^2} \tag{6}$$

Where

$$V_{DS}^* = V_{DS} + 2(V_{bi} + \Psi_{s2} - \Psi_{s1}) \pm \\ \pm 2\sqrt{(V_{bi} + \Psi_{s2} - \Psi_{s1})(V_{DS} + V_{bi} + \Psi_{s2} - \Psi_{s1})} \tag{7}$$

where V_{DS} is the drain-source voltage, $\psi_{bi}=V_T\ln(N_{S\text{-}D}N_A/n_i^2)$ is the built-in potential. The back-gate surface potential ψ_{s2} is given:

$$\Psi_{s2} = \frac{qN_A t_{Si} L_{eff}}{C_{BOX}} \tag{8}$$

The silicon body capacitance with short channel effects (VDT) taken into account is therefore:

$$C_{Si,d}^* = \frac{dQ}{d\Psi} = \frac{qN_A^* t_{Si} L_{eff}}{\Psi_{s1} - \Psi_{s2}} \tag{9}$$

As the subthreshold slope is defined in the regime before the onset of the strong inversion, the silicon body capacitance $C^*_{Si,d}$ will be evaluated for the front gate surface potential:

$$\Psi_{s1} = \Psi_{s1}(\text{inv}) = 2\Psi_b \tag{10}$$

where $\psi_b=V_T\ln(N_A/n_i)$ is the difference between Fermi level and intrinsic level.

2.3 Subthreshold slope model

Using the definition for the subthreshold slope as the gate voltage variation needed for the change of one decade in the drain current /8/ and applying the gate voltage solution (5) and the VDT approximation (6–10), the subthreshold slope follows as:

$$S = \frac{dV_G}{d\log I_D} = \ln(10)\cdot\frac{kT}{q}\cdot\frac{dV_G}{d\Psi_{s1}} = \\ = \ln(10)\cdot\frac{kT}{q}\cdot\left(1 + \frac{2C_{Si,d}^* C_{BOX}}{C_{GOX}(C_{Si,d}^* + 2C_{BOX})}\right) \tag{11}$$

The complex influence of the VFD SONFET parameters are combined in a simple form of (11) with second term in the bracket being responsible for the difference from the ideal S value of 60 mV/dec at 300 K. The scaling tendencies are clear from the capacitance ratio, where C_{GOX} should be increased and $C^*_{Si,d}$ and C_{BOX} decreased to approach the ideal value.

3 Calculation and simulation results

In order to verify the accuracy of the analytical model for the subthreshold slope, the calculated results are compared to a two-dimensional numerical device simulator, MEDICI /9/. Concentration dependent model for the low-field carrier mobility and the velocity saturation mobility model at high parallel electric field were used. Band-gap narrowing in silicon and polysilicon, Shockley-Read-Hall recombination and Auger recombination are taken into account. The gate current was modeled by the Lucky-electron gate current model and the simulation temperature was 300 K. The simulator does not include quantum effects. Focus of this paper is the device subthreshold characteristics where the quantum effects are less pronounced and the drift-diffusion model can be considered accurate.

The calculated and simulated subthreshold slope values plotted against effective channel-lengths L_{eff} are shown in Fig. 4. for different: (a) gate oxide thickness t_{GOX}, (b) gate dielectric k_{GOX}, (c) BOX dielectric k_{BOX}, and (d) BOX thickness t_{BOX}. The examined devices take advantage of the fully-depleted structure and have an effectively undoped channel for higher mobility. The range of effective channel-lengths investigated was between 288 nm – long channel case, and 22 nm – very short-channel. The simulated structures in each plot varied only in the effective channel-length with other dimensions and technological parameters kept the same.

For the effective channel lengths down to 100 nm, subthreshold values are close to ideal values of approximately 60 mV/dec. Agreements between the values obtained by the numerical simulations and analytical model are within 2 mV/dec (3%) for the channel lengths down to 50 nm. For shorter channel lengths (<50 nm) the deviation of our model is mainly due to the rough VDT approximation of the effective doping in channel area N^*_A and thus the calculation of the silicon body capacitance $C^*_{Si,d}$. As the channel length is reduced the influence of the last term in relation (11) becomes higher and more accurate modeling of $C^*_{Si,d}$ is necessarry.

The subthreshold slope can be improved by increasing the value of the gate oxide capacitance C_{GOX}, or by decreasing the value of the buried oxide capacitance C_{BOX}. If the gate oxide thickness t_{GOX} is scaled down /Fig. 4. (a)/ or the material with higher dielectric constant k_{GOX} is used for the gate oxide /Fig. 4. (b)/ the characteristics show expected improvements. The case of material with the lower dielectric constant k_{BOX} used for the buried oxide /Fig. 4. (c)/ also improves the subthreshold slope, as well as thinner buried oxide thickness t_{BOX} /Fig. 4. (d)/.

4 Conclusions

The subthreshold slope model extracted from the compact capacitance model of the VFD SONFET has been demonstrated. It has been shown that the developed model has high accuracy for channel lengths down to 50 nm and can be extended even further with improvement of the voltage-doping transformation, which is used to account for short-channel effects. With the simple processing of the VFD SONFET, devices with very short gates can be fabricated and the presented model used for the prediction of the subthreshold behavior. The specific, two-dimensional

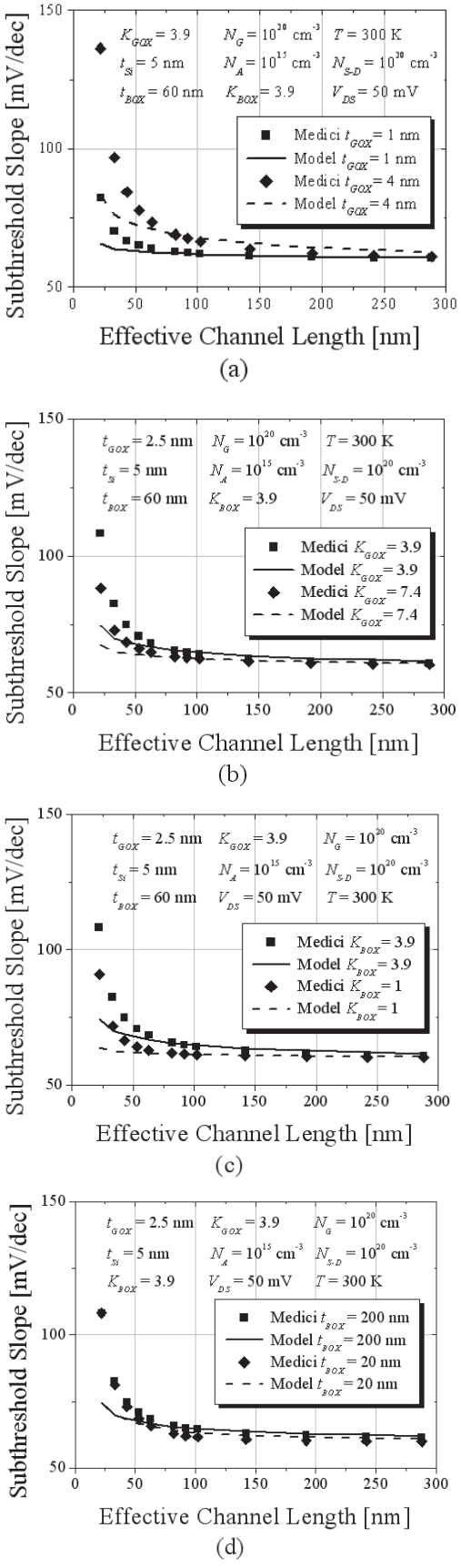

Fig. 4. Comparison of subthreshold slope values against effective channel lengths obtained by MEDICI simulations and analytical model for different: (a) t_{GOX}*, (b)* k_{GOX}*, (c)* k_{BOX}*, (d)* t_{BOX}*. K=k/*ε_0*.*

characteristics of the VFD SONFET structure are accurately described in the model and combined in a simple relation for the subthreshold slope. This offers clear insight into influences of different parts of the structure and can be used to estimate the performance of scaled devices.

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B. Sviličić,
Faculty of Maritime Studies, University of Rijeka,
Studentska ulica 2, 51000 Rijeka, Croatia
Phone: +385 (0)51 338 411, Fax: +385 (0)51 336 755,
E mail: svilicic@pfri.hr

V. Jovanović,
ECTM-DIMES, Delft University of Technology,
The Netherlands

T. Suligoj
Faculty of Electrical Engineering and Computing,
University of Zagreb, Croatia

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