UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

INFORMACIJE MIDEM 4 ◦ 1998

Strokovno društvo za mikroelektroniko elektronske sestavne dele in materiale

Strokovna revija za mikroelektroniko, elektronske sestavne dele in materiale
Journal of Microelectronics, Electronic Components and Materials

INFORMACIJE MIDEM, LETNIK 28, ŠT. 4(88), LJUBLJANA, december 1998

METAL OXIDE (ZnO) VARISTORS

IS
V230K20

Iskra
VARISTOR

INFORMACIJE MIDEM 4 ◦ 1998

INFORMACIJE MIDEM LETNIK 28, ŠT. 4(88), LJUBLJANA, DECEMBER 1998

INFORMACIJE MIDEM VOLUME 28, NO. 4(88), LJUBLJANA, DECEMBER 1998

Izdaja trimesečno (marec, junij, september, december) Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale.

Published quarterly (march, june, september, december) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

Glavni in odgovorni urednik / Editor in Chief
Dr. Iztok Šorli, dipl.ing., MIKROIKS d.o.o., Ljubljana

Tehnični urednik / Executive Editor
Dr. Iztok Šorli, dipl.ing.,

Uredniški odbor / Editorial Board
Doc. dr. Rudi Babič, dipl.ing., Fakulteta za elektrotehniko, računalništvo in informatiko Maribor
Dr.Rudi Ročak, dipl.ing., MIKROIKS d.o.o., Ljubljana
mag.Milan Slokan, dipl.ing., MIDEM, Ljubljana
Zlatko Bele, dipl.ing., MIKROIKS d.o.o., Ljubljana
Dr. Wolfgang Pribyl, Austria Mikro Systeme International AG
mag. Meta Limpel, dipl.ing., MIDEM, Ljubljana
Miloš Kogovšek, dipl.ing., Ljubljana
Dr. Marija Kosec, dipl. ing., Inštitut Jožef Stefan, Ljubljana

Časopisni svet / International Advisory Board
Prof. dr. Slavko Amon, dipl.ing., Fakulteta za elektrotehniko, Ljubljana, PREDSEDNIK - PRESIDENT
Prof. dr. Cor Claeys, IMEC, Leuven
Dr. Jean-Marie Haussonne, EIC-LUSAC, Octeville
Dr. Marko Hrovat, dipl.ing., Inštitut Jožef Stefan, Ljubljana
Prof. dr. Zvonko Fazarinc, dipl.ing., CIS, Stanford University, Stanford
Prof. dr. Drago Kolar, dipl.ing., Inštitut Jožef Stefan, Ljubljana
Dr. Giorgio Randone, ITALTEL S.I.T. spa, Milano
Prof. dr. Stane Pejovnik, dipl.ing., Kemijski inštitut, Ljubljana
Dr. Giovanni Soncini, University of Trento, Trento
Prof.dr. Janez Trontelj, dipl.ing., Fakulteta za elektrotehniko, Ljubljana
Dr. Anton Zalar, dipl.ing., ITPO, Ljubljana
Dr. Peter Weissglas, Swedish Institute of Microelectronics, Stockholm

Naslov uredništva / Headquarters
Uredništvo Informacije MIDEM
Elektrotehniška zveza Slovenije
Dunajska 10, 1000 Ljubljana, Slovenija
tel.: + 386 (0)61 1512 221
fax: + 386 (0)61 1512 217

Iztok.Sorli@guest.arnes.si
http://pollux.fer.uni-lj.si/midem/journal.htm

Letna naročnina znaša 12.000,00 SIT, cena posamezne številke je 3000,00 SIT. Člani in sponzorji MIDEM prejemajo Informacije MIDEM brezplačno.
Annual subscription rate is DEM 200, separate issue is DEM 50. MIDEM members and Society sponsors receive Informacije MIDEM for free.

Znanstveni svet za tehnične vede I je podal pozitivno mnenje o reviji kot znanstveno strokovni reviji za mikroelektroniko, elektronske sestavne dele in materiale. Izdajo revije sofinanci rajo Ministrstvo za znanost in tehnologijo in sponzorji društva.
Scientific Council for Technical Sciences of Slovene Ministry of Science and Technology has recognized Informacije MIDEM as scientific Journal for microelectronics, electronic components and materials.
Publishing of the Journal is financed by Slovene Ministry of Science and Technology and by Society sponsors.

Znanstveno strokovne prispevke objavljene v Informacijah MIDEM zajemamo v podatkovne baze COBISS in INSPEC.

Prispevke iz revije zajema ISI® v naslednje svoje produkte: Sci Search®, Research Alert® in Materials Science Citation Index™

Scientific and professional papers published in Informacije MIDEM are assessed into COBISS and INSPEC databases.

The Journal is indexed by ISI® for Sci Search®, Research Alert® and Material Science Citation Index™

Po mnenju Ministrstva za informiranje št.23/300-92 šteje glasilo Informacije MIDEM med proizvode informativnega značaja, za katere se plačuje davek od prometa proizvodov po stopnji 5 %.

Grafična priprava in tisk / Printed by: BIRO M, Ljubljana

Naklada / Circulation: 1000 izvodov / 1000 issues

Poštnina plačana pri pošti 1102 Ljubljana
Slovenia Taxe Percue

UDK621.3:(53+54+621+66), ISSN0352-9045 | Informacije MIDEM 28(1998)4, Ljubljana

ZNANSTVENO STROKOVNI PRISPEVKI		PROFESSIONAL SCIENTIFIC PAPERS
MIDEM'98 KONFERENCA - POVABLJENI REFERATI		MIDEM'98 CONFERENCE - INVITED PAPERS
K. Reichmann, N. Katsarakis, A. Reichmann: Elektronsko prevodni perovskitni materiali	**205**	K. Reichmann, N. Katsarakis, A. Reichmann: Electronically Conductive Perovskite Type Materials
S. Sokolić, S. Amon: Modeli za transport nosilcev v bazi npn SiGe heterospojnega transistorja	**211**	S. Sokolić, S. Amon: Models for Carrier Transport in the Base of npn SiGe HBTs
H. Gugg-Schwaiger: Mešana CMOS tehnologija firme Alcatel Microelectronics z minimalno razsežnostjo 0.5 μm	**218**	H. Gugg-Schwaiger: Alcatel Microelectronics 0.5μm Mixed CMOS Technology
M. Topič, F. Smole: Amorfnosilicijevi tankoplastni detektorji barv	**223**	M. Topič, F. Smole: Thin Film Color Detectors Based on Amorphous Silicon
M.H. LaBranche, C.J. McCormick, J.D. Smith, R.L. Keusseyan, R.C. Mason, M.A. Fahey, C.R.S.Needes, K.W. Hang:Naslednja generacija materialov za večplastna debeloplastna vezja	**230**	M.H. LaBranche, C.J. McCormick, J.D. Smith, R.L. Keusseyan, R.C. Mason, M.A. Fahey, C.R.S. Needes, K.W. Hang: Next-generation, Advanced Thick Film Multilayer System
KONFERENCA MIDEM'98 - POROČILO	**236**	MIDEM'98 CONFERENCE - REPORT
PREDSTAVLJAMO PODJETJE Z NASLOVNICE	**242**	REPRESENT OF COMPANY FROM FRONT PAGE
Iskra Varistor		Iskra Varistor
MIDEM IN NJEGOVI ČLANI		MIDEM SOCIETY AND ITS MEMBERS
Ervinu Pirtovšku v spomin	**247**	Ervin Pirtovšek in memoriam
VESTI	**248**	NEWS
KOLEDAR PRIREDITEV	**254**	CALENDAR OF EVENTS
VSEBINA LETNIKA 1998	**256**	VOLUME 1998 CONTENT
MIDEM prijavnica	**259**	MIDEM Registration Form
Slika na naslovnici: Iskra Varistor, proizvajalec varistorjev in supresorjev		Front page: Iskra Varistor, Varistor and Couplings Manufacturing Company

VSEBINA CONTENT

DRUŠTVO MIDEM IN KONFERENCA MIDEM NA INTERNETU

Dragi člani društva in bralci revije!

Predstavitev društva MIDEM in predstavitev konferenc MIDEM lahko poiščete na INTERNETU in sicer :

1. Predstavitev društva MIDEM in revije " Informacije MIDEM " na naslovu
http://pollux.fer.uni-lj.si/midem/society.htm
http://pollux.fer.uni-lj.si/midem/journal.htm

2. Predstavitev konference MIDEM na naslovu
http://pollux.fer.uni-lj.si/midem/conf98.htm

3. Elektronsko pošto lahko pošiljate na naslov :
Iztok.Sorli@guest.arnes.si
Pri vpisu naslovov pazite na velike in majhne črke !!

Vse člane vljudno prosimo, da poravnajo članarino za leto 1998.

MIDEM SOCIETY AND MIDEM CONFERENCE ON INTERNET

Dear readers and Society members !

Presentation of MIDEM Society and the information on the MIDEM Conference can be found on INTERNET as follows :

1. Presentation of MIDEM Society and Journal "Informacije MIDEM", address
http://pollux.fer.uni-lj.si/midem/society.htm
http://pollux.fer.uni-lj.si/midem/journal.htm

2. Presentation of the MIDEM Conference, address
http://pollux.fer.uni-lj.si/midem/conf98.htm

3. Email can be sent to :
Iztok.Sorli@guest.arnes.si
Please, use exact lower and upper case letters as indicated.

We kindly ask all our members to pay the membership fee for 1998.

ELECTRONICALLY CONDUCTIVE PEROVSKITE TYPE MATERIALS

Klaus Reichmann, Nikos Katsarakis, Angelika Reichmann
Institute for Chemical Technology of Inorganic Materials
Graz University of Technology

INVITED PAPER
MIDEM´98 CONFERENCE
23.09.98 – 25.09.98, Rogaška Slatina, Slovenia

Keywords: perovskite type materials. electronically conductive materials, oxide materials, electronic conductance, ion conductance, proton conductance, polaronic conductance, band type conductance, polarons, semiconductor technology, band formation, band structures, temperature dependence

Abstract: Since oxide materials with exceptional electronic properties recently found their application in semiconductor technology, materials research has got important stimulation. New preparative techniques offer the possibility to integrate materials, whose utilisation for a long time was considered to be confined to the ceramics world. This contribution will give a review on a group of electronically conductive oxides with perovskite structure. A short introduction into the crystallography is followed by an overview of theoretical models of band type conduction and polaronic conduction. General considerations for the formation of bands are discussed and the conditions for itinerant or localised electrons are outlined. Examples are given to illustrate these concepts.

Elektronsko prevodni perovskitni materiali

Ključne besede: materiali tipa perovskite, materiali prevodni elektronsko, materiali oksidni, prevodnost elektronska, prevodnost ionska, prevodnost protonska, prevodnost polaronska, prevodnost tipa pas, polaroni, tehnologija polprevodnikov, oblikovanje pasov, strukture pasovne, odvisnost temperaturna

Povzetek: Uporaba oksidnih materialov z izjemnimi elektronskimi lastnostmi v polprevodniški tehnologiji je dodatno vzpodbudilo raziskovanje na področju materialov. Nove tehnike priprave so omogočile izdelavo komponent, v katerih so kombinirani oksidni materiali z različnimi karakteristikami. V prispevku obravnavamo skupino elektronsko prevodnih oksidov s perovskitno strukturo. Po kratkem uvodu, ki obravnava kristalografijo teh materialov, nadaljujemo s pregledom teoretičnih modelov pasovnega in polaronskega prevajanja. Obravnavamo splošne pogoje za tvorbo prevodnih pasov kakor tudi pogoje za pojav lokaliziranih elektronov. Z nekaj primeri tudi podpremo opisane koncepte.

1. INTRODUCTION

Perovskites represent a very common type of ternary compounds with the general formula ABO_3. They exhibit a wide range of interesting electrical and magnetic properties, which depend primarily on the character of the d-electrons of the metal cation at the B-site. Most ABO_3 compounds are semiconductors or insulators. However a few of them show metal-like electronic conductivity, while others are good ionic conductors. Similar is the range of magnetic properties including the interesting effect of giant magnetoresistance. The source of electric conductivity in some cases is the electronic structure and the formation of bands like in $SrRuO_3$ or $LaNiO_3$. Such compounds theoretically can be treated as "metals". Due to the temperature dependence of spin and valence states and coupling of the electronic orbitals non-metal to metal transitions or semiconductor to metal transitions can be observed.

Another reason for conductivity may be the formation of polarons as charge carriers. Polarons are electrons, partially localised by the polarisation of the lattice. The transport of a polaron in an electric field needs the hopping over an energy barrier located between neighbouring cations of the same species with different valence state. The preparation and modification of such mixed valence compounds can be done by doping with heterovalent cations (examples will be given). In other cases the mixed valence is caused intrinsically by oxygen deficiency. The temperature characteristics of such polaron conductors is similar to semiconductors because of the activated charge transport.

Just to complete this overview it has to be mentioned that also ionic conductivity occurs in perovskite type oxides as oxide ion conduction (e.g. $LaAlO_3$ and $CaTiO_3$) or as proton conduction (e.g. doped $SrZrO_3$). The effect depends strongly on the concentration and distribution of vacancies in the lattice. Ionic conductivity is combined in some cases with a certain electronic conductivity. For some applications e.g. electrode materials for solid oxide fuel cells (SOFC) such a mixed ionic and electronic conductivity is highly appreciated.

Principal investigations and the theoretical treatment of these types of conductors have been done years and decades ago. The application of these materials however is just on the start. Nowadays conductive perovskites are under investigation as electrode material as well as solid electrolyte for solid oxide fuel cells (SOFC), to replace noble metal electrodes or as sensor material. As thin films these compounds have raised attention as buffer layers or even electrodes for ferroelectric /1/ or superconductive /2/ thin films. New preparative techniques such as pulsed laser deposition, magnetron sputtering or chemical solution deposition are vital for extending the field of application.

2. STRUCTURAL CONSIDERATIONS

Particular for the crystallography of ABX_3 perovskites is the combination of cations of different size. The bigger A-cation, similar in size to the anion X, forms together with this anion a close packed cubic structure. There the A-cation is twelve-fold co-ordinated. The smaller B-cation occupies octahedrally co-ordinated interstices in that structure entirely formed by the anions. By this way, octahedra containing B-cations are linked at their corners to form a three-dimensional framework (fig. 1).

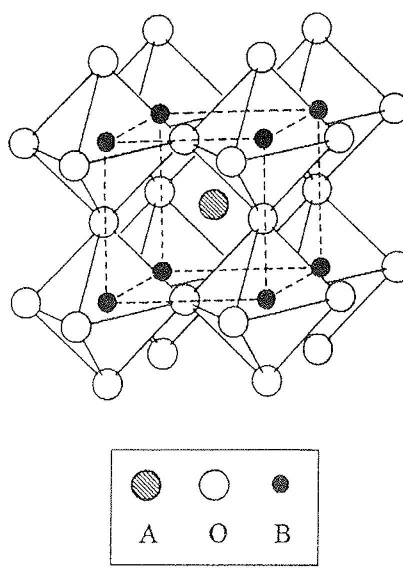


Fig. 1: Unit cell of an ideal perovskite ABO_3.

The stability of the perovskite structure is primarily derived from the electrostatic energy achieved by the twelve-fold co-ordination of the A-cation. These sites are formed by the corner sharing octahedra containing the B-cation. Thus the first prerequisite of a stable perovskite is the existence of a rigid octahedral framework, which, in turn, requires the preference of the B-cation for an octahedral co-ordination. Moreover a high effective charge is favourable. Since any A-cation must occupy the relatively large interstices created by these corner sharing octahedra, a second prerequisite is the appropriate size of the A-cation. If the A-cation is too large, the B-X bond length cannot be optimised, thus hexagonal stacking with face sharing octahedra becomes competitive /3,4/. If the A-cation is too small, A-X bonding stabilises structures with a lower anionic co-ordination around the A-cation. It should be noted that the ionic radii strongly influence the bonding between the ions and by that way also the band structure.

Goldschmidt /5/ defined a very useful relationship for the stability of perovskites containing a tolerance factor t.

$$R_A + R_X = t\sqrt{2}(R_B + R_X) \qquad (1)$$

R_A, R_B and R_X are the empirical ionic radii of the respective ions. The perovskite structure occurs only for values of $0.8 < t < 1.1$. The ideal close packing with cubic structure corresponds to $t = 1$. In most cases however orthorhombic and rhombohedral distortions occur, but also tetragonal, triclinic and monoclinic structures are found. Small values for t ($t < 0.8$) correspond to a comparable size of A-and B-cations and lead to more close packed structures like ilmenite. For $t > 1$ the space available for the B-cation in its oxygen cage becomes so large that a displacement is possible. This is the origin of the ferroelectric effect of $BaTiO_3$.

The valences of the A- and B-cation can be chosen nearly arbitrarily as long as they sum up to six. Thus perovskites can be classified as I-V-perovskites (e.g. $KNbO_3$), II-IV-perovskites (e.g. $BaTiO_3$) and III-III-perovskites (e.g. $LaCoO_3$). Even ReO_3 can be treated as perovskite with Re^{6+} as B-cation and a vacancy as "A-cation". Because of the different size of the cations, an inversion, i.e. an exchange between A- and B-cations like in spinels, is impossible. On the other hand the perovskite structure is very tolerant towards defects and so deviations from stoichiometry (oxygen excess or deficiency) can cause mixed-valence compounds. The defect distribution can be statistical or ordered, forming superstructures. Well known for such defect superstructures are the perovskite type high temperature superconductors.

3. PEROVSKITES WITH BAND STRUCTURE

Several perovskite oxides exhibit metallic conductivity. Typical examples are ReO_3, A_xWO_3, $AMoO_3$ (A = Ca, Sr, Ba), $SrVO_3$, $LaTiO_3$ and $LaNiO_3$. An early but still very valuable approach to the band structure of transition metal compounds was derived by Goodenough /6, 7, 8/. With empirically formulated criteria for the overlap of cation-cation and cation-anion-cation orbitals, Goodenough rationalises the nature of the d-electrons in transition metal compounds and the conditions for localised and itinerant electrons.

The concept is based on the transfer energy term b_{ij}, which measures the strength of the interaction between two neighbouring atoms i and j:

$$b_{ij} = \langle \Psi_i H \Psi_j \rangle \approx \varepsilon_{ij} \langle \Psi_i \Psi_j \rangle \qquad (2)$$

In this equation H is the Hamilton operator for the electronic wave functions or orbitals Ψ_i and Ψ_j of the neighbouring atoms i and j and ε_{ij} is the one-electron energy term. The expression $\langle \Psi_i \Psi_j \rangle$ is known as overlap integral. Although it is not possible to get good absolute estimates of b_{ij}, one can predict its variation in a series of isostructural compounds. In oxides with significant cation-cation interaction, b_{ij} is proportional to the reciprocal cation-cation separation. Where the cation-anion-cation interaction is important, b_{ij} is related to the covalent mixing of the cation-anion orbitals. For small values of b_{ij}, the outer d-electrons are localised, for large values of b_{ij} they are itinerant in a band and behave like in a metal. In a series of isostructural compounds, there is a critical value of the transfer energy, separating the localised from the itinerant electron regime. This critical transfer energy b_c is expressed in terms of the position of the cation in the periodic table, the principal quantum number of the d-orbital, the formal charge and the total spin of the cation.

In the case of the perovskite the B-cations are octahedrally co-ordinated by the anions. That means that d-orbitals of the B-cation are no longer degenerated but split into e_g-and t_{2g}-orbitals. This splitting has to be taken into account for estimating the overlap integrals. Figure 2 illustrates the position and the interesting electron orbitals in the perovskite structure. The B-cations are placed in the corners of a cube with the anions inbetween on the edges. To simplify at one B-cation only the e_g-orbitals and on another B-cation only the t_{2g} -orbitals are drawn. For the one anion the p-orbitals are drawn. The bonding between anion and B-cation thus can be σ- or π-type. In principle also a bonding between B-cations across the face of the cube has to be considered. Hence the following overlap integrals between neighbouring B-cations labelled 1, 2 and 3 (fig. 2) are possible:

$$\Delta\sigma_{cc} = \langle \Psi_{t2}\ \Psi_{t3} \rangle \quad (3)$$

$$\Delta\sigma_{cac} = \langle \Psi_{e1}\ \Psi_{e2} \rangle \quad (4)$$

$$\Delta\pi_{cac} = \langle \Psi_{t1}\ \Psi_{t2} \rangle \quad (5)$$

$\Delta\sigma_{cc}$ is the overlap integral between the t_{2g} orbitals between the cations 2 and 3 (the label cc is for cation-cation overlap). Since the distance across the face of the cube is 5 - 6 Å the contribution of $\Delta\sigma_{cc}$ is considered negligibly small. $\Delta\sigma_{cac}$ and $\Delta\pi_{cac}$ are the corresponding overlap integrals along the edge of the cube involving the covalent bonding with the anion. These integrals determine the behaviour of the d-electrons and if they are large enough, it is appropriate to construct collective electron orbitals or bands. On the other hand, if these overlap integrals are small, the d-electrons are localised on discrete cationic sites. Therefore it is possible to define a critical overlap integral that is proportional to a critical transfer energy b_c and to distinguish between systems with localised d-electrons and such with itinerant or "band" electrons.

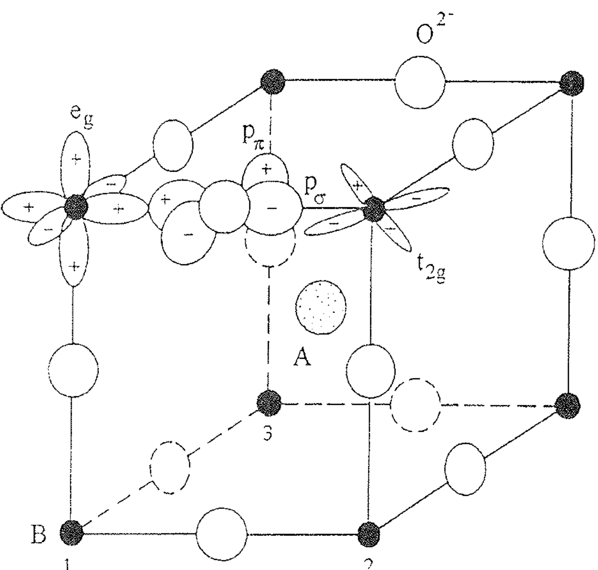


Fig. 2: Unit cell of a perovskite with electron orbitals. Overlap integrals can be distinguished as $\Delta\sigma_{cac}$, $\Delta\pi_{cac}$ (between cation 1 and 2 or 1 and 3) and $\Delta\sigma_{cc}$ (between cation 2 and 3).

As mentioned before, bc is related to the atomic number, the formal charge, the principal quantum number of the d-electrons and the total spin of the B-cation. Applied to the $LaBO_3$-series, with B from the first period of the transition metals (Ti^{3+}, V^{3+}, Cr^{3+}, Mn^{3+}, Fe^{3+}, Co^{3+}, Ni^{3+}) it turns out that the total spin determines the electron behaviour /9/. Figure 3 contains the data for the electrical resistivity ρ and the activation energy E_a for the conductivity of these $LaBO_3$ compounds. In $LaTiO_3$ and $LaNiO_3$ (Ni in the "low-spin" configuration) the spin of the transition metal ions S is equal to 1/2 resulting in itinerant electrons and metallic behaviour (low resistivity and low activation energy). Compounds with $S \geq 1$ for the B-cations, such as V^{3+}, Cr^{3+}, Mn^{3+} and Fe^{3+} are insulators with localised electrons (high resistivity and high activation energy). A special case is found with the compound $LaCoO_3$ where the temperature dependent population of "low-spin"- and "high-spin"-states causes a transformation from an insulator (or better semiconductor) to a metallic conductor around 1200 K /10, 11/.

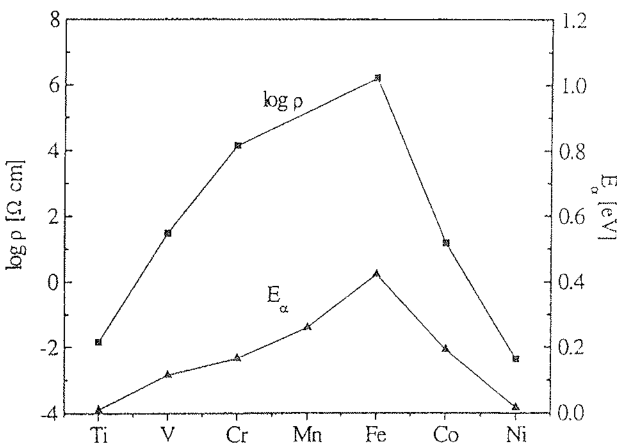


Fig. 3: Activation energy E_a and resistivity ρ at 300 K for $LaMeO_3$ compounds (from /9/).

The influence of the A-cation is demonstrated in the case of $LnTiO_3$ (Ln = La, Nd, Sm, Dy, Yb) in a work published by P. Ganguly et al. /9/. The electrical resistivities of these compounds are shown in figure 4. $LaTiO_3$ has the lowest resistivity with a weak temperature dependence according to its metallic behaviour. $NdTiO_3$ shows similar characteristics. In $SmTiO_3$ temperature dependence of the resistivity becomes pronounced but is comparable to thermal excitation energies of degenerate semiconductors. Thus it appears, that at least in the lighter rare-earth titanates exist itinerant d-electrons. With decreasing size of the rare-earth ion (Dy, Yb) a distinct increase of the resistivity is observed. This trend indicates narrowing of the d-band due to the decreasing overlap of the orbitals of the B-cation. As the electronic configuration of the Ti^{3+}-ion is $t_{2g}^1 e_g^0$, which means that only one electron occupies a t_{2g}-orbital, the bonding along Ti-O-Ti is π-type over the oxygen p-orbital. Such type of bonding would have competition from Ln-O bonding, which becomes favourable as the electron affinity of the Ln^{3+}-ion increases or its size decreases (both leads to a shorter bond length).

Measurement of the Seebeck-coefficient /9/ reveals, that $LaTiO_3$ is a p-type conductor. $LaNiO_3$ is reported to be a metallic oxide with n-type conduction /12, 13, 14/. It crystallises in a rhombohedrally distorted perovskite structure where the nickel ions (Ni^{3+}) are in the low spin configuration of $t_{2g}^6e_g^1$. According to a first approximation the conduction band is formed by the hybridisation of the e_g-orbitals of nickel and the oxygen p-orbitals. Since the t_{2g}-band is filled and the e_g electron takes place in forming the delocalised, quarter filled σ^*-band, the compound has no local components at the Ni^{3+} site and shows a temperature independent susceptibility (Pauli-paramagnetic behaviour). The Seebeck-coefficient of $LaNiO_3$ is small and negative (around -20 μV/K). Its magnitude increases linearly with temperature, thereby confirming the presence of a partially filled band /12/.

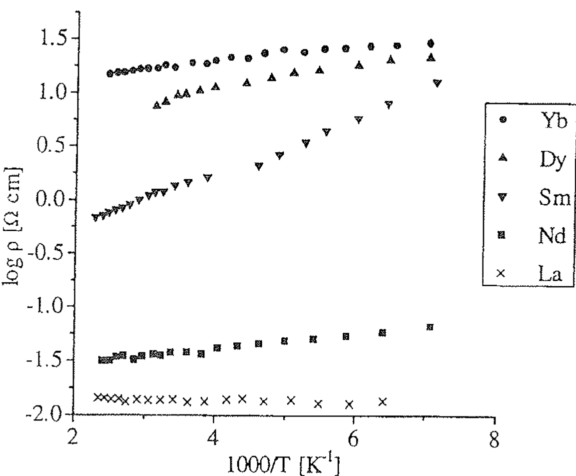


Fig. 4: Temperature dependence of the resistivity ρ of $LnTiO_3$ (from /9/).

In air $LaNiO_3$ decomposes above 860°C /15, 16/ emitting oxygen and NiO. There exists a series of intergrowth phases with the general formula $(LaO)(LaNiO_3)_n$ or $La_{n+1}Ni_nO_{3n+1}$. It can be understood as a phase with n perovskite layers followed by one LaO layer with rock salt structure. For n = 1 this will end up with the compound La_2NiO_4 (and NiO). La_2NiO_4 is a two-dimensional conductor with complex electrical behaviour /17/. To overcome the problem of decomposition the perovskite can be stabilised by doping with other transition metals such as Cr, Mn, Fe or Co. For each system $LaNi_{1-x}Me_xO_3$ there exists a critical composition or x_c, where the temperature coefficient of resistivity changes its sign. Thus x_c formally defines the concentration at which a metal-semiconductor transition takes place. The best stabilisation can be achieved with Co ($x_c \approx$ 0.35-0.5) /18, 19/. The compound $LaNi_{0.6}Co_{0.4}O_3$ can be sintered in air up to 1300 °C.

4. POLARONIC CONDUCTION IN PEROVSKITES

In a polar crystal the electron-lattice interaction in many cases is so strong that a band model is not applicable. The polarisation and the decrease of the overlap integrals leads to a narrowing of the band width. To a certain extent of the electron-lattice interaction the band model is still valid, only with a higher effective mass of the electron. With increasing electron-lattice interaction the band structure breaks down and one has to consider localised electrons. Electronic conductivity in such materials is still possible but the behaviour is fundamentally different from band conductors. The charge transport is described by the polaron model. A polaron is an electron or hole which polarises its surrounding and thus gets trapped at a lattice site in an energy minimum. Through interaction with phonons the polaron can overcome this energy barrier and move in an electric field to an appropriate neighbouring lattice site, where it will be localised again for a certain time. As a consequence the charge transport is thermally activated with a low but strongly temperature dependent mobility.

A simple model compound for polaronic conduction is NiO doped with lithium /20/. The Li^+ ions occupy nickel-sites giving rise to the formation of Ni^{3+}-ions. These Ni^{3+}-ions can be regarded as holes trapped by polarisation and surrounded by Ni^{2+}-ions. The number of charge carriers is determined by the lithium concentration. Activated by phonons an electron can hop from a neighbouring Ni^{2+} to the Ni^{3+}. Thus in first order the charge transport can be treated similar to the movement of an ion into a defect. The mobility μ and hence the conductivity σ exhibit an exponential temperature dependence:

$$\sigma = \sigma_0 \exp\left(\frac{E_A}{kT}\right) \qquad (6)$$

In this expression E_A is the activation energy necessary for the hopping over the energy barrier, k is the Boltzmann-factor, T the absolute temperature. The activation energy E_A usually lies in the region of 0.2 - 0.8 eV. The forefactor σ_0 is considered temperature dependent and contains a hopping probability, which usually is taken near one.

However at low temperatures (below the Debye temperature exactly spoken) the conductivity deviates intrinsically from this purely exponential characteristics and more sophisticated models have to be applied to explain the behaviour in this region. A detailed description of polaron transport is given by Appel /21/ or Austin and Mott /22/. Generally it can be said that polaronic charge transport occurs between neighbouring ions of the same species on crystallographically equivalent sites with a valence difference of one. The conductivity characteristics is determined by the temperature dependence of the mobility whereas the number of carriers in principle remains constant. The most common way to influence the number of carriers, i.e. the ration between Me^{n+} and $Me^{(n+1)+}$ is doping with heterovalent ions.

In the case of perovskite type materials, most of the compounds assigned as "insulators" or "semiconductors" exhibit polaronic conductivity, if one of the cations is able to posses different valence states. The development of electrode materials for solid oxide fuel cells has focused on perovskite type materials based on lanthanum as A-cation and Cr, Mn, Fe, Co as B-cations with various dopants added, because of their thermal stabil-

Informacije MIDEM 28(1998)4, str. 205-210

ity and good electrical conductivity at high temperatures. The same materials can be used for temperature sensors as well /23/. For this application a high temperature coefficient of resistivity and a suitable resistivity range is important. Depending on the application one is interested either in an increase or in a decrease of the electrical conductivity. This is achieved in most cases by doping either with heterovalent ions or aliovalent ions, the latter causing simply a dilution of carriers. Due to the high tolerance of the perovskite structure towards defects, the excess or deficiency of oxygen has a considerable impact on the carrier concentration as well. Thus the oxygen partial pressure during preparation and operation is an important parameter for the electrical characteristics. The consequences of all these aspects should be demonstrated in the following examples.

$LaCoO_3$ is known to be a p-type semiconductor between 200 K and 1210 K. The relatively high conductivity of this compound is found to be due to a disproportion of high spin and low spin Co^{3+} into Co^{4+} and low spin Co^{2+} /11/. Both species in a matrix of Co^{3+} act as polarons with an activation energy of 0.35 eV /24/. The p-type conductivity is explained by the higher mobility of the "holes" (i.e. the Co^{4+}).

Addition of strontium to $LaCoO_3$ will increase the conductivity. The Sr^{2+}-ions will substitute La^{3+}-ions on A-sites. For electroneutrality reasons Co^{4+}-ions are formed, which act as additional p-type carriers. The same effect will be caused by doping with Mg^{2+}-ions for example, which occupy B-sites. This electronic charge compensation however is limited to low dopant concentrations. As the valence of +4 of cobalt is rather unstable, also ionic charge compensation can occur by the formation of oxygen vacancies:

$$2\,Co^{\bullet}_{Co} + O_O \rightarrow V_O^{\bullet\bullet} + 2\,Co_{Co} + 1/2\,O_2 \qquad (7)$$

In the Kröger-Vink notation the $Co^{\bullet}_{Co}$ corresponds to the Co^{4+}-ion. It is eliminated by the formation of an oxygen vacancy. Thus ionic charge compensation does not contribute to the polaronic conduction and the conductivity (i.e. charge carrier concentration) exhibits a pronounced dependence on oxygen partial pressure. Contrary to $LaCoO_3$ is the behaviour of $LaMnO_3$. As the Mn^{4+}-ion is much more stable, this species already exists in undoped $LaMnO_3$ causing an oxygen excess. Even after doping with two-valent ions such as Sr^{2+}, an oxygen excess can be observed at high oxygen partial pressure /25, 26/. The excess oxygen is not found at interstitial sites but causes cation vacancies on A- and B-sites /27/.

For n-type conductivity $LaCoO_3$ has to be doped with ions with a valence of four. Examples are Th^{4+} (on A-sites) and Ti^{4+} (on B-sites). For low dopant concentrations the perovskite exhibits n-type conductivity, due to the formation of Co^{2+}. In the case of $LaCo_{1-x}Ti_xO_3$ the electronic charge compensation takes place up to $x \approx 0.2$, higher concentrations of titanium result in compounds with oxygen excess. The Seebeck coefficient however, indicating the conduction type, turns its sign already for $x \approx 0.1$. This unusual behaviour is due to the formation of Ti^{4+}-Co^{2+} clusters. In these clusters Co^{2+}-ions are bound and cannot act as donors for the polaronic conduction.

5. SUMMARY

Among perovskite type oxides electronic conduction, either as band-type or polaronic conduction, is frequently found. The differentiation between these mechanisms is done mainly by considerations about magnitude and temperature dependence of the conductivity and the charge carrier concentration. From the estimation of overlap integrals, which involves the atomic number, the formal charge, the principal quantum number of the d-electrons and the total spin of the B-cation, one can derive an approximate band-structure and roughly explain the electrical behaviour. Additional influences come from the crystal structure (ionic radii of A- and B-cation, superstructures, lattice distortions). That is why, despite of the availability of good commercial software for the calculation of band structures, the estimation and prediction of electric properties still needs a great deal of empirical assumptions and experimental efforts.

In many cases a band picture is not applicable, due to the more or less polar character of oxides. The polarisation causes a narrowing of the bands leading finally to a break down of the band structure, because of the uncertainty relation. In such a case the charge transport is described with a hopping process of an electron from a cation Me^{n+} to a cation $Me^{(n+1)+}$ over an energy barrier. Thus the conductivity is mainly influenced by the height of the energy barrier and the probability that the neighbouring cation is an appropriate one. For the great variety of semiconducting oxides the polaron model has turned out to be a good tool to explain the electrical behaviour over a wide range of temperature and conductivity values.

6. REFERENCES

/1/ M. Izuha, K. Abe, M. Koike, N. Fukushima, Solid State Ionics, 108, 99, 1998.

/2/ M. S. Hedge, K. M. Satyalakshmi, R. M. Mallya, M. Rajeswari, H. Zhang, J. Mat. Res., 9, 4, 898, 1994.

/3/ J. B. Goodenough, J. M. Longo, Crystallographic and Magnetic Properties of Perovskite and Perovskite-Related Compounds, Landolt-Börnstein New Series III/4a, Springer, Berlin, 1970.

/4/ L. Tejuca, J. Less Common Met., 146, 251, 1989.

/5/ V. M. Goldschmidt, Skr. Nor. Vidensk.-Akad. Oslo, 1, 8, 1926.

/6/ J. B. Goodenough, J. Appl. Phys., 37, 3, 1415, 1966.

/7/ J. B. Goodenough, Progress in Solid State Chemistry, 5, 145, 1971.

/8/ J. B. Goodenough, in Solid State Chemistry, (C. N. R. Rao ed), Dekker, New York, 1994.

/9/ P. Ganguly, Om Parkash, C. N. R. Rao, Phys. Status Solidi (a), 36, 669, 1976.

/10/ C. N. R. Rao, J. B. Goodenough, Phys. Rev., 155, 3, 932, 1967.

/11/ V. G. Bhide, D. S. Rajoria, G. Rama Rao, C. N. R. Rao, Phys. Rev. B, 6, 3, 1021, 1972.

/12/ P. Ganguly, C. N. R. Rao, Mat. Res. Bull., 8, 405, 1973.

/13/ K. P. Rajeev, G. B. Shivashankar, A. K. Raychaudhuri, Solid State Commun., 79, 7, 591, 1991.

/14/ K. Sreedhar, J. M. Honig, M. Darwin, M. McElfresh, P. M. Shand, J. Xu, B. C. Crooker, J. Spalek, Phys. Rev. B, 46, 10, 6382, 1992.

/15/ J. Drennan, C. P. Tavares, B. C. H. Steele, Mat. Res. Bull., 17, 621, 1982.

/16/ P. Odier, Y. Nigara, J. Coutures, M. Sayer, J. Solid State Chem., 56, 32 1985.

/17/ C. N. R. Rao, D. J. Buttrey, N. Otsuka, P. Ganguly, H. R. Harrison, C. J. Sandberg, J. M. Honig, J. Solid State Chem., 51, 266, 1984.

/18/ P. Ganguly, N. Y. Vasanthacharya, C. N. R. Rao, P. P. Edwards, J. Solid State Chem., 54, 400, 1984.

/19/ N. Katsarakis, O. Fruhwirth, W. Sitte, Proc. Fourth Euro Ceramics, 5, 89, 1995.

/20/ R. R. Heikes, W. D. Johnston, J. Chem. Phys., 26, 582, 1957.

/21/ J. Appel, Solid State Phys., 21, 193, 1968.

/22/ I. G. Austin, N. F. Mott, Adv. Phys., 18, 41, 1969.

/23/ A. Macher, K. Reichmann, O. Fruhwirth, K. Gatterer, G. W. Herzog, INFORMACIJE MIDEM, 26, 2, 79, 1996.

/24/ N. Ramadass, J. Gopalakrishnan, M. V. C. Sastri, J. Less Common Met., 65, 129, 1979.

/25/ J. Kuo, H. Anderson, D. Sparlin, J. Solid State Chem., 52-60, 83, 1989.

/26/ J. Palma, P. Duran, J. Jurado, C. Pascual, Proc. Second Euro Ceramics, 2, 251, 1991.

/27/ B. Tofield, W. Scott, J. Solid State Chem., 183, 10, 1974.

Klaus Reichmann,
Nikos Katsarakis,
Angelika Reichmann
Institute for Chemical Technology of Inorganic Materials
Graz University of Technology
Stremayrgasse 16/III, A-8010 Graz
e-mail: f537mac@mbox.tu-graz.ac.at

Prispelo (Arrived): 21.09.98　　*Sprejeto (Accepted): 16.11.98*

MODELS FOR CARRIER TRANSPORT IN THE BASE OF npn SiGe HBTs

Sasa Sokolić*, Slavko Amon
Faculty of Electrical Engineering, University of Ljubljana, Slovenia
*METRONIK, Ljubljana, Slovenia

INVITED PAPER
MIDEM´98 CONFERENCE
23.09.98 – 25.09.98, Rogaška Slatina, Slovenia

Keywords: semiconductors, HBT, Heterojunction Bipolar Transistors, carrier transport, npn bipolar transistors, Si-Ge transistors, carrier transport modeling, minority carriers, analytical modeling, numerical modeling, BGN, BandGap Narrowing, transistor bases, diffusion constants

Abstract: Based on recalculated experimental and theoretical data, a consistent set of models for minority carrier transport in p-type SiGe HBT base is presented. Models are valid in wide range of temperature, doping level and Ge content (77K<T<350K, $N_A<10^{20}cm^{-3}$, $x_{Ge}<0.2$) and are appropriate for advanced analytical and numerical modeling of SiGe HBTs.

Modeli za transport nosilcev v bazi npn SiGe heterospojnega transistorja

Ključne besede: polprevodniki, HBT transistorji bipolarni heterospojni, transport nosilcev nabojev, npn transistorji bipolarni, Si-Ge transistorji, modeliranje transporta nosilcev nabojev, nosilci minoritetni, modeliranje analitično, modeliranje numerično, BGN oženje pasu prepovedanega, baze transistorjev, konstante difuzijske

Povzetek: Delo predstavlja skupek modelov za transport manjšinskih nosilcev v p-bazi SiGe heterospojnega bipolarnega transistorja, določenih na osnovi ponovno preračunanih eksperimentalnih in teoretičnih podatkov. Modeli so uporabni v širokem intervalu temperatur, dopiranja in Ge vsebnosti (77K<T<350K, $N_A<10^{20}cm^{-3}$, $x_{Ge}<0.2$) ter so primerni za analitično in numerično modeliranje SiGe heterospojnih bipolarnih transistorjev.

1. INTRODUCTION

Improved performance of SiGe HBTs compared to Si BJTs is closely related to the effects in the SiGe base /1/. As a consequence of germanium and related compressive strain, several phenomena appear in the base, affecting carrier transport. The most important effect - bandgap narrowing (bgn) due to strain and alloying - results in an increased electron injection from the emitter to the base and, consequently, in an increased collector current. Graded germanium profile in the base introduces graded bandgap and, consequently, an accelerating built-in electric field in the base that improves high frequency characteristics of SiGe HBTs. Beside bandgap reduction, several other effects in the SiGe base (mobility enhancement etc.) influence the device characteristics /2-9/.

Due to considerable scattering of experimental and theoretical data on SiGe materials and devices found in the literature, making their direct application almost imposible, a rigorous analysis of data available is made. It is found that different authors use in their evaluations different values for constants and material parameters, different definitions for effects involved and different formulations of models (such as $D_{n,SiGe}$, $\mu_{n,SiGe}$, n_i^2, ΔG_{SiGe} etc.). All this caused large discrepancies of reported results, in spite of excelent experimental or theoretical work performed by several authors. Therefore, all experimental and theoretical data used in our work were recalculated with the unified definitions for involved constants, parameters and models. As will be seen in the following, close agreement between recalculated data from different authors was obtained, enabling use of those data for the derivation of improved model. Models derived are adequate in a wide range of temperature T, doping level N_A and Ge content x_{Ge} (77K < T < 350K , $N_A < 10^{20}$ cm^{-3}, $x_{Ge} < 0.2$).

2. SiGe HBT BASE OPERATION

To get a clear insight into the transistor base operation, classical Moll-Ross /10/ approach for the calculation of base minority current j_n and transit time τ_B was applied. Assumptions of this approach are:

- Ideal homogenous base (N_A = const, n_i^2 = const, D_n = const, etc.)
- Carrier transport correctly described by Drift-Diffusion model
- Recombinations in the base neglected (R_{Base}= 0 or j_{nBase} = const)
- Low Level Injection

Moll-Ross approach was generalised for the case of nonuniform doping and band gap grading by H. Kroemer /11/

$$j_n = \frac{q(\exp(qV_{BE}) - 1)}{\int_0^{W_b} \frac{N_A(x)dx}{(pn)_{SiGe} D_{n,SiGe}(x)}} \quad (1)$$

$$\tau_B = \int_0^{W_b} \left[(pn)_{SiGe}(z) \int_z^{W_b} \frac{N_A(x)dx}{(pn)_{SiGe}(x) D_{n,SiGe}(x)} \right] dz \quad (2)$$

As can be seen from (1) and (2), for adequate analytical studies of HBT base properties - similar conclusion is valid also for numerical modeling - accurate models for minority carrier diffusion constant $D_{n,SiGe}$ and $(pn)_{SiGe}$-product, in whole the range of interest ($77K < T < 350K$, $N_A < 10^{20}$ cm^{-3}, $x_{Ge} < 0.2$), must be provided! Derivation of these models is the main goal of our work and will be reviewed in the following.

3. MINORITY CARRIER DIFFUSION CONSTANT $D_{n,SiGe}$

In normal HBT operation, minority carriers are nondegenerated. Therefore classical Einstein relation is valid and minority carrier diffusion constant ($D_{n,SiGe}$) is easily calculated from minority carrier mobility ($D_{n,SiGe} = (kT/q)\ \mu_{n,SiGe}$).

Modeling of minority carrier mobility ($\mu_{n,SiGe}$) in the necessary range of temperature, doping and Ge content is based on two assumptions. First, we assume that the doping and temperature dependence of minor mobility in SiGe is equal to that in Si. This assumption is applied due to similar carrier scattering mechanisms on dopants and on phonons, both decreasing the mobility. In this case, for the determination of Si mobility, Klaassen´s unified mobility model /12/ can be used. Second, we assume that mobility enhancement in SiGe, due to strain and alloying, can be treated independently from the mobility doping and temperature dependence. In this case, for SiGe minor mobility enhancement, the model of Decoutere et al. /13/ is selected. Here, enhanced minority carrier mobility in SiGe compared to that in Si, in dependence of Ge content x_{Ge}, is described by a mobility enhancement factor $D_{Ge}(x_{Ge})$, reported in /13/ as D_{nrel}.

Therefore, model for minority electron mobility in p-type SiGe base is in our case given by the following equation, joining Klaassen´s and Decoutere´s model

$$\mu_{n,SiGe}(T,N_A,x_{Ge}) = \mu_{n,Si}(T,N_A)_{Klaassen/12/}\, D_{Ge}(x_{Ge})_{Decoutere/13/} \quad (3)$$

4. $(pn)_{SiGe}$ - PRODUCT

The $(pn)_{SiGe}$-product is a fundamental parameter for bipolar SiGe device modeling, influencing many device properties. Usually in modeling, thermal equilibrium minority carrier concentrations are calculated from pn-product for given majority carrier concentrations or doping.

Adequate model for $(pn)_{SiGe}$-product, performing well in the wide temperature, doping concentration and Ge content range which is defined by the operation of real SiGe HBTs, and at the same time being appropriate for efficient modeling, does not exist at present. Work on the derivation of $(pn)_{SiGe}$-product model, taking into account available recalculated experimental and theoretical data, is reviewed in the following.

To model $(pn)_{SiGe}$-product, it is convenient to introduce apparent bgn ΔG_{SiGe}. Throughout this work we will strictly use the following definition for apparent bgn /14/

$$(pn)_{SiGe} = n_{i,Si}^2 \exp\left(\frac{\Delta G_{SiGe}}{kT}\right) \quad (4)$$

Therefore, by definition (4), apparent bgn ΔG_{SiGe} is a measure for the deviation of the pn-product in SiGe, from its value in intrinsic silicon. For reference intrinsic carrier concentration in silicon ($n_{i,Si}$), the temperature dependent model suggested by Green /17/ was selected and will be used throughout this work.

5. APPARENT BAND GAP NARROWING ΔG_{SiGe}

An expression for apparent bgn ΔG_{SiGe}, derived by Sokolić et al. /15/, will be used throughout this work

$$\Delta G_{SiGe} = \left[\Delta E_{g,hd}\right] + \left[\Delta E_{g,Ge}\right] + \left[kT \ln\left(\frac{N_{C,SiGe} N_{V,SiGe}}{N_{C,Si,i} N_{V,Si,i}}\right)\right] + \left[kT \ln\left(\frac{N_A}{N_{V,SiGe}}\right) - kT G_{1/2}\left(\frac{N_A}{N_{V,SiGe}}\right)\right] \quad (5)$$

where N_C, N_V are effective densities of states in conduction and valence band, respectivelly, and $G_{1/2}$ is the inverse of the $F_{1/2}$ (Fermi-Dirac integral of order 1/2). As seen from eq. (5), apparent bgn ΔG_{SiGe} consists of four contributions:

1. Term $\Delta E_{g,hd}$ gives bgn due to high doping
2. Term $\Delta E_{g,Ge}$ gives bgn due to Ge induced strain and alloying
3. Term with $N_C N_V$ ratio gives bgn due to lower density of states in SiGe compared to that in intrinsic Si
4. Term with ln-$G_{1/2}$ difference gives bgn due to Fermi-Dirac statistics (degeneracy)

Eq. (5) leads to an important conclusion: for apparent bgn ΔG_{SiGe} and consequently $(pn)_{SiGe}$ determination, several phenomena ($\Delta E_{g,hd}$, $\Delta E_{g,Ge}$, $N_{C,SiGe}$, $N_{V,SiGe}$) as a function of doping, temperature and Ge content must be known! The determination of those models, based on available experimental and theoretical data, remains the main goal of this work.

5.1. Effective Density of States in Conduction Band $N_{C,SiGe}$

Due to Ge induced strain and alloying, conduction band in SiGe splits into 4-fold and 2-fold degenerated bands /9/:

$$N_{C,SiGe} = 2/3\ N_{C,Si} \qquad (6)$$

For low values of x_{Ge}, also upper 2-fold degenerated conduction band states contribute to electron concentration. The model proposed by Pejćinović et al. /16/ takes this smooth transition from Si to SiGe into account. As mentioned above, we assume that $N_{C,Si}$ is described as proposed by Green /17/.

5.2. Effective Density of States in Valence Band $N_{V,SiGe}$ and hole effective mass m_p^* (N_A,T,x_{Ge})

Effective density of states in valence band $N_{V,SiGe}$ can be determined from properly defined hole effective mass m_p^* /19/, taking into account the entire effect of nonparabolicity

$$N_{V,SiGe} = 2\ (\,2\pi\ m_p^*\ kT\ /\ h^2\,)^{3/2} \qquad (7)$$

Nevertheless, the problem of $N_{V,SiGe}$ determination remains unsolved because a closed form model for hole effective mass $m_p^*(N_A,T,x_{Ge})$ in the necessary range of temperature, doping and Ge content, and at the same time appropriate for device modeling, is not available. Existing sophisticated theoretical models are computer time consuming and difficult to be tuned with measurements – especially with transport data. Therefore, the derivation of appropriate model for hole effective mass $m_p^*(N_A,T,x_{Ge})$ is one of the major tasks in this work.

After recalculation of experimental and theoretical data found in the literature, and a critical study of different approaches to the effective mass derivation /18, 20/, a procedure for fast hole effective mass $m_p^*(N_A,T,x_{Ge})$ evaluation was proposed by Sokolić et al /25/. The procedure consists of the following steps:

1. Determination of hole effective mass for nondegenerated case $m_p^{*0}(T,x_{Ge})$
2. Determination of degeneracy transition temperature T_{deg}
3. Determination of doping dependent hole effective mass $m_p^*(N_A,x_{Ge})$ at specific low temperature
4. Construction of model for hole effective mass $m_p^*(N_A,T,x_{Ge})$. Graphic results of this model are presented in diagrams in Figs.1,2.

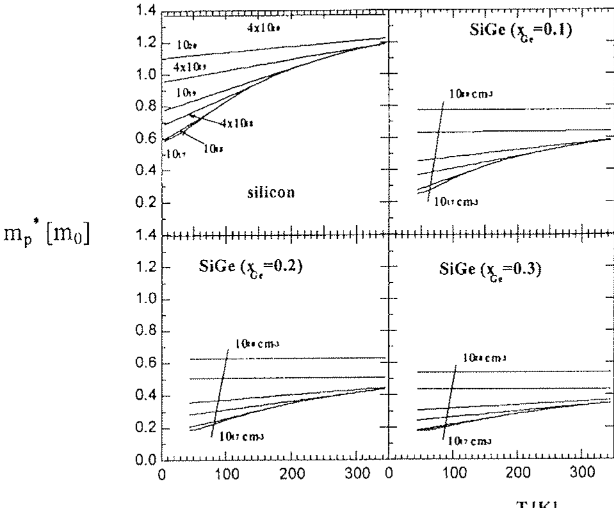


Fig.1. Calculated hole effective mass $m_p^*(N_A,T,x_{Ge})$ vs. temperature T

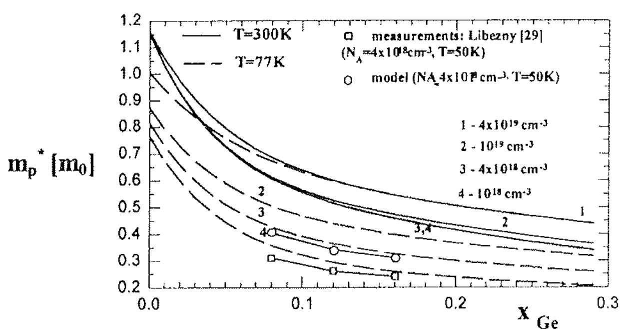


Fig. 2. Calculated hole effective mass $m_p^*(N_A,T,x_{Ge})$ vs. Ge content x_{Ge}. Experimental values for m_p^* from Libezny /29/ are shown as well.

5.3. Bandgap narrowing due to high doping $\Delta E_{g,hd}$

To determine bgn due to high doping $\Delta E_{g,hd}$, we follow a procedure proposed by Sokolić et al. /14/. The procedure is based on the following assumptions:

- in Si, we assume that $\Delta E_{g,hd}$ has a negligible temperature dependence and is only doping dependent. This assumption is generally accepted in the literature and is confirmed by both theoretical calculations of Thuselt /30/ and Jain /31/ and by experiments of Wagner /32/.
- in SiGe, we assume that $\Delta E_{g,hd}$ has negligible dependence on Ge content x_{Ge}, due to the same origin of the effect. This assumption is supported by work of Poortmans et al. /22/ and Souifi et al. /23/. Consequence of this assumption is that $\Delta E_{g,hd}$ in SiGe and in Si are equal!

Determination of bgn due to high doping $\Delta E_{g,hd}$ is based on recalculated experimental data for apparent bgn in p-type Si, obtained from measurements of I_C characteristics in Si BJTs. To enable the inclusion of the results from different authors, all experimental data had to be recalculated for the same mobility model, taken from Klaassen /12/, and for the same intrinsic Si concentration model $n_{i,Si}(T)$, taken from Green /17/. In particular, using the same procedure as proposed in Klaassen /33/, we recalculated the data for p-type Si

from Klaassen /33/ (including data from several authors) for $n_{i,Si}$ at 300K (1.08 10^{10} cm^{-3}) and the temperature dependence of intrinsic N_CN_V product ($CT^{3.43}$). In addition to $CT^{3.43}$ recalculation, the data from Poortmans et al /22/ were recalculated also for the mobility from Klaassen /12/. $\Delta E_{g,hd}$ was then evaluated from those recalculated ΔG_{Si} data by means of eq. (5), noting that in silicon $\Delta E_{g,Ge}$ = 0, and that other terms can be calculated with models described above.

The final result of this procedure, bgn due to high doping ($\Delta E_{g,hd}$) vs. doping, is shown in Fig.3. It can be observed in Fig.3 that after recalculation, the experimental values from different authors are in agreement. For the purpose of analytical and numerical modeling, best fit approximation (solid line in Fig.3) was determined /14/

$$\Delta E_{g,hd} = ((a\,N_A^{c})^{-4} + (b\,N_A^{d})^{-4})^{-4} \quad [eV] \qquad (8)$$

where a = 6.76x10^{-11}, b = 3.58x10^{-7}, c = 0.5, d = 0.28 and N_A [cm^{-3}]

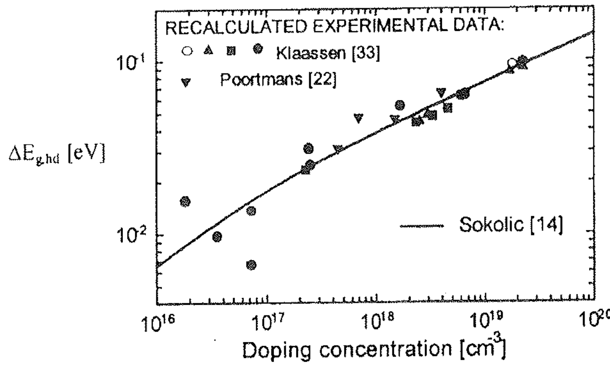


Fig. 3. Bgn due to high doping $\Delta E_{g,hd}$ vs. doping

5.4. Bandgap narrowing due to Ge induced strain and alloying $\Delta E_{g,Ge}$

To determine bgn due to Ge strain and alloying $\Delta E_{g,Ge}$, we follow a procedure proposed by Sokolić et al. /14/. Determination of $\Delta E_{g,Ge}$ is based on recalculated experimental data for apparent bgn in SiGe (ΔG_{SiGe}) and various measured effective bandgap narrowing data, obtained from measurements of I_C characteristics in SiGe BJTs. To enable inclusion and the analysis of the experimental results from different authors, all the data involved had to be recalculated for the same mobility model, taken from Klaassen /12/, for the same Ge dependence of mobility, taken from Decoutere /13/, for the same temperature dependence of N_CN_V - for intrinsic Si taken from Green /17/ and in doped Si and SiGe based on the derivations above -, for E_g in intrinsic Si as suggested by Green /17/ and for the definition of apparent bgn ΔG_{SiGe} adopted in this work, eq. (5). As a final result, bgn due to Ge induced strain and alloying $\Delta E_{g,Ge}$ is evaluated from recalculated experimental data for apparent bgn ΔG_{SiGe}, for different values of T, N_A, x_{Ge} by means of eq. (5). Note that in eq. (5), $\Delta E_{g,Ge}$ is now to be determined, ΔG_{SiGe} is measured, and other terms are calculated with models derived previously.

$\Delta E_{g,Ge}$ vs. x_{Ge} data, obtained from recalculation procedures described above, are shown in Fig.4. Recalculated data exhibit clear dependence on Ge content and almost no dependence on doping (this is not the case with row, nonrecalculated data!). It is worth mentioning that recalculated $\Delta E_{g,Ge}$ vs. x_{Ge} data points are in good agreement also with models from Bean /9/ and Robins /42/, obtained from absorbtion and photoluminescence, respectively.

All these observations lead to a conclusion that: 1. Modeling of apparent bandgap narrowing described in this work was appropriate, and 2. Recalculations of the experimental data were done correctly. In other words, we can conclude that temperature and doping dependence of effects involved were taken into account correctly with the models for m_p* (N_A, T, x_{Ge}) and $\Delta E_{g,hd}(N_A)$ derived above.

For the purposes of analytical and numerical modeling, best fit approximation (solid curve in Fig. 4) was determined, based on recalculated $\Delta E_{g,Ge}$ values /14/

$$\Delta E_{g,Ge} = a\,x_{Ge} - b\,x_{Ge}^2 \quad [eV] \qquad (9)$$

where a = 0.937 , b = 0.5 and x_{Ge} [%Ge / 100]

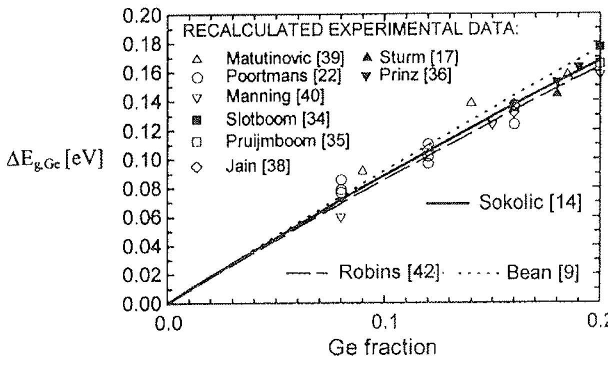


Fig. 4. Bgn due to Ge induced strain and alloying $\Delta E_{g,Ge}$ vs. Ge content x_{Ge}

5.5. Apparent bandgap narrowing ΔG_{SiGe}

With models for m_p* (N_A, T, x_{Ge}), $\Delta E_{g,hd}(N_A)$ and $\Delta E_{g,Ge}(x_{Ge})$ derived in previous sections, apparent bgn ΔG_{SiGe} can be calculated for arbitrary N_A, T and x_{Ge} by means of eq. (5). The result of this calculation, ΔG_{SiGe} vs. doping N_A, temperature T and Ge content x_{Ge}, is shown in Fig. 5.

It can be seen in Fig. 5 that ΔG_{SiGe} increases with doping and Ge content. It can also be observed that ΔG_{SiGe} increases at low temperatures for higher Ge contents, that is due to lower influence of N_CN_V ratio at low temperatures. On the other hand, degeneracy is more pronounced at low temperatures, resulting in lower ΔG_{SiGe} at low temperatures and high doping levels. In Si, in agreement with experiments, apparent bgn ΔG_{Si} is temperature independent.

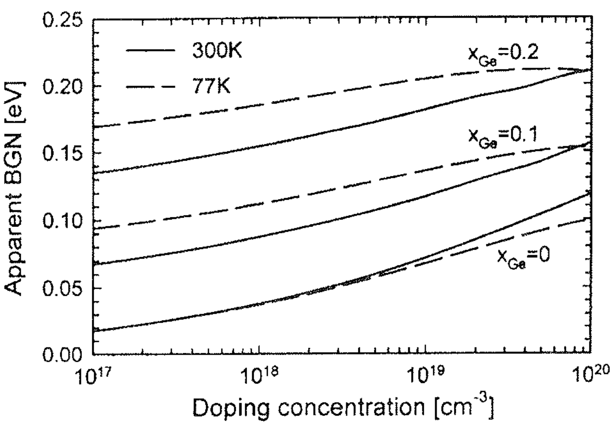


Fig. 5. Apparent bgn ΔG_{SiGe} vs. doping N_A, temperature T and Ge content x_{Ge}

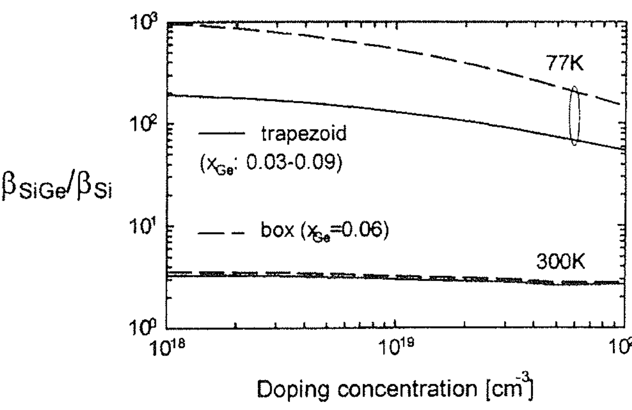


Fig. 6. Current gain ratio (β_{SiGe} / β_{Si}) vs. doping N_A

To conclude, we should not forget that all ΔG_{SiGe} curves are obtained indirectly, by considering available Si BJT and SiGe HBT measurements and can therefore, to some extent, be treated as empirical. Moreover, models for m_p^* (N_A, T, x_{Ge}), $\Delta E_{g,hd}(N_A)$, $\Delta E_{g,Ge}(x_{Ge})$ represent a consistent set of models based on available theoretical and experimental data, which determines ΔG_{SiGe} in a wide range of temperatures, doping levels and Ge content (77K<T<350K, $N_A<10^{20}$ cm^{-3}, x_{Ge}<0.2). It should be reminded that the entire analysis is based on $n_{i,Si}$ and $N_{C,Si}$ models suggested by Green /17/, mobility model proposed by Klaassen /12/ and Ge induced mobility enhancement according to Decoutere /13/. Finally, a Fortran or C+ subroutine based on derived models for fast calculation of hole effective mass, appropriate for numerical simulators, was concieved /28/ and is free available on Internet (http://pollux.fe.uni-lj.si/lee1).

6. APPLICATION OF DERIVED MODELS IN SiGe HBT ANALYSIS

To controll their correctness, derived models were applied in SiGe HBTs. HBT analysis is in this case based on an analytical approach (reviewed in Chapter 2). npn SiGe HBTs were studied for two Ge profiles in the SiGe base: box Ge profile /x_{Ge}=const = 6% / and trapezoid Ge profile / x_{Ge} = 3% - 9% /. SiGe HBT calculations were compared to calculations on equivalent Si bipolar junction transistor (BJT), having the same structure as HBT but no Ge. Analysis was performed at two temperatures, at room temperature (300K) and at low temperature (77K). Several basic HBT properties were studied such as current gain, base transit time, influence of Fermi-Dirac statistics etc.

6.1. Current gain

Analysis of current gain β was based on equations and models described previously in this work. Calculated current gain β for different doping and Ge profiles at 300K and 77K is shown in Fig. 6. In agreement with experimental data from the literature, it can be observed in Fig. 6 that HBT has always higher current gain β than Si BJT, due to Ge induced bandgap narrowing in the SiGe base. It can also be observed in Fig. 6 that box Ge profile results in higher β than trapezoidal Ge profile, due to higher bandgap narrowing and consequently minority carrier concentration at the base side of emitter-base depletion layer. It can be seen as well that β ratio decreases with doping. Due to the lower hole effective mass m_p^* in SiGe, Fermi-Dirac statistics becomes more influent, and apparent bgn difference (ΔG_{SiGe} - ΔG_{Si}) decreases with doping. Effect is stronger at low temperatures.

6.2. Base transit time

Analysis of base transit time τ is based on equations and models described previously in this work. Result of these calculations is shown in Fig. 7. It can be observed in Fig. 7 that, compared to equivalent Si BJT, box Ge profile results in slight decrease of transit time, due to increased minor electron mobility in SiGe. On the contrary, trapezoidal Ge profile results in a strong decrease of transit time, due to accelerating built-in electric field as a consequence of graded SiGe base. It can be observed also that transit time improvement (lowering) is smaller at high doping, due to the influence of Fermi-Dirac statistics which decreases effective Ge grading and consequently decreases accelerating electric field in the base.

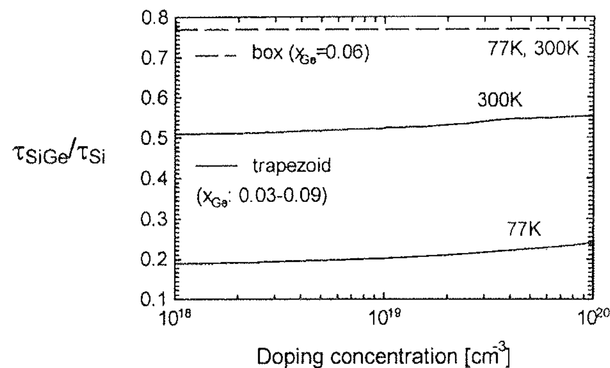
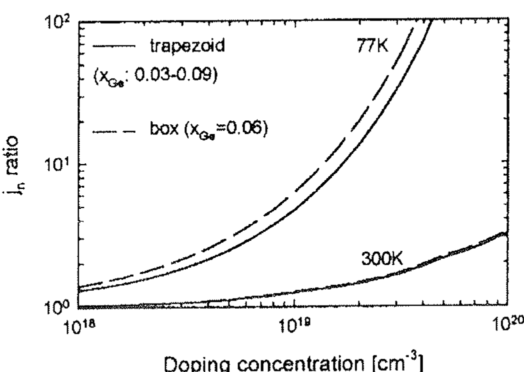


Fig. 7. Base transit time ratio (τ_{SiGe} / τ_{Si}) vs. doping N_A

6.3. Influence of Fermi-Dirac statistics

The influence of Fermi-Dirac statistics on the operation of SiGe HBT was analysed recently /24/ and recognised to be of great importance in these devices. In SiGe HBT base, greater influence of Fermi-Dirac statistics is expected than in Si BJT for several reasons - due to lower hole effective mass in SiGe, possible low temperature operation of SiGe HBT and possible high doping in SiGe base. Fermi-Dirac statistics influences minority carrier transport basicaly through two effects: major effect is Fermi level shift lowering minority electron current (4th term in expression for apparent bgn ΔG_{SiGe}, eq.(5)), and minor effect is the increase of m_p^* (through 3rd term in (5)), attenuating Fermi level shift.

Analysis of the influence of Fermi-Dirac statistics on SiGe HBT performance presented in this work was based on equations and models described previously in this work. Result of these calculations, minority carrier current density and base transit time ratios (Fermi-Dirac vs. Boltzmann) are shown in Fig.8. It can be seen from Fig.8 that at 300K Fermi-Dirac statistics is important for doping concentrations higher than 10^{19} cm^{-3}. At low temperatures (77K), Fermi Dirac statistics influences the device properties significantly and should be taken into account as soon as doping concentration in the base extends 10^{18} cm^{-3}. It can be concluded that due to the high doping in SiGe HBT base, Fermi-Dirac statistics should be applied for the majority of cases. On the contrary, the application of Fermi-Dirac statistics in Si BJTs - which are not well suited for low temperature operations - is important only for the highly doped emitter regions, and therefore does not affect base transport properties.



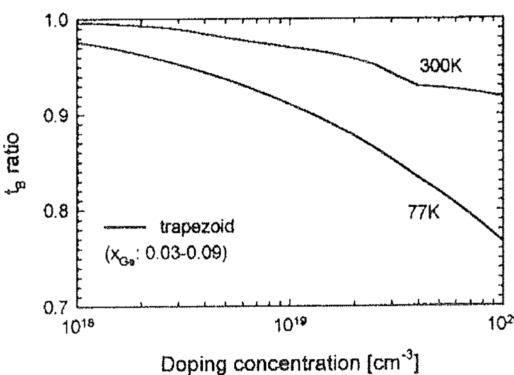


Fig. 8. Current and transit time ratio (Fermi-Dirac / Boltzmann) vs. doping N_A

CONCLUSION

A set of models for SiGe HBT carrier transport, based on criticaly and consistently recalculated experimental and theoretical data, was derived and is reviewed. Proposed set of models accounts for important effects in SiGe base such as BGN due to high doping as well as due to strain and alloying (Ge), distortion of density of states and Fermi-Dirac statistics. Proposed models are adequate for advanced analytical and numerical modeling of SiGe HBTs. A Fortran or C+ subroutine for fast calculation of hole effective mass, appropriate for numerical simulators, is free available on Internet (http://pollux.fe.uni-lj.si/lee1). Validity range of derived models is

$$77K < T < 350K, \ N_A < 10^{20} \text{ cm}^{-3}, \ x_{Ge} < 0.2$$

REFERENCES

/1/ D.L. Harame, J.H. Comfort, J.D. Cressler, E.F. Crabbé, J.Y.-C. Sun, B.S. Meyerson and T. Tice, IEEE Trans. Electron Devices, 42, 455 (1995), and references therein.

/2/ D.L. Harame, J.H. Comfort, J.D. Cressler, E.F. Crabbé, J.Y.-C. Sun, B.S. Meyerson and T. Tice, IEEE Trans. Electron Devices, 42, 469 (1995), and references therein.

/3/ A. Gruhle, H. Kibbel, U. König, U. Erben and E. Kasper, IEEE Electron Dev. Lett., 13, 206 (1992).

/4/ D.L. Harame, E.F. Crabbé, J.D. Cressler, J.H. Comfort, J.Y.-C.Sun, S.R.Stiffer, E.Kobeda, J.N. Burghartz, M.M. Gilbert, J.C. Malinowski and A.J. Dally, IEDM Tech. Dig., 19 (1992).

/5/ J.D. Cressler, J.H. Comfort, E.F. Crabbé, G.L. Patton, J.M.C. Stork, J.Y.-C.Sun and B.S. Meyerson, IEEE Trans. Electron Devices, 40, 525 (1993).

/6/ J.D. Cressler, J. Phys. IV, 4, C6-101 (1994).

/7/ J.D. Cressler, in Proc. of the 1995 ECS Symp. on Low Temperature Electronics and High Temperature Superconductivity, eds. C.L. Claeys, S.I. Raider, R.K.Kirschman and W.D. Brown, Electrochemical Soc. Proc. 95-9, 159 (1995).

/8/ J.D. Cressler, E.F. Crabbé, J.H. Comfort, J.Y.-C. Sun and J.M.C. Stork, IEEE Electron Dev. Lett., 15, 472 (1994).

/9/ J.C. Bean, Proc. IEEE, 80, 571 (1992).

/10/ J.L.Moll, I.M.Ross, Proc.IRE, 44, 72 (1956)

/11/ H. Kroemer, Solid-State Electron., 28, 1101 (1985)/

/12/ D.B.M. Klaassen, Solid-State Electron., 35, 953 (1992); and 35, 961 (1992)

/13/ S. Decoutere, J. Poortmans, L. Deferm and J. Nijs, SSE 38, 157 (1995)

/14/ S. Sokolić and S. Amon, in Proc. ESSDERC´96, 657 (1996) /

/15/ S. Sokolić and S. Amon, Informacije MIDEM, 26, 161 (1996).

/16/ B. Pejćinović, L.E. Kay, T.-W. Tang and D.H. Navon, IEEE ED 36,2129 (1989).

/17/ M.A. Green, J. Appl. Phys., 67, 2944 (1990).

/18/ T. Manku and A. Nathan, J. Appl. Phys., 69, 8414 (1991).

/19/ F. L. Madarasz, J. E. Lang and P. M. Hemeger, J. Appl. Phys., 52, 4646 (1981).

/20/ Y. Fu, S.C. Jain, M. Willander and J.J. Loferski, J. Appl. Phys., 74, 402 (1993).

/21/ J. Wagner, Solid-St. Electron., 28, 25 (1985).

/22/ J. Poortmans, S.C. Jain, D.H.J. Totterdell, M. Caymax, J. Nijs, R. Mertens and R.VanOverstraeten, Solid-State Electron., 36, 1763 (1993).

/23/ A. Souifi, G. Brémond, T. Benyattou and G. Guillot, Appl.Phys.Lett.,62, 2986 (1993).

/24/ S. Sokolić and S. Amon, "Influence of Fermi-Dirac Statistics on Collector Current of npn SiGe HBT at Low Temperatures", J. Phys. IV, Vol.6, C3, pp.131-136, (1996).

/25/ A. Sokolić and S. Amon, "Temperature Dependent Model for Hole Effective Massin Heavily Doped p-type SiGe", J. Phys. IV, Vol.6, C3, pp.137-142, (1996).

/26/ C. E. Lang , F. L. Madarasz and P. M. Hemeger, J. Appl. Phys., 54, 3612 (1981).

/27/ Y. Fu, K. J. Grahn, and M. Willander, "Valence Band Structure of Ge_xSi_{1-x} for Hole Transport Calculations", IEEE Trans. Electron Dev., Vol. 41, No. 1, pp. 26-31, 1994 (Remarque: expressions for density of states in SiGe given in this work were found incorrect - Y. Fu has given us correct expressions in a private correspondence)

/28/ S. Sokolić, B.Ferk and S. Amon, "SiGe HBT simulation based on m_p*(T,N_A,x_{GE}) numerical model HEM", J. Phys. IV, Vol.8, Pr3, pp.117-120 (1998).

/29/ M. Líbezný, S. C. Jain, J. Poortmans, M. Caymax, J. Nijs, R. Mertens, K. Werner, and P. Balk, "Photoluminescence determination of the Fermi energy in heavily doped strained $Si_{1-x}Ge_x$ layers", Appl. Phys. Lett., Vol. 64, No. 15, pp. 1953-1955, 1994.

/30/ F. Thuselt, and M. Rösler, "Gap Shift in Doped Semiconductors at Finite Temperatures", Phys. Stat. Sol. (b), Vol. 130, pp. 661-673, 1985.

/31/ S. C. Jain, and D. J. Roulston, "A Simple Expression for Band Gap Narrowing (BGN) in Heavily Doped Si, Ge, GaAs and Ge_xSi_{1-x} Strained Layers", SSE, V34, No.5., pp. 453-465, 1991.

/32/ J. Wagner, and J. A. del Alamo, "Band-gap narrowing in heavily doped silicon: A comparison of optical and electrical data", J. Appl. Phys., Vol. 63, No. 2, pp. 425-429, 1988.

/33/ D. B. M. Klaassen, J. W. Slotboom, and H. C. de Graaff, "Unified Apparent Bandgap Narrowing in n- and p-Type Silicon", Solid-St. Electron., Vol. 35, No. 2, pp.125-129, 1992.

/34/ J. W. Slotboom, G. Streutker, A. Pruijmboom, and D. J. Gravesteijn, "Parasitic Energy Barriers in SiGe HBT´s", IEEE Electron Dev. Lett., Vol. 12, No. 9, pp. 486-488, 1991 .

/35/ A. Pruijmboom, J. W. Slotboom, D. J. Gravesteijn, C. W. Fredriksz, A. A. van Gorkum, R. A. van de Heuvel, J. M. L. van Rooij-Mulder, G. Streutker, and G. F. A. van de Walle, "Heterojunction Bipolar Transistors with SiGe Base Grown by Molecular Beam Epitaxy", IEEE Electron Dev. Lett., Vol. 12, No. 7, pp. 357-359, 1991.

/36/ E. J. Prinz, P. M. Garone, P. V. Schwartz, X. Xiao, and J. C. Sturm, "The Effect of Base-Emitter Spacers and Strain-Dependent Densities of States in $Si/Si_{1-x}Ge_x/Si$ Heterojunction Bipolar Transistors", IEDM Tech. Dig., pp. 639-642, 1989.

/37/ J. C. Sturm, E. J. Prinz, P. M. Garone, and P. V Schwartz., "Band-gap shifts in silicon-germanium heterojunction bipolar transistors", Appl. Phys. Lett., Vol. 54, No. 26, pp. 2707-2709, 1989.

/38/ S. C. Jain, J. Poortmans, S. S. Iyer, J. J. Loferski, J. Nijs, R. Mertens, and R. Van Overstraeten, "Electrical and Optical Bandgaps of Ge_xSi_{1-x} Strained Layers", IEEE Trans. Electron Dev., Vol. 40, No. 12, pp. 2338-2343, 1993.

/39/ Z. Matutinović-Krstelj, "Base Doping Effects and Design of Si/SiGe/Si Heterojunction Bipolar Transistors", Dissertation, Princeton University, 1994.

/40/ B. M. Manning, C. J. Peters, N. G. Tarr, J.-P. Noel, and D. C. Houghton, "Effect of heavy doping on band gap in SiGe base regions", J. Vac. Sci. Technol. B, Vol. 11, No. 3, pp. 1190-1192, 1993.

/41/ J. W. Slotboom, and H. C. de Graaff, "Measurements of Bandgap Narrowing in Si Bipolar Transistors", Solid-St. Electron, Vol. 19, pp. 857-862, 1976.

/42/ J. Robins, L. T. Canham, S. J. Barnett, A. D. Pitt, and P. Calcott, "Near-band-gap photoluminiscence from pseudomorfic $Si_{1-x}Ge_x$ single layers on silicon", J. Appl. Phys., Vol. 71, No. 3, pp. 1407-1414, 1992.

Sasa Sokolić, Slavko Amon*
Faculty of Electrical Engineering,
University of Ljubljana
Tržaska 25, 1000 Ljubljana, Slovenia
**METRONIK*
Stegne 21, 1000 Ljubljana, Slovenia
email: slavko.amon@fe.uni-lj.si

Prispelo (Arrived): 21.9.1998 *Sprejeto (Accepted): 16.11.1998*

 UDK621.3:(53+54+621+66), ISSN0352-9045

ALCATEL MICROELECTRONICS 0.5 μm Mixed CMOS Technology

Hans Gugg-Schwaiger
Alcatel Microelectronics, München, Germany

INVITED PAPER
MIDEM´98 CONFERENCE
23.09.98 – 25.09.98, Rogaška Slatina, Slovenia

Keywords: semiconductors, microelectronics, mixed 0.5 μm CMOS technologies, mixed 0.35 μm CMOS technologies, ADS, ASIC Design System, Application Specific Integrated Circuit, Design System, design for quality

Abstract: The features of the submicron silicon 0.5 μm mixed CMOS technology are described. Process options, process parameters & design rules, cross-section and DOC-references are shown. Achieved Quality levels and design for Quality are discussed briefly. The ADS Asic Design System is described. Finally the CMOS roadmap and 0.35μm mixed CMOS technology are briefly described.

Mešana CMOS tehnologija firme Alcatel Microelectronics z minimalno razsežnostjo 0.5μm

Ključne besede: polprevodniki, mikroelektronika, CMOS tehnologije mešane 0,5 μm, CMOS tehnologije mešane 0,35 μm, ADS ASIC sistem snovanja za vezja integrirana za aplikacije specifične, snovanje za kakovost

Povzetek: V prispevku opisujem osnovne značilnosti mešane CMOS tehnologije z minimalno razsežnostjo 0.5μm. Prikažem procesne možnosti, procesne parametre, načrtovalska pravila, preseke in ustrezno dokumentacijo. Na kratko se dotaknem koncepta vgrajene zanesljivosti in pokažem dosežen nivo kvalitete. Opišem tudi ADS – sistem za načrtovanje ASIC vezij. Na koncu podam možne poti razvoja v bodočnosti in na kratko obravnavam novo mešano CMOS tehnologijo z minimalno razsežnostjo 0.35 μm.

1 INTRODUCTION

Combining the power of a 32bit RISC processor, with its on-board program, VHDL-described hardware and the analog front-end to communicate with analog signals to the external world is the every-day-work for the design community at Alcatel Microelectronics. This type of architectural construction is possible on a single chip thanks to the digital density and the analog capabilities offered by the described half-micron CMOS process.

Applications that have taken advantage of this integration capability are numerous. From integrated toll payment module for cars to low power integrated hearing aids and advanced chip-sets for GSM using the unique zero IF technique.

Speaking about the Application Specific Standard Products (ASSP), the same technology is used to develop the Asymmetrical Digital Subscriber Line (ADSL) chip set, the integrated Power Line Carrier (PLC) modem and the Integrated Services Digital Network (ISDN) product series. Alcatel Microelectronics has made the mixed mode communication chips his niche-flagship.

This breakthrough is the result of a strong revolution within the company. The technological development carried out in the last 5 years has allowed Alcatel Microelectronics to be able to switch its main production to the sub half-micron mixed mode CMOS technology. The company succeeded to bring its digital design methodologies and technology capabilities to the level of expertise recognised for the analog design.

The developed methodologies have been put into the Alcatel Microelectronics EDA system "ADS" (Asic Design System). In parallel the clear strategy for the re-use of value added blocks has been put in place as well as a continued improvement of the product quality.

2 0.5 μm Mixed CMOS Technology

Alcatel Microelectronics started 5 years ago with his first sub-micron mixed mode 0.7 μ CMOS technology. This technology was based on the 1.2 μm generation. Two years after, the new generation 0.5u CMOS was presented to the market. This new generation is characterised by an impressive list of features.

2.1 Digital 0.5 μm CMOS base technology

The efficiency for digital circuitry is obtained by providing self aligned Poly-gate CMOS transistor with size (L and W) down to 0.5 μm. The routing density is made very good by the use of triple metal layers and by the use of stackable vias and contacts. This last feature allows to contact the drain of a CMOS transistor to the highest metal by consuming only the size of one contact. The triple metal allows also to route over the cell, this virtually avoids the need for channel routing. Routing density better than 80% is possible. (see fig. 1, 2, 3)

C05 General Characteristics

Voltage Supply	2.0 V to 3.6 V, 5 V compliant I/O's
Base wafer	6" epi wafers
Dynamic characteristics	
typical gate delay	102 ps
power consumption	0.9μW/Gate/MHz at 3V
ring oscillator delay	104 to 111 ps/Stage
Protection	
latch up resistance	>±200mA
ESD protection	> ±2000V

Fig.1: C05 General Characteristics

Base process features

	self aligned twin tub N & P Poly Gates
	stackable contacts and vias
	digital & analog NMOS & PMOS transistors
	3V operation / 5V compliant I/O's

Fig.2: C05 Base process features

C05 basic design rules

number of masks: C05D	15
metal interconnect / Poly layers	3M / 1P
Layout rules	
transistor min. width & length	0.5 μm
analog transistors	0.8 μm
Poly line pitch	1.3 μm
Metal 1 pitch	1.6 μm
Metal 2 pitch	1.9 μm
Metal 3 pitch	2.5 μm

Fig.3: C05 basic design rules

2.2 Analog modules of the 0.5 μm CMOS technology

The analog module consists of precision capacitance and resistance. The analog capacitance is build with 2 Poly layers placed on the field oxide. This construction provides a precision capacitance that features a 1.1nF/mm^2 and a voltage non-linearity better than 30ppm/V. The resistance is a high ohmic (HIPO) type. Its sheet resistance is higher than the 1kOhm.

The analog characteristics of the CMOS transistors shows well controlled threshold voltage under the 0.69V in worst case conditions. The thermal noise is limited to 1e-29 V/sqrt(Hz). In addition to the CMOS, capacitance and resistance characteristics, the documentation provided by Alcatel Microelectronics contains characteristics of the junction capacitance, interconnect capacitance, matching data for CMOS transistors, resistances and capacitances. (see fig. 4, 5, 6)

Analog options C05A

number of masks: C05A	18
metal interconnect / Poly layers	3M / 2P
second Poly layer, capacitor	Poly1-Poly2 linear capacitor, 1.1nF/mm2, tol ±10%, Vcl <20ppm/V, Vcq <-10ppm/V, Matching <0.1% (3 sigma) @W/L = 20/20
high-ohmic Poly resistor	1kΩ/sq tol ±10%, voltage linearity: Vcl < 200 ppm/V, temperature coefficient: Tcl < -1500 ppm/°C, matching <0.35% (3 sigma) @W/L = 10/100
bipolar transistor	vertical PNP

Fig.4: C05 Analog options

2.3 Design for reliability

In order to get ultimate quality in production without screening, Iddq and Vscreen testing are implemented in all the designs.

Definitions:

Iddq: Test of Idd leakage current @Vdd_nom & all bias off
Vscreen: Some real testpattern, e.g. ScanPath @ 1.4xVdd_max

These two methods improve the quality and reliability of the IC´s drastically. In order to be able to do the above tests, the IC has to be designed already covering Iddq, which needs some skills especially in analog (e.g. switching off a reference voltage resistor divider, but don´t degrade the matching).

C05 electrical characteristics (worst case)

	NMOS	PMOS	unit
Oxide Tickness	10	10	nm
Threshold Voltage	0.69	-0.66	V
Beta lin	2480	600	$\mu A/V^2$
Noise (Kf)	3E-28	1E-29	V/sqrt(Hz)
Leakage current	1	1	$pA/\mu m^2$
f_T	15	15	GHz
Bipolar transistor		**vertical PNP**, collector to substrate, typical	
Vbe:		0.680	V
Tcl_Vbe		-1.97	mV/K
Hfe		8	
Vearly		170	V
Area		6.76	μm^2

Fig.5: C05 electrical characteristics

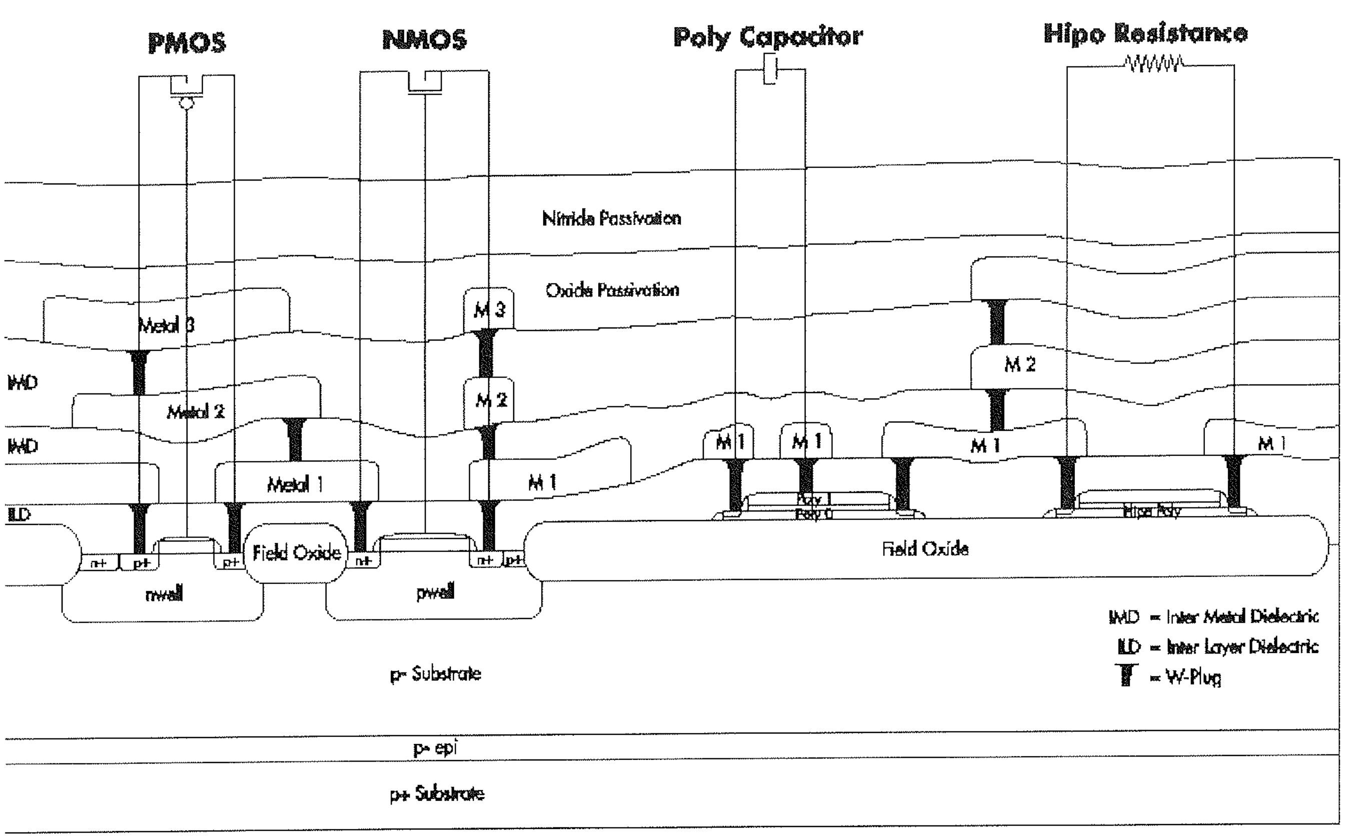


Fig. 6 C05A Cross Section

 Informacije MIDEM 28(1998)4, str. 218-222

Two other techniques are the well known ATPG and the use of JTAG, Boundary Scan.

Finally reliability data are provided in the documents to determine the expected live time of circuits stressed under extreme conditions. This allows the designer to anticipate design tuning to maximise the life-time.

2.4 C05 Libraries & Document reference

C05 Libraries

core digital library (Doc)	MTC 35000
high profile IO (Doc)	MTC 35100
low profile IO (Doc)	MTC 35200
5V safe IO (Doc)	MTC 35300
medium profile IO (Doc)	MTC 35400
ROM RAM compilers (Doc)	MTC 35500
functional blocks (CD ROM)	MTC 8332: 32bit RISK, MTC 8308: 8bit μRISC, etc.
functional blocks Analog library	MTC 35800

C05 Documentation

the available material	.. and where ..
the C05 data sheet MTC 35000	CD ROM
SPICE Models for C05M BSIM3V3	DS 13314 CONTROLLED DOCUMENT
C05M-D Design Rule Manual	DS 13315 CONTROLLED DOCUMENT
C05M-A Design Rule Manual	DS 13316 CONTROLLED DOCUMENT
C05 Scribe Lane Insert Description	DS 10994 CONTROLLED DOCUMENT
Assembly Layout Rules	DS 13600 CONTROLLED DOCUMENT
the ADS reference manual	DOCUMENT
the ADS data sheet	CD ROM
the software development tools	CD ROM
and more on the web http://www.alcatel.com/telecom/micro	

Fig. 7 C05 Libraries & Document reference

3 ADS Asic Design System

3.1 ADS description

ADS is the result of thoroughly re-engineering the design methodologies that have supported the growth of the Alcatel Semiconductor Company on the market place. This effort is now released in a new quality-driven and consistent front-end and back-end environment.

ADS is an open design system, based on the best commercial tools and standard interfaces between them (EDIF, Verilog, VHDL, SDF, PDEF, GDSII). The entry of the ADS system is RTL-level both in Verilog HDL and VHDL language. ADS offers, through the complete design flow, a consistent concept of timing constraints and delay, delay calculation, and library timing information. Based on this, ADS provides a tight coupling between engines for logic synthesis and place & route. This enables the ADS system to converge quickly to a design that meet the initial timing constraints.

Within ADS front end, both Verilog & VHDL and co-simulation tools can be used. For the backend operation, Avant! floor-planning and place & route tools are supported. ADS provides an accurate characterisation of the libraries done at worst case with guaranteed accurate de-rating within a restricted range of voltage and temperature.

ADS is a mixed mode design system. The realisation of analog blocks is done by using the most advanced design methodology for the analog components. ADS supports behavioural (HDLA) description of analog circuits. This allows to implement high level description of circuits that are used for the specification distribution during the co-design phase. In-depth design and verification of the analog circuits are done at the transistor level with SPICE simulation. Finally, top-level simulation is possible by running mixed mode simulation. Last but not least ADS is used to control the backend integration.

In addition, ADS allows the mapping of the most common FPGA prototypes. The documentation is provided through an easy to use on-line documentation tool. ADS quality is ensured by a dedicated QA-flow whenever a new tool release is supported by the environment.

3.2 The value added re-usable blocks

ADS includes several compilers for ROM and RAM blocks, as well as a long list of high added-value Application Specific Standard Blocks (ASFB) in the telecom and data-processing area.

ADS brings into the design flow a family of embedded 8bit, 16bit and 32bit RISC μ-cores, capable to deliver up to 30 MIPS, and microprocessors peripherals: UART, DMA, IRQ, PIC, RTC, ..., and telecommunication blocks: ISDN interface, HDLC controller, RS encoder, QAM demodulator, ... (see also our Internet web site: http://www.alcatel.com/telecom/micro).

The ASFB strategy supports also value added analog blocks like broadband and/or high dynamic A/D and D/A converter, PLL, pass-band filters.

4 THE QUALITY

Alcatel Microelectronics is a quality-minded company.

A state of the art Average Quality Level (AQL) of 3ppm is the result by today of a long and continuous improvement of the quality system put in place to track the defects. Methods like Iddq (test of Idd leakage current @Vdd_nom & all bias off) and Vstress/Vscreen (some real test-pattern, e.g. ScanPath, @ 1.4xVdd_max) are standard test methodologies put in place to reduce the AQL-level to the target number of 0.5ppm in the year 2000.

This commitment to the quality has been re-enforced by the decision to fulfil the QS9000 by year 1999.

5 CMOS ROADMAP

The commitment of Alcatel Microelectronics to the state of the art mixed mode technologies is dedicated to mixed CMOS.

The 0.5 μm mixed CMOS technology and the I^2T technology (0.7 μm mixed high voltage CMOS) are in production since begin 1996.

The 0.35 μm digital CMOS technology is in production since end 1997.

The analog 0.35 CMOS technology is in prototype phase since mid 1998 and will be released for production begin 1999.

The next generation will be 0.25 μm digital CMOS, start of the prototype phase is spring 1999, production release is forecasted begin 2000.

6 0.35 μm Mixed CMOS Technology preview

Based on the same technology route as the 0.5 μm CMOS, the mixed mode CMOS 0.35 μm will be available fall 98. This technology provides an increased digital density: About a factor of 4. It is based on a five-layer metal obtained by Chemical Mechanical Planarisation (CMP). This technology makes use of amorphous silicon gates.

Analog options C035A, target parameters

second Poly layer, capacitor	Poly0-Poly1 linear capacitor, 1.1nF/mm2, tol ±10%, Vcl <20ppm/V, Vcq <10ppm/V, matching <0.1% (3 sigma) @W/L = 20/20
high-ohmic Poly resistor	1kΩ/sq, tol ±10%, voltage linearity: < 300 ppm/V temperature coefficient: < 2000 ppm/°C matching <0.5% (3 sigma) @W/L = 5/50
bipolar transistor	vertical PNP

Fig.8: C035 Analog options

7 CONCLUSION

Alcatel Microelectronics, leader of the mixed mode ASIC market, is bringing the technologies for the mixed-mode system-on-a-chip. This strategy is the result of an important investment in the technologies and design methodologies fitted for sub-micron design. This important step in the mixed mode design shows the move from large analog / small digital (Ad) to the large digital / small analog (Da) chip manufacture technique. This strategy is supported by a continuous improvement of the product quality.

Finally, the commitment of Alcatel Microelectronics to the state of the art mixed mode technologies is now continued in the set-up of the first 0.35 μm mixed mode technology.

8 Acknowledgements

I want to explicitly express my thanks to my colleagues from the Technical Marketing, Design, CAD and R&D departments for all the discussions and the perfect support.

9 REFERENCES

/1/ B. Goffart, "C05 technology details", internal presentation, Alcatel Microelectronics, 13. May. 1998

/2/ J. De Greve, "CMOS 0.50um Technology Seminar", internal presentation, Alcatel Microelectronics, 1. October 1997

/3/ B. Goffart, "C035 short, The Dynamite Hardware", internal presentation, Alcatel Microelectronics, 3. July 1998

/4/ R. Lannoo, "ADS presentation May 98", internal presentation, Alcatel Microelectronics, 5. May. 1998

/5/ Internet web site of Alcatel Microelectronics: http://www.alcatel.com/telecom/micro

Hans Gugg-Schwaiger
Alcatel Microelectronics
Arabellastrasse 4, D-81925 München, Germany
e-mail: hans.gugg-schwaiger@mie.alcatel.be

Prispelo (Arrived): 21.09.98 *Sprejeto (Accepted): 16.11.98*

THIN FILM COLOR DETECTORS BASED ON AMORPHOUS SILICON

Marko Topič and Franc Smole
Faculty of Electrical Engineering, University of Ljubljana, Slovenia

INVITED PAPER
MIDEM'98 CONFERENCE
23.09.98 – 25.09.98, Rogaška Slatina, Slovenia

Keywors: optoelectronics, semiconductors, color detectors, RGB colors, Red Green Blue colors, thin film technologies, a-Si:H, Hydrogenated amorphous Silicon, PIIIN structures, Positive-Intrinsic-Intrinsic-Intrinsic-Negative structures, two-terminal structures, PIN-PINIP structures, Positive-Intrinsic-Negative-Positive-Intrinsic-Negative-Intrinsic-Positive structures, PINIP-PIN structures, Positive-Intrinsic-Negative-Intrinsic-Positive-Positive-Intrinsic-Negative structures, three-terminal structures, TFA sensors, Thin-Film-on-Application-specific-integrated-circuits sensors, PECVD, Plasma-Enhanced Chemical Vapor Depositions, numerical modeling, TCO, Transparent Conductive Oxides, bipolar biases, forward biases, reverse biases

Abstract: The operational principle of two-terminal and three-terminal three-color detectors with the a-Si:H-based multi-layer multi-bandgap structures is investigated. Two different approaches (the two-terminal and three-terminal approach, which lead to either unipolar or bipolar bias-controlled three-color detection, are described and evaluated in terms of spectral response, rejection ratio and color suppression with regard to illumination intensity and bias-light. For the two-terminal PIIIN structure, numerical simulation results showed strong negative correlation between color separation and bias-light sensitivity, i.e. the better the color separation the worse insensitivity to bias-light and stronger non-linearity with illumination intensity. For the three-terminal PIN/PINIP and PINIP/PIN structures, the thicknesses of the individual layers were first optimized for the detection of the fundamental chromatic components using the numerical simulator and afterwards fabricated and characterized.

Amorfnosilicijevi tankoplastni detektorji barv

Ključne besede: optoelektronika, polprevodniki, detektorji barv, RGB barve rdeča zelena modra, tehnologije tankoplastne, a-Si:H silicij amorfni hidrogeniziran, PIIIN strukture pozitivno-notranje-notranje-notranje-negativno, strukture dvo-terminalne, PIN-PINIP strukture pozitivno-notranje-negativno-pozitivno-notranje-negativno-notranje-pozitivno, PINIP-PIN strukture pozitivno-notranje-negativno-notranje-pozitivno-pozitivno-notranje-negativno, strukture tro-terminalne, TFA senzorji tankoplastni na vezjih integriranih aplikacijsko specifičnih, PECVD nanosi CVD plazemsko izboljšani, modeliranje numerično, TCO oksidi transparentni prevodni, točke delovne bipolarne, točke delovne propustne, točke delovne zaporne

Povzetek: Prispevek obravnava delovanje dvokontaktnih in trikontaktnih trobarvnih detektorjev, ki temeljijo na večplastnih strukturah iz amorfnega silicija. Dvokontaktni pristop zaznava vse tri barve s spreminjanjem zunanje napetosti reverzne polaritete, trikontaktni pa s spreminjanjem zunanje napetosti obeh polaritet. Barvno zaznavanje smo za oba pristopa ovrednotili s spektralno občutljivostjo, rejekcijskimi faktorji in faktorji barvnega dušenja v odvisnosti od intenzitete osvetlitve in dodane osvetlitve. Za dvokontaktno PIIIN strukturo so numerični simulacijski rezultati pokazali močno negativno korelacijo med kvaliteto ločevanja barv in neobčutljivostjo na dodano svetlobo. Z izboljšano kvaliteto ločevanja barv torej izgubljamo na neobčutljivosti na dodano svetlobo. Hkrati postaja spektralni odziv PIIIN strukture v odvisnosti od intenzitete osvetlitve vedno bolj nelinearen. Za trikontaktne PIN/PINIP in PINIP/PIN strukture smo debeline posameznih plasti optimirali za detekcijo osnovnih kromatskih komponent s pomočjo numeričnega simulatorja, jih izdelali in okarakterizirali.

1. INTRODUCTION

Hydrogenated amorphous silicon (a-Si:H) thin film optoelectronic devices are not only easily applicable in intelligent image thin-film-on-application-specific-integrated-circuits (TFA) sensors /1/, but they can also be simply integrated upon amorphous, poly- or monocrystalline readout electronics /2,3/. The optoelectronic properties of a-Si:H based films can be changed by deposition parameters of plasma-enhanced chemical vapour deposition (PECVD) process and by modifying the optical gap by the addition of carbon or germanium atoms in the plasma during the deposition. Such an approach enables detection from ultraviolet to the infrared /4,5/. High photosensitivity in the visible light spectrum, homogeneous deposition over large areas by PECVD, and low-cost fabrication make a-Si:H and its alloys a promising candidate for color detectors /6/. In multi-layer a-Si:H based structures for detection of two, three or more colors, spectral response is bias-controlled. Since all the signals (e.g. red, green and blue (RGB)) are bias-controlled at the same spatial detector position without the need of optical filters, the color-moiré effect can be prevented. The possibility of producing large area photosensing arrays makes a-Si:H-based devices even more attractive.

Recent advances in the two-terminal a-Si:H based three-color detectors exhibit the potential of these devices for the color sensor arrays. Unresolved speed limitation of the two-terminal transparent conducting oxide (TCO)/NIPIIN/metal detectors /7/ speaks in favour of the alternative two-terminal TCO/PIIIN/metal detectors /8,9/. In order to achieve bias-controlled spectral separation of fundamental chromatic components RGB, the PIIIN structures need to be band-gap profiled. To examine such an approach, the ASPIN numerical simulator is used.

Beside two-terminal devices, a family of three-terminal three-color detectors based on stacked a-Si:H based structures is theoretically and experimentally investigated. The detectors have the structure

TCO/PI$_1$N/TCO/PI$_2$NI$_3$P/metal or TCO/PI$_1$NI$_2$P/TCO/PI$_3$N/metal. Using the ASPIN numerical simulator, device physics of different design concepts is analyzed and presented. Optimization criteria deduced from simulation and experimental results and their comparison are investigated and discussed.

2. NUMERICAL MODELING

The ASPIN computer model /10/ is used for steady-state analysis of different PIIIN structures with the aim to explain the red-green-blue (RGB) three-color detection mechanism and to gain detailed insight into the operating principle of the PIIIN structures. For the three-terminal structures, the ASPIN simulator was used to optimize the thickness of the individual layers.

The light generation model is based on the particle nature of light and takes into account only the reflection at the front glass surface. The flux of photons is taken to decay exponentially. The absorption coefficient in each layer is wavelength dependent and corresponds to the imaginary part of the complex refractive index. Although the model does not account either for interference or for the numerous reflections in the multi-layer structure, the model gives a good agreement with the experimental results for structures deposited on rough TCO (with haze) /11,12/. For flat TCOs (without haze), an accurate numerical modeling should include the wave nature of light that accounts for light interference effects, especially in the long wavelength range of the visible light spectrum /13,14/.

3. UNIPOLAR BIAS-CONTROLLED COLOR DETECTION PRINCIPLE IN PIIIN DETECTORS

For high short-circuit current in PIN a-Si:H solar cells, the collection efficiency is to be as high as possible throughout the whole visible spectrum. Under reverse bias, the collection efficiency (CE) usually only slightly improves. In a-Si:H color detectors, the CE must be bias controlled. Since PIIIN color detectors operate only under reverse bias, this detection principle is described as unipolar bias-controlled detection principle. By increasing the externally applied reverse bias the CE of PIIIN device can only improve. Thus, to enable different spectral response as a function of reverse bias, the CE at short-circuit conditions must be worse than that one of the PIN solar cell. The electric field plays a key role in governing the CE. To worsen CE of the PIIIN structure at short-circuit conditions, the built-in electric field must be weaker throughout the structure and strongly non-uniform. There are several possibilities:

- to insert appropriate compensational doped layers next to the P and N layer,
- to reduce the doping concentration in the P and N layer,
- to use worse quality I layers with higher defect density.

The thickness of constituent layers with their optical absorption coefficients (α) determine the spatial distribution of the photogeneration of excess carriers. Fig. 1 shows typical generation rate profiles in a P(a-SiC:H)I$_1$(a-SiC:H)I$_2$(a-Si:H)I$_3$(a-SiGe:H)N(a-Si:H) three-color detector. Since the P and I$_1$ layer have a high optical gap (E_{opt}=2.2 eV), the photogeneration region of blue monochromatic illumination (λ=450 nm) dominates in the front part of the PIIIN structure. The abrupt changes of profiles denote interfaces between layers and they are due to higher α in the subsequent layers with the lower optical gap. For red monochromatic illumination (λ=630 nm), the photogeneration region spreads in the last third of the PIIIN structure.

Simulations showed that strong non-uniform electric field profiles in the PIIIN structures always lead to an increased electric field in the front part of the structure, especially at the PI$_1$ interface. Therefore, the PIIIN devices under low reverse bias detect only shorter wavelengths and under higher reverse bias the electric field strengthens throughout the structure, so the whole

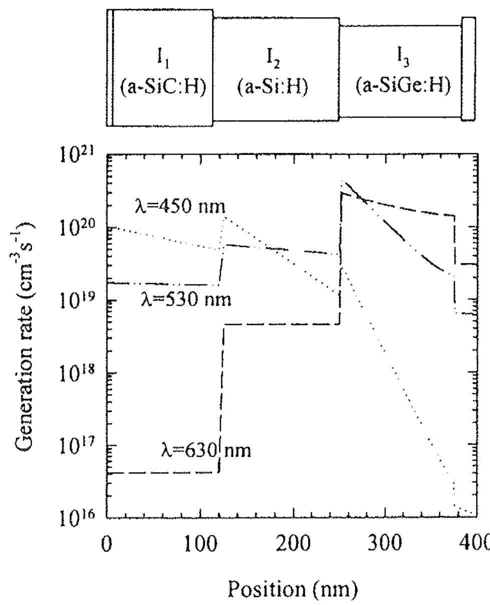


Fig. 1 Generation rate profiles throughout a PI$_1$I$_2$I$_3$N structure for different monochromatic illuminations (1 mW/cm^2).

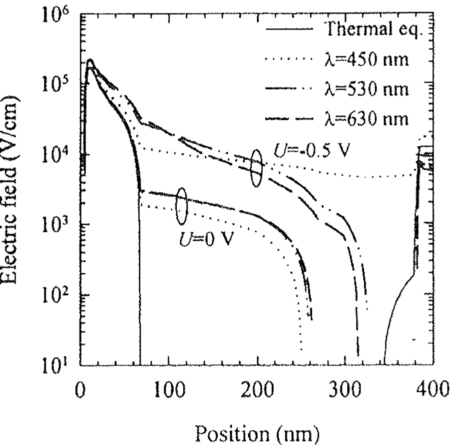


Fig. 2 Calculated electric field profile of the optimized PνI$_1$I$_2$I$_3\pi$N structure for a three-color detector under different monochromatic illuminations and two biases.

range of the visible light spectrum is detected. In case of three-color detector, such a detection principle can generate three signals with the information: blue (B), blue+green (B+G), blue+green+red (B+G+R). The signals are to be transformed into the RGB components. However, the extraction is justified only if the three-color detector behaves as a linear system, i.e. linearly as a function of illumination intensity and insensitively to the bias-light.

4. THREE-COLOR PIIIN DETECTORS

In the study of PI_1I_2N structures /15/, the built-in electric field was profiled using the compensational doping approach in the $P\nu I_1I_2\pi N$ structure or using the high-defect-density I_1* layer approach in the PI_1*I_2N structure. Both analyzed structures suffered the non-linearity and bias-light sensitivity.

In the $PI_1I_2I_3N$ detectors, an a-SiGe:H layer with E_{opt}=1.6 eV is added as the third I layer (I_3) to improve the detection of the long wavelength illumination. The germanium content in a-SiGe:H increases the slope of the tail states and defect density. From /16/, a 5-times higher density of dangling bond states than in the I_2(a-Si:H) layer was selected. The calculated generation rate profiles of the optimized $PI_1I_2I_3N$ structure with 10-100-150-115-25 nm thickness are shown in Fig. 1.

Under short-circuit condition, the electric field should only assist in the collection of excess carriers from short wavelength photons (up to 450 nm). Thus, the built-in electric field should be high only in the front part of the structure, otherwise it should even change its direction. For this purpose, we inserted between the P and I_1 layer a compensational N layer (ν layer) and between the I_3 and N layer a compensational P layer (π layer). The built-in electric field profile of the optimized structure is shown in Fig. 2 (full line). Under short-circuit condition with monochromatic illumination, the electric field changes due to recharging of defects (Fig. 2). Increasing the reverse bias, the electric field recovers first for blue illumination, afterwards for green and finally, also for red illumination. For a good color separation, the doping concentrations in the compensational ν and π layers are to be high or the same effect can be achieved by selecting the P and N layer with lower doping concentration.

Calculated spectral response of the optimized $PI_1I_2I_3N$ structure as a function of reverse bias is presented in Fig. 3. Calculated current-voltage (J-U) characteristics of the optimized $PI_1I_2I_3N$ device for different monochromatic illuminations (1 mW/cm^2) is plotted in Fig. 4. Current-voltage behavior under blue and green illumination is qualitatively similar to the behavior of the PIIN structures. In contrast to the PIIN J-U characteristics under red illumination, a postponed red response with regard to the reverse bias occurred. From the color-separation point of view, this postponed or sometimes even an S-shape behavior is beneficial, since it provides better rejection ratios under lower reverse bias, and different groups /8,9/ experimentally observed it. The origin comes from increased defect states in the I_3 layer, hindering the extraction of excess carries therein due to increased recombination. The extent of increase of the defect states in the I_3 layer increase determines the

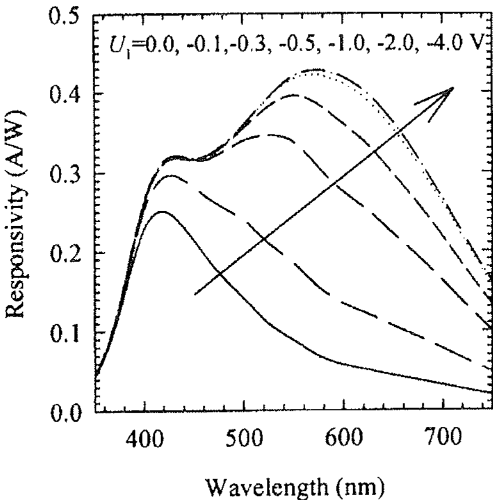


Fig. 3 Calculated spectral response of the optimized $PI_1I_2I_3N$ structure for a three-color detector as a function of reverse bias.

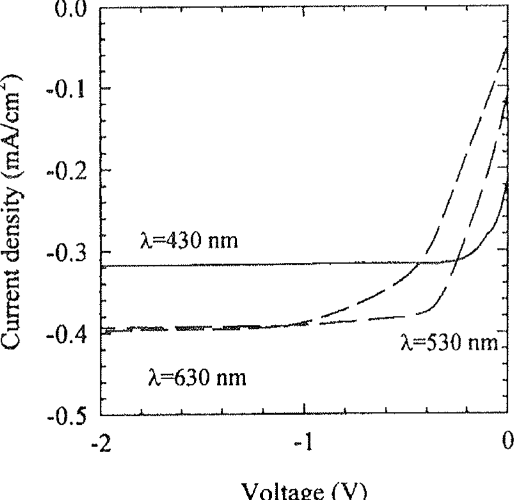


Fig. 4 Calculated J-U characteristics of the optimized $PI_1I_2I_3N$ device for different monochromatic illuminations (1 mW/cm^2).

triggering reverse bias, beyond which the red response steeply starts to increase.

4.1. Examination of bias-light and illumination intensity

For correct extraction of an RGB signal, the PIIIN three-color detectors should exhibit no monochromatic bias-light dependence. We examined the bias-light dependence under the short (450 nm) and long wavelength (650 nm) bias-light. The optimized three-color PIIIN structure, exhibits weak bias-light dependence under short-circuit (detection of B) and under high reverse bias (detection of B+G+R). Unfortunately, strong bias-light dependence occurs in the middle

range of reverse bias (Fig. 5). Significant variation of the spectral response is due to the redistribution of the electric field caused by the recharging of defects in the front or the rear part of the device for short wavelength or long wavelength bias-light, respectively. We managed to mitigate the bias-light dependence by reducing the thickness of the device. At the same time, reduced thickness almost proportionally shrinks the reverse bias range of detection, but it affects the spectral response only in the long wavelength region. The results showed that the bias-light dependence correlates with the reverse bias dependence of the long wavelength spectral response (under no bias-light). The higher the variation of red response as a function of reverse bias is, the more bias-light dependent is the device. To reduce the bias-light dependence, we have to sacrifice the suppression of long wavelength response under short-circuit conditions, resulting in a worse color separation. Thus, a trade-off between good color separation and low bias-

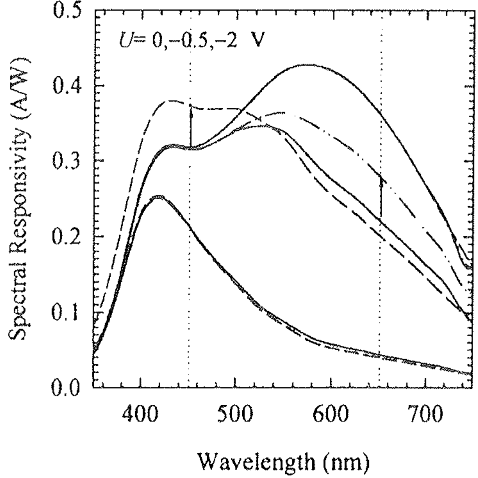


Fig. 5 Calculated spectral responses of the optimized 400 nm thick PIIIN color detector for (0 V, -0.5 V, -2 V) bias without (full line), with 450 nm (dash-dot-dot line) and 650 nm (dashed line) monochromatic bias-light (1 mW/cm²).

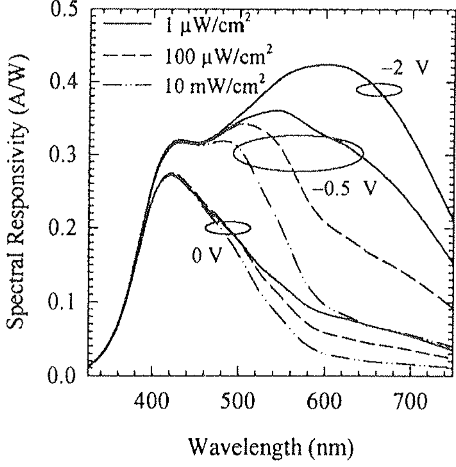


Fig. 6 Calculated spectral responses as a function of illumination intensity (0.001, 0.1, 10 mW/cm²).

light sensitivity is in the unipolar bias-controlled PIIIN structures unavoidable.

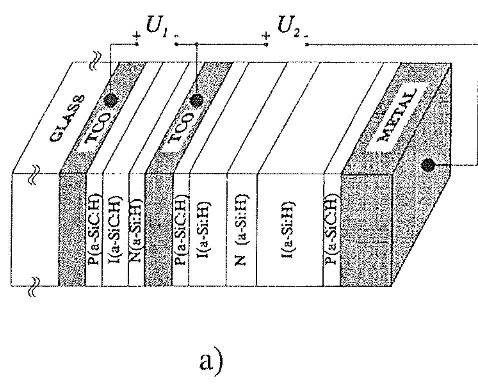
All structures were also examined for different illumination intensities, ranging from μW/cm² up to 100 mW/cm². Again, larger differences in spectral response arose only in the middle reverse bias range (Fig. 6). Simulations showed that thinner devices exhibit better linearity. Again, a trade-off between good color separation and illumination linearity together with bias-light sensitivity is therefore necessary.

5. BIPOLAR BIAS-CONTROLLED DETECTION PRINCIPLE IN THREE TERMINAL DETECTORS

A family of bipolar bias-controlled three-terminal three-color detectors based on stacked a-Si:H based structures has recently been proposed /17,11,12/. The detectors have the structure TCO/PI_1N/TCO/PI_2NI_3P/metal or TCO/PI_1NI_2P/TCO/PI_3N/metal. Numerical analysis of both stacked structures, and the optimization of their layer thicknesses for the detection of the fundamental chromatic components - blue, green and red - was performed using the ASPIN numerical simulator /17/.

5.1. Bipolar bias-controlled detection principle

The TCO/PI_1N/TCO/PI_2NI_3P/metal structure (Fig. 7a) consists of a top PI_1N diode and two anti-serial diodes in the sequence PI_2NI_3P accompanied by three contacts (TCO_1, TCO_2 and metal). The PI_1N diode independently detects the blue color under reverse bias (U_1 < 0 V), while the PI_2NI_3P structure acts under differ-



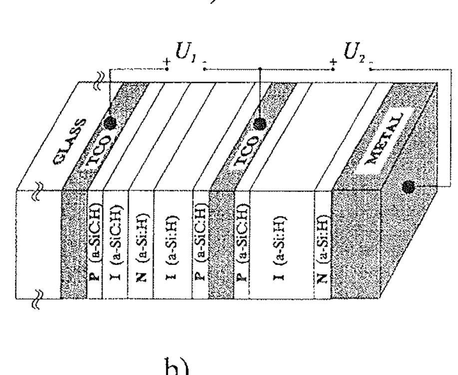


Fig. 7 Schematic view of a three-terminal detectors a) TCO/PI_1N/TCO/PI_2NI_3P/metal and b) TCO/PI_1NI_2P/TCO/PI_3N/metal structure.

ent polarity of the externally applied voltage U_2 as the photodetector for the green or red color. For a negative bias (U_2<0 V), the PI_2N diode operates as a photodetector and the NI_3P diode as an impedance. While most of the high energy photons (blue light) are already absorbed in the top PI_1N diode, the photons of green light generate electron/hole pairs mainly in the PI_2N diode. The red light has the longest penetration depth, and it should be collected in the NI_3P diode under a positive bias (U_2>0 V), under which the PI_2N diode operates as an impedance and the NI_3P as a photodetector. Since both polarities of bias are used, this color detection principle is called bipolar bias-controlled principle.

In the TCO/PI_1NI_2P/TCO/PI_3N/metal structure (Fig. 7b), the PI_3N diode detects the red color independently (U_2<0 V), while the PI_1NI_2P structure acts under application of different bias voltages as a photodetector for the blue and green color (analogous to the operation of PI_2NI_3P discussed above).

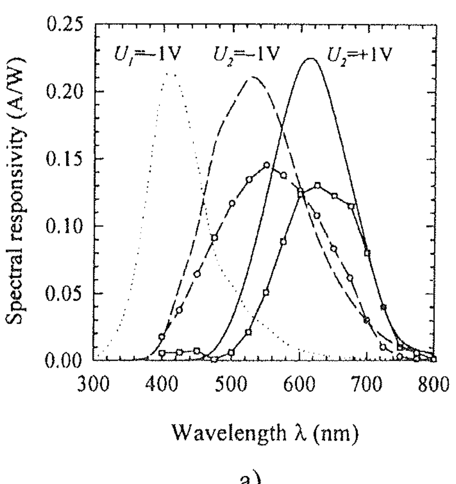
The only sophistication is the three-terminal approach that requires some additional technological steps (deposition of TCO_2, interconnections), which have already been successfully utilized for parallel-connected tandem solar cells /18/. With regard to the electronic detection system, this three-terminal approach for the detection of three colors is even more simple than the two-terminal approach.

5.2. Simulation results

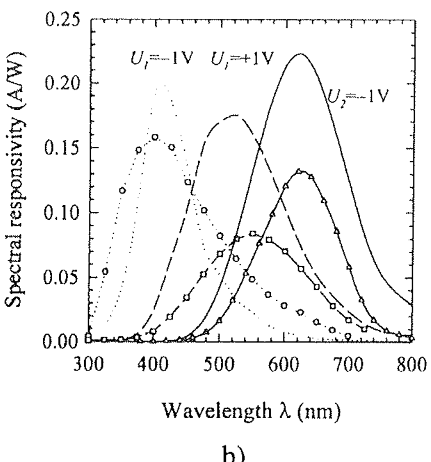
Simulations and optimization of the TCO/PI_1N/TCO/PI_2NI_3P/metal and TCO/PI_1NI_2P/TCO/PI_3N/metal structure was performed using the ASPIN numerical device simulator. The optimized thicknesses of the individual layers are listed in Table 1.

For the top I_1-layer and all P-layers, a wide bandgap (a-SiC:H) material is used. The N layer in the PI_1NI_2P structure is thicker in order to provide spectral separation between blue and green color, and hence to have good rejection ratios (>2.0).

The calculated spectral responsivity of the TCO/PI_1NI_2P/TCO/PI_3N/metal structure is plotted in Fig. 8. The structure exhibits narrow spectral responses (full width half magnitude - FWHMs below 150 nm) and high rejection ratios: for the PI_1NI_2P structure both at 430 nm (R_{-1V}/R_{+1V}= 3.0) and at 530 nm (R_{+1V}/R_{-1V}= 5.3). The color suppression is R_{430nm}/R_{530nm}= 5.6 at U_1= -1 V and R_{530nm}/R_{430nm}= 2.8 at U_1= +1 V. For the PI_3N diode, which independently detects red color at reverse applied voltage, the color suppression is also good (R_{630nm}/R_{530nm}= 2.7 at U_2= -1 V).



a)



b)

Fig. 8 Calculated (lines) and measured (lines drawn as guides for the eyes with symbols) spectral responsivity of
a) TCO/PI_1N/TCO/PI_2NI_3P/metal and
b) TCO/PI_1NI_2P/TCO/PI_3N/metal structure.

Table 1 Optimised geometrical parameters of three-terminal three-color detectors

	TCO	P	I_1	N	TCO	P	I_2	N	I_3	P
d_S (nm)	1000	5	40	5	1000	11	50	140	369	11
d_E (nm)	740	10	30	10	1000	10	50	130	270	20

	TCO	P	I_1	N	I_2	P	TCO	P	I_3	P
d_S (nm)	1000	5	35	45	60	11	1000	30	365	20
d_E (nm)	1000	10	35	60	60	11	1000	20	365	20

S- simulation; E - experiment

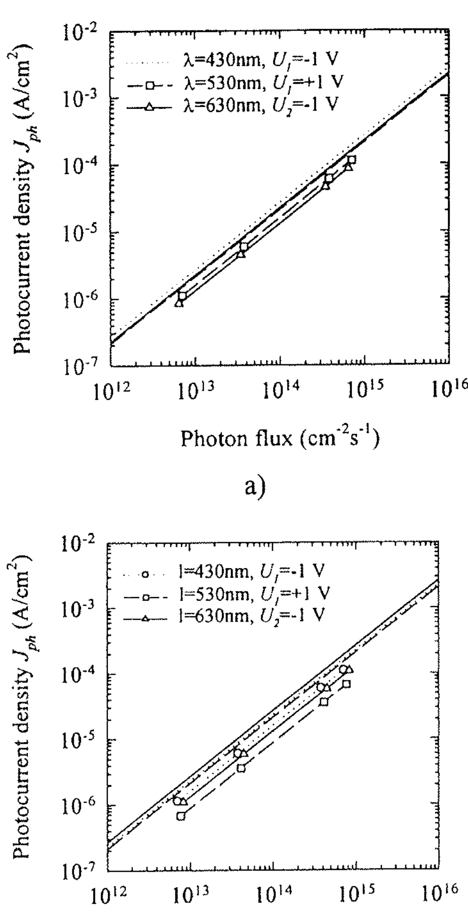


Fig. 9 Calculated (lines) and measured (symbols) photocurrent vs. photon flux under blue (430 nm) and green (530 nm) and red (630 nm) illumination of
a) TCO/PI$_1$N/TCO/PI$_2$NI$_3$P/metal and
b) TCO/PI$_1$NI$_2$P/TCO/PI$_3$N/metal structure.

Simulations showed that both structures had a linear photocurrent/generation-rate relationship for all three colors at peak wavelengths 450, 530, 635 nm, applying a bias of ±1 V or more (Fig. 9). This linearity allows all three colors to be easily detected with adequate rejection ratios.

5.3. Experimental results

A conventional two-chamber PECVD deposition system (30 x 30 cm^2) was used for the deposition of PIN and PINIP structures. A smooth glass/indium tin oxide substrate was used for the front TCO, and sputtered ZnO for the second TCO. Patterning steps were made by laser scribing /18/.

We started the experimental investigation with the TCO/PI$_1$N/TCO/PI$_2$NI$_3$P/metal structure. It had already been demonstrated /11/ that the PI$_2$NI$_3$P structure exhibits very good (>3.0) rejection ratios and color suppressions between green and red color (Fig. 8a, lines with symbols). However, the thickness of the top PI$_1$N diode (10-30-10 nm) was too small to prevent the shunt defects, thus hindering the detection of the blue color. We managed to reduce the top PI$_1$N diode thickness (while preserving its functionality) to 90 nm. But, the spectral response is too broad (FWHM=210 nm) and the maximum is located at 455 nm. Despite the I$_1$ layer thickness reduction, the spectral responsivity of PI$_1$N diode decreases very slowly in the wavelength region above 500 nm, indicating that an a-SiC:H material with a higher optical gap should be preferred.

The problem of the top PI$_1$N diode functionality was solved with the TCO/PI$_1$NI$_2$P/TCO/PI$_3$N/metal stacked structure. Since the whole PI$_1$NI$_2$P (10-35-60-60-15 nm) structure was around 180 nm thick, local defects impeding the photodetection function were eliminated. The fabricated PI$_1$NI$_2$P structure shows good detection of blue and green color (Fig. 8b; lines with symbols). It exhibits narrow spectral responses ($FWHM_{(U1=-1V)}$=165nm and $FWHM_{(U1=+1V)}$=180 nm) and high rejection ratios, at λ=450 nm with R_{-1V}/R_{+1V}= 7.8 and at λ=530 nm with R_{+1V}/R_{-1V}= 1.3. The measured color suppression is high, R_{450nm}/R_{530nm}= 4.1 at U_1= -1 V and R_{530nm}/R_{450nm}= 2.3 at U_1= +1 V, and the dynamic range is also very high.

The fabricated bottom PI$_3$N (20-365-20 nm) diode detects independently the red color under reverse bias. Its measured spectral responsivity at U_2= -1 V is plotted in Fig. 8b (lines with triangles). It has the narrowest FWHM (140 nm) in the structure and a high color suppression (R_{630nm}/R_{530nm}= 3.1 at U_2= -1 V).

The linear photocurrent/generation-rate dependence of both three-terminal structures derived from the simulations was confirmed by measurements under different monochromatic illumination intensities ranging from 10^{12} to 10^{15} photons per cm^{2}s (Fig. 9; lines with symbols).

Comparison between simulated and measured results in Fig. 8 reveals the following: a) losses in the glass and front TCO were higher than assumed; b) the I$_1$ layer absorbs too large a part of the long-wavelength light; c) the second TCO acts as a good reflector, resulting in a large difference between simulated and measured results for the PI$_3$N diode.

Thickness optimization of the second TCO will be necessary. Good reflectivity of the second TCO and thus low responsivity of the PI$_3$N diode could be partly mitigated with an improved reflection at the back contact.

6. CONCLUSIONS

We used numerical modeling as a tool for analysis of thin film color detectors based on a-Si:H.

The device physics of two-terminal a-Si:H based three-color detectors with the multi-layer multi-bandgap PIIIN structure was investigated. They operate under different reverse (unipolar) biases. The PIIIN structures suffer from high bias-light sensitivity and non-linearity of the illumination intensity, although this sensitivity can be mitigated with the higher built-in electric field at the expense of worse color separation. The optimized PIIIN

structure operates under lower range of reverse bias and the I_3 layer with an increased defect density results in a postponed red response. The results lead to the conclusion that for a more linear and bias-light independent color detection in the PIIIN devices, we have to sacrifice the quality of three color separation or vice versa.

The three-terminal structures operate under forward and reverse (bipolar) biases. They exhibit excellent linearity, a high dynamic range and they directly generate a RGB-signal.

Due to stringent thickness conditions (<60 nm) for the top PI_1N diode in the $TCO/PI_1N/TCO/PI_2NI_3P$/metal structure, and additionally due to high reflection of the second TCO, the steady-state experimental results indicate that the $TCO/PI_1NI_2P/TCO/PI_3N$/metal structure gained an advantage over the $TCO/PI_1N/TCO/PI_2NI_3P$/metal structure.

ACKNOWLEDGMENTS

The authors want to thank J. Furlan (University of Ljubljana) for helpful discussions, W. Kusian (Siemens AG) for the encouragement and the fabrication of three-terminal samples. The work was supported by the Ministry of Science and Technology Republic of Slovenia, which is gratefully acknowledged.

REFERENCES

/1/ M. Böhm et al., "Image sensors in TFA technology", Mat. Res. Soc. Symp. Proc. 507 (1998) in print.

/2/ R. A. Street, R. L. Weisfield, R. B. Apte, S. E. Ready, A. Moore, M. Nguyen, W. B. Jackson, P. Nylen, "Amorphous silicon sensor arrays for X-ray anddocument imaging", Thin Solid Films 296 (1997) 172.

/3/ P. Mei, J. B. Boyce, D. K. Fork, G. Anderson, M. Hack, R. Lujan, "Hybrid amorphous and polycrystalline silicon devices for large-area electronics", Mat. Res. Soc. Symp. Proc. 507 (1998) in print.

/4/ G. de Cesare, F. Irrera, F. Palma, M. Tucci, E. Jannitti, G. Naletto, P. Nicolosi, "Amorphous silicon/silicon carbide photodiodes with excellent sensitivity and selectivity in the vacuum ultraviolet spectrum", Appl. Phys. Lett. 67 (1995) 335.

/5/ Y. K. Fang, S. B. Hwang, K. H. Chen, C. R. Liu, L. C. Kuo, "A Metal-Amorphous Silicon-Germanium Alloy Schottky Barrier for Infrared Optoelectronic IC on Glass Substrate Application", IEEE Trans. on Electron Devices 39 (1992) 1350.

/6/ H. Stiebig, D. Knipp, J. Fölsch, F. Finger, H. Wagner, "Optimized three-color detector based on a-SiGe:H heterojunctions", Mat. Res. Soc. Proc. 420 (1996) 153.

/7/ H. Stiebig, C. Ulrichs, T. Kulessa, J. Fölsch, F. Finger, H. Wagner, J. Non-Crystalline Solids 198-200 (1996) 1180.

/8/ T. Neidlinger, M. B. Schubert, G. Schmid, H. Brummack, "Fast color detection with two-terminal P-I-I-N devices", Mat. Res. Soc. Proc. 420 (1996) 147.

/9/ D. Knipp, H. Stiebig, J. Fölsch, R. Carius, H. Wagner, "Improved concept for NIPIIN and PIIIN color sensitive two-terminal devices with high linearity", Mat. Res. Soc. Proc. 467 (1997) 931.

/10/ F. Smole, M. Topič, J. Furlan, "Analysis of TCO/p(a-SiC:H) heterojunction and its influence on p-i-n a-Si:H solar cell performance", J. Non-Crystalline Solids 194 (1996) 312.

/11/ M. Topič, F. Smole, J. Furlan, W. Kusian, "Stacked a-SiC:H/a-Si:H heterostructures for bias-controlled three-colour detectors", J. Non-Crystalline Solids 198-200 (1996) 1180.

/12/ M. Topič, F. Smole, J. Furlan, W. Kusian, "Stacked a-Si:H-based three-colour detectors", J. Non-Crystalline Solids 227-230 (1998) 1326.

/13/ G. Tao, M. Zeman, J. W. Metselaar, "Accurate generation rate profiles in a-Si:H solar cells with textured TCO substrates", Solar Energy Materials and Solar Cells 34 (1994) 359.

/14/ P. Popović, J. Furlan, W. Kusian, "The wave nature of light in computer analysis of solar cells", Solar Energy Materials and Solar Cells 34 (1994) 393.

/15/ M. Topič, F. Smole, J. Furlan, "Investigation of a-Si:H PIIN color detector operation", Mat. Res. Soc. Symp. Proc. 507 (1998) in print.

/16/ J. Fölsch, F. Finger, T. Kulesa, F. Siebke, W. Beyer, H. Wagner, "Improved ambipolar diffusion length in a-$Si_{1-x}Ge_x$:H alloys for multi-junction solar cells", Mat. Res. Soc. Symp. Proc. 377 (1995) 517.

/17/ M. Topič, F. Smole, J. Furlan, " New bias-controlled three-color detectors using stacked a-SiC:H/a-Si:H heterostructures", Mat. Res. Soc. Symp. Proc. 377 (1995) 779.

/18/ W. Kusian, R. D. Plättner, J. Furlan, G. Conte, "A new double stacked a-Si:H solar cell having the structure pin/TCO/nip", Proc. 23rd IEEE PVSC (1993) 955.

Marko Topič and Franc Smole
Faculty of Electrical Engineering
University of Ljubljana
Tržaška 25, SI-1000 Ljubljana, Slovenia
E-mail: Marko.Topic@fe.uni-lj.si

Prispelo (Arrived): 21.9.1998 Sprejeto (Accepted): 16.11.1998

NEXT-GENERATION, ADVANCED THICK FILM MULTILAYER SYSTEM

Marc H. LaBranche, Cornelius J. McCormick, Jerome D. Smith, Roupen L. Keusseyan, Robert C. Mason, Mark A. Fahey, and Christopher R. S. Needes
DuPont Electronic Materials, Research Triangle Park, NC
Kenneth W. Hang
DuPont Electronic Materials, Experimental Station, Wilmington DE

INVITED PAPER
MIDEM´98 CONFERENCE
23.09.98 - 25.09.98, Rogaška Slatina, Slovenia

Keywords: electronic materials, dielectric materials, thick film multilayer materials, industrial electronics, automotive electronics, CG, Crystallizing-Glass, FG, Filled-Glass, automotive electronic circuits, reliability of electronic systems, thermal cycling

Abstract: A new thick film multilayer material system has been developed to meet the increasingly demanding cost and performance requirements of the marketplace. The key feature of the system is a new two print multilayer dielectric composition that survives -40/+125 °C thermal cycle excursions with soldered components, and has good yield and electrical reliability at 30 μm fired thickness instead of the usual 40 μm. The dielectric has a wide conductor compatibility, the system including solderable silver-bearing and wire bondable Au conductors. The dielectric can be used with mixed metals (Ag, Pd/Ag, Au) without blistering. The surface resistors have ±75 ppm TCR´s and less than 0.5% drift after 1000 hours aging. Cadmium-free versions of all materials are available, for compliance with environmental regulations. The dielectric, via fill, and a solderable Pd/Ag conductor can be cofired together, reducing the number of process steps in the circuit manufacture and so reducing manufacturing cost. The system has already been qualified for use in a high-volume, cost-sensitive automotive application.

Naslednja generacija materialov za večplastna debeloplastna vezja

Ključne besede: materiali za elektroniko, materiali dielektrični, materiali debeloplastni večplastni, elektronika industrijska, elektronika avtomobilska, CG steklo kristalizirajoče, FG steklo polnjeno, vezja elektronike avtomobilske, zanesljivost sistemov elektronskih, cikliranje termično

Povzetek: Razvili smo nov sistem debeloplastnih materialov, s katerim bomo ustregli naraščajočim zahtevam trga po izboljšanih tehničnih latnostih in cenovno ugodnih izdelkih. Ključna lastnost sistema je nova sestava večplastnega dielektrika za dvojno tiskanje. Le-ta vzdrži termične cikle -40/+125°C skupaj s prispajkanimi komponentami. Po žganju je pri debelini 30 μm po izkoristku in električni zanesljivosti enakovreden prejšnjemu sistemu z 40 μm debelino. Dielektrik je kompatibilen z mnogimi debeloplastnimi prevodniki, tako s spajkljivimi na osnovi srebra kakor tudi tistimi na osnovi zlata, predvidenimi za bondiranje. Dielektrik lahko uporabimo za vezja s kombinacijo prevodnikov na osnovi različnih kovinskih sistemov (Ag, Pd/Ag, Au), ne da bi pri žganju prišjo do napihovanja ali luščenja plasti. Upori, izdelani na površini dielektrika, imajo ±75 ppm TCR in manj kot 0.5% spremembe uporovnih vrednosti po 1000 urnem staranju. Na voljo so tudi verzije brez vsebnosti kadmija, ki ustrezajo vsem okoljevarnostnim predpisom. Dielektrik, prevodnik za tiskanje skozi povezovalne odprtine in spajkljivi Pd/Ag prevodnik lahko žgemo hkrati, s čimer zmanjšamo število procesnih korakov in s tem proizvodne stroške. Opisani sistem so že ovrednotili v velikoserijski, stroškovno občutljivi proizvodnji avtoelektronike.

INTRODUCTION

Thick film multilayer materials systems have to be both electrically and mechanically reliable, as well as cost-effective in high volume manufacturing environments. Crystallizing-glass (CG) dielectric compositions have become a technology of choice because of their high electrical reliability associated with their high density and resistance to migration of silver, but have not had the same mechanical reliability as highly filled, traditional filled-glass (FG) dielectrics, particularly during thermal cycling with soldered components /1/. Thermal cycle performance is critical for automotive applications, especially with the trend of moving components under the hood.

In order to obtain the best features of the CG and FG materials, a system was adopted based on a stratified dielectric scheme employing a single layer of QM42, plus two layers of 5707H dielectrics /2/, and has been used successfully to build automotive electronic circuits. However, it was recognized that it would be valuable to have a single dielectric material that would have the functionality of the two, especially if thermal cycle performance and electrical reliability could be obtained with only two prints of dielectric instead of the three. Furthermore, to be the most cost-effective, such a new multilayer system needed to incorporate as much cofiring as possible in order to reduce the number of process steps.

This paper describes a new thick film multilayer dielectric system that was developed to meet the challenging needs of the industry. It has already been qualified for automotive applications in the US /3/. An example of an engine control module made with this system is shown in Fig.1.

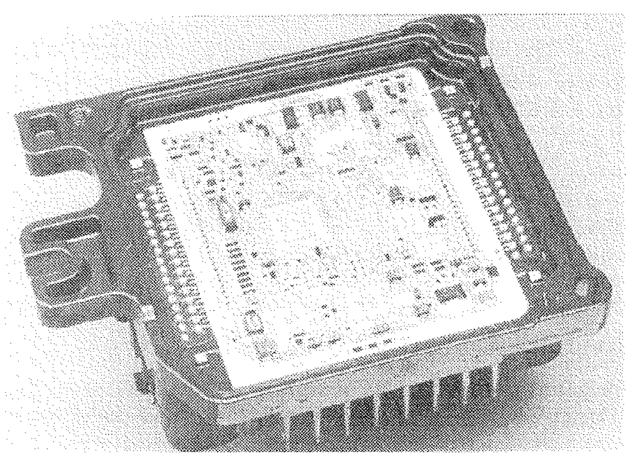


Fig. 1. Engine control module made with QM44 dielectric system, Delco Electronics

SYSTEM PERFORMANCE

Build Scheme

There are several ways of introducing cofiring to a two print dielectric multilayer circuit, as listed in Table I. For simplicity, the discussion will assume a two metal layer circuit, though the build scheme concepts apply to circuits that have additional levels of circuitry. Also, only build schemes that employ one via fill print per pair of dielectric prints are listed since a new via fill material was developed that was optimized for filling with a single print.

In Table 1, D1 and D2 refer to the first and second dielectric prints, respectively, C2 refers to the top conductor, and V refers to the via fill. The control build using sequential firing requires four firing steps to create the second metal layer after the first metal layer has been printed and fired. The ultimate approach to cofiring, which involves firing D1,D2,V, and C2 together, requires only one firing, but is not practical because printing large areas of dielectric over unfired dielectric typically leads to print defects in the second layer. Similarly, cofiring D1 and the substrate level conductor C1 is not recommended because of the potential for defects in the dielectric when printing over the dried (unfired) conductor.

Firing the via fill and C2 together but separately from the dielectric is technically feasible, but requires three firings and so is not an aggressive enough approach to removing firing steps. Similar comments apply to firing D1 and V separately and cofiring D2 and C2. The remaining two build schemes, which both employ metals cofired with dielectric, require two firings, and represent the most process savings that can realistically be achieved. Cofiring V and D 1 left a modest via posting before printing D2, complicating the printing of D2. The approach of cofiring V, D2, and C2 is preferred from a printing point of view. This cofire build scheme eliminates two firings for each metal layer beyond the substrate level conductor.

Table I. Possible cofire build schemes.

Build Scheme	Number of firings
Fire D1, D2, V and C2 sequentially	4 firings
Fire D1 and D2 sequentially Cofire V and C2	3 firings
Fire D1 and V sequentially Cofire D2 and C2	3 firings
Cofire D1 and V Cofire D2 and C2	2 firings
Fire D1 sequentially Cofire D2, V, and C2 (Preferred build)	**2 firings**
Cofire D1, D2, V and C2	1 firing

Dielectric

The basis of the new system is a novel dielectric composition, QM44. It is a Pb-free and alkali-free, ceramic filled crystallizing glass composition, where the filler loading and crystallization kinetics are controlled to optimize both fired film density and strength properties. It is dense and hermetic, with good print yields and reliability at 30 μm fired thickness. The dielectric constant is approximately 9, and dissipation factor is 0.1-0.2% at 1 kHz. The dielectric can be fired with mixtures of silver and gold conductors more than 30 times without blistering. Excellent adhesion is obtained with a wide range of conductors.

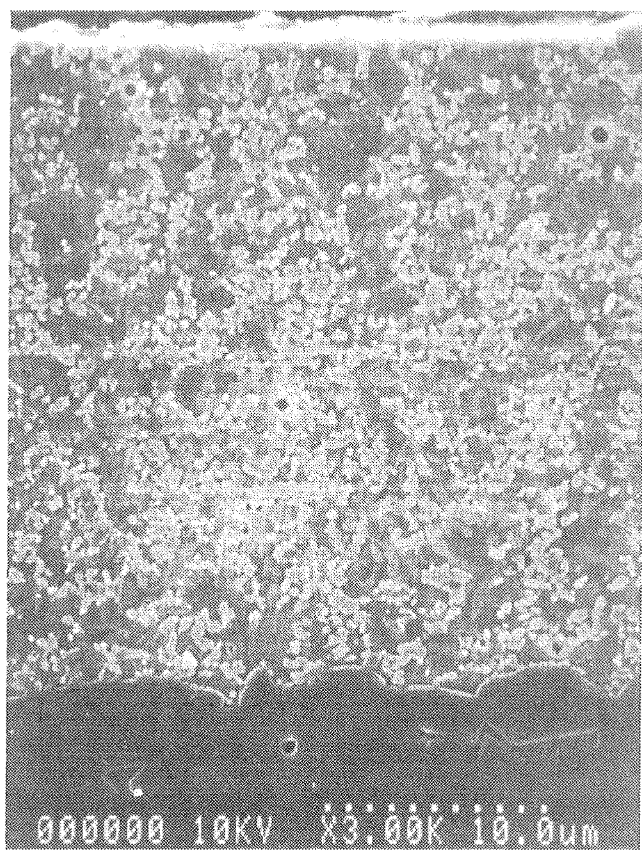


Fig. 2. Cross-section of the QM44 dielectric.

The glass viscosity and starting particle size are the critical factors in determining the maximum fired density a dielectric can achieve, and the filler loading that it can accommodate. Furthermore, to obtain high density films, crystallization must be delayed until after densification. Since glass crystallization often nucleates heterogeneously /4/, premature glass crystallization can occur with small particle size glass powders, especially through interaction with the ceramic fillers. By maintaining a wide difference between the softening point and the crystallization point in the dielectric, dense fired microstructures were obtained, as shown in Fig. 2.

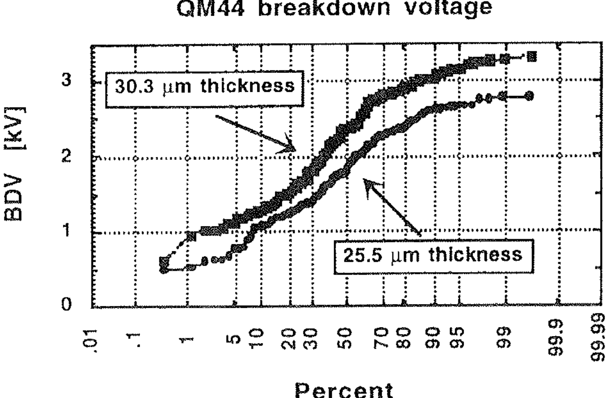


Fig. 3. QM44 breakdown voltage using 7484 3:1 Ag-Pd conductor.

The breakdown voltage (BDV) of the dielectric is shown in Fig. 3. The data is presented as a probability plot, showing the percentage of BDV data less than the Y-axis values. Data is plotted for two different dielectric thicknesses. Excellent BDV results were obtained even at approximately 25 μm thickness, though the distribution of low breakdown voltage values was better at 30 μm. The electrode was a 3:1 Ag-Pd sequential fire conductor printed to 17 μm squares. Only minor differences in QM44 BDV have been observed when using Ag-Pd, Ag-Pt, and pure Ag conductors, and between cofired and sequentially fired builds. The average BDV in Fig. 3 is 2.2 kV normalized to 30 μm.

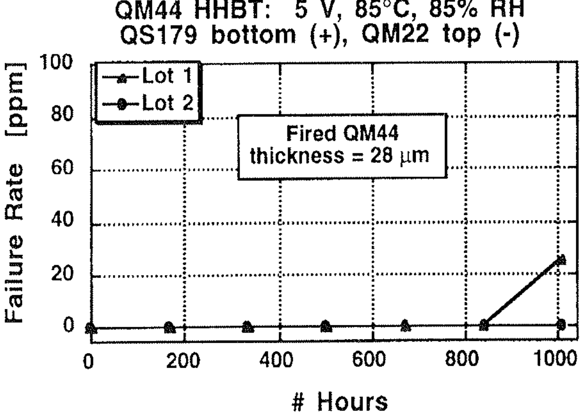


Fig. 4. High humidity biased test results with QM44 (unencapsulated).

High humidity biased test (HHBT) data is presented in Fig. 4. The bottom electrode selected was QS179 Ag-Pt, and the top conductor was QM22 cofired Ag-Pd. Test conditions were 5 V DC, 85°C and 85% relative humidity (RH). A total of 40,000 crossovers were evaluated in the test for each dielectric lot. The line widths were 250 μm, and the dielectric was tested at 28 μm fired thickness. No surface encapsulation was employed. Only one short was detected, at the 1000 hour mark.

Conductors

Excellent conductor adhesion is a key feature of this system. High aged adhesion with the new dielectric is obtained with a variety of standard conductors, as depicted in Fig. 5. The solder employed in Fig. 5 was 62/36/2 Sn/Pb/Ag.

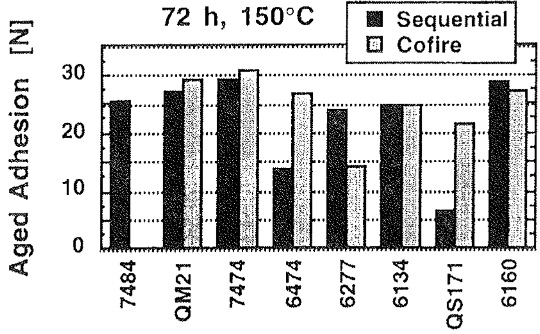


Fig. 5. Soldered aged adhesion of a range of standard conductors over QM44 dielectric. The conductors are 3:1 Ag-Pd (7484, QM21, 7474, 6474), 6:1 Ag-Pd (6277, 6134), Ag-Pt (QS171), and pure Ag (6160). The 7484 was not cofired in this test.

The soldered aged adhesion over QM44 of QM22, a new cofired, 3:1 Ag-Pd composition, is shown in Fig. 6. The adhesion failure mode was solder/conductor separation, indicating superior adhesion of the conductor to the dielectric. The failure rate of this conductor after thermal cycling is shown in Fig. 7. In this test, the standard wire peel geometry was used, but the test was modified to measure electrical continuity instead of adhesion. Three pads were soldered together in a row with a single wire, and each part employed three rows of wires connected together electrically in a daisy chain pattern. Furthermore, the edges of the pads were covered with an organic solder stop in a so-called window-frame geometry /1,5/. Failure was defined as an electrical open. Ten parts were tested, employing a total of 90 pads (30 wires). No failures were observed through approximately 800 thermal cycles.

Thermal cycle data with wire peel geometries can sometimes lead to difficulties in data interpretation if the failure modes don't match those with actual components /6,7/. The failure mode of most concern with multilayer constructions is cracking or divoting into the dielectric layer, a brittle type of failure mode often associated with failure at low numbers of thermal cycles /1,3,5,8/. To be certain that early thermal cycle failures

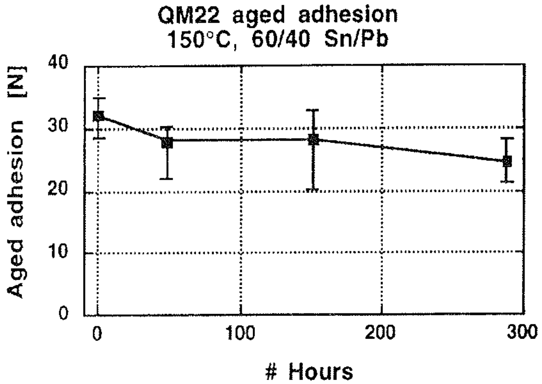


Fig. 6. Aged adhesion (min/max) of QM22 cofired 3:1 Ag-Pd conductor over QM44 dielectric.

associated with dielectric cracking won't occur, the most unambiguous thermal cycle data is obtained with actual soldered components. The reliability after thermal cycling of several electronic components soldered to the QM22 cofire Ag-Pd conductor over the QM44 dielectric was previously published /3/, showing good reliability through 1000 cycles of -40/125°C. Similar thermal cycle data with components soldered to the 7484 sequential fire Ag-Pd conductor over QM44 was also presented previously /1,3/, again showing good performance through 1000 cycles.

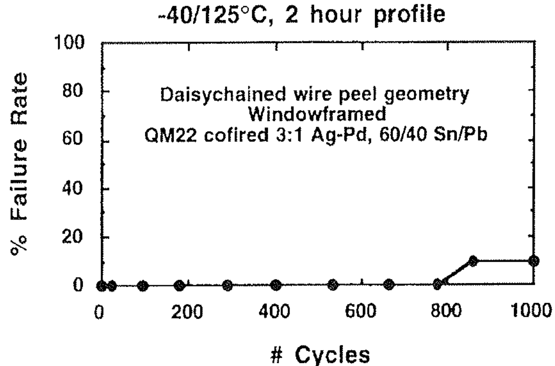


Fig. 7. Thermal cycled reliability of QM22/QM44, using a 3-pad wire peel orientation.

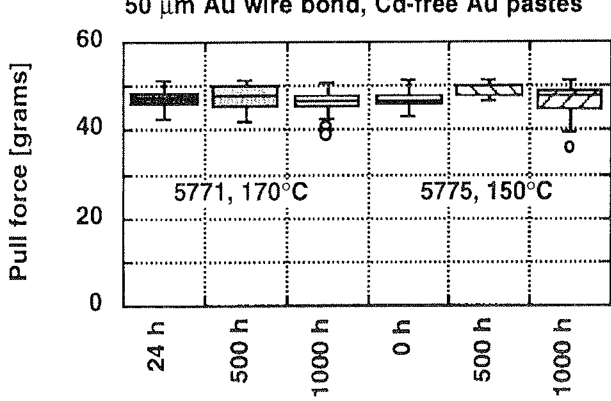


Fig. 8 Wire bond aged adhesion of Au conductors with 50 micron Au wire.

The new dielectric is also compatible with wire bondable gold compositions, including newer Cd-free materials. Wire bond aged adhesion with 50 µm Au and 250 µm Al wire is shown in Figs. 8 and 9, respectively. The data is presented as boxplots, with each box typically representing approximately 30 data points. The median adhesion values are shown at the center of the boxes, with the 25% and 75% points in the distributions at the bottom and top of the boxes, and the extremes of the data shown by the lines from the boxes (open circles are also part of the distributions, but are statistical outliers, and fall outside of the lines. The pull test failure mode after ageing in all cases was 100% wire breaks - failures were either within the wire, or at the heel of the first or second bond sites. No metallization lifts or bond lifts were observed, indicating superior adhesion of the Au pastes to the dielectric, and of the wire to the Au pastes. The reduction in pull strength in Fig. 9 with the 250 µm Al wire is believed to be due to annealing of the Al wire.

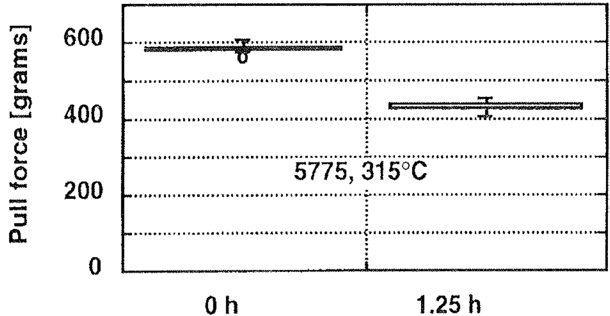


Fig. 9 Wire bond aged adhesion of Au conductor with 250 micron Al wire.

Via Fill

A new via fill material, QM35, was developed to facilitate cofiring in this system. Control of the metal particle size for reduced shrinkage was essential in order to allow cofiring without cracking around the vias. However, since this material must connect Ag-Pt substrate conductor and Ag-Pd top conductor, the via fill must fire sufficiently densely to prevent electrical opens on refiring that can occur due to Kirkendall-type void formation.

The circuit yield in a manufacturing setting with this material was described previously /3/, indicating no opens after a total of 10 firings when connecting Ag-Pt and Ag-Pd materials. Furthermore, preliminary data shows this via fill material to be useful in connecting pure silver and gold conductors, as depicted in Fig.10. The conductors, dielectric, and via fill in Fig.10 were all fired sequentially. The dielectric was printed to a total of 30 µm fired, with 10 µm vias. No opens were obtained through three top Au conductor refirings (four total firings), with approximately 4 ppm opens occurring after 5 refires, and larger amounts of opens occurring only from 10-15 refirings. For circuits that employ wire bondable top Au traces, there might also be resistors and solderable Ag-Pd conductor pads at the top surface, so that the Au prints might be subject to a limited

amount of refiring. The expected refiring is within the ability of the QM35 via fill to connect the Ag and Au lines without electrical opens.

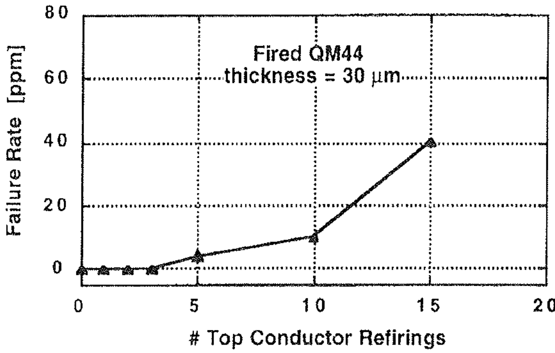


Fig.10 Via fill failure rate (ppm open circuits) connecting Ag and Au conductors.

A second via fill material is available for the system when larger number of metal layers are employed. The QM34 is especially suitable in the inner layers when stacked vias are designed in the circuit, with no cracks and flat via fill topologies obtained through three sets of dielectric/stacked via fill/ conductor prints, which is equivalent to a four metal layer circuit (including the substrate level conductor). The QM34 can also connect Ag-Pd and Ag-Pt (or pure Ag) conductors, but is not suitable for connecting Ag and Au conductors, with opens occurring after the first refire.

Resistors

A new resistor series S100 was developed for the dielectric system. The technology is based on a new hybrid series that features improved power handling and process insensitivity, tighter temperature coefficients of resistivity (TCR), and reduced noise vs. older hybrid resistor series /9/. The resistor series spans 10 Ω/sq to 1 MΩ/sq.

The resistance and hot and cold TCR's for the members are plotted in Fig. 11. The TCR's fall within ± 75 ppm/°C, except for the 10 Ω/sq member which is within 100 ppm/°C. Laser trim stability data of unencapsulated resistors are plotted in Fig.12 after 1000 hours aging at 150°C, 1000 hours at 85°C/85% RH, and after 1000 hours at room temperature (see also /3/ for -50/150°C stability data). Excellent trim stability of less than ± 0.5% average drift was obtained under all ageing conditions.

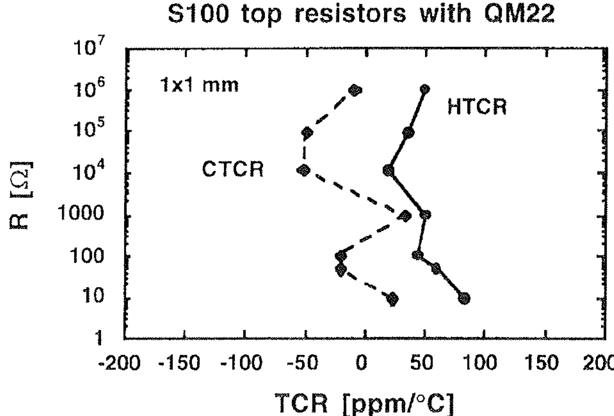


Fig.11. Resistance and TCR values of S100 resistor members over QM44 dielectric.

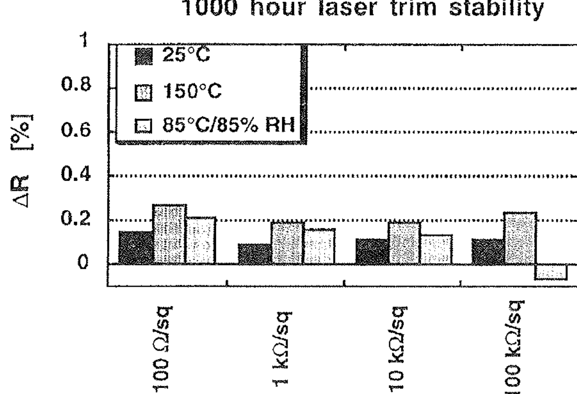


Fig.12. Laser trim stability of S100 resistor series.

SUMMARY AND FUTURE PLANS

A new thick film multilayer system has been developed for applications that require thermal cycle reliability with soldered components. The key feature is a new dielectric material that is tuned for good conductor compatibility, yet has high density for good circuit yield and reliability with only two prints. The dielectric can be cofired with the system via fill and top conductor, which further reduces manufacturing costs. Upcoming enhancements for the system include a set of buried capacitor and resistor materials that will become available (see also ref. /10/). The buried resistors are expected to span a range of 100 Ω to 100 kΩ, with 300 ppm TCR's and ±10% tolerance. A buried capacitor member will be based on barium titanate and will have a dielectric constant of approximately K1300 with X7R temperature characteristics. A pair of relaxor-based capacitor compositions are already commercially available and span a range of K1600-K3900; however, their Y5U temperature characteristics are not suitable for under-the-hood automotive applications.

AGKNOWLEDGMENTS

The authors gratefully acknowledge and thank the following for their useful discussions and technical help: Rudy Bacher, Ken Souders, Lourian Burwell, Keith Dorricott, Judi Stuart, Tom Davenport, Bryan Neve, and Dennis Sabol, all of DuPont Electronic Materials, and Tony Stankavich, John Isenberg, Adam Schubring, Chris Coapman, Chris Paszkiet, Frans Lautzenhiser, Ed Ellis, and D. H. R. Sarma, all of Delco Electronics.

REFERENCES

/1/ R.L. Keusseyan, M.H. LaBranche, and K.W. Hang, *"Thick Film Multilayer Material Systems for Thermal Cycle Applications"*, Proceedings ISHM, Boston, Nov. IS-17,1994, pp.185-190.

/2/ D.H.R. Sarma, F.E. Richter, M.G. McDermott, C.R.S. Needes, C.J. McCormick and D.K. Anderson, *"Multilayer Materials System for Automotive Applications"*, Proceedings ISHM, Los Angeles, California, Oct. 24-26,1995, pp. 497-502.

/3/ M.H. LaBranche, C.J. McCormick, J.D. Smith, C.R.S. Needes, K.W. Hang, J.K. Isenberg, A.W. Schubring, C.R. Coapman, C.A. Paszkiet, F.P. Lautzenhiser, M.E. Ellis, and D. H. R. Sarma, *"Next-Generation Engine Corctrol Modules Using Advanced Multilayer Technology Materials"*, Proceedings ISHM, Minneapolis, Oct. 8-10, 1996, pp. 476-481.

/4/ *Introduction to Ceramics*, 2nd Ed., W.D. Kingery, H.K. Bowen, D.R. Uhlmann, John Wiley & Sons, NY,1976.

/5/ R.L. Keusseyan and J.L. Dilday, *"Barrier Thick Film Approach for the Enhancement of Thermal Cycling Reliability of Soldered Thick Films"*, Proceedings ISHM, Dallan, Texas, Nov. 9-11,1993, pp. 44-49.

/6/ K. Yamamoto, S. Uchida, H. Kojo, H. Hara, Y Yamamoto, B. E. Taylor, and M. H. LaBranche, *"Thermal Cycle Performance of Ag-Bearing Thick Film Conductors for Automotive Applications"*, Proceedings European IEMT, Mainz, April 1-3,1992.

/7/ K. Yamamoto, S. Abou, S. Uchida, H. Kojo, H. Hara, Y Yamamoto, B. E. Taylor, and M. H. LaBranche, *"High-Reliabilily Silver-Bearing Thick Film Conductors for Automotive Applications"*, Proceeding ECTC, San Diego, May 18-20,1992.

/8/ R.L. Keusseyan, P.T. Goeller, L.E. Dellis, J.R. Thrash, T.G. Davenport and R.F. Hazelwood, *"Thermal Cycling of Soldered Thick Films Part I: Theory, and Part 2: Experiment"*, Proceeding ISHM, Chicago, Oct.15-17,1990, pp.190-202.

/9/ A.T. Walker, L.A. Silverman, K.W. Hang, T. Pfeiffer, V.P. Siuta, L.H. Slack, and R.J. Bouchard, *"A New Hybrid Resistor System for* TCR *Control and Process Insensitivity"*, Proceedings ISHM, Dallas, Nov. 9-1 I,1993, pp. 695-699.

/10/ H. Kanda, R.C. Mason, C. Okabe, J.D. Smith and R. Velasquez, *"Buried Resistors and Capacitors for Multilayer Hybrids"*, Proceedings ISHM, Los Angeles, Oct. 24-26, 1995, pp. 47-52.

Marc H. LaBranche,
Cornelius J. McCormick,
Jerome D. Smith,
Roupen L. Keusseyan,
Robert C. Mason,
Mark A. Fahey,
Christopher R. S. Needes
DuPont Electronic Materials,
Research Triangle Park, NC
Kenneth W. Hang
DuPont Electronic Materials,
Experimental Station,
Wilmington DE

The paper was presented by Mr. Alan Buckthorpe

Prispelo (Arrived): 21.9.1998 *Sprejeto (Accepted): 16.11.1998*

MIDEM KONFERENCA - POROČILO
MIDEM CONFERENCE - REPORT

34th INTERNATIONAL CONFERENCE ON MICROELECTRONICS, DEVICES AND MATERIALS

With the Satellite Minisymposium on

SEMICONDUCTOR RADIATION DETECTORS

CONFERENCE '98

September 23. - 25. 1998
HOTEL SAVA
Rogaška Slatina, SLOVENIA

CONFERENCE REPORT

ORGANIZER

MIDEM - Society for Microelectronics, Electronic Components and Materials
Dunajska 10, 1000 Ljubljana, SLOVENIA

CONFERENCE SPONSORS

Ministry of Science and Technology of the Republic of Slovenia
Iskra IEZE Holding d. o. o., Ljubljana, Slovenia
ELES, Ljubljana, Slovenia
STEKLARNA ROGAŠKA d. d., Slovenia
IEEE Slovenia Section
IMAPS Slovenia Chapter

INTERNATIONAL PROGRAMME COMMITTEE

Marko Hrovat, Jožef Stefan Institute, Ljubljana, Slovenia, **Chairperson**
Dejan Križaj, Faculty for Electrical Engineering, Ljubljana, Slovenia, Co**Chairman**
Cor Claeys, IMEC, Leuven, Belgium
Gerhard W. Herzog, Technische Universitat, Graz, Austria
Bruno Cvikl, Faculty for Civil Engineering, Maribor, Slovenia
Slavko Amon, Faculty for Electrical Engineering, Ljubljana, Slovenia
Marija Kosec, Jožef Stefan Institute, Ljubljana, Slovenia
Bojan Jenko, Ministry of Science and Technology of the Republic of Slovenia
Wilhelm Kusian, SIEMENS Corporate Research & Development Department, Munchen, Germany
Peter Panjan, Jožef Stefan Institute, Ljubljana, Slovenia
Stane Pejovnik, National Institute of Chemistry, Ljubljana, Slovenia
Wolfgang Pribyl, SIEMENS EZM, Villach, Austria
Nava Setter, Ecole Polytechnique Federal de Lausanne, Lausanne, Switzerland
Giovanni Soncini, University of Trento, Trento, Italy
Iztok Šorli, MIKROIKS d. o. o. , Ljubljana, Slovenia
Jiri Toušek, Charles University, Prague, Czech Republic
Lojze Trontelj, Faculty for Electrical Engineering, Ljubljana, Slovenia
Anton Zalar, ITPO, Ljubljana, Slovenia
Miloš Simora, Technical University, Košice, Slovakia
Leszek J. Golonka, Technical University, Wroclaw, Poland
Zsolt Vitez, Technical University, Budapest, Hungary

CONFERENCE ORGANIZING COMMITTEE

Meta Limpel, MIDEM, Ljubljana, Slovenia, **Chairperson**
Milan Slokan, MIDEM, Ljubljana, Slovenia
Igor Pompe, Iskra IEZE Holding, Ljubljana, Slovenia
Miloš Komac, Ministry of Science and Technology of the Republic of Slovenia
Rudolf Ročak, MIKROIKS d. o. o., Ljubljana, Slovenia
Iztok Šorli, MIKROIKS d. o. o., Ljubljana, Slovenia

MINISYMPOSIUM ORGANIZING COMMITTEE

The Minisymposium will be organized by the Laboratory for Electron Devices of the Faculty of Electrical Engineering, Ljubljana, Slovenia aided by a minisymposium program committee:
Dejan Križaj and Slavko Amon, Laboratory for Electron Devices, Faculty of Electrical Engineering, University of Ljubljana, Slovenia
Vladimir Cindro and Marko Mikuž, Department for Elementary Particle Physics, Institute Jožef Stefan, Slovenia
Walter Bonvicini and Andrea Vacchi, INFN Trieste and University of Trieste, Italy
Giovanni Soncini and Giorgio Pignatel, IRST Trento and University of Trento, Italy

34th International Conference on Microelectronics, Devices and Materials, MIDEM´98, continued the tradition of annual international conferences organized by MIDEM Society. These conferences have always attracted a large number of Slovene and foreign experts working in these fields. Again this year our scientists had the opportunity to present their work at home to the international public and to meet and discuss trends, news and problems related to their fields of work.

Topics covered by the conference were quite diverse. 55 papers in nine sessions in three days were presented.

Starting this year, the programme of the MIDEM Conference was expanded by the organization of satellite minisymposia. This year **Minisymposium on SEMICONDUCTOR RADIATION DETECTORS** was organized. A special report on this event will be given in the next issue of the Journal.

The work of the Conference was divided into several sessions as follows: Ceramics, Metals and Composites; Device Physics and Modeling; Technology and Devices; Integrated Circuits; Semiconductor Radiation Detectors; Sensors; Optoelectronics; Thick Films and Thin Films. As every year distinguished invited speakers gave an overview presentations as introductions to these sessions. All invited papers are presented in this issue as special contributions.

Some statistical data:

Number of participants: total 72, 21 from abroad

Number of papers published in the Proceedings: total 55, 16 from abroad

Participant countries: Slovenia, Italy, Switzerland, Austria, Germany, France, England and Argentina

Conference Proceedings was published before the Conference and has 354 pages. It can be ordered through MIDEM Society.

For the sake of completeness we here present complete Conference program, as well as the list of participants.

CONFERENCE PROGRAM

WEDNESDAY, SEPTEMBER 23

08:45 WELCOME AND OPENING CEREMONY

09:00 SESSION ON CERAMICS, METALS AND COMPOSITES

CHAIR: M. Kosec

09:00 INVITED PAPER

K. Reichmann, N. Katsarakis, A. Reichmann: Electronically Conductive Perovskite Type Materials

09:45 COFFEE BREAK

10:00 **G. Dražič:** Analytical Electron Microscopy of Grain Boundaries in Advanced Ceramic Materials

10:15 **M. I. Valič, J. Stepišnik:** An Ultrasonic Shear Wave Apparatus and its Applications in Materials Research

10:30 **M. Holzinger, W. Jantscher, I. Rom, W. Sitte, K. Reichmann, B. Trummer, O. Fruhwirth, G. W. Herzog:** Conductivity Relaxation and Oxygen Exchange Experiments on Mixed Conducting Oxides at High Temperatures

10:45 **K. Žužek, P. J. McGuiness, B. Saje, S. Kobe:** Gaseous Interactions With Sm-Fe and Sm-Fe-Ta Inter Metallic Alloys

11:00 **M. Marinšek, K. Zupan, J. Maček:** Improvement of Sintering Conditions in Cofire Processing of SOFC Anode and Interconnect Materials

11:15 **M. Hrovat, S. Bernik, J. Holc:** Evaluation of $SrRuO_3$ as a Possible SOFC Thick Film Cathode

11:30 **M. Pinterič, S. Tomić, J. U. von Schütz:** Transport Properties of Charge-density Wave in the $(2,5(OCH_3)_2DCNQI)_2Li$

12:00 LUNCH

14:30 SESSION ON DEVICE PHYSICS AND MODELLING

CHAIR: S. Amon

14:30 INVITED PAPER

S. Sokolić, S. Amon: Models for Carrier Transport in the Base of npn SiGe HBTs

15:15 **B. Cvikl, D. Korošak, M. Koželj:** Evidence of Interface Charge Density Bias Voltage Dependence of (Ua=300V) Ionized Cluster Beam Deposited Ag and Pb/p-Si(100) Schottky Junctions

15:30 **D. Korošak, B. Cvikl, M. Koželj:** On the Origin of a Possible Disorder Induced Charge Transport in ICB Schottky Structures for Nonzero Acceleration Voltage

15:45 **A. Vercik, A. Faigon:** Currents Modelling for a Metal Oxide Semiconductor Tunnel Diode Pulsed in Inversion

16:00 SESSSION ON TECHNOLOGY AND DEVICES

CHAIR: J. Trontelj

16:00 INVITED PAPER

H. Gugg-Schwaiger: Alcatel Microelectronics 0. 5 μm Mixed CMOS Technology

16:45 COFFEE BREAK

17:00 SESSSION ON TECHNOLOGY AND DEVICES

CHAIR: J. Trontelj

17:00 **J. Černetič**: Development of the 500V Electrolytic Capacitors, Problems and Solutions

17:15 **S. Malnarič, J. Rožman, A. Bukovec, A. Dragoš, B. Požek, N. Marentič, S. Fir, F. Smole, J. Furlan:** Ionization in Metallized Foil Capacitors

17:30 **S. Bernik, A. Tavčar, M. Cergolj, Bui Ai:** ZnO Based Varistors for Medium Voltage Arresters

17:45 **B. Ferk, S. Amon, S. Sokolić:** Analysis of SiGe Heterojunction Bipolar Transistors at Low Temperatures

18:00 **D. Resnik, U. Aljančič, D. Vrtačnik, M. Cvar, S. Amon:** Low Temperature Direct Bonding of Silicon Wafers for Pressure Sensor Application

18:15 SESSSION ON INTEGRATED CIRCUITS

CHAIR: J. Trontelj

18:15 **D. Raič:** Performance Evaluation and Optimization Problems of CMOS Latching Circuits

18:30 **D. Strle:** Low-power, Analog Front-end for Voice Applications

18:45 **S. Starašinič:** CMOS Differential Line Drivers and Receivers

19:00 **J. Trontelj jr., J. Trontelj:** CAD Topology Evaluation Tool for Integrated Current Measurement Magnetic Circuit

20:00 COCKTAIL

THURSDAY, SEPTEMBER 24

08:30 MINISYMPOSIUM ON SEMICONDUCTOR RADIATION DETECTORS TUTORIAL SESSION

CHAIR: D. Križaj

08:30 INVITED PAPER

R. Richter, G. Lutz: Semiconductor Radiation Detector Physics and Structures

09:20 INVITED PAPER

P. Weilhammer: Semiconductor Radiation Detector Devices and Applications

10:10 INVITED PAPER

W. Bonvicini: Semiconductor Radiation Detector Characterization and Measurements

11:00 INVITED PAPER

V. Re: Front End Electronics for Radiation Detectors

12:00 LUNCH

14:30 MINISYMPOSIUM ON SEMICONDUCTOR RADIATION DETECTORS REGULAR SESSION

CHAIR: G. U. Pignatel

14:30 **CMS Silicon Group:** Review of the R&D Program on Silicon Microstrip Detectors in CMS

14:45 **F. Arfelli, V. Bonvicini, A. Bravin, G. Cantatore, E. Castelli, M. Fabrizioli, R. Longo, A. Olivo, S. Pani, D. Pontoni, P. Poropat, M. Prest, L. Rigon, F. Tomasini, G. Tromba, A. Vacchi, E. Vallazza:** A Multi-layer Silicon Microstrip Detector for Single Photon Counting Digital Mammography

15:00 **T. Mali, V. Cindro, M. Mikuž, R. Richter:** Effect of Cutting Distance on Noise of Silicon Microstrip Detectors

15:15 **M. Boscardin, L. Bosisio, N. C. Barnea, G. F. Dalla Betta, L. Ferrario, G. U. Pignatel, M. Zen, N. Zorzi:** First Results on Double-sided AC-coupled Silicon Strip Detectors

15:30 **M. K. Gunde, V. Cindro, M. Mikuž, E. N. Orlowska:** Annealing of Infrared Active Defects in Neutron-irradiated Silicon Samples

15:45 **D. Križaj, D. Vrtačnik, S. Amon:** Configurations of JFET and Detector on High-resistivity Silicon Wafer

16:00 **D. De Venuto, F. Corsi:** Investigation of Radiation Damages in Analogue Front-end of a Pixel Detector

16:15 **R. Turchetta, Y. Hu, C. Colledani, V. Frick, A. Loge, Y. Zinzius:** Low-noise Mixed Mode VLSI ASICs for Hybrid VLSI Radiation Detectors

16:30 **A. Vacchi:** The NINA Experiment: A Satellite Born Silicon Telescope for the Study of the Isotopic Composition of Cosmic Rays

16:45 **R. Della Marina:** Design and Production of Silicon Radiation Detectors for the Future High-energy Physics Experiments, An Industrial Point of View

17:00 COFFEE BREAK

17:15 SESSION ON SENSORS

CHAIR: M. Maček

17:15 **M. Maček:** Polysilicon Microbolometer

17:30 **U. Aljančič, K. Požun, D. Resnik, D. Vrtačnik, M. Topič, F. Smole, J. Furlan:** A Capacitive Humidity Porous Silicon Sensor

17:45 **M. Pavlin, S. Šoba, D. Belavič:** Cheap ASICs vs. Discrete Electronics in Sensor Applications

18:00 Visit to the GLASS FACTORY ROGAŠKA SLATINA

20:00 CONFERENCE DINNER

FRIDAY, SEPTEMBER 26

08:30 SESSION ON OPTOELECTRONICS

CHAIR: J. Furlan

08:30 INVITED PAPER

M. Topič, F. Smole: Thin Film Color Detectors Based on Amorphous Silicon

09:15 **Ž. Gorup, J. Furlan, F. Smole:** Influence of Tunneling Charge Carriers on Forward Characteristics of P^+N^+ a-Si:H Junction

09:30 **M. Vukadinović, F. Smole, M. Topič, J. Furlan:** Inclusion of the Trap-assisted Tunnelling Mechanism in the a-Si:H Heterostructures Numerical Modelling

09:45 **K. Brecl, F. Smole, J. Furlan:** Comparison of Conventional and Thin Film Multilayer Solar Cell Structures

10:00 **D. Vrtačnik, D. Križaj, D. Resnik, U. Aljančič, S. Amon:** Ultraviolet-enhanced Sensitivity of Silicon Photodiode

10:15 COFFEE BREAK

10:30 SESSION ON THICK FILMS

CHAIR: M. Hrovat

10:30 INVITED PAPER

M. H. LaBranche, C. J. McCormick, J. D. Smith, R. L. Keusseyan, R. C. Mason, M. A. Fahey, C. R. S. Needes, K. W. Hang: Next-generation, Advanced Thick Film Multilayer System

11:15 **S. Maček, D. Ročak, S. Mojstrovič:** Evaluation of Thick Film Conductor and Dielectric Paste Developed for AlN Substrates Application Used with Resistor Paste of Standard Composition

11:30 **K. Bukat, B. Smejda:** Solder Paste for "Fine-pitch" Technology

11:45 **D. Belavič, M. Pavlin, M. Hrovat:** Evaluation of Thick Film Materials for Diffusion Patterning – Preliminary Results

12:00 **M. Hrovat, J. Holc, Z. Samardžija, D. Belavič:** Characterization of "Equilibrated" Thick Film Resistors

12:15 **I. Šorli, D. Ročak, J. F. Plut, R. Ročak, B. Praček:** Microwave Plasma Cleaning Influence on Chip Wire Bonding Quality on Hybrid Circuits

12:30 COFFEE BREAK

12:45 SESSION ON THIN FILMS

CHAIR: P. Panjan

12:45 M. K. Gunde, M. Maček: Infrared Spectroscopic Characterization of Silicon Nitride and Oxynitride Films Produced by Plasma-enhanced Chemical Vapour Deposition

13:00 **P. Panjan, B. Zorko, B. Navinšek, A. Zalar, M. Čekada:** Standard Reference Materials (SRM) for Compositional Depth Profiles of Transition Metal Oxide and Nitride Thin Films with Different Chemical Composition

13:15 **J. Kovač, L. Gregoratti, S. Guenther, M. Marsi, M. Kiskinova:** A Spectromicroscopy Study of the Ni/Si-oxide/Si Interface

13:30 **M. Mozetič, A. Zalar, I. Arčon, R. Prešeren:** Characterization of Copper Aluminide Thin Films

13:45 **L. Čakare, B. Malič, M. Kosec:** Characterization of Thick PZT 53/47 Films Prepared by Sol-gel Processing

14:00 CLOSING OF THE CONFERENCE

List of Participants - MIDEM´98 CONFERENCE

	NAME	INSTITUTION - COMPANY	PLACE	ZIP	ADDRESS
1	ALJANČIČ UROŠ	FAKULTETA ZA ELEKTROTEHNIKO	LJUBLJANA	1000	TRŽAŠKA 25
2	AMON SLAVKO	FAKULTETA ZA ELETROTEHNIKO	LJUBLJANA	1000	TRŽAŠKA 25
3	BELAVIČ DARKO	HIPOT HYB	ŠENTJERNEJ	8310	TRUBARJEVA 7
4	BERNIK SLAVKO	INŠTITUT JOŽEF STEFAN	LJUBLJANA	1000	JAMOVA 39
5	BONVICINI VALTER	INFN-TRIESTE	TRIESTE	I-34012	PADRICIANO 99
6	BRECL KRISTIJAN	FAKULTETA ZA ELEKTROTEHNIKO	LJUBLJANA	1000	TRŽAŠKA 25
7	BUCKTHORPE ALAN	DUPONT	BRISTOL ENGLAND		COLDHARBOURLANE
8	CIANO BOSISIO	UNIVERSITA DI TRIESTE AND INFN	TRIESTE	I-34127	VIA VALERIO 2
9	CORSI FRANCESCO	POLITECNICO DI BARI	BARI	I-70125	VIA ORABONA 4
10	CVIKL BRUNO	UNIV. OF MARIBOR, FG	MARIBOR	2000	SMETANOVA 17
11	DE VENUTO DANIELA	UNIVERSITYOF LECCE-FAC. ENG.	LECCE	I-73100	VIA PER MONTERONI
12	DRAŽIČ GORAN	INŠTITUT JOŽEF STEFAN	LJUBLJANA	1000	JAMOVA 39
13	FERK BRANKO	FAKULTETA ZA ELEKTROTEHNIKO	LJUBLJANA	1000	TRŽAŠKA 25
14	FURLAN JOŽE	FAKULTETA ZA ELEKTROTEHNIKO	LJUBLJANA	1000	TRŽAŠKA 25
15	GERHARD HERZOG	TU GRAZ	GRAZ	A-8010	STREMAYRGASSE 16
16	GIRALDO VLADIMIR	JOŽEF STEFAN INSTITUTE	LJUBLJANA	1000	JAMOVA 39
17	GORUP ŽARKO	FAKULTETA ZA ELEKTROTEHNIKO LJ.	LJUBLJANA	1000	TRŽAŠKA 25
18	GUGG-SCHWAIGER HANS	ALCATEL MICROELECTRONICS	MUNCHEN	D-81925	ARABELLA STRASSE 4
19	HREN JOHN	INŠTITUT JOŽEF STEFAN	LJUBLJANA	1000	JAMOVA 39
20	HROVAT MARKO	INŠTITUT JOŽEF STEFAN	LJUBLJANA	1000	JAMOVA 39
21	JANTSCHER WOLFGANG	GRAZ UNIVERSITY OF TECHNOLOGY	GRAZ	A-8010	RECHBAUERSTR. 12
22	KLANJŠEK GUNDE MARTA	NATIONAL INSTITUTE OF CHEMISTRY	LJUBLJANA	1000	HAJDRIHOVA 19
23	KOBE SPOMENKA	INŠTITUT JOŽEF STEFAN	LJUBLJANA	1000	JAMOVA 39
24	KOROŠAK DEAN	FACULTY OF CIV.ING. UNIVERSITY OF MARIBOR	MARIBOR	2000	SMETANOVA 17
25	KOSEC MARIJA	INŠTITUT JOŽEF STEFAN	LJUBLJANA	1000	JAMOVA 39
26	KOVAČ JANEZ	ITPO	LJUBLJANA	1000	TESLOVA 30
27	KRAMBERGER GREGOR	INŠTITUT JOŽEF STEFAN	SLOVENIJA	1000	JAMOVA 39
28	KRIŽAJ DEJAN	FAKULTETA ZA ELEKTROTEHNIKO LJ.	LJUBLJANA	1000	TRŽAŠKA 25
29	LUSITANI ANTONO	DUPONT	COLOGNO MONZESE	I-20093	VIA VOLTA 16
30	MALI TADEJ	INŠTITUT JOŽEF STEFAN	LJUBLJANA	1000	JAMOVA 39
31	MALNARIČ SAMOEL	FACULTY OF ELECTRONIC ENGINEERING	LJUBLJANA	1000	TRŠAŠKA 25
32	MARINŠEK MARJAN	FKKT	LJUBLJANA	1000	AŠKERČEVA 5
33	MARJAN MAČEK	FACULTY OF ELECTRONIC ENGINEERING	LJUBLJANA	1000	TRŽAŠKA 25
34	MAČEK SREČO	INŠTITUT JOŽEF STEFAN	LJUBLJANA	1000	JAMOVA 39
35	MCGUINESS PAUL	INŠTITUT JOŽEF STEFAN	LJUBLJANA	1000	JAMOVA 39
36	MIKUŽ MARKO	JOŽEF STEFAN INSTITUTE	LJUBLJANA	1000	JAMOVA 39
37	MONIKA JENKO	IMT	LJUBLJANA	1000	LEPI POT
38	MOZETIČ MIRAN	ITPO	LJUBLJANA	1000	TESLOVA 30
39	OLIVO ALESSANDRO	INFN	TRIESTE	I-34100	AREA DI RIC.-PADRICIANO 99
40	PANJAN PETER	INŠTITUT JOŽEF STEFAN	LJUBLJANA	1000	JAMOVA 39
41	PAVLIN MARKO	HIPOT-RDG	ŠENTJERNEJ	8310	TRUBARJEVA 7
42	PIGNATEL GIORGIO	UNIVERSITY OF TRENTO	MESIANO TN	I-38050	MATERIALS ENG DEPT.
43	PINTERIČ MARKO	UNIVERSITY OF MARIBOR	MARIBOR	2000	SMETANOVA 17
44	PIPEROV STEFAN	HUMBOLDT UNIVERSITY-BERLIN AND CERN	GENEVA	CH-1211	CERN/EP
45	RAIČ DUŠAN	FAKULTETA ZA ELEKTROTEHNIKO LJ.	LJUBLJANA	1000	TRŽAŠKA 25
46	RE VALERIO	UNIVERSITY OF PAVIA	PAVIA	I-27100	VIA FERRATA 1
47	REICHMANN KLAUS	GRAZ UNIV. OF TECHNOLOGY	GRAZ	A-8010	STREMAYRGASSE 16/III
48	RESNIK DRAGO	FAKULTETA ZA ELEKTROTEHNIKO	LJUBLJANA	1000	TRŽAŠKA 25
49	RICHTER R.	MPI-MUNICH	MUNICH	D-81245	MPI-HLL,
50	ROČAK DUBRAVKA	INŠTITUT JOŽEF STEFAN	LJUBLJANA	1000	JAMOVA 39
51	SITTE WARNER	GRAZ UNIVERSITY OF TECHNOLOGY	GRAZ	A-8010	RECHBAUERSTR.12
52	SMOLE FRANC	FAKULTETA ZA ELEKTROTEHNIKO	LJUBLJANA	1000	TRŽAŠKA 25
53	STARAŠINIČ SLAVKO	FACULTY OF ELECTRONIC ENGINEERING	LJUBLJANA	1000	TRŽAŠKA 25
54	STRLE DRAGO	UNIVERSITY OF LJUBLJANA	LJUBLJANA	1000	TRŽAŠKA 25
55	TOPIČ MARKO	FAKULTETA ZA ELEKTROTEHNIKO	LJUBLJANA	1000	TRŽAŠKA 25
56	TRONTELJ JANEZ	FACULTY OF ELECTRONIC ENGINEERING	LJUBLJANA	1000	TRŽAŠKA 25
57	TRONTELJ JANEZ	FAKULTETA ZA ELEKTROTEHNIKO	LJUBLJANA	1000	TRŽAŠKA 25
58	TURCHETTA RENATO	LEPSI	STRASBOURG	F-67037	23 RUE DU LOESS
59	VACCHI ANDREA	ZNFN	TRIESTE	I-34012	PADRICEANO 99
60	VALIČ MARKO	FAKULTETA ZA POMORSTVO IN PROMET	PORTOROŽ	6320	POT POMORŠČAKOV 4
61	VERCIK ANDRES	UNIVERSITY OF BUENOS AIRES	BUENOS AIRES	AR-1069	PASEO COLON 850
62	VITE DAVIDE	UNIVERSITY OF GENEVA	GENEVA	CH-1211	24 GUZI ERNEST-AU
63	VRTAČNIK DANILO	FAKULTETA ZA ELEKTROTEHNIKO	LJUBLJANA	1000	TRŽAŠKA 25
64	VUKADINOVIČ MIŠO	FAKULTETA ZA ELEKTROTEHNIKO	LJUBLJANA	1000	TRŽAŠKA 25
65	WEILHAIMMER P.	CERN	SWITZERLAND	1211	GENEVA 23
66	ZUPAN KLEMENTINA	FKKT	LJUBLJANA	1000	AŠKERČEVA 5
67	ŠOBA STOJAN	HIPOT HYB	ŠENTJERNEJ	8310	TRUBARJEVA 7
68	ŠORLI IZTOK	MIKROIKS	LJUBLJANA	1000	DUNAJSKA 5
69	ŽONTAR DEJAN	JOŽEF STEFAN INSTITUTE	LJUBLJANA	1000	JAMOVA 39
70	ŽUŽEK KRISTINA	INŠTITUT JOŽEF STEFAN	LJUBLJANA	1000	JAMOVA 39
71	ČAKARE LAILA	INŠTITUT JOŽEF STEFAN	LJUBLJANA	1000	JAMOVA 39
72	ČERNETIČ JOSIPINA	ISKRA ELEKTROLITI	MOKRONOG	8230	STARI TRG 36

PREDSTAVLJAMO PODJETJE Z NASLOVNICE
REPRESENT OF COMPANY FROM FRONT PAGE

WHO ARE WE?

Iskra VARISTOR is a manufacturing company producing a wide range of ZnO varistors on the base of our own knowledge and research.

The beginnings of the company date back to the early 1970, when in the research laboratory a great deal of energy and enthusiasm was invested in the development of the ZnO varistor for an over voltage protection. The production started in 1980.

From the very beginning it has been our goal to offer varistors at reasonable costs. The chosen way has proven to be the right one. This concept, together with the working ethics of all employees and the confidence of our customers, has allowed the small company to enter all major world markets.

Our production complies with the IEC in VDE standards, we are holders of the UL, CSA and ISO 9003 Quality Certificates. We sell our products all over the world; the export is done mainly through a distributors' net.

Although we offer a whole range of low, medium and high voltage varistors; we are currently very much focused especially to the high energy field. Our advantages are:
- flexibility
- products designed according to the customers' specific requests and requirements
- short lead times
- competitive prices

Throught the requests and requirements of customers and our many years of experience, we have developed and applied technologies to our manufacturing processes and our products. The quality assurance policy of Iskra VARISTOR is based on the continious improvement of all elements involved in the sales process.

Quality is a tradition for Iskra VARISTOR and has strong roots in the company's operating philosophy.

And it shall always stay in the future – for our customers we always want to be one step ahead of the general development.

ISKRA VARISTOR WILL TAKE CARE OF PROGRESS FOR YOU!

General Data

Varistors, also called VDR (Voltage Dependent Resistors), show a high degree of non-linearity between their resistance value and the applied voltage.

A metal oxide varistor is a voltage dependent, symmetrical non-linear resistor. The current through the varistor is exponentially dependent of voltage. Dependence is expressed with the equation $I=K \cdot V^{\alpha}$

Where I = current through the varistor
V = voltage on the varistor
K = a material constant
α = non-linear index

The varistor curve is steeper the higher the value of the non-linear index. It is intended for safeguarding sensitive electronic components against voltage pulses of various sources. The characteristics enable them to protect against high transient voltage spikes to meet anticipated loads. They are also used for stabilizing higher DC voltages. Should a high-voltage pulse occur, the varistor resistance shifts from a very high value to a level of good conductance instantly. The varistor absorbs the energy of the pulse and decreases voltage to a safe level thereby, protecting the electronic component against damages.

Construction of the Disk Varistors with the Radial Terminals

Silver electrodes are placed on both sides of the tablet shaped varistor ceramics. Contact wires are soldered to these electrodes. The tablet is then coated with protection layer, necessary for insulation and safeguarding against mechanical and chemical influences.

Construction of the High Energy Varistors

Electrodes are soldered on both sides of the varistor tablet, connected to external terminals. This tablet is then properly encapsulated.

Standard Dimensions of the Disk Varistors with the Radial Terminals

The basic design of the metal oxide varistors is a disk with radial wire terminals. Standard range covers five module sizes: K5, K7, K10, K14 and K20.

The numerals indicate the diameters of varistor disks in millimeters.

Available on request:
- non-standard voltages V_{RMS}, V_{DC}, V_N
- non-standard tolerance of nominal voltage V_N
- preformed leads
- non-standard leads spacing and length

Application Areas

- Telecommunications
- Rectifier Electronics
- Power Electronics
- Measuring and Control Devices
- Processing Systems
- Computer Equipment
- Industrial Electronics
- Medical Devices
- Household Appliances
- Fun Electronics
- Automotive Electronics
- Switching Techniques
- Electric Automobiles
- Electric Vehicles
- Traffic Controllers
- Test Equipment
- Instrumentation

PRODUCT SURVEY

Disk Varistors with Radial Therminals

	K 5	K 5 P	K 7	K 7 P	K 10	K 10 P	K 14	S 14 P	K 20	K 20 P
Varistor Element Diameter	5 mm	5 mm	7 mm	7 mm	10 mm	10 mm	14 mm	14 mm	20 mm	20 mm
Varistor Voltage V_N	18 V ... 560 V	18 V ... 68 V	18 V ... 560 V	18 V ... 68 V	18 V ... 1,200 V	18 V ... 68 V	18 V ... 1,200 V	390 V, 430 V	18 V ... 1,800 V	205 V ... 750 V
Surge Current I_{max} (8x20μs)	0.4 kA	0.25 kA	1.2 kA	0.5 kA	2.5 kA	1.0 kA	4.5 kA	5.5 kA	6.5 kA	8.0 kA
Energy Absorption W_{max} (2ms)	11 J	3 J	27 J	6.5 J	100 J	13 J	190 J	75 J	420 J	261 J
Average Power Dissipation P_{max}	0.10 W	0.02 W	0.25 W	0.05 W	0.40 W	0.10 W	0.60 W	0.60 W	1.00 W	1.00 W

High Energy Varistors and High Energy Suppressor Disks

	E 25 E 32 E 40	HE 25 HE 32	D 32 LE	S 40 LE	D 25 D 32 D 40	S 40
Varistor Voltage V_N	205 V...1,200 V	205 V ... 1,200 V	205 V ... 1,800 V	205 V ... 1,800 V	205 V ... 1,800 V	205 V ... 1,800 V
Surge Current I_{max} (8x20μs)	15 kA ... 40 kA	15 kA, 25 kA	25 kA	40 kA	15 kA ... 40 kA	40 kA
Energy Absorption W_{max} (2ms)	425 J ... 1,230 J	425 J ... 820 J	1,200 J	1,350 J	425 J ... 1,850 J	1,850 J
Average Power Dissipation P_{max}	1.0 W ... 1.4 W	1.0 W, 1.2 W	1.2 W	1.4 W	1.0 W ... 1.4 W	1.4 W

SPECIAL HIGH ENERGY VARISTOR VERSIONS

VARISTORS FOR **SPD**

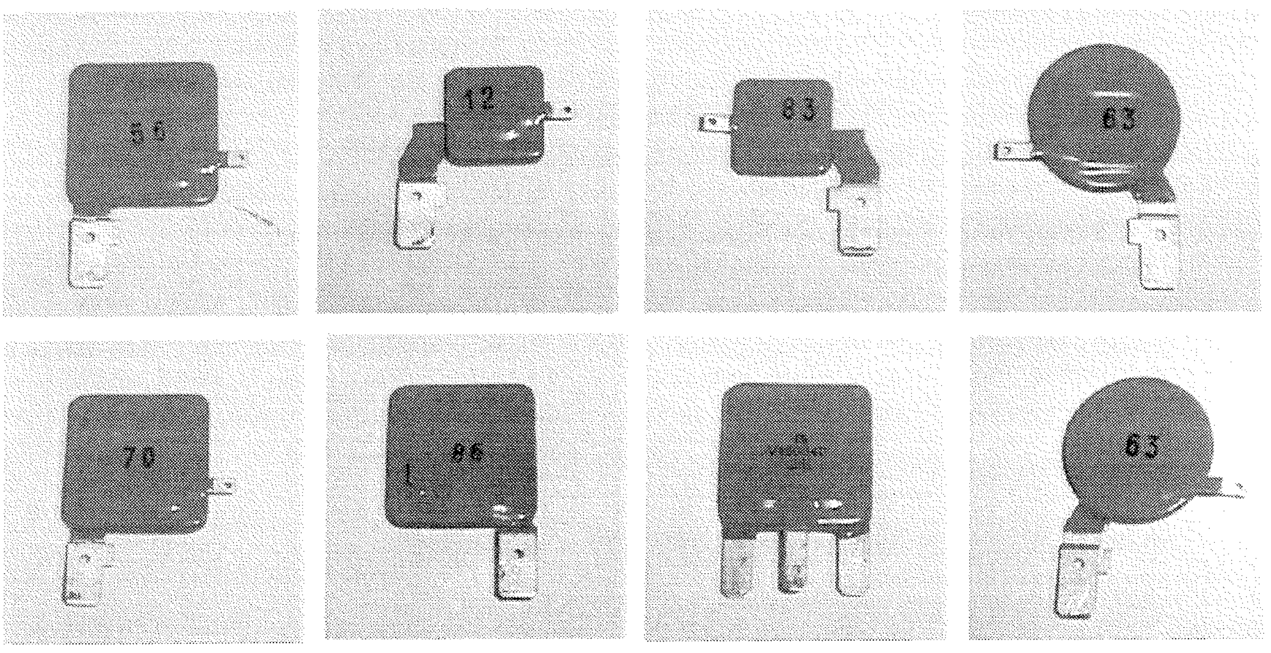
Iskra VARISTOR High Energy Programme includes a wide range of different dimensions, coatings and voltages. High Energy varistors can be used for the surge protective device - SPD. SPDs are devices which mainly consist of voltage dependent resistors such as varistors and isolated spark gaps. SPDs are used to protect other equipment and systems against excessive overvoltages class C or D (according to E DIN VDE 0675 Part 6/11.89).

- SPD for use in Fixed building installations (class C)
- SPD for use at end in main sockets (class D)
- SPD for use in equipment

All SPDs for power supply use which are equiped with a varistor are fitted with an integral disconnector which disconnects the SPD from the mains in the event of a fault.

This disconnector responds to the heat generated by the faulty varistor and trips the SPD at the certain temperatures. The disconnector is to disconnect the faulty SPD from the mains quickly enough to prevent the risk of a fire. The correct function of the thermic disconnector can be checked by a simulated overload of the SPD.

All ISKRA VARISTOR varistors are checked to withstand this overload test and perform the disconnection. All contacts are made of copper to enable good heat transfer to the disconnection device.



Data for some varistor elements:

Type	V_{RMS}	V_{DC}	I_{NOM}	I_{MAX}	$V_{C(5kA)}$	V_C	P_{MAX}	W_{MAX}	C
V275DSM40	275 V	350 V	15 kA	40 kA	1000 V	710 V (300 A)	1,4 W	565 J	2,9 nF
V275DSM32	275 V	350 V	10 kA	25 kA	1000 V	710 V (200 A)	1,2 W	370 J	2,0 nF

V_{RMS} Maximum continuous sinusoidal RMS voltage (50-60Hz) which may be applied.

V_{DC} Maximum continuous DC voltage which may be applied.

I_{NOM} Nominal discharge current is the peak value of the discharge current of 8/20μs waveform for which the varistor is rated. In this case varistor must withstand the nominal discharge current for 20 times without any deterioration of the functioning features.

I_{MAX} The maximum current with a varistor voltage change of less than $\pm$10% when one impulse of 8/20 μs is applied.

$V_{C(5kA)}$ The voltage protection level is the peak value of the voltage on the varistor at 5kA 8/20μs.
V_C Maximum clamping voltage is a residual voltage when a current impulse of specified amplitude and waveform (8/20μs) is applied.
P_{MAX} The maximum power applied within specified ambient temperature.
W_{MAX} The maximum energy absorbed with a varistor voltage change of less than ±10% when one impulse of 2 ms is applied.
C Typical values measured at a test frequency of 1kHz.

SPECIAL HIGH ENERGY VARISTOR VERSIONS

WHERE TO USE THEM?

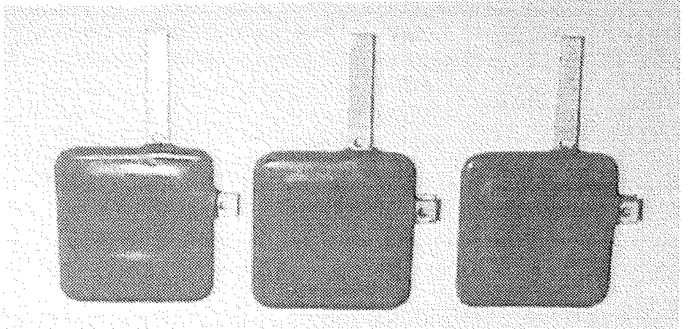
PARALLEL CONNECTION

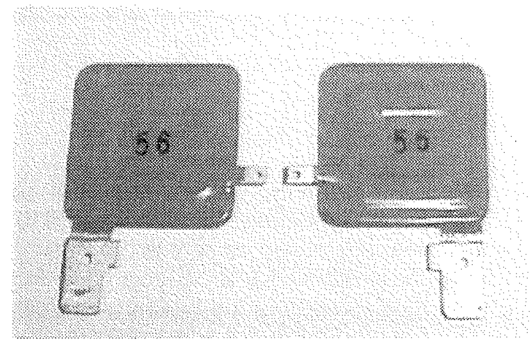
Applications may require higher peak currents and energy dissipation than the high energy series can supply individually. When this occurs, the logical alternative is to examine the possibility of paralleling varistors.

Fortunately, all our varistors have a prominent series-resistance at high current levels that make paralleling possible. Even so the best way is to match the varistors in our factory.

We have a few applications where we need to match two, three or even five varistors. With special tehnique of matching we can provide good current sharing.

If you use five varistors in parallel connection, you can make an SPD that can protect the low voltage network of an installation against direct effect of lightnings. In that case the SPD can withstand a 15kA-10/350 μs lightning impulse (similar to the effect of a direct strike on the building) and because you don't need to use gaps, there is no follow current.





Type	V_{RMS}	V_{DC}	I_{NOM}	I_{MAX}	$V_{C(5kA)}$	V_C	P_{MAX}	W_{MAX}	C
V275DSM70	275 V	350 V	25 kA	70 kA	1000 V	710 V (400 A)	2,6 W	1000 J	5,4 nF
V275DSM150	275 V	350 V	70 kA	150 kA	1000 V	710 V (1 kA)	1,2 W	2200 J	14,5 nF

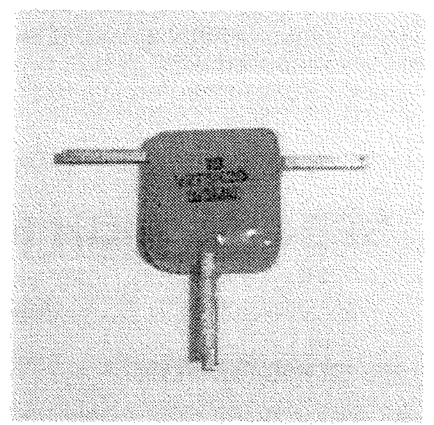
V_{RMS} Maximum continuous sinusoidal RMS voltage (50-60Hz) which may be applied.
V_{DC} Maximum continuous DC voltage which may be applied.
I_{NOM} Nominal discharge current is the peak value of the discharge current of 8/20μs waveform for which the varistor is rated. In this case varistor must withstand the nominal discharge current for 20 times without any deterioration of the functioning features.
I_{MAX} The maximum current with a varistor voltage change of less than ±10% when one impulse of 8/20 μs is applied.
$V_{C(5kA)}$ The voltage protection level is the peak value of the voltage on the varistor at 5kA 8/20μs.
V_C Maximum clamping voltage is a residual voltage when a current impulse of specified amplitude and waveform (8/20μs) is applied.
P_{MAX} The maximum power applied within specified ambient temperature.
W_{MAX} The maximum energy absorbed with a varistor voltage change of less than ±10% when one impulse of 2 ms is applied.
C Typical values measured at a test frequency of 1kHz.

SINGLE PHASE LINE SURGE PROTECTION

a) simple power supply protection using only one varistor between phase conductor and neutral conductor.

b) power supply protection using three varistors between all three lines phase-neutral, neutral-ground, phase-ground.

c) Iskra VARISTOR has found an effecftive solution for protection against the overvoltage on single phase line.



We´ve made a **block** of three varistors (instead of using three varistors separately) which saves time and space. Additionally it also enables you to make – and this is the major advantage – a thermal fuse with two external springs.

V275K20S/3M

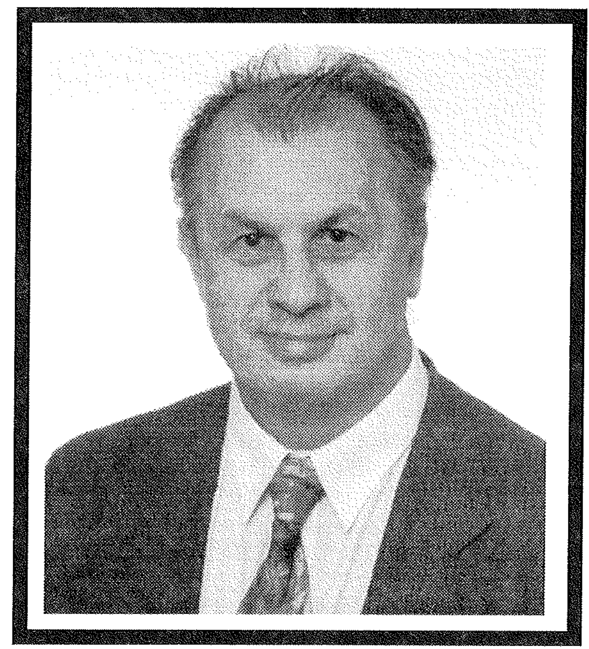
Type	V_{RMS}	V_{DC}	I_{NOM}	I_{MAX}	$V_{C(5kA)}$	V_C	P_{MAX}	W_{MAX}	C
V275K20S/3M	275 V	350 V	3 kA	10 kA	1200 V	710 V (125 kA)	1 W	155 J	930 nF

V_{RMS} Maximum continuous sinusoidal RMS voltage (50-60Hz) which may be applied.
V_{DC} Maximum continuous DC voltage which may be applied.
I_{NOM} Nominal discharge current is the peak value of the discharge current of 8/20μs waveform for which the varistor is rated. In this case varistor must withstand the nominal discharge current for 20 times without any deterioration of the functioning features.
I_{MAX} The maximum current with a varistor voltage change of less than $\pm$10% when one impulse of 8/20 μs is applied.
$V_{C(5kA)}$ The voltage protection level is the peak value of the voltage on the varistor at 5kA 8/20μs.
V_C Maximum clamping voltage is a residual voltage when a current impulse of specified amplitude and waveform (8/20μs) is applied.
P_{MAX} The maximum power applied within specified ambient temperature.
W_{MAX} The maximum energy absorbed with a varistor voltage change of less than $\pm$10% when one impulse of 2 ms is applied.
C Typical values measured at a test frequency of 1kHz.

Iskra VARISTOR, d.o.o.
Stegne35
1000 Ljubljana
Slovenia
Tel: + 386/61 151 15 98
Fax: + 386/61 151 21 73
Home page: http//www.iskra-varistor.si
E-mail:info@iskra-varistor.si

MIDEM IN NJEGOVI ČLANI
MIDEM SOCIETY AND ITS MEMBERS

Umrl je



Ervin Pirtovšek

Vsem članom društva Midem in ostalim znancem sporočamo, da je nenadoma umrl gospod Ervin Pirtovšek dipl. ing., dolgoletni in prizadevni član društva.

Ervin se je rodil leta 1942 v Slovenj Gradcu. Gimnazijo je obiskoval v Ravnah na Koroškem. Na univerzi v Ljubljani je diplomiral iz fizike - meteorologije. Leta 1970 se je zaposlil v razvojnem oddelku za avtoelektriko v Iskrinem Zavodu za avtomatizacijo na Tržaški cesti v Ljubljani.

V letu 1976 se je zaposlil v razvojno-tehničnem področju v tedanji Iskri-Elementi v Stegnah v Ljubljani in kmalu postal vodja razvoja. Prizadeval si je za ustanavljanje razvojnih oddelkov v takratnih temeljnih organizacijah proizvajalcev elementov, za njihovo sodelovanje in skupen nastop, kot tudi za povezavo z drugimi razvojnimi oddelki v Iskri ter za sodelovanje z univerzama in razvojno-raziskovalnimi zavodi – inštituti. V imenu Iskre Elementi, kasneje Iskre IEZE in razvojnih oddelkov podjetij, ki so delovala v njenem okviru, je navezoval stike z Raziskovalno skupnostjo in kasneje z Ministrstvom za znanost in tehnologijo. Uspešno je pomagal pri uvajanju projektnega pristopa in prijavi razvojnih projektov. Razvojne dosežke je znal tudi primerno objaviti.

V času prestrukturiranja se je morala reorganizirati tudi razvojna dejavnost. Leta 1992 je dotedanjo razvojno enoto registriral kot raziskovalno-razvojni inštitut Iskra RRI IEZE, ki je še nadalje skrbel za čim boljše sodelovanje med razvoji posameznih podjetij in kakovost prijav na razpisih MZT.

Neusmiljena smrt je nepričakovano prekinila njegovo delo.

Vsi, ki smo z Ervinom sodelovali, smo ga imeli radi. Pogrešali ga bomo in se ga bomo hvaležno spominjali.

Igor Pompe
Aleševčeva 4, Ljubljana

VESTI - NEWS

News from AMS

Sensational participation of Austria in Nasa mission: chips of **Austria Mikro Systeme International AG** are flying to Mars

The Styrian semiconductor manufacturer Austria Mikro Systeme Int. AG is represented by two chips as part of the Nasa mission "New Millennium Deep-Space 2" to Mars which started yesterday night from Cap Canavaral. The mission is supposed to research the density of water and ice on Mars in order to provide information about possible life on the planet.

The space capsule Mars Polar Lander will reach the red planet in December 1999 after a flight of approximately one year. Two measuring systems the so called "microprobes" are the size of a football and equipped with detectors. They will be cast off the capsule shortly before the impact. Both microprobes are identical and consist of two linked parts. The front part, the so called Fore-Body, will penetrate the surface of the planet whereas the back part, the so called Aft-Body, will remain on the surface after the impact. This way the front part will sample information from the rock as to the nature and the structure of the surface of Mars and will pass it on to the back part, which in turn transmits the signals by wireless.

The Austria Mikro Systeme Int. AG chips are constructed as application specific integrated circuits, the so called ASICs and they each will take over an important function in the front part of the measuring system during this "extra-terrestrial project". Both ASICs are put into application in the so called Power Microelectronics Unit (PMEU), which is responsible for the entire power supply of the microcomputers as well as for the measuring systems in the Fore-Body. One of the chips is in charge of the control system of the power supply and will optimize the power consumption. The chip was designed to be suitable for power supplies up to 50 volts in order to avoid requiring additional power-consuming switching units. Austria Mikro Systeme's successful "High Voltage-process" made this possible. The other chip's function is to steer the linear control and the command functions in the PMEU, as well as to coordinate the switching on and off of the measuring instruments.

The optimization of energy is of top priority to ensure the success of the Mars mission since the total supply is limited to 50 hours. This fact makes the important functions of both chips very clear. It was an additional challenge for this internationally active Austrian company to design the chips so that they could withstand an impact on the surface of Mars at a speed of 700 km an hour, and tolerate changes in temperature between +50 °C and -120 °C.

For further inquiry please contact:

Austria Mikro Systeme International AG
Mr. Michael Buchbauer
Tel.: +43 3136 500 277
Fax: +43 3136 500 501

PS: for more information about the NASA-mission "New Millennium Deep-Space 2" please contact the NASA- homepage http://nmp.jpl.nasa.gov

News from Siemens

Siemens Passive Components and Electron Tubes Group on track for expansion, plans to go public

In the fiscal year ending September 30,1998, the Siemens Passive Components and Electron Tubes Group (PR) continued its policy of expansion with a significant increase in sales and profits. At the Group's annual press conference, held at the *Electronica* 98 trade fair in Munich, its president, Klaus Ziegler, stated that PR's forthcoming conversion into an independent legal entity and subsequent listing on the stock market would lay the foundation for sustained growth and strengthen the new company's role as a global player in passive components. The steps announced would result in greater autonomy and flexibility.

According to preliminary figures for fiscal 1997/98, the Passive Components and Electron Tubes Group, which belongs to the components business segment of Siemens AG (Berlin and Munich), increased sales by some 14% from DM 2.3 to 2.6 billion. New orders rose by 11 % from DM 2.5 to 2.7 billion, while income before taxes climbed 34% from DM 216 to 290 million.

With some 9600 employees, Siemens Passive Components and Electron Tubes is one of the world's leading manufacturers of key electronic products, such as capacitors, ceramic components, special magnetic materials, and other high-tech components. International business accounted for almost two thirds of PR's total sales in the past fiscal year, Ziegler stated.

Over the past 10 years, PR has grown significantly faster than the market. One of the main reasons for this growth

is the success of the joint venture Siemens Matsushita Components, which accounts for about two-thirds of PR's total sales. Siemens and Matsushita have equal shares in the joint venture with a total of 5400 employees. In the past fiscal year, Siemens Matsushita Components managed to boost sales by 23% to DM 1.69 billion, while income before taxes even climbed 41 % to DM 195 million.

Ziegler also commented in detail on the planned transformation of the Passive Components and Electron Tubes Group into an independent legal entity and subsequent listing on the stock market. Together with the Semiconductor Group and the Electromechanical Components Group, PR belongs to the components business segment, from which Siemens is to withdraw as part of a ten-point plan to refocus its business portfolio. In a first step, PR's Divisions are to be integrated into Siemens Matsushita Components, and the new company thus resulting is then be listed on the stock market. The ten-year joint venture contract between Siemens and Matsushita expires on September 30,1999. Against this background, PR's management has proposed going public to Siemens' Corporate Executive Committee. Ziegler stated that Siemens Matsushita Components would thus form the nucleus of a new enterprise with much more clout. Siemens and Matsushita would remain major shareholders in the new company. In-depth negotiations are currently being held with Matsushita.

Various trends shaped the course of business in the Passive Components and Electron Tubes Group over the past fiscal year. Development of new materials and miniaturization continued unabated. This called for a major commitment to research and development by all players in the global components market, Ziegler stressed. In the past fiscal year alone, PR stepped up R&D expenditure by 15% to DM 118 million. A further increase of 24% to DM 146 million was planned for the current fiscal year. At the same time, customers were more frequently calling for a reduction in the number of suppliers, combined with perfect logistics. For this reason, PR opened new facilities in Singapore and Évora, Portugal, in fiscal 1997/98. These two major projects accounted for a 60% increase in investments to DM 395 million.

During fiscal 1997/98, the number of employees at PR rose from 8700 to about 9600, over half of whom work in Germany - in Berlin, Hanau and Heidenheim as well as at the Group's Munich plants and headquarters. PR consists of several organizational units, some of which are independent companies. As well as Siemens Matsushita Components, they include the Electron Tubes Division headquartered in Berlin; Vacuumschmelze, a manufacturer of special magnetic materials based in Hanau, Germany; Icotron in Gravatai, Brazil, which mainly serves the NAFTA market; and Crystal Technology in Palo Alto (CA) USA.

For more information on Siemens Passive Components and Electron Tubes, visit our website:
http://www. siemens. de/pr

Reference No PR UK 1198.800e
Press Office Passive Components and Electron Tubes
Thomas Kuther
P.O.Box 8017 09, D-81617 Munich
Tel.:++49 89 636-28083, Fax - 22471
E-mail: thomas.kuther@.uk.siemens.de

Siemens Semiconductors opens a new research and development center in Graz

Siemens Semiconductors today opened a new research and development facility in Graz, Austria. The design center's tasks will be the development of new products and the creation of intellectual property (IP) for biometrics, security, chipcard and RF integrated circuits. The new facility will employ around 100 design engineers.

The design center will meet the growing need for new developments arising from Siemens Semiconductors' logic initiative. All projects will be handled in full on site, in other words every phase in the development process - from product definition through to the transfer to manufacturing - will take place in Graz.

In advance of the facility's inauguration, Dr. Ulrich Schumacher, CEO and President of the Siemens Semiconductors and member of the Managing Board of Siemens AG, emphasized that outstanding system expertise in product development and IP, as well as manufacturing and marketing know-how, were essential success factors for a major semiconductor company. With the new R&D center, the Semiconductor Group was further extending its reach in design and IP, as well as driving Semiconductors' logic initiative by consistently building up greater systems expertise. This new product development center will play an important role in Siemens Semiconductor's worldwide design network, through which the Group's individual center of competence constantly exchange the results of research in each of their respective fields of specialization.

The Semiconductor Group also has design centers in Singapore, in Bangalore (India), in Cupertino, San Jose and San Diego (California, U.S.A.), in Tel Aviv (Israel), in Sophia Antipolis (France), and in Düsseldorf (Germany). Siemens Semiconductors also has another design center in Villach, Austria, which employs 220 developers and specializes in smart power, telecommunications, sensor and consumer electronics products. In Villach the Group also has a manufacturing facility with 1,600 workers, where it fabricates power semiconductors.

Siemens' Semiconductor Group is a leading worldwide provider of integrated circuits, memory products, RF components and discrete and power semiconductors, sensors and fber optic components. The comprehensive product line of Siemens Semiconductors serves a wide range of customers active in telecommunications, automotive and consumer electronics, data processing and automation. Siemens is the market leader for chip card ICs. In fiscal 1997/98, Siemens Semiconductors achieved sales of $3.8 billion (DM 6.7 billion) and employed 25,000 people worldwide. The group plans to go public.

Further information:

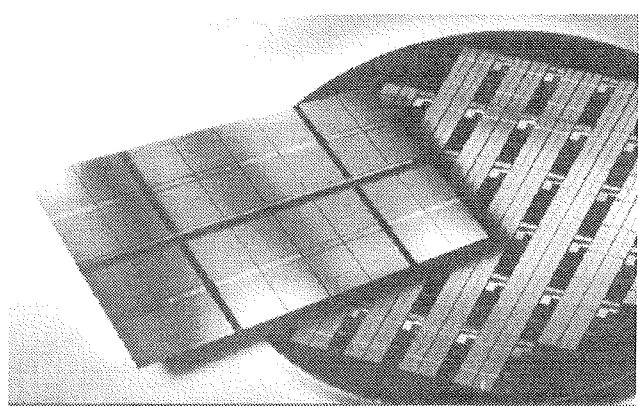
http://www.siemens.com/Semiconductor/index. htm

Reference number: HL XX 1198.016 e
Press Office Semiconductors
Katja Schlendorf
Postfach 8017 09, D-81617 Munich
Tel.: ++49 89 636-28480,
Fax: -28482
E-mail: katja.schlendorf@uk.siemens.de

News from Semiconductor International

Siemens dumps semis

Pressure from profit-hungry investors pushed Siemens' chief executive Heinrich von Pierer into radical DM4bn restructuring that will see semiconductors outside the conglomerate.



At Munich's Electronica show Siemens presented first silicon of its 1 Gbit SDRAM. The chip is manufactured using a 0.18 μm CMOS process, width an area of 390 mm^2.

At the Electronica show in Munich, Semiconductor group president Ulrich Schumacher said that the new IC company - without the Siemens name - will float 20-25% of Siemens' holdings by Initial Public Offering by the end of 1999 or early 2000. It will also set up a separate DRAM business and look for partnerships with other manufacturers. The aim is to boost Siemens' current 10% standing, in the face of consolidation by competing DRAM blocs - LG/Hyundai, Micron/TI, Samsung - with roughly 20% market share each.

The joint ventures with Motorola (White Oak VA and the 300 mm pilot, SC300, in Dresden) will continue, as will Corbeil-Essones, France (IBM). The forming of the semiconductor group as a separate legal enitity could be as early as Q1 1999.

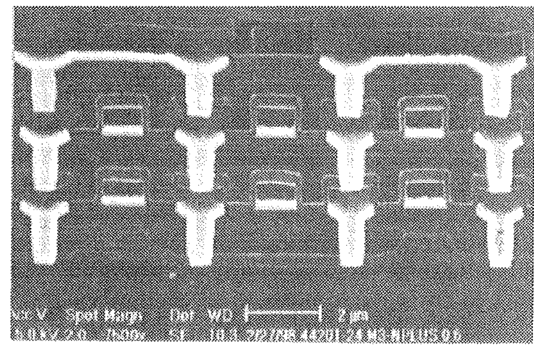
Siemens has wafer fabs and assembly plants in Germany, France, Austria, Singapore, Malaysia and Portugal. The components division, of which Semiconductors currently forms a part, employs 47,000 people worldwide. Including other businesses to be shed from the conglomerate, some 60,000 workers will be affected (25,000 in Germany). Sales for components were DM11bn with a loss of DM1.2bn in the last financial year to September. The main factor has been the DRAM price collapse.

Total sales for the conglomerate were DM118bn. The businesses to be put out the door account for a seventh of this. Von Pierer said there were no plans to cut the 60,000 jobs or to make large-scale reductions in worldwide workforce (just over 400,000 people).

The company plans to concentrate on four divisions: information and communications, industry rail systems and power generation. Plans for a big acquisition in telecoms are to be announced in the near future. Von Pierer. hinted that this would be in the US: "The real music is not playing in Europe. It is in the US, in particular Silicon Valley."

RF BiCMOS

Philips Semiconductors' has a new silicon-only BiCMOS processQUBiC3, which integrates high-frequency RF bipolar with high-speed CMOS logic. Re-



QUBiC3 has a fourth metal layer allowing for Inductors on-chip

searchers in Albuquerque (where it was developed) have shown that it can achieve an f_{max}=70 GHz, about double the norm for silicon and comparable to silicon germanium and gallium arsenide but at two-thirds the cost. This opens up the possibility of wristwatch-sized video phones.

QuBiC3 has 3 V 0.5 μm CMOS (0.42 μm effective gate length) and f_T=32 GHz. The bipolar npn transistors use an improved double-polysilicon technology with low-k (3.0) HSQ (hydrogen silsesquioxane) dielectric for 45% less interconnect capacitance. A thick, low-resistance fourth metal interconnect layer has been added to allow on-chip integration of inductors. The number of masking stages is 26. The next research aim is to reduce noise from 0.6 dB for integration of power amplifiers. Scheduled for release in the coming months are 25 new products - RF front-end ICs for CDMA and GSM. Initially f_{max} will be 60 GHz.

QUBiC4 (to be released for design 2000, production 2001-2) will use QUBiC3's transistor structures but with 0.25 μm CMOS and deep trench isolation to reduce cross-talk for f_{max}=90 GHz. QUBiC5 (probably 0.18 μm) could use either bipolar SiGe or pure RF CMOS in silicon.

France-Bulgaria JV

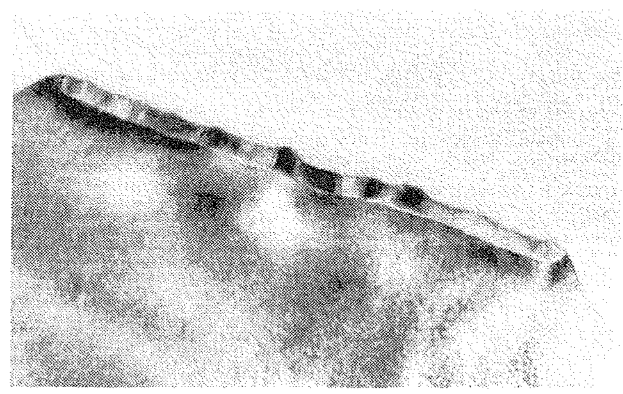
Silway (recently formed by EGP Holdings, France) has announced an ASSP and ASIC venture, with design at MISIL (Paris and Bordeaux) and design and manufacturing at Silway Semiconductor in Sofia, Bulgaria. The focus will be mixed-signal, high-voltage and high gate density technologies. The Sofia fab has 2 μm (double-poly) and highvoltage bipolar technology (250 V, 400 V in 1999). It is migrating to 1.2 μm double-poly double-metal (0.25 μm available from partners).

News from IMEC

New $CoSi_2$ silicidation process demonstrated for 0.13 μm

A new Co-silicidation process with a Ti-cap layer has been demonstrated and characterized for 0.13 μm CMOS technology and is ready for transfer to industry.

Scaling CMOS processes below 0.25 μm features imposes problems on the silicidation module as the formation of the low-resistance C49 $TiSi_2$ phase can become troublesome when scaling down to narrow silicide lines.



Cross-sectional TEM of a $CoSi_2$ layer formed from 15 nm Co / 8 nmTi (cap) along a field oxide.

$CoSi_2$ can be a viable altemative to $TiSi_2$ for CMOS processes of 0.25 μm and below. Similar to $TiSi_2$, Co-silicidation is a two step process: reaction of Co with the exposed Si by rapid thermal processing (RTP), in between wet removal of unreacted Co and a second RTP cycle, to form $CoSi_2$. It has been shown that the nucleation of $CoSi_2$ from CoSi is not delayed by narrow feature sizes, in contrast to $TiSi_2$. Although Co is less reactive with the ambient and its contaminants than Ti, ambient contamination indeed plays a significant role in the reproducibility of the silicidation process, especially for narrow dimensions.

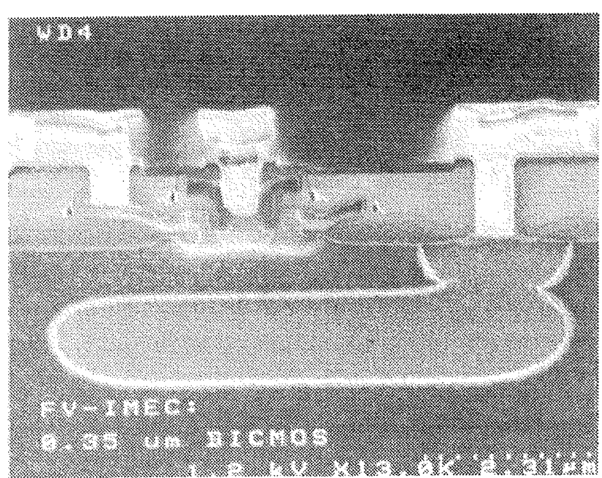
To overcome this problem, IMEC has investigated the use of a Ti cap layer on top of Co to increase the reproducibility of the silicidation process. Results show that the Ti cap is very efficient in reducing the ambient contamination to a strict minimum by reacting with any residual moisture in the chamber. In addition, no. edge thinning could be observed.

The Co/Ti (cap) silicidation process has been demonstrated and characterized for 0.13 μm CMOS technology. The patented silicidation process is now ready for transfer to industry. Two major semiconductor companies have already implemented IMEC's Co/Ti (cap) silicidation module in their industrial processes.

Development of 0.35 μm BiCMOS with 50 GHz Fmax bipolar transistors

The development of process modules for 0.35 μm BiCMOS technology has been finalized at IMEC and integration evaluated.

The combination of high-density low-power CMOS and high-performance npn transistors makes BiCMOS technology very attractive for high level integration for mixed analog/digital and RF applications. The expanding interest in RF applications together with demands for increasing bandwidth and available number of channels, drive new applications to higher frequencies, while the typical analog specifications such as low noise and high linearity remain very strict. Epitaxial base technology offers an interesting alternative to low-energy ion implant, since neither the channeling tail nor the implant damage are present with this technique. This way high cutoff frequencies can be combined with high Early voltages and low base resistance, thereby fulfilling both the high speed and good analog specifications.



Cross-sectional electron microscope picture of epitaxial base bipolar transistor.

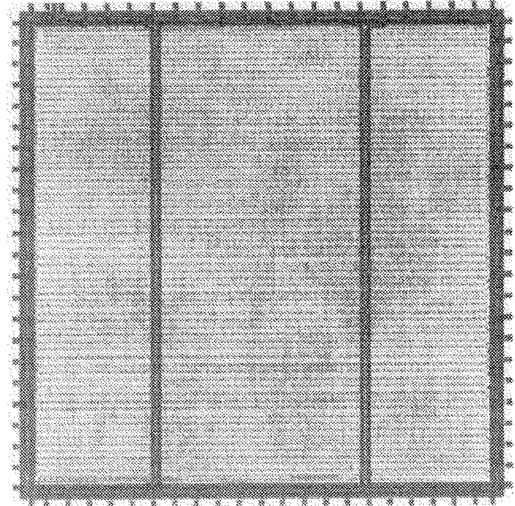
IMEC has chosen a selective Si epitaxial growth process compatible with a double poly inside spacer architecture for the emitter/base formation as a precursor to a SiGe technology The resulting structure shows very low device parasitics, very good ideality of the base current, current gain > 80 and high breakdown voltages.

The combination of 24 GHz with 30 Volt Early voltage is very attractive for RF designs. The reduction of the device parasitics resulted in a maximum oscillation frequency Fmax of 50 GHz.

LTMS: on board time distribution support

The LTMS ASIC was developed by IMEC for the European Space Agency as key element of a decentralized distribution scheme for correct time information in spacecrafts.

With the advent of packet-switched networks on board of spacecraft, non-deterministic delays occur in the communication between the central terminal unit of the spacecraft and local experiments. Distribution of correct time information over the spacecraft therefor became a problem. The radiation-hard LTMS (Local Time Management System) enables users to overcome this problem. LTMS is the key element of a decentralized time distribution scheme, providing time coherence throughout the spacecraft without requiring processing power from the applications using it. Local copies of the centralized Elapsed Time reference of a spacecraft are maintained by LTMS devices located close to the users, according to ESA and CCSDS standards. The central reference is to be managed by a Central Time Management System (CTMS).



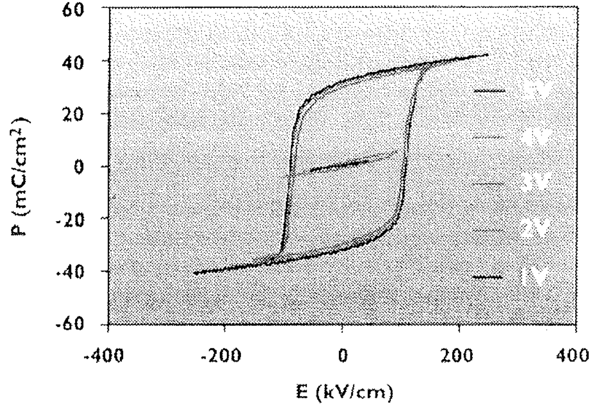
The coherence between local and central reference is maintained by means of time, synchronization messages distributed by the CTMS. The LTMS performs regular synchronization with respect to the central reference using such messages and provides its users with several time facilities related to the local Elapsed Time reference: a time-stamp, an alarm clock, a pulse generator, a wave-form generator and a stopwatch. The LTMS synchronizes with the CTMS with an accuracy of 1 μs, and offers 250-ns resolution to the experiments. An extension interface allows building customized time facilities. The LTMS automatically maintains a high resolution and high precision local time reference, without discontinuities.

LTMS can be found in the Hi-Reliability space component catalog of MITEL Semiconductor and is available to system houses to use in their on-board applications.

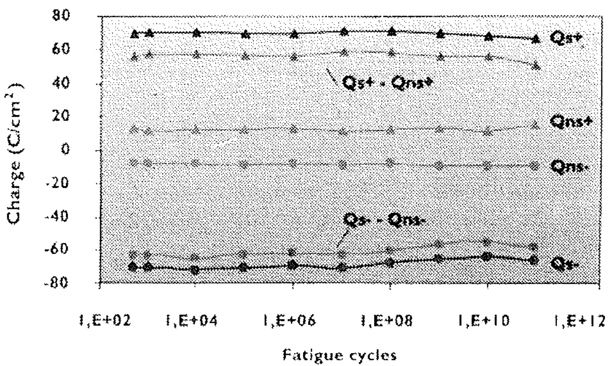
New ferroelectric technology developments for embedded FERAM

The first technology test chip integrating PZT ferroelectric capacitors in IMEC's 0.5 μm CMOS process was successfully fabricated. Applying RuO_2 electrode technology drastically improves the endurance performance with 5 orders of magnitude compared to that of Pt electrodes.

The microdisplay module was developed by IMEC/INTEC, associated laboratory of IMEC at the University of Gent, Belgium, one of the pioneers in this technology in Europe. Recently research on miniature displays (microdisplays) made on silicon has been launched in the. US. This technology does not require major invest-



Hysteresis characteristics of fully integrated PZT ferroelectric capacitor (area: 10 μm^2), measured in an array of 100 capacitors, using a 1 kHz triangular signal with 1-5 V amplitude.



Endurance characteristics of PZT ferroelectric capacitor with RuO_2 electrodes. After 10^{11} cycles, less than 10 % degradation of the memory signal (= difference between switched charge Qs and non-switched charge Qns) is observed. Measured on a 1,000 μm^2 area capacitor, with 5 V, 1 MHz pulses.

ment - relying on existing silicon foundries - and therefore becomes extremely attractive. At this moment first products are announced envisaging extremely high resolutions.

The microdisplay module shown consists of a 160x120 pixel paper-white reflective polymer dispersed liquid crystal on an analog DRAM chip processed in a 2μHBIMOS technology and packaged on 5x5 cm ceramic substrate. By means of thick-film technology a fast serial digital data link (LVDS), a digital-to-analog converter and a video amplifier are integrated on the ceramic substrate. A simple flat cable connects the module to the PC controller board. In this way parts of the PC screen are captured and displayed on the microdisplay module. Due to the reflective nature of the microdisplay extremely low power consumption can be realized. The module enables gray shade images and video. First samples will soon become available for evaluation.

Dow Corning announces IMEC affiliation to support low-k ILD development

In a move expected to boost development of new materials and facilitate processing innovations for semiconductor fabrication, Dow Corning has joined the *IMEC* Industrial Affiliation Program (IIAP). The IIAP encourages collaboration between *industrial* researchers and a special IMEC team focused on low-k dielectric technology.

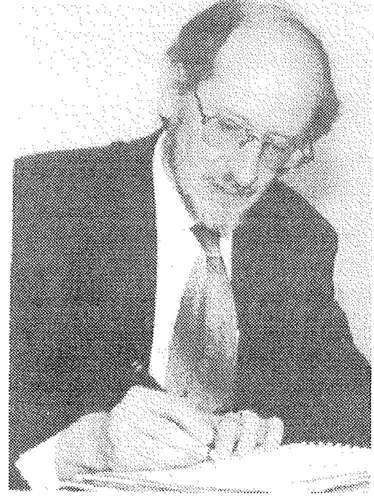
As part of the collaboration, IMEC is sharing part of relevant technology in low-k dielectrics with Dow Corning. IMEC has also agreed to share data from research that has involved FOx (flowable oxide materials) and has granted Dow Corning early access to the non-proprietary results of further testing.

"Because IMEC uses FOx in its process of record for 0.35 μm and 0.25 μm applications, IMEC has a significant amount of data on the integration of FOx Flowable Oxide as an interlayer dielectric," according to Dow Corning's application development group leader Phil Dembowski. "IMEC is also using this technology for development of devices with 0.18 μm architecture."

Dow Corning plans to use the newly available resources to explore a number of key issues: dual-damascene technology lower dielectric constant materials, unlanded via integration and direct-on-metal integration.

In a related move, Dow Corning announced that application and development engineer Doug Gray has been reassigned from the Fremont office (California, USA) to work on the IMEC program full time. "This is the kind of cooperative effort required to accelerate implementation of low-k materials into leading edge 0.18 μm applications and beyond," Dembowski concluded.

Gilbert Declerck COO of IMEC



The board of directors and Prof. Roger Van Overstraeten, president of IMEC, have appointed Prof. Gilbert Declerck to Chief Operating Officer of IMEC. The new COO was up to now senior-vice president and director of the Advanced Semiconductor Processing division of IMEC.

Prof. Van Overstraeten will continue to act as president of IMEC and will focus its activities on the overall IMEC strategy and external initiatives such as the creation of spin-off companies.

KOLEDAR PRIREDITEV 1999

FEBRUARY 1999

01.02. - 02.02.99
EUROPEAN MULTICHIP MODULE CONFERENCE
London, UK
Info : + 44 171 287 4898

01.02. - 05.02.99
DISPLAY WORKS '99
San Jose, CA, USA
Info.: + 1 650 940 6905

16.2., 19.2., 24.2., 26. 2. 1999
ICE's 34th ANNUAL REVIEW AND FORECAST OF THE IC INDUSTRY
Paris, France; Munich, Germany; Rome, Italy; Copehagen, Denmark
Info.: +45 43 71 20 44

21.02. - 23.02.99
SEMI EUROPEAN INDUSTRY STRATEGY SYMPOSIUM
Rome, Italy
Info.: + 32 2 289 6492

23.02. - 25.02.99
SMART CARD '99
London,UK
Info.: + 44 1895 454 438

MARCH 1998

08.03. - 10.03.99
MAM '99 - MATERIALS FOR ADVANCED METALLIZATION
Oostende , Belgium
Info.: + 32 16 29 00 10

09.03. - 12.03.99
DATE '99 - DESIGN, AUTOMATION AND TEST IN EUROPE
Munich, Germany
Info.: + 44 131 225 2892

15.3.99 - 19.3.99
AMERICAN VACUUM SOCIETY'S INTERNATIONAL CONFERENCE ON ADVANCED MATERIALS AND PROCESSES FOR MICROELECTRONICS
San Jose, CA, USA
Info.: + 212/ 248 0200

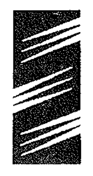
16.03. - 18.03.99
MICROELECTRONICS TEST STRUCTURES
Göteborg, Sweden
Info.: + 45 38 880 600

MAY 1999

02.05. - 07.05.99
195th MEETING OF THE ELECTROCHEMICAL SOCIETY
(Process Control, Diagnostics and Modeling in Semiconductor Manufacturing III)
Seattle, WA, USA
Info.: +1 609 737 1902

JUNE 1999

28.06. - 02.07.99
9th INTERNATIONAL SYMPOSIUM ON NONDESTRUCTIVE CHARACTERIZATION OF MATERIALS
Sydney, Australia
Info.: + 1 410 516 7126



SODOBNA ELEKTRONIKA

Ljubljanski sejem d.d.
Ljubljana fair
Dunajska 10, p.p. 3558
1001 Ljubljana Slovenija
tel +386/61/173 53 31
fax +386/61/173 52 32
+386/61/173 52 31
+386/61/131 71 01

Spoštovani!

Zahvaljujemo se Vam za sodelovanje na letošnjem že 45. Mednarodnem sejmu SODOBNA ELEKTRONIKA'98, v Ljubljani na Gospodarskem razstavišču od 5. do 9. oktobra 1998. Ocenjujemo da je prireditev bila uspešna tako za organizatorja, kot tudi za večino razstavljalcev in obiskovalcev. Dovolite da Vam predstavimo osnovne podatke iz statistike sejma in rezultate ankete, ki smo jo opravili med razstavljalci in obiskovalci.

Na sejmu se je predstavilo skupaj 582 podjetij in ustanov iz 26 držav. Neposredno je bilo prijavljenih 264 razstavljalcev iz 10 držav in sicer 214 iz Slovenije, med tujimi pa največ (22) iz Avstrije, 9 iz Hrvaške, 7 iz Nemčije, 4 iz Češke republike, 3 iz Švice, 2 iz Italije, po eden pa iz Belgije, Francije in Velike Britanije. Med 318 zastopanimi podjetij jih je bilo največ iz Nemčije (104), ZDA (59), Japonske in Velike Britanije (21), Avstrije (20), Italije (19) in Švice (18). Zastopana so bila še podjetja iz Avstralije, Kanade, Danske, Finske, Irske, Izraela, Koreje, Malezije, Nizozemske, Norveške, Nove Zelandije, Singapura, Španije, Švedske in Tajske.

V razstavnem programu je bilo največ komponent (vključno z elektroinštalacijami 26%), avtomatizacije z merilno elektroniko 24%, telekomunikacij 18%, inženiring, servisne dejavnosti in R & R 11%, opreme za proizvodnjo 7%, radiodifuzije in kabelsko satelitske tehnike 5%, pisarniške avtomatizacije 4%, audio-video elektronike pa 2%. Zasedeno je bilo 8000 m2 neto razstavnih površin.

Sejem je videlo po oceni organizatorja okoli 31.000 ljudi, medtem ko je število prodanih vstopnic po kriterijih mednarodne revizije FKM znašalo 27.034. Bistveno večji je delež poslovnih kuponov (za 20% več kot lani), kar pomeni da je že skoraj vsak tretji obiskovalec registriran in osebno vabljen. To potrjuje vse večjo poslovno orientiranost sejma. Anketa je tudi pokazala, da je na sejem službeno prišlo 41% obiskovalcev, 23% vseh obiskovalcev pa namerava v roku 14 dni po sejmu tudi naročati prikazane izdelke. Kar 76% vseh namerava sejem elektronike v Ljubljani v naslednjem letu ponovno obiskati, le 3% obiskovalcev pa je odgovorilo negativno. Večina (67%) razstavljalcev je v anketi napovedala ponovno udeležbo na sejmu Sodobna elektronika v naslednjem letu. Glede na to in ker želimo organizacijo še izboljšati smo se odločili, da Vas spoštovani razstavljalci, že s tem pismom povabimo k evidenčni prijavi. V kolikor torej nameravate ponovno sodelovati na sejmu SODOBNA ELEKTRONIKA'99, ki je na sporedu

od 4. do 8. oktobra 1999

Vas prosimo, da nam do konca novembra letos sporočite Vašo odločitev, želeno razstavno površino in morebitne druge pripombe in predloge.

V želji po še nadaljnjem uspešnem sodelovanju Vas lepo pozdravljamo,

Projektni vodja
Gorazd Majcen, dipl.oec.

Ljubljana, 30.10.1998

VSEBINA LETNIKA 1998 — VOLUME 1998 CONTENT

UDK621.3:(53+54+621+66), ISSN03529045 — **Informacije MIDEM 28(1998)1, Ljubljana**

VSEBINA	Str.	CONTENT
Obvestilo o konferenci MIDEM ´98	2	Call for Papers - Conference MIDEM ´98
ZNANSTVENO STROKOVNI PRISPEVKI		PROFESSIONAL SCIENTIFIC PAPERS
M. Šalamon, B. Jarc, T. Dogša: Uporabnost cenovno ugodnih CAE/CAD orodij za načrtovanje integriranih vezij	3	M. Šalamon, B. Jarc, T. Dogša: Applicability of Low Cost CAE/CAD Tool for Designing Integrated Circuits
S. Solar: Temperaturno in napetostno stabilni tokovni izvori v podmikrometerskih tehnologijah	9	S. Solar: Voltage and Temperature Independent Current Sources in Submicron Technologies
J. Hauptmann, W. Pribyl, J. Sevenhans, Z. Chang: A/D in D/A pretvorniki - osnovni gradniki telekomunikacijskih vezij	18	J. Hauptmann, W. Pribyl, J. Sevenhans, Z. Chang: A/D and D/A Converters - Basic Building Blocks for Telecom Applications
R. Čop: Razvoj strojne in programske opreme	22	R. Čop: The Development of Hardware and Software Components
J. Pirš, R. Petkovšek, S. Pirš, S. Kralj, S. Žumer: Vpliv površinskih pogojev na strukturo zig-zag defektov v feroelektričnih LCD prikazalnikih	25	J. Pirš, R. Petkovšek, S. Pirš, S. Kralj, S. Žumer: Influence of Surface Topography on Zig-zag Defects in Ferroelectric Liquid Crystal Displays
D. Lisjak, M. Drofenik: PTCR efekt v kompozitni keramiki	33	D. Lisjak, M. Drofenik: PTCR Effect in Composite Ceramics
M. Pavlin, D. Belavič, S. Šoba, S. Amon, U. Aljančič: Senzorji tlaka s tokovnim napajanjem	38	M. Pavlin, D. Belavič, S. Šoba, S. Amon, U. Aljančič: Pressure Sensors with Constant Current Excitation
D. Belavič: Delovanje mešane raziskovalno razvojne skupine na področju hibridne debeloplastne mikroelektronike	43	D. Belavič: Activities of Joint Research and Development Group on Hybrid Microelectronics
MIDEM IN NJEGOVI ČLANI, NOVICE IZ DRUGIH SREDIN		MIDEM SOCIETY AND ITS MEMBERS, NEWS FROM OTHER INSTITUTIONS
M. Budnar: Tandemski pospeševalnik na IJS, Informacija ob postavitvi TANDETRONa	48	M. Budnar: Information on TANDETRON: New Accelerator at IJS
PREDSTAVLJAMO PODJETJE Z NASLOVNICE		REPRESENT OF COMPANY FROM FRONT PAGE
IJS Odsek za keramiko	54	IJS Department of Ceramics
POROČILA		REPORTS
D. Vrtačnik: SEMICON Europa´98	55	D. Vrtačnik: SEMICON Europa´98
PRIKAZ MAGISTRSKIH DEL IN DOKTORATOV V LETU 1997	56	M.S. and PhD ABSTRACTS, YEAR 1997
VESTI	64	NEWS
KOLEDAR PRIREDITEV	67	CALENDAR OF EVENTS
MIDEM prijavnica	69	MIDEM Registration Form

Slika na naslovnici:
Shematski prikaz termično vzpodbujenega naraščanja viskoznosti keramične suspenzije, ki ji je dodan prah AlN in posnetek delcev AlN po hidrolizi (SEM). Postopek oblikovanja keramičnih izdelkov iz vodne suspenzije s pomočjo hidrolize AlN (HAS) je bil razvit na Institutu J. Stefan (SI patent 1995, Evropska patentna prijava 1998).

Front page:
Thermally activated viscosity increase for AlN containing ceramic suspensions (schematic) and AlN particles after hydrolysis (SEM). The process for forming ceramic parts from aqueous suspensions by hydrolysis assisted solidification (HAS) was invented at Jozef Stefan Institute (SI patent 1995, Europ. Patent application 1998).

UDK621.3:(53+54+521+66), ISSN0352-9045 — Informacije MIDEM 28(1998)2, Ljubljana

ZNANSTVENO STROKOVNI PRISPEVKI		**PROFESSIONAL SCIENTIFIC PAPERS**
M. Maček: Mikro bolometer, I. del: Teoretične osnove	77	M. Maček: Micro Bolometer, Part I: Theoretical Backgrounds
M. Maček: Mikro bolometer, II. del: Meritve karakteristik in primerjava z izračuni	81	M. Maček: Micro Bolometer, Part II: Measurements of Characteristics and Comparison with Calculations
A. Lechner: Mikrostrukturirani senzorji in aktuatorji - Pregled	90	A. Lechner: Micro-structured Sensors and Actuators: an Overview
J. Trontelj: Elektronika za polje integriranih Hallovih senzorjev	95	J. Trontelj: Integrated Hall Sensor Array Electronics
M. Kovač, S. Pejovnik: Identifikacija polimernih elektrolitov PEO-M(SO_3Cl)x (M = Li, LiAl, Ca)	102	M. Kovač, S. Pejovnik: Identification of PEO-M(SO_3Cl)x (M = Li, LiAl, Ca) Polymer Electrolytes
APLIKACIJSKI PRISPEVKI		**APPLICATION ARTICLES**
I. Šorli, R. Mauri: Odprava EMI motenj, I. del. Definicije in osnove	110	I. Šorli, R. Mauri: EMI Suppression, Part I. Definitions and Basics
PREDSTAVLJAMO PODJETJE Z NASLOVNICE		**REPRESENT OF COMPANY FROM FRONT PAGE**
Siemensov mikroelektronski načrtovalski center v Beljaku in Grazu	117	Siemens Microelectronics Design Center, Villach and Graz
POROČILA		**REPORTS**
D. Križaj: 8. Evropska konferenca o polprevodniških detektorjih	120	D, Križaj: 8th European Symposium in Semiconductor Detectors
M. Hrovat: 4. Evropska konferenca EC-MCM´98	120	M. Hrovat: 4th European Conference on Multi Chip Modules EC-MCM´98
M. Hrovat, D. Belavič: 21. Mednarodni spomladni seminar o elektronski tehnologiji	123	M. Hrovat, D. Belavič: 21st International Spring Seminar on Electronic Technology ISSE´98
VESTI	126	**NEWS**
KOLEDAR PRIREDITEV	137	**CALENDAR OF EVENTS**
Navodila avtorjem	138	Information for Contributors
MIDEM prijavnica	139	MIDEM Registration Form
Slika na naslovnici: Siemensov mikroelektronski načrtovalski center v Beljaku in Grazu - pravi naslov za mikroelektronsko sistemsko integracijo		Front page: Siemens Microelectronics Design Center Villach and Graz - A Competence Center for Microelectronic System Integration

UDK621.3:(53+54+621+66), ISSN0352-9045 — Informacije MIDEM 28(1998)3,Ljubljana

ZNANSTVENO STROKOVNI PRISPEVKI		**PROFESSIONAL SCIENTIFIC PAPERS**
P.J. Mach, P.M. Svasta: Študij povezave med diferencialno nelinearnostjo, nelinearnostjo in šumom debeloplastnih uporov	149	P.J. Mach, P.M. Svasta: Study of Correlation Among Differential Nonlinearity, Nonlinearity and Noise of Thick Film Resistors
D. Raič: Merjenje porabe moči v pomnilnih strukturah CMOS	154	D. Raič: Measuring the Weighted Power of CMOS Latching Circuits
V. Jenuš, B. Horvat: Audio vmesnik za računalnik	162	V. Jenuš, B. Horvat: Audio Interface for Workstation
W. Pribyl, T. Scheiter, G. Hribernig: CMOS integrirano vezje za senzor prstnih odtisov z ločljivostjo 500 dpi	167	W. Pribyl, T. Scheiter, G. Hribernig: A 500 dpi Fingerprint Sensor IC in CMOS Technology
M. Mozetič, B. Praček: Interakcija vodikove plazme s korodirano površino srebra	171	M. Mozetič, B. Praček: Interaction of Hydrogen Plasma With Corroded Silver Surface
M. Mozetič: Reakcije na površini katalitične sonde med plazemsko obdelavo polieter sulfona	175	M. Mozetič: Reactions on Catalytic Probe Surface During Oxygen Plasma Treatment of Polyether Sulphone

APLIKACIJSKI PRISPEVKI		APPLICATION ARTICLES
V. Murko: Novitete iz razvoja podjetja Iskra Žarnice Elvelux	180	V. Murko: New Products from the company Iskra Žarnice Elvelux
PREDSTAVLJAMO PODJETJE Z NASLOVNICE		REPRESENT OF COMPANY FROM FRONT PAGE
Iskra Avtoelektrika d.d.	184	Iskra Avtoelektrika d.d.
POROČILA		REPORTS
D. Belavič, R. Ročak: XXII IMAPS - konferenca Poljske sekcije	185	D. Belavič, R. Ročak: XXII IMAPS - Poland Chapter Conference and Exhibition
D. Belavič: ISHMž98 - konferenca Nemške sekcije	186	D. Belavič: Deutsche ISHM Konferenze 1998
VESTI	187	NEWS
KOLEDAR PRIREDITEV	195	CALENDAR OF EVENTS
MIDEM prijavnica	197	MIDEM Registration Form
Slika na naslovnici: Brushless DC motor z ločenim (levo) in prigrajenim (desno) elektronskim krmiljem, nov izdelek Iskre Avtoelektrike d.d.		Front page: Brushless DC motor with separate (left) and built-in (right) electronic control, new product of Iskra Avtoelektrika d.d.

UDK621.3:(53+54+621+66), ISSN0352-9045 | **Informacije MIDEM 28(1998)4, Ljubljana**

ZNANSTVENO STROKOVNI PRISPEVKI		PROFESSIONAL SCIENTIFIC PAPERS
MIDEMž98 KONFERENCA - POVABLJENI REFERATI		MIDEMž98 CONFERENCE - INVITED PAPERS
K. Reichmann, N. Katsarakis, A. Reichmann: Elektronsko prevodni perovskitni materiali	205	K. Reichmann, N. Katsarakis, A. Reichmann: Electronically Conductive Perovskite Type Materials
S. Sokolić, S. Amon: Modeli za transport nosilcev v bazi npn SiGe heterospojnega transistorja	211	S. Sokolić, S. Amon: Models for Carrier Transport in the Base of npn SiGe HBTs
H. Gugg-Schwaiger: Mešana CMOS tehnologija firme Alcatel Microelectronics z minimalno razsežnostjo 0.5 μm	218	H. Gugg-Schwaiger: Alcatel Microelectronics 0.5μm Mixed CMOS Technology
M. Topič, F. Smole: Amorfnosilicijevi tankoplastni detektorji barv	223	M. Topič, F. Smole: Thin Film Color Detectors Based on Amorphous Silicon
M.H. LaBranche, C.J. McCormick, J.D. Smith, R.L. Keusseyan, R.C. Mason, M.A. Fahey, C.R.S.Needes, K.W. Hang:Naslednja generacija materialov za večplastna debeloplastna vezja	230	M.H. LaBranche, C.J. McCormick, J.D. Smith, R.L. Keusseyan, R.C. Mason, M.A. Fahey, C.R.S. Needes, K.W. Hang: Next-generation, Advanced Thick Film Multilayer System
KONFERENCA MIDEM´98 - POROČILO	236	MIDEM´98 CONFERENCE - REPORT
PREDSTAVLJAMO PODJETJE Z NASLOVNICE	242	REPRESENT OF COMPANY FROM FRONT PAGE
Iskra Varistor		Iskra Varistor
MIDEM IN NJEGOVI ČLANI		MIDEM SOCIETY AND ITS MEMBERS
Ervinu Pirtovšku v spomin	247	Ervin Pirtovšek in memoriam
VESTI	248	NEWS
KOLEDAR PRIREDITEV	254	CALENDAR OF EVENTS
VSEBINA LETNIKA 1998	256	VOLUME 1998 CONTENT
MIDEM prijavnica	259	MIDEM Registration Form
Slika na naslovnici: Iskra Varistor, proizvajalec varistorjev in supresorjev		Front page: Iskra Varistor, Varistor and Couplings Manufacturing Company