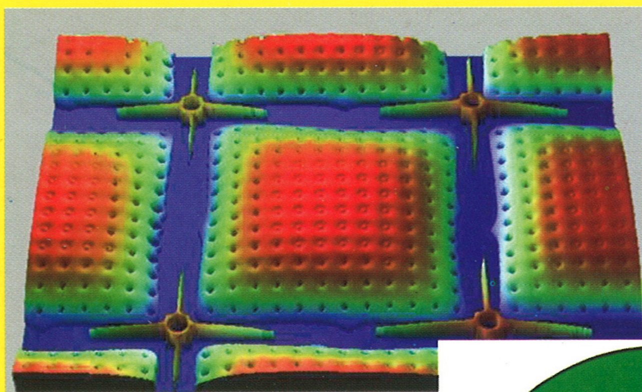
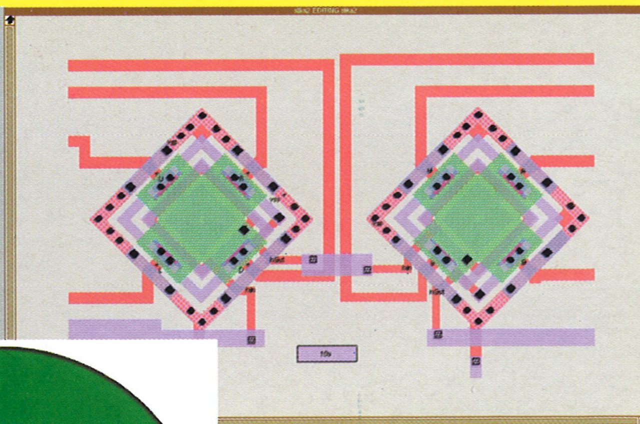
UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

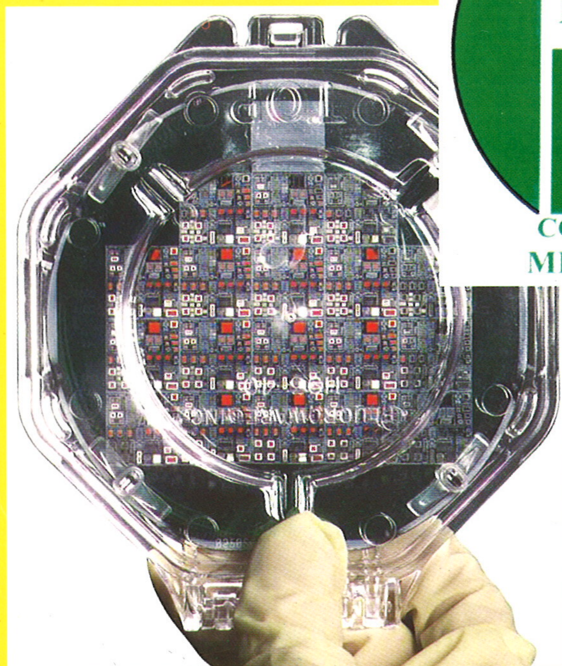
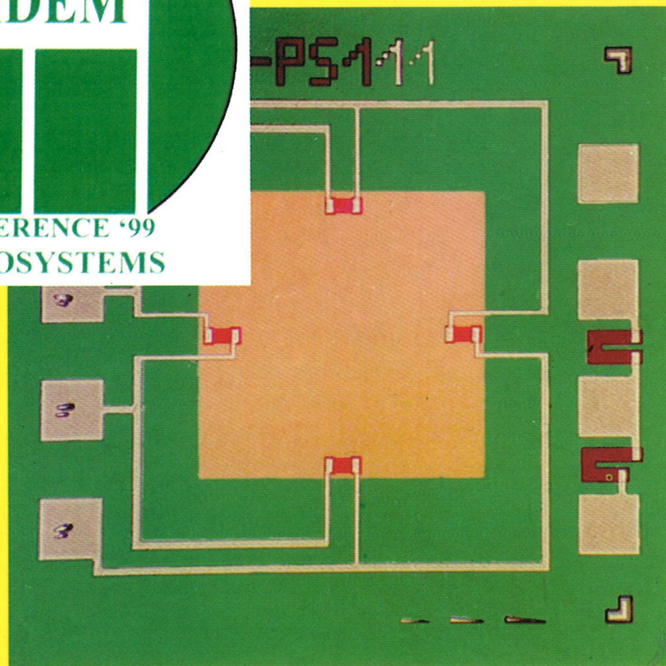
INFORMACIJE MIDEM 4 • 1999

Strokovno društvo za mikroelektroniko elektronske sestavne dele in materiale

Strokovna revija za mikroelektroniko, elektronske sestavne dele in materiale
Journal of Microelectronics, Electronic Components and Materials

INFORMACIJE MIDEM, LETNIK 29, ŠT. 4(92), LJUBLJANA, december 1999

UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

INFORMACIJE MIDEM 4 ∘ 1999

INFORMACIJE MIDEM LETNIK 29, ŠT. 4(92), LJUBLJANA, DECEMBER 1999

INFORMACIJE MIDEM VOLUME 29, NO. 4(92), LJUBLJANA, DECEMBER 1999

Revija izhaja trimesečno (marec, junij, september, december). Izdaja strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale - MIDEM.
Published quarterly (march, june, september, december) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

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Scientific Council for Technical Sciences of Slovene Ministry of Science and Technology has recognized Informacije MIDEM as scientific Journal for microelectronics, electronic components and materials.
Publishing of the Journal is financed by Slovene Ministry of Science and Technology and by Society sponsors.

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Grafična priprava in tisk
Printed by
BIRO M, Ljubljana

Naklada
Circulation
1000 izvodov
1000 issues

Poštnina plačana pri pošti 1102 Ljubljana
Slovenia Taxe Percue

UDK621. 3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 29(1999)4,Ljubljana

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Slika na naslovnici: Na konferenci MIDEM´99 smo v okviru delavnice "MIKROSISTEMI" videli primere mnogih uspešno realiziranih mikrosistemov. Zgoraj levo: CBM matrika (Fraunhofer IMS), sliko prispeval CTR; zgoraj desno: Par Hallovih elementov z integrirano tuljavo, sliko prispeval LMFE; spodaj levo: Zadnja stran rezine po globinski mikroobdelavi, sliko prispeval AMS; spodaj desno: Si tabletka senzorja pritiska, sliko prispeval LMSFE;

Front page: MIDEM´99 Conference workshop on MICROSYSTEMS showed several examples of successfully realized projects from this field. Upper left: CBM matrix (Fraunhofer IMS), courtesy of CTR; Upper right: Hall element pair with integrated coil, courtesy of LMFE; Lower left: Backside bulk micromachined wafer, courtesy of AMS; Lower right: Si pressure senzor chip, courtesy of LMSFE;

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SURFACE COATING OF HDDR PROCESSED NANOCRYSTALLINE POWDERS

S. Kobe, S. Novak, P.J. McGuiness,
Jožef Stefan Institute, Ljubljana, Slovenia

INVITED PAPER
MIDEM´99 CONFERENCE
13.10.99 - 15.10.99, Ljubljana, Slovenia

Keywords: Ni-Fe-B POWDERS Nickel-Iron-Boron, HDDR processes, Hydrogen Disproportionation Desorption Recombination PROCESSES, nanocrystalline powders, surface protection, surface coating, coercivity, high coercivity, RE magnets, Rare Earth magnets, magnetic properties, coated powders

Abstract: Chemical surface modification can be used as a method for corrosion protection of sensitive powders based on intermetallic alloys between rare earth and transition metals /1/. Surface coating is used for preventing fine powders, based on Nd-Fe-B, $Sm_2Fe_{17-x}Ta_x$ and $Sm_2Fe_{17-x}Ta_xN_{3-\delta}$ prepared by HDDR processing and mechanically alloying, from hydrolysis. Powders coated by chemisorbed organic substance, after exposing to a humid atmosphere, do not show any chemical or physical change.

Different coating agents were used and the sufficient amount of various materials was optimised with the emphasis on minimising their quantity. Simple experiment shows that the surfactant is successfully chemisorbed on the powder surface and that the coated powders are hydrophobic indefinitely.

Magnetic properties were measured on samples after they were exposed to the same corrosion tests. Measurements on coated and bonded samples were compared with the measurements of non-coated samples. By using Auger electron spectroscopy the thickness of the coating was controlled. In order to distinguish the nature of the bonding between the powder surface and the surface-active substance FT-IR spectroscopy in absorbance and diffuse reflection modes was used.

The protection of the fine particles is based on the formation of a covalent bond between the hydroxyl groups at the particle surface and the surface-active substance. The monomolecular layer of organic substance does not damage the magnetic properties of the powder, but successfully protects the powder against humidity.

Površinska zaščita nanokristaliničnih prahov pripravljenih po HDDR postopku

Ključne besede: Ni-Fe-B prahovi Nikelj-Železo-Bor, HDDR procesi z vodikovo disproporcionalno desorpcijsko rekombinacijo, prahovi nanokristalinični, zaščita površin, prekrivanje površin, koercitivnost, koercitivnost visoka, RE magneti zemelj redkih, lastnosti magnetne, prahovi prekriti

Povzetek: Kot zaščito pred korozijo občutljivih prahov na osnovi intermetalnih zlitin redkih zemelj in elementov prehoda je mogoče uporabiti kemijske metode površinskega prekrivanja prahov. Tako prekrivanje smo uporabili za prahove na osnovi Nd-Fe-B, $Sm_2Fe_{17-x}Ta_x$ in $Sm_2Fe_{17-x}TaxN_{3-\delta}$, ki so bili izdelani po HDDR postopku in s postopkom mehanskega legiranja oziroma visokoenergijskega mletja. Prahove smo prekrivali z organskimi sredstvi s kemisorbcijo in po korozijskih testih ti prahovi niso kazali nobenih kemijskih ali fizikalnih sprememb.

Uporabili smo različna sredstva in optimizirali njihovo količino. Enostaven laboratorijski poskus nam je pokazal, da je organsko sredstvo vezano na površino prahov s kemisorbcijo in da je prekrit prah trajno hidrofoben.

Prahovom smo izmerili magnetne lastnosti po korozijskih eksperimentih in jih primerjali z prahovi, ki so bili izmerjeni takoj po HDDR postopku in so bili brez zaščite. Za oceno debeline površinske plasti smo uporabili Augerjevo spektroskopijo. Naravo vezi med površino prahu in površinsko aktivnim sredstvom smo določali z uporabo FT-IR spektroskopije v absorbcijski in difuzijski refleksiji.

Ugotovili smo, da zaščita finih prahov temelji na tvorbi kovalentne vezi med hidroksilnimi skupinami na površini prašnih delcev in površinsko aktivne snovi. Zelo tanka plast organske substance ne poslabša magnetnih lastnosti prahov vendar pa zelo učinkoviti zaščiti njihovo površino.

Introduction

Several routes can be used to prepare high coercivity Nd-Fe-B powders, which can be used as a basic material for bonded magnets. For achieving high coercivities, in addition to composition the average particle size, grain size and its distribution are the most important parameters. Single domain sized grains (~300 nm) are preferable. For the production of nanocrystalline powders, in addition to melt spinning, the hydrogenation, disproportionation, desorption, recombination (HDDR) process /1,2/ and intensive milling /3/ can be used successfully as preparation methods for obtaining nanocrystalline powders without any further milling. It is well known that magnetic powders based on rare-earth and transition metals are very sensitive to the atmospheric conditions and one of the tasks of many researchers was, and still is, to improve the properties of the basic material by lowering the sensitivity of the bulk powder itself. The addition of small quantities of Co and Al improved the corrosion resistance of Nd-Fe-B magnets /4/. Also refractory elements like Zr /5,9/ and V /6/ or ZrO_2 can achieve this in sintered magnets /7,8/ and HDDR processed powders /10/. The addition of Zr

or ZrO_2 has been the subject of our further research /11/, together with the study of additional improvement of corrosion resistivity in powders, which is the basis of this paper.

Based on the results achieved with other materials /12/ and our preliminary experimental results, the idea was to improve the basic resistivity of Nd-Fe-B powder not only with additives, but also by coating individual particles with a very thin protective layer of organic molecules. It is important that the magnetic properties of the powders processed either by the HDDR processing route or intensive milling (IM) should not be damaged by the coating process. The resistivity against corrosion should be improved to the extent that very fine powders can be handled without any protective atmosphere in the production environments and that this procedure also should not significantly increase the production costs.

Surface modification of powders is based on the formation of a covalent bond between the hydroxyl groups that are usually present at metal or metal oxide surfaces, and surface modifying agents, such as long-chain carboxylic acids or silanes. The surface-active agent is first physically adsorbed onto the powder surface while during heating, condensation takes place, resulting in the formation of a covalent bond. After the reaction, the powder surface is covered with a monomolecular layer of organic molecules.

Experiment

Different powders: $Nd_{16}Fe_{76}B_8$, $Nd_{15}Dy_1Fe_{76}B_8$, $Nd_{15}Dy_1Fe_{75.3}Zr_{0.7}B_8$ were produced from 5 kg batches by HDDR processing. The compositions were chosen on the basis of our previous work /10/. For HDDR processing the alloys were exposed to a hydrogen atmosphere in a specially constructed rotating furnace. Detailed processing parameters were published previously /13/. After HDDR processing the resulting powder was hand crushed and coated with a thin organic layer. Silanes were used for this purpose. The experimental procedure is published elsewhere /14/. Coated and non-coated powders prepared by different routes and with different compositions were exposed to atmospheric conditions as well as more severe corrosive tests in a humidity chamber (Weiss) (95 % relative humidity and 40°C, 8 hours; ~ 40 % relative humidity and 25°C, 16 hours) in accordance with the DIN 50017 standard. The weight increase was followed and after the corrosion tests were completed, magnetic properties were measured and compared with the properties of the basic powders. The morphology of the powders was observed using a JEOL 840A SEM. The surface of the coated powders was analysed using high-resolution field emission AES (Microlab 310-F VG Scientific) combined with XPS. AES analysis was performed under standard conditions: a primary electron beam of 5 keV and the current between 1 and 10 nA. AES point analyses were performed on different grains of powder. Points for AES analysis were selected from SEM images with magnifications between 200 and 1000. XPS (X-ray Photoelectron Spectroscopy) of the same sample was used to determine the chemical state of the silicon. For XPS analysis MgKα radiation was used. In order to determine the nature of the bonding between the powder surface and the surface-active substance, FT-IR spectroscopy (Digilab FTS-80 spectrometer) in absorbency and diffuse reflection modes was used.

Results and discussion

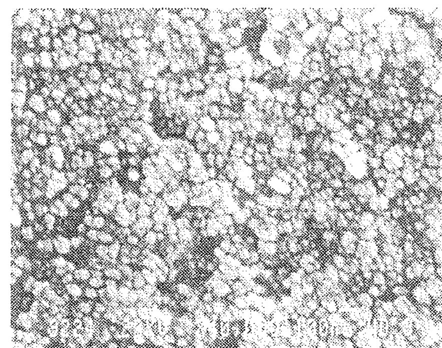

Fig. 1. SEM image of HDDR processed powder ($Nd_{15}Dy_1Fe_{75.3}Zr_{0.7}B_8$).

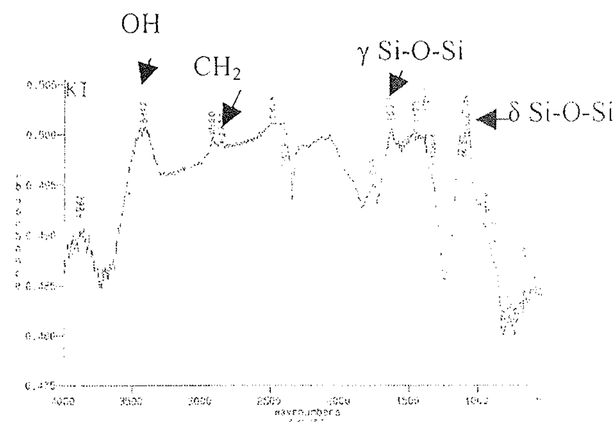

Fig. 2. FT-IR spectrum of the coated powder.

Figure 1 shows a SEM image of the HDDR processed powder. The thin organic layer cannot be seen from this image, but a simple experiment shows that the surfactant is successfully chemisorbed on to the powder surface. If the powder is mixed with water, uncoated powder sinks immediately, but coated powder is hydrophobic and therefore floats on the water. Powders coated by chemisorbed silanes are hydrophobic indefinitely, while powders with only physisorbed organic molecules are not sufficiently resistant to the water and sink after a finite time. It is known from previous work that if the temperature used for the chemical reaction is too low, the water molecules replace the organic molecules /12/. With AES analysis the presence of C and Si on the powder surface was detected. Adsorbed carbon from the air was removed from the sample surface by Ar ion sputtering. XPS analysis of the same sample

showed that peaks of Si 2s at 153.1 eV and Si 2p at 101.4 eV correspond to Si in silanes. Further analyses showed besides Si (2p 101.4 eV) also Fe (3s 92.6 eV), which indicates the thickness of the organic layer on the surface of the Nd-Fe-B powder. AES and XPS analyses show that the coated powder is covered with an ultra thin layer of organic material and one can estimate the thickness of this coating as a monolayer.

By using FT-IR spectroscopy on the powders observed in absorbency and diffuse reflection modes, we expected that the vibrational modes observed in the measured spectra could help to differentiate between species which are present on the surface and in the bulk of the crystallites. In order to distinguish between the surface of the powders with respect to the bulk, we measured the diffuse reflectance spectra of the powders. Polycrystalline samples were simply mixed with KBr without applying pressure, which may cause grinding and crushing of the powder particles. In such a way, the surface of the particles remained unaffected and the inner part of the bulk of the crystallites did not become exposed to infrared radiation when examined in the diffuse scattering mode. The spectrum obtained is shown in Figure 2. We can estimate the characteristic peaks for Si-O-Si groups (γ and δ), as well as CH_2 groups, which must be the consequence of some remaining organic surface modifying agent´s groups not used for the reaction. This can only indicate that the number of OH^- groups on the powder surface was a minimum, but enough for the reaction and consequently for the protection of the powder with a monomolecular layer.

Nanocrystalline powders with highly reactive surfaces react with the atmosphere immediately and most likely form a passivated surface of a thin NdO_x or/and Nd_2O_3 layer, corrosion does not proceed any further. Coated powders with silane showed a marginal weight gain (less than 0.01 %) in the first 50 hours of exposure to the severe corrosion conditions with complete passivation afterwards. One can conclude that not a 100 % coating of particles was achieved and those uncoated particles oxidise, which contributes to the observed weight gain.

Magnetic properties of the HDDR processed powders measured before the corrosion tests (844 kA/m) compared to the properties of the powders coated with silane and measured after the test (860 kA/m) show that coercivity did not change as a result of the chemical treatment. This makes the use of tested organic substances suitable for the coating of nanocrystalline Nd-Dy-Fe-B powders with a very thin (~10 nm) protective layer and without damaging the magnetic properties. With the very high resistance to corrosion of the coated surface in the first 20-hours free handling of the powder in laboratory atmospheric conditions (~ 40 % R.H.) is possible.

This is of great importance in the production where the handling of sensitive powders in the air without any consequences would contribute to the lowering of production costs. The above results imply that the starting powder is covered with a thin layer of hydroxyl groups that enable the adhesion of silane molecules to the powder´s surface. Presumably the Nd-rich phase has to be the reacting precursor for hydrolysis of the particle´s surface. Even with very careful handling of the powder in a protective atmosphere and/or liquid, a very small number of OH- groups in a protective gas or organic liquid are always present. It is not clear yet, if these groups adhere onto the extremely sensitive powder from the surrounding in spite of the very careful handling in the protective atmosphere throughout the processing. It seems to be more likely, that these groups proceed from the organic liquid used as a solvent for silane. According to the proposed reaction schemes, during the subsequent heating in vacuum, condensation takes place (water or alcohol molecules are eliminated) and the covalent bond forms.

Conclusion

Coating achieved by the chemical reaction between the Nd-Fe-B powder´s surface and silane molecules is a very powerful method for the protection of sensitive nanocrystalline powders. HDDR processed powders coated with stearic acid show a marginal weight gain (less than 0.01%) in the first 50 hours of exposure to the severe corrosion conditions. The weight increase after the corrosion test of the more sensitive mechanically milled powders coated with silanes shows a weight increase in the first few hours which is lower than 0.05%, suggesting that this coating has excellent prospects. The magnetic properties are not damaged and the coating enables free handling of the powder for at least 20 hours in air. The results achieved could be of great importance in production where the handling of sensitive powders in air without any significant degradation would contribute to a lowering of production costs.

Acknowledgements

Prof. Boris Orel is gratefully acknowledged for providing us with FT-IR analyses and fruitful discussions. Prof. Monika Jenko is gratefully acknowledged for AES and XPS measurements and the presentation of results. The Ministry of Science and Technology of Slovenia is gratefully acknowledged for the financial support necessary to carry out this program of research.

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Prispelo (Arrived): 15.10.99 *Sprejeto (Accepted): 25.11.99*

UDK621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 29(1999)4, Ljubljana

APPLICATION OF THICK FILMS IN LTCC TECHNOLOGY

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MIDEM´99 CONFERENCE
13.10.99 - 15.10.99, Ljubljana, Slovenia

Keywords: thick film materials, LTCC TECHNOLOGIES, Low Temperature Cofired Ceramic TECHNOLOGIES, HTCC TECHNOLOGIES, High Temperature Cofired Ceramic TECHNOLOGIES, MCM-C, Multi-Chip Modules Ceramics, TFM materials, Thick Film Multilayer materials

Abstract: Typical thick film materials are widely used in Low Temperature Cofiring Ceramics (LTCC) technology due to its low cofiring temperature. This is a great advantage of LTCC in comparison with HTCC multichip modules. Thick film materials give a possibility of making not only network of conductive paths in a package but also building other electronic elements and devices. The number of thick film materials with various electrical properties used in LTCC technology is growing. The properties of these elements are very promising. The paper gives a description of LTCC technology and thick film materials used there. The information on construction and properties of buried and surface resistors, thermistors, varistors, inductors and capacitors is given. Moreover, non-conventional application of thick film materials is presented.

Uporaba debeloplastnih materialov v LTCC tehnologiji

Ključne besede: materiali debeloplastni, LTCC tehnologije žganja keramike nizkotemperaturne, HTCC TEHNOLOGIJE žganja keramike visokotemperaturne, MCM-C moduli multichip keramika, TFM materiali debeloplastni večplastni

Izvleček: Tipične debeloplastne materiale na široko uporabljamo v LTCC (Low Temperature Cofiring Ceramics) tehnologiji zaradi nizkih temperatur žganja. To je ena od velikih prednosti LTCC tehnologije v primerjavi s HTCC multičip moduli. Dodatno debeloplastni materiali omogočajo poleg izdelave prevodnih povezav, tudi izvedbo drugih elektronskih elementov. Število debeloplastnih materialov z različnimi lastnostmi, ki jih uporabljamo v LTCC tehnologiji stalno rase. Električne lastnosti iz njih izdelanih elementov pa so zelo obetavne. V prispevku podajamo opis LTCC tehnologije, uporabo debeloplastnih materialov znotraj te tehnologije, kakor tudi informacijo o strukturi in lastnostih pokopanih in površinskih uporov, termistorjev, varistorjev, dušilk in kondenzatorjev. Dodatno opišemo še nekonvencionalno uporabo debeloplastnih materialov.

1. INTRODUCTION

Ceramic based multichip modules (MCM-C) have been used in the electronics industry for over 25 years /1/. Three ceramic based technologies are used to make MCM-C structures: Thick Film Multilayer (TFM), High Temperature Cofired Ceramic (HTCC) and Low Temperature Cofired Ceramic (LTCC) /1-4/. TFM is the oldest, and LTCC the youngest one of MCM-C. In TFM technology multilayer is processed serially - layer by layer. Each layer is printed and fired separately. In HTCC and LTCC technologies the process is carried out in a parallel way and all foils are cofired in a single step, building a multilayer structure. Materials of the foil and firing temperature are the main differences between HTCC and LTCC elements. HTCC foil consists of alumina and is fired at 1600 ÷ 1800 °C in hydrogen atmosphere. Only W and Mo can be used as conductor because of the high firing temperature. LTCC foils are made from alumina filled glasses or glass ceramic material. Typical thick film materials can be used, because foils are cofired at 850 ÷ 1000 °C.The paper presents steps of LTCC technology. The review of thick film integral passives and other elements and devices in LTCC technology is given.

2. LTCC TECHNOLOGY

Typical LTCC structure is presented in Figure 1. It consists of dielectric foils, external and internal conductors, surface and buried passive elements, thermal and

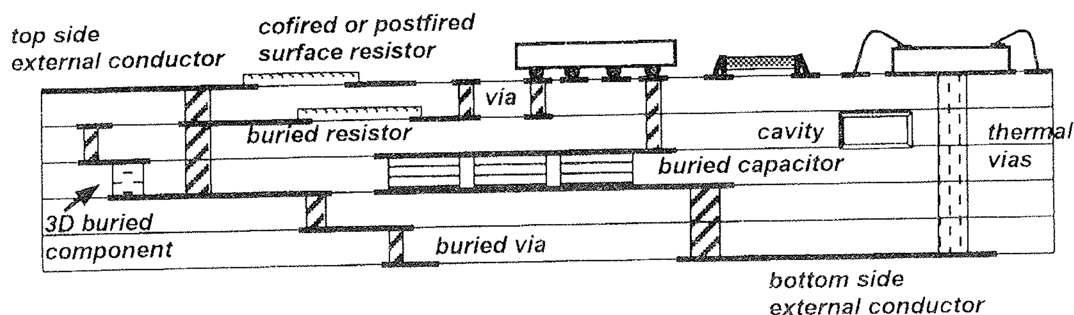

Fig. 1: Cross-section of a LTCC structure with integral passive elements

electrical conductive vias. Additional circuits and elements are added on the top of the structure using various assembling methods.

LTCC MCM-Cs have a number of advantages over HTCC structures. Because the cofiring process takes place at 850°C, typical thick film materials and processing are used. Metals of higher conductivity like gold, silver or copper replace tungsten or molybdenum. The basic LTCC ceramic foil can be modified producing dielectric materials with different electrical and physical properties. The dielectric constant can be varied in a wide range from 4 to 12000 /5/. The coefficient of thermal expansion can be adopted to match alumina, gallium arsenide, or silicon. Standard thick film conductor, resistor and capacitor materials are used in LTCC circuits as buried (2D or 3D) or surface elements. Lower mechanical strength and thermal conductivity are the main disadvantages of LTCC, in comparison with HTCC.

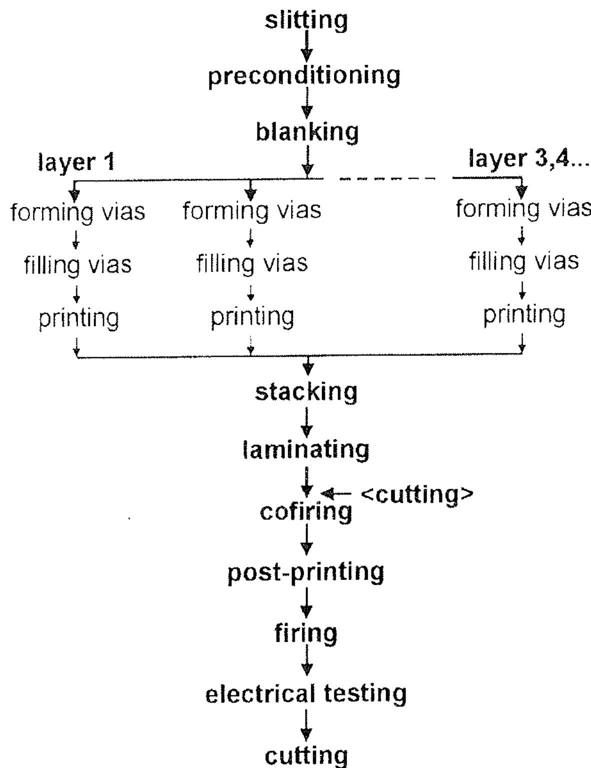

Fig. 2: Process flow diagram for LTCC

Two basic materials are used in LTCC fabrication – alumina filled glasses and glass-ceramic materials. Flow diagram of a typical LTCC process is presented in Figure 2. Tape is cast on mylar and stored in this way. After removing from the roll, the tape goes through a low temperature preconditioning bake to stabilise it. Then the tape is blanked to a specific standard size and registration holes are made. In the next step vias are formed in the individual sheets of tape by mechanical punching, drilling, laser formation or photo patterning. The vias are filled with a special via fill conductor inks (Ag or Au). The conductors and passive elements are printed by a standard screen printing method. After

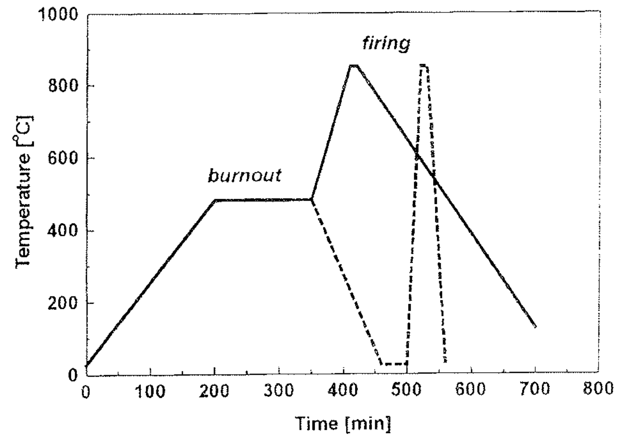

Fig. 3: Various cofiring profiles of LTCC

printing the cavities are made using automatic punch or laser. Finished sheets are stacked on a laminating plate and laminated in uniaxial or isostatic laminator. The typical laminating parameters are 200 atm at 70°C for 10 minutes. After the lamination process the structures are cofired in two steps (Figure 3). The first step, typical at around 500°C is the binder burnout step. The second, at 850°C, makes the ceramic material to densify. The firing process is carried out in one programmable oven or in two separate ovens. The second step can be made in an ordinary thick film furnace. The fired parts typically shrink 12% $\pm$0.2 in the x- and y- directions and 17% $\pm$2 in the z-direction. After cofiring and postfiring operations the structures are singulated using dicing saw, ultrasonic cutting, laser cutting or green tape punching /6/.Typical LTCC properties are presented in Table 1, whereas the design guidelines are given in Table 2.

The limitations of LTCC technology are shrinkage variations and poor thermal conductivity.

To eliminate shrinkage, some manufacturers have promoted a "tape-on-substrate" (called also "tape-transfer") technology /1,3,7/. Shrinkage is eliminated by laminating and firing each layer of tape on a substrate made of alumina, BeO or AlN. Sheets of dielectric tape, with performed vias, are registered and laminated to substrate at a fixed temperature and pressure. The tape adheres to the substrate and does not shrink in the x- or the y- direction. It shrinks only in the z- direction.

Another method of suppressing the lateral shrinkage for LTCC laminates of 15 layers or less is to fire the tape on suitably prepared thin metal plates of Cu-Mo-Cu /8-10/. Early in the sintering process the glass ceramic layer adheres to metal plate which totally suppresses the lateral shrinkage.

Using 0-shrinkage alumina foils on both sides of the structure allows to avoid the shrinkage of the LTCC structure. The foils are removed after the process by sunblaster methods /11,12/. The use of constrained sintering minimizes process shrinkage variability. Two methods of constrained sintering of LTCC are in use – pressure assisted constrained sintering (PAS) and

Table 1: Typical LTCC properties /1,3,6/

Material composition	Glass ceramic or alumina filled glasses
Coefficient of thermal expansion	3 ÷ 8 ppm/K
Thermal conductivity	2 ÷ 6 W/mK
Relative permittivity	4 ÷ 12 (1 MHz)
Dissipation factor	15 ÷ 30 x 10^{-4} (1 MHz)
Insulation resistance	10^{12} ÷ 10^{15} Ω cm
Breakdown voltage	800 V / 12 μm
Flexural strength	150 ÷ 250 MPa
Shrinkage z – axis x -, y – axis (tolerance)	15 ÷ 25 % 12 ÷ 16 % (±0.2 %)
Number of layers	1 ÷ 75
Thickness (fired)	95 ÷ 210 μm

Table 2: LTCC design guidelines /1,3,6/

Conductor material	inner Ag	3.3. mΩ/□ (6 μm)
	inner Au	5.0 mΩ/□ (6 μm)
	outer Ag	2.0 mΩ/□ (15 μm)
	outer PdAg	15 ÷ 40 mΩ/□ (15 μm)
	outer Au	4.0 mΩ/□ (8 μm)
	outer PtAu	80 mΩ/□ (15 μm)
	outer Cu	2.0 mΩ/□ (15 μm)
Resistor values	0.1 Ω ÷ 1MΩ	
	Standard	possible
Line width/spacing/pitch (min)	200/250/400 μm	100/100/200 μm
Via diameter/spacing/pitch	250/500/500 μm	125/300/300 μm
Via cover pad	2x via ϕ	1x via ϕ
Thermal via diameter/pitch	250/500 μm	600/1250 μm
Cavities min/max thickness	400/1500 μm	400/2500 μm
Cavities size min/max	1500/not limited μm	1000/not limited μm
Windows max depth	1000 μm	2500 μm
Windows size min/max	1000/not limited μm	500/not limited μm
Circuit size	≤5" x 5"	≤8" x 8"
Circuit thickness min	1 mm	0.4 mm

pressureless constrained sintering (PLAS) /13,14/. PAS technology was developed by Du Pont /15/ to sinter glass filled dielectric systems to full density at low temperatures (850°C), low pressure (<0.068 MPa) and short times (10 min). Firing requires sandwiching the unfired laminate between constraining die, a refractory porous plate, and a refractory porous release layer. PLAS technology does not require special tooling /11-13,16/. The laminate is sandwiched between refractory constraining tape layers on the top and bottom surfaces of the green multilayers before firing. After firing the refractory constraining the layers are removed. Shrinkage during firing for PAS and PLAS is only in the z- direction and is of the order of 41%.

LTCC's thermal conductivity of 2.0 ÷ 2.5 W/mK is a limitation to the structures dissipating many watts of power. The most common method of increasing heat transfer in the z-axis is through thermal vias /17/. Thermal vias are holes that are filled with silver or gold and

are placed beneath the hot components. The thermal conductivity in the z- axis can be improved to 120 W/mK or 70 W/mK in the case of Ag and Au, respectively /18/.

Another method of spreading the heat is by the application of a thick film layer of gold on the back side or by the use of "transfer tape" method on higher conductive materials such as copper tungsten (CuW 190 W/mK) and copper-molybdenum-copper (Cu-Mo-Cu 160 W/mK) /17/. The additional weight is the disadvantage of the using of those materials.

LTCC offers the possibility of fine lines and spaces. The following methods are used to achieve better resolution:

- fine line printing through steel screens or metal masks /19,20/,
- gravure offset printing /21-23/,
- photoimageable gold and silver FODEL inks /19,24-27/,
- photo-patterning process (etching) /28,29/,
- laser patterning /30,31/.

Moreover, after cofiring thin film deposition process can be used on the outer layer. However, it is a very expensive one, and the surface of the fired tape must be extremely smooth for good adhesion /17/.

3. INTEGRAL PASSIVES

Integral passives are defined as functional elements either embedded or incorporated on the surface of an interconnecting substrate /32/. **Discrete passive devices** are simply a single passive element (capacitor, resistor or inductor) in a leaded or surface mount technology (SMT) case. **Arrays** are multiple passive elements of more than one function in a single SMT case /33/. It is estimated that 1 trillion resistors and capacitors were built in 1997. Of that number, 55 billion were integrated into 11 billion arrays and networks. This doubles the number from 1996. The passive components technology roadmap predicts that the number of arrays and networks will grow to 15 billion replacing 75 billion discrete components in 1999 and to 32 billion replacing 160 billion in 2000 /33/. There are four great reasons for the integration: performance, cost, reliability and size /34/. The ratio of passive devices can be greater than 20:1 in some of today's high volume applications /35/. The PC microprocessor speed increased over the last 15 years from 4 to 4000 MHz and the microprocessor voltage has dropped by about 50%. Both these trends require much more passives /36/.

LTCC offers a possibility of high scale integration of passive components in one module. The elements can be made both inside the structure (buried) and on the top (surface) as presented in Figure 1. The buried elements are formed as planar (2D) or three – dimensional (3D) inside LTCC structure /37/. The basic electrical properties of 3D resistors, thermistors or varistors are similar to the planar ones /37/. The properties of LTCC integral passives are widely investigated. The aim of the research is to improve the element performance by a better understanding of the structure of LTCC system and the electrical conduction mechanisms in the components. In the Wrocław University of Technology the research is carried out on the properties of the integral passives in a wide temperature range (-180°C ÷ 130°C) /25,37-41/. We study also the influence of high voltage pulses on thick film integral resistors /41-43/ and long term stability of various integral passives /37,41,43/. Part of the investigation has been done as a close cooperation with Ilmenau University of Technology /41/ and Dresden University of Technology /25,40,41/.

Resistors

Cofired resistors must be chemically compatible with the material of the tape. The glasses in the resistors and in the tape interact with each other influencing the sheet resistance and Temperature Coefficient of Resistance (TCR). The electrical properties of the buried and the surface resistors are presented in /25,37,39,41,43-49/. The buried resistors can be trimmed by laser through the special hole in the upper foil, or through one thin layer /43,44,46-49/. The other possibility of trimming is by the use of the high voltage pulses. In this case deeply buried resistors can be trimmed without making any hole /42,43,46-50/.

Capacitors

The capacitors can be made by the following methods /47,51-56/:

- burried interdigital electrodes on one side of a tape,
- printing capacitor electrodes on both sides of a tape,
- filling vias with high permittivity materials,
- entering high ε tape into a hole in the typical low ε tape,
- adding thin tape with high ε.

Inductors

Inductors can be made as planar or 3 dimensional ones. The planar types are preferred for the coils, which are arranged serially to other elements and 3D – coils for inductors which are connected to the ground /22,47,52,53,56-60/

Transmission lines

Two types of integral transmission lines are made in LTCC technology: buried microstrip or the stripline realised as an off center stripline /47,58/.

4. OTHER APPLICATIONS

LTCC technology is now used not only for typical MCM applications as a package with conduction lines, but also for production of sensors or devices in the military equipment, avionics, medicine, automotive industry, wireless devices etc. The main reason for such wide area of application is their high reliability, hermeticity, usability of typical thick film materials and possibility of making 3D structure with various shapes and cavities inside.

The first application of LTCC in the sensors area was reported by Bansky et al. in 1993 /61,62/. They made multilayer green tape ion extraction optic with gold layers as grid for plasma application and reflection structure improving the performance of ion sources /61/. At the same year Bansky described 3D LTCC planar Langmuir sensor structure for plasma diagnostics /62/. Another 3D green tape sensor for "in situ" plasma diagnostics was made in 1995 /63/.

Platinum heater buried inside LTCC with a possibility of simultaneous measuring the temperature for gas sensor application is described in /64-68/. The tin oxide gas sensor design and properties are presented in /19,64,67,68/, the electrochemical ones in /69-72/. Thermistor based flow sensor made on LTCC in the meso scale microelectrochemical system is shown in /73/.

The temperature sensor on LTCC made by gravure offset printing with platinum line width 75 μm on 3.5x3.5 mm structure was presented by Leppävuori /21/.

The detailed description of the cavities technology is presented in /19,63,74,75/. It is very useful for making various sensors and devices. A very interesting application of cavities are active cooling systems /19,76/.

LTCC technology allows for easy making pressure sensors where piezoresistive effect is utilised /63/. The pressure sensor for the tissue pressure application in medicine is presented in /77/, whereas pressure/vacuum sensor in /78/.

A very interesting method of increasing current carrying capacity by making special ditches filled in with conduction material is presented in /79,80/.

Production of microwave devices is a great area for LTCC application. The design and electrical properties of various kind of thick film LTCC microwave elements are presented in /30,57,58,81-84/.

5. CONCLUSION

LTCC is one of the most important among MCM technologies for the future. This technology is used not only for typical MCM applications as a package, but also for sensors or devices in the military equipment, avionics, medicine, automotive industry, and wireless devices. The main reason for a wide area of application is usability of typical thick film materials, high reliability and good hermeticity. Standard thick film conductor, resistor and capacitor materials can be used in LTCC circuits as buried (2D or 3D) or surface elements. Moreover, a great advantage of LTCC is that the basic ceramic foil can be modified giving dielectric materials with different physical properties. The coefficient of thermal expansion can be adopted to match alumina, gallium arsenide, or silicon.

ACKNOWLEDGEMENTS

This work was supported in part by Wrocław University of Technology, Grant no 342 346

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Prispelo (Arrived): 15.10.99 *Sprejeto (Accepted): 25.11.99*

MICROSYSTEMS AT AUSTRIA MIKRO SYSTEME

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TUTORIAL INVITED PAPER
MIDEM´99 CONFERENCE - Workshop on MICROSYSTEMS
13.10.99 - 15.10.99, Ljubljana, Slovenia

Keywords: microelectronics, semiconductors, MST, MicroSystem Technologies, development problems, problem solutions, CMOS, Complementary Metal Oxide Semiconductors, magnetic sensors, IC, Integrated Circuits, HALL elements, mechanical systems, acceleration sensors, monolithic integration, CMOS compatible preprocessing, CMOS compatible postprocessing, bulk machining, MM, MicroMachining

Abstract: Based on the Microsystem development activities of Austria Mikro Systeme Int., the typical problems of Microsystem development and the most important solutions are presented for a microelectronic compatible manufacturing environment. With it, the paper describes CMOS-compatible products like magnetosensor ICs based on Hall elements, mechanical systems like acceleration sensors and specific pre and post processing process extensions with service possibilities for external organizations, which enable them to develop monolithically integrated Microsystems within a microelectronic manufacturing environment.

Mikrosistemi v podjetju AMS

Ključne besede: mikroelektronika, polprevodniki, MST tehnologije mikrosistemske, problemi razvoja, rešitve problemov, CMOS polprevodniki kovinskooksidni komplementarni, senzorji magnetni, IC vezja integrirana, HALL elementi, sistemi mehanski, senzorji pospeška, integracija monolitna, CMOS kompatibilno predprocesiranje, CMOS kompatibilno poprocesiranje, obdelava globinska, MM obdelava najfinejša

Izvleček: Na osnovi dosedanjih aktivnosti pri razvoju mikrosistemov v podjetju AMS, predstavljam tipične probleme in rešitve, ki smo jih uporabili pri vpeljavi tehnologije mikrosistemov v mikroelektroniki kompatibilno proizvodno okolje. V prispevku so predstavljeni izdelki kompatibilni s CMOS tehnologijo, kot so magnetosenzorsko integrirano vezje na osnovi Hallovih elementov ter nekateri mehanski mikrosistemi, kot je senzor pospeška. Opisani so tudi pred in po-procesni dodatki osnovni CMOS tehnologiji, vključno z nekaterimi zunanjimi uslugami, ki omogočajo izvedbo monolitnih integriranih mikrosistemov znotraj mikroelektroniki kompatibilnega proizvodnega okolja.

Introduction

Computers and communication technique created an information processing environment penetrating, more and more, all spheres of human activities. The performance of modern computers has grown over the last three decades with a speed unprecedented in the history of technique. Communication networks have extended not only the information transfer between individuals but have also created computer networks and clusters leading to an information processing power comparable with the performance of high developed living organisms. Assuming the same performance growth as in the past, the local processing power of parallel computers will reach the performance of the human brain within the next 10 years.The basis for this development is undoubtedly the microelectronics with its unbelievable capability to double the complexity of integrated circuits every 18 months. The DRAM-memory of the year 2010 is expected to have a capacity of 64 Gbit, which is nearly the amount necessary to store the information of the human genome.

Contrary to this, the complexity of technical sensing and actuating remains far behind the technical information processing capabilities. The human eye has more than 120 Mio rods and 7 Mio cones with up to 160 thousand receptors per mm^2. The human skin has 20 thousand tactile sensors per cm^2 plus nearly 1600 temperature, pressure and pain sensors on the same area - altogether nearly one billion sensors, all of them with complex transducing and signal processing capabilities. Even for technical vision, which represents the area of sensors with the highest technical integration level, the nature will remain an unreachable model for a long time yet. However, to our present understanding, an adequate and comparable integration level of sensors and actuators on the one side, and information processing on the other, is necessary for the development and implementation of really intelligent systems. Intelligence is not an information processing issue but the result of an evolution of systems, which are able to sense, to act and to process the information perceived from its environment and from the interaction with it. The first technological revolution has opened the way towards very large scale on-chip integrated information processing systems. The second Silicon revolution brings additional non-electrical functions like mechanical structures and multifunctional materials onto the same chip. Pressure and acceleration sensors, micropumps and valves, optical and RF blocks, chemical and thermal sensors, non-electrical interface elements and micro-actuators are monolithically integrated together with transistors and other electrical devices creating a new generation of integrated Microsystems. Chips emerge which are able to sense, to think, to act and to communicate. The first modest steps on the way towards really intelligent systems have been made.

However, presently the market success of Microsystems depends on the price/performance ratio of the new systems. Low production costs and mature manufacturing technologies are necessary preconditions for

the commercial success. Therefore, going back to the well proven and cost efficient microelectronic technologies and production plants was one of the most important ways towards the broad market penetration of Microsystems. For the Microsystem technologies, microelectronics offers a unique basic material – the Si -, a variety of additional materials, powerful technologies for the construction of planar structures, mature test environments as well as a lot of packaging and assembly technologies.

Some of the microsystems like temperature sensors or special magnetosensors can be created by using these microelectronic technologies without significant extensions. Most of the microsystems however, require additional possibilities to build three-dimensional structures and often need new materials. An extension of the microelectronic technologies is inevitable.

2. Microsystem technologies

2.1. Principles of Microsystems

There are a lot of physical effects which can be used for the transformation of mechanical, magnetic, thermal, chemical, optical and electromagnetic impacts in electrical signals and vice versa. For instance, mechanical deformations can be transferred in capacitance or resistance changes or can be measured by using the piezoelectric or piezoresistive effects.

Magnetic fields can be measured using the Hall effect, the Gauss-effect, magnetoresistive changes, and the Wiegand-effect or inductance changes. Thermal values are captured by using the thermodependence of resistors, the thermoelectric (Seebeck) effect, polarization changes in crystals (pyroelectric effect), and temperature effects in semiconductors etc.Optical and infrared radiation can be transformed into electrical signals using internal and external photoeffects in semiconductors, changes of the photoresistance, or the photovoltaic effect. For chemical and biological values, a broad spectrum of mass or conductivity changes, as well as the gas-sensitive field effect, or the Volta effect can be used.

Part of these effects is reversible and suited for the generation of actions (forces, fields, deformations, motions and radiation).

However, all the well known manifestations in the macroworld and properties of these effects can not simply be transferred into the world of Microsystems. Microsystems are not only small macrosystems but are often dominated by effects negligible in a macrosystem environment. New and unknown phenomena appear which have to be understood.

In the world of Microsystems, the relation between gravitational and inertial forces on the one side, and adhesive and frictional forces on the other, changes dramatically. Volume and mass of moving microparts shrink with the third power of the dimension, while the surface-proportional friction and stiction decreases with the second power only. Surface effects increasingly exceed inertial effects. The missing inertia of flywheels for example makes it difficult to get a smooth rotation of micromotors and requires multiple stimulation of the rotating part within one turn.

Very often already for parts as small as tens of micrometers , forces caused by adhesion, capillary tension and friction begin to dominate and dictate the construction of the microsystem. A well known and feared effect in micromechanical systems is the Stiction –Effect, a combination of adhesive and frictional forces, which lead to an undesired sticking of moving parts at surfaces of the Microsystems. Due to the complicated dependency of the adhesive forces on the surface state and the remaining liquids, this effect is difficult to cope with. Parts may become useless within the manufacturing process especially during the removal of etchants, surface tension of which lets stick two parts. More dramatically, Microsystems like airbag sensors may become defect during exploitation losing their function after the functional part sticks to surfaces in its vicinity. Low-tension surface layers are able to reduce the adhesive forces by some orders of magnitude and can reduce the risk of failures after shock-like mechanical loads.

However, the high adhesive forces may have a positive impact, too. They can be used for handling fluids in new microvalves and pumps. Electrostatic forces also offer new possibilities.

Generally, a better understanding of surface energies, stiction, friction and lubricant free wear in microdimensions is necessary.

Surface interactions are often the key for chemical microsensors. Usually, chemical sensors are based on electrochemical, optoelectrical or surface acoustical transducer effects. The transfer response of such systems is changed by the corresponding chemical components. For the detection of individual components, a selective embedding of the corresponding molecules into the basic structure is required - a process mainly based on surface sensitive interactions.Other separation techniques are based on the different transit times for different chemical components passing microchannels. These differences are caused by the different surface chemical bindings.

Completely new structures are needed for microoptical systems. Traditional approaches for manufacturing of laser diodes, photorecievers, optical switches, filters, modulators, mirrors, diffractive gratings etc. are based on the usage of the corresponding best suited materials like compound III/V semiconductors or special crystals. However, due to technological reasons, the monolithic integration limits the spectrum of usable materials and methods of structurisation already. Consequently, new developments are orientated towards monolithic integrated lenses, diffractive gratings and other optical elements that are based on digital structures in the sub-wavelength area. Photonic lattices (periodic structures of posts or beams in the sub-wavelength area with directional or wavelength selectivity allowing the construction of filters, mirrors, resonators or prisms) or monolithic integrated lasers like VCELs (Vertical-cavity surface-emitting lasers) as well as other elements allow the on-chip integration of complete systems for optical communication and analysis and follow the same trend.

3.2. Monolithic Integration of Microsystems

The overwhelming part of Microsystems developments in the last 20 years have followed the classical approach of developing discrete sensor and actuator components and integrating them together with signal and information processing ICs on the package level in the final system.The on-chip monolithic integration of Microsystems is mainly cost driven. Monolithic integration leads to less packaging and interface costs. Additionally, volume, weight and power consumption can be reduced. The reliability increases mainly due to the reduction of the number of bond wires and mechanical connectors. On-chip integration of sensors and signal conditioning is often crucial for robustness against electromagnetic disturbances and for high sensitivity/low noise applications.

On the other hand, for small volumes of monolithic integrated Microsystems, the unit costs are often higher than for hybrid, package level integrated systems because the cost potential of the microelectronics usually only becomes effective for relatively high volumes. Computer aided Microsystems design and reuse of cells and macros will close this gap in the future.

The elements described in 3.1 and the effects on the monolithic integration of Microsystems require well defined, customized geometric structures, which usually cannot be directly realized by standard microelectronic technologies. For instance, a simple, one sided clamped beam with additional mass on the other side for acceleration measurement cannot be manufactured using the well established microelectronic technology flow of repeated cycles for planar layer deposition, photolithography exposition and material removal. Consequently, technology extensions of the basic microelectronic technologies are needed to fabricate monolithic integrated Microsystems.

The most important requirement for developing technologies for monolithic integration is the closeness to the well established microelectronic manufacturing technologies because any deviation from proven manufacturing steps and established materials may jeopardize the whole production or will require a great effort to verify a riskless compatibility with the basic technology.

3.3. CMOS Pre- and Postprocessing

The compatibility requirement with respect to Microsystems-specific process and material extensions of basic microelectronic processes represents the fundamental challenge for the monolithic integration of Microsystems. It includes the request for separate handling of special process steps, which can be realized most easily as Pre- or Postprocessing. These process steps should not in any way destroy, or even only degrade the devices built up within the basic process. This means, for instance, that only temperature treatments within the allowed temperature budget of the basic process are possible.

For instance, one of the most frequently used materials for mechanical structures is polysilicon. To eliminate the stress within thin polysilicon beams, membranes or fingers, a high-temperature annealing process around 1000 °C is necessary; otherwise, the structures will bend, curl and show mechanical properties which are difficult to predict. However, temperatures of 1000°C exceed the melting point of the aluminum connections and destroy the chip. Additionally, junctions will be driven deeper into Silicon and diffusion profiles will change. Consequently, it was necessary to develop low temperature annealing processes or to use metallic materials like tungsten with higher melting points.

Over the last few years, PolySiGe became more and more favorable because it can be manufactured nearly stress free at temperatures below 650°C. Additionally, the thermal conductivity is lower then with polysilicon and allows the creation of thermally isolated elements like Infrared sensors.At Austria Mikro Systeme Int. we solved the problem of polysilicon stress of beams and membranes by using a separate body of bulk Si carrying the polysilicon structures. This sensor die is than connected to the IC by a special soldering procedure. The high temperature annealing process allows to tune precisely the remaining stress and to set a well defined, reproducible bending of a beam.

A second problem is the material incompatibility: Foreign materials which are used as structural components of the Microsystems or as technological tools like etchants, gases etc. have to belong to the class of CMOS-compatible materials, otherwise, their integration has to be realized in strict separation from the basic CMOS process.

Considering these basic limitations, it was necessary to extend the traditional microelectronic technologies with respect to the creation of different transducer and actuator components on-chip.

The first high volume manufacturing technology for Microsystems was the wet chemical anisotropic etching of monocristallyne Silicon – the so-called Bulk Micromachining. It is based on the differences of the etch rates of alkaline etchants like KOH along the different crystal planes. Anisotropic active etch solutions have a two order of magnitude higher etch rate in the <110> and <100> direction than in the <111> direction. In (100) and (110) Silicon, they can create structures lateral borders of which consist of {111}planes. These planes establish a well-defined angle with the crystal surface: for (100) Si – 54,7°.

Photolithographically structured etch stop layers can be used to form cantilever beams, membranes or other fine structures.

This Bulk Micromachining process can also be used as a process subsequent to the CMOS-fabrication (CMOS compatibility). Front and backside etching is possible.

KOH slightly attacks Sioxid, is CMOS incompatible and therefore can only be used for backside etching, whereas the toxic EDP (Ethilendiamin based) which slightly attacks the Alu-metallisation as well as the TMAH (Tetramethylammonium) can also be used for front side etching.

CMP Grenoble (Circuits Multi Projects) and Austria Mikro Systeme Int. offer an integrated Microsystems process with Front Side Bulk Micromachining. This process is based on the 0,8 μm CMOS and BiCMOS

processes of AMSInt and on a corresponding postprocess of CMP. It is also part of the EUROPRACTICE Service.

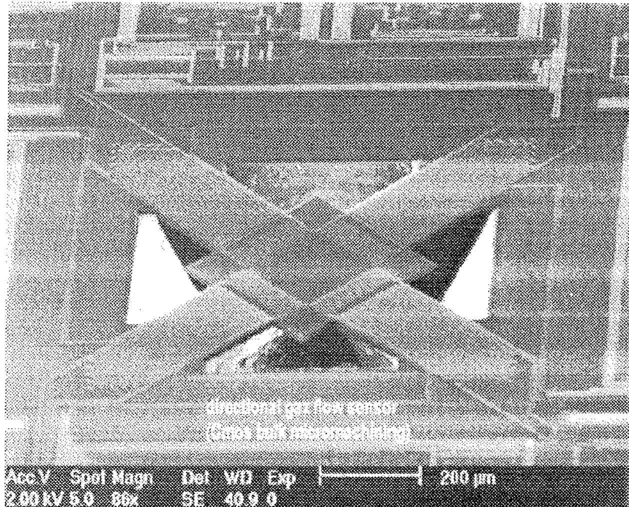

Fig. 1: *Gas Flow Sensor (by courtesy of CMP)*

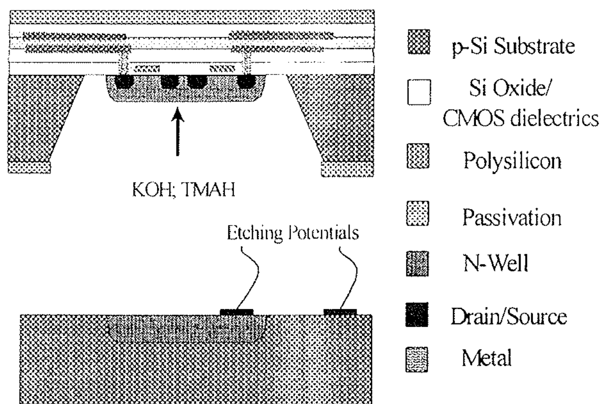

Fig. 2: *Bulk Micromachining with elektrochemical etch stop*

In the last few years, a great number of microsystem prototypes and small volume products were developed using this process.A typical example is the Gas Flow Sensor shown in Fig.1. The working principle is based on the measurement of the temperature differences of a locally heated gas flow. For reasons of thermal isolation, the whole system is placed on a membrane.

Very precise etch stops can be realized at reverse biased pn-junctions. Austria MikroSysteme Int. and the ETH Zurich developed a corresponding Back-Side Bulk Micromachining process which is used for different sensor developments.

In Fig. 2 the principle of the electrochemical etch stop is presented: the p-substrate and the n-doped well, which normally represents the active area for the implementation of the p-channel transistors, are supplied by appropriate potentials. These potentials guarantee a precise etch stop during the KOH etch process. They are initially applied to all dies using a wafer level connecting network (see Fig. 3). Within the dies, the potentials are applied to the stop-wells and to the substrate by metal connections corresponding to the chip level design rules. This process is available for all CMOS and BiCMOS processes of Austria Mikro Systeme Int. between 2 μm and 0.8 μm.

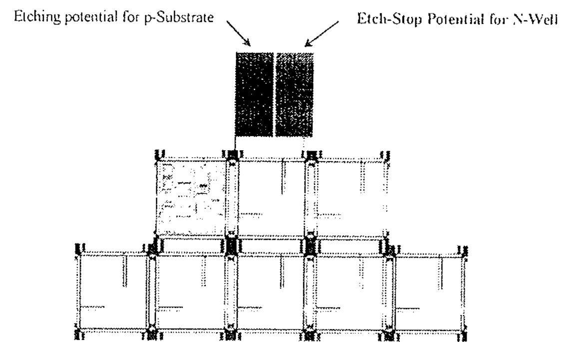

Fig. 3: *Connecting network*

Besides Bulk Micromachining, the structuring of surface layers – the so-called Surface Micromachining – has become a widely used technology. One of the first monolithically integrated Microsystems in volume production was the capacitive accelerometer of Analog Devices manufactured with surface micromachining technologies.

The basic idea of surface micromachining is the usage of sacrificial layers to form freestanding structures like beams. For instance, sacrificial layers can be the dielectric layers of the basic CMOS process (SiO_2) or the first metal layer (Alu). Buffered with ammonium fluoride, flour acid is well suited for the release of polysilicon structures by etching away the surrounding dielectric layers. In case of metallic sacrificial layers, all metal contacts on the surface have to be carefully protected by photoresist, leaving only the access openings to the sacrificial layer unprotected.

Usually both techniques can be combined and are performed as postprocessing steps with the fully processed CMOS wafer.

However, to make high temperature annealing possible, the surface micromachining should be integrated into the CMOS process before deposition of the metal layers. Care has to be taken in this integration to control the additional diffusion during the high temperature steps, which may enlarge the source- drain areas up to transistor shorts. Special deposition steps for low stress polysilicon deposition lower the requirements for high temperature treatment and ease this integration.

The preprocessing of micromechanical structures may cause considerable difficulties for the subsequent processing of active devices and connections. Destroyed planarity is one of the reasons. Sacrificial fillings of the

prefabricated cavities are complicated and expensive. Such processes are used only in singular cases.

Micromachining technologies based on Reactive Dry Etching (RIE-Reactive Ion Etching) or deep RIE have reached a broad acceptance in the last years. A decisive factor for high aspect ratios and etch deepness in Si is the formation of the passivation layer on the etched walls to avoid further lateral etching.

In the case of anisotropic etching of dielectric layers, the top metal layer can be used as etch mask.This means that no additional mask is required. By combining the deep RIE through all dielectric layers of the CMOS wafer with a subsequent Si underetch process, one can release complete sandwich structures as shown in Fig.4. These sandwiches may contain metal or/and polysilion structures and offer wide possibilities for the creation of complex micro-structures.

With the cooperation of partners Austria Mikro Systeme Int. is considering the preparation of a corresponding process service.

High Aspect Ratio Micromachining

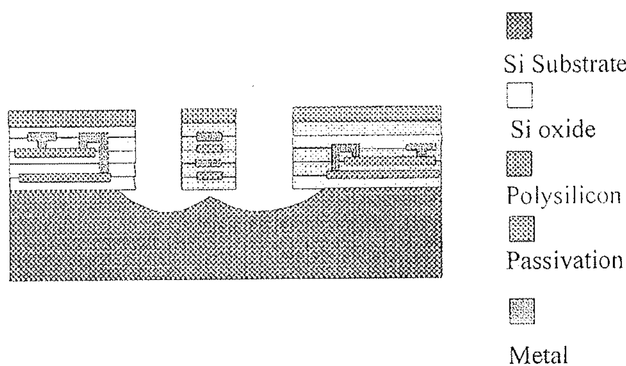

Fig. 4: Deep RIE based Surface micromachining

The spectrum of wafer level Microsystems technologies is much broader than the described methods.

For instance, the well-known LIGA process allows the realization of extremely large aspect ratios. However, many of these technologies are very special and only seldom suited for a cost efficient production. Additionally, often they do not allow the integration of signal and information processing blocks on the same chip.

This lack of monolithic integrability is also especially true for many of the joining technologies like Silicon Fusion Bonding or Field Assisted Bonding where sensor chips or Si wafers are connected with glass or Si. Planar surfaces in close mechanical contact are needed for this kind of joining technologies. Therefore, a hermetical connection of an IC surface with a corresponding Si or glass top part is difficult due to the insufficient planarity of the IC surface. Generally, the major problem of Microsystems development is packaging, including first level packaging.

ICs only need electrical and thermal contact to the environment. To a great extent, they can be protected from other environmental impacts. In contrast, Microsystems like pressure sensors, flow sensors, optical components etc. often need a direct contact to the environment. The packages have not only to protect the system, but also to guarantee a well-defined access to the outer world.

But even if no additional contact is necessary, the fragile microstructures are difficult to protect during wafer sawing and packaging. Consequently, dicing becomes more complicated and the clean room requirements for Microsystems assembly are usually stricter than for ICs.

However, the main problem is the cost. For microelectronic devices, plastic packages often represent the most cost efficient solution. Special assembly technologies, leadframes, mold materials, coating and soldering techniques allow the realization of dedicated plastic packages for different space and topology requirements, pin counts, thermal resistances, temperature ranges, humidity protection etc. The relative insensitivity of digital ICs to the internal package stress and –more important- to stress changes, is one of the preconditions for such solutions. In contrary, some analog devices like bandgap references and, to a much larger extent, many Microsystems are extremely sensitive to stress. This stress sensitivity makes the plastic packaging of many Microsystems like stress sensitive mechanical or magnetic structures, a very challenging task. Many promising Microsystems projects failed due to problems with finding cost efficient package solutions. This is true not only for monolithic integrated systems but also for discrete and hybrid approaches. When commencing with the development of Microsystems, it is necessary to include the development of the package concept and its verification from the very beginning of the project.

4. A new accelerometer

Analog Devices developed the first monolithic integrated, commercially available accelerometer sensor for airbag release. It is based on the measurement of the capacitance changes which are caused by the in-chip plane movement of a finger-like structure relative to the opposite fingerlike electrodes. The whole structure with the fixed parts, as well as the movable part suspended by springs is manufactured by a special surface micromachining process embedded in a CMOS process, with a total of 23 masks. The process is complicated, as the structure is yield critical and endangered by the sticing effect. Other manufacturers like Sensonor, Temic or Bosch also offer hybrid or integrated solutions.

Austria Mikro Systeme Int. has developed a prototype of high performance low cost accelerometer sensors. The goal was to develop a customizable sensor module and a corresponding control and signal conditioning module which could be adapted to the different requirements, such as different measurement ranges (from Low G sensor for 2-3 g until High G sensors for up to 200 g) and different accuracies.

The principle of the system is shown in Fig. 5. The sensor module consists of an elastic polysilicon beam over a cavity and represents the top die of the two

component system. A two-mask Front Bulk Micromachining process releases the beam. The bottom die consists of the ASIC part including sensing, actuating and reference electrodes as well as all control and signal processing electronics. The signal interface between both of the components is the capacitance between the polysilicon beam and the sensing electrode of the ASIC part.

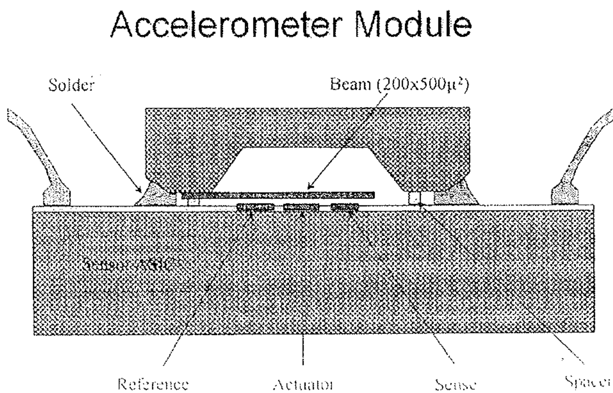

Fig. 5: Principle of Austria Mikro Systeme's accelerometer sensor module

The capacitance measurement allows the exact determination of the distance between the beam and ASIC and in particular, the distance changes caused by accelerations perpendicular to the chip plane. The measurement is realized with accuracies in the area of some ato-Farad (10^{-18} Farad) and includes the elimination of the parasitic, signal dependant capacitances. The high precision measurement method was developed in cooperation with the Laboratory of Electronics of ULM.

The acceleration measurement is performed in closed loop operation, where the beam is fixed with high accuracy in a predefined bended position by the electrostatic force of the actuator. The control signal within the loop is linearly proportional to the acceleration of the beam.

The prebending of the beam guarantees a sufficient return force to eliminate instabilities caused by large excitations in the direction of the sensing electrode. For an acceleration range between + 50 g and -50 g, the beam has a thickness of 1 μm and a size of 500 x 200 μm^2 (see Fig. 6). The noise of the system is better than 0,1 g (peak to peak) for 200 Hz bandwidth.

Selftest of the system is realized using the actuator electrode.

The stress of the polysilicon beam is exactly controlled by a high temperature annealing process. Together with an exact distance control of the two dies, this allows an accurate positioning of the tip of the beam with respect to the surface of the chip. The sensor IC is manufactured in standard CMOS process with Solder Bump Post-processing extension. This manufacturing concept is insensitive against process variations. Customer specific information processing can be easily realized. The enormous shock resistance and robustness against electromagnetic disturbances are additional advantages of the concept. Stiction effects are completely excluded.

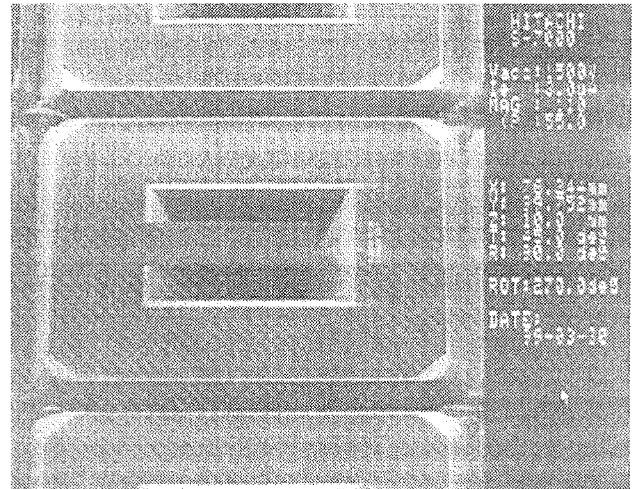

Fig. 6: Etched polysilicon beam

The system can be assembled in standard plastic packages or in special SIP packages, which are mounted perpendicularly to the PCB-surface.

5. Magnetosensors

Magnetosensors are a good example for the monolithic integration of Microsystems formerly realized mainly by discrete components like Hall or magnetoresistive sensors. Especially in case of Hall sensors, the monolithic integration can be realized using standard CMOS processes. On-chip magnetoresistive sensors or Flux Gate Magnetometers require additional deposition of permalloy or other magnetic materials, which can be performed on top of the dielectric layers or the planarized and finalized chip surface.

Austria Mikro Systeme has concentrated its efforts on the development of integrated Hall sensor systems. Hall Sensor ICs are used for angular, position, current and field measurements or as magnetic switches in machinery, automotive environment, white and consumer goods etc.

In comparison with discrete Hall elements monolithic integrated Hall sensor ICs are better suited for many applications, because build in offset compensation, calibration and application specific trimming as well as array topology adaptation to the external field can be realized more easily.

In Fig. 7 the principle of the Hall element is presented. The magnetic induction B via Lorentz forces affects the current I through the plate, generating the Hall voltage V_H which is perpendicular to the orientation of the magnetic field and the current. This voltage is inversely proportional to the carrier concentration n. Therefore, for the practical exploitation of the Hall effect semiconductors are the best-suited materials (R_H-Hall factor,

G-Formfaktor, τ - average time of free carriers between two collisions which depends on their energy). For instance, doped Silicon like a n-well in p-Si forms an appropriate Hall plate, which only yet has to be contacted. This horizontal Hall element is sensitive against magnetic fields perpendicular to the surface of the integrated circuit.

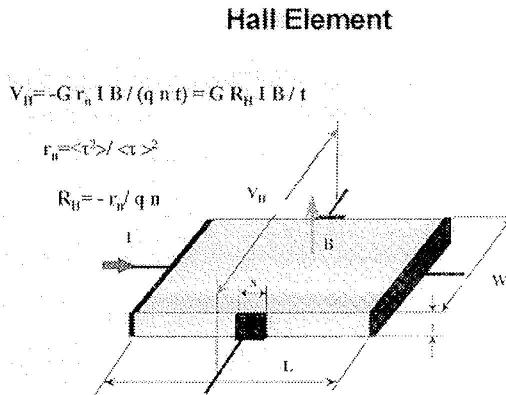

Fig. 7: Principle of the Hall element

The basic problem of all semiconductor Hall elements is the large, temperature dependent offset signal at zero induction. It is mainly caused by piezo effects within the crystal and by anisotropic geometric mismatches and doping gradients. It is stress dependent. The offset compensation is based mainly on the so called spinning current principle, which can be much more easily implemented on-chip than with discrete Hall elements. The idea behind this is the switching of the current direction through the Hall plate using different configurations of the plate with 2, 4, 6 etc. contact pairs and averaging of the Hall voltages over one turn. Sometimes Hall plates with different orientations arranged closely to each other are used synchronously assuming a nearly homogenous stress field over short distances. A solution patented by ETH Zurich solution is based on a continuous rotation of the vector of the current density by applying periodical supply currents to both of the contact pairs and measuring the Hall voltages between the same contacts. Generally, depending on the crystal orientation, suppression rates in the range of three to five orders of magnitude can be reached.

Another problem is the stability of the intrinsic sensitivity of the Hall elements. First of all, the sensitivity depends on temperature changes of the Hall coefficient itself, on the impact of the stress or stress changes on the Hall effect (the Piezo- Hall effect) and on the piezoresistive (stress-dependent) changes of the Hall element (strain gauge effect). Especially during packaging the stress conditions may change considerably changing the overall temperature behaviour of sensitivity.

If the measurement can be interrupted by calibration intervals, sensitivity changes can be measured and corrected using calibration coils around the Hall elements. A very precise voltage or current reference as well as relatively high calibration currents are requested.

In many cases for technical and cost reasons, the stress dependence has to be eliminated by appropriate packaging.

Austria Mikro Systeme Int. has specially developed very thin packages for Magnetosensor ICs. Here, the single in line arrangement of the pins allows using these packages for small magnetic gaps or mechanical slots. Temperature and reliability ranges typical for automotive applications are covered.

A great advantage of integrated Magnetosensors is the possibility to design array topologies, which are well adaped to the structure of the magnetic field to be measured on chip.

An example is shown in Fig. 8. Here, the angular measurement is based on the evaluation of the magnetic field in all four quadrants. The vertical components of the magnetic field under the magnet change periodically with the rotation angle. The point by point measurement of the field is substituted by a multiple measurement with higher accuracy and robustness against eccentricities. Of course, the measurement in any of the quadrants may again be a distributed measurement by sensors arranged along segments and followed by a weighted or unweighted summing of the component signals.

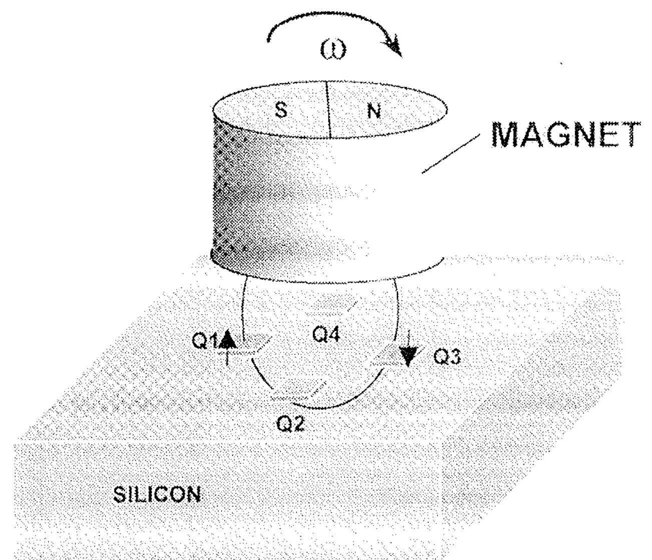

Fig. 8: Measurement of absolute angle using lateral Hall elements

AMSInt has also successfully used the principle of array measurement for the determination of the relative angular position where a multi-periodic field is generated by pole pairs arranged along a full circle. In the case of current measurement, this principle is extremely useful: using a corresponding sensor arrangement for the differential measurement of the field on both sides of the current conductor can eliminate external-disturbing fields.

Application specific sensor arrays on-chip, high performance compensation circuitry for the elimination of offset and temperature dependencies of sensitivity, pro-

grammability of dynamic range, of bandwidth and temperature behaviour, on-chip generation of magnetic fields for test and in field calibration, special packages, 3 D magnetic measurement capabilities for system design support – these are the techniques used respectively developed at Austria Mikro Systeme for the creation of customer specific solutions. Some of the methods are the result of the EU funded ESPRIT project MagIC and of the close cooperation with research institutes like ETH Zürich and University of Ljubljana.

As mentioned, the used lateral Hall elements are sensitive against the magnetic field component that is perpendicular to the chip surface. In some cases the parallel measurement of both in plane field components would be beneficial. For instance, the both components of a homogeneous field parallel to the chip surface could be measured allowing deriving the angular position of the chip relative to the field orientation. The implementation of the corresponding vertical Hall elements requires special technology steps. Austria Mikro Systeme Int. and ETH Zürich developed prototypes of vertical Hall elements which were realized by preprocessing steps consisting of the etching of two parallel, deep trenches, subsequent n- diffusion via the walls and isolation of the created perpendicular plate by oxidation. The trenches are filled with polysilicon.

Today, integrated Magnetosensors are mainly based on Hall elements and magnetoresistors.

Roughly one third of the worldwide market are magnetoresistive systems. Emerging products are based on integrated Flux-Gate magnetometers /4/, NMR systems / 5 / and magneto-mechanical resonators, which are opening the way to considerably higher sensitivities.

Austria Mikro Systeme offers not only its system and implementation competence to its customers but permanently completes its technological base in the magnetosensor area by acquiring and developing newest sensor principles and devices.

6. Conclusion

The monolithic integration of sensors, actuators and information processing on-chip is one of the main trends in the Microsystems area. The base is formed by the well-established microelectronic technologies that are properly extended for the integration of mechanical, optical, chemical and other functional elements. To use the cost advantages of the established microelectronic manufacturing equipment and infrastructure, the additional Microsystems-specific technology steps must be at least CMOS compatible.

Based on its high flexibility and the availability of all technological steps from design over mask production, chip manufacturing, test and assembly under one roof Austria Mikro Systeme Int. follows the sketched approach of CMOS compatible pre and post processing. In the first step, fully CMOS based sensors like horizontal Hall Plates and photodiodes were used to create a design and application environment for monolithically integrated Magneto and Opto Sensor Systems for absolute and relative angular measurement, position measurement, field measurement and magnetic data transmission. Especially for Magneto Sensor Systems well characterized sensor models, and a special library including different Hall structures, spinning current offset compensation blocks, on-chip field generators, different arrays for angular and field measurement, temperature compensation systems, field programming blocks etc, were developed. Special packages, test and evaluation techniques support the system design and application.

In a second step – which was practically done in parallel – Austria Mikro Systeme Int. introduced the surface and Bulk Micromachining technologies, most of them in cooperation with partners like CMP and ETH Zürich. The in house technologies were used for the development of mechanical sensors like a new accelerometer module. A special electrostatic etch stop technique was developed for backside bulk micro machining, which allows the manufacturing of very precise Si-membranes or beams.

The strong emphasis of monolithic integration and a high degree of CMOS compatibility for well selected Micro system products and market segments within the focus areas of the company are the guidelines for the present and future development of Microsystems at Austria Mikro Systeme.

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Prispelo (Arrived): 15.10.99 *Sprejeto (Accepted): 25.11.99*

CMOS PROCESSES AS BASIS FOR MICROSYSTEM TECHNOLOGY

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TUTORIAL INVITED PAPER
MIDEM´99 CONFERENCE - Workshop on MICROSYSTEMS
13.10.99 - 15.10.99, Ljubljana, Slovenia

Keywords: CMOS, Complementary Metal Oxide Semiconductors, MST, MicroSystem Technologies, IC, Integrated Circuits, mass production, monolithic integration, transducers, sensors, actuators, imagers, miniature displays

Abstract: CMOS ICs have become the dominant technology in the semiconductor industry and will continue to be the fastest growing segment. At IMEC we try, for our R&D work in the microsystems technology (MST) field, to built as much as possible on the know-how and infrastructure available at IMEC for the development of CMOS process steps, modules and fully integrated processes. Monolithic integration is pursued by industry for mass-produced transducers or for microsystems with large array of sensors or actuators. Today´s monolithic devices include visible and IR imagers, miniature displays, biochemical, pressure, flow and acceleration sensors. The application of technologies developed for CMOS are not limited to monolithic integration alone. They can also used to improve the performance of the more classical micromachining technologies. The present paper gives an overview of work in this field at IMEC.

CMOS procesi kot osnova tehnologijam za izdelavo mikrosistemov

Ključne besede: CMOS polprevodniki kovinskooksidni komplementarni, MST tehnologije mikrosistemske, IC vezja integrirana, proizvodnja množična, integracija monolitna, pretvorniki, senzorji, aktivatorji, upodabljalniki, zasloni miniaturni

Izvleček: CMOS je postala dominantna tehnologija v polprevodniški industriji in bo še nadalje predstavljala njen najhitreje rastoči del. V IMECu si prizadevamo naše raziskovalno delo na področju tehnologije mikrosistemov čim bolj osnovati na znanju in infrastrukturi, ki je že na razpolago. oz. nam jo nudijo že razviti procesni moduli in CMOS tehnologije. Monolitno integracijo danes industrija potiska v ospredje predvsem zaradi množične proizvodnje pretvornikov, oz. mikrosistemov z velikim deležem površine senzorjev in aktuatorjev. Današnja monolitna integrirana vezja vsebujejo IR detektorje slike, miniaturne prikazalnike, biokemične senzorje ter senzorje pritiska, pretoka in pospeška. Vendar uporaba tehnologij razvitih za CMOS vezja ni omejena samo na opisano. Lahko jih uporabimo tudi za izboljšanje delovanja bolj klasičnih mikromehanskih tehnologij. Namen tega prispevka je prikazati tovrstna prizadevanja in aktivnosti v IMECu.

1. Introduction

Sensors and actuators transform an input signal to an output signal. In case of a sensor, the input signal is e.g. optical, chemical, the output usually electrical. In most system applications, the transducer is complemented by dedicated electronic circuitry for output signal treatment. The interconnection between both is either done by hybrid mounting (flip-chip, wire bonding) or by monolithically integrating transducers and transistors on the same Si-substrate using a dedicated process flow. This is feasible because many transducers use similar process technology as microelectronics, namely planar thin film processing.

Monolithic integration has substituted the hybrid approach in some but not all cases. The hybrid approach will continue to co-exist because of its specific merits. Hybrid integration allows an independent optimisation of the technology and specifications for the electronic circuitry and the transducer. Further, the longer development cycle of monolithically integrated transducers, due to the lengthy and complicated process sequences (typically 15...20 mask levels), implies a longer time-to-market.

There are two typical situations where monolithic integration is generally preferred. If the transducer is used as a transducer matrix array, containing thousands up to millions of identical pixels, these pixel signals have to be multiplexed in order to reduce the number of output connections to a reasonable level. This massively parallel interconnection can not always be realised by flip-chip techniques, because of the technological limitations (pitch, yield, reliability, ...) that arise for large pixel numbers and densities. The other advantage of monolithic integration is towards mass-production. Silicon transducer markets vary in size from niche-applications where a few 10000´s of devices a year are made, up to mass-applications in the automotive or consumer sector where 10´s per millions/year are produced. For the largest markets, economics often dictate the monolithic solution because the reduced assembly and packaging costs outweighs the increased process cost.

At IMEC we focus on the development of fabrication technologies for microsystems. Since the background and main activity at IMEC is sub micron CMOS process development we try built for the work in MST as much as possible on the available infrastructure and know-how in that area. The CMOS know-how is complemented by expertise in other areas such as thin film multi-chip-module (MCM-D) technology, ferro-electric materials processing for non-volatile memory applica-

tions, III-V materials processing and the processing of organic materials for opto-electronic applications. As shown in figure 1 the MST activities are built upon broad and solid general thin film materials processing foundation. The work in the MST group focuses on the development of process flows avoiding as much as possible non-standard materials and equipment. Non-standard modules are developed taking into account the limitations imposed by the CMOS environment.

The advantages of such an approach are obvious: maximum usage of what has already been developed resulting in a reduction of the technological risk, development time and cost. From the start of the project the involvement of a commercial foundry is pursued, in order to facilitate the transfer of the process from IMEC to an industrial environment. Depending on the process flow part of the processing can be done in a standard CMOS foundry, part in a MST foundry environment. Industrial project partners usually provide the application know-how and device concepts. Typically this results in trilateral relationship with a user initiating the device concept, IMEC developing the process flow and specific non-standard process modules and a foundry for the later mass production.

This relationship is schematically represented in figure 2 indicating the information flow between the partners.

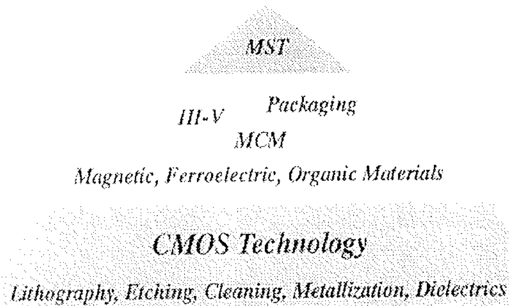

Fig. 1: IMEC MST process development approach

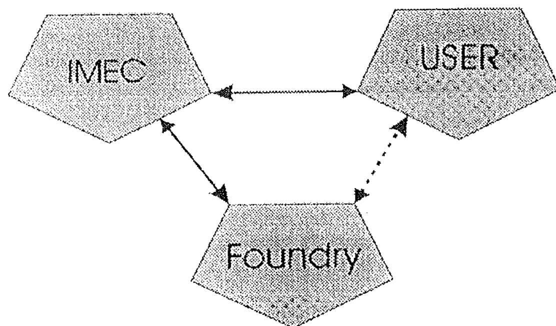

Fig. 2: MST process development partnership

2. Integrated processing

As shown in figure 3 adding transducer specific process steps and modules can be done in 3 different ways: as pre-processing, as a modified-back-end process or as post-metal processing. The first approach is not widespread because it requires that a foundry accepts pre-processed wafers, When the third route, post-metal processing, is followed, all transducer specific process modules are added after completion of the CMOS processing steps. The advantage of this route is that the CMOS part remains intact and therefore the influence of the added transducers on the behavior of the transistors is minimized.

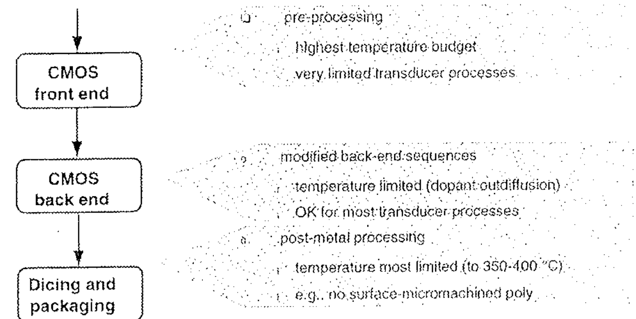

Fig. 3: addition of transducer-specific processes

The base wafers can be purchased from any standard CMOS fabrication facility, resulting in a large choice of available technologies. Also there is nearly no limitation on the kind of metal materials used to fabricate the transducers. However there is one main limitation on the kind of processing steps that can be added after full CMOS completion: the allowable thermal budget. Process temperatures above 400°C are not allowed, limiting e.g. depositions to mainly PECVD. This excludes e.g. poly-Si surface micromachining technology, LPCVD nitride as an ISFET-gate, wafer fusion bonding. In the second option, some or all of the transducer specific process modules are placed in between the CMOS process modules. When this route is followed, the possible impact of the added process steps on the CMOS behavior and on manufacturing issues has to be fully investigated. These main issues are related to additional thermal budget, additional layers which are deposited or grown, regions where additional etches are done and the addition of metal layers not commonly used in semiconductor fabrication which can cause contamination problems.

The impact of additional thermal steps depends on the position of the step in the process flow. Additional thermal budget will result in a change in the concentration profile under the transistor gate due to additional diffusion, especially for temperatures higher or equal to 900°C, leading to V_t-shifts. Having these temperature steps after junction implantation will also result in a further diffusion of the junction profiles, resulting in reduced channel lengths. If these effects occur, compensation is required by changing the implantation conditions, reduction of already existing temperature steps or additional mask biases.

The addition of layers above transistor areas also has its impacts. When a nitride layer is placed on top of a transistor, this layer will block hydrogen diffusion during

the final sintering step in the process. The effects of the added layers on hot carrier degradation can also be very important. In many applications, openings have to be made in the oxide layers on top of the silicon to clear the silicon or another layer (e.g. nitride). In the pre-metal and the intermetal dielectrics, different kinds of oxide layers have to be etched: undoped and doped LPCVD oxides, doped and undoped PECVD oxides, SOG layers, PECVD nitrides. This means that etching has to be controlled in these different layers in terms of profile, etch rate and selectivity. Combination of dry and wet etch is often the best solution because the dry etch gives the required profile control and the wet etch the required selectivity. To be able to control these etches higher densification temperatures of the oxides are required, especially in more advanced sub-micron technologies.

The monolithic integration of transducers further often requires the introduction of materials not standard used in semiconductor fabrication like Pt, Ag, PZT... Before these materials are introduced, careful contamination studies are required and additional working procedures need to be installed.

3. Examples

We can distinguish distinct application groups: those dealing with images, with physical signals, and with biochemical signals. Transducers dealing with images by nature, have to deal with 2-dimensional optical information which is captured, displayed, reproduced etc. This requires 1-dimensional or linear arrays (which are mechanically scanned in the second dimension) or 2-dimensional matrix arrays (which are static). The large majority of the 2D-arrays, and some of the 1D-arrays, are made monolithically to solve the interconnect problem. Physical sensors (primarily pressure sensors and accelerometers) for the automotive market, are produced in both monolithic /1/ and hybrid versions. Integrated biochemical sensor arrays are the most novel application group. Within the limited scope of this paper, we will not give an exhaustive review of all applications, but highlight selected work in the imaging and biochemical field.

3.1 Imaging transducer arrays

Recent improvements in CMOS imagers have allowed CMOS-based imagers to reach an image quality comparable to CCD´s /2/. CMOS imagers are made using fully standard process sequences. Additional process steps can enlarge their functionality. One example is full color imagers, on which a red-, blue- and green-died pattern is applied. The pattern formation can be done using commercially available died resists and standard i-line or g-line exposure systems. Another example is resist-based microlenses, which increase the fill-factor.

For infrared imagers, a recent innovation has been the introduction of Si-based uncooled infrared imagers. Infrared radiation can be captured by photon sensors (e.g. diodes with a small barrier height converting infrared photons to excited electrons) or by phonon sensors. Photon sensors can be made very sensitive but cryogenic operation is required in order to suppress the dark currents. Phonon sensors (converting infrared photons to phonons and thus heat) have demonstrated room temperature performance comparable to cooled detectors /3, 4/. A bolometer consists of a temperature dependent resistor and an IR absorber. The bolometer has a thermal capacity, and it is connected to an infinite heat sink at constant temperature through supports having a thermal conductance G. The absorbed IR radiation increases the temperature of the bolometer. In order to maximize the temperature increase, the bolometer must be thermally insulated (low G). The use of surface micromachining techniques allowed reducing the thermal conductance of the device to values close to the radiation limit. A SEM picture of an IR bolometer is displayed in figure 4. The structure is separated from the substrate by a vacuum gap, which is realized by surface micromachining using a sacrificial oxide. The only remaining thermal path to the substrate is through the supports.

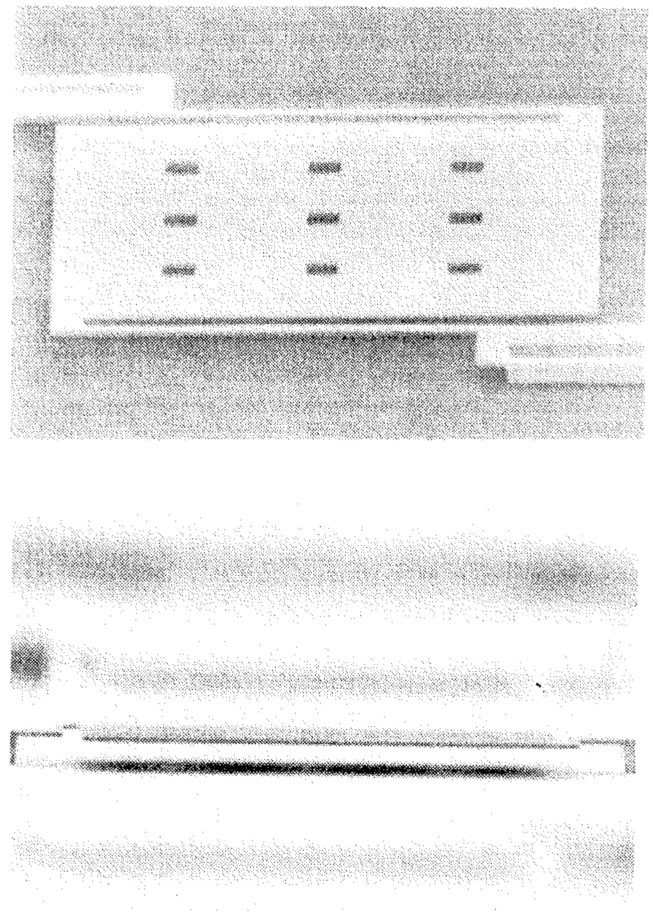

Fig. 4: SEM picture of 50μm x 50μm poly SiGe bolometer, supports are 400 nm thick and 1.5 μm wide.

The resistor element used is poly SiGe because of its advantageous properties as compared to poly-Si. Its stress can be tuned to the desired value at low temperature (figure. 5), which is not possible for poly-Si. It can be easily integrated with the driving electronics without running out of the thermal budget or damaging the existing electronics. Another attractive feature of using poly SiGe is its lower thermal conductivity, which en-

ables reducing the thermal conductance of the device to $7x10^{-8}$ W/K (which is only a factor of three higher than the radiation limit). Integrating poly SiGe bolometers into Focal Plane Arrays (FPA) yields an NETD of 65mK for an array of 320x240, comparable to the state of art /5/.In a thermopile, the increase in heat is detected by a Seebeck element. A poly-Si-to-Al Seebeck element can be made in a standard CMOS process flow, using the gate-poly and Al-metallisation. Also here, the use of poly-SiGe results in increased performance /6/. Bulk micromachined linear imagers with integrated signal processing capability have been demonstrated /7/. As compared to bolometers, the pixel size of thermopiles cannot be miniaturized to the same extent without sacrificing the NETD. For larger densities where small pixels are required, the bolometer principle is hence preferred.Si-based transducers are also used in image displaying. One approach is the Digital Micromirror Device (DMD), in which the change in tilt of tiny micromachined mirrors is used to modulate a light beam /8/. The other approach is using LCD´s as light modulators in transmissive or reflective displays.

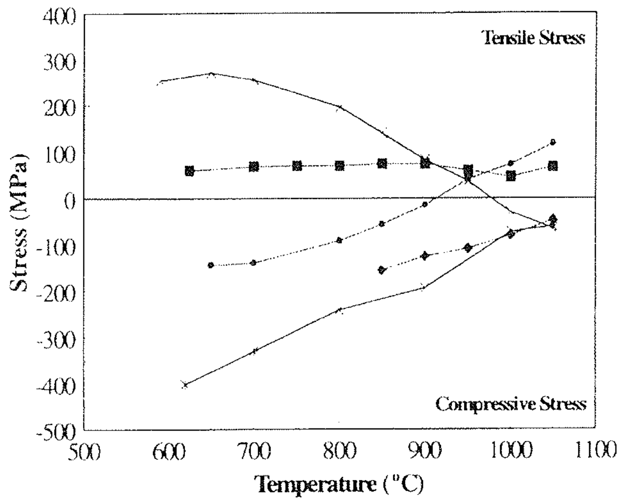

Fig. 5: Dependence of stress on annealing temperature (•APCVD poly SiGe grown at 650°C, ■RPCVD poly SiGe grown at 625°C, ◆APCVD poly Si grown at 850°C, ✳ LPCVD poly Si grown at 620°C and X LPCVD poly Si grown at 590°C).

Transmissive LCD displays are based on a-Si or poly-Si transistors, which are deposited on a quartz or glass substrate. Figure 6 shows a part of a transmissive display made in CMOS technology. Since the display need to be transparent, the only CMOS technology which could be used is a SOI technology from which the bulk of the silicon wafer is removed, using the buried oxide as an etch stop layer. A 1μm SOI technology was used. The active CMOS layer, less than 1μm thick was transferred to a transparent (glass) substrate. A parasitic effect of the display being transparent and illuminated by a light source, is the generation of photocurrents in every p-n junction. Using the SOI technology p-n junctions from source/drain to substrate are not present, but junctions from source/drain to channel are available. These photocurrents are parasitic currents compromising the operation of the logic. To suppress these currents a light shield over the CMOS areas is necessary.

In order to circumvent the transfer of technology and hence make use of an almost standard process, a CMOS-based reflective display is a very attractive approach /9/.

CMOS-based transducers are further encountered in image reproduction technology. Well-know developments are in inkjet technology. Micromachining is used in this case in order to create the miniature ink nozzles and containers /10/.

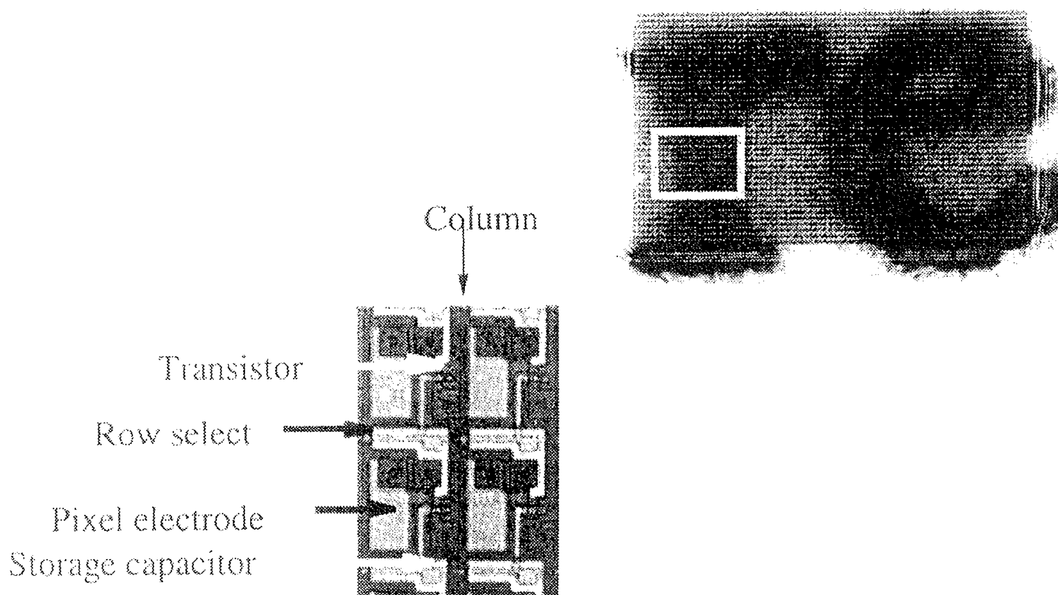

Fig. 6: Top left is shown a test array of the active plate for a LCD transmissive array. The inset right bottom shows a magnified view of 4 pixels.

3.2 Biochemical sensor arrays

The most recent area where integrated sensors are emerging, is biochemical sensor arrays. The characteristics of these devices are in several respects distinct. The sensor dimension is usually quite large (0.01 - 1 mm^2) due to the practical difficulties in handling sub-μL quantities of liquids. Also, the number of sensor sites is rarely higher than a few hundred. Lastly, the preference to use disposable devices makes the use of Si a possible but not exclusive choice. CMOS integration is hence not a mainstream for biochemical sensors, but nevertheless used in several devices.

An example is the Ion-Sensitive Field Effect Transistor (ISFET), which can be used as an ion sensor. The structure of an ISFET is similar to a MOSFET, the poly silicon gate is absent and the gate insulator is in contact with a sample liquid. Unlike the working principle of a MOSFET, the flatband voltage of an ISFET depends on the surface potential at the insulator-liquid interface. The surface of the gate insulator contains hydroxyl groups that can be protonated and deprotonated and thus an electrochemical relation between the electric field and the pH of the sample liquid exists. ISFETs can directly be integrated with MOSFETs in an opamp configuration /11/. Arrays of ISFETs were integrated with operational amplifiers in a standard 1.25μm CMOS technology (figure 7).

A sacrificial layer was used to protect the ISFET-gates during aggressive post-processing. Thin film Ag was deposited and patterned by a lift-off technique or by electroplating. Electrochemical Ag/AgCl reference electrodes are formed from it by electrochemical chloridation. The voltage of the sample liquid is kept constant by means of an immersed Ag/AgCl reference electrode. Pt electrodes were incorporated in the process flow to allow making also amperometric sensors. Thin and thick polymer micropools are structured by photo patterning and are used for electrolyte and membrane dispensing. Other ions (e.g. K^+, Ca^{2+}, and Na^+) can be measured by covering the device with an appropriate electrolyte layer and gas-permeable membrane.

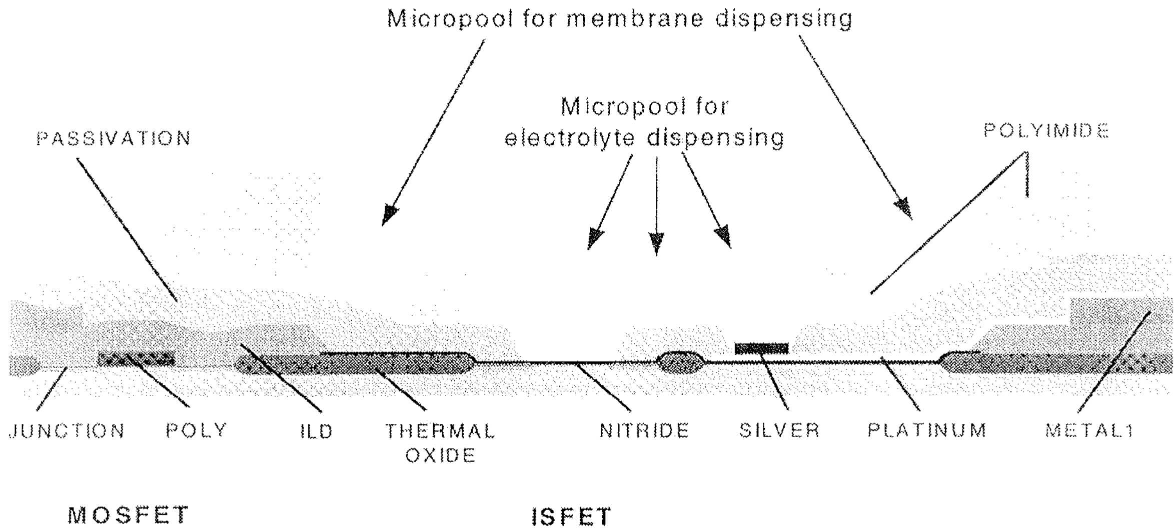

Fig. 7: Cross-section of an Ion-Sensitive Field Effect Transistor integrated in a 1.25μm CMOS technology

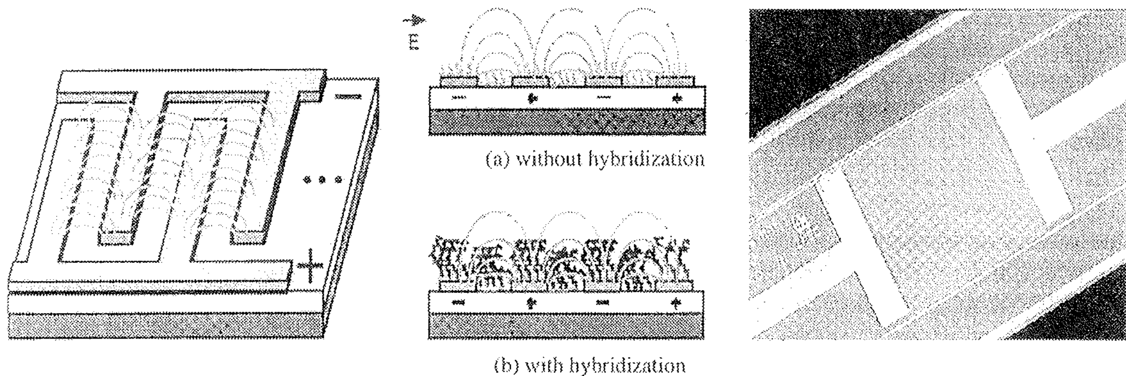

Fig. 8: Plan view (left) and cross-section (middle) of IDE sensor. The field lines are disturbed by hybridization at the surface. Photograph of IDE sensor (right)

All values for the nMOS parameters after the completion of the transducer specific processing are within the specifications and do not induce considerable shifts in the nMOS parameters. Using phosphate buffers between pH 6.0 and pH 8.0, the pH-sensitivity of a CMOS-processed ISFET-opamp module has been measured. The pH-sensitivity of the ISFET had a value of 53mV/pH.

Impedimetric sensors can also easily be integrated in CMOS. The basic structure is that of a planar interdigitated capacitor (figure 8). Nanoscaled interdigitated electrode arrays (IDEs) were made with Deep UV lithography. Electrode width and spacing from 500 nm down to 300 nm were achieved on large active areas (0.5mm x 1mm). 50 nm thick palladium electrodes or 40 nm thick gold electrodes were evaporated on 1.2 μm thermal SiO_2 and structured by lift-off. The interdigitated electrodes were between 300 nm and 500 nm wide, with spacings in the same order of magnitude. The response of the impedimetric sensors can be modeled electronically by an equivalent circuit consisting of an interface impedance, represented as a constant phase element, a solution resistance and a dielectric capacitance between the electrodes. Due to the distribution of the field-lines, information is detained about interface phenomena as well as about properties of the bulk in the vicinity of the electrodes. Genetic diseases and infectious agents can be traced by looking for specific DNA-sequences. The presence of these DNA-sequences or antigens/antibodies can be detected by looking for the binding of these molecules to selective probes. When target nucleic acid hybridizes to oligonucleotide probes or when antibodies bind to antigens, the change in electric properties, in the vicinity of an electrode, results in a change of impedance, enabling the measurement of a direct electrical signal.

In a series of experiments, the possibilities of impedimetric sensing of DNA hybridization with nanoscaled IDEs were explored. Thiol-linked oligo´s were coupled to gold IDEs by chemisorption. After coupling of the probes to the structures non-specific binding was avoided by blocking with cysteine. The solution resistance lowered by a relative decrease of approximately 38% and 18% respectively. After hybridization with PCR product the solution resistance lowers significantly by a relative decrease of approximately 50%. These results clearly demonstrate that the nanoscaled impedimetric sensors are capable of detecting DNA fragments. A similar technology can also be used for a different purpose in DNA sensing, e.g. when the electrodes are used not for sensing, but for controlling the hybridization /12/.

4. Conclusions

CMOS based sensors and actuators have found applications in a wide range of products. Well-developed markets are e.g. in automotive sensors; novel developments are in the area of uncooled IR imaging, reflective displays and recently biochemical sensor arrays. Most transducer-specific process steps such as micro machining can be incorporated in a CMOS flow. The post-metal processing approach is the most attractive, but will only reach its full potential if we can achieve lower temperature process for e.g. surface micro-machining, ISFET dielectrics, wafer fusion bonding. The research and development activities in the field of CMOS process development puts IMEC in an excellent position to contribute to the development of novel MST fabrication processes.

5. Acknowledgement

The authors acknowledge Siemens Co. and IMT for the characterization of the ISFET sensitivity. Part of this work was performed in the Brite/EuRam project (BE 95-1334).

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Prispelo (Arrived): 15.10.99 *Sprejeto (Accepted): 25.11.99*

UDK621.3:(53+54+621+66), ISSN0352-9045

INTEGRATED MAGNETIC SENSORS DESIGN EXAMPLES

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TUTORIAL INVITED PAPER
MIDEM´99 CONFERENCE - Workshop on MICROSYSTEMS
13.10.99 - 15.10.99, Ljubljana, Slovenia

Keywords: integrated magnetic sensors, intelligent magnetic sensors, MFS, Magnetic Field Sensors, design examples, ASIC, Application Specific Integrated Circuits, electric current measurements, electrical energy measurement, proximity sensors, proximity switches, position measurements, two-dimensional magnetic fields

Abstract: Various design examples for integrated magnetic sensor ASICs are presented. They include current and energy metering, proximity switches position and angle measurements and complex two-dimensional magnetic field measurements. Design approach based on Hall element array is iintroduced. Sensor properties optimization by design approach is analyzed. Potentials of micromachining sensor element are discussed.

Primeri načrtovanja integriranih magnetnih senzorjev

Ključne besede: senzorji magnetni integrirani, senzorji magnetni inteligentni, MFS senzorji polja magnetnega, primeri snovanja, ASIC vezja integrirana za aplikacije specifične, meritve toka električnega, merjenje energije električne, senzorji bližinski, stikala bližinska, meritve položaja, polja magnetna dvodimenzionalna

Povzetek: Prikazani so razni primeri načrtovanja vezij ASIC z integriranimi magnetnimi senzorji. Med njimi so primeri vezij za merjenje toka in energije, magnetna stikala, vezja za merjenje pozicije in kota ter za merjenje kompleksnih dvodimenzionalnih magnetnih polj. Uvedena je načrtovalska metoda s poljem Hallovih elementov. Predlagana je optimizacija lastnosti senzorjev s pomočjo načrtovalske metode. Prikazane so možnosti za mikroobdelavo senzorskega elementa.

1. Introduction

Integrated magnetic sensors can be used in a variety of applications. Classification of the ASIC with integrated magnetic circuit could be either by its application or it could rather be based on the design approach. By design approach one can distinguish between two classes. In the first class there are the ASICs with open loop approach. This means that such circuit relies on the actual sensitivity of the integrated sensor, so sensor sensitivity should be very well calibrated during ASIC testing and the ASIC should provide good compensation of the temperature coefficient of the sensor and of sensitivity changes due to other internal or external conditions.

The other alternative is a closed loop approach. In this case a magnetic signal is feed-back to the sensor which is used only as a signal source for the error amplifier. The accuracy of such ASICs is therefore dependent only on the feed-back elements of the magnetic circuit.

The magnetic circuit providing the feed back can be either external or it could be integrated. In the second case the field strength is limited by the capability of the integrated coils. If this is not enough it is necessary to use a combination of open loop and closed loop approach.

In the paper various design examples of these design approaches are presented.

2. Design Approaches for ASICs with Integrated Magnetic Sensors

Table 1 shows different design approaches for various applications. The simplest application is a proximity switch. Typical specification for such ASIC is the magnetic field, usually of both polarities and its current consumption. To achieve the lowest current consumption the reaction time of the ASIC is relatively slow. Figure 1 shows the block diagram of such ASIC. Some of the design approaches for such ASIC were already described /1/.

Table 1

OPEN LOOP	CLOSED LOOP	COMBINED
Absolute magnetic field measurement: 1. Proximity switches 2. Relative/absolute position/angle measurement 3. Current/energy measurement	Current measurement Energy measurement	Accurate field measurement for position, current or energy measurement

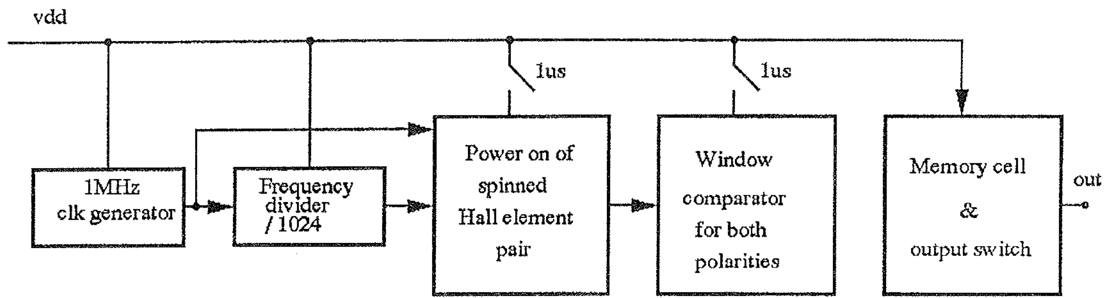

Fig.1: Block diagram of battery operated magnetic switch

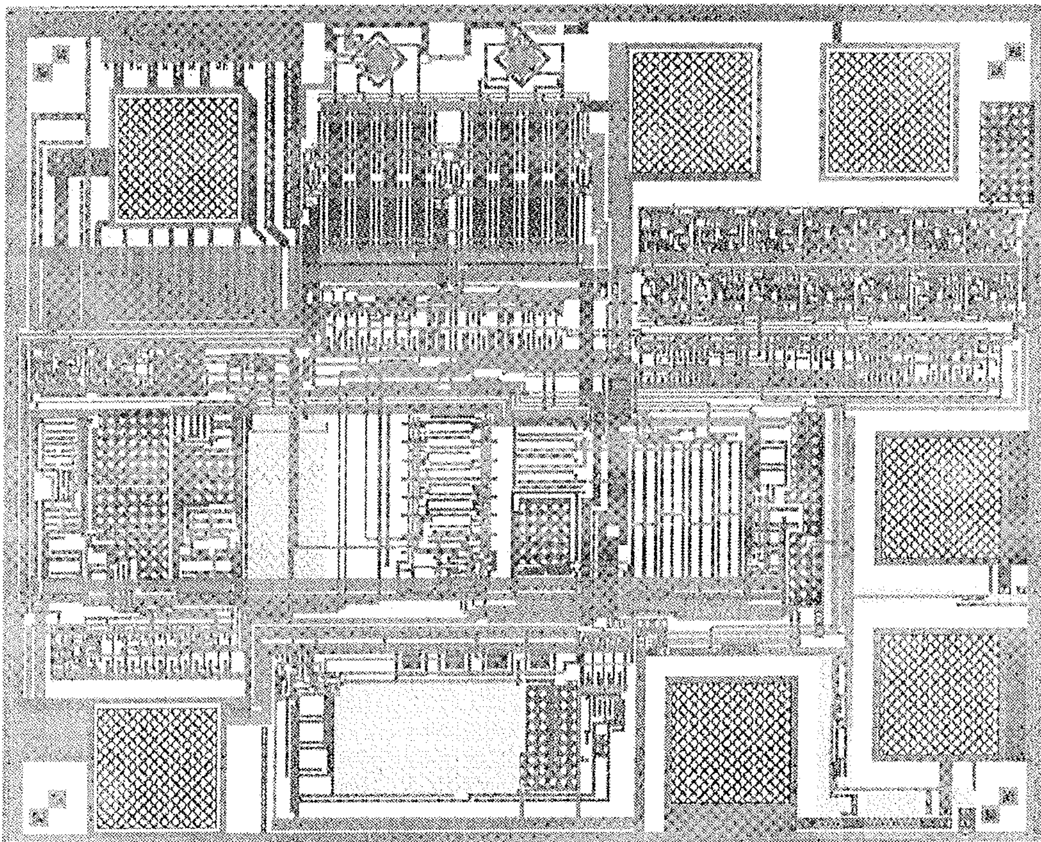

Fig. 2: Realization of magnetic switch

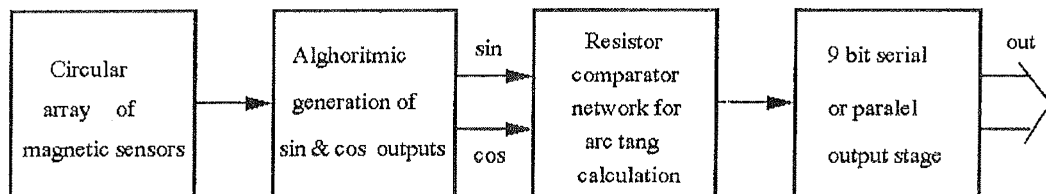

Fig. 3: Block diagram of absolute angular encoder ASIC

The critical specifications for such magnetic switch are continuous current consumption, the response time, accuracy and chip size.

Figure 2 shows the realization of such magnetic switch, while Table 2 summarizes some of the most important parameters.

Table 2

Operating voltage	2V - 3V
Current consumption	< 15 μA
Response time	< 1 msec
"ON" magnetic field	± 2 mT_{min}, ± 3 mT_{max}
"OFF" magnetic field	± 1 mT_{min}, ± 2 mT_{max}
chip size	<0.5mm^2

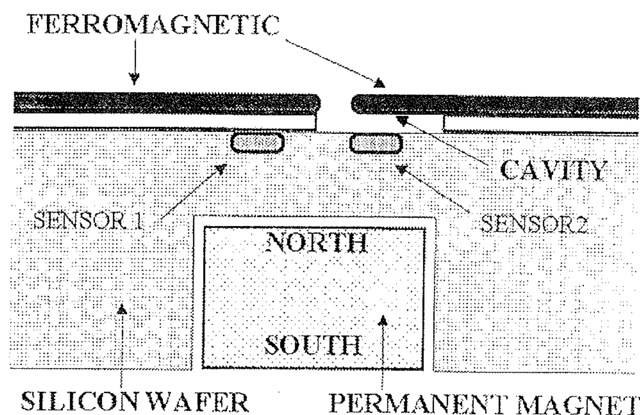

Fig. 6: Proposal for micromachined accelerometer based on integrated magnetic sensor

Another example for open loop approach is absolute angular encoder ASIC. Block diagram of such ASIC is shown in figure 3.

In this ASIC a patented algorithm was used to generate an accurate absolute angle position of North-South polarized permanent magnet to the ASIC.

Since only a ratio of sin/cos signals determine the angle neither accurate magnetic field strengths nor accurate absolute sensitivity of sensors is required to obtain 9-bit absolute accuracy with less than 0.2LSB relative accuracy, the result which will allow this type of ASICs to take over a big part of the opto-encoders market due to lower price and high robustness of the design. Figure 4 shows the realization of this circuit. Energy metering using Hall element approach has been a design goal of many electricity meters producers, but only few succeeded. The design approach for such high performance ASIC was described in /2/.

A design example of such meter ASIC is shown in figure 5. It was designed in 1.2 μm CMOS process. The die size of less than 10mm^2 offers a price advantage compared to other types of electronic meters specially the ones using digital signal processing of the current transformers or shunts for current sensing.

3. Micromachining of Magnetic Sensors

Micromachining offers a possibility to make Hall element perpendiculars to the ASIC plane. Such vertical Hall element allows various possibilities to measure a complete vector of the magnetic field strength, not only the vector component which perpendiculars to the ASIC plane.

Typical volume application for such devices are electronic compass and personal dosimeter of exposure to various magnetic fields.

Table 3

	Achieved	**New designs**
Sensitivity	10 mV/G; 100 V/T	not limited
Linearity	> 0.1%	limited by test equipment
TC	100 ppm	50 ppm
Offset voltage -40 °C 150 °C	1.5 G; 150 μT ± 8 G; 800 μT	0.5 G; 50 μT 2 G; 200 μT (10 mG; 1 μT) special cases
Noise	2 mG/√Hz; 200nT/√Hz	1mG/√Hz; 100 nT/√Hz (0.1 mG/√Hz; 10 nT/√Hz) for B > 100 kHz
Frequency response	10 MHz	application dependent
Current consumption	10 μA	application dependent
Resolution	10 μm; 40′	2.5 μm, 20′
Accuracy	20 μm/m; 40′	10 μm/m; 20′

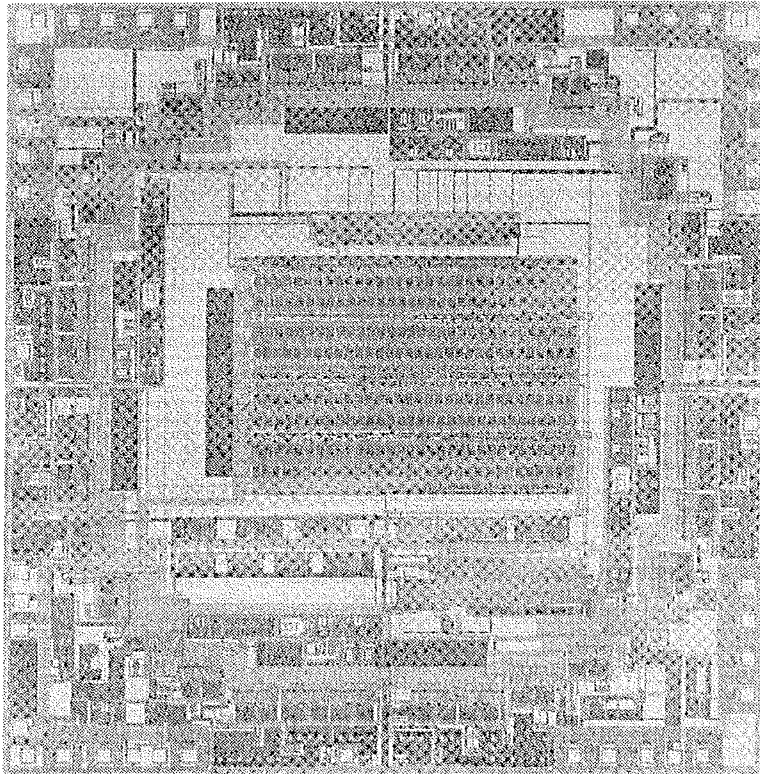

Fig.4: 9-bit absolute angular encoder, die size 5mm x 5mm

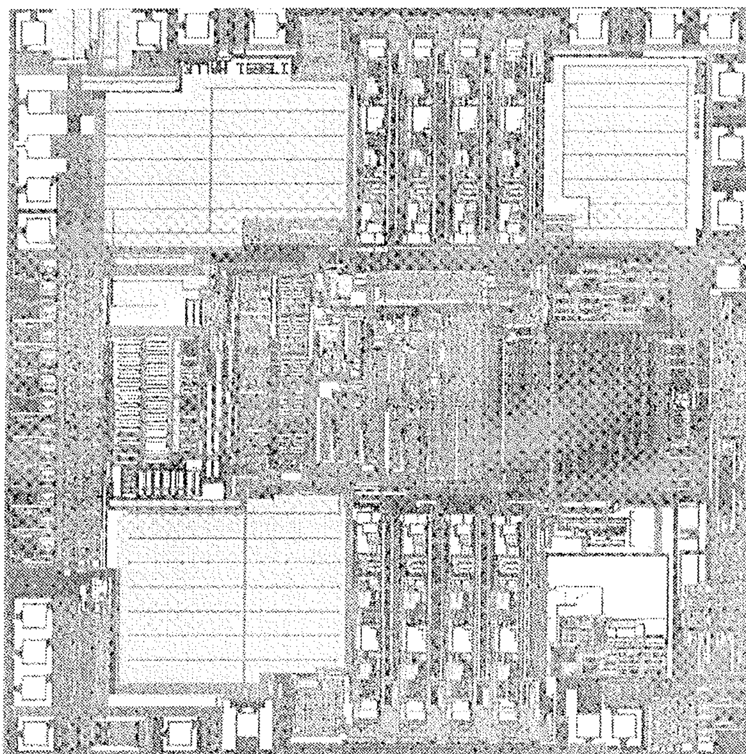

Fig.5: Realization of electrical energy meter ASIC

An interesting application of micromachined magnetic systems is accelerometer. Cross-section of such accelerometer is shown in figure 6.

The system consists of classical ASIC with micromachined cavity to insert a permanent magnet. On the top of the sensor 2 there is a micromachined movable membrane made of ferromagnetic material. The same material is above the sensor 1 but fixed. By this arrangement a differential measurement of the field modulation due to membrane movements is possible.

A closed loop approach with integrated coils /2/ to measure field strengths difference is appropriate since the differential field strengths quite small.

The described approach has also the advantage over other solution due to the possibility to calibrate the sensor using external magnetic field to move the ferromagnetic membrane instead of a real accelerometric force.

4. Conclusion

Several designs using integrated magnetic sensors were realized in Laboratory for microelectronics on Faculty of Electrical Engineering. Some of the achievements are summarized in Table 3.

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CHANCES OF MICROSYSTEMS

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TUTORIAL INVITED PAPER
MIDEM´99 CONFERENCE - Workshop on MICROSYSTEMS
13.10.99 - 15.10.99, Ljubljana, Slovenia

Keywords: microsystems, MST technology, MicroSystem Technologies, increased functionality, cost efficiency, mass production, technology overview, industrial process control, automobiles, medicine, consumer articles, miniaturization, microelectronics

Abstract: Microsystem technologies offer new possibilities to increase functionality, utilize cost efficient mass production technology and thus explore new applications. These technologies combine electronic, mechanical, optical and chemical elements and use several physical effects. Applications can be found in industrial process control, automobiles, medicine, and consumer articles. The multidisciplinary requirements offer chances especially for innovative companies and networks. This presentation gives an overview of technologies and applications with emphasis on some outstanding examples.

Mikrosistemi in njihova priložnost

Ključne besede: mikrosistemi, MST tehnologije mikrosistemske, funkcionalnost povečana, uspešnost cenovna, proizvodnja množična, pregled tehnologij, vodenje procesov industrijskih, avtomobili, medicina, predmeti potrošniški, miniaturizacija, mikroelektronika

Izvleček: Tehnologije mikrosistemov ponujajo nove možnosti za povečanje funkcionalnosti, izrabljajo že obstoječo cenovno in stroškovno učinkovito masovno proizvodno tehnologijo in tako ponujajo možnosti novim aplikacijam. Te tehnologije kombinirajo elektronske, mehanske, optične in kemične elemente in izrabljajo nekatere fizikalne efekte. Uporabo mikrosistemov lahko najdemo na področju industrijske procesne kontrole, avtoelektronike, medicine in široke potrošnje. Zahteva po multidisciplinarnosti ponuja nove možnosti predvsem inovativnim firmam. V prispevku podajam pregled tehnologij in aplikacij mikrosistemov s poudarkom na nekaterih izjemno uspešnih primerih.

1. Introduction

Microelectronics, in the past two decades, has developed into one of the biggest industries of the world. Almost all goods of normal life could be penetrated by semiconductors with new functionality, better performance, higher userfriendlyness and other benefits at low cost levels. This has been made possible, as we know, by submicron CMOS and related IC technologies, mass production of 8 inch silicon wafers and a globalized, highly competitive semiconductor industry.

Today integrated circuits (IC´s) perform computational and signal processing tasks, run telecommunication networks, store large amounts of digital information. Analog signals can be processed by audio-, ZF- and RF-circuits, A/D- and D/A-converters, while dedicated Smart Power ASIC´s and Power Components like IGBT´s open the door to new power supply concepts and advanced drive systems for actuators.

The tremendous price/performance development has been made possible by four main factors:

- Continuous advances in lithography down to 0,25 μm and below.
- Wafer batch processing with growing wafer diameters.
- Silicon CMOS as nearly optimal „flagship" technology
- Standardizations in process technology, equipment, CAD engineering.

Microelectronics, however, is confined to the world of electrical units and electronic signals. Interfacing to the environment requires sensors and actuators in order to obtain a complete system. As a consequence sensors and actuators very often turned out to be the most costly and less reliable part of the system. Microsystems is the way to integrate also non-electronic components and functions into microelectronic systems while maintaining their benefits. Several efforts in partly overlapping directions have been made in the past years leading to names like MST (Microsystem technologies), MEMS (Micro-Electro-Mechanical Systems) or MOEMS (Micro-Opto-Electro-Mechanical Systems).

Mechanical systems play an important role in most microsystems. A new dimension of MST thus can be created by combining the requirements of precision engineering with microtechniques, as shown in fig.1. Microsystem technologies are therefore characterized by the combination of mechanical, optical and electrical functions in which the functional elements have microdimension and are suited for batch production. Additional applications may include chemical and biological microsystems.

MST makes it possible to realize complete miniaturized systems with new functionality, either on a silicon chip or in a hybrid combination. For that reason it is regarded as a breakthrough or „disruptive" technology, allowing unparalleled synergism between hitherto unrelated fields of endeavor such as biology and microelectronics. Many new MST applications will emerge, expanding beyond what is currently identified or well-known.

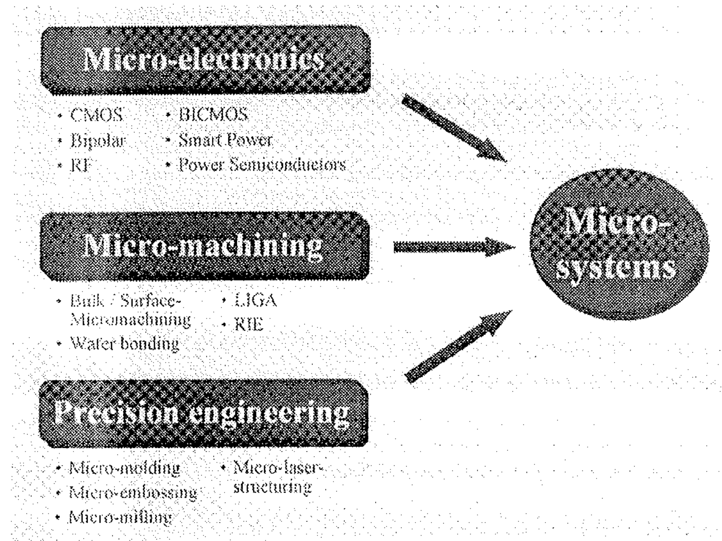

Fig. 1: Microsystems by combining technologies

2. MST – a „disruptive" technology

Basic research in microsystem technologies started in the 1970s, mainly in the research labs of huge companies like IBM or Bell Labs and at some universities. In the 1980s, in Germany the LIGA technology, originally intended for separation nozzles for the nuclear industry, was developed. In addition first microelectronic companies like Analog Devices became aware of the chances of fully integrated micromaching technologies e.g. for accelerometers. In the 1990s first attempts to commercialize MST products as well as coordinating efforts in the US and in Europe like NEXUS or the IVAM Microstructure Initiative NRW were made. These coordinating initiatives proved to be most useful in building up networks of SME´s, R&D institutes and universities. First market studies and summary data have been collected, standardization and roadmap activities have been started. Also application-oriented r&d institutes like the IMS of the Fraunhofer society concentrated on the realization of microsystems.

In 1996 the worldwide industrial activity in microsystems was evaluated at 12 bio US$ (7"2 in US, 3"2 in JP and 1"5 in EU), based on the employment of 60.000 people in this field (40.000 in US, 15.000 in Asia and 5000 in EU) /1/. A high number of international conferences dedicated to MST takes place around world, as can be seen from the short collection of the current half year, shown in table 1.

The commercialization of microstructures today is already supported by:

- Networks of companies and research institutes offering design and manufacturing service taylored to specific MST-based product needs.
- First dedicated MST production equipment: Some semiconductor equipment manufacturers already

Table 1: International events for MEMS and microsystems

07.07.-10.07.99	Dortmund	Commercialization of Microsystems
30.08.-01.09.99	Mainz	3rd Conference on Micro Opto Electro Mechanical Systems
20.09.-22.09.99	Santa Clara	SPIE´s 1999, Micromachining and Microfabrication
29.09.-01.10.99	Stuttgart	MicroEngineering´99, Fair and Congress for Microsystems and Precision Engineering
27.09.-02.09.99	Gif-sur-Yvette	MME´99 – Micromechanics Europe
27.10.-29.10.99	Tokyo	MICROMACHINE´99
27.10.-29.10.99	Queensland (AUS)	International Symposium on Microelectronics and Micro Electro Mechanical Systems
01.11.-04.11.99	Boston	MEMS Technology Workshop
11.11.-19.11.99	Nashville	MEMS Symposia
23.01.-27.01.00	Miyazaki (JP)	MEMS´2000 Conference

offer machines specialized on MEMS-specific processes like wafer bonding, double-sided alignment of wafers or RIE for structures with high aspect ratios. New concepts like „scalable" equipment, where the same process and basic tools can be applied for prototype manufacturing up to fully automated volume production, help to overcome investment barriers.

- First CAD systems oriented on MEMS design requirements: These systems mainly integrate 3D-modelling into IC design tools.
- MEMS foundry services.

4. Applications and markets for microsystems

Microsystems very often are embedded in products or bigger systems, the applications are highly diversified due to the versatile structure of MST. This makes it very hard to

1. define, what a „microsystem" is
2. determine and predict application areas, markets and volumes

The first comprehensive market study for MST based products has been published by the NEXUS consortium this year. Fig. 2 shows the projected market development for MST products with an 18% average growth rate. The contribution coming from new or unknown products (in 1996), which is relatively small for a new technology, reflects the situation, that big steps still have to be overcome regarding production and reliability related issues in commercialization. Fig. 3 shows the main applications for MST products. It can be seen, that the mass storage and inkjet printer market today and also in the next years will dominate significantly the MST arena, applications in the medical and biomedical field are the most promising candidates for the future of MST.

It can also be seen that MST products will penetrate applications in nearly all fields like IT-peripherals, medical / biomedical, telecommunication, industry and process control, automotive, environmental monitoring and facility control.

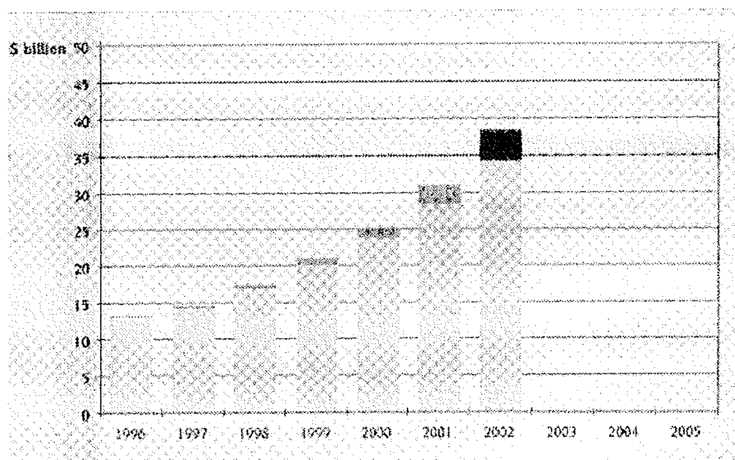

Fig. 2: MST market (source: NEXUS)

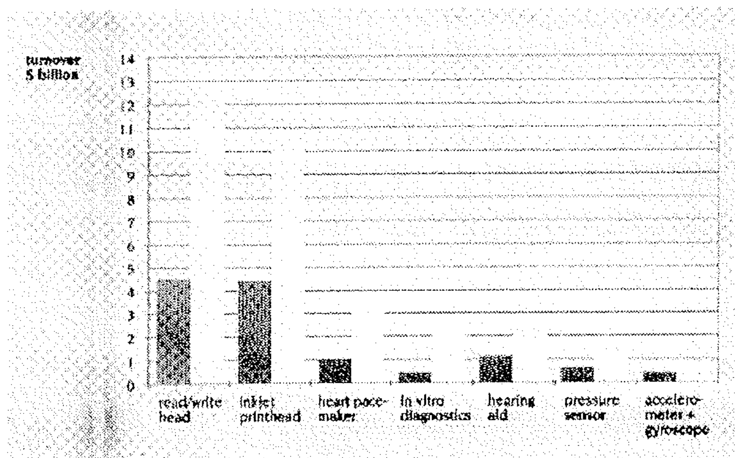

Fig.3: MST applications (source: NEXUS)

5. The complexity pitfall

As shown before, microsystems, as a breakthrough technology for system miniaturization for a broad range of applications, open up several new dimensions. Additional materials (e.g. PMMA, Ni,...) are involved, new processes required, specialized packages become necessary. Testing concepts and reliability issues have to be worked out and solved. Also the design process, especially in integrated solutions, becomes more complex. On the one hand all these factors create chances for exceptional new solutions, on the other hand they contribute to complexity. Standardization is far behind the level achieved in microelectronics and will never reach it. Therefore predictions on the progress of MST and commercializations are much more difficult than for microelectronics, where progress has been following „Moore´s law" for 20 years.

These situations require new and more flexible structures, that can provide and combine the required capabilities. Networks and clusters like IVAM or EMSIC /2/ have proved to be able to handle this complexity in an efficient way. While multinational companies deal with applications based on high volume and high potential like read-write heads for HDD or the „finger print sensor", the high diversity of microsystems opens chances not only for SME´s that concentrate on specific technologies, but also for r&d-organizations that act in an integrative way working on system design and system integration aspects as well as on standardization.

This situation will not change in the near future: the diversity will remain dominant, only a few applications will reach production volumes known in the IC world and will become interesting for large companies.

6. Promising application areas

Applications of microsystems can be divided into the following areas:

- Read-/write heads for hard-disk drives and printheads for inkjet printers. These, as they are driven by highly-dynamic EDP markets, are the dominating MST-applications today.

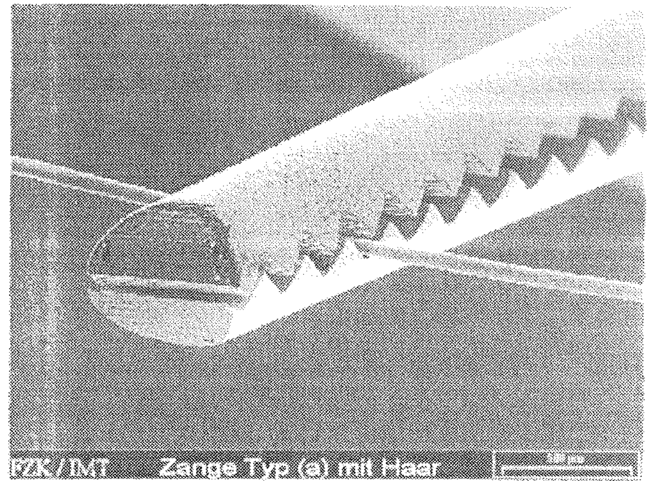

Fig. 4: Microsurgery: forceps with hair (source: Forschungszentrum Karlsruhe)

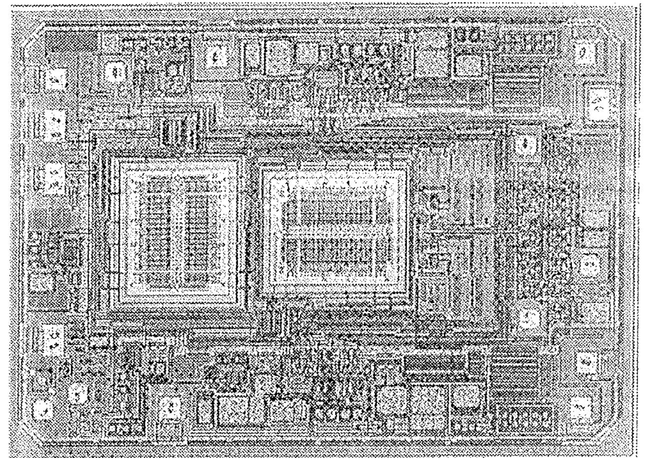

Fig.5: Monolithic accelerometer (source: Analog Devices)

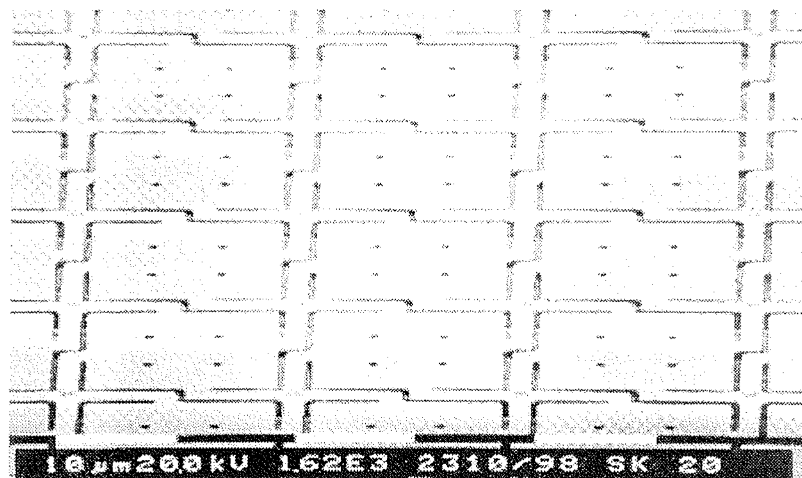

Fig. 6: Micromirror display (source: Fraunhofer Gesellschaft/ IMS)

- Interfaces for microelectronic systems. Microsensors and microactuators contribute the main part to these applications /3/.
- Micro resonators and filters. These devices may replace quartz oscillators or LC filters.
- High-precision or highly-miniaturized mechanical systems, based on MST technologies. Most promising examples can be found in medical areas, i.e. for micro-surgery (see fig. 4).
- Completely new application fields like MST for chemical analysis, providing complete micro-labs for complex analysis tasks, or bio-MEM´s, capable of identification and handling DNA structures. Both applications are in the field of medical and biotechnology.

Resonating devices, realized by surface-micromachining, offer an excellent opportunity to combine sophisticated mechanical structures with CMOS or BICMOS technologies monolithically. Accelerometers, gyroscopes, but also micro-resonators and filters can be built in this way (see fig. 5).

Very promising MST-devices can be found in applications that require large array configurations, e.g. for:

- identification („fingerprint")-sensors
- micromirror displays (see fig. 6).

Both applications can be realized by CMOS technology, combined with a MST surface structure containing the microsensor/microactuator function. Micromirror arrays seem very promising for large-scale projection displays, maskfree lithography or laser-printing.

7. Conclusion

Microsystems technologies offer new chances for further miniaturization and for the implementation of completely new systems in a broad variety of application fields. The technologies are just starting to emerge from experimental and research state into industrial commercialization. The large diversity of technologies prohibits or, at least, slows down standardization processes known from the microelectronics industry. This situation gives special chances to specialized organizations operating in well-organized networks.

The criteria for the success of microstructures lie in the ability of creative engineers to apply the well-known benefits of microelectronics batch production techniques to applications representing high production volumes.

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Prispelo (Arrived): 15.10.99 *Sprejeto (Accepted): 25.11.99*

SILICON BULK MICROMACHINING FOR SENSOR TECHNOLOGIES

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TUTORIAL INVITED PAPER
MIDEM´99 CONFERENCE - Workshop on MICROSYSTEMS
13.10.99 - 15.10.99, Ljubljana, Slovenia

Keywords: sensors, sensor technology, MM, MicroMachining, Si technologies, silicon technologies, bulk machining, pressure sensors, flow sensors, microsensors, flow microsensors, gas sensors, hybrid technologies, microsystems

Abstract: Micromachining and related technologies are needed to develop a large variety of sensors and actuators, i.e. the basic components of Microsystems or MEMS (MicroElectroMechanical Systems) as they are also commonly called. Microsystems are designed and fabricated by integrating different microcomponents into one functional unit comprising of sensors, actuators, I.C.s for data processing etc. In this development a variety of micromachining technologies, ranging from the conventional silicon bulk and surface micromachining to LIGA and LASER techniques are employed, each one having specific merits for specific products /1/. This review focus on silicon bulk micromachining applied to the fabrication of sensors suitable for being integrated into Microsystems, which are under development at IRST Microsystem Division.

Mikroobdelava silicija v senzorskih tehnologijah

Ključne besede: senzorji, tehnologija senzorjev, MM obdelava najfinejša, Si tehnologije silicijeve, obdelava globinska, senzorji tlaka, senzorji pretoka, mikrosenzorji, mikrosenzorji pretoka, senzorji plina, tehnologije hibridne, mikrosistemi

Izvleček: Mikroobdelavo in podobne tehnologije potrebujemo za razvoj in izdelavo različnih senzorjev in aktuatorjev, ki tvorijo osnovne elemente tki. mikrosistemov, oz. kot jih pogosto kličemo MEMS (MicroElectroMechanicalSystems). Mikrosisteme načrtujemo in izdelujemo z integracijo različnih komponent v eni funkcijski enoti, ki se sestoji iz senzorjev, aktuatorjev, elektronike za obdelavo podatkov itn. Za izvedbo tega cilja uporabljamo različne tehnologije mikroobdelave silicija od konvencionalne površinske, oz. globinske do LIGA in laserskih tehnik, ki pa vsaka ima svoje prednosti za realizacijo določenih izdelkov. V tem pregledu predstavimo tehniko mikroobdelave silicija, ki jo uporabljamo za izdelavo senzorjev, primernih za integracijo v mikrosisteme, ki jih trenutno razvijamo na inštitutu IRST na oddelku za mikrosisteme.

1. Introduction

Micromachining and related technologies are needed to develop a large variety of sensors and actuators, i.e. the basic components of Microsystems or MEMS (MicroElectroMechanical Systems) as they are also commonly called. Microsystems are designed and fabricated by integrating different microcomponents into one functional unit comprising of sensors, actuators, I.C.s for data processing etc. In this development a variety of micromachining technologies, ranging from the conventional silicon bulk and surface micromachining to LIGA and LASER techniques are employed, each one having specific merits for specific products /1/. This review focus on silicon bulk micromachining applied to the fabrication of sensors suitable for being integrated into Microsystems, which are under development at IRST Microsystem Division.

2. Microsystem technologies for medium-small volume applications

Market studies (forecast) indicate that the world-wide Microsystem market is slated to reach about 3 billion Euros at the beginning of year 2000, while simultaneously enabling applications reaching a market value 5 to 10 times bigger. Undoubtedly these numbers are staggering and should make many companies eager to participate. But the large variance in market estimates is a warning that the market is still in its development phase, and that these forecast are based on assumptions that remain largely to be verified. The examples of the inkjet print head, of the manifold absolute pressure sensors and of the airbag crash accelerometers are routinely invoked to illustrate the market opportunities that Microsystem devices can enable. But the majority of these large volume applications are dominated by large Corporations. In this type of developments and large volume production the preferred technology is CMOS with a few post-processing steps to add the sensor layers. The monolithic approach represents the preferred solution especially when large matrix of sensors made of identical pixels, where massively parallel interconnections are needed, are to be fabricated in large volumes.

Small and Medium size Enterprises (SMEs) are also interested in microsystems and can survive by carving themselves small niche markets based on innovative products and technologies. In this case highly dedicated microsystems have to be produced in small-medium quantities. Due to cost and risk SMEs are forced to cooperate with Research Centres to reduce prototyping development cost and time to market. This creates

a unique opportunities to link Research Centers and SMEs to join efforts in feasibility studies and prototypes design and development.

Dedicated microsystems aimed at niche markets represent a difficult task to be solved, both in terms of design, development technologies, market penetration and the ensuing financial profit. For this type of developments related to small volume production the hybrid approach is more suitable. Hybrid integration allows an independent optimisation of the different technologies required for the fabrication of the different types of sensors and actuators to be coupled with the IC driving electronics to form the microsystem. Furthermore, it takes advantage of an increasing number of basic components and subsystems made available on the market by specialised manufacturers. The idea is then that different suppliers will offer a catalogue of standardised micromodules, such as power supplies, sensors and sensors arrays, actuators, fluidic modules etc., and that the system producer concentrate in the development of only a few specific modules, if not available, and especially on the connecting of all these micromodules and related electronics, usually CMOS ASICs, to form the microsystem. In this strategy an increasingly important role is played by the optimum microsystem partitioning and by the packaging and interconnection(not only electrical!) technologies.

The microelectronics analogy of this foreseen approach is the gate array, which can be tailored to the desired performance by acting only on the metal interconnection level.

The hybrid solution based on standardised micromodules offers to SMEs the following main advantages:

- small investment to start a microsystem oriented activity;
- short development for prototyping and time to market;
- low cost manufacturing of small volumes,
- flexibility in designing new microsystems, and reuse of already established and optimised subunits.

All the above mentioned points are to be considered by SMEs in planning a successful exploitation of small volume production for microsystems aimed at niche markets

3.IRST approach to microsystems R&D

IRST intends to be an active partner in this emerging field. To this end during the few past years IRST-Microsystem Division has been active in developing silicon based micromachining technologies and sensor prototypes. Some of the most significant research and developments efforts and the results so far obtained are presented in this review.

Silicon micromachining represent a flexible technology suitable to address many different applications, yet mantaining a unique and fully manufacturable platform based on the mature know-how of the silicon VLSI processing.

Efforts aimed at adequate the IRST-Microsystem Division to successfully tackle and to take advantage of the sensors/microsystems emerging field resulted in a redefinition of the different technical tasks as follows.

a) IRST Microfabrication Facility

The Microfabrication Facility of IRST Microsystem Division is fully equipped to process small-medium volumes of standard CMOS and monolithic silicon integrated devices with a resolution of the order of 1 micron. To address sensor and microsystem developments a new automatic cassette to cassette double side proximity printing photolitography and micromachining dedicated wet-etch benches have been added to the silicon processing pilot line. Furthermore new technological steps mainly aimed at silicon surface and bulk micromachining have been developed and made available for internal prototyping and for external joint research and development projects. Among these new technologies, it seems worth mentioning the anisotropic etching in TMAH solutions, which has been optimised and is now routinely used in fabrication of the sensor micromachined prototypes.

b) TMAH anisotropic silicon etching

Tetra-methyl ammonium hydroxide, or TMAH, is an anisotropic silicon etchant that is gaining more and more attention in the fabrication process of mechanical microstructures and device isolation, as an alternative to the more conventional KOH and EDP etchants because of its high compatibility with conventional IC processes, due to the absence of metal ions in it. The possibility to passivate the aluminum metalization in properly saturated TMAH solution has also been demonstrated by doping the solution with appropriate amounts of silicon or silicic acid /2, 3/. This permits to etch devices with no protection of the aluminum metalization thus increasing the range of application of this etchant while simplifying both the post processing and the etch set-up configuration. As an example the micrograph shown in fig. 1 shows the results of an anisotropic TMAH etch performed on <100> silicon using only aluminum as the masking layer.

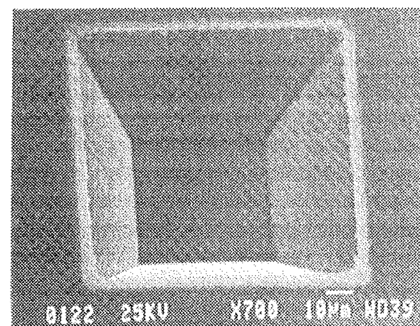


Fig. 1. Cavity produced by the dual-doped 5wt.% TMAH etch using an aluminum masking layer

c) Design and Modelling

Along with the fabrication of microdevices, another important area in the micromachined sensor development cycle is the use of micromechanical device simulators to be coupled with the more conventional TCAD

tools for silicon device and processing simulation. Care is needed on how such tools can be combined to provide an overall design strategy for microdevice design and modelling and for the accurate simulation of all the fabrication cycle. The simulation activity in terms of electro-mechanical device characteristics is routinely carried out at IRST by using ANSYS and ISE-TCAD. In order to evaluate the results of some critical microfabrication process steps (pre-deposition, ion implantation, annealing) and the geometry of the etched 3D-structures, a process simulation with dedicated software tools (SILVACO and ACES) is also performed.

For the electro-mechanical simulation the software package ISE-TCAD is especially useful. This software is based on the finite element method and allows to obtain detailed stress and displacement maps on the membranes, cantilevers and on all the micromachined structures of interest. The simulation maps shown in this review are examples of the results mainly obtained by ISE-TCAD simulation.

d) Packaging and testing

The sensor prototypes developed at IRST-Microsystem Division are packaged and tested internally in order to have a feed-back on the device design and on the technological fabrication process. Once optimised, the device is tested to completely characterised its performance. Due to the large variety of different sensors under development, a number dedicated packaging techniques and of PC controlled characterisation benches, each one dedicated to a specific sensor typology, have been settled and are now routinely used. Modelling is usually needed for a detailed "in depth understanding" of the sensor behaviour. Such a phase involves also numerical simulation work on fluid dynamics and mechanics, with subsequent changes in the packaging solutions developed to meet the performance requirements. In addition, the packaging design has to be optimised to reduce cross-sensitivity between different measurands.

For small volume production the sensor packaging and mounting into an application specific microsystem is carried out externally by an IRST-spin off company, where the due attention to cost and reliability is given. The real challenge for sensor-microsystem manufacturer is to develop custom packaging technologies that meet all the necessary performance and reliability criteria, while keeping the cost of the microsystem assembly at a minimum. Additional requirements arise from the sensor interaction with the external environment to be tested. Hybrid packaging with dedicated IC or conventional electronics is routinely employed. The hybrid solution is usually preferred for niche markets, where a limited number of microsystems tuned to meet special requirements are to be delivered.

1. Examples of micromachined sensors under development at IRST Microsystem Division

a) pressure sensors

Piezoresistive silicon pressure sensors play an important role in many fields of applications, as automotive, process control and biomedical devices, due to their excellent performances, small size and low production cost /4,5/. The transduction of the pressure is accomplished by two pairs of piezoresistors which are placed close to the membrane edge in order to maximize the stress-induced effects (see fig. 2). The four piezoresistors are arranged in a Wheatstone bridge configuration (see fig. 3) where the resulting resistance change is easily converted in a voltage output.

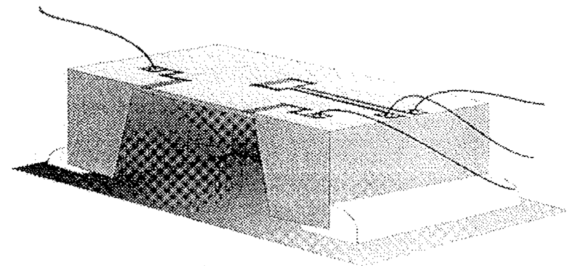


Fig.2. Device cross section.

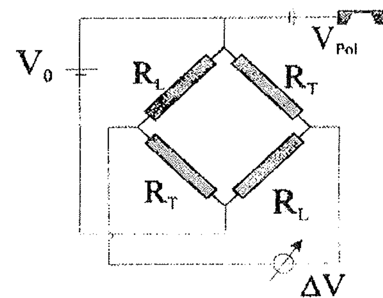


Fig. 3. Wheatstone bridge configuration

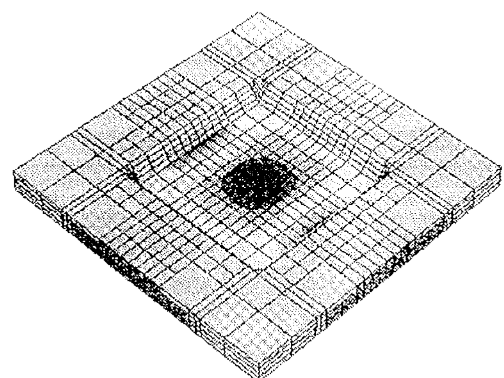


Fig. 4. Stress map simulated by ISE-TCAD. Highly stressed regions are dark. Backside view.

To achieve maximum sensitivity, the four piezoresistors should be centred on the membrane edge where the stress is maximum. 3D modelling of the stress and displacement on the membrane has been extensively used to optimise the piezoresistors layout. Example

shown in fig. 4 refers to a silicon membrane area is 3200x3200μm^2 and the resistor dimensions are 100x500μm^2. The minimum distance between the resistors and the membrane edge is 100μm. Another important design parameter is the maximum load that can be applied to the membrane. This is related to the maximum stress induced in the structure and in turn to the maximum yield of silicon.

A 7-mask dedicated fabrication process, schematically illustrated in fig. 5, has been developed at IRST Microsystem Division for silicon micromachined pressure sensors prototyping and small volume production. The silicon wafers (n-type, 12 Ω·cm, 525 μm thick) are cleaned and a screen oxide (43 nm) is grown at 975°C in pure oxygen. Then a succession of three lithography and ion implantation steps is performed to dope the regions for n^+ contacts, p resistors and p^+ contacts (a). To electrically isolate the device a 700 nm thick LPCVD silicon oxide layer (TEOS) and a 100 nm thick LPCVD silicon nitride are deposited. At this point the contact holes are opened and a 600nm aluminium is sputtered and patterned (b). The frontside of the wafers is then covered by 800nm Low Temperature Oxide (LTO). Next the etching windows, defining the membrane size, are patterned and opened on the backside masking layers. A timed anisotropic etching forms the membranes of the desired thickness (c). Finally the wafers are diced, and the sensors chips are packaged (d) for testing.

No attempt has been carried out toward CMOS compatibility. The required electronics, tailored to specific applications, is available as a separate CMOS chip to be connected externally and mounted in the same sensor hybrid package.

b) flow microsensor

The flow microsensors, now under development, are based on well-known thermal anemometer principles, employing a central resistive heater, R_2, and two temperature sensing resistors, R_1 and R_3, placed on either side /6/. When there is no fluid flow, the heat produced by the central heater will be equally distributed to the symmetrically located temperature sensors. When a fluid flow exists, the symmetry of heat exchange will be modified resulting in an imbalance in temperature. This imbalance is used to determine the flow rate of the liquid.

The microheater fabrication process for flow sensor is schematically shown in fig. 6. The starting material is a 4 inch, 525μm thick, 16-24 Ω·cm, p-type, (100) oriented silicon wafer. A 300 nm TEOS oxide is first deposited by LPCVD, followed by thermal growth of 1150 nm SiO_2. Polysilicon (450 nm) is then deposited by LPCVD, doped with $POCl_3$ to yield a sheet resistance of 27 $\Omega/\square$, and subsequently patterned by photolithography to form the meander-type resistor heater. Upon 100 nm

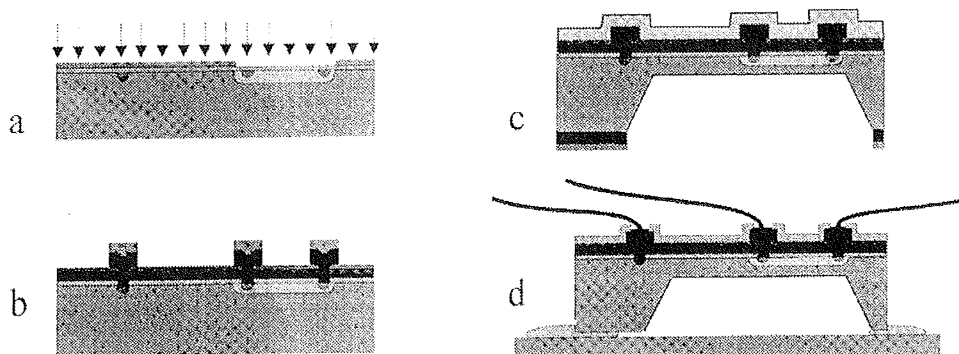


Fig. 5. Main process steps for the fabrication of a piezoresistive pressure microsensor.

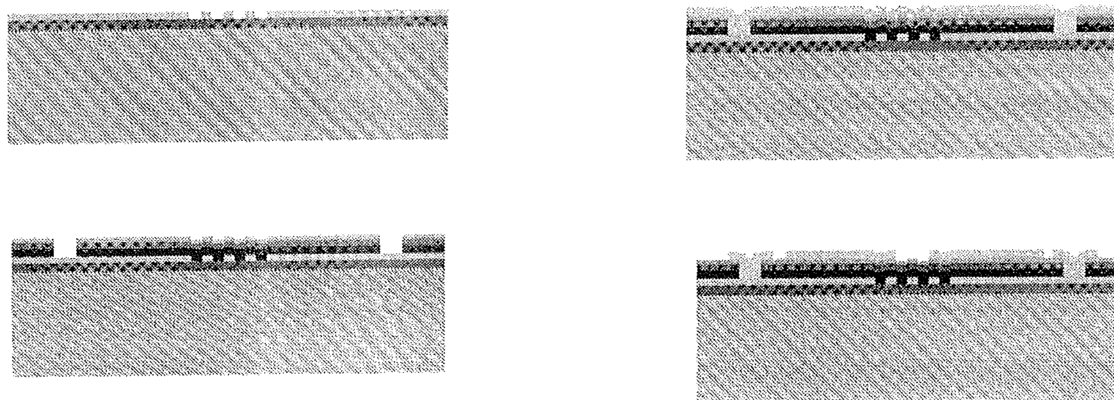


Fig. 6. MIS technological process steps for the realization of polysilicon resistor for flow sensors.

TEOS, 800 nm BPSG is deposited, patterned to contact polysilicon and then reflowed at 925 °C. A 100 nm TEOS and 150 nm Si_3N_4 layers are then LPCVD deposited and patterned to connect the resistor. By sputtering Ti and TiN (30 nm and 200 nm, respectively) and Al (360 nm) are performed to obtain the bonding pads for the polysilicon resistor. The frontside of the wafers is then covered by 800 nm Low Temperature Oxide (LTO) and patterned to contact the metal pads.

Also in this development no attempt will be made toward full CMOS compatibility. The required electronics, tailored to specific applications, will be designed as a separate CMOS chip to be connected externally and mounted in the same sensor hybrid package.

c) microheaters for gas sensors

Chemoresistive, thin- and thick-film gas sensors based on metal-oxide semiconductors necessitate suitable heating modules to achieve the relatively high temperatures (in the range of 300-400°C) required for optimal sensor sensitivity /7, 8/. Basic requirements for such heating modules are excellent temperature uniformity over the sensitive surface area, small dimensions, and minimal power consumption. The latter requirement is essential for portable battery operated gas monitoring systems. Microheater modules consisting of a dielectric stacked membrane micromachined from bulk silicon, with an embedded polysilicon resistors acting as heating and temperature monitoring elements have been developed and are now routinely fabricated by a dedicated process. The microheater enables a temperature up to 500°C to be achieved with a power consumption of less than 30mW. The simplified flow chart of the microheater fabrication process available in IRST is shown in fig. 7. The silicon is anisotropically removed from the backside by TMAH etching, leaving a $2.5x2.5mm^2$ thin diaphragm supported by a surrounding silicon rim. The $5x5mm^2$ chips resulting from wafer dicing are covered by the thick film sensor and mounted and bonded onto TO5 metal cans. A top-view photograph of a fabricated device is shown in fig. 8.

Also in this example the thermal behaviour of the structure was investigated through simulations performed using the finite-element analysis program SOLIDIS. Fig. 9 shows a contour plot of the simulated temperature distribution within the 150x210 μm^2 n+polySi heater area at a heating power of 27.5 mW. A maximum temperature of 490 °C is achieved. By thermal simulation in air and in vacuum it can be seen that, at 490 °C, almost two third of the electrical power provided to the module is dissipated by heat losses to the air.

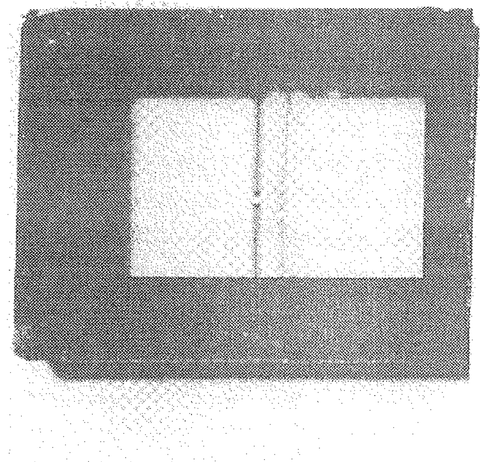
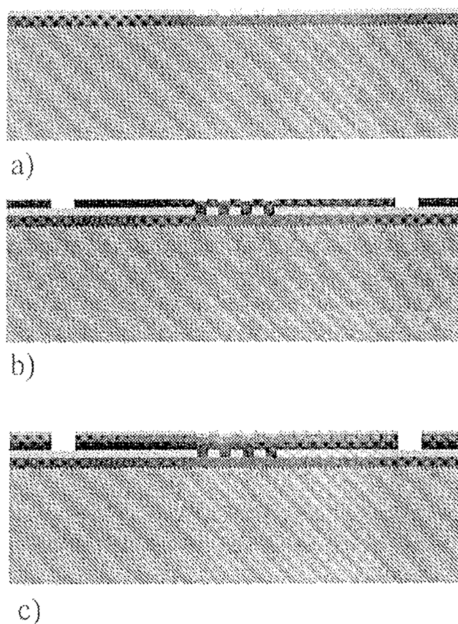


Fig. 8. Top-view photograph of a fabricated device



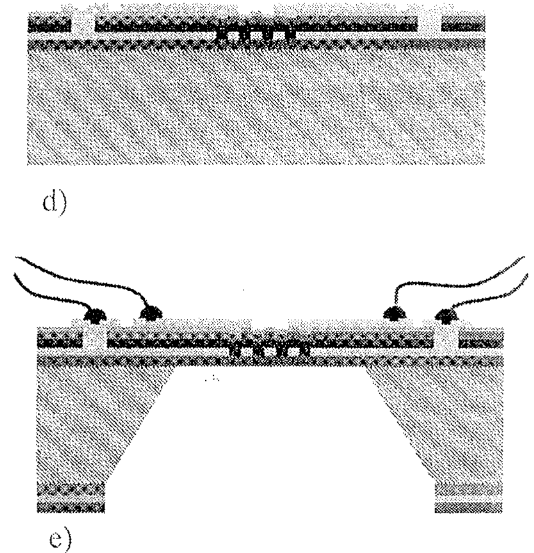


Fig. 7. Gas sensor microheater main technological steps

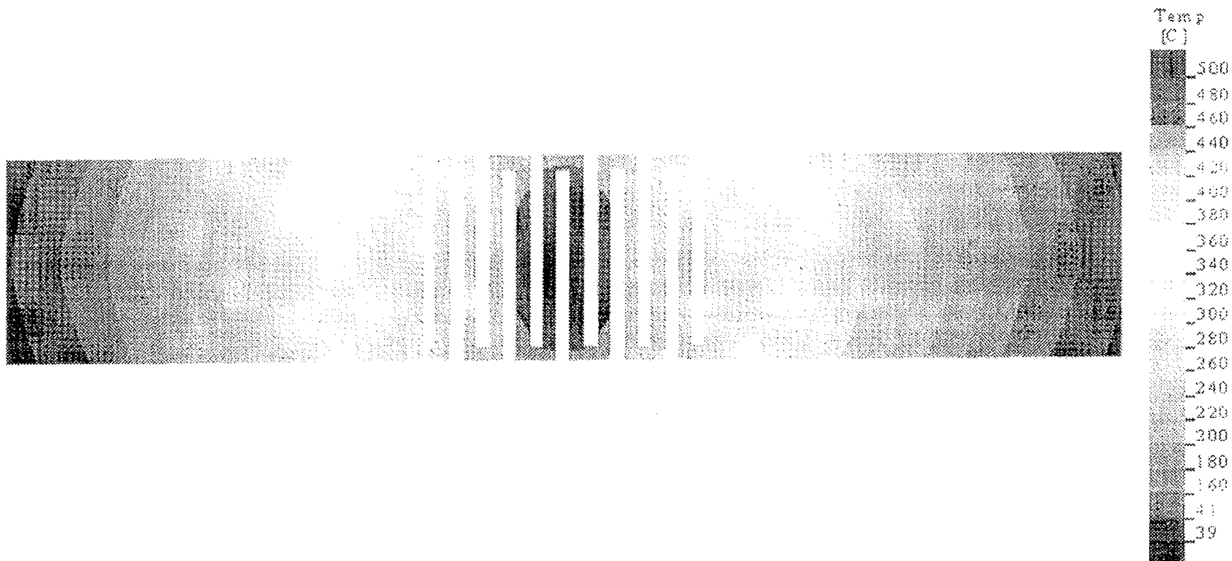


Fig. 9. 2D temperature map within the polysilicon resistor for a heating power of 27.5 mW

d) microcomponents for MW and MMW

Silicon bulk micromachining is becoming an interesting area of activity in the framework of microwave (MW) and millimeter wave (MMW) devices, because of its promising improvements for packaging, decrease of insertion losses and dispersion control /9, 10/. Simple configurations like coplanar waveguides (CPWs) offer such possibilities up to more than 100GHz, and they can be easily used for planar interconnections. Moreover, owing to an intrinsically improved ground control, CPW are favoured for the next generation of MMW subsystems, being suitable of applications for simple interconnections as well as for MMIC and sensor applications.

Coplanar waveguide structures were fabricated on dielectric membranes. The substrates were high resistivity (5 kΩ·cm) <100> p type Si wafers. The dielectric membrane, used to support the coplanar waveguide, was a three-layer of $SiO_2/Si_3N_4/SiO_2$ with an effective dielectric permitivity close to 1. On the backside of the wafers, the same three -layer is used as a hard mask for the TMAH anisotropic etching. 30 nm of Cr and 2.3μm of Au were thermally evaporated and then the desired structures were obtained by wet etching. An example of a 75 Ω micromachined coplanar waveeguide is shown in fig.10.

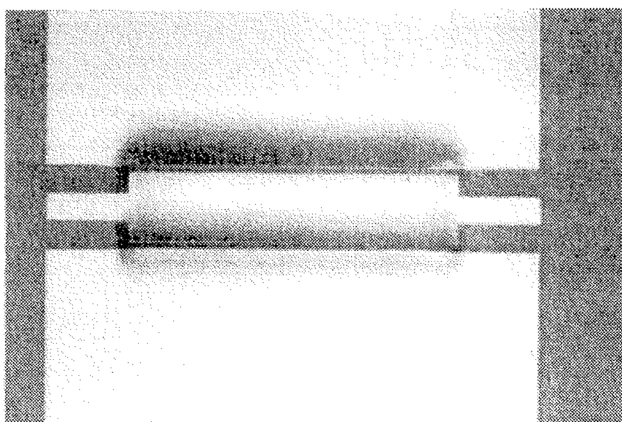


Fig.10. Top view of a coplanar waveguide over the dielectric membrane. The central section of the Au line over the membrane, is 1500 μm long.

e) biomedical microsystems

A new activity worth mentioning refers to biomedical application. The proposed research project will be directed towards the design, fabrication and characterisation of silicon integrated microsystems specifically designed for cancer detection and therapeutics. The term silicon microsystem here refers to microfabricated silicon based structures with biologically activated functions that are realised using standard integrated circuit processing techniques coupled with micromachining techniques /11/. The first project, now under development, refers to a microdevices where the integrated pressure and flow microsensing unit is to be used externally in order to detect urinary disfunction by simultaneously measuring bladder pressure and urine voiding rate as a function of time. These parameters render characteristic pressure-flow signature patterns related to a normal urodynamic condition, and to either abnormal constrictive or compressive obstructions. The device, fitted on a rigid tube attached either to an open-ended condom or onto a modified funnel, can be used to take instantaneous measurements during an annual prostate examination. The same device can be used for in-home monitoring, with the microsensor interfaced with a memory chip for recording yearlong pressure-flow data. The memory chip is then taken to a urologist for data analysis and interpretation on a yearly basis. In this way, changes in urodynamic behavior can be monitored, and any anomalies from the normal function can be identified for a specific period in time.

The miniaturisation of such a sensor allows for disposability and ease of use during bladder voiding. Most importantly, a take-home unit minimises the overall level of discomfort during regular prostate examinations. The fabricated microsensors will be tested parametrically in order to have a feed-back on the technological process: a complete functional characterisation of the devices behaviour will follow before developing the subsequent superficial treatment and the in-vivo tests. In addition, the design will be optimised to reduce cross-sensitivity issues such that measurements of pressure and flow can be taken without one measurand affecting the other.

The prototype chip will be attached to a standard 40-pin dual-in-line package and a plastic tube with a hole cut in the sidewall was firmly attached to the sensor's active region. The hole in the tube will be fitted above the silicon membrane region forming a leak-proof flow channel over the sensor. Pressure sensitivity testing will be performed by sealing one end of the tubing while applying a known pressure using compressed air at the other end.

f) microcalorimeters for High Energy Physics

The above mentioned TMAH etching conditions for aluminum passivation were used to develop a micromachining module aimed to the realisation of three dimensional suspended microcalorimeters (also called microbolometers) in order to optimise the device performances in terms of energy resolution /12/. The dual-doped TMAH solution, beeng passivated with respect to aluminum, permits to simplify both the device fabrication process and the post-processing procedure. As it is shown in Fig. 11 (a) and (b), the microbolometers have been processed with no low temperature oxide (LTO) above the metal pads as metal protection layer. The <100> silicon etched surface shows no hillock protusion on it. Moreover, the absence of oxide protection layer reduce the stress on the suspended bridges.

The Si-implanted thermistor is made by integrating within the suspended layer a resistance doped just below the Metal Insulator Transition, corresponding to the sensitive volume of the thermistor, and by two contact diffusions and low-resistance metal connections for the thermistor electrical contacts. Because the temperature coefficient T_0 for a resistor following the Variable Hopping Range Coulomb gap model is extremely sensitive to dope not uniformly, in principle the resistance should have a box doping profile with a high doping volume uniformity. Furthermore, the doping profile should extend as deep as possible into the bulk silicon in order to obtain an adequate sensitive volume. These requirements can be reasonably satisfied by a series of successive implants with different doses and energies, followed by an appropriate annealing step. In our devices the multi-implant for the thermistor resistance is performed through a photoresist masking of the regions external to the active area. Five Phosphorous implants are necessary to obtain a flat (within few percentages) doping profile, ranging from 0.1μm to 0.6μm under the surface. The profile has been optimised by process modelling. A subsequent series of five Boron implants is necessary in order to partially compensate the thermistor resistance. After photoresist

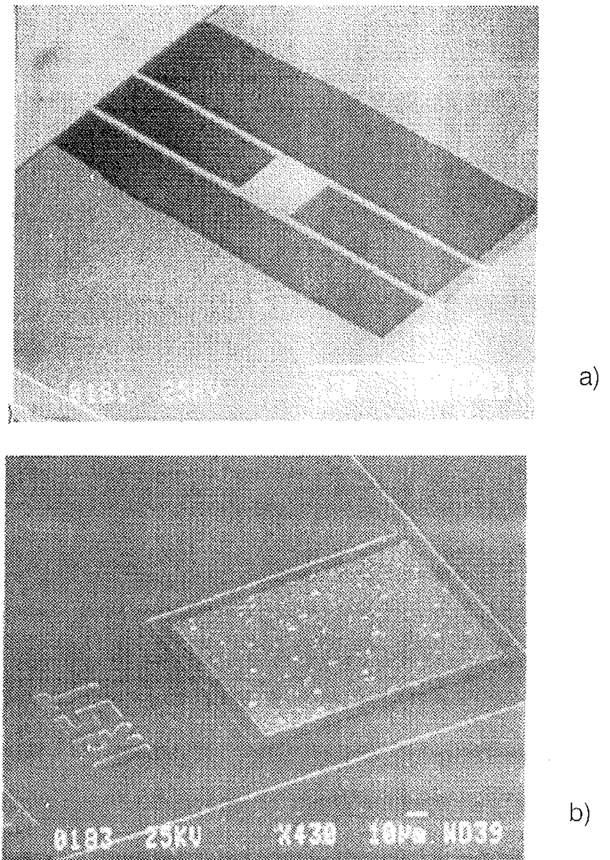


Fig. 11 SEM micrographs of a suspended bolometer (a) and of an aluminum pad with no oxide protection (b).

removal the multi-implant is electrically activated. This is accomplished by a thermal treatment aimed at full dopant activation and implant induced damage removal, but at the same time preserving as much as possible the box like implant profile. Prototipes with an energy resolution of the order of 15eV have been obtained.

Conclusions

Silicon micromachined sensors and devices already available for small volume production or under development at IRST Microsystem Division have been presented. No attempt is made toward CMOS compatibility. The IRST microsystem approach favours hybrid solution, where the components are fabricated by dedicated processing and separately mounted and interconnected together and with the IC driving electronics onto a dedicated package.

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Prispelo (Arrived): 15.10.99 *Sprejeto (Accepted): 25.11.99*

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Lojze Trontelj, Faculty of Electrical Engineering, Ljubljana, Slovenia, **cochairman**

Marko Hrovat, Jožef Stefan Institute, Ljubljana, Slovenia,

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Leszek J. Golonka, Technical University, Wroclaw, Poland

Zsolt Vitez, Technical University, Budapest, Hungary

Monika Jenko, Institute for Metals and Technology, Ljubljana, Slovenia

CONFERENCE ORGANIZING COMMITTEE

Meta Limpel, MIDEM, Ljubljana, Slovenia,

Drago Resnik, Faculty of Electrical Engineering, Ljubljana, Slovenia,

Radko Osredkar, Faculty of Electrical Engineering, Ljubljana, Slovenia

Iztok Šorli, MIKROIKS d. o. o. , Ljubljana, Slovenia

GENERAL INFORMATION

35th International Conference on Microelectronics, Devices and Materials MIDEM´99, continued the tradition of annual international conferences organized by MIDEM Society. These conferences have always attracted a large number of Slovene and foreign experts working in these fields.

Topics covered by the conference are quite diverse. 54 papers in six sessions in three days were presented.

WORKSHOP on MICROSYSTEMS

Starting in 1998, to the programme of the MIDEM Conferences were added workshops, dedicated to each year´s selected special topic. In the framework of the workshop, four to six invited speakers present the chosen topics from different aspects, thus offering the audience valuable information. Time for thorough discussions is provided between invited presentations, and the Conference attendees are encouraged to present their research results in the Conference session dealing with the same topic. For Conference participants, attendance to the workshop is covered in the Conference registration fee with no extra charge. This year we organized

Workshop on MICROSYSTEMS

Selected topics associated but not limited to CMOS main stream fabrication technology covering the design, fabrication and testing of different types of MEMS and MOEMS and other structures were discussed.

Volume production aspects of some microsystems and its future market development were considered.

The workshop was organized by Laboratory of Microelectronics of the Faculty of Electrical Engineering.

Some statistical data:

Number of participants: total 66, 15 from abroad

Number of papers published in the Proceedings: total 51, 14 from abroad

Participant countries: Slovenia, Italy, Austria, Germany, Great Britain, Belgium, Israel, Poland

Conference Proceedings were published before the Conference and have 318 pages. The proceedings can be ordered through MIDEM Society.

For the sake of completeness we here present Conference program, as well as the list of participants.

Same information can be found on our WEB page: http://paris. fe. uni-lj. si/midem/conference99. htm

CONFERENCE PROGRAM

WEDNESDAY, OCTOBER 13

09:00 **WELCOME AND OPENING CEREMONY**

09:15 **SESSION ON CERAMICS, METALS AND COMPOSITES**

CHAIR: M. Kosec

09:15 **INVITED PAPER**

S. Kobe, S. Novak, P. J. McGuiness: Surface Coating of HDDR Processed Nanocrystalline Powders

10:00 **COFFEE BREAK**

10:15 **SESSION ON CERAMICS, METALS AND COMPOSITES**

CHAIR: M. Kosec

10:15 **K. Reichmann, B. Malič, M. Hrovat, M.Kosec:** Densification and Phase Formation in $BaTiO_3/La(Ni,Co)O_3$ Powder Mixtures

10:30 **S. D. Škapin, D. Suvorov:** Diffusion Studies in the Heterogeneous Ceramic-metal MLCs Systems

10:45 **M. Hrovat, Z. Samardžija, A. Ahmad-Khanou, J. Holc:** Interactions Between $LaGaO_3$ Based SOFC Oxide Electrolyte and Ceria Based Anode

11:00 **A. Benčan, M. Hrovat, J. Holc, Z. Samardžija, M. Kosec:** Investigation of $(La_{1-x},Sr_x)RuO_{3+y}$ Based Materials for SOFC Cathodes

11:15 **M. Pinterič, N. Biškup, S. Tomić, D. Schweitzer, W. Strunz, I. Heinen:** The Low-frequency Dielectric Response and Non-linear DC Electrical Transport in κ-$(BEDT\text{-}TTF)_2Cu[N(CN)_2]Cl$

11:30 **M. Mozetič, A. Zalar, J. Jagielski, G. A. Evangelakis, V. Chab:** Theoretical and Experimental Study of Nitrogen Implantation in Titanium Substrate

11:45 **A. Vesel, M. Mozetič, V. Nemanič, A. Pregelj:** Electric Characteristics of Magnetron Cells

12:00 **LUNCH**

14:30 **SESSION ON CERAMICS, METALS AND COMPOSITES**

CHAIR: B. Malič

14:30 **B. Malič, M. Kosec, J. Razinger, Z. Živić:** Cofiring of Capacitor and Varistor Ceramics

14:45 **S. Bernik, Z. Samardžija, N. Daneu, A. Tavčar, M. Cergolj, B. Ai:** Influence of Firing Temperature and Time on Characteristics of ZnO Based High-voltage Varistors

15:00 **P. Panjan, B. Navinšek:** PVD Processes for Environmentally Acceptable Coatings

15:15 **M. Klanjšek Gunde, M. Maček:** Vibrational, Structual, and Macroscopic Properties of Silicon Nitride-Silicon Oxynitride Thin Films Produced by Plasma-enchanced Chemical Vapour Deposition

15:30 **SESSION ON DEVICE PHYSICS AND MODELING**

CHAIR: D. Križaj

15:30 **A. Levstek, J. Furlan, F. Smole:** Screening Effects on Potential Distribution of Ionized Impurities in Semiconductors

15:45 **G. Röhrer, M. Knaipp, R. Minixhofer, H. Noll:** Investigations of Sidewall Effects in Bipolar Transistors

16:00 **B. Cvikl, D. Korošak:** On Current Characteristics Across the Interface of ICB Deposited Schottky Junctions

16:15 **D. Korošak, B. Cvikl:** On Possible Occurrence of Quantum Well States in ICB Deposited Metal/Si Schottky Structures

16:30 **COFFEE BREAK**

16:45 **SESSSION ON THICK FILMS**

CHAIR: M. Hrovat

16:45 **INVITED PAPER**

Leszek J. Golonka: Application of Thick Films in LTCC Technology

17:30 **R. Kisiel:** Exploitation Parameters of Electrically Conductive Adhesive Joints onto PCBs - Preliminary Results

17:45 **D. Belavič, N. Dragos-Codreanu, M. Ruszinko:** A Thick-film Low Cost Multichip Module - A Case Study

18:00 **M. Hrovat, D. Belavič, M. Pavlin:** Some Results Obtained with Thick Film Diffusion Pattering Technology

18:15 **M. Hrovat, D. Belavič, Z. Samardžija, J. Holc:** The Development of Thick Film Resistor Properties During Firing

18:30 **Z. Morawska, K. Bukat , G. Koziol, H. Hackiewicz:** Solderability Preservative Coatings: Electroless Sn in Comparison with Conventional Sn/Pb Surface Finishes of PCB´s

18:45 **M. Santo Zarnik, S. Maček, F. Novak, U. Kač:** Introducting IEEE 1149. 4 Standard - A Feasibility Study

19:15 **COCKTAIL (FACULTY OF ELECTRICAL ENGINEERING)**

THURSDAY, OCTOBER 14

09:00 **WORKSHOP ON MICROSYSTEMS - TUTORIAL SESSION**

CHAIR: L. Trontelj

09:00 **INVITED PAPER**
V. Kempe: Microsystems at Austria Mikro Systeme

09:50 **INVITED PAPER**
L. Hermans, K. Baert: CMOS Processes as Basis for Microsystem Technology

10:40 **INVITED PAPER**
J. Trontelj: Integrated Magnetic Sensors Design Examples

11:30 **INVITED PAPER**
A. Lechner: Chances of Microsystems

12:20 **LUNCH**

14:30 **WORKSHOP ON MICROSYSTEMS – TUTORIAL SESSION**
CHAIR: R. Osredkar

14:30 **INVITED PAPER**
M. Zen, G. U. Pignatel: Silicon Bulk Micromachining for Sensor Technologies

15:30 **WORKSHOP ON MICROSYSTEMS**
CHAIR: R. Osredkar

15:30 **D. Strle:** Open Loop, High Frequency, Programmable Gain CMOS Amplifier

15:45 **A. Pleteršek:** High PSRR Digitally Programmable Differential Oscillator

16:00 **S. Starašinič:** Pipelined Word Comparator

16:15 **D. Raič, A. Vodopivec:** Upgrading IRSIM for Timing Checking

16:30 **COFFEE BREAK**

16:45 **WORKSHOP ON MICROSYSTEMS**
CHAIR: R. Osredkar

16:45 **A. Pevec:** CMOS Hall Device Modeling

17:00 **D. Resnik, U. Aljančič, D. Vrtačnik, S. Amon:** Micromachining of (100) Silicon Pyramidal Tips by Wet Chemical Etching

17:15 **S. Šoba, D. Belavič, M. Pavlin:** Multipoint Thick-film Load Sensor

17:30 **M. Mandeljc, B. Malič, M. Kosec:** Synthesis and Characterization of Lanthanum Doped PZT Thin Films

18:00 **MIDEM SOCIETY CHOIR**

20:00 **CONFERENCE DINNER (GRAND HOTEL UNION)**

FRIDAY, OCTOBER 15

09:00 **SESSION ON SENSORS**
Chair S. Amon

09:00 **INVITED PAPER**
K. Smith: Pixel Detectors

09:45 **D. Križaj, D. Vrtačnik, D. Resnik, S. Amon:** Design of Silicon Microstrip Test Detector Structures for Digital Mammography

10:00 **D. Vrtačnik, D. Križaj, D. Resnik, U. Aljančič, S. Amon:** Fabrication and Characterization of FOXFET Biased Microstrip Detector

10:15 **T. Mali, D. Vrtačnik, D. Križaj, V. Cindro, M. Miku':** New Silicon Microstrip Detector for Digital Mammography – Test and Evaluation

10:30 **U. Uljančič, D. Resnik, D. Vrtačnik, M. Cvar, S. Amon:** Temperature Effects and Compensation for Temperature Drift of Offset Voltage in Silicon Piezoresistive Pressure Sensor

10:45 **U. Uljančič, D. Križaj, D. Resnik, D. Vrtačnik, J. Furlan:** Local Formation of Porous Silicon in Humidity Sensor Processing

11:00 **G. Pasciak, W. Mielcarek, K. Prociow:** Selection of Solid Electrolytes for NO_2 Thick Film Sensor

11:15 **COFFEE BREAK**

11:30 **SESSION ON OPTOELECTRONICS**
Chair: J. Furlan

11:30 **D. Knipp, M. Krause, P. G. Herzog, H. Stiebig, F. König:** Amporphous Silicon Based Multi-channel Sensors with Reduced Metameric Errors

11:45 **K. Brecl, F. Smole, J. Furlan:** Thyristor -like Thin-film Solar Cell Under Illumination

12:00 **T. Brammer, H. Stiebig, J. Zimmer, A. Lambertz, H. Wagner:** Study of the Optoelectronic Properties of μc-Si:H PIN Solar Cells

12:15 **M. Topič, H. Stiebig, F. Smole, J. Furlan:** Transient Behavior of a-Si:H Based PINIP Structures After Voltage Switching

12:30 **J. Krč, M. Topič, M. Vukadinović, F. Smole:** A Detailed Optical Investigation of a-Si:H PIN Solar Cell

12:45 **M. Vukadinović, F. Smole, M. Topič, J. Krč, J. Furlan:** Application of Trap-assisted Tunnelling Theory in a-Si:H Tandem Solar Cells Numerical Modelling

13:00 **Ž. Gorup, J. Furlan:** Modeling Reverse Biased p^+n^+ Tunnel Junctions in a-Si:H Tandem Solar Cells

13:15 **CLOSING OF THE CONFERENCE**

KONFERENCA MIDEM'99 SEZNAM UDELEŽENCEV

MIDEM'99 LIST OF PARTICIPANTS

	NAME	COMPANY - INSTITUTION	ADDRESS	POST.CODE	CITY
1	ALJANČIČ UROŠ	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
2	AMON SLAVKO	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
3	BELAVIČ DARKO	HIPOT-HYB	TRUBARJEVA 7	8310	ŠENTJERNEJ
4	BENČAN ANDREJA	INSTITUT JOZEF STEFAN	JAMOVA 39	1000	LJUBLJANA
5	BERNIK SLAVKO	INSTITUT JOZEF STEFAN	JAMOVA 39	1000	LJUBLJANA
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8	CVIKL BRUNO	FAKULTETA ZA GRADBENIŠTVO	SMETANOVA 17	2000	MARIBOR
9	FAJFAR-PLUT JANETA	HIPOT-HYB	TRUBARJEVA 7	8310	ŠENTJERNEJ
10	FURLAN JOŽE	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
11	GOLONKA LESZEK	UNIVERSITY OF TECHNOLOGY	WYBRZEZE WYSPIANSKIEGO 27	PL-50370	WROCLAW POLAND
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13	HERMANS LOU	IMEC	KAPELDREEF 75	3001	LEUVEN BELGIUM
14	HROVAT MARKO	INSTITUT JOZEF STEFAN	JAMOVA 39	1000	LJUBLJANA
15	JAN FRANC	MIDEM	DUNAJSKA 5	1000	LJUBLJANA
16	JAVORIČ SAŠA	INSTITUT JOZEF STEFAN	JAMOVA 39	1000	LJUBLJANA
17	KENWAY SMITH	UNIVERSITY OF GLASGOW			GLASGOW GB
18	KIESIEL RYSZARD	WARSAW UNIVERSITY OF TECHNOLOGY	UL. KASZIKOWA 75	PL-00662	WARSZAWA POLAND
19	KLANJŠEK-GUNDE MARTA	NATIONAL INSTITUTE OF CHEMISTRY	HAJDRIHOVA 19	1000	LJUBLJANA
20	KNAIPP MARTIN	AUSTRIA MIKROSYSTEME INT. AC	UNTERPREMSTÄTTEN	A-8141	GRAZ AUSTRIA
21	KOBE SPOMENKA	INSTITUT JOZEF STEFAN	JAMOVA 39	1000	LJUBLJANA
22	KOMAC MILOŠ	MZT	TRG OF 13	1000	LJUBLJANA
23	KOROŠAK DEAN	FAKULTETA ZA GRADBENIŠTVO	SMETANOVA 17	1000	LJUBLJANA
24	KOSEC MARIJA	INSTITUT JOZEF STEFAN	JAMOVA 39	1000	LJUBLJANA
25	KRIŽAJ DEJAN	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
26	KRČ JANEZ	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
27	LECHNER ALEXANDER	CTR	BADSTUBEN 40	A-9500	VILLACH AUSTRIA
28	LEVSTEK ANDREJ	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
29	LIMPEL META	MIDEM	STEGNE 11	1521	LJUBLJANA
30	MALI TADEJ	INSTITUT JOZEF STEFAN	JAMOVA 39	1000	LJUBLJANA
31	MALIČ BARBARA	INSTITUT JOZEF STEFAN	JAMOVA 39	1000	LJUBLJANA
32	MALNARIČ SAMO	ISKRA KONDENZATORJI	VRTAČA 1	8333	SEMIČ
33	MAČEK MARIJAN	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
34	MAČEK SREČKO	INSTITUT JOZEF STEFAN	JAMOVA 39	1000	LJUBLJANA
35	MIELCAREK WITELD	ELECTROTECHNICAL INSTITUTE	UL. M.SKLODOWSKIEJ CURIE 55/61	PL-50369	WROCLAW POLAND
36	MORAWSKA ZOFIA	TELE AND RADIO RESEARCH INSTITUTE	UL. RATUSZOWA 11	03-450	WARSAW POLAND
37	MOZETIČ MIRAN	ITPO	TESLOVA 30	1000	LJUBLJANA
38	OSREDKAR RADKO	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
39	PANJAN PETER	INSTITUT JOZEF STEFAN	JAMOVA 39	1000	LJUBLJANA
40	PAVLIN MARKO	HIPOT-HYB	TRUBARJEVA 7	1000	LJUBLJANA
41	PEVEC ALBIN	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
42	PINTERIČ MARKO	FACULTY OF CIVIL ENGINEERING	SMETANOVA 17	2000	MARIBOR
43	PLETERŠEK ANTON	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
44	RAIČ DUŠAN	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
45	REICHMANN KLAUS	TU-GRAZ	STREMAYRG. 16/3	A-8010	GRAZ AUSTRIA
46	RESNIK DRAGO	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
47	REŠETIČ ALEŠ	HIPOT-HYB	TRUBARJEVA 7	8310	ŠENTJERNEJ
48	ROČAK RUDOLF	MIDEM	STEGNE 11	1521	LJUBLJANA
49	SANTO-ZARNIK MARINA	HIPOT-HYB	TRUBARJEVA 7	8310	ŠENTJERNEJ
50	SONCINI GIOVANNI	UVIVERSITY OF TRENTO	TRENTO	38050	MESIANO ITALY
51	STARAŠINIČ SLAVKO	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
52	STIEBIG HELMUT	FORSCHUNGZENTRUM JÜLICH		D-52725	JÜLICH GERMANY
53	STOLYAROVA SARA	HAIFA TECHNION CITY			ISRAEL
54	STRLE DRAGO	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
55	TIETZ FRANK	FORSCHUNGZENTRUM JÜLICH		D-52425	JÜLICH GERMANY
56	TOPIČ MARKO	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
57	TRONTELJ JANEZ	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
58	TRONTELJ LOJZE	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
59	VESEL ALENKA	ITPO	TESLOVA 30	1000	LJUBLJANA
60	VOLKER KEMPE	AUSTRIA MIKRO SYSTEME INT. AC		A-8141	UNTERPRAMSTAETTEN
61	VRTAČNIK DANILO	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
62	VUKADINOVIČ MIŠO	FAKULTETA ZA ELEKTROTEHNIKO	TRŽAŠKA 25	1000	LJUBLJANA
63	ZAJC IGOR	INSTITUT JOZEF STEFAN	JAMOVA 39	1000	LJUBLJANA
64	ŠKARPIN SREČO	INSTITUT JOZEF STEFAN	JAMOVA 39	1000	LJUBLJANA
65	ŠOBA STOJAN	HIPOT-HYB	TRUBARJEVA 7	1000	LJUBLJANA
66	ŠORLI IZTOK	MIKROIKS	DUNAJSKA 5	1000	LJUBLJANA

PREDSTAVLJAMO PODJETJE Z NASLOVNICE
REPRESENT OF COMPANY FROM FRONT PAGE

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COMPANY PROFILE

The company

For nearly 20 years Austria Mikro Systeme International AG has specialised in developing and producing application-specific integrated circuits - ASICs - and application-specific standard products - ASSPs. Austria Mikro Systeme International offers a broad range of customer solutions for the automotive, communications and industrial markets. The company, whose headquarters are located near Graz/Austria, is one of Europe's market leaders in mixed analog/digital ASICs.

Austria Mikro Systeme International offers a flexible interface according to the customers requirements and provides all elements of the value chain as a "one stop shop" for IC- and system solutions: R+D, design, process development, mask lithography, wafer production, assembly and testing. The company provides a wide range of semiconductor processes tailored to the customer's needs, such as HV-CMOS, BiCMOS, SiGe and CMOS in structural widths down to 0.35 um.

In addition Austria Mikro Systeme International maintains design centres in Unterpremstätten, Dresden and Budapest and sales offices in Paris, Milano, Stockholm, London, Munich, Hamburg, Ludwigsburg, Budapest, Barcelona, San Jose/California and Yokohama/Japan.

Austria Mikro Systeme International has been listed on the Vienna Stock Exchange since June 1993. 100% of the shares are free float.

Customer focused

The interests of the customers are pursued by three business units: automotive, communications and industrial. Taking its lead from clearly defined core objectives each business unit resumes full responsibility for sales, marketing and design for its group of customers.

Quality oriented

All quality assurance measures are based on ISO 9000. The company is certified according to ISO 9001 and QS9000/VDA6.1. Austria Mikro Systeme has also been awarded the CECC 90000 certificate, the STACK Technical Approval for advanced quality management by STACK and the Q1-approval by Ford. The company committs itself to responsible, visionary environmental management. Based on this commitment Austria Mikro Systeme International has been one of the first semiconductor manufacturers certified according to ISO 14001 and validated EMAS (Eco Management and Audit Scheme).

COT service

A unique feature of the company's technical capabilities is the COT (Customer Own Tooling) service for mixed signal circuits. These projects involve the customer carrying out the design of the circuit, whilst Austria Mikro Systeme International provides the "Design Kits". They consist of library elements, component models, process-specific parameters and interface files for the CAD software, all for very diverse design platforms. Depending on customer requirements the COT service package is completed by support in evaluation and ramp up of production. For these projects, customers have access to a broad range of high performance processes available.

A special service is provided to customers through the supply of so-called MPWs (Multi-Product Wafer runs). By combining several different chips on a wafer, the customer is offered a cheap entry to modern microelectronics. This is also of extreme interest to universities and research laboratories because it means they can try out the most advanced process technologies (e.g. SiGe-BiCMOS) at an early stage in their development.

AUTOMOTIVE

The penetration of integrated circuits in today's cars amounts to 5% of production value. According to forecasts it will increase to over 15% within the next 5 years. Therefore Austria Mikro Systeme International offers for its automotive customers a range of different CMOS, HV-CMOS, BiCMOS and SiGe process families. The company focuses on the following areas:

- RF-Applications such as keylessEntry and keylessGo systems based on 433/868 MHz
- Distance control-, car protection-, GPS-, telematics- and diversity systems.
- Integrated hall-, acceleration-, pressure-, temperature-, capacitive- and optical sensors
- Airbag-ICs, powerFET-controls, signal processing circuits for sensors
- Micromachines

Austria Mikro Systeme International offers assistance and support for the development and manufacturing of application-specific ICs, based on a comprehensive cell library, combining analog functions with digital parts and high-voltage peripheral cells. Sensor elements and special devices like bipolar transistors complete the library. Different types of micro-controller cors (4-bit, 6805) and DSPs are available for integration.

Furthermore proved A/D-converters in resolutions from 6 to 16 bit in different conversion technologies (SAR, Flash and Sigma Delta) and with sample rates from 8 KSamples/s up to 200 MSamples/s are part of the analog cell library.

Austria Mikro Systeme International is QS9000/VDA6.1 certified.

For further information please contact: Hubert Christ, hubert.christ@amsint.com

COMMUNICATIONS

The communications business unit is the reliable and flexible partner of its customers for ASIC and ASSP applications within the market segments telecommunications, consumer and computer.

The communication products of Austria Mikro Systeme International are the result of a long-term custom design experience and dedication to the communications market which today has become the fastest and most steadily growing field within the electronics industry.

The development of integrated circuits is based on proven building blocks including high performance operational amplifiers, digitally controlled AGCs, data converters, etc. Highly motivated staff with extensive experience in mixed signal design in CMOS and BiCMOS guarantee efficient silicon solutions and shortest design cycles.

The company offers a high degree of system level integration on silicon providing ASIC and ASSP solutions for:

- Analog voice transmission (wire-line telephony, intercom solutions)
- Combined voice-data communications for mixed-media applications (caller ID, ADSI, and other screen-phone services)
- Cordless communications (DECT)
- Pager RF receivers and protocol processors (ERMES)
- Highly integrated cellular radio RF transceivers (CDMA/FM transmit and receive AGC)
- Consumer communications equipment (low power LCD drivers, audio, video)
- Control systems and accessories for domestic appliances (stoves, refrigerators, washing machines, etc.)

Besides the central services of integrated circuit design and manufacturing, the communications business unit provides all services for transformation of a product idea to silicon including assistance at specification, prototyping, application and design/layout support.

For further information please contact:
Hartwin Breitenbach,
hartwin.breitenbach@amsint.com

INDUSTRIAL

Austria Mikro Systeme International has established working relationships with industrial customers around the world. Hundreds of ASICs for applications in measurement-, control- and automation-equipment have been developed and brought into production so far. They provide a stable and continuously growing turnover.

The company focuses on ASICs and ASSPs for precision measurement and metering in industrial and transportation equipment, buildings and homes. Specifically for the emerging electronic meters market quite a number of products are in production today. The development portfolio is extensive: integrated circuits not only for power-meters, but also for heat-, gas-, water- and carburant-metering applications.

The capability to integrate magnetic and optical sensors alongside digital and analog processing circuitry on the same silicon chip will be further exploited. As a result system level costs will be reduced while at the same time performance in terms of power-consumption, EMC and reliability is improved.

Technologically the platforms of CMOS and BiCMOS-processes with structural widths of 0.8 and 0.6 um for current designs are continuously scaled into the deep submicron area to assure highest system level integration.

For further information please contact:
Franz Faschinger,
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KOLEDAR PRIREDITEV - CALENDAR OF EVENTS

DECEMBER 1999

December 1-3, 1999
SEMICON JAPAN 99, CHIBA, JAPAN
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December 5-8, 1999
PLASMA-BASED ION IMPLANTATION,
KYOTO, JAPAN
Fifth international workshop.
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December 5-8, 1999
INTERNATIONAL ELECTRON DEVICES MEETING,
WASHINGTON DC, USA
Contact Phyllis Mahoney, IEDM manager
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e-mail: pwmahoney@aol.com
web: www.ieee.org/conference/iedm

JANUARY

January 9-12, 2000
SEMI INDUSTRY STRATEGY SYMPOSIUM, PEBBLE BEACH, CA, USA
Contact Nancy Stewart, SEMI
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January 18-20, 2000
DECT 2000, ROME, ITALY
Contact Simon, Moss IBC Global Conferences
Tel: +44 20 7453 5495
Fax: +44 20 7636 1976
e-mail: cust.serv@ibcuk.co.uk
web: www.ibctelecoms.com/dect2000

January 23-27, 2000
IEEE MEMS 2000 CONFERENCE, MIYAZAKI, JAPAN
Focus on interdisciplinary research topics on micro electro mechanical devices and systems fabricated on the micrometre and millimetre scales. Plenary talks: Dr. Crhistofer Hierold (Infineon Technologies, Germany) on "Intelligent CMOS Sensors"; Dr. Nobuo Takeda (Ball Semiconductor, Japan) on "Ball Semiconductor Technology and its Application to MEMS".
Contact MESAGO Japan
Tel: +81 3 3359 0894
Fax: +81 3 3359 9328
e-mail: mems@mesago-jp.com
web: www.mesago-jp.com/mems

January 24-25, 2000
EC-MCM 2000, LONDON, UK
Sixth European Conference on MCMs alongside the European Conference on Microsystems. Organised by UK branch of the International Microelectronics And Packaging Society and co-sponsored by Europractice, IEE, IEEE CPMT.
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FEBRUARY

FEBRUARY 2-4, 2000
GSM WORLD CONGRESS, CANNES, FRANCE
Contact Laura Sykes, IBC Global Conferences
Tel: +44 20 7453 5493
Fax: +44 20 7636 1976
e-mail: cust.serv@ibcuk.co.uk
web: www.gsmworldcongress.com

February 7-11, 2000
INTERNATIONAL CONFERENCE ON MICROELECTRONICS AND INTERFACES,
SANTA CLARA, CA, USA
Organised by the American Vacuum Society.
Contact AVS.
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Fax: +1 212 248 0245
e-mail: avsnyc@vacuum.org
web: www.vacuum.org

February 23-26, 2000
BIAS 2000, MILAN, ITALY
International automation, instrumentation and microelectronics conference and exhibition - microelectronics special edition: DSP micro and nanotechnologies, optoelectronics, biomedical applications, smartcards, microsystems.
Contact Ente Italiano Organizzazione Mostre
Tel: +39 2 5518 1842
Fax: +39 2 5501 6755
e-mail: bias.group@bias-net.com
web: www.bias-net.com

February 23-27, 2000
SMARTCARD 2000, LONDON, UK
Contact Martin Scott, Turret RAI
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Fax: +44 1895 454588
e-mail: info@smart.card.uk.com
web: www.smart.card.uk.com

FEBRUARY 23-27, 2000
EUROPEAN INDUSTRY STRATEGY SYMPOSIUM,
MARSEILLES, FRANCE
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web: www.semi.org

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Slika na naslovnici:
Zgoraj: polovica sestavljenega detektorja sledi nabitih delcev z mikropasovnimi silicijevimi detektorji pred vgradnjo v spektrometer DELPHI na trkalniku LEP v Evropskem laboratoriju za fiziko delcev CERN v Ženevi. Z leve proti desni so vidni: sodčasti del detektorjev (črne ploščice), njihova čitalna elektronika na hibridnem vezju (modro), detektorji v smeri naprej (temnozlate ploščice), delno prekriti s hibridnim vezjem (modro in zlato, na enem oznaka B-25), krmilna elektronika in napajanje. Hibridna vezja za prednji del detektorja so bila izdelana na Institutu "Jožef Stefan".
Spodaj: SDX-100S silicijev detektor x-žarkov s stranskim vpadom x-žarkov

Front page:
Upper picture: one half of the assembled silicon microstrip vertex detector before installation in the DELPHI spectrometer on the LEP collider at CERN – European Laboratory for Particle Physics in Geneva. From left to right: detectors of the barrel part (dark plates) their readout electronics on hybrids (blue), forward detectors (dark gold plates), partially covered by hybrids (blue and gold, one marked B-25), electronics drivers and supplies. The forward detector hybrids were produced at the "Jožef Stefan" Institute.
Lower picture: SDX-100S side illumination silicon x-ray strip detector

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Slika na naslovnici: Planarni transformator, novi prozvod Iskre Feritov

Front page: Planar transformer, a new product from Iskra Feriti

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Slika na naslovnici: V letu 1999 firma Mikroiks d.o.o. praznuje deseto letnico obstoja

Front page: In year 1999 Mikroiks d.o.o. celebrates its 10th anniversary

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Slika na naslovnici: Na konferenci MIDEM´99 smo v okviru delavnice "MIKROSISTEMI" videli primere mnogih uspešno realiziranih mikrosistemov. Zgoraj levo: CBM matrika (Fraunhofer IMS), sliko prispeval CTR; zgoraj desno: Par Hallovih elementov z integrirano tuljavo, sliko prispeval LMFE; spodaj levo: Zadnja stran rezine po globinski mikroobdelavi, sliko prispeval AMS; spodaj desno: Si tabletka senzorja pritiska, sliko prispeval LMSFE;

Front page: MIDEM´99 Conference workshop on MICROSYSTEMS showed several examples of successfully realized projects from this field. Upper left: CBM matrix (Fraunhofer IMS), courtesy of CTR; Upper right: Hall element pair with integrated coil, courtesy of LMFE; Lower left: Backside bulk micromachined wafer, courtesy of AMS; Lower right: Si pressure senzor chip, courtesy of LMSFE;

CTR: Carinthian Tech Research, Villach
AMS: Austria Mikro Systeme Intl. AG, Graz
LMFE: Laboratorij za mikroelektroniko, Fakulteta za elektrotehniko, Ljubljana
LMSFE: Laboratorij za mikrosenzorske strukture, Fakulteta za elektrotehniko, Ljubljana