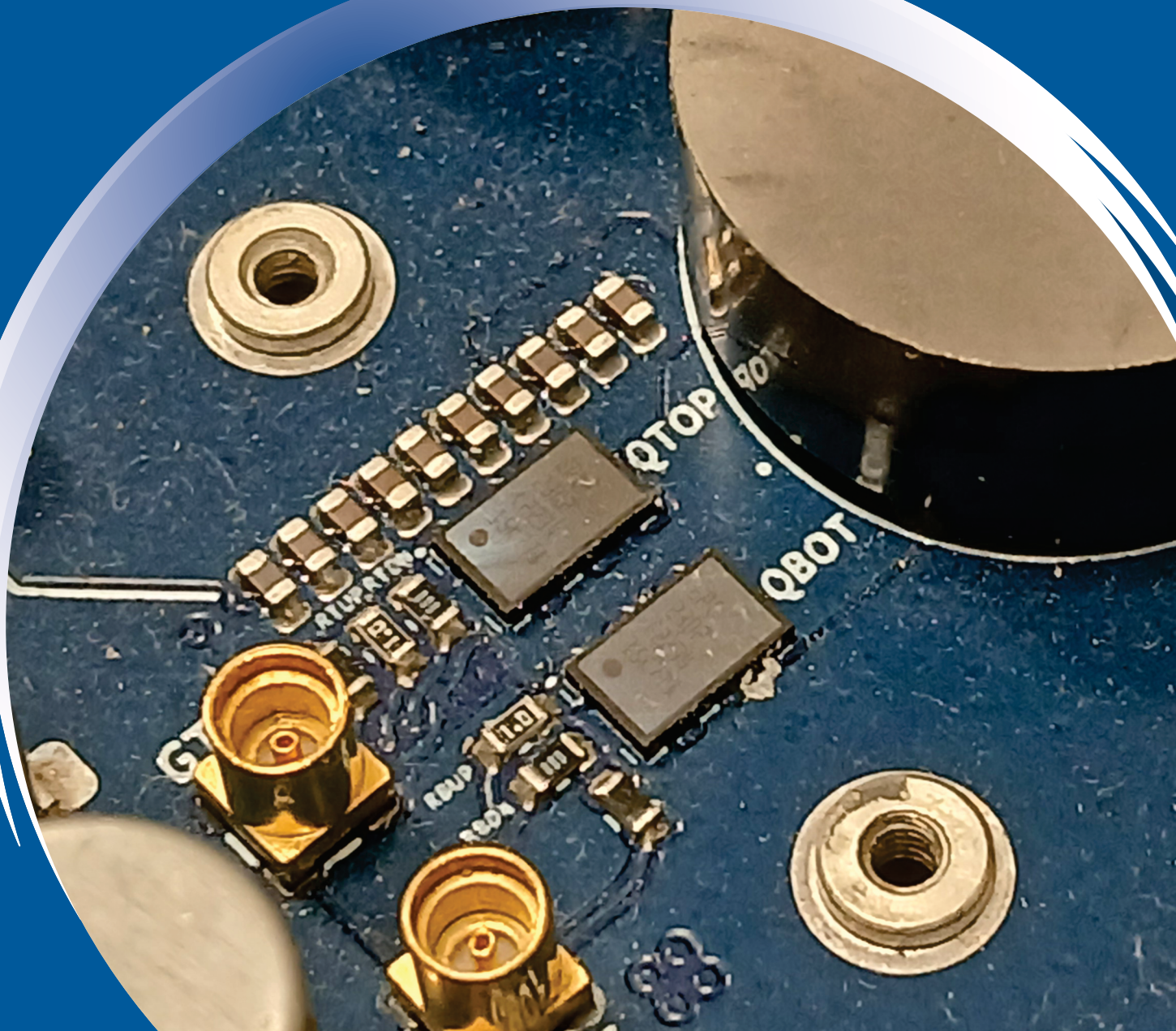
ISSN 0352-9045

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials
Vol. 55, No. 1(2025), March 2025

Revija za mikroelektroniko, elektronske sestavne dele in materiale
letnik 55, številka 1(2025), Marec 2025



UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

Informacije MIDEM *1-2025*

Journal of Microelectronics, Electronic Components and Materials

VOLUME 55, NO. 1(193), LJUBLJANA, MARCH 2024 | LETNIK 55, NO. 1(193), LJUBLJANA, MAREC 2025

Published quarterly (March, June, September, December) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

Headquarters | Naslov uredništva
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Design | Oblikovanje: Snežana Madić Lešnik; Printed by | tisk: Biro M, Ljubljana; Circulation | Naklada: 1000 issues | izvodov; Slovenia Taxe Percue | Poštnina plačana pri pošti 1102 Ljubljana

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
vol. 55, No. 1(2025)

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Editorial / Uvodnik

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- JCR IF-2023= 0.6,
- SNIP-2023=0.366,
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5 March 2025

Original scientific paper
https://doi.org/10.33180/InfMIDEM2025.101

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 55, No. 1(2025), 3 – 23

Challenges for Large-Scale Deployment of WBG in Power Electronics

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Abstract: As the demand for efficient and high-performance power electronic devices continues to grow, wide bandgap (WBG) semiconductors have emerged as a promising solution due to their superior characteristics. However, realizing their full potential requires not only the development of advanced semiconductor materials but also the optimization of packaging techniques. This paper examines the crucial role of packaging in leveraging the benefits of WBG devices, with a particular focus on mitigating inductance and addressing other critical concerns. Drawing from previous research and discussions, we explore various strategies to minimize inductance effects, enhance thermal management, ensure reliability, and optimize electrical performance. Through an interdisciplinary approach that encompasses electrical engineering, materials science, and mechanical engineering principles, this paper highlights the latest advancements in WBG device packaging, providing valuable insights for researchers and engineers working towards more efficient and reliable power electronic systems.

Keywords: wide bandgap; semiconductors; power electronics; packaging; design

Polprevodniki s širokim prepovedanim pasom v pretvornikih močnostne elektronike

Izvleček: Ob nenehno naraščajočem povpraševanju po učinkovitih in visokozmogljivih napravah močnostne elektronike, se polprevodniki s širokim prepovedanim pasom (WBG) zaradi svojih izjemnih karakteristik kažejo kot obetavna rešitev. Uresničitev njihovega polnega potenciala poleg razvoja naprednih polprevodniških materialov zahteva tudi optimizacijo tehnik načrtovanja in pakiranja. Članek predstavi ključno vlogo načrtovanja pri izkoriščanju prednosti WBG naprav, s posebnim poudarkom na zmanjševanju induktivnosti in obravnavanju drugih ključnih vprašanj. Na podlagi prejšnjih raziskav in razprav raziskuje različne strategije za zmanjšanje učinkov parazitnih parametrov, izboljšanje odvoda toplote izgubnih moči, zagotavljanje zanesljivosti in optimizacijo električnih zmogljivosti. S pomočjo interdisciplinarnega pristopa, ki zajema načela elektrotehnike, materialov in strojništva, članek poudarja najnovejši napredek pri načrtovanju WBG naprav ter ponuja dragocen vpogled raziskovalcem in inženirjem, ki si prizadevajo za bolj učinkovite in zanesljive sisteme močnostne elektronike.

Ključne besede: širok prepovedan pas; polprevodniki; močnostna elektronika; pakiranje; načrtovanje

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1 Introduction

Over the past few decades, various sectors, including aerospace, automotive, consumer electronics, industrial, and utilities, have increasingly adopted partial or complete electrification and digitization. This transition, largely driven by advancements in power electronics [1], has not only enhanced existing systems such as industrial electric drives but also facilitated the emergence of new applications, including transportation electrification and renewable energy systems.

By 2030, it is estimated that power electronics will be instrumental in processing about 80 % of global energy production and consumption, underscoring their critical role across multiple industries. Concurrently, the global power electronics market has seen substantial growth, with its value reaching approximately $20

How to cite:
H. Lavrič et al., "Challenges for Large-Scale Deployment of WBG in Power Electronics", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 55, No. 1(2025), pp. 3–23

billion in 2022 (Figure 1). This market is forecasted to expand to around $32.6 billion by 2032, reflecting the increasing dependence on integration of power electronics technologies in diverse applications [2].

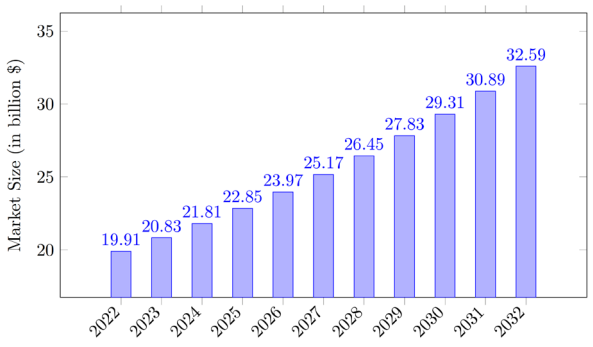


Figure 1: Projections of global market size for power electronics in $ billion. Adapted from [2].

An important shift in modern power electronics is an increasing adoption of wide bandgap (WBG) semiconductor devices [3], which offer superior performance characteristics compared to traditional silicon-based devices. WBG semiconductors, particularly silicon carbide (SiC) and gallium nitride (GaN), are pivotal in driving technological advances across various industries due to their ability to operate at higher efficiencies, frequencies, and temperatures, thus boosting reliability and enabling reduced size and higher power densities.

These improvements are especially important for applications in sectors such as renewable energy, automotive, and industry, where improved performance leads to greater energy savings and reduced environmental impact (Figure 2). The global market for WBG semiconductors is still relatively small but expected to exceed $5 billion by 2032 [4].

However, to fully realize the potential of WBG technologies, several issues must be addressed. Foremost among these is the development of robust packaging solutions capable of withstanding the increased thermal and electrical stresses present in high-performance applications [3], [5]. Additionally, the optimization of device characteristics, such as switching speeds and thermal management, is essential to reduce losses and improve the overall reliability of devices.

One of the key challenges in packaging of WBG devices is the mitigation of parasitic elements such as inductance, capacitance, and resistance. These elements can affect device performance and reliability, with inductance being particularly problematic due to its impact on switching transients, power losses, and electromagnetic interference (EMI). As operating frequencies increase, minimizing inductance is critical for harnessing the high-frequency capabilities of WBG devices.

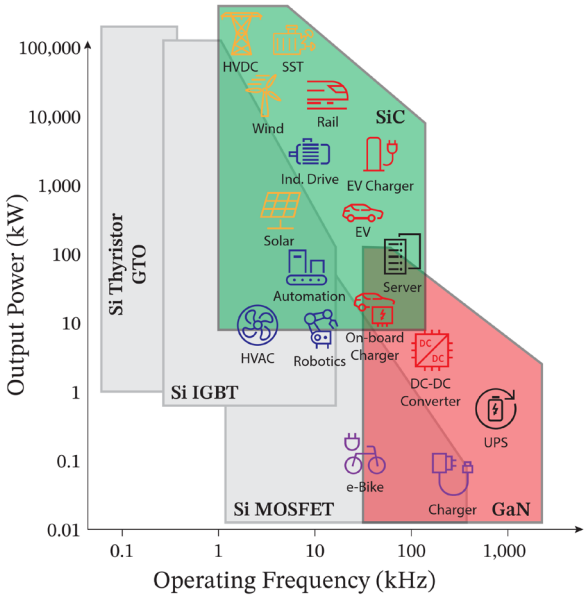


Figure 2: Typical applications with Si and WBG semiconductor switching devices, positioned according to their approximate rated values in terms of output power (kW) and operating frequency (kHz).

Moreover, the demand for compact, lightweight, and thermally efficient packaging solutions adds another layer of complexity to designing and implementing WBG device packages. Traditional packaging materials and techniques may no longer suffice to meet the stringent requirements imposed by the unique characteristics of WBG semiconductors, necessitating innovative approaches and materials to ensure optimal performance and reliability under various operating conditions.

This paper begins with an analysis of the switching phenomena in semiconductor devices (Section 2), followed by a review of WBG semiconductors including material properties, benchmarks, and benefits over silicon-based devices (Section 3). In Section 4 we discuss the effects of WBG device packaging, focusing on parasitics, thermal management, and reliability. Section 5 addresses packaging technologies for mitigation of parasitics effects, covering die attach methods, topside bonding, and innovative cooling strategies. Techniques for enhancing system performance through the integration of gate drivers, passive devices, sensors, and cooling bodies are outlined in Section 6. Section 7 details parasitics parameter estimation techniques and describes design optimization through co-simulation, as well as machine learning (ML) and artificial intelligence (AI) concepts. The paper concludes with a summary of key findings and future directions for WBG technology research in power electronics (Section 8).

2 Power electronics: why switching frequency and transition times matter

Power electronics focuses on efficient control of energy flow using semiconductor switches. Various converter topologies are employed, each designed for specific applications and performance criteria. The half-bridge topology is the most common one. This configuration typically consists of a switching leg with two serial connected power switches (Q_1 and Q_2) and either integrated or external freewheeling diodes, as illustrated in Figure 3.

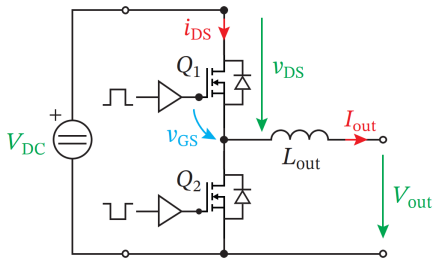


Figure 3: Switching leg with indicated input voltage/current and output voltage/current.

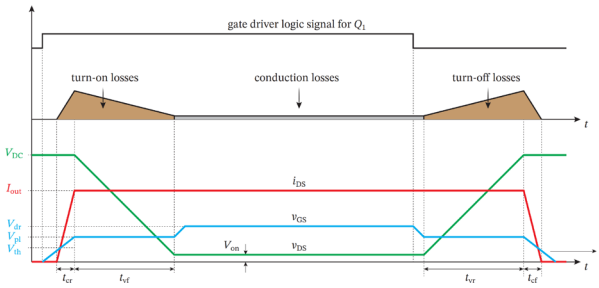


Figure 4: Simplified switching waveforms for turn-on and turn-off transitions in a half-bridge circuit for upper transistor Q_1

In a half-bridge converter, the switches Q_1 and Q_2 are usually driven complementarily using Pulse Width Modulation (PWM) logic signals, producing two distinct voltage levels at the output terminal. The converter operates with a constant input voltage V_{DC}. When Q_1 is on, the output terminal connects to the positive voltage rail; when Q_2 is on, it connects to the negative voltage rail. An output inductance L_{out} is typically included to smooth the output current I_{out}.

If output (and load) inductance is high enough we can simplify the analysis by assuming continuous output current and represent the converter as a constant current source I_{out}. Consequently, when the individual switch undergoes a state transition, a dead-time interval initiates during which the current commutates from the switch to the body diode of the opposite switch.

During the switching action (Figure 4) the transistor is transitioning from off-state to on-state, voltage across the terminals is slowly decreasing after the current increases. A comparable situation occurs when the transistor switches back to the off-state.

Switching losses P_{sw} in MOSFETs occur during these transitions. When the MOSFET is off ($V_{GS} = 0$ V), the voltage V_{DS} between the drain and source is blocked by the device, resulting in zero current ($I_{DS} = 0$ A) and no energy dissipation. Upon turning on the MOSFET, the current I_{DS} begins to increase, while V_{DS} remains constant until I_{DS} reaches its steady-state value. Subsequently, V_{DS} decreases to nearly zero, indicating the MOSFET is fully on and conduction losses commence. The instantaneous power during this transition forms a triangular profile, with the area beneath representing the energy dissipated during turn-on event. The transition time comprises the current rise t_{cr} and voltage fall t_{vf} times.

Turn-off losses are analogous to turn-on losses. In the on-state, V_{DS} is minimal, and current flows through. When turning off, V_{DS} increases while I_{DS} initially remains constant. Once V_{DS} reaches V_{DC}, I_{DS} decreases to zero. The energy dissipated during turn-off is similarly represented by the area beneath the power curve. Switching losses are a sum of turn-on and turn-off power losses that are determined by the product of the dissipated energy and the switching frequency.

Conduction losses P_{cond} in a MOSFET occur when the device is on ($V_{DS} = V_{on}$) and conducting I_{out}. The path between the drain and source acts as a resistance, denoted as $R_{DS,on}$. Thus, the conduction losses depend on the RMS current squared multiplied by the resistance and duty cycle. The losses in off-state can be ignored, as leakage current is negligible.

Thus, total power losses P_{tot} for switch Q_1 are

$$\begin{aligned} P_{tot} &= P_{sw} + P_{cond} \\ &= V_{DS} I_{DS} f_{sw} \left(\frac{t_{cr} + t_{vf}}{2} + \frac{t_{cf} + t_{vr}}{2} \right) + I_{DS}^2 R_{DS,on} D \end{aligned} \tag{1}$$

The thermal power in a converter attributed to losses must be removed by a cooling system. In most applications, the maximum output power is limited by thermal resistance (R_{th}) and the capacity of the cooling system to dissipate this heat, thereby limiting the overtemperature. Thus, the high-efficiency power switches allow for reduced cooling requirements which enables the design of devices with higher power density. Further reduction in volume and mass can be achieved by using smaller passive components such as capacitors and inductors.

Throughout periodic switching transitions, the average output voltage can be adjusted in accordance with the desired duty cycle mandated by PWM, thereby regulating the current flowing through the predominantly inductive output circuit. However, its RMS value is also subjected to the triangular waveform's superimposed AC component. Its peak-to-peak amplitude is directly influenced by the load's inductance, thereby impacting the physical dimensions of the inductor.

In the case of additional smoothing capacitors inserted behind the inductor, such as in DC/DC converters, a similar correlation between the switching frequency and the RMS current of the capacitor emerges. In both scenarios, passive elements can be significantly reduced in size (and cost) with an increase in switching frequency.

3 WBG semiconductors: material characteristics and operational benefits

WBG semiconductors have emerged as an alternative to traditional silicon due to their ability to operate more efficiently and/or to withstand higher voltage and temperature. This chapter focuses on their material properties and operational advantages. The section begins by classifying their bandgaps and detailing their physical material properties, and then discusses various benchmarking metrics. Towards the end, the chapter covers the system-level benefits of using WBG devices and provides a brief comparison of today's commercially available WBG devices, specifically SiC and GaN.

3.1 General WBG characteristics

3.1.1 Bandgap classification

The bandgap is essentially a non-existent or forbidden energy state for electrons, and its value equals the difference between the minimum energy of electrons in the conduction band and the maximum energy of electrons in the valence band. It is expressed in eV (electron-Volts) and depends on the type of material. In conventional semiconductors, the bandgap typically falls within the range of 0.6 eV to 1.5 eV. For example, germanium, silicon, and gallium arsenide have bandgaps of approximately 0.66 eV, 1.12 eV, and 1.42 eV, respectively [6]. Wide bandgap semiconductors are those with an energy gap of over 2.0 eV, including GaN and SiC, which are considered current or future alternatives to Si. In addition to wide bandgap semiconductors like GaN and SiC, the term ultrawide bandgap semiconductor applies to materials with even larger bandgaps, such as diamond and AlN [7]. These, along with Ga_2O_3, are considered by some to be the semiconductor materials of the future [8], [9].

3.1.2 Physical material properties

The most important physical properties of semiconductor materials are summarized in Table 1. The values or ranges of values in the table consist of minimum and maximum values obtained from various sources and are also to some extent conditioned by the development and progress of research over the years [8], [9], [10], [11], [12], [13], [14], [15], [16]. Some parameters are more and others less temperature-dependent [17]. For GaN technology, the upper value of electron mobility equals 2000 cm^2/Vs for the 2DEG layer [12]. This is a 2D layer of freely moving electrons (two-Dimensional Electron Gas) that forms at the interface between AlN and GaN materials due to the polar properties of the base cells of the crystal structures and the shear force at the interface between the two materials [18]. The freely moving electrons in the 2DEG layer essentially make the GaN HEMT (High Electron Mobility Transistor), a normally on transistor.

The wider bandgap leads to better electrical stability of the material at higher electrical fields and higher temperatures. WBG dies are therefore smaller compared to silicon ones, have better channel conductivity in the conduction state and enable higher switching speeds. The higher values of these two parameters are due to the easier movement of electrons through the crystal structure of the material under the influence of an electric field. The smaller dimensions of the WBG dies and consequently the smaller electrode dimensions as

Table 1: Basic material properties including minimum and maximum values from the sources [8] - [16].

	Si	4H SiC	GaN	Diamond	AlN	Unit
Bandgap E_G	1.1 - 1.12	3.25 - 3.26	3.39 - 3.44	5.46 - 5.6	6.2	eV
Critical electric field E_C	0.3 - 0.4	2.0 - 3.18	3.0 - 3.5	4.0 - 7.0	15	MV/cm
Electron mobility μ	1350 - 1500	650 - 1000	900 - 2000	1800 - 2200	450	cm^2/Vs
Hole mobility μ_H	450	90 - 120	10 - 120	1800	-	cm^2/Vs
Thermal conductivity λ	130 - 150	370 - 700	110 - 210	600 - 2300	285 - 340	W/mK
Relative permittivity ε_r	11.8	10	9.0 - 9.5	5.5	8.5	-
Electron saturation velocity v_S	1	2	2.4 - 2.5	2.3 - 2.7	1.4	10^7 cm/s

well as the slightly lower values of the relative permittivity result in small parasitic capacitances of the dies, which further accelerate the switching processes. Fast switching ensures low switching losses and the low resistance of the channel in the conductive state ensures low conduction losses. The small parasitic capacitances at the gate of the transistor also lead to low driving losses [19]. The blocking state of WBG dies is characterized by a lower leakage current, as fewer charge carriers are released due to the large bandgap. In WBG dies, there is only a very small, practically negligible (SiC) or no (GaN) reverse recovery charge, as the latter have no inherent reverse conducting diode. The lower power losses of the individual contributions lead to relatively low total power losses during device operation. The physical properties of the materials enable higher operating temperatures and better thermal conductivity, so that heat can be dissipated more efficiently.

3.1.3 Material's benchmarking

Based on certain physical parameters, various authors have derived criteria for comparing the performance or suitability of materials for specific applications, which can also be used to predict to some extent the properties of the semiconductor devices produced. Johnson's Figure of Merit (JFOM) gives a power-frequency product for low-voltage transistors. Keyes' FOM predicts the switching behaviour of transistors in integrated circuits. For power transistors, two Baliga's FOMs are of interest [20]. The first (BFOM) represents the denominator in an expression for calculating the specific resistance R_{on} of a material in the conductive state

$$R_{\text{on}} = \frac{4 \cdot V_B^2}{\varepsilon_r \cdot \mu \cdot E_C^3} = \frac{4 \cdot V_B^2}{\text{BFOM}} . \tag{2}$$

The BFOM essentially indicates the dependence of the conduction losses on the physical properties and is a measure of the performance of materials for low-frequency operation. The calculated dependencies of the specific resistances on the breakdown voltage V_B for the parameter limits of the individual materials listed in Table 1 are shown in Figure 5. The minimum values of the individual parameters were considered for the lines marked with _min (solid lines), while the maximum values were taken into account for the lines marked with _max (dashed lines). Explicitly, Figure 5 shows that the specific resistance of SiC is a hundred times or more lower than the specific resistance of Si and the specific resistance of GaN is four times or more lower than the specific resistance of SiC.

The second performance metric, BHFFOM (Baliga's High Frequency FOM), establishes the link between the physical characteristics and the ability to operate at higher frequencies, where a significant portion of the

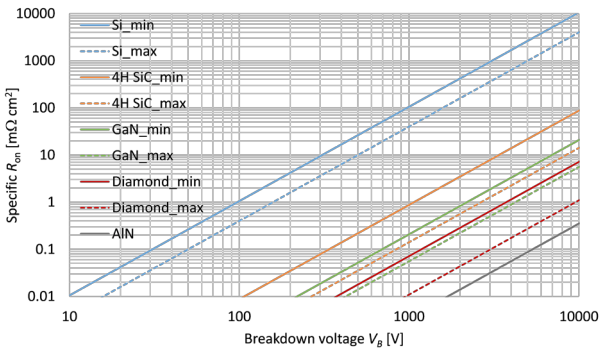


Figure 5: Specific resistances for five semiconductor materials; the calculations are based on minimum and maximum values of parameters taken from various sources.

losses are due to the charging and discharging of the specific input capacitance C_{in}. It has essentially been defined as the reciprocal of the product of specific resistance and specific input capacitance and is written with certain assumptions regarding the basic material properties [20] and the assumed control voltage at the gate of the transistor V_G

$$\text{BHFFOM} = \frac{1}{R_{\text{on}} \cdot C_{\text{in}}} = \mu \cdot E_C^2 \cdot \sqrt{\frac{V_G}{4 \cdot V_B^3}} . \tag{3}$$

The BHFFOM versus breakdown voltages for the minimal and maximal values of the individual materials listed in Table 1 are shown in Figure 6. Different V_G values were used for the calculations, namely 15 V for Si, 20 V for SiC and diamond, and 6 V for GaN and AlN. As can be seen in Figure 6, SiC has a BHFFOM value 25 times higher than Si and GaN has a value more than 40 times higher than Si.

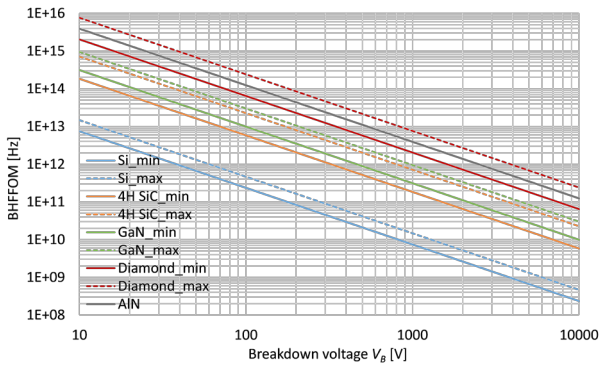


Figure 6: BHFFOM for five semiconductor materials, taking into account the minimum and maximum values of the material properties.

The total losses on the power FET can be calculated by using BHFFOM and assuming I_{rms} in the conduction direction

$$P = I_{\text{rms}}^2 \cdot \frac{R_{\text{on}}}{A} + \frac{A \cdot V_G^2}{R_{\text{on}}} \cdot \frac{f}{\text{BHFFOM}}. \quad (4)$$

The situation for the switching transistor is optimal with minimum losses, which are obtained by deriving eq. (3) on the area of A (dP/dA=0)

$$P_{\text{min}} = 2 I_{\text{rms}} V_G \cdot \sqrt{\frac{f}{\text{BHFFOM}}}. \quad (5)$$

Finally, the required minimum area of the die is determined by

$$A_{\text{min}} = I_{\text{rms}} \cdot \frac{R_{\text{on}}}{V_G} \cdot \sqrt{\frac{f}{\text{BHFFOM}}}. \quad (6)$$

The power loss ratios for the materials under consideration are shown graphically in Figure 7 and for the area ratios in Figure 8. The superiority of wide bandgap materials over Si is clear in Figure 7, but even more evident in Figure 8. It can be seen that the theoretically required active material area of the WBG dies is less than 3 % of the Si material area. In practice, the physical implementation of dies with extremely small areas is difficult due to the implementation of physical contacts and the efficient dissipation of waste heat.

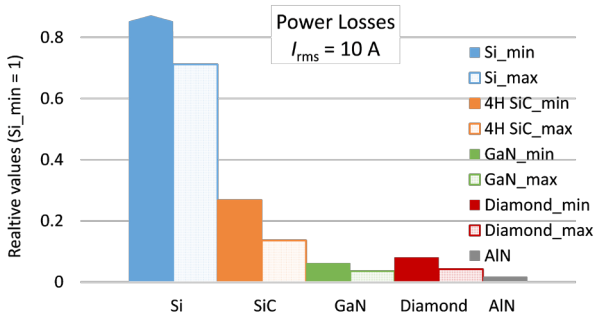


Figure 7: Power loss ratios for various semiconductor materials, taking into account minimum and maximum values of the material properties.

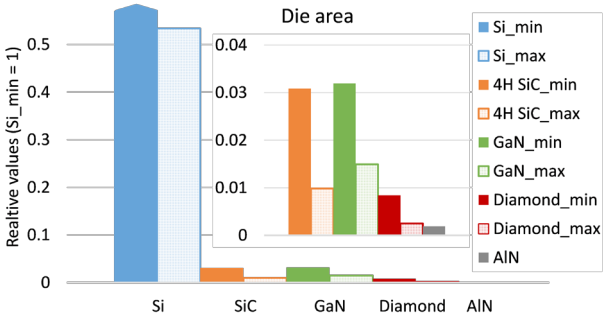


Figure 8: Die area ratios for various semiconductor materials, taking into account minimum and maximum values of the material properties.

3.2 System advantages and market overview

3.2.1 System benefits of using wbg devices

Figure 9 outlines the advantages of WBG semiconductors over traditional silicon-based devices, tracing the impact from material properties to system-level benefits. WBG semiconductors possess a low intrinsic carrier concentration and a high critical electric field, leading to beneficial device properties (Table 2), such as breakdown voltage $V_{\text{B,DSS}}$, Figure of Merit (FOM), thermal conductivity coefficient λ, gate threshold voltage $V_{\text{G,th}}$, and reverse recovery charge Q_{rr}. Low on-resistance reduces power loss during operation, while high blocking voltages improve suitability for high-power applications.

The combination of low on-resistance and high blocking voltage reduces conduction and switching losses. This enhancement not only improves device efficiency but also allows for higher switching frequencies compared to traditional silicon-based devices. Consequently, it enables the use of smaller passive filter components and cooling solutions, significantly reducing both the size and weight of the overall system. Overall, WBG semiconductors have become the first choice for high-power and high-frequency applications.

Table 2: Comparison of main characteristic parameters for Si, SiC and GaN HEMT technologies [21].

Technology	Si-MOSFET (SJ)	SiC-MOSFET	GaN HEMT Cell	Unit
$V_{\text{B,DSS}}$	> 1200	> 1200	650	V
Avalanche capability	YES	YES	NO	-
Short circuits	YES	YES	NO	-
RDS(A) FOM	10	2-3	3-7	mohm·cm^2
λ	1.5	5	1.3	W/cm^{2}K
$V_{\text{G,th}}$	3.5	2.8	1.3	V
Normalized die area	5x	1x	1.5x	-
Q_{rr}	10,000	76	~0	nC
Reverse diode effect V_{forward}	~1.5	~4	1.3-6	V

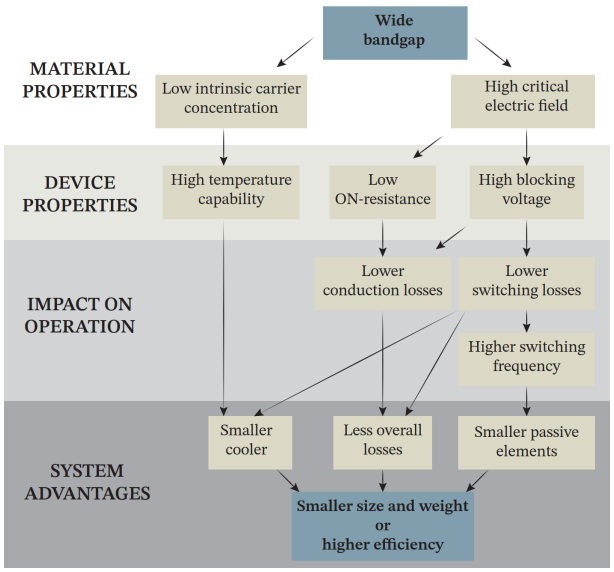


Figure 9: Impact of WBG semiconductor properties on system performance.

3.2.2 WBG market presence: SiC and GaN devices

SiC and GaN dominate the commercial market for wide bandgap (WBG) power devices, each offering distinct advantages over traditional silicon in power electronics. The commercialization of SiC devices began with the first SiC Schottky barrier diodes (SBDs) introduced to the market by Infineon in 2001 and the first SiC MOSFETs in discrete packages by Cree and Rohm in 2010–2011. SiC devices are now commercially available in the voltage class of 650–3300 V [22]. The principal benefits of SiC devices are most evident in applications within the automotive and energy sectors, where their high efficiency and high-voltage blocking capability are required.

The market introduction of GaN power devices dates back to 2010 when International Rectifier released the first GaN-based power transistor. The commercially available GaN devices are primarily classified as lateral GaN HEMTs, which have brought significant benefits to applications that demand high frequency and efficiency, particularly in RF and power supply sectors. GaN devices are currently available primarily in the voltage class of 100–650 V.

Figure 10 compares typical values of key material properties of GaN, SiC and Si. GaN devices, with their high electron mobility, inherently support much higher switching frequencies. They operate effectively at relatively high voltages due to their high critical electric field and exhibit lower leakage currents. In contrast, SiC devices have significantly higher thermal conductivity, enabling better heat dissipation. This advantage is particularly beneficial as it compensates for the relatively

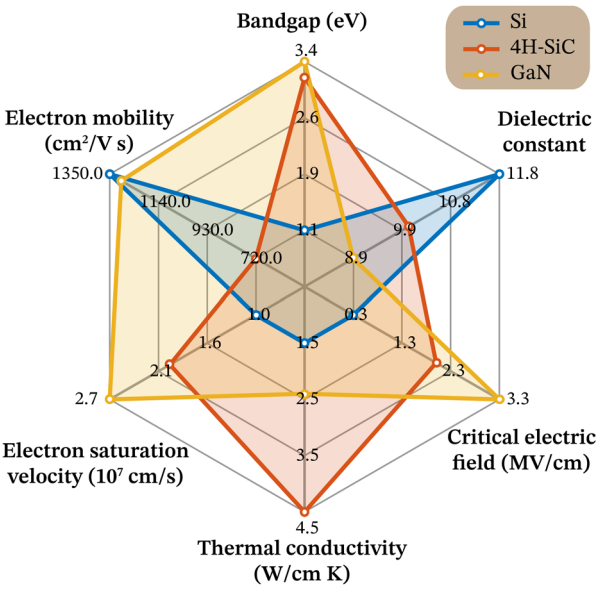


Figure 10: Graphical visualization of material characteristics using typical values for Si, SiC and GaN.

higher specific losses compared to GaN, thus improving overall system performance and reliability.

4 Packaging: electrical and thermal challenges

The use of bare semiconductor dies is uncommon due to handling and reliability concerns. Therefore, semiconductor dies are typically enclosed in various packages containing critical components, such as the semiconductor dies, substrates, baseplate, die bonding, and encapsulant (Figure 11).

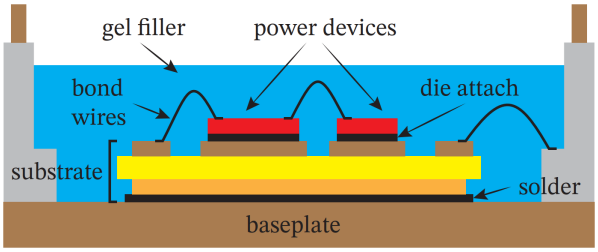


Figure 11: Mockup view of the package cross section showing the power devices (dies with die attachment and bond wires), soldered onto a baseplate. Adapted from [23].

The primary function of the baseplate is to mechanically support the substrate. This is usually a ceramic (alumina, aluminum nitride or silicon nitride) with a metallization of copper (DBC – Direct Bonded Copper) or aluminum (DBA – Direct Bonded Aluminum) on the top and bottom. The top side of the DBC is attached to

the semiconductor power die and supports heat dissipation and electrical conduction, similar to bond wires. The bottom of the DBC is soldered to the baseplate to provide a path for semiconductor chips to dissipate heat, while the core of the DBC provides electrical isolation. The power terminals, including bond wires, provide the electrical connection between the die and the external circuit.

Environmental effects have a significant impact on the performance of the power module and make protective measures necessary. In conventional packaging, an encapsulant covers the surfaces of power devices and bond wires to protect against adverse environmental conditions such as exposure to chemicals, humidity, and gases. Consequently, all elements, except the bottom side of the baseplate, are encased in a plastic covering.

4.1 Power and gate drive commutation loop parasitics

The package structure and applied materials significantly influence the electrical and thermal performance of the device. Specifically, they introduce additional stray resistance, inductance, and capacitance into the power and gate drive loops. These interact with the inherent capacitances of the semiconductor device, which are the key factors in turn-on/off switching behaviour, impacting switching losses, voltage and current oscillations, and resulting in thermal stress [24], [25]. The effect of these parasitics varies on the type of packaging used, as illustrated in Figure 12, and varies on the source contact configurations inside the package, as shown in Figure 13.

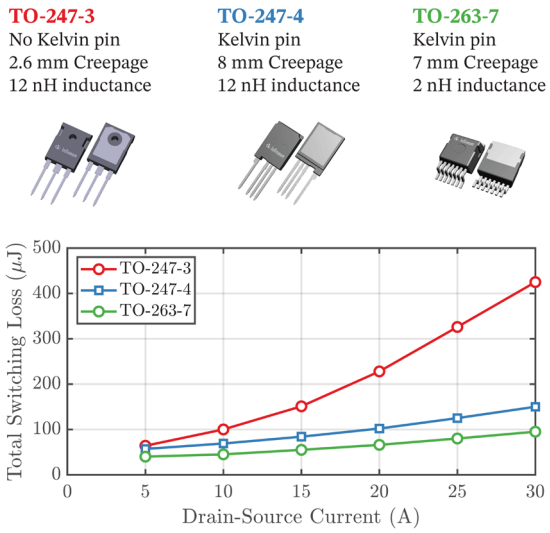


Figure 12: Comparison of parasitic inductance values and switching energy loss for different package types. Adapted from [26].

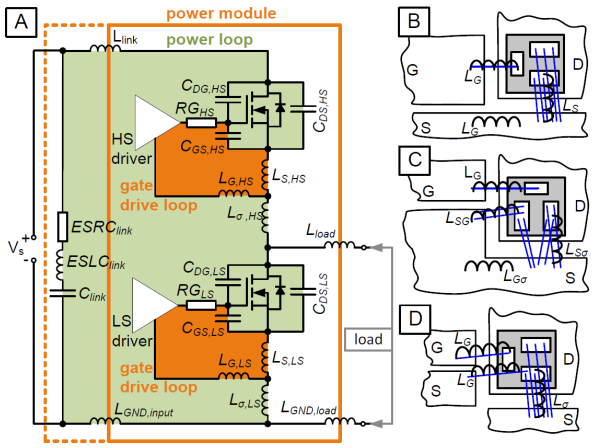


Figure 13: Equivalent circuit of a transistor leg containing structurally introduced parasitic inductances in power and gate drive loop interacting with die capacitances of the MOSFET (**A**). Subfigures (**B**)-(**D**) show various source contact configurations [27].

Furthermore, it is essential to understand that the causes leading to the deteriorated switching performance extend beyond the boundaries of the device package. They encompass all high-frequency current commutation paths (Figure 13), including components like the DC link capacitor, the interconnected traces on printed circuit boards (PCBs), as well as stray capacitances between the power and the gate drive and towards the heatsink (not depicted in Figure 13).

With the increased switching speeds of WBG devices, the circuit experiences higher induced voltages due to the inductance (L_σ). This results in drain-source voltage overshoot and significantly elevates the voltage stress on MOSFETs compared to their (Si) counterparts. Additionally, the L_σ can during the switching transients resonate with various capacitors, such as the MOSFET output capacitor and the body diode junction capacitance. This resonance can couple into the gate drive loop through the Miller capacitor, affecting the driver signal [28]. As a result, this interaction increases switching losses [23] and generates high-frequency electromagnetic interference (EMI).

4.2 Thermal aspects of packaging

In addition to electrical considerations, the design and materials used in packaging are critical for determining heat dissipation capabilities, which in turn affect the overall mechanical design of the converter. As modern WBG devices become more efficient, their physical footprint decreases. Consequently, the heat flux is concentrated over a smaller die area, and the reduced dimensions of the packaging limit heat spreading and dissipation, leading to hotspots within the device. In-

creased temperatures can also compromise the reliability of bonding, interconnections, and insulation layers.

To prevent power derating and improve power density, packaging design must address both electrical and thermal aspects simultaneously [23], [28].

5 Mitigating parasitic effects and thermal challenges in packaging

To fully leverage the advantages of WBG materials [Vecchia, 2019], which are capable of operating efficiently at high temperatures, frequencies, and voltages, traditional packaging designs used for Si-based semiconductors are no longer adequate.

Key drivers for optimizing packaging designs for power devices include:

- **High-speed switching and short current paths**: This necessitates advancements in bonding techniques such as using new materials, employing copper clips instead of wires, and adopting ribbon bonding.
- **High current carrying capability**: Achieved by integrating copper layers with thickness of up to 300 micrometers.
- **Die attachment methods**: Incorporating advanced techniques such as sintering and soldering, whether single-sided or double-sided.
- **Enhanced cooling efficiency**: Techniques such as double-side cooling, thermal vias, microchannels for liquid cooling, and the use of high thermal conductivity substrate materials (such as Al_2O_3, AlN, and Si_3N_4) [29] are crucial. Considerations also include managing the coefficient of thermal expansion (CTE) mismatch and integrating of heat-spreading materials.
- **High-temperature capability:** Ensuring reliability at temperatures exceeding 200 °C.
- **Cost-effective production**: Focusing on precision and reliability in the manufacturing processes.

The importance of these factors varies by application, such as in automotive systems or custom electronic chargers, highlighting the need for specialized packaging solutions tailored to specific voltage, current, and power requirements in different contexts.

5.1 Die attach

For silicon devices, the dies are generally attached to the substrate using lead (Pb)-based solders. These solders have lower thermal conductivity compared to the much higher thermal conductivity of WBG devices. Consequently, WBG devices are usually attached using sintering processes performed under controlled temperature and pressure conditions. Another commonly used method is transient liquid-phase bonding [30], [31]. When selecting materials, factors such as melting temperature, thermal conductivity, and CTE must be considered, as they influence performance degradation during thermal cycling.

However, many current materials and designs are not suitable for operating temperatures above 250 °C. Silver (Ag) sintering is becoming a preferred alternative due to its benefits, including lower thermal resistance

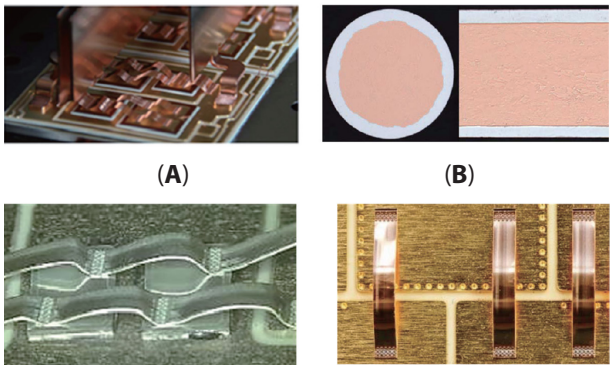
Table 3: New innovative die attach techniques for SiC [26].

Die attach technology	Thermal conductivity	Advantages	Risks
Semi Ag sinter	75-100 W/mK	- Lower R_{th} - Thinner BLT - HVM - Enables 200 °C	- Volatiles - Ag migration - New die/LF interface - Die size limitation
Full Ag sinter	150-300 W/mK	- Lower R_{th} - Better BLT control - Better surge - Higher power density - Enables 200 °C	- Ag migration - High thermo-mechanical stresses - Voiding/porosity - No HVM at assembly vendor
Cu sintering	150-250 W/mK	- Lower R_{th} - Better surge - Higher power density - Lower cost - Enables 200 °C	- Process challenges - Storage challenges
AuSn eutectic (80/20) die backside	57 W/mK	- Lower R_{th} - Thinnest BLT - Better BLT control - Non-Pb	- High thermo-mechanical stresses - Die size limitation - Voiding

(R_{th}), reduced bond line thickness (BLT), and support for higher operating temperature of up to 200 °C (Table 3). Despite these advantages, concerns about Ag migration and increased thermo-mechanical stresses remain. Pressureless Ag sintering, which uses a polymer matrix for densification is a viable option but may offer inferior R_{th} compared to pressure-assisted methods. While copper (Cu) sintering is cost-effective and provides lower R_{th}, its use is limited by the lack of a film-based format and the need for an inert atmosphere. Gold-tin (Au-Sn) eutectics offer a significant advantage with a notably reduced BLT of just 3-4 µm, compared to the more than 50 µm typical of other materials.

Mechanical stresses resulting from power and thermal cycling can lead to cracks between the substrate and die. As a result, self-healing die attachment has become a notable area of interest. However, this emerging technology is still in its developmental stages and may present risks to improving package reliability [32].

5.2 Topside-bonding



(**A**) (**B**)

(**C**) (**D**)

Figure 14: Top: wire-bonding: (**A**) Cu wire-bonding, (**B**) Cu-Al wire bonding. Bottom: Ribbon bonding: (**C**) Al ribbon, (**D**) Cu ribbon [35].

The prevalent use of conventional wire bonding in commercial SiC power module packaging is attributable to its compliance with stringent testing standards, such as successfully passing power cycle tests exceeding 20 million without failure [33], [34]. Aluminum (Al) wires, typically 20 mils in diameter, are predominantly used for wire bonding, despite their limitations on pad size and bonding throughput. Alternatives like heavy Cu wires (Figure 14 A) offer better current capacity and superior thermal conductivity compared to aluminum, as well as enhanced reliability, although they require additional processing steps such as die top system integration or plated topside Cu layers [35]. These challenges are effectively addressed by novel composite materials that combine Al and Cu (Figure 14 B), aiming to optimize bonding processes without changing chip metallization. Moreover, Al and Cu ribbon bonding (Figure 14 C, D) provide a compelling solution for higher current carrying capabilities and improved power cycling performance [31], [36].

5.2.1 Mitigating the magnetic field in the commutation loop

Traditional wire-bonding methods have inherent drawbacks, such as increased parasitic inductance and impeded power module switching speeds. Additionally, predominant material failures like bond wire lift-off and heel cracks, caused by thermomechanical stress, elevate bonding failure to a critical operational concern during power and thermal cycling. In 2002, Nexperia introduced Cu clip bonding technology (Figure 15), marking a significant advancement in power module assembly. Replacing conventional wire bonds with flat Cu clips not only reduces parasitic inductance but also improves heat dissipation from the die's surface. While this approach has been initially introduced for Si technology it has since been transfered to WBG devices [37].

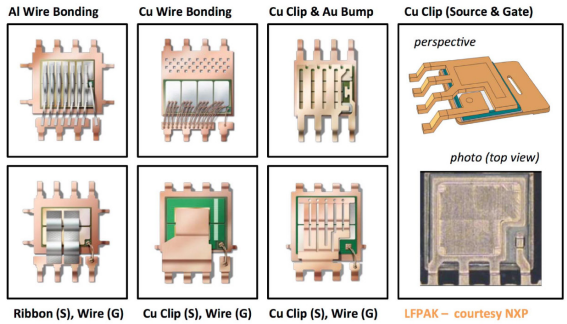


Figure 15: Example of bond-wire and clip-lead power SOP-8 leaded packages [38].

ONSEMI reported a 14 % reduction in junction-to-case thermal resistance for a single-sided PQFN package compared to its conventional wire-bonded counterpart. Nexperia's LFPAK88 package, on the other hand, boasts a source inductance that is five times smaller than that of the D2PAK package [39] (Figure 16).

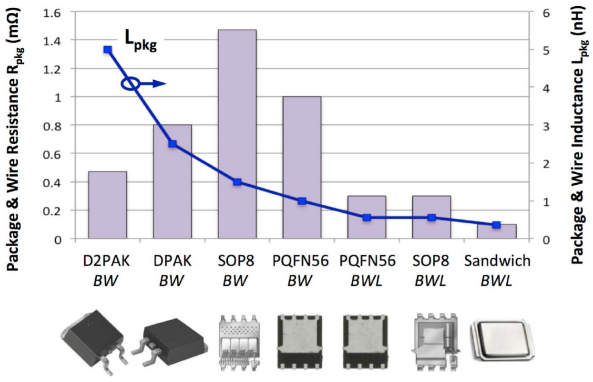


Figure 16: Power package parasitic resistance (bars) and inductance (line) [38].

In 2011, Semikron-Danfoss introduced SKiN technology, a concept designed to minimize stray inductance in their 750 V/1200 V six-pack compatible package. Instead of a solid Cu clip, they utilized a two-layer flex foil tightly positioned over the top and bottom transistors, creating three-layer current paths with minimal loop area. This approach is also employed in standard power stage modules [40], where Ag sintering is used to connect one side of the power chip to the DBC and the other to a flexible circuit board for current conduction. This design achieves remarkably low stray inductance, measuring as low as 2.5 nH per module, including overlapping terminals (DC+ and DC-, Figure 17). In comparison, the equivalent SEMITRANS module exhibits 15 nH stray inductance. The reduction in inductance in structures with close-fitting parallel traces is due to the cancellation of the magnetic field by having opposite current paths. Additionally, a separate study highlights that a significant portion of this reduction is attributable to the overlapping terminals alone. However, replacing Al material with flexible circuit boards imposes limitations on packaging reliability at high temperatures.

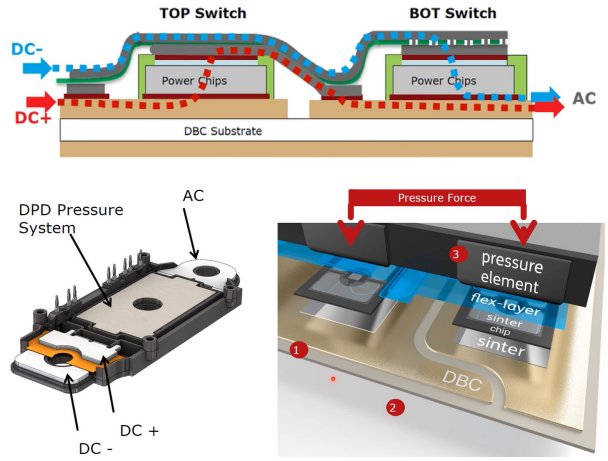


Figure 17: Concept of stray inductance reduction in eMPack package. Adapted from [41] and [42].

The design also incorporates the following features: (1) a ceramic substrate with DSS (Double-Side Sintering) sintered chips, (2) the absence of a rigid joint between the substrate and the cooler, resulting in a low thermal and mechanical stress on the substrate, and (3) a DPD (Direct Pressed Die) pressure system that flattens out cavities downward, ensuring low thermal resistance R_{th}.

5.2.2 Bonding within double-sided cooling structures

A concept similar to SKiN technology has been widely adopted across various packaging designs, with a primary focus on double-sided cooling structures. These configurations are common in high-power-density automotive applications exposed to elevated temperatures from liquid coolants. A notable example is Infineon's HybridPACK DSC (Double Sided Cooling) Power Module featuring SiC MOSFETs. Since the DSC module utilizes indirect cooling, optimizing the thermal interface material (TIM) becomes crucial. Remarkably, the R_{th} of a DSC module can be reduced by 40 % compared to a single-sided cooled module of the same footprint operating under identical conditions [43].

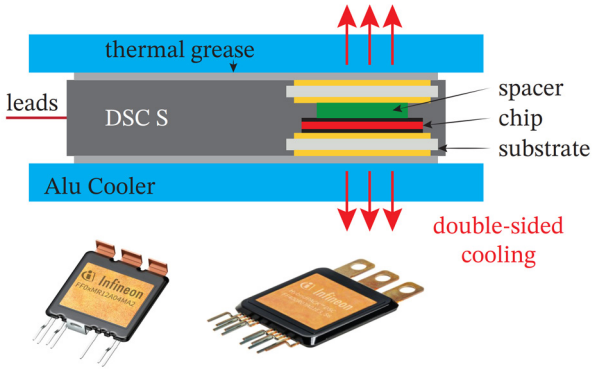


Figure 18: DSC package and its thermal stack

A refined thermal stack configuration, illustrated in Figure 18, showcases improved efficacy. In this design, dies are attached and electrically interconnected on both the top and bottom of DBC. Instead of using traditional spacers, which mainly offer structural support and, in some stack configurations, apply sufficient pressure on current pads to form spring-interconnected stacked power modules, this configuration replaces solder bumps or advanced alternatives with a gold-plated pin-fin-based copper connector (Figure 19). This substitution enhances reliability and addresses common issues such as void formation and cracking that occur in extensive soldering processes.

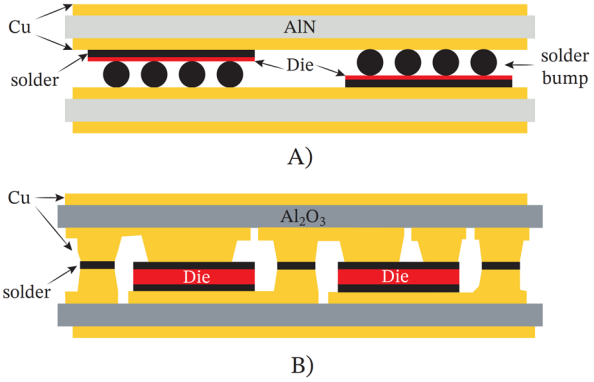


Figure 19: The cross section with (**A**) simple flip-chip technology implementing solder bumps vs (**B**) double-side sintered chips employing gold-plated pin-fin-based copper connection. Adapted from [44].

Consequently, this enhanced structure facilitates an even higher current-carrying capacity. In contrast, the

impact of parasitic capacitances (between the die and baseplate), particularly those subjected to high d*v*/d*t* during switching transients, has a much more significant effect on electromagnetic interference (EMI) and switching performance compared to single-sided configurations [25], [45]. In flip-chip technology (Figure 19), where the die of the bottom MOSFET is mounted opposite to the substrate, reducing the surface with high d*v*/d*t*, alternative methods such as increasing the thickness of the DBC substrate, incorporating an additional copper layer within the DBC for shielding, and introducing low permittivity materials into the thermal stack are found to be less advantageous due to the associated increase in thermal resistance within the power modules.

5.2.3 Kelvin-source connection

Power terminals in higher current-carrying packages are typically designed in blade terminal configurations. Conversely, gate-loop terminals often maintain internal connectivity through wire bonding in many designs. Due to fabrication constraints or safety considerations, the gate drive circuitry is usually kept separate from the power modules on distinct substrate boards. Therefore, it is crucial to minimize gate loop inductance by positioning the gate driver circuitry close to the power device. In three-terminal packages, the gate-loop also includes parasitic inductance L_s, which is placed in series with the source terminal.

As a result, the voltage at the die level may substantially differ from the voltage measured at the terminals due to voltage drops caused by the large current flowing through the power loop [46]. To mitigate the adverse effects of L_s, especially as switching frequencies increase, it is crucial to isolate the gate-loop from the effects of the switch power-loop current. This can be accomplished by implementing a Kelvin-source connection. Given the rising switching speeds of WBG devices, this approach is becoming increasingly important, both in discrete components and in packages containing multiple dies [46]. However, in multi-die modules, the layout of the Kelvin-source connection requires careful consideration, as it significantly impacts current sharing among the dies [47], [48].

6 Comprehensive integration in power modules

One of the prominent trends in power converter design over the past decade has been the increasing level of integration. At the device level, packaging has evolved to minimize stray inductance, facilitate Kelvin-source connections, enhance thermal coupling between the die and the package, and support cooling from both sides.

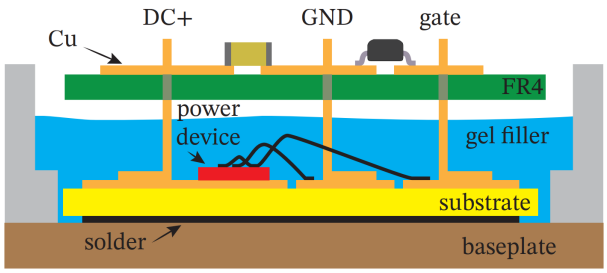
At the package level, integration began with transitioning from discrete devices to power modules, where multiple dies are attached to the same substrate to create the desired circuit topology [49]. This shift significantly simplifies power connections and streamlines converter manufacturing.

6.1 Integration of gate driver

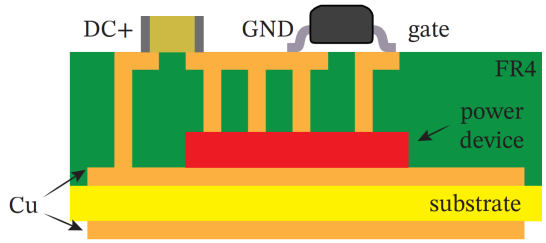
Both the power and gate drive commutation loops significantly affect the dynamics of semiconductor switches, driving extensive efforts to minimize their loops and reduce parasitic parameters. Various methods have been proposed, including the use of new packaging techniques, the addition of Kelvin pins, and the adoption of advanced bonding technologies, as presented in Sections 4 and 5. However, these approaches have their limitations and do not always yield the desired improvements in performance. Studies highlight that while these strategies contribute to reduced parasitic effects, they cannot fully overcome the inherent challenges posed by high-speed switching and the complexity of modern semiconductor devices.

The ultimate step in integration involves incorporating gate driver circuitry [50], [51] directly into the power module. This approach not only simplifies the signal routing for the converter but also substantially reduces stray inductances between the gate driver and the transistor. As a result, it decreases gate voltage overshoots and minimizes ringing [52]. This integration is particularly beneficial for converters using GaN devices, which have stricter gate terminal specifications.

Integrated gate drive GaN products can deliver superior efficiency, increased power density, and reduced magnetic component size across various applications, such as data center power supplies and solar inverters. Specifically, the Texas Instruments' LMG3522R030-Q1, which is automotive-qualified, can switch at 650 V with a frequency of 2.2 MHz and achieve high slew rates of up to 150 V/ns. This combination enables a significant 59 % reduction in the size of power magnetics [53]. Research demonstrates that positioning gate driver integrated circuits and their coupling capacitors on the direct-bonded copper substrate within the power module, rather than on the PCB, can achieve up to 45 % reduction in the gate driver's thermal resistance from junction to ambient. Incorporating an auxilliary source bond wire used as a Kelvin connection for the gate circuitry allows for effectively decoupling of the gate and power loops, achieving gate-source and drain-source loop inductances of 4.6 nH and 6.3 nH, respectively [54].



(**A**) Conventional



(**B**) Integrated

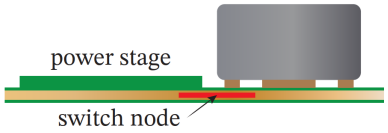
Figure 20: Packaging technologies. (**A**) presents a conventional power module structure. (**B**) demonstrates a PCB/DBC hybrid power module structure. Adapted from [55].

Another option is integrating all components of the switching device into a multilayer PCB, which further optimizes performance by embedding the semiconductor die directly into the PCB, with copper planes connecting peripheral units. This design eliminates bond wires, reducing power loop parasitic inductance to 2.8 nH [55]. However, the use of FR4 PCB material increases thermal impedance, potentially impacting thermal and electrostatic performance. This shortcoming can be addressed with a PCB/DBC hybrid power module structure (Figure 20), where a ceramic substrate is attached to the multilayer PCB with integrated semiconductor die [55]. Gate loop inductance is particularly critical in parallel-connected high-current WBG semiconductors, where synchronized gate voltages are essential to avoid timing mismatches. This synchronization requires low-inductance switching cell designs and equal gate loop parasitics, achieved through PCB layouts with length-matched signal traces connecting drivers to power switches [56].

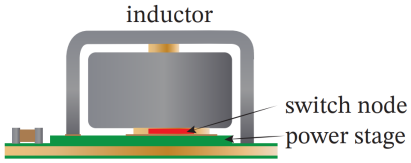
6.2 Integration of passive devices

The increased switching speeds associated with WBG devices make the effects of stray inductances and capacitances more pronounced. To address these issues, some power modules incorporate decoupling capacitors [57]. By positioning the capacitor closer to the transistor leg (Figure 13), voltage oscillations during switching events are significantly reduced, which in turn decreases the required voltage margin.

Integrating an inductor also proves advantageous [58]. As illustrated in Figure 21, this integration offers several benefits. When placed on top of the power stage, the integrated solution has a smaller footprint. It also reduces the capacitive coupling at the switching node, leading to lower electromagnetic interference (EMI). Additionally, if the inductor losses are minimal, it aids in extracting heat from the top side of the power stage.



(**A**) Discrete



(**B**) Module

Figure 21: Integration of inductor with the power module. Adapted from [58] and [59].

6.3 Integration of sensors

The integration of sensors into power modules began with simple inclusion of NTC thermistors. This approach allows for more dynamic measurement of substrate temperature, enabling the converter to operate with a reduced temperature margin. To enhance thermal coupling between the transistor and the temperature sensor, some manufacturers prefer to use a diode as a temperature sensor, which can be mounted on the same die as the power transistor [60].

Another commonly integrated sensor, especially in modules with gate drivers, is the current sensor [61], primarily used for overcurrent protection. Utilizing current mirroring based on sense MOSFETs, as suggested in [61], offers advantages by significantly reducing temperature dependence compared to the $R_{DS,on}$ method.

6.4 Complete control system integration

The complete integration of power devices, gate drivers, current and temperature sensors, and all control logic, including a processing unit (MCU), represents the culmination of integration efforts. Initial attempts, such as IR's PIIPM devices from two decades ago (Figure 22), succeeded in miniaturizing the control electronics to within the power module. However, rapid advance-

ments in silicon technology quickly rendered these devices obsolete.

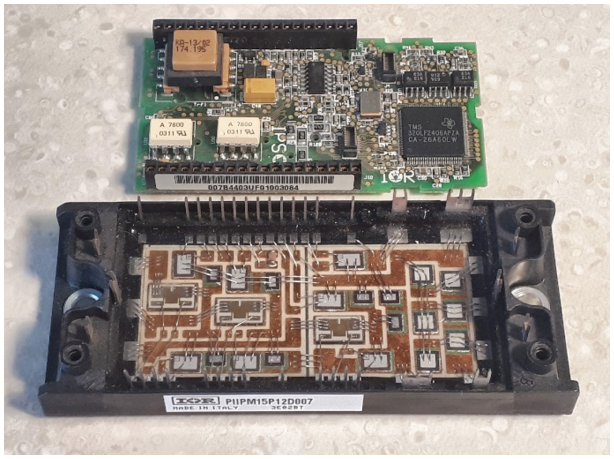


Figure 22: PIIPM power module with corresponding signal electronics including current/voltage sensing, gate drivers and processing unit

Recent examples include the "System in a Package" ST-SPIN32F0, which integrates an MCU along with complete sensing and gate-driving circuitry into a single chip (Figure 23) [62]. DRV10983 takes this a step further by also incorporating a low-power output stage, thereby delivering a complete power system within a single package.

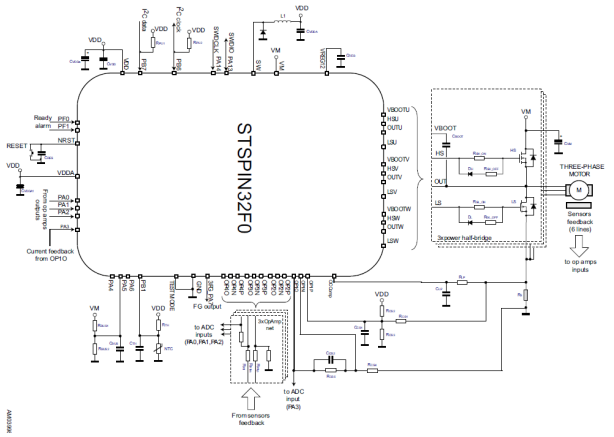


Figure 23: System in a package including processing unit, sensing and gate drivers [62].

Although this level of integration is currently limited to Si-based designs, it is anticipated that similar solutions will soon be available for GaN and SiC power devices.

6.5 Integration of cooling body

Even though the theoretical operating temperature for WBG devices can reach up to 500 °C, leading manufacturers currently offer these devices with a maximum operating temperature of 175 °C. This limitation is primarily due to reliability concerns, specifically the failure rates at the die level, which are further exacerbated by packaging constraints [63].

At the package level, a key focus is on thermo-mechanical reliability, which is particularly well-addressed by double-sided structures due to the robust interconnections between individual dies and their substrates.

Further improvements in reliability can be achieved by integrating the semiconductor die and cooling body into a single component, typically featuring liquid cooling (Figure 24). An advanced example of this integration is seen in embedded designs, where these components are integrated into the printed circuit board [64].

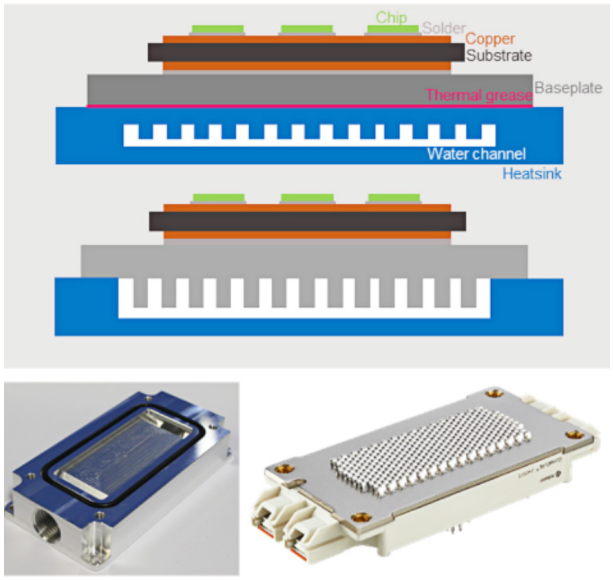


Figure 24: Schematic of power modules (upper section) with both closed (top) and open (bottom) liquid heat sink solutions. Photograph of the wave technology applied to the power module baseplate, along with the open heat sink (lower section) [65].

7 Advanced techniques in power electronics design optimization

The approach to designing power electronics systems has evolved significantly in recent decades. Traditional methods, based on experience and analytical techniques, are now heavily supplemented by multi-domain simulations, including electromagnetic, thermal, and mechanical analyses, and lately also by machine learning and artificial intelligence concepts. The focus has shifted towards accelerating prototyping and optimizing parameters such as efficiency, compactness, and EMC/EMI characteristics. The rise of WBG semiconductors, with their higher switching frequencies and dynamics, has made parasitic parameters of PCBs, pow-

er modules and even integrated circuits – inductances, capacitances, and resistances – critical to performance.

Accurate modeling of parasitic elements is essential for WBG modules, as small deviations can significantly affect converter operation. For instance, errors exceeding 10 % in loop inductance modeling can impact performance notably, highlighting the need for precise electromagnetic simulations [66].

Three main methods are used to estimate parasitic parameters: numerical simulations, analytical approaches, and experimental measurements.

7.1 Numerical simulations

Numerical tools such as Ansys Q3D, which uses finite element analysis (FEA) and the Method of moments (MOM), accelerated by the Fast multipole method (FMM) help analyze parasitics and optimize designs by accounting for proximity effects and skin effects, dielectric and resistive losses, and frequency dependencies [67]. Such tools have been validated for both discrete and module-level analyses [68], [69], improving designs by reducing the inductance and optimizing current distribution.

Authors in [70] demonstrate reduction of power loop inductance by 70 % by changing the design from lateral to vertical. A similar method was also presented for a 135 kW SiC-based traction inverter [71]. The authors in [72] significantly reduced the inductance by using multiple PCB layers for improved current distribution and magnetic field cancellation.

Sun et al. emphasized the importance of evaluating parasitic inductances for estimating the oscillation challenges during the hard switching process [73], while Liu et al. show through LTSpice simulations that the common-source inductances can increase the converter losses by up to 20 % [74].

The common-source inductance is affected by several parameters (leakage inductances of the common conductive path between power and gate loop, coupling factor of power and gate loop, presence of Kelvin source connection, internal bond structure, number of bond wires, gate loop area, submount size), which have different effects as shown by the analysis using the CST studio software [75].

As operating frequencies approach 1 MHz, the design of passive components becomes increasingly complex. Novel high-frequency GaN converters sometimes employ PCB inductors, where FEMM simulations are essential for accurate design and evaluation of parasitic elements [76].

7.2 Analytical methods

Analytical methods, though often more complex to derive, can offer speed and accuracy. Traditional inductance calculations using the Biot-Savart law may overestimate values when PCB trace dimensions are small. To address this, updated analytical methods [77] provide more accurate estimates and are validated through FEA analyses (program package Magnet) and experimental results. Simplified parasitic models are also employed to reduce the complexity of numerical simulations, streamline parameter sweeps, and improve design efficiency [73].

7.3 Experimental measurements

Parasitics can also be estimated through experimental measurements, either indirectly through transient signals and ringing characteristics [78], [79] or directly through impedance measurements. The latter are particularly useful for the characterization of decoupling capacitors [78], SMD resistors, and ferrite beads [79].

The extraction of parasitic parameters and characteristics of packaged SiC [80] and GaN [81] power transistors can also be done by measurements using the S-parameters. A similar approach using S-parameters is also useful for verifying the results of simulation models using Advanced Design Systems (ADS) software [82].

7.4 Design Optimization through Co-Simulation

In addition to parasitic inductances and capacitances [83], optimizing thermal performance is a critical aspect of the design process. Tools like Ansys Icepak, combined with Ansys Q3D and Maxwell, facilitate electro-thermal co-design by balancing inductance, capacitance, and thermal management [78]. Parasitic RLC parameters estimated by simulations are often used in combination with SPICE models of devices in conjunction with other simulation packages, such as COMSOL Multiphysics to evaluate electro-thermal properties and improve designs of power modules [79].

Overall, the integration of these advanced techniques into the design process is crucial for maximizing the performance and reliability of modern WBG-based power electronics systems.

7.5 Machine learning and artificial intelligence concepts

Machine learning and artificial intelligence concepts are rapidly transforming the field of power electronics and semiconductors by addressing challenges across design, control, and maintenance life-cycle phases [84]. These technologies excel in tasks, such as optimization, classification, regression, and data structure explora-

tion. For instance, ML facilitates the discovery of novel semiconductor materials through classification and predicts their physical, electrical, magnetic, or chemical properties [85]. Such materials are essential for the design of integrated circuits and power module packages, where advanced ML methods like deep learning and reinforcement learning are widely implemented in electronic design automation (EDA) for tasks such as placement, routing, and performance prediction [86]. Furthermore, AI enables reliability-focused design by mitigating the computational burden of finite element method simulations through dataset-driven predictions applied across functional design, reliability design, manufacturing, and testing phases [87].

AI and ML further enhance the design and prognostics of power modules, particularly in thermal management and material selection [88], [89], [90]. Combined approaches using genetic algorithms and FEM simulations have demonstrated significant optimizations, including a 27 % reduction in heat sink volume and a 6 °C decrease in junction temperature [91]. Similarly, multi-objective genetic algorithms have been applied to optimize Al ribbon loop dimensions, minimizing plastic strain and temperature [88]. ML also improves manufacturing processes by increasing wafer yield, optimizing die pickup procedures [85], [88], [92], and enabling fault diagnosis for wire-bonding equipment [93]. Conventional power converter design, often iterative and time-consuming, is now accelerated using genetic algorithms and artificial neural networks for multi-objective circuit parameter design with reduced computational time, as demonstrated in a 1 kW GaN inverter prototype [94], [95]. AI-driven digital twin modeling enables the prediction of transient behaviours and failure mechanisms, such as bond wire lift-off and junction temperature estimation in wide bandgap semiconductors [96], [97]. A new class of intelligent systems, called cognitive power electronics [98], integrates AI with embedded sensors and real-time analytics, demonstrating the transformative potential of these technologies. As computational capabilities continue to advance, ML and AI are expected to play an increasingly critical role in shaping the future of power electronics design and optimization.

8 Conclusions

WBG semiconductor switches such as SiC and GaN offer significant advantages compared to traditional Si-based counterparts.

The rise of WBG materials demands advanced packaging and design strategies to fully exploit their high-temperature and high-frequency capabilities. Traditional Si-based packaging techniques are insufficient, necessitating innovations in die attach methods, bonding techniques, and module integration.

High switching speeds necessitate a substantial reduction in parasitic parameters. This process is supported by accurate modeling and advanced design optimization techniques, such as multi-model co-simulation, novel analytical methods, and extensive experimental measurements. Moreover, machine learning and artificial intelligence concepts are playing an increasingly important role in supporting these design and optimization processes in power electronics, leading to reducing design times and improved performance. As computational power continues to grow, the impact of ML and AI in these areas is expected to expand further.

In summary, leveraging these innovations and design techniques will drive the next generation of power electronics, improving efficiency, compactness, and reliability in a wide range of applications.

9 Acknowledgments

The authors gratefully acknowledge the financial support of the Slovenian Ministry of Higher Education, Science, and Innovation, as well as the Slovenian Research and Innovation Agency (Grant: P2-0258).

10 Conflict of interest

The authors declare no conflict of interest.

11 Author contributions

Henrik Lavrič: Investigation, writing. Peter Zajec: Conceptualization, writing. Klemen Drobnič: Visualization, writing. Andraž Rihar: Conceptualization, writing. Vanja Ambrožič: Group supervision, writing. Danjel Vončina: Funding acquisition, writing. Mitja Nemec: Conceptualization, writing. All authors read, reviewed, edited, and approved the final version of the manuscript.

12 References

1. O. S. Chaudhary, M. Denaï, S. S. Refaat, and G. Pissanidis, "Technology and Applications of Wide Bandgap Semiconductor Materials: Current State and Future Trends," *Energies*, vol. 16, no. 18, p. 6689, Sep. 2023, https://doi.org/10.3390/en16186689.

2. "Power Electronics Market Size to Hit US$ 32.59 Billion by 2032." Accessed: Jan. 19, 2024. [Online]. Available: https://www.precedenceresearch.com/power-electronics-market
3. J. Millan, "A review of WBG power semiconductor devices," in *CAS 2012 (International Semiconductor Conference)*, Sinaia, Romania: IEEE, Oct. 2012, pp. 57–66. https://doi.org/10.1109/SMICND.2012.6400696.
4. Allied Market Research, "Wide Bandgap Semiconductors Market Size & Trends 2032," Allied Market Research. Accessed: Sep. 06, 2024. [Online]. Available: https://www.alliedmarketresearch.com/wide-bandgap-semiconductors-market
5. J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014, https://doi.org/10.1109/TPEL.2013.2268900.
6. C. Kittel, *Introduction to solid state physics*, 8. ed., [Repr.]. Hoboken, NJ: Wiley, 2005.
7. M. H. Wong, O. Bierwagen, R. J. Kaplar, and H. Umezawa, "Ultrawide-bandgap semiconductors: An overview," *J. Mater. Res.*, vol. 36, no. 23, pp. 4601–4615, Dec. 2021, https://doi.org/10.1557/s43578-021-00458-1.
8. S. J. Pearton, F. Ren, M. Tadjer, and J. Kim, "Perspective: Ga_2O_3 for ultra-high power rectifiers and MOSFETS," *J. Appl. Phys.*, vol. 124, no. 22, p. 220901, Dec. 2018, https://doi.org/10.1063/1.5062841.
9. A. L. Hickman, R. Chaudhuri, S. J. Bader, K. Nomoto, L. Li, J. C. M. Hwang, H. G. Xing, and D. Jena, "Next generation electronics on the ultrawide-bandgap aluminum nitride platform," *Semicond. Sci. Technol.*, vol. 36, no. 4, p. 044001, Apr. 2021, https://doi.org/10.1088/1361-6641/abe5fd.
10. J. L. Hudgins, G. S. Simin, E. Santi, and M. A. Khan, "An assessment of wide bandgap semiconductors for power devices," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 907–914, May 2003, https://doi.org/10.1109/TPEL.2003.810840.
11. K. Takahashi, A. Yoshikawa, and A. Sandhu, *Wide bandgap semiconductors: fundamental properties and modern photonic and electronic devices*. Berlin: Springer, 2007.
12. T. P. Chow, "Progress in High Voltage SiC and GaN Power Switching Devices," *Mater. Sci. Forum*, vol. 778–780, pp. 1077–1082, 2014, https://doi.org/10.4028/www.scientific.net/MSF.778-780.1077.
13. T. P. Chow, "Wide bandgap semiconductor power devices for energy efficient systems," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Blacksburg, VA, USA: IEEE, Nov. 2015, pp. 402–405. https://doi.org/10.1109/WiPDA.2015.7369328.
14. X. Ding, Y. Zhou, and J. Cheng, "A review of gallium nitride power device and its applications in motor drive," *CES Trans. Electr. Mach. Syst.*, vol. 3, no. 1, pp. 54–64, Mar. 2019, https://doi.org/10.30941/CESTEMS.2019.00008.
15. N. Kim, J. Yu, W. Zhang, R. Li, M. Wang, and W. T. Ng, "Current Trends in the Development of Normally-OFF GaN-on-Si Power Transistors and Power Modules: A Review," *J. Electron. Mater.*, vol. 49, no. 11, pp. 6829–6843, Nov. 2020, https://doi.org/10.1007/s11664-020-08284-7.
16. M. Meneghini, C. De Santi, I. Abid, M. Buffolo, M. Cioni, R. A. Khadar, L. Nela, N. Zagni, A, Chini, F. Medjdoub, G. Meneghesso, "GaN-based power devices: Physics, reliability, and perspectives," *J. Appl. Phys.*, vol. 130, no. 18, p. 181101, Nov. 2021, https://doi.org/10.1063/5.0061354.
17. L. Cheng, J.-Y. Yang, and W. Zheng, "Bandgap, Mobility, Dielectric Constant, and Baliga's Figure of Merit of 4H-SiC, GaN, and β-Ga_2O_3 from 300 to 620 K," *ACS Appl. Electron. Mater.*, vol. 4, no. 8, pp. 4140–4145, Aug. 2022, https://doi.org/10.1021/acsaelm.2c00766.
18. A. Lidow, M. de Rooij, J. Strydom, D. Reusch, and J. Glaser, "GaN Transistors for Efficient Power Conversion," *John Wiley Sons*, 2019.
19. A. Udabe, I. Baraia-Etxaburu, and D. G. Diez, "Gallium Nitride Power Devices: A State of the Art Review," *IEEE Access*, vol. 11, pp. 48628–48650, 2023, https://doi.org/10.1109/ACCESS.2023.3277200.
20. B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Lett.*, vol. 10, no. 10, pp. 455–457, Oct. 1989, https://doi.org/10.1109/55.43098.
21. Avnet, "Combining GaN and SiC for cost-effective power conversion | Avnet Silica." Accessed: Sep. 06, 2024. [Online]. Available: https://my.avnet.com/silica/resources/article/combining-gan-sic-for-cost-effective-power-conversion/
22. Y. Qin *et al.*, "Thermal management and packaging of wide and ultra-wide bandgap power devices: a review and perspective," *J. Phys. Appl. Phys.*, vol. 56, no. 9, p. 093001, Mar. 2023, https://doi.org/10.1088/1361-6463/acb4ff.
23. Y. Yang, L. Dorn-Gomba, R. Rodriguez, C. Mak, and A. Emadi, "Automotive Power Module Packaging: Current Status and Future Trends," *IEEE Access*, vol. 8, pp. 160126–160144, 2020, https://doi.org/10.1109/ACCESS.2020.3019775.
24. K. Wada and M. Ando, "Switching Loss Analysis of SiC-MOSFET based on Stray Inductance Scaling," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, Niigata: IEEE, May 2018, pp. 1919–1924. https://doi.org/10.23919/IPEC.2018.8507986.
25. D. N. Dalal, N. Christensen, A. B. Jørgensen, J. K. Jørgensen, S. Bęczkowski, S. Munk-Nielsen, and C. Uhrenfeldt, "Impact of Power Module Parasitic

Capacitances on Medium-Voltage SiC MOSFETs Switching Transients," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 1, pp. 298–310, Mar. 2020, https://doi.org/10.1109/JESTPE.2019.2939644.
26. S. Daryanani, "Package Innovations for SiC Power Devices," Power Electronics News. Accessed: Sep. 06, 2024. [Online]. Available: https://www.powerelectronicsnews.com/package-innovations-for-sic-power-devices/
27. M. Meisser, M. Schmenger, and T. Blank, "Parasitics in Power Electronic Modules: How parasitic inductance influences switching and how it can be minimized," presented at the PCIM Europe 2015, Nuremberg, Germany, 2015.
28. H. Ma, Y. Yang, L. Wu, Y. Wen, and Q. Li, "Review of the designs in low inductance SiC half-bridge packaging," *IET Power Electron.*, vol. 15, no. 11, pp. 989–1003, 2022, https://doi.org/10.1049/pel2.12290.
29. M. Goetz, "Silicon Nitride Substrates for Improved Performance in Power Electronics." Accessed: Sep. 06, 2024. [Online]. Available: https://eepower.com/technical-articles/silicon-nitride-substrates-for-improved-performance-in-power-electronics/
30. Y. Shi, Z. Wang, and Z. Wang, "Fine-Pitch Cu-Sn Transient-Liquid-Phase Bonding Based on Reflow and Pre-Bonding," in *2022 China Semiconductor Technology International Conference (CSTIC)*, Jun. 2022, pp. 1–3. https://doi.org/10.1109/CSTIC55103.2022.9856899.
31. L. Wang, W. Wang, R. J. E. Hueting, G. Rietveld, and J. A. Ferreira, "Review of Topside Interconnections for Wide Bandgap Power Semiconductor Packaging," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 472–490, Jan. 2023, https://doi.org/10.1109/TPEL.2022.3200469.
32. E. M. Dede, "Thermal Packaging Challenges for Next-Generation Power Electronics," presented at the Applied Power Electronics Conference, New Orleans, LA, USA, 2020.
33. R. Zhang and Y. Zhang, "Power device breakdown mechanism and characterization: review and perspective," *Jpn. J. Appl. Phys.*, vol. 62, no. SC, p. SC0806, Apr. 2023, https://doi.org/10.35848/1347-4065/acb365.
34. A. J. Wileman, S. Aslam, and S. Perinpanayagam, "A road map for reliable power electronics for more electric aircraft," *Prog. Aerosp. Sci.*, vol. 127, p. 100739, Nov. 2021, https://doi.org/10.1016/j.paerosci.2021.100739.
35. C. Chen, F. Luo, and Y. Kang, "A review of SiC power module packaging: Layout, material system and integration," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 3, pp. 170–186, Sep. 2017, https://doi.org/10.24295/CPSSTPEA.2017.00017.
36. H. Kang, A. Sharma, and J. P. Jung, "Recent Progress in Transient Liquid Phase and Wire Bonding Technologies for Power Electronics," *Metals*, vol. 10, no. 7, p. 934, Jul. 2020, https://doi.org/10.3390/met10070934.
37. F. Hou, W. Wang, L. Cao, J. Li, M. Su, T. Lin, G. Zhang, and B. Ferreira, "Review of Packaging Schemes for Power Module," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 1, pp. 223–238, Mar. 2020, https://doi.org/10.1109/JESTPE.2019.2947645.
38. R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter, and Y. Kawaguchi, "The Trench Power MOSFET—Part II: Application Specific VDMOS, LDMOS, Packaging, and Reliability," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 692–712, Mar. 2017, https://doi.org/10.1109/TED.2017.2655149.
39. N. Massey, "LFPAK88 takes a shorter path to efficiency," Nexperia. Accessed: Sep. 13, 2024. [Online]. Available: https://efficiencywins.nexperia.com/efficient-products/LFPAK88-takes-a-shorter-path-to-efficiency
40. T. Radke and N. Lakshmanan, "The Next Generation of High Power IGBT Modules," *Bodos Power Syst.*, vol. 5, pp. 42–45, 2019.
41. I. Kasko, S. E. Berberich, M. Spang, and S. Oehling, "SiC MOS Power Module in Direct Pressed Die Technology and some Challenges for Implementation," in *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Sep. 2020, pp. 364–367. https://doi.org/10.1109/ISPSD46842.2020.9170196.
42. "Semikron Danfoss, Webinar: eMPack Power Module Family – Building Scalable and Highly Effcient Traction Inverters | Semikron Danfoss." Accessed: Sep. 13, 2024. [Online]. Available: https://www.semikron-danfoss.com/about-semikron-danfoss/webinars/empack-power-module-family-building-scalable-and-highly-effcient-traction-inverters.html
43. A. P. Pai, M. Ebli, T. Simmet, A. Lis, and M. Beninger-Bina, "Characteristics of a SiC MOSFET-based Double Side Cooled High Performance Power Module for Automotive Traction Inverter Applications," in *2022 IEEE Transportation Electrification Conference & Expo (ITEC)*, Jun. 2022, pp. 831–836. https://doi.org/10.1109/ITEC53557.2022.9813878.
44. M. Liu, A. Coppola, M. Alvi, and M. Anwar, "Comprehensive Review and State of Development of Double-Sided Cooled Package Technology for Automotive Power Modules," *IEEE Open J. Power Electron.*, vol. 3, pp. 271–289, 2022, https://doi.org/10.1109/OJPEL.2022.3166684.
45. C. DiMarino, B. Mouawad, K. Li, Y. Xu, M. Johnson, D. Boroyevich, and R. Burgos, "A Wire-bond-less 10 kV SiC MOSFET Power Module with Reduced Common-mode Noise and Electric Field," presented at the PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent

Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2018, pp. 1–7.
46. F. Denk, K. Haehre, S. E. Cabrera, C. Simon, M. Heidinger, R. Kling, and W. Heering, "$R_{DS(on)}$ vs. inductance: comparison of SiC MOSFETs in 7pin D2Pak and 4pin TO-247 and their benefits for high-power MHz inverters," *IET Power Electron.*, vol. 12, no. 6, pp. 1349–1356, May 2019, https://doi.org/10.1049/iet-pel.2018.5838.
47 C. Zhao, L. Wang, F. Zhang, and F. Yang, "A Method to Balance Dynamic Current of Paralleled SiC MOSFETs With Kelvin Connection Based on Response Surface Model and Nonlinear Optimization," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2068–2079, Feb. 2021, https://doi.org/10.1109/TPEL.2020.3009008.
48. S. Wang, "Electrical Design Considerations and Packaging of Power Electronic Modules," Master Thesis, University of Arkansas, Fayetteville, AR, USA, 2013. [Online]. Available: https://scholarworks.uark.edu/cgi/viewcontent.cgi?article=1857&context=etd
49. M. Portico, "Exploring Innovation in Motion Control Technology - Industry Articles." Accessed: Sep. 13, 2024. [Online]. Available: https://eepower.com/industry-articles/driving-innovation-in-motion-control-applications/
50. M. Albayrak, K. Yamaguchi, and T. Nagahara, "„All-In-One" DIPIPM+ Series for Compact Inverter Designs," *Bodo's Power Systems*, vol. 9, pp. 30–36, 2016.
51. A. Lidow, "GaN Integrated Power Stage – Redefining Power Conversion," *Bodo's Power Systems*, vol. 5, pp. 26–27, 2020.
52. G. Tang, M. H. Kwan, Z. Zhang, J. He, J. Lei, R. Y. Su, F. W. Yao, Y. M. Lin, J. L. Yu, T. Yang, and C. H. Chern, "High-speed, high-reliability GaN power device with integrated gate driver," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2018, pp. 76–79. https://doi.org/10.1109/ISPSD.2018.8393606.
53. S. Daryanani, "The Integrated Gate Driver Approach," Power Electronics News. Accessed: Nov. 28, 2024. [Online]. Available: https://www.powerelectronicsnews.com/the-integrated-gate-driver-approach/
54. A. B. Jørgensen, "Packaging of Wide Bandgap Power Semiconductors using Simulation-based Design," Ph.d, Aalborg University, 2019. https://doi.org/10.54337/aau311246578.
55. A. B. Jørgensen, S. Beczkowski, C. Uhrenfeldt, N. H. Petersen, S. Jorgensen, and S. Munk-Nielsen, "A Fast-Switching Integrated Full-Bridge Power Module Based on GaN eHEMT Devices," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2494–2504, Mar. 2019, https://doi.org/10.1109/TPEL.2018.2845538.
56. R. Risch and J. Biela, "Low Voltage GaN-Based Gate Driver to Increase Switching Speed of Paralleled 650 V E-mode GaN HEMTs," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, Lyon, France: IEEE, Sep. 2020, p. P.1-P.11. https://doi.org/10.23919/EPE20ECCEEurope43536.2020.9215773.
57. L. Yang, K. Li, J. Dai, M. Corfield, A. Harris, K. Paciura, J. O'Brien, and C. M. Johnson, "Electrical Performance and Reliability Characterization of a SiC MOSFET Power Module With Embedded Decoupling Capacitors," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10594–10601, Dec. 2018, https://doi.org/10.1109/TPEL.2018.2809923.
58. P. Yeaman, "Powering the AI Revolution Efficiently and Cost Effectively - Technical Articles," EEPower. Accessed: Sep. 13, 2024. [Online]. Available: https://eepower.com/technical-articles/powering-generative-ai-platforms-with-tco-at-the-core/
59. Infineon Technologies, "High density dual-phase power modules| TDM22544D & TDM22545D - Infineon Technologies." Accessed: Sep. 13, 2024. [Online]. Available: https://www.infineon.com/cms/media/pss-3dmodels/dual-phase-power-module/
60. Infineon Technologies, "600 V CoolMOS™ S7 with temperature sense." Jul. 29, 2024. [Online]. Available: https://www.infineon.com/dgdl/Infineon-MOSFET_CoolMOS_600V_S7T_with_integrated_temparature_sensor-ApplicationNotes-v01_00-EN.pdf?fileId=8ac78c8c8b6555fe018bd8faa70d47ba
61. Infineon Technologies, "OptiMOS Powerstage TDA21570." Accessed: Sep. 13, 2024. [Online]. Available: https://www.infineon.com/dgdl/Infineon-TDA21570-DataSheet-v02_00-EN.pdf?fileId=5546d46279cccfdb0179e505726c7d7a&ack=t
62. STM, "STSPIN32F0: Advanced BLDC controller with embedded STM32 MCU." Mar. 2017. [Online]. Available: https://www.st.com/resource/en/datasheet/stspin32f0.pdf
63. Y. Wang, Y. Ding, and Y. Yin, "Reliability of Wide Band Gap Power Electronic Semiconductor and Packaging: A Review," *Energies*, vol. 15, no. 18, p. 6670, Sep. 2022, https://doi.org/10.3390/en15186670.
64. S. Daryanani, "Embedded PCB packaging of WBG Power Electronics," Power Electronics News. Accessed: Sep. 13, 2024. [Online]. Available: https://www.powerelectronicsnews.com/embedded-pcb-packaging-of-wbg-power-electronics/
65. S. Buschhorn, "Advanced Cooling Concept Improves Lifetime Performance – A Case Study - Technical Articles," EEPower. Accessed: Sep. 13, 2024. [Online]. Available: https://eepower.com/technical-articles/advanced-cooling-concept-improves-lifetime-performance-a-case-study/

66. I. Kovacevic-Badstubner, D. Romano, G. Antonini, J. Ekman, and U. Grossner, "Electromagnetic Modeling Approaches Towards Virtual Prototyping of WBG Power Electronics," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, Niigata: IEEE, May 2018, pp. 3588–3595. https://doi.org/10.23919/IPEC.2018.8507365.
67. Ansys, "Ansys Q3D Extractor." [Online]. Available: https://www.ansys.com/content/dam/amp/2022/may/asset-creation/q3d-extractor-datasheet/ansys-q3d-extractor-datasheet.pdf
68. I. Kovacevic-Badstuebner, R. Stark, U. Grossner, M. Guacci, and J. W. Kolar, "Parasitic Extraction Procedures for SiC Power Modules," in *CIPS 2018; 10th International Conference on Integrated Power Electronics Systems*, Mar. 2018, pp. 1–6. Accessed: Sep. 13, 2024. [Online]. Available: https://ieeexplore.ieee.org/document/8403157/?arnumber=8403157
69. S. Mazumder, M. Mandal, B. K. M, M. G, S. K. Roy, and K. Basu, "Measurement of Circuit Parasitics of a 200kW SiC based Stack," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA: IEEE, Feb. 2024, pp. 1120–1124. https://doi.org/10.1109/APEC48139.2024.10509473.
70. B. Sun, Z. Zhang, and M. A. E. Andersen, "Research of Low Inductance Loop Design in GaN HEMT Application," in *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, Washington, DC: IEEE, Oct. 2018, pp. 1466–1470. https://doi.org/10.1109/IECON.2018.8591732.
71. B. Aberg, R. S. K. Moorthy, L. Yang, W. Yu, and I. Husain, "Estimation and minimization of power loop inductance in 135 kW SiC traction inverter," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, USA: IEEE, Mar. 2018, pp. 1772–1777. https://doi.org/10.1109/APEC.2018.8341257.
72. J. Hammer, I. G. Zurbriggen, M. Ali Saket, and M. Ordonez, "Low Inductance PCB Layout for GaN Devices: Interleaving Scheme," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, USA: IEEE, Jun. 2021, pp. 1537–1542. https://doi.org/10.1109/APEC42165.2021.9487045.
73. B. Sun, K. L. Jorgensen, Z. Zhang, and M. A. E. Andersen, "Research of Power Loop Layout and Parasitic Inductance in GaN Transistor Implementation," *IEEE Trans. Ind. Appl.*, vol. 57, no. 2, pp. 1677–1687, Mar. 2021, https://doi.org/10.1109/TIA.2020.3048641.
74. X. Liu, S. Shafie, M. A. M. Radzi, N. Azis, and A. H. A. Karim, "Modelling and mitigating oscillation in E-mode GaN HEMT: A simulation-based approach to parasitic inductance optimization," *Microelectron. Reliab.*, vol. 152, p. 115293, Jan. 2024, https://doi.org/10.1016/j.microrel.2023.115293.
75. X. Geng, C. Kuring, M. Wolf, O. Hilt, J. Wurfl, and S. Dieckerhoff, "Study on the Optimization of the Common Source Inductance for GaN Transistors," in *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, Ghent, Belgium: IEEE, Sep. 2021, pp. 1–10. https://doi.org/10.23919/EPE21ECCEEurope50061.2021.9570437.
76. A. Chafi, N. Idir, A. Videt, and H. Maher, "Design Method of PCB Inductors for High-Frequency GaN Converters," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 805–814, Jan. 2021, https://doi.org/10.1109/TPEL.2020.3000438.
77. A. Letellier, M. R. Dubois, J. P. F. Trovao, and H. Maher, "Calculation of Printed Circuit Board Power-Loop Stray Inductance in GaN or High di/dt Applications," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 612–623, Jan. 2019, https://doi.org/10.1109/TPEL.2018.2826920.
78. Z. Qi, Y. Pei, L. Wang, Q. Yang, and K. Wang, "A Highly Integrated PCB Embedded GaN Full-Bridge Module With Ultralow Parasitic Inductance," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4161–4173, Apr. 2022, https://doi.org/0.1109/TPEL.2021.3128694.
79. A. B. Jorgensen, S. Beczkowski, C. Uhrenfeldt, N. H. Petersen, S. Jorgensen, and S. Munk-Nielsen, "A Fast-Switching Integrated Full-Bridge Power Module Based on GaN eHEMT Devices," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2494–2504, Mar. 2019, https://doi.org/10.1109/TPEL.2018.2845538.
80. T. Liu, T. T. Y. Wong, and Z. J. Shen, "A New Characterization Technique for Extracting Parasitic Inductances of SiC Power MOSFETs in Discrete and Module Packages Based on Two-Port S-Parameters Measurement," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9819–9833, Nov. 2018, https://doi.org/10.1109/TPEL.2017.2789240.
81. L. Pace, N. Defrance, A. Videt, N. Idir, J.-C. De Jaeger, and V. Avramovic, "Extraction of Packaged GaN Power Transistors Parasitics Using S-Parameters," *IEEE Trans. Electron Devices*, vol. 66, no. 6, pp. 2583–2588, Jun. 2019, https://doi.org/10.1109/TED.2019.2909152.
82. L. Pace, N. Idir, T. Duquesne, and J.-C. De Jaeger, "Parasitic Loop Inductances Reduction in the PCB Layout in GaN-Based Power Converters Using S-Parameters and EM Simulations," *Energies*, vol. 14, no. 5, p. 1495, Mar. 2021, https://doi.org/10.3390/en14051495.
83. W. Meng, F. Zhang, G. Dong, J. Wu, and L. Li, "Research on Losses of PCB Parasitic Capacitance for GaN-Based Full Bridge Converters," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4287–4299, Apr. 2021, https://doi.org/10.1109/TPEL.2020.3024881.

84. S. Zhao, F. Blaabjerg, and H. Wang, "An Overview of Artificial Intelligence Applications for Power Electronics," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4633–4658, Apr. 2021, https://doi.org/10.1109/TPEL.2020.3024914.
85. D.-Y. Liu, L. M. Xu, X. M. Lin, X. Wei, W. J. Yu, Y. Wang, and Z. M. Wei, "Machine learning for semiconductors," *Chip*, vol. 1, no. 4, p. 100033, Dec. 2022, https://doi.org/10.1016/j.chip.2022.100033.
86. G. Huang, J. Hu, Y. He, J. Liu, M. Ma, Z. Shen, J. Wu, Y. Xu, H. Zhang, K. Zhong, X. Ning, "Machine Learning for Electronic Design Automation: A Survey," *ACM Trans. Des. Autom. Electron. Syst.*, vol. 26, no. 5, pp. 1–46, Sep. 2021, https://doi.org/10.1145/3451179.
87. C. Yuan, S. D. M De Jong, and W. D. V. Driel, "AI-assisted Design for Reliability: Review and Perspectives," in *2024 25th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, Catania, Italy: IEEE, Apr. 2024, pp. 1–12. https://doi.org/10.1109/EuroSimE60745.2024.10491447.
88. P. Paret, D. Finegan, and S. Narumanchi, "Artificial Intelligence for Power Electronics in Electric Vehicles: Challenges and Opportunities," *J. Electron. Packag.*, vol. 145, no. 3, p. 034501, Sep. 2023, https://doi.org/10.1115/1.4056306.
89. P. V. Acharya, M. Lokanathan, A. Ouroua, R. Hebner, S. Strank, and V. Bahadur, "Assessing the impact of novel polymers and thermal management in a power electronics module using machine learning approaches," in *2021 20th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (iTherm)*, San Diego, CA, USA: IEEE, Jun. 2021, pp. 162–171. https://doi.org/10.1109/ITherm51669.2021.9503255.
90. Y. Qian, F. Hou, J. Fan, Q. Lv, X. Fan, and G. Zhang, "Design of a Fan-Out Panel-Level SiC MOSFET Power Module Using Ant Colony Optimization-Back Propagation Neural Network," *IEEE Trans. Electron Devices*, vol. 68, no. 7, pp. 3460–3467, Jul. 2021, https://doi.org/10.1109/TED.2021.3077209.
91. T. Wu, B. Ozpineci, M. Chinthavali, Z. Wang, S. Debnath, and S. Campbell, "Design and optimization of 3D printed air-cooled heat sinks based on genetic algorithms," in *2017 IEEE Transportation Electrification Conference and Expo (ITEC)*, Jun. 2017, pp. 650–655. https://doi.org/10.1109/ITEC.2017.7993346.
92. H. Fan, P. Yao, and H. Chen, "Application of AI-enabled Simulation in Power Package Development," in *2023 24th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, Graz, Austria: IEEE, Apr. 2023, pp. 1–5. https://doi.org/10.1109/EuroSimE56861.2023.10100811.
93. S.-X. Kao and C.-F. Chien, "Deep Learning-Based Positioning Error Fault Diagnosis of Wire Bonding Equipment and an Empirical Study for IC Packaging," *IEEE Trans. Semicond. Manuf.*, vol. 36, no. 4, pp. 619–628, Nov. 2023, https://doi.org/10.1109/TSM.2023.3243775.
94. X. Li, X. Zhang, F. Lin, and F. Blaabjerg, "Artificial-Intelligence-Based Design for Circuit Parameters of Power Converters," *IEEE Trans. Ind. Electron.*, vol. 69, no. 11, pp. 11144–11155, Nov. 2022, https://doi.org/10.1109/TIE.2021.3088377.
95. R. Rajamony, S. Wang, G. Calderon-Lopez, I. Ludtke, and W. Ming, "Artificial Neural Networks-Based Multi-Objective Design Methodology for Wide-Bandgap Power Electronics Converters," *IEEE Open J. Power Electron.*, vol. 3, pp. 599–610, 2022, https://doi.org/10.1109/OJPEL.2022.3204630.
96. A. J. Sellers, M. R. Hontz, R. Khanna, A. N. Lemmon, B. T. DeBoi, and A. Shahabi, "An Automated Model Tuning Procedure for Optimizing Prediction of Transient and Dispersive Behavior in Wide Bandgap Semiconductor FETs," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12252–12263, Nov. 2020, https://doi.org/10.1109/TPEL.2020.2986928.
97. A. Mehrabi, K. Yari, W. D. Van Driel, and R. H. Poelma, "AI-Driven Digital Twin for Health Monitoring of Wide Band Gap Power Semiconductors," in *2024 IEEE 10th Electronics System-Integration Technology Conference (ESTC)*, Berlin, Germany: IEEE, Sep. 2024, pp. 1–8. https://doi.org/10.1109/ESTC60143.2024.10712146.
98. "The Perfect Match – (U)WBG Semiconductors and Information Technology are Revolutionizing Power Electronics," Fraunhofer Institute for Integrated Systems and Device Technology IISB. Accessed: Nov. 28, 2024. [Online]. Available: https://www.iisb.fraunhofer.de/en/press_media/press_releases/pressearchiv/archiv_2024/pcim2024.html

Arrived: 25. 09. 2024
Accepted: 04. 12. 2024

Original scientific paper
https://doi.org/10.33180/InfMIDEM2025.102

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 55, No. 1(2025), 25 – 35

CMOS Low-Power, Fully-Programmable Gaussian/Trapezoidal Fuzzy Membership Function Generator

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Abstract: Design of a novel flexible structure for fuzzy Membership Function Generator (MFG) has been discussed in this article. The main advantage of the proposed circuits is the capability for the production of all Trapezoidal, Gaussian, S and Z shapes, simultaneously. This objective has been achieved at the first step by means of two interconnected differential pairs which generate Gaussian, S and Z shapes. Thereafter, with the help of an improved Min/Max circuit, the Trapezoidal shape with sharp edges has been constructed. The circuits are designed in a way to produce all shapes with the feature of full programmability for slope, core, and height. These features, along with small active area and low power consumption, qualify this work to be repeatedly used in Fuzzy Logic Controllers (FLCs). Post-layout simulation results for TSMC 0.18µm CMOS technology confirm the correct behavior of the designed circuits. Based on the results, the power consumption of the whole structure is 54µW from a 1.8V power supply.

Keywords: Fuzzy membership function; Fuzzy logic controller; Fuzzifier; Min/Max circuits

CMOS nizkoenergijski programabilni gausov/ trapezoidni fuzzy funkcijski generator

Izvleček: V tem članku je obravnavana zasnova nove prilagodljive strukture za fuzzy funkcijski generator (MFG). Glavna prednost predlaganih vezij je možnost hkratne izdelave vseh trapeznih, Gaussovih, S in Z oblik. Cilj je bil v prvi fazi dosežen z dvema povezanima diferencialnima paroma, ki ustvarjata Gaussovo, S in Z obliko. Nato je bila s pomočjo izboljšanega vezja Min/Max izdelana trapezoidna oblika z ostrimi robovi. Vezja so zasnovana tako, da omogočajo izdelavo vseh oblik z možnostjo popolnega programiranja naklona, jedra in višine. Te lastnosti, skupaj z majhno aktivno površino in majhno porabo energije, omogočajo, da se to delo uporabi v fuzzy logičnih krmilnikih (FLC). Rezultati simulacije po izdelavi za tehnologijo TSMC 0,18 µm CMOS potrjujejo pravilno obnašanje zasnovanih vezij. Na podlagi rezultatov je poraba energije celotne strukture 54 µW pri napajalni napetosti 1,8V.

Ključne besede: Fuzzy funkcija; Krmilnik Fuzzy logike; Min/Max tokokrogi

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1 Introduction

Analog nature of the environment around us necessitates the operation of human-made signal processing systems in the analog domain. The main reason for this purpose lies behind the fact that analog systems can capture the natural signals more suitably than their digital counterparts. Also, the digital circuits mostly need extra blocks for the digitization of those obtained signals. Hence, the analog systems are economically efficient due to their lower power consumption [1]. Moreover, based on the information obtained from the

How to cite:
S. Azizian et al., "CMOS Low-Power, Fully-Programmable Gaussian/Trapezoidal Fuzzy Membership Function Generator", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 55, No. 1(2025), pp. 25–35

literature, hardware realization for most of the fuzzy systems and neural networks has been done in the analog domain.

On the other hand, there has been intense competition between fuzzy systems and neural networks over recent years for the emulation of human brain behavior. Started by McCulloch and Pitts in 1943 for the realization of the first neuron model [2, 3], the historical background of neural systems seems to be older than Fuzzy Logic Controllers (FLCs). But since the practical realization of fuzzy logic systems at the end of the 1970s, in less than half a century, they have justified their capabilities for industrial use. Their applications cover a wide range of commercial consumer products such as cameras, rice-cookers, washing machines, and so forth [4].

The critical fact behind the population of fuzzy systems comes from the human brain translation ability for incorrect and imperfect sensory information which comes from perceptive organs [5]. It is because that the fuzzy set theory prepares a systematic computation which deals with such details linguistically. Moreover, it carries out the numerical calculations through linguistic labels arranged by membership functions [6]. Although Lukasiewicz and Tarski perused fuzzy logic as multi-valued logic in the 1920s [7], it was Lotfi A. Zadeh who announced his fuzzy set theory in 1965. It was the starting point for fuzzy systems [8].

In contrast to the standard binary sets where the variables usually pick up true or false values, in fuzzy sets, they can obtain a truth value revolving in the interval of 0 and 1 [9]. Meanwhile, for the case of utilizing linguistic variables, the degrees can be modeled by specific functions [10]. By considering these points, the general concept of an FLC will be brought up using the structure of Figure 1. As it is evident, each fuzzy system is composed of three main stages:

1) Fuzzification (membership function generation)
2) Fuzzy inference or fuzzy rule evaluation
3) Defuzzification

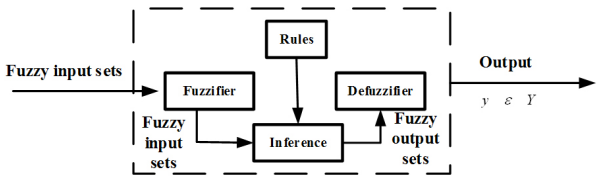


Figure 1: Structure of a Fuzzy Logic Model.

At the starting point, the fuzzification interface maps the inputs so that they can be interpreted and evaluated by the rules of the inference engine [11]. In hardware realization, the fuzzification is done by means of Membership Function Generator (MFG) circuits. The main objective of the fuzzification process is to transmute the analog input into a set of fuzzy variables. For higher accuracy, more fuzzy variables must be chosen where the outputs should be produced simultaneously [6, 12].

Because of their continuous nature and lower costs, analog Membership Function Circuits (MFCs) have drawn the attention of circuit designers over previous years. Many structures have been reported in the literature for hardware implementation of fuzzifiers in the analog domain. Depending on the purpose of the application, each structure contains different characteristics such as single or multi-variable outputs, specific waveforms, etc. In order to save power, most of the reported works can only generate one fuzzy variable at their outputs [13, 14, 15, 16, 17, 18]. The characteristic feature of these works is the function waveforms with smooth edges making them unsuitable for high-precision applications. One of the famous low-power exceptions has been introduced in [1], which has the capability of producing six fuzzy variables simultaneously. The drawback of such structure is the low resolution of the output waveforms as the drain-source voltages of the transistors are not equal in transients. Moreover, the circuit doesn't have the capability of programmability, which limits its usage in high-performance FLCs.

Piece-Wise Linear (PWL) membership functions are the waveforms with sharp edges which are used for special purpose applications. Despite higher precision, more power dissipation is expected for their generating circuits. Those circuits are designed mostly in current-mode because of the simplicity for current summation or subtraction at the connecting nodes [19, 20, 21, 22, 23]. The reported works in this criterion only produce the triangular or trapezoidal functions. The thorough analysis depicts that the problems concerning power and active area consumption have rarely been considered in most of these architectures.

One of the notable works has been presented in [21] in which by means of a simple mathematical idea an MFC has been designed using Min/Max operations. Since the circuit has been implemented in current-mode, it contains two advantages. Providing the Max and Min operations is the first privilege of this structure, while the flexibility to be configured as an MFG constitutes its second benefit. This idea can further be expanded to obtain multi-waveform membership functions.

As a conclusion, the main emphasis in this paper is to achieve the unique ability to generate all functional waveforms in a single scheme. Along with this, the programmability feature, along with low power and active area consumption, must be taken into account.

This work introduces a novel Min/Max architecture based MFG, which is implemented in current-mode using TSMC 0.18µm CMOS technology. Input voltages are used to control the slope, height, and location of waveforms. The main idea is based on the expansion of the scheme introduced in [21]. Figure 2 illustrates the initial concept, which is adapted to the differential pair based MFG so that all of the waveforms can be produced in one single architecture.

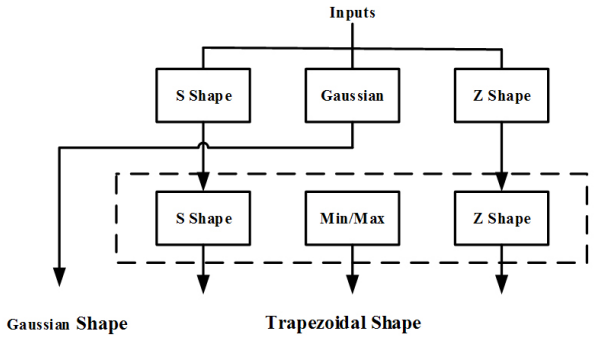


Figure 2: Structure of a Fuzzy Logic Model.

The designed circuit is composed of two parts. The first lock which is composed of a differential pair configuration generates the Gaussian, S and Z shapes simultaneously. Then, with the help of the optimized Min/Max circuit, which was initially reported in [24], the Trapezoidal/Triangular shapes with sharpened edges have been produced. It must be mentioned that the optimized Min/Max circuit can calculate the minimum of three input signals.

In Section 2, the main idea for the fuzzifier circuit is discussed, and the architecture has been demonstrated with a complete analysis. Section 3 is about the optimized Min/Max structure and its usage for customization of the output waveforms. Section 4 contains the simulation results and comparison of the designed work with previous ones. Finally, the conclusions have been summarized in Section 5.

2 Materials and methods

Fuzzification is well described by the procedure which generates a fuzzy value from an analog value of the real world. For this purpose, different classes of fuzzifiers can be employed [25]. The most important groups, utilized for the fuzzification process are:

1) Single-tone fuzzifiers
2) Gaussian fuzzifiers
3) Trapezoidal/Triangular fuzzifiers

It must be considered that the base set determines the class of representation for the membership function. For multi-valued or continuous fuzzy sets the *parametric representation* is usually suitable, and to do this, the modification of some parameters is often enough for the adjustment of the membership function. On the other hand, PWL membership functions are the most employed ones because of their computational efficiency. Trapezoidal and triangular functions constitute the central part of PWL waveforms and are distinguished by four and three parameters, respectively [5, 19, 23].

The normalized Gaussian function (which is the difference of two sigmoid waves), and the generalized bell function are also used for modeling of fuzzy sets in some special cases. In such functions, continuously differentiable curves with smooth transitions are needed where those features cannot be fulfilled by trapezoids [1, 16, 17, 26].

In General, for hardware realization of a fuzzy membership function, the following four features must be remarked [7]:

a) The *height*, as the highest membership value achieved by any element in the set.
b) The *support*, as the crisp set including all the elements of *X* with non-zero membership values.
c) The *core,* as the crisp set consisting of all the elements of *X* with the membership values of one.
d) The *boundary,* as the crisp set having all the elements of *X* with the membership values of $0 < \mu_A(x) < 1$.

The main emphasis in this work is to design a flexible architecture for achieving all of the mentioned waveforms simultaneously. Therefore, the initial idea comes from the generation of S, Z, and Gaussian functions in the first step. After that, with the help of an auxiliary circuit, the trapezoidal waves will be produced.

Therefore, the first part of the MFC will produce Gaussian, S, and Z shapes, where the initial idea has been illustrated in Figure 3. This circuit is composed of two differential pairs: the first pair consisting of M_1 and M_2 transistors, and the second pair in the right side which is constructed of M_3 and M_4 transistors. These pairs generate both S and Z shapes at their output loads.

The input voltage V_{in} is applied to M_1 and M_3 transistors at the same time. These transistors are initially in the cut-off region. Along with the increment of V_{in}, the gate-source voltages of M_1 and M_3 will grow, and they become ON. Therefore, they will produce S shape waveform at their drains while M_2 and M_4 transistors have the responsibility of generating Z shape.

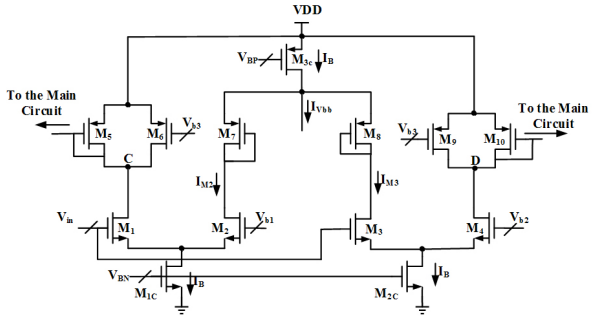


Figure 3: Initial idea for realization of the MFG.

To generate the Gaussian shape waveform, the currents of M_2 and M_3 are summed together, and the result will be subtracted from a normalized $10\mu A$ current. The current is specified as I_{Vbb} in Figure 3. These three currents will constitute three fuzzy variables.

Equations (1) and (2) illustrate the currents of M_2 and M_3, respectively [27]:

$$I_{M2} = \frac{1}{2}\left(I_B - V_1\sqrt{2kI_{ss} - k^2V_1^2} \right) \quad (1)$$

$$I_{M3} = \frac{1}{2}\left(I_B + V_2\sqrt{2kI_{ss} - k^2V_2^2} \right) \quad (2)$$

where $k = \frac{1}{2}\mu C_{ox}\frac{W}{L}$, $V_1 = V_{in} - V_{b1}$, and $V_2 = V_{in} - V_{b2}$. Moreover, I_B is the bias current which has a normalized value of $10\mu A$. Table 1 illustrates the values for I_{M2}, I_{M3}, and I_{Vbb} for different intervals of the input voltage. It is assumed that $V_{b1} < V_{b2}$.

The subtraction of V_{b1} from V_{b2} determines the width for the Gaussian shape. To explain the slope changes, let's consider the current of MOS transistor in the saturation region [27]:

$$I_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{gs} - V_{th} \right)^2 \quad (3)$$

In (3), V_{gs} and V_{th} are the gate-source and the threshold voltage of the MOS transistor, respectively. μ and C_{0x} demonstrate the process coefficients, while W and L represent the dimensions of the MOS transistor. In order to change the slop, the sizes of M_1, M_2, M_3 and M_4 must be changed to achieve the desired values. It can be done by parallel transistors of differential pair inputs in Figure 3.

Table 1: Different values of three fuzzy variables.

	IM2	IVbb	IM3
$V_{in} < V_{b1} - \sqrt{2}\Delta V$	I_B	0	0
$V_{in} = V_{b1}$	$I_B/2$	$I_B/2$	0
$Vin = (V_{b1} + V_{b2})/2)$	0	I_B	0
$Vin = _{b2}$	0	$I_B/2$	$I_B/2$

M_6 and M_9 are current sources with constant values. Their role is to sharpen the lower part of the current for M_5 and M_{10}, which is illustrated in (4):

$$I_{M5,10} = \begin{cases} I_{M1,4} - I_{M6,9} & if \quad I_{M1,4} > I_{M6,9} \\ 0 & if \quad I_{M1,4} \le I_{M6,9} \end{cases} \quad (4)$$

The current waveforms of M_5 and M_{10} are S and Z shape, respectively which are expected to have sharpened edges. These currents will be transferred to the Min/Max circuit to produce the Trapezoidal/Triangular shape. Practically, the architecture of Figure 3 has two major problems:

1) The currents of M_2 and M_3 cannot be replicated easily as their loads are not directly connected to V_{dd}.
2) The currents of M_5 and *10* M_{10} transistors are not sharp enough to generate a Trapezoid waveform with sharp edges because of the poor linear operating range of differential pairs.

In order to solve these problems, the configuration of Figure 4 has been proposed and used as the final version of Gaussian, S, and Z shape MFG. M_{7a} and M_{8a} transistors are used to replicate currents of M_2 and M_3, respectively. For equalizing all of the currents, the bias current must be doubled for upside M_{3c} transistor. So I_{Vbb} will be doubled, too and it must be considered for current mirroring.

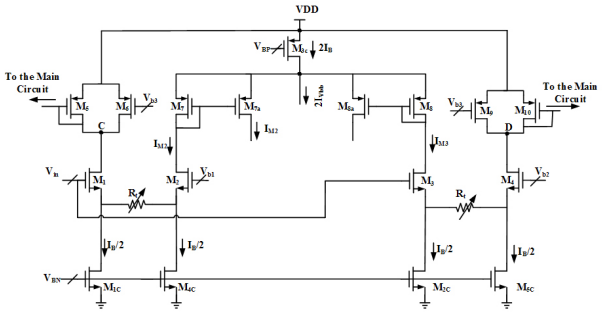


Figure 4: The proposed MFG.

The variable resistance R_t is used to increase the linearity range of differential pairs. It is implemented by means of a single transistor biased in the triode region. The current of the transistor in the triode region can be expressed as follows [27]:

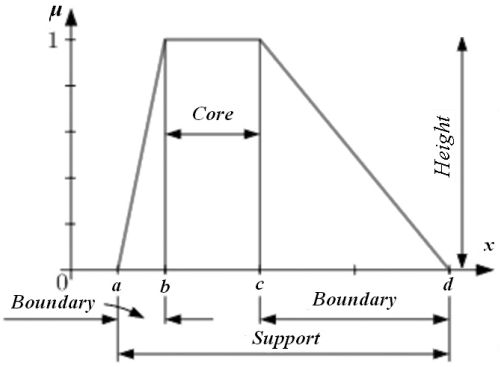
$$I_d = \mu C_{ox} \frac{W}{L}\left[\left(V_{gs} - V_{th}\right)V_{ds} - \frac{1}{2}{V_{ds}}^2\right] \quad (5)$$

V_{gs}, V_{th} and V_{ds} are the gate-source, threshold, and drain-source voltages of the MOS transistor, respectively. μ and C_{0x} represent the process coefficients while W and L denote the dimensions of the MOS transistor. If $V_{ds} \ll V_{gs} - V_{th}$, the resistance can be calculated as follows:

$$R = \frac{V_{ds}}{I_d} = \frac{L}{\mu C_{ox} W\left(V_{gs} - V_{th}\right)} \quad (6)$$

The resistance sharpens the edges of output currents I_{M5} and I_{M10}, which will be transferred to the Min/Max circuit.

(a)



(b)

$$\text{trapezoid}(x;a,b,c,d) = \begin{cases} 0 & x \le a \\ \frac{x-a}{b-a} & a \le x \le b \\ 1, & b \le x \le c \\ \frac{d-x}{d-c} & c \le x \le d \\ 0 & d \le x \end{cases}$$

Figure 5: Trapezoidal membership function (a) general waveform (b) mathematical expressions.

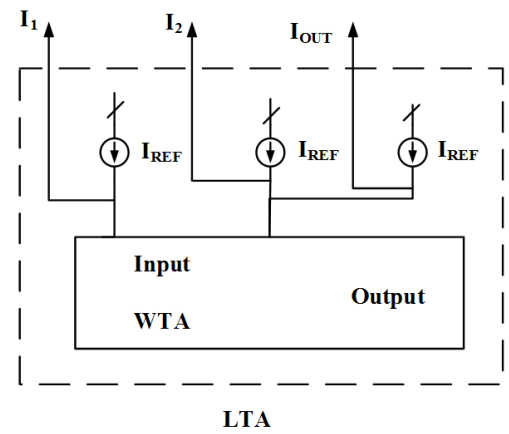
As mentioned before, the circuit of Figure 4 can only produce Gaussian, S, and Z shapes. By means of the current replicas (which perform the operations of summation and subtraction), the Trapezoid shape can be generated. However, the feature of full programmability along with good accuracy can be achieved using an additional circuit. Figure 5 demonstrates the general figure of a Trapezoidal membership function where in Figure 5(a), its four main characteristics are emphasized. Moreover, the mathematical expressions of this function are illustrated in Figure 5(b). For $b = c$, the trapezoidal shape will migrate to a triangular membership function.

In order to construct a programmable circuit, the height, core, boundary, and support must be adjustable. With a two input Min/Max circuit, at most only three of four features would be controlled. For achieving full programmability feature, a three-input Min/Max circuit is needed.

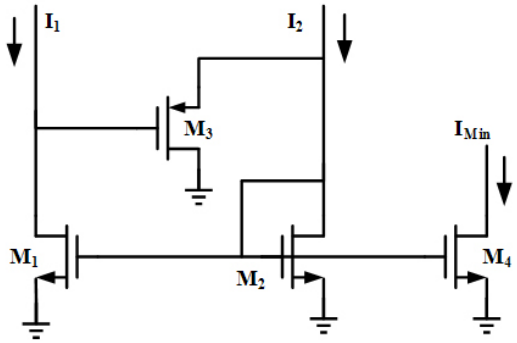
3 The optimized min/max circuit

In hardware design, the most popular fuzzy logic functions which implement logical 'AND' and 'OR' functions, are MIN and MAX operators, respectively. Therefore, they will play an essential role in the fuzzy inference engine implementation, and most of the reported works in the literature have put their basis on them.

(a)



(b)



(c)

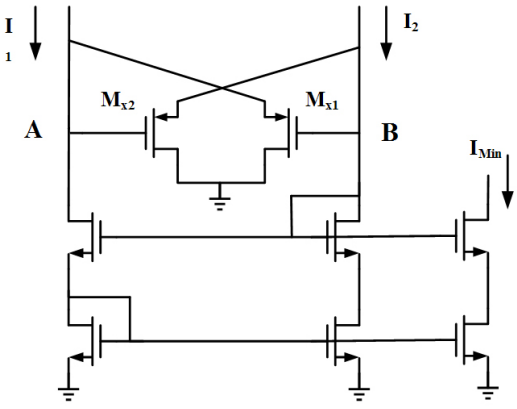


Figure 6: LTA network design by means of WTA network (a) general concept (b) Initial idea of Min circuit, (c) Structure of Min circuit proposed in [24].

One of the notable advantages of current-mode MIN and MAX circuits is that they do not necessarily need resistors in their architectures. On the other hand, the summation and subtraction of currents can simply be achieved just by wire connections. This leads to discriminating and straightforward configurations, which represent high speed and great functional density [24].

Because single fan-out is one of the drawbacks of current-mode based MIN/MAX circuits, then the current repeatability is considered as of prime importance for these structures. Also, the distribution of signals necessitates the utilization of multiple-output current mirrors. To design the MIN/MAX structure, current-mode is chosen because of the mentioned benefits, while the disadvantages are also taken into account.

After Lazzaro's work which was a novel report on Winner-Takes-All (WTA) structures (released in 1988) [28], a lot of WTA and closely related Loser-Takes-All (LTA) circuits have been proposed to realize Min/Max circuits [29, 30] (Figure 6). In some of the reported structures, the LTA function is obtained by means of WTA function. This fact is illustrated in Figure 6(a) whereby subtraction of the input values from a fixed reference current, the LTA function has been obtained. In order to explain the procedure, one can say that at the first step, one circuit performs the subtraction from a fixed current. Then, the maximum current selector behaves as the minimum current selector function. By considering the structure of Figure 6(b) as the initial idea, a newly designed structure has been reported in [24] (Figure 6(c)).

Wilson current mirror transistors are used to increase the output resistance. Also, the subtraction of currents at the input nodes enhances the accuracy of the output current.

According to Figure 6(c), If $I_1 > I_2$, then the voltage of node A rises to a high level while the voltage of node B drops down. Therefore, the gate-source voltage of M_{x1} will be increased, and this transistor will become on. On the other side, M_{x2} goes to cut off region. The extra current $I_1 - I_2$ passes through M_{x1} to the ground, which results in the reflected current in output as minimum current ($I_{min} = I_2$). The same reason holds for I_1 as the minimum current when $I_1 < I_2$.

The improved version in [31] has the extra feature of generating both maximum and minimum of input signals simultaneously. But the major problem associated with both of [24] and [31] is that they can only accept two signals as the inputs. As discussed in the previous section, for achieving the full control feature over four common characteristics of a Trapezoid waveform, at least the minimum of three input signals should be calculated. The optimized circuit with three inputs is shown in Figure 7.

The circuit is composed of two cascaded Min circuits of Figure 6(c). M_{11} and M_{12} are the input transistors. I_{M5} and I_{M10} are applied from the circuit of Figure 4 to M_{11} and M_{12}. In order to miniaturize the configuration and avoid more wiring, the second Min part is designed as the complement of the first part. The first part is the same as the circuit of Figure 6(c). At the second part, PMOS transistors are employed as the active loads (M_{19}, M_{20}, M_{21} and M_{22}). M_{25} and M_{26} are the input transistors of this part. M_{23} and M_{24} have the same role as their counterparts (M_{13} and M_{14}) in the first part of the Min circuit.

If $I_{M25} > I_{M26}$, then the gate voltage of M_{24} grows high and the gate voltage of M_{23} drops down. The extra current $I_{M25} - I_{M26}$ passes through M_{24} to V_{dd}. The result, which is the reflected current in output, gives the minimum current (I_{M26}).

The current of M_{25} can also represent the Trapezoidal/Triangular waveform. But it only controls *core*, *boundary*, and *support* of the membership function. Transistor M_{26}, which is the third input of Min circuit, is biased with a constant current to control the *height* of the Trapezoid function. Its maximum value which represents the fuzzy value of one is $10\mu A$.

The final waveform which has been obtained from cascode transistors (M_{27} and M_{28}) is the output of the fuzzifier to produce the Trapezoidal membership function. It must be mentioned that in the circuit of Figure 7 if the location of $M_{23} - M_{24}$ configuration is replaced with its counterpart $M_{13} - M_{14}$ pair, the three input Max circuit can also be obtained.

4 Simulations and comparison

4.1 Behavioral simulation

Post-Layout simulations are performed based on the TSMC 0.18µm standard process and 1.8V supply voltage by HSPICE to evaluate the correct behavior of designed fuzzifier architecture.

For the circuit of Figure 4, the simulation results of three fuzzy variables (I_{M2}, I_{Vbb}, and I_{M23}) constituting Z, Gaussian, and S shapes, respectively, are shown in Figure 8. The normalized $10\mu A$ current represents the fuzzy value of 1. For the overlapping areas, the summation of *heights* won't pass the normalized value.

To show programmability feature of the designed MFG, simulation results for different values of the sec-

ond bias voltage of differential pair V_{b2} (applied to the gate of M_4) are shown in Figure 9. The result indicates that the increment of V_{b2} stretches the *core* of Gaussian shape and turns it into Bell shape membership function, whilst the position of S shape will be relocated, too.

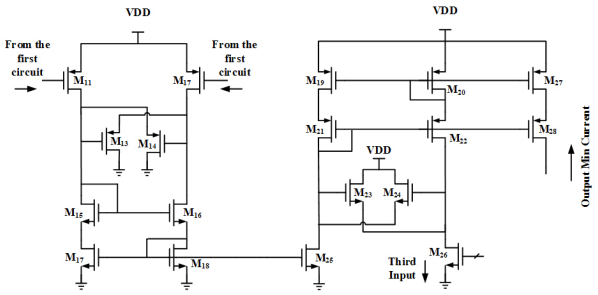


Figure 7: The optimized Min circuit.

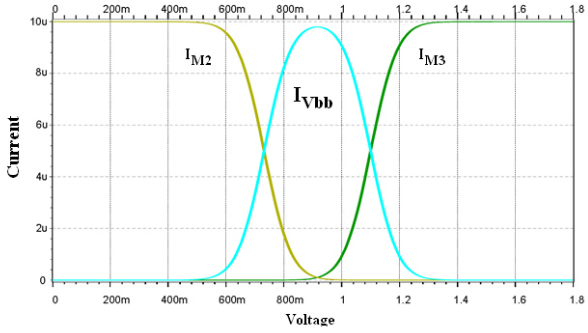


Figure 8: Simulation results for the architecture of Figure 4.

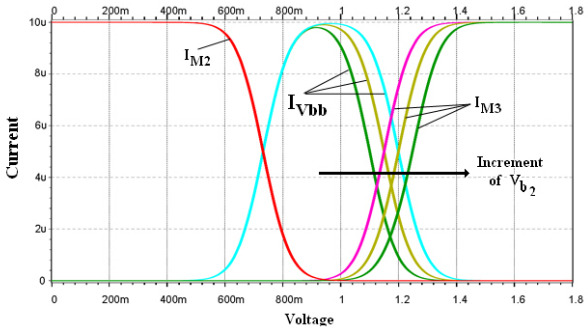


Figure 9: Core changes in the proposed MFG.

In order to investigate effect of input transistors dimensional variations on the slope changes of S, Z and Bell shapes, simulations have been done for three different values of $\frac{W}{L}$. The result which is illustrated in Figure 10 depicts that along with *core* and *support* changes, the *slope* can be regulated, too.

In order to adjust the height, the four bias currents ($\frac{I_B}{2}$) can be modified. As discussed in sections 2 and 3, I_{M5} and I_{M10} are the outputs of the first part, which constitute the inputs of Min circuit. Figure 11 shows the waveforms for these currents.

As illustrated in Figure 2, these waveforms are fed to the Min/Max circuit to produce the trapezoidal output with sharp edges.

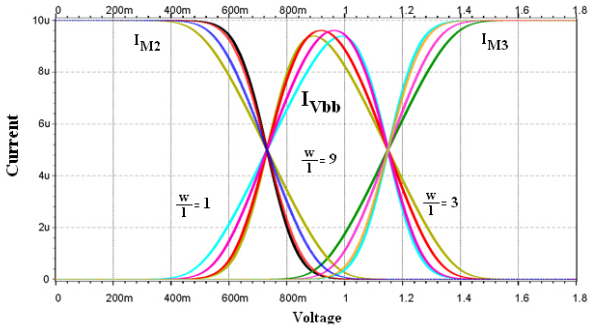


Figure 10: Slope changes of the proposed MFG for all three shapes.

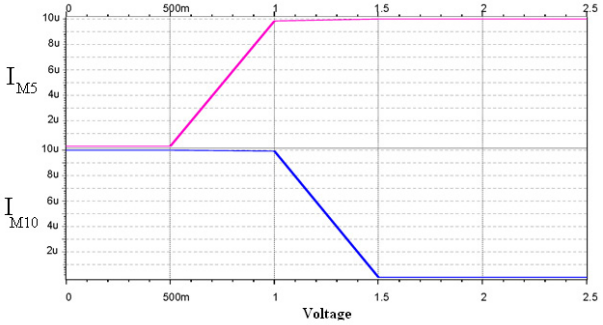
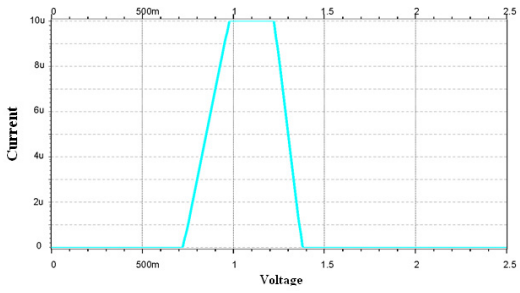


Figure 11: Waveforms of I_{M5} and I_{M10}.

(a)



(b)

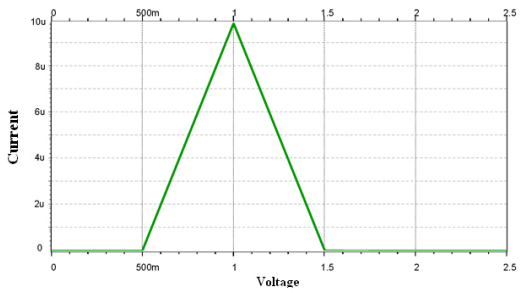


Figure 12: Simulation results for optimized Min Circuit (a) Trapezoidal shape (b) Triangular shape.

Also, Figure 12 shows the output of Min circuit, which produces the desired shapes. In Figure 12(a), the Trapezoidal waveform is illustrated, whilst by some modifications in bias voltages, the Triangular membership function can be achieved easily (Figure 12(b)).

In Figure 13, the programmability feature of Trapezoidal shape has been shown according to changes of V_{b1} and R_t. The increment of V_{b1} shifts the left side of the waveform to the higher voltages, while the changes of R_t adjusts the slope.

As the simulation results depict, full programmability of the designed structure (either for Gaussian and Trapezoid shapes) has been achieved successfully. This is a unique feature which is not reported in previous works.

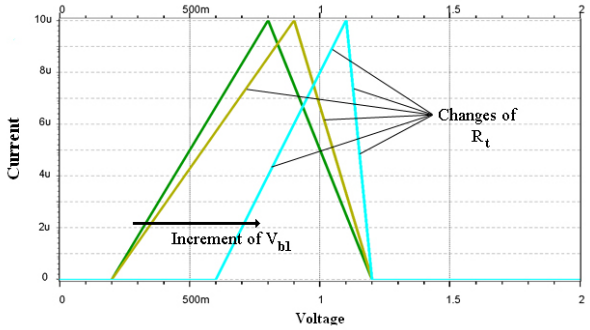


Figure 13: Simulation results for programmability of optimized Min Circuit considering Triangular shape.

The layout of the proposed work is illustrated in Figure 14, which consumes a small area of $500\mu m^2$ on-chip. In order to minimize the active area consumption, we have merged the transistors of membership function and Min/Max circuits together. Finally, Table 2 shows a comparison of this work with previous designs.

As the comparison results illustrate, the power consumption of the proposed architecture is less than the reported works. Moreover, the transistor count with the consideration of the fact the designed architecture produces all four classes of waveforms needed for fuzzy inference engine remains in a reasonable range.

It must be noted that only [1] and [15] have measurement results, and the other works have relied on simulation results. For the architecture of [18], the feature of full programmability has not been mentioned as the Trapezoidal shape has smooth edges for this work.

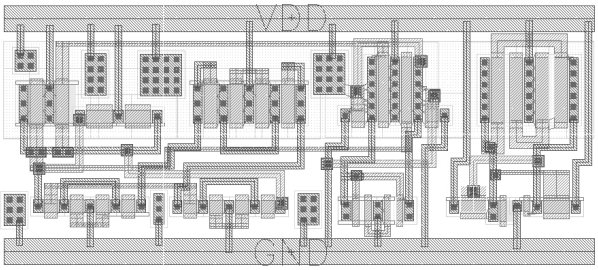


Figure 14: Layout of the proposed work.

4.2 Monte carlo simulation

At the final stage of the design performance evaluation, the Monte Carlo simulation results are provided to show the effect of process variations on the proposed structure. To achieve this, random values with Gaussian distribution were assigned to the device parameters

Table 2: Comparison of this work with previous designs.

Work	[1]	[15]	[16]	[17]	[18]	[21]	[22]	[23]	This Work
Technology (µm)	2	0.5	0.35	0.35	0.18	0.35	0.35	0.5	0.18
Supply (V)	10	3	3.3	3.3	1.8	3.3	3.3	1.5	1.8
S and Z Waves	√	×	√	×	√	×	×	×	√
Gaussian Wave	√	×	√	√	√	×	×	×	√
Trapezoid Wave	×	√	×	×	×	√	√	√	√
Slope Programmability	×	√	√	√	√	√	√	√	√
Height Programmability	×	√	√	√	√	√	√	√	√
Core Programmability	√	√	√	√	√	√	√	√	√
Transistor Count	17	28	43	23	16	48	24	61	33
Power (µW)	500	300	260	105	108	--	426	200	54
Input signal	Voltage	Voltage	Voltage	Voltage	V/I	Current	Current	Current	Voltage
Output Signal	Current	Current	Current	Current	Current	Current	Current	Current	Current
Implementation	Fab.	Fab.	Sim.	Sim.	Sim.	Sim.	Sim.	Sim.	Sim.

such as threshold voltage and size of transistors for each sample of Monte Carlo simulation.

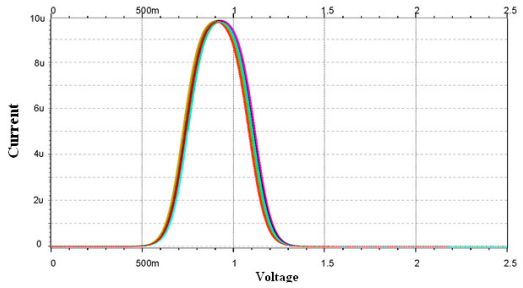
Then by running a complete simulation, a series of measurement results have been obtained. The designed circuit has been examined for 50 iterations, and the results for Gaussian and Triangular simulations are shown in Figure 15. In Figure 15(a) the results Gaussian waveform have been demonstrated while Figure 15 (b) illustrates the results for Trapezoidal shape. As the results indicate, the negative effect of process variations such as device mismatches and threshold voltage do not significantly affect the performance of the circuit.

Along with Monte Carlo analysis, the effect of temperature variations has also been considered on the current variations of the MOS transistors for performance evaluation of the designed circuits. As Figure 16 illustrates, temperature changes from 0 to 60°C do not cause any concern for the Gaussian waveform. It is because that in the configuration of Figure 4, the variable resistance behaves like a local feedback configuration and compensates the current changes related to temperature variations.

For the total power consumption of the designed architecture, one can say that the power dissipation can be calculated using the following relation:

$$P_{total} = V_{dd} \times \left(I_F + I_M \right) \tag{7}$$

(a)



(b)

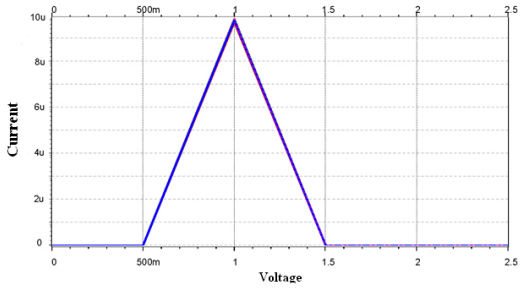


Figure 15: Monte Carlo simulation results (a) for Gaussian waveform (b) for Triangular shape.

in which I_F is the bias current-driven from M_{3c} transistor in Figure 4 and I_M is the summation of currents in

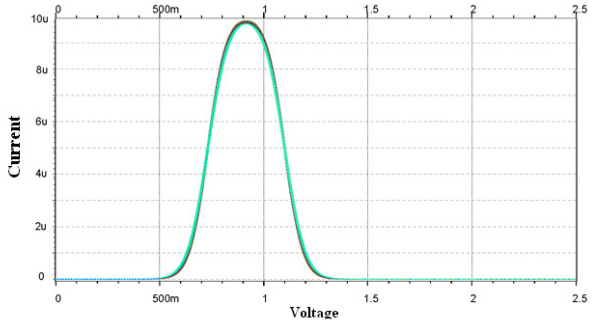


Figure 16: Temperature simulation results for Gaussian waveform.

the Min circuit of Figure 7 (driven from voltage source). Therefore, with the consideration of 1.8V as the supply voltage, $I_F = 10\mu A$, and $I_M = 20\mu A$ in the design process, the total power consumption will be equal to 54µW while the HSPICE simulation results have confirmed this value.

5 Conclusions

In this paper, a novel architecture for a fully programmable MFC is presented which produces Gaussian shape along with the Trapezoidal waveform. The improved Min/Max circuit enables us to obtain full programmability feature for Trapezoidal function, too. None of the previously published works could get both of the mentioned waveforms in a single scheme, and this is the main advantage of the designed architecture. Low power consumption and small active area are the other advantages of the designed architecture. These features, along with careful design considerations and reasonable transistor count, qualify the proposed work to be widely used in high-speed Fuzzy Logic Controllers.

Post-Layout simulation results confirm the correct behavior of the designed structure while the Monte Carlo and temperature simulation results demonstrate the low sensitivity feature of this work for process variations. The power consumption of the whole structure is 54µW from a 1.8V power supply using TSMC 0.18µm CMOS technology.

6 Conflict of Interest

The authors declare no conflict of interest. The authors also declare that there is no funding support for this work.

7 References

1. Wilamowski B. M., Jaeger R. C., Kaynak M. O., (1999) "Neuro-Fuzzy Architecture for CMOS Implementation", IEEE Transactions on Industrial Electronics, 46(6): 1132-1136, https://doi.org/10.1109/41.808001.
2. Azizian S., Fathi K., Mashoufi B., Derogarian F., (2011) "Implementation of a programmable neuron in 0.35 mm CMOS process for multi-layer ANN applications", IEEE EUROCON-International Conference on Computer as a Tool, 1-4, https://doi.org/10.1109/EUROCON.2011.5929284.
3. Azizian S., Aghchegala V. A., Azizian S., Dilmaghani M. S., (2019) "CMOS Bulk-Controlled Fully Programmable Neuron for Artificial Neural Networks", IETE Journal of Research, 65(3): 320-328, https://doi.org/10.1080/03772063.2018.1431570.

[4] Ota Y., Wilamowski B. M, (1996) "CMOS Implementation of a Voltage-Mode Fuzzy Min-Max Controller", Journal of Circuits, Systems, and Computers, 6(2): 171-184, https://doi.org/10.1142/S0218126696000145.

5. Ding L., (2001) "A new paradigm of knowledge engineering by soft computing", Singapore, River Edge, World Scientific.
6. Castillo O., (2008) "Soft computing for hybrid intelligent systems", Berlin, Springer.
7. Pelletier F. J., (2000) "Review of Metamathematics of fuzzy logics", The Bulletin of Symbolic Logic, 6 (3): 342–346, https://doi.org/10.2307/421060.
8. "Fuzzy Logic", Stanford Encyclopedia of Philosophy, Bryant University, (2006).
9. "Psychology and Mental Health: Concepts, Methodologies, Tools, and Applications (3 Volumes)", Information Resources Management Association (USA), (2016).
10. Nishant A., Gautam A., Sharma N., (2014) "Use of Logic Gates to Make Edge Avoider Robot", International Journal of Information & Computation Technology, 4(6).
11. El-Wakeel A. S., Sarhan A. A., (2014) "Step Response Enhancement of Hybrid Stepper Motors Using Soft Computing Techniques", I.J. Intelligent Systems and Applications, 06: 21-28, https://doi.org/10.5815/ijisa.2014.06.02.
12. Bishop R. H., (2007) "Mechatronic System Control, Logic, and Data Acquisition", CRC Press.
13. Conti M., Orcioni S., Turchetti C., (1998) "A Current Mode Neuro-Fuzzy Network", Proc. of 5th IEEE Int. Conf. on Electronics, Circuits and Systems, https://doi.org/10.1109/ICECS.1998.813355.
14. Ota Y., Wilamowski B. M., (1998) "Current-Mode CMOS Implementation of a Fuzzy Min-Max Network", Proceedings of World Congress on Neural Networks.
15. Kachare M., Ramírez-Angulo J., Carvajal R. G., López-Martín A. J., (2005) "New Low-Voltage Fully Programmable CMOS Triangular/Trapezoidal Function Generator Circuit", IEEE Transactions on Circuits and Systems-I: Regular Papers, 52(10): 2033-2042, https://doi.org/10.1109/TCSI.2005.853243.
16. Baradaranrezaeii A, Zarei M, Khalilzadegan A, Khoei A, Hadidi K., (2011) "An ANFIS based fuzzy controller for corner compensation", Springer Journal of Analog Integrated Circuits and Signal Processing, 72: 215–225, https://doi.org/10.1007/s10470-011-9806-3.
17. Khaneshan T. M., Nematzadeh M, Khoei A, Hadidi K., (2012) "An analog reconfigurable Gaussian-shaped membership function generator using current-mode techniques", Iranian Electrical Eng Conference, 145-149, https://doi.org/10.1109/IranianCEE.2012.6292341.
18. Yaghmourali Y. V., Fathi A., Hassanzadazar M., Khoei A., Hadidi K., (2018) "A low-power, fully programmable membership function generator using both transconductance and current modes", Fuzzy Sets and Systems, 337: 128-142, https://doi.org/10.1016/j.fss.2017.03.005.
19. Saavedra P., Lopez A., Zrilic J., Ramirez-Angulo J., (1997) "New Analog Current-Mode/Voltage-Mode Fuzzifier With Continuously Adjustable Parameters", IEEE Midwest Symposium on Circuits and Systems, https://doi.org/10.1109/MWSCAS.1997.666026.
20. Carvajal R. G., Torralba A., Colodro F., Franquelo L. G., (1999) "Mixed-Signal CMOS Fuzzifier with Emphasis in Power Consumption", IEEE Midwest Symposium on Circuits and Systems, https://doi.org/10.1109/MWSCAS.1999.867787.
21. Mesgarzadeh B., (2004) "A CMOS Implementation of Current-Mode Min-Max Circuits and A Sample Fuzzy Application", IEEE International Conference on Fuzzy Systems, 2: 941-946, https://doi.org/10.1109/FUZZY.2004.1375534.
22. Beyraghi N., Khoei A., Hadidi K., (2013) "A Current-Mode Membership Function Generator With Continuous Slop Tunability and Low Power Consumption", 21st Iranian Conference on Electrical Engineering (ICEE), https://doi.org/10.1109/IranianCEE.2013.6599652.
23. Muniz-Montero C., Sanchez-Gasparino L. A., Rocha-Perez J. M., Molinar-Solis J. E., Sanchez-Lopez C., (2013) "1.5V Fully Programmable CMOS Membership Function Generator Circuit with Proportional DC-Voltage Control", Radio Engineering, 22(2).

24. Yosefi Gh., Mirzakouchaki S., Neda Sh., (2009) "Design of New CMOS Current Mode Min and Max Circuits for FLC ChipApplications", European Conference on Circuit Theory and Design (ECCTD), 89 – 92, https://doi.org/10.1109/ECCTD.2009.5274973.
25. Tiwari S., Khemariya M., Singh A., (2013) "Comparative Analysis of PI, PID and Fuzzy Logic Controller Based Relay for Power System Protection", International Journal of Electrical, Electronics and Computer Engineering, 2(1): 48 – 51.
26. Bijar A, Khayati R, and Peñalver Benavent A, (2013) "Increasing the Contrast of the Brain MR FLAIR Images Using Fuzzy Membership Functions and Structural Similarity Indices in Order to Segment MS Lesions", PLoS ONE, 8(6): e65469, https://doi.org/10.1371/journal.pone.0065469.
27. Fathi A., Azizian S., Sharifan N., (2016) "Sensors and amplifiers: Sensor output signal amplification systems," in Handbook of Research on Nanoelectronic Sensor Modeling and Applications. Pennsylvania: IGI Global Publishing, 423–504, https://doi.org/10.4018/978-1-5225-0736-9.ch016.
28. Lazzaro J., Ryckebusch S., Mahowald M. A., Mead C. A., (1989) "Winner take-all networks of O(n) complexity", Advances in neural information processing system, 1, D. S. Touretsky, Ed. Los Altos, CA: Morgan Kaufman, 703-711.
29. Huang C.-Y., Liu B.-D., (1994) "Current-mode multiple input maximum circuit for fuzzy logic controllers", Electronics Letters, 30(23): 1924–1925, https://doi.org/10.1049/EL%3A19941342.
30. Donckers N., Dualibe C., Verleysen M., (2000) "A Current-Mode CMOS Loser-Take-All with Minimum Function for Neural Computations", Proceedings of The IEEE International Symposium on Circuits and Systems (ISCAS), 415-418, https://doi.org/10.1109/ISCAS.2000.857119.
31. Alikhani A., Ahmadi A., (2012) "A novel current-mode min–max circuit", Springer Journal of Analog Integrated Circuits and Signal Processing, 72: 343–350, https://doi.org/10.1007/s10470-012-9867-y.

Arrived: 12.12. 2023
Accepted: 24. 05. 2024

Original scientific paper
https://doi.org/10.33180/InfMIDEM2025.103

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
Vol. 55, No. 1(2025), 37 – 45

Efficient Resource Allocation for Ultra Reliable Low Latency Communication Delay Minimization in Fifth Generation Networks

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Abstract: In Modern world, Fifth Generation (5G) technology is ubiquitous, so it is necessary to meet all of its service requirements. Hence, resource allocation for every service is very important. This research addresses the problem of resource allocation for both Enhanced Mobile Broadband (eMBB) and Ultra Reliable Low Latency Communication (URLLC) users. The work comprises both static and dynamic resource allocation for eMBB and URLLC users. This research aims to minimize latency for URLLC users by taking into account the time and energy constraints of both eMBB and URLLC in static resource allocation, formulating these constraints as a convex optimisation problem. The results show that the static resource allocation strategy performs better than the fixed bandwidth and Central Processing Unit (CPU) cycle schemes. However, the use of static resource allocation becomes inefficient as the number of users increases. We propose a dynamic resource allocation strategy to address this issue, which uses online conformal prediction to schedule URLLC traffic on top of eMBB. The dynamic resource allocation strategy outperforms all previous resource allocation methods, ensuring 67% eMBB efficiency and 1 millisecond latency for URLLC users.

Keywords: 5G; eMBB; URLLC; Conformal Prediction; Resource Allocation

Učinkovita dodelitev virov za izjemno zanesljivo komunikacijo z nizkimi zakasnitvami za zmanjšanje zakasnitev v omrežjih pete generacije

Izvleček: V sodobnem svetu je tehnologija pete generacije (5G) prisotna povsod, zato je treba izpolniti vse zahteve glede storitev. Zelo pomembno je dodeljevanje virov za vsako storitev. Raziskava obravnava problem dodeljevanja virov za uporabnike izboljšanega mobilnega širokopasovnega omrežja (eMBB) in ultra zanesljivega komuniciranja z nizko zakasnitvijo (URLLC). Delo vključuje statično in dinamično dodeljevanje virov za uporabnike eMBB in URLLC. Cilj te raziskave je čim bolj zmanjšati zakasnitve za uporabnike URLLC z upoštevanjem časovnih in energetskih omejitev eMBB in URLLC pri statičnem dodeljevanju virov, pri čemer se te omejitve oblikujejo kot konveksni optimizacijski problem. Rezultati kažejo, da je strategija statičnega dodeljevanja virov boljša kot sheme s fiksno pasovno širino in cikli centralne procesne enote (CPU). Vendar, ko se poveča število uporabnikov, postane uporaba statičnega dodeljevanja virov neučinkovita. Predlagamo dinamično strategijo dodeljevanja virov za reševanje tega vprašanja, ki uporablja spletno konformno napovedovanje za načrtovanje prometa URLLC na vrhu eMBB. Dinamična strategija dodeljevanja virov je boljša od vseh prejšnjih metod dodeljevanja virov in zagotavlja 67-odstotno učinkovitost eMBB ter milisekundno zakasnitev za uporabnike URLLC.

Ključne besede: 5G; eMBB; URLLC; konformno napovedovanje; dodeljevanje virov

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How to cite:
P. Ramesh et al., "Efficient Resource Allocation for Ultra Reliable Low Latency Communication Delay Minimization in Fifth Generation Networks", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 55, No. 1(2025), pp. 37–45

1 Introduction

The need for high-speed internet in the modern world increases rapidly as automotive industries, augmented reality, and Internet of Things (IoT) based automation provide real-time data for processing, and the world is moving towards a greener future. Therefore, we need to reduce the energy consumption of cyber physical devices and base stations. The above requirements are satisfied by the Fifth Generation (5G) [1]. It offers a 20-G bit/s data rate, which is 20 times faster than Fourth Generation (4G). It can offer an ultra-low latency of 1 ms [2]. It has massive capacity so that it can connect billions of devices, enabling smart cities, connected homes, and the revolution in automobiles through vehicle-to-vehicle (V2V) communication [3]. It offers three services, namely massive machine-type communication (mMTC), enhanced mobile broadband (eMBB), and ultra-reliable low-latency communication (URLLC) [4]. URLLC devices require low latency (<1 ms), high reliability (99%), and moderate data rates. eMBB devices require ultra-high data rates, low energy, and high capacity. mMTC requires massive connectivity, extended battery life, and low data rates. The eMBB and URLLC are critical for day-to-day applications. Hence, this research focuses on the requirements of eMBB and URLLC.

Resource to the huge network traffic and computational resource requirements, resource allocation is crucial for all 5G services. The resource allocation ensures that bandwidth, power, energy, and Central Processing Unit (CPU) cycles are used optimally based on the user needs. The resource allocation strategy ensures spectral efficiency, as well as a reduction in latency and energy consumption.

In current technology, 5G uses dynamic spectrum sharing to allow for flexible allocation of frequency spectrum based on real-time needs. We use spectrum management algorithms for dynamic resource allocation to prevent interference. However, this strategy lacks the URLLC reliability constraint and eMBB efficiency, which gives scope for research.

The goal of this research is to address the reliability and efficiency of URLLC and eMBB, propose a static resource allocation strategy for a limited number of users and a dynamic resource allocation strategy to efficiently use the available bandwidth, computational capacity, and power, and develop an efficient scheduler based on conformal prediction to dynamically allocate resources to both eMBB and URLLC services, satisfying their Quality of Service (QoS) requirements.

The structure of the paper is outlined below: Section II describes the purpose of the literature survey of various research perspectives in relation to the research. Section III describes the proposed methodology and scenario for the research. Section IV presents the results and offers insights gleaned from them. Finally, Section V concludes with future work on the research.

2 Literature survey

In [5], the authors proposed a downlink scheduler to regulate URLLC traffic and eMBB traffic using superposition techniques that share resources related to frequency and power. They made an optimization problem to make sure that the rate loss for eMBB users and the segmentation loss of URLLC packets were kept to a minimum while still meeting their QoS requirements. The considered problem is solved by decomposing into two sub-problems: one for finding the optimal resource and power allocation for each eMBB-URLLC pair, and another for finding an optimal pairing policy that uses a greedy algorithm.

In [6], the authors developed a mechanism to maximize the efficiency of eMBB User Equipment (UE) and address the latency specifications of URLLC users. They have developed a dynamic, programmable approach to satisfy the above requirements. When a URLLC packet arrives, the algorithm uses puncturing mechanisms to stop the ongoing eMBB traffic.

The author in [7] addressed the issues related to URLLC and eMBB. The authors have developed mechanisms to address energy consumption and resource allocation between eMBB and URLLC. The authors divide a major problem into several minor problems, then transform them into convex functions that run in a loop until they converge. To implement it, the authors have adapted the Block Coordinate Descent (BCD) algorithm.

In [8], the authors used particle swap optimization and graph allocation-based algorithms to minimize interference. These mechanisms did not compromise data rates or throughput. They also used the TOPSIS technique to order the user preferences.

In [9], authors used the concept of network slicing to allocate resources to eMBB and URLLC within a 5G Cloud Random Access Networks (CRAN). The authors solved the allocation problem using mixed-integer nonlinear programming. They defined the separation between eMBB and URLLC services. They also introduced randomness to their traffic load. The authors have considered transmitting data packets of small size to ensure the characteristics of URLLC, which are low response

time and high reliability. Further, they have used successive convex approximation algorithms to provide solutions to the framed problem statements.

In [10], the authors focused on higher-order layers and provided solutions to avoid Packet Duplication (PD). The authors also presented techniques to enhance the performance of URLLC. The authors provided an optimization problem based on URLLC constraints and solved it as a heuristic function so that the asset configuration can be in terms of Modulation Coding Scheme (MCS) and Physical Resource Block (PRB) reservation over many links. The final outputs indicate that the implementation of PD in the different network scenarios provides efficient usage of radio resources.

The above literature reveals that the authors scheduled the time slots for the URLLC data based on previous URLLC traffic data, resulting in a system reliability of less than 90%. The authors have also overlooked the crucial factor of high eMBB efficiency. The traffic to URLLC varies with time. This is due to the dynamic nature of URLLC devices. URLLC devices have a minimal delay tolerance, and timeouts result in the loss of some generated packets. Hence, it is necessary to design a scheduler that takes care of the delay tolerance capability of URLLC devices. In this work, we design the scheduler to guarantee a reliability of more than 90% for URLLC devices, while also ensuring eMBB efficiency through both static and dynamic scheduling. Using a conformal prediction-based scheduler, URLLC's reliability is increasing.

3 Proposed methodology

This section describes the suggested model flow for the static resource allocation system model. It is followed by the formulation of constraints and the dynamic resource allocation network scenario, as well as the naive scheduler and the Conformal Prediction (CP)-based scheduler [11].

3.1 System model

A network setup of 10 users is considered, as well as a mobile edge computing offloading scenario is shown in the Figure 1. Two types of 5G services are considered here, namely eMBB and URLLC, and each user will fall under one of the two categories. There are two sets of users here: one is URLLC users with a total number of 5 users, and another is eMBB users with a total number of 5 users again. The primary goal of URLLC users is to achieve the lowest possible delays. The delay includes the time required for transmitting data to the edge cloud, analysing, evaluating, and downloading the solutions to each of the URLLC UEs; this should be executed with an acceptable level of power consumption constraint, and in the case of eMBB users, the throughput and capacity are of the utmost importance. We built a single antenna within the network setup to serve as a gateway to the edge cloud, allowing users to offload. In addition to power and latency constraints [12], computation capacity and bandwidth constraints are also considered.

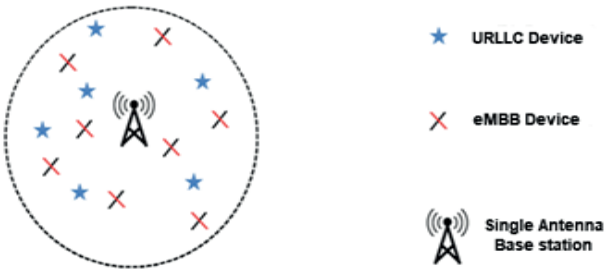

Figure 1: System model for static resource allocation

Constraint of computation capacity, with C_i being the computation capacity allotted to ith user [13]

$$\sum_{i=1}^{10} C_i \leq C \tag{1}$$

and for bandwidth, consider a total of i sub-channels, where BW_i is the bandwidth allotted to the i[th] sub-channel.

$$\sum_{i=1}^{I} BW_i \leq BW \tag{2}$$

And for Transmission Power

$$0 < PW_i < PW_{max_i} \; \forall \, i \in I \tag{3}$$

3.1.1 URLLC data packets estimation

In this research, we have run simulations for a total of 2000 frames, and for each frame f within that range, a total of $P_f \leq A$. URLLC data packets will be generated. The n[th] generated packet can be denoted as $P_f[n] \in A$ slot within the frame. Basically, we implement the process based on two assumptions

Along with the computation capacity, bandwidth, and transmission power constraints, a total of seven constraints are formulated [14]:

$$t_x \leq T_x = \frac{N_x}{BW_x \log 2\left(1 + \frac{pw_x g_x}{BW_x N_0}\right)} + \frac{CP_x N_x}{C_x} \leq T_x \;, t_x \geq 0 \; \forall \, x \in X \tag{4}$$

$$t_e \le T_e = \frac{N_e}{BW_e \log 2\left(1+\frac{pw_e g_e}{BW_e N_0}\right)} + \frac{CP_e N_e}{C_e} \le T_x \ , t_x \ge 0 \forall e \in E \quad (5)$$

$$t_x \le T_x = \frac{N_x}{BW_x \log 2\left(1+\frac{pw_x g_x}{BW_x N_0}\right)} + \frac{CP_x N_x}{C_x} \le T_x \ \ , t_x \ge 0 \forall x \in X \quad (6)$$

$$E_{off.e} \le E_e = \frac{pw_e N_e}{BW_e \log 2\left(1+\frac{pw_e g_e}{BW_e N_0}\right)} \le \le E_e \ , E_{off.e} \ge 0 \forall x \in E \quad (7)$$

Equations (4) and (5) represent delay constraints for both URLLC and eMBB users, while equations (6) and (7) represent energy constraints.

For URLLC [15] users, the delay constraint is crucial, and for eMBB users, the energy constraint ensures a limit in energy consumption, and vice versa. We solve these constraints as convex optimization problems to determine the optimal delay and energy consumption for each user.

3.2 Dynamic resource allocation network scenario

Frame-based communication is discussed here, and each frame contains both eMBB and URLLC data packets as shown in the Figure 2. Moreover, we divide each frame into 12 slots, each lasting 0.5 ms. The scheduler at the base station generates either an eMBB or URLLC data packet for a specific slot, stores and displays this information as set A. Every time a new frame begins, the base station's scheduler defines each slot by assigning it to one of the users, and records this information in a set $D_f \subset \mathrm{A}$.

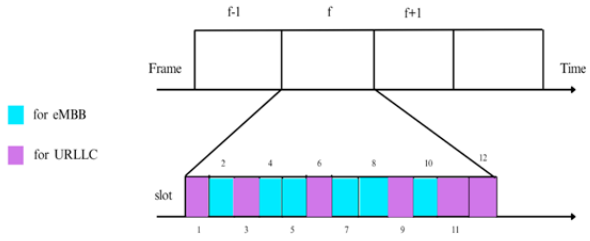

Figure 2: Network scenario of dynamic resource allocation

3.2.1 URLLC data packets estimation

In this research, we have run simulations for a total of 2000 frames, and for each frame f within that range, a total of $P_f \le A$. URLLC data packets will be generated. The n[th] generated packet can be denoted as $P_f[n] \in A$ slot within the frame. Basically, we implement the process based on two assumptions: first, that the number of URLLC data packets generated within a single slot will not exceed one. Another thing is that the total number of data packets generated will not exceed the number of slots.

We note the slots allocated for the URLLC data packets and add them to a new set defined as in the equation 8,

$$p_f = \left\{ p_f[1], \ldots . p_f\left[p_f\right] \right\} \subseteq A \quad (8)$$

3.2.2 Latency and reliability constraints associated with URLLC user

Here, we express the latency as two slots, imposing a latency threshold of 1 ms. We set the threshold for reliability to be 90 percent by defining the unreliability rate alpha at 0.1. Frame f's reliability measure can be defined as in the equation 9 [16].

$$r\left(d_f | p_f\right) = \begin{cases} 1, \ if \ d_f \ L-Covers \ p_f \\ 0, \ otherwise \end{cases} \quad (9)$$

This is for a single frame and for the total of F frames,

$$RU\left(d1:F | p1:F\right) = \frac{1}{F}\sum_{f=1}^{F} r\left(d_f | p_f\right) \quad (10)$$

3.2.3 eMBB efficiency

We can mathematically express the eMBB efficiency [17] in equation 11 as the ratio of the number of slots allocated for the eMBB users to the total number of slots within a given frame window:

$$\eta_{eMBB}\left(d_{1:E}\right) = \frac{1}{F}\sum_{f=1}^{F}\frac{A-\left|d_f\right|}{A} = 1 - \frac{1}{FA}\sum_{f=1}^{F}\left|d_f\right| \quad (11)$$

3.3 Naive prediction based scheduler

The conventional scheduler [15] is shown in the Figure 3, and its output entirely depends on the predictor that the base station has adapted.

We use the Naive Scheduler to minimize the U_f of assigned slots, ensuring that the sum of possibilities $q_f(h)$ across all intervals h that are L-covered by d_f is no smaller than $1 - \varphi$. To address this issue, we use a two-step heuristic approach in equation 13.

Figure 3: Naive prediction-based scheduler

Initially, we identify the smallest set φ of slot birth patterns hf to which the predictor $q_f(.)$ assigns a probability of at least $1 - \varphi$

$$\Gamma\left(\frac{\alpha}{\mathrm{qf}}\right) = argmin_{\Gamma\in 2^s} \left|\Gamma\right| \sum_{P\in\Gamma} q_f \text{ (h)} \geq 1 - \varphi \qquad (13)$$

The scheduler first finds the subset $\varphi(\alpha/q_f)$, then identifies an assignment df that guarantees maximum reliability and eMBB efficiency.

3.4 CP Based scheduler

A conformal-based scheduler will output prediction intervals is shown in the Figure 4. Based on the confidence value and interval obtained from the conformal prediction, it is useful for the users to understand the nature of the input given and analyse the data efficiently. The online conformal prediction works initially with a smaller number of datasets, but as time progresses, the test data, i.e., the generated URLLC packets on successful transfer, will also become the trained dataset, and the model will get stronger as the dataset increases. We use the cumulative distribution function to calculate reliability constraints. The slot allocation will be made based on reliability. We will allocate the URLLC packet with high resource requirements and high reliability first, and then schedule the subsequent packets. Gamma indicates whether the URLLC packet reached its destination. We transform the beta using the stretching function to update our online conformal prediction model using the stretching function μ.

Figure 4: CP based scheduler

The equation 14 gives the CP-based traffic predictor's stretching function. The predictor uses stretching functions and learning rates to optimize the online CP algorithm and predict URLLC traffic.

$$\mu(\beta) = \frac{1}{2}\left(1 + \cos\left(\pi\left(max\left\{0, \min\left(1, \beta\right)\right\} - 0.5\right)\right)\right) \qquad (14)$$

4 Results and discussion

4.1 Simulation parameters

This section delves into the simulation outcomes and provides a comprehensive discussion on the implications of these results. We conducted the simulations under various sets of parameters, each tailored to explore specific aspects of the system under study. Following this, we detail the performance metrics derived from these simulations, offering a comprehensive assessment of the system's behavior and efficacy under various conditions. Table 1 depicts the parameters for the static resource allocation.

Table 1: Simulation parameters for static and dynamic resource allocation

	Parameters	Value
Static Resource Allocation Parameters	Bandwidth	1 MHz
	Capacity	10 bit/s
	Power Spectral Density	-174 dB/Hz
	Input Data	50 K bits
	Total CPU Cycles	100
	Maximum Power of each user	0.5 Watts
	Radius	500 meters
	Number of users	10
Dynamic Resource Allocation Parameters	b_mismatch	0,1
	h_case	0,1
	b_adaptive	0,1
	p_plus pop	0.16
	p_plus hat	0.16
	G_num_min_pop	0

4.2 Performance Analysis

The suggested optimization beats the constant CPU frequency strategy by 10% and the fixed bandwidth method by 72%, as shown in Figure 5. In order to achieve the lowest feasible latency without sacrificing time limitations for the eMBB customers, it increases CPU computation capacity and bandwidth for the URLLC users.

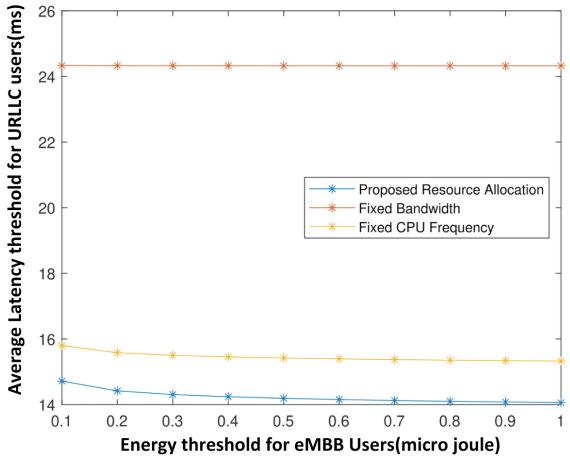

Figure 5: Average latency threshold for URLLC user vs energy threshold

According to Figure 6, the proposed optimization performs significantly better than the fixed bandwidth scheme (by 71%) and the fixed CPU frequency scheme (16%). By increasing CPU capacity and bandwidth, it ensures optimal latency for URLLC users while also addressing the needs of eMBB users.

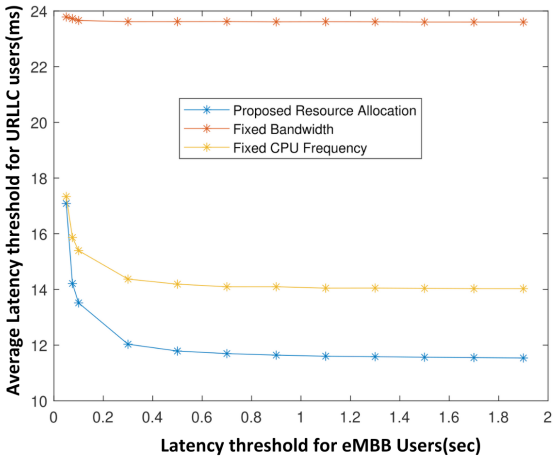

Figure 6: Average latency threshold for URLLC user vs energy threshold for URLLC users

As shown in Figure 7, the proposed optimization significantly outperforms the fixed bandwidth and fixed CPU frequency approaches. The proposed optimization has a 17% decrease in delay when compared to a fixed CPU frequency and an 87% decrease in delay in comparison with the fixed bandwidth scheme.

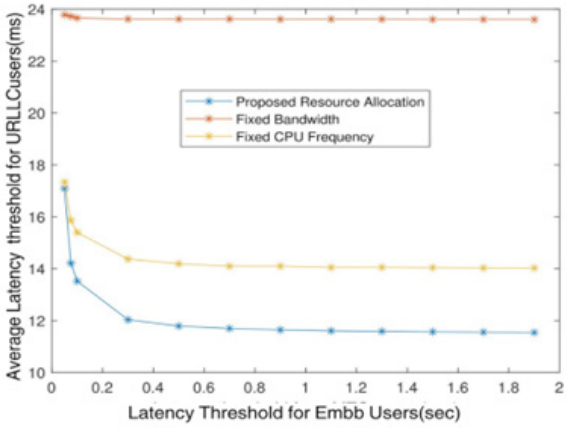

Figure 7: Average latency threshold for URLLC user vs latency threshold for eMBB users

As expected, as the number of devices increases, the delay also increases due to the increased complexity, as illustrated in Figure 8. The proposed optimization has reduced the latency by 4% compared to a fixed CPU capacity and by 45% compared to a fixed bandwidth.

The suggested optimization outperforms the fixed bandwidth and fixed CPU frequency methods, as seen in Figure 9. It exhibits superior performance compared to the fixed allocated Multi Access Edge Computing (MEC) capacity and fixed bandwidth schemes, leading to a reduction in latency of 16% and 90%, respectively.

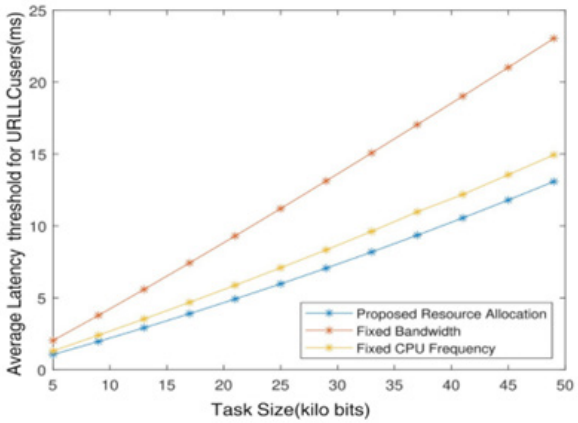

Figure 8: Average latency threshold for URLLC users vs. task size

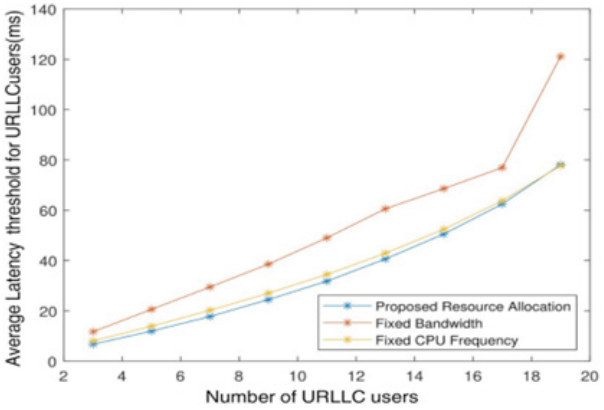

Figure 9: Average latency threshold for URLLC user vs number of URLLC Users

The contour plot illustrates the comparison of resource allocation between the conventional scheduler and the CP-based scheduler [18] as shown in the Figure 10. The contour plot illustrates the comparison of resource allocation between the conventional scheduler and the CP-based scheduler. The first column in the contour represents URLLC traffic generated, which has pink-coloured slots, and eMBB traffic, which has blue-coloured slots. When the predictor underestimates URLLC traffic, the second and third columns represent comparisons between conventional schedulers and CP-based schedulers. According to equation 10, the average frame success ratio for predicting URLLC traffic in the conventional scheduler in figure 2 is 83 percent, whereas it is 93 percent in the CP-based scheduler. The fourth and fifth columns are the comparisons between conventional schedulers and CP-based schedulers. When the predictor overestimates URLLC traffic, the average frame success ratio for conventional schedulers is 90 percent, and CP-based schedulers is 92 percent based on equation 10. In both cases, the CP-based scheduler achieves URLLC reliability of more than 90 percent. This makes it perfect for forecasting URLLC traffic.

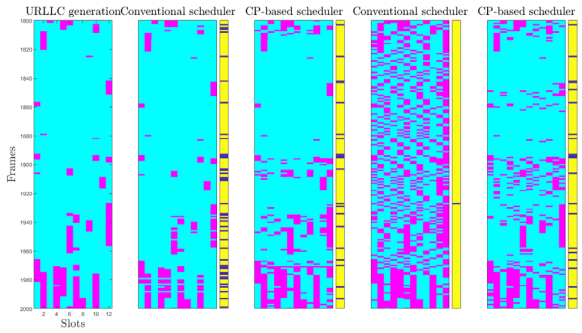

Figure 10: CP-based scheduler output

4.3 Performance metrics

4.3.1 Efficiency

When the mismatch factor is zero, Figure 11 illustrates the relationship between the number of delayed slots and efficiency. It demonstrates that as the number of slots rises, the efficiency steadily rises until it reaches 0.70, at which point it stabilizes.

When the mismatch factor is one, Figure 12 illustrates the relationship between the number of delayed slots and efficiency. It demonstrates that as the number of slots rises, the efficiency consistently rises until it reaches 0.75, at which point it stabilizes.

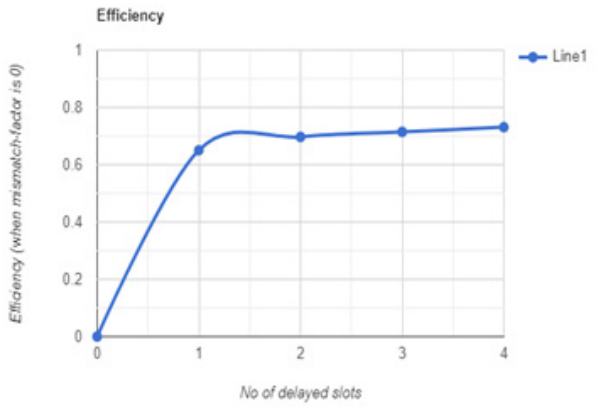

Figure 11: Efficiency (mismatch factor is 0)

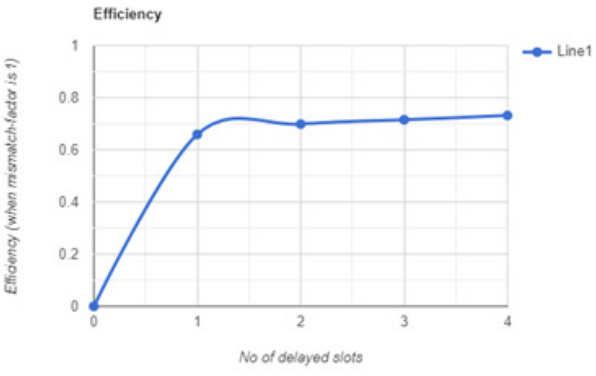

Figure 12: Efficiency (mismatch factor is 1)

4.3.2 Coverage reliability

When the mismatch factor is zero, Table 2 displays the coverage reliability of a normal scheduler and a CP-based scheduler. From the table, we infer that the coverage reliability is independent of the number of delayed slots because it is almost constant for all the delayed slots, and the coverage reliability of the CP-based scheduler is slightly greater than that of the normal scheduler.

Table 2: Coverage reliability-when mismatch factor 0

Number of delayed slots	Coverage Reliability of normal scheduler	Coverage reliability of CP- based scheduler
1	0.8185	0.8990
2	0.8186	0.8993
3	0.8188	0.8995
4	0.8189	0.8998
5	0.8191	0.8999

When there is a mismatch factor 1, Table 3 shows the coverage reliability of a normal scheduler and a CP-based scheduler. From the table, we infer that the coverage reliability is independent of the number of delayed slots because it is almost constant for all the delayed slots, and the coverage reliability of the CP-based scheduler is slightly greater than that of the normal scheduler.

Table 3: Coverage reliability-when mismatch factor 1

Number of Delayed Slots	Coverage Reliability of Normal Scheduler	Coverage Reliability of CP- Based Scheduler
1	0.9855	0.9525
2	0.9856	0.9535
3	0.9856	0.9555
4	0.9858	0.9575
5	0.9859	0.9585

5 Conclusions

The proposed work creates a framework for static resource allocation for a limited number of users and a dynamic resource allocation for a larger number of users. The proposed static resource allocation strategy has outperformed the fixed bandwidth and fixed frequency resource allocation strategies. The parameters such as efficiency, Reliability of the users has been carried out to monitor the performance of it and with respect to mismatch values. The proposed dynamic resource allocation strategy achieves an eMBB efficiency of 70% and URLLC reliability of 90%.

6 Acknowledgments

The authors are grateful to the Centre for Internet of Things (CIoT), Madras Institute of Technology Campus, Anna University, for providing the resources needed to complete the research.

7 Conflict of interest

The authors declare that there is no conflict of interest.

8 References

1. P. Ramesh and P. T. V. Bhuvaneswari, "Non Orthogonal Multiple Access Requirements for 5G and Its Myths," 2022 IEEE Delhi Section Conference (DELCON), 2022, pp. 1-6, https://doi.org/10.1109/DELCON54057.2022.9752790.
2. M. Alsenwi, S. R. Pandey, Y. K. Tun, K. T. Kim, and C. S. Hong,``A chance constrained based formulation for dynamic multiplexing of eMBB-URLLC traffics in 5G new radio," in Proc. Int. Conf. Inf. Netw. (ICOIN), Kuala Lumpur, Malaysia, Jan. 2019, pp.
3. M. Kokilavani, R. Siddharth, S. Mohamed Riyaz, P. Ramesh, S. Ezhilarasi and P. T. V. Bhuvaneswari, "Downlink Performance Analysis of 5G PD-NOMA System," 2022 IEEE Global Conference on Computing, Power and Communication Technologies (GlobConPT), 2022, pp. 1-6, https://doi.org/10.1109/GlobConPT57482.2022.9938331.
4. P. Ramesh et al., "Software Defined Network Architecture Based Network Slicing in Fifth Generation Networks", Inf. Midem-J. Microelec- tron. Electron. Compon. Mater., Vol. 54, No. 2(2024), pp. 123–130
5. A. Anand, G. De Veciana and S. Shakkottai, "Joint Scheduling of URLLC and eMBB Traffic in 5G Wireless Networks," IEEE INFOCOM 2018 - IEEE Conference on Computer Communications, Honolulu, HI, USA, 2018, pp. 1970-1978, https://doi.org/10.1109/INFOCOM.2018.8486430.
6. R. Kassab, O. Simeone and P. Popovski, "Coexistence of URLLC and eMBB Services in the C-RAN Uplink: An Information-Theoretic Study," 2018 IEEE Global Communications Conference (GLOBECOM), Abu Dhabi, United Arab Emirates, 2018, pp. 1-6, https://doi.org/10.1109/GLOCOM.2018.8647460.
7. Y. L. Lee, J. Loo, T. C. Chuah and L. -C. Wang, "Dynamic Network Slicing for Multitenant Heterogeneous Cloud Radio Access Networks," in IEEE Transactions on Wireless Communications, vol. 17, no. 4, pp. 2146-2161, April 2018, https://doi.org/10.1109/TWC.2017.2789294.

8. S. Cavallero et al., "A New Scheduler for URLLC in 5G NR IIoT Networks with Spatio-Temporal Traffic Correlations," ICC 2023 - IEEE International Conference on Communications, Rome, Italy, 2023, pp. 1010-1015, https://doi.org/10.1109/ICC45041.2023.10279558.
9. Praveenkumar Korrai , Eva Lagunas , Shree Krishna Sharma , Ashok Bandi, Symeon Chatzinotas And Björn Ottersten , " A Ran Resource Slicing Mechanism For Multiplexing Of eMBB And URLLC Services In OFDMA Based 5g Wireless Networks . " IEEE Access – 2020 .
10. S. Chauhan, A. Gupta, V. T, and N. S, "Efficient Resource Allocation algorithms for Multihop D2D approach in 5G network," International Journal of Communication Systems, 2023. https://doi.org/10.1002/dac.5520.
11. P. Popovski, K. F. Trillingsgaard, O. Simeone, and G. Durisi, "5G wireless network slicing for eMBB, URLLC, and mMTC: A communication-theoretic view," IEEE Access, vol. 6, pp. 55 765–55 779, Sept. 2018.
12. Yan Kyaw Tun , Do Hyeon Kim , Madyan Alsenwi ,Nguyen H. Tran , Zhu Han And Choong Seon Hong " Energy Efficient Communication and Computation Resource Slicing for eMBB and URLLC Coexistence in 5G and Beyond . " IEEE Access – 2020
13. A. A. Esswie and K. I. Pedersen, ``Opportunistic spatial preemptive scheduling for URLLC and eMBB coexistence in multi-user 5G net-works," IEEE Access, vol. 6, pp. 38451 38463, Jul. 2018.
14. K. M. Cohen, S. Park, O. Simeone, P. Popovski and S. Shamai, "Guaranteed Dynamic Scheduling of Ultra-Reliable Low-Latency Traffic via Conformal Prediction," in IEEE Signal Processing Letters, vol. 30, pp. 473-477, 2023, https://doi.org/10.1109/LSP.2023.3264939
15. A. A. Esswie and K. I. Pedersen, "Opportunistic Spatial Preemptive Scheduling for URLLC and eMBB Coexistence in Multi-User 5G Networks," in *IEEE Access*, vol. 6, pp. 38451-38463, 2018, https://doi.org/10.1109/ACCESS.2018.2854292.
16. C. Padilla, R. Hashemi, N. H. Mahmood and M. Latva-Aho, "A Nonlinear Autoregressive Neural Network for Interference Prediction and Resource Allocation in URLLC Scenarios," *2021 International Conference on Information and Communication Technology Convergence (ICTC)*, Jeju Island, Korea, Republic of, 2021, pp. 184-189, https://doi.org/10.1109/ICTC52510.2021.9620845.
17. P. R and B. P. T. V, "Performance Analysis of NOMA under Power Control Mechanism," 2021 Innovations in Power and Advanced Computing Technologies (i-PACT), Kuala Lumpur, Malaysia, 2021, pp. 1-5, https://doi.org/10.1109/i-PACT52855.2021.9696636.
18. Xu & Xie "Conformal prediction for time series "- IEEE Transactions on Pattern Analysis and Machine Intelligence – 2023

Arrived: 06. 05. 2024
Accepted: 01. 10. 2024

Original scientific paper
https://doi.org/10.33180/InfMIDEM2025.104

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
Vol. 55, No. 1(2025), 47 – 54

Fractal Resonator Based Frequency Reconfigurable Antenna with Varying Capacitive Effect for Wireless Applications

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Abstract: A frequency reconfigurable antenna for wireless applications using a fractal antenna structure is proposed. The fractal antenna is composed of a step resonator type which has a mirror image at the vertical axis in the top with a slit and a parallel mirror image at the vertical axis in the bottom without a slit. The resonating frequency of the fractal antenna is controlled by a Positive-Intrinsic-Negative (PIN) diode. Two PIN diodes are connected between the top and bottom of the fractal antenna. With the varying capacitance effect, the four possible modes of operation of the diode are obtained at the dual resonating frequency of 2.7 and 3.2 GHz. The proposed design holds significant potential for applications in Fifth Generation New Radio (5G NR) n1 band, and Wireless Fidelity (Wi-Fi) access points due to its small size and easy control mechanism. The Specific Absorption Rate (SAR) values were analyzed and are within the safety limits.

Keywords: Reconfigurable Antenna, Fractal, PIN diodes, Wireless, SAR

Frekvenčno nastavljiva antena s spreminjajočim se kapacitivnim učinkom za brezžične aplikacije, ki temelji na fraktalnem resonatorju

Izvleček: Predstavljena je frekvenčno nastavljiva antena za brezžične aplikacije, ki uporablja fraktalno strukturo antene. Fraktalna antena je sestavljena iz stopničastega resonatorja, ki ima zrcalno sliko na vrhu navpične osi z režo in vzporedno zrcalno sliko na dnu navpične osi brez reže. Resonančno frekvenco fraktalne antene nadzoruje dioda PIN (Positive-Intrinsic-Negative). Dve diodi PIN sta povezani med zgornjim in spodnjim delom fraktalne antene. S spreminjajočim se kapacitivnim učinkom se pri dvojni resonančni frekvenci 2,7 in 3,2 GHz dosežejo štirje možni načini delovanja diode. Predlagana zasnova ima zaradi svoje majhnosti in enostavnega mehanizma upravljanja velik potencial za uporabo v frekvenčnem pasu n1 nove radijske zveze pete generacije (5G NR) in dostopnih točkah brezžične povezave (Wi-Fi). Analizirane so bile vrednosti specifične absorpcijske hitrosti (SAR), ki so v mejah varnosti.

Ključne besede: Konfigurabilna antena, fraktali, diode PIN, brezžična povezava, SAR

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1 Introduction

The use of wireless technologies such as Wi-Fi, Wireless Gigabit Alliance (WiGig), Light fidelity (Li-Fi), Near-field communication technology, Fifth Generation (5G), Sixth Generation (6G), etc., in mobile phones has been increasing nowadays. The antenna for operating at the modes mentioned earlier is designed separately [1] and integrated into a single smartphone unit. As the space complexity is high, the heat liberated from the

How to cite:
A. Thangam Manoharan et al., "Fractal Resonator Based Frequency Reconfigurable Antenna with Varying Capacitive Effect for Wireless Applications", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 55, No. 1(2025), pp. 47–54

phones is increasing day to day. Also, there are some major considerations to be taken care of in the design of 5G smartphones, such as resonant frequency, antenna size, isolation, and SAR.

Reconfigurable Antenna finds applications where different frequencies are utilized in the same node like smartphones, Security, Radio Detection and Ranging (RADAR), and Automation etc.,. A frequency reconfigurable antenna [2] is a single antenna that switches to multiple frequencies, instead of using several antenna array elements for different frequencies. This reduces the antenna space, cost and also improves the compactness of the antenna size. The magneto-electric dipole [3] and Vivaldi antenna [4], [5] are large in size and have unidirectional beams. These characteristics are not suitable for portable devices, where a compact size is preferred. The proposed antenna is designed to reduce the size of the reconfigurable antenna and aims at reducing the SAR.

The switching in the reconfigurable antenna is achieved by electrical, mechanical, and optical modes. The electrical switching of frequencies is obtained by PIN diodes, Varactor diodes and Radio Frequency Microelectromechanical Systems (RF MEMS) switches. The mechanical switching is done by rotation in angular or linear motion, whereas the optical switching is done using Optical Fibre Cable (OFC), Light-emitting diode (LED) and Light amplification by stimulated emission of radiation (LASER). Of all the modes, electrical switching consumes power because an external supply is needed to bias the diodes. Despite huge power consumption, electrical switching is more advantageous due to its efficiency, reliability, and ease of integrating with microwave circuitry [6].

To switch the PIN diodes used in a reconfigurable antenna, some of the techniques used are external biasing circuit with a battery [7] and a remotely controlled Arduino unit [8]. Switching ON the PIN diode needs a high tuning speed, a high direct current (DC) bias current in the ON state, and a high power-handling capacity [6]. Owing to its reliability and cost-effectiveness, electrical switching using PIN diodes is more suitable for reconfigurable antenna.

The Electromagnetic (EM) radiation emitted from the antenna gets coupled to the human tissue and alters the biological functions of the body [9]. The EM absorption by humans is measured in terms of SAR. As per the Federal Communications Commission (FCC), American National Standards Institute / Institute of Electrical and Electronics Engineers (ANSI / IEEE), and Safety Code 6 standards the recommended SAR values are 0.08 W/kg for a Whole body and 1.6 W/kg for over any 1gram (g) of tissue [10].

A compact reconfigurable antenna of size 18 x 20 x 0.035 mm^3 has been designed. The top and bottom patches are connected through PIN diodes, and the frequency reconfigurable antenna switches at four different cases. The SAR analysis was done for the four cases of PIN diode switches and the results were analyzed.

2 Antenna design

The FR4 epoxy substrate of thickness 1.6 mm, and a loss tangent of 4.4 is constructed over the ground plane. To achieve the resonant frequency at the desired level, the defective ground is designed as an inverted E and C-shaped structure. The substrate has a cross-sectional area of 20 x 21 mm^2 and the patch has a cross-sectional area of 18 x 20 mm^2. The fractal antenna is composed of a step resonator type which has a mirror image at the vertical axis in the top with a slit and a parallel mirror image at the vertical axis in the bottom without a slit. The dimensions of the fractal antenna design are shown in Table 1. The top view and bottom view of the antenna are shown in Figure 1 (a) and (b).

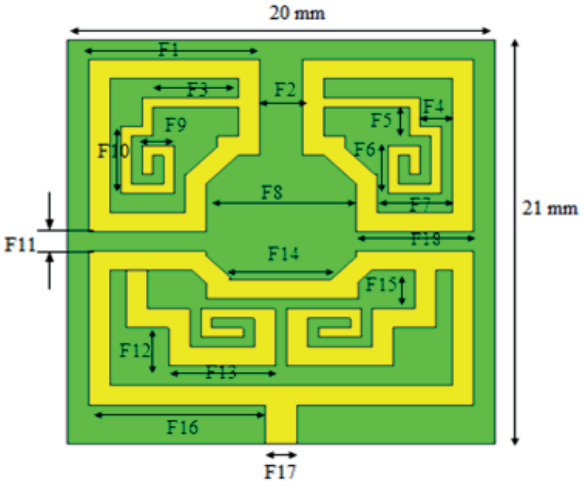

Figure 1: (a) Top view of antenna

The proposed antenna is designed and simulated using Computer Simulation Technology (CST) Microwave Studio software. The PIN diode is inserted between the antenna phases at two points and is shown in Figure 2. For different switching cases of PIN diodes, the return loss and resonant frequency are tabulated. For the four switching states of the diode, the value of the inductance and capacitance are chosen from the PIN diode datasheet. The diode ON state is formulated using an equivalent circuit consisting of 4.7 Ω resistor connected in series with 0.015 nH inductor. While the OFF state is formulated with an equivalent circuit of parallel combination of 4.7 Ω resistor and 0.017 pF capacitor connected in series with 0.015 nH inductor.

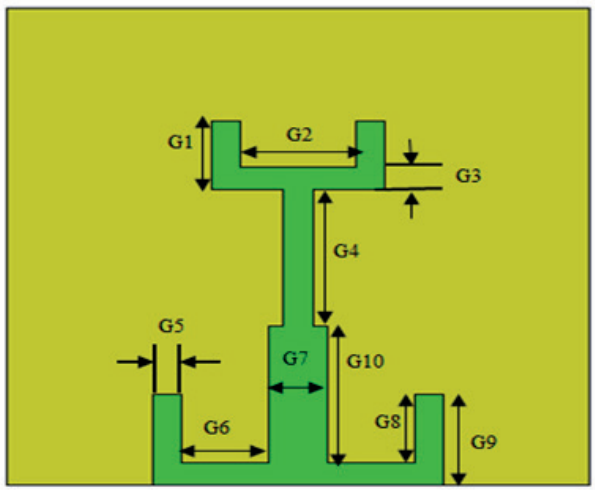

Figure 1: (b) Bottom View of Antenna

Table 1: Dimension of antenna structure

Parameters	Dimension (mm)	Parameters	Dimension (mm)	Parameters	Dimension (mm)
G1	1	F1	8	F11	1
G2	4	F2	2	F12	2
G3	1	F3	4.5	F13	5
G4	6	F4	1.5	F14	5
G5	1	F5	1.5	F15	2
G6	3	F6	2.5	F16	8.25
G7	2	F7	3.5	F17	1.5
G8	3	F8	7	F18	5.5
G9	4	F9	1.5		
G10	6	F10	3.5		

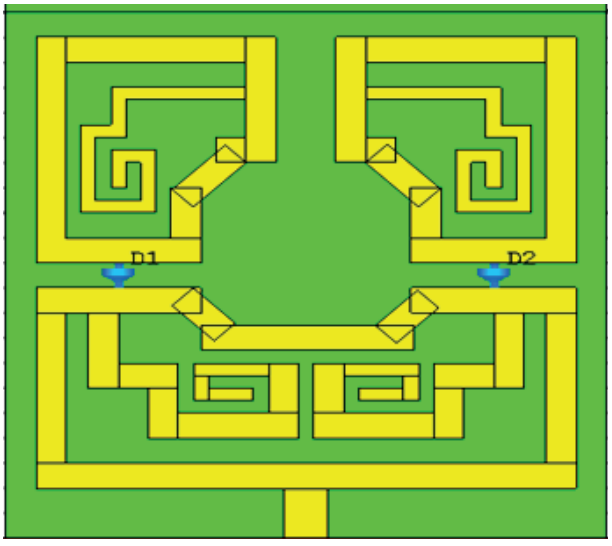

Figure 2: Antenna with PIN diode

2.1 Antenna working strategy

The substrate of the antenna was designed initially considering a conventional rectangular Microstrip patch antenna for the frequency of 3.5 GHz using the equation (1) and (2) by calculating the effective dielectric constant based on the height, dielectric constant & width of the patch antenna, and effective length [11], [12].

$$L_{eff} = \frac{c}{2 f_r \sqrt{\varepsilon_{eff}}} \tag{1}$$

$$\varepsilon_{eff} \approx \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 12\left(\frac{h}{w}\right)\right)^{-0.5} \tag{2}$$

The antenna design is then optimized to incorporate the fractal step resonator structure with a split in the middle. This creates a capacitive effect between the structures as shown in Figure 3 and shifts the frequency based on the diode switching condition. For case (i) when two diodes are off, the large area is utilized for the capacitance effect and the distance between the plates is increasing [13], thereby decreasing the capacitance as computed in the equation.(3). Due to this, the resonant frequency shifts lower to 2.878 GHz.

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d} \tag{3}$$

where, ε_o – permittivity of air
ε_r – relative permittivity
A – Area of the plate
d – distance between the plates

For case (ii), when the diode D1 is inserted- Diode (10) case, the capacitance values are reduced by 3.09 x 10^{-15} F. This result in another resonant frequency shifted left at 3.175 GHz in addition to 2.729 GHz. Similar results were obtained for case (iii)-Diode (01). For case (iv), When the diodes D1 and D2 are inserted, both the diodes are ON, and the resonant frequency is shifted higher to 3.252 GHz.

At the bottom of the substrate, an inverted E- shaped structure is tilted towards the horizontal plane. In the middle of the E-structure, a small projection is connected to an inverted C-shaped structure. The inverted E and C-shaped structures together constitute the defective ground structure. The defects introduced in the ground plane alter the current distribution and result in variations of slot resistance, capacitance, and inductance.

3 Experimental results

The designed antenna is fabricated and tested using Vector Network Analyzer (VNA). The width and height of the antenna are 18 mm and 20 mm respectively and are depicted in Figure 4 (a) and (b). The antenna is provided with a port extension to check the output at the VNA connected. The bottom view of the antenna with defective ground inverted E and C-shaped structure is shown in Figure 5.

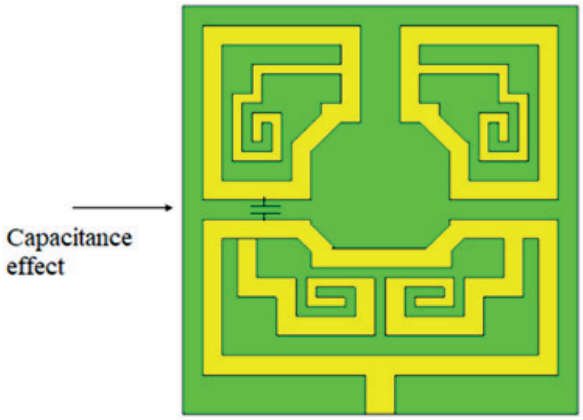

Figure 3: Illustration of capacitive effect

The PIN diode of type BAP65-03,115 is used as an RF switch for achieving frequency reconfigurability in the fractal antenna. The insertion of two PIN diodes in between the antenna elements results in four different switching cases such as 00, 01, 10 and 11 for OFF-OFF, OFF-ON, ON-OFF and ON-ON conditions. When one of the diodes is ON, the diode acts as a short circuit, and the inductive reactance dominates. As the diode is OFF, the diode acts as an open circuit, and capacitive reactance dominates. The inductive reactance shifts the resonant frequency (f_r) to a higher frequency (f_r +Δf) whereas capacitive reactance shifts it to a lower frequency (f_r -Δf).

Figure 4: (a) Width of antenna

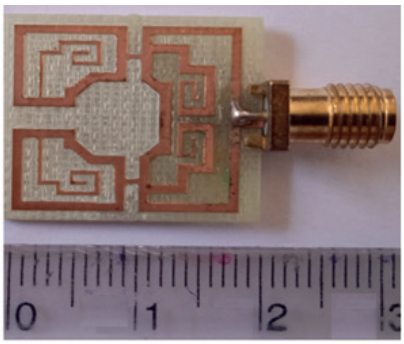

Figure 4: (b) Height of antenna

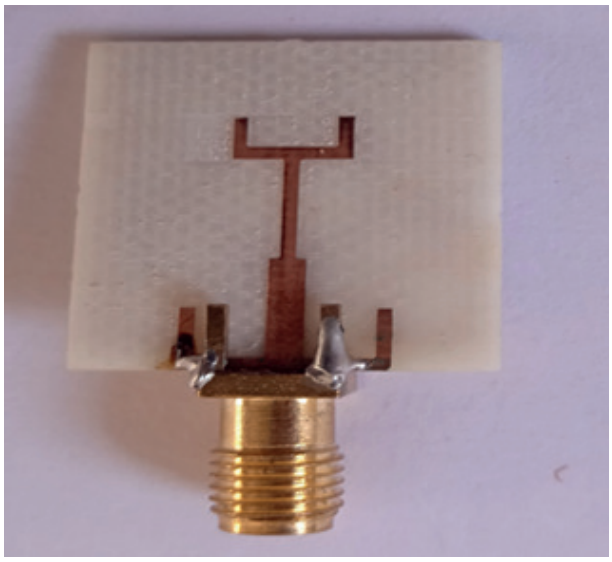

Figure 5: Fabricated antenna – bottom View

The experimental setup consisting of the fabricated fractal antenna with PIN diode and VNA is shown in Figure.6. To switch ON the diode, a 3V battery is connected across the PIN diodes through wires. The diode is said to be in OFF state when the battery is disconnected, as no current flows through the diode. The return loss values are tabulated in Table 4 where the switching of the diode results in antenna resonating between 2.713 GHz and 3.252 GHz frequencies. The experimental results obtained through VNA are depicted in Figure 7 for the diode 10 state.

The switching in the diode is considered to be a short circuit case for each of the diodes being set ON. The inductive reactance dominates when both the diodes are ON and resonate at a high frequency of 3.252 GHz. Similarly, when both the diodes are OFF, it acts as open-circuited capacitance. The fractal antenna resonating frequency is shifted to the lower frequency of 2.878 GHz. The average frequency, f_{av} is calculated by taking the mean of the highest and the lowest frequency values considering ON-ON and OFF-OFF cases of the diodes. From the results obtained the average frequency of

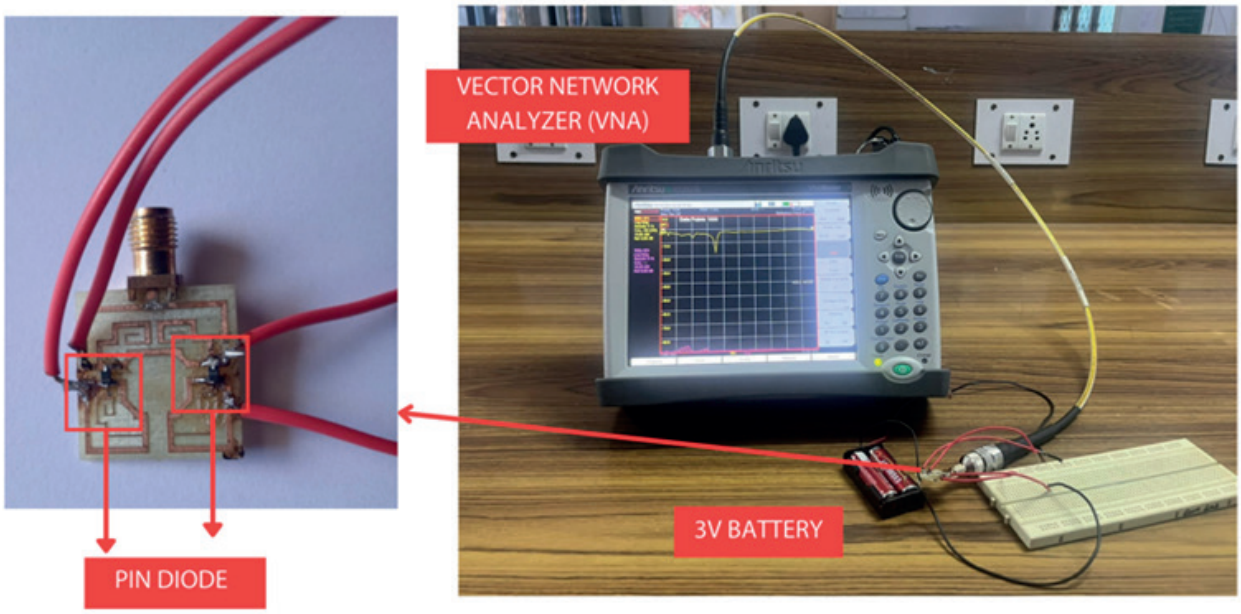

Figure 6: Antenna testing with VNA

3.065 GHz shifts higher to 3.252 GHz with a Δf of 0.187 GHz due to inductive effect, and shifts lower to 2.878 GHz due to capacitive effect.

The scattering parameter S11 depicts the return loss obtained for each case of the connected diode in the fractal antenna. From the obtained results given in Table 4, the antenna exhibits a return loss of less than -10 dB for all four combinations of diodes. The lowest return loss value of -31.57 dB is obtained for the antenna operating at 2.729 GHz when the diode is in ON-OFF (10) state.

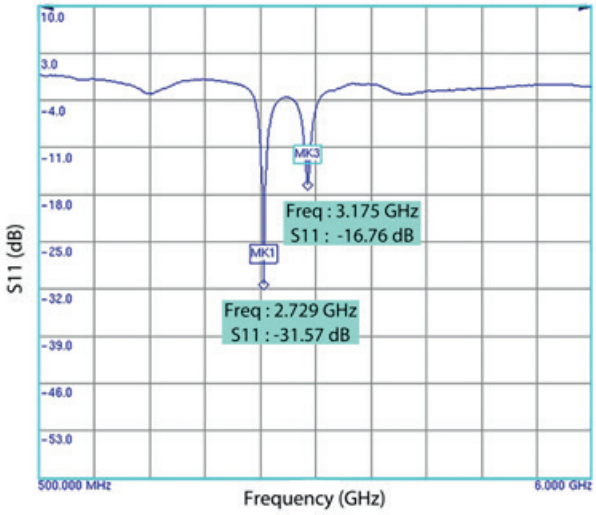

Figure 7: Return loss for diode – ON-OFF (10) state

4 SAR Measurement

The Electromagnetic absorption by humans is measured in terms of specific absorption rate (SAR). As per the FCC, ANSI/IEEE and Safety code 6 standards the recommended SAR values for smartphones are 0.08 W/kg for a Whole body and 1.6 W/kg for over any 1gram (g) of tissue. This maximum is set to 1.6 W/kg averaged over 1g of tissue, or 2 W/kg averaged over 10g of tissue [14].

The six-layer human head model (Figure 8) consisting of skin, fat, bone, Dura, Colony-Stimulating Factor (CSF), and brain is assumed to be a sphere and it is designed based on the properties of permittivity, conductivity, and thickness [15]. It acts as an absorbing surface for the radiations from the proposed antenna.

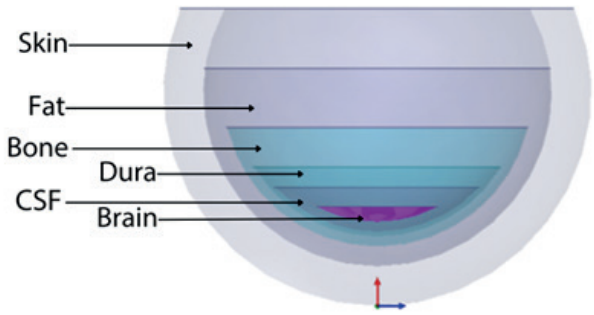

Figure 8: Six layer human head model

The tissue properties of these layers are taken into account to examine the amount of radiation. The tissue properties considered are permittivity, conductivity,

and thickness, and the values corresponding to each layer are shown in Table 2 cited in [15]. The six-layer human head model is placed in the front of the antenna designed and the SAR is computed in CST Microwave studio as shown in Figure 9.

Table 2: Tissue properties of human head model

Tissue	Permittivity	Conductivity (S/m)	Thickness (mm)
Skin	40.7	0.65	1
Fat	10	0.17	0.14
Bone	20.9	0.33	0.41
Dura	40.7	0.65	0.5
CSF	79.1	2.14	0.2
Brain	41.1	0.86	81

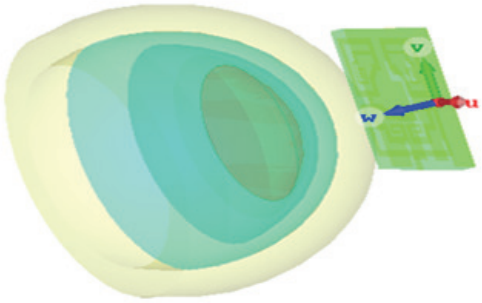

Figure 9: Head model with Antenna in CST

The computed SAR value for diode 00 state at 2.878 GHz is shown in Figure. 10 and is well within the standard safety limits. The SAR value for diode 10 state operating at 2.729 GHz is 0.648 which is higher as compared with other cases of diode switching (Table 4). The comparison of State-of-the-art antennas is given in Table 3. The proposed antenna is compact as compared to other state-of-the-art antennas. As the space occupied is lesser, it can be used in 5G smartphones to be operated at 2.713 GHz, 2.729 GHz, 2.878 GHz, 3.175 GHz, 3.183 GHz and 3.252 GHz frequencies.

Table 4: Return loss and SAR values

Diode Switching States D1D2	Resonant frequencies (GHz)	Return loss (dB)	SAR (W/kg)
00	2.878	-18.44	0.294
01	2.713	-30.52	0.334
	3.183	-17.71	0.149
10	2.729	-31.57	0.648
	3.175	-16.76	0.173
11	3.252	-37.52	0.174

In the proposed work, SAR analysis is performed in the human head model considering 10 g of tissue to test the electromagnetic absorption from the antenna. The simulation results infer that the SAR value holds within the safety limit of 2 W/kg averaged over 10g of tissue.

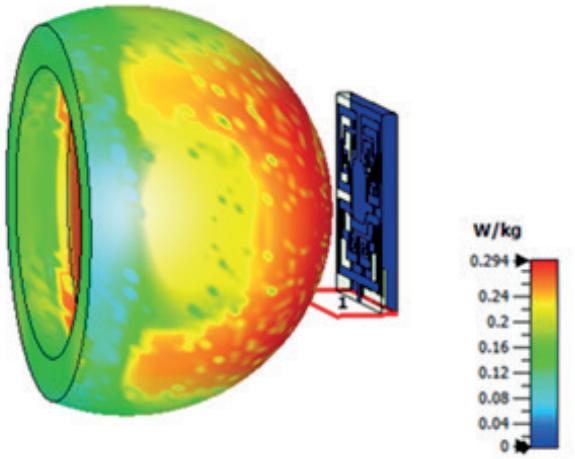

Figure 10: SAR Analysis- diode 00 state-2.878 GHz

Table 3: Comparison with the state-of-the-art antennas

Ref	Antenna size (mm^2)	Substrate (ε_r , h in mm)	Resonant Frequencies (GHz)	Reconfigurable	SAR Analysis
[16]	33×21	FR4-ε_r =4.3, h =1.6	3.3-3.7, 5-5.30	Yes	No
[17]	30×40	Rogers (RO4350B) – ε_r =3.66, h =0.76	3, 6.8	Yes	No
[18]	46×52	FR4-ε_r =4.4, h =1.6	3.42 – 3.82, 5.17- 6.07, 6.89 -7.48 (OFF-OFF State)	Yes	No
[19]	24×30.5	RO4003C-εr =3.38, h =1.5	3.5 and in between 5.45-5.9	Yes	No
[20]	82.77x83.53	Taconic RF-30 – ε_r=4.4, h= 1.6 mm	1.8,2.7,3.1,3.3,4.1,5.1,5.4	Yes	No
This Work	18 x 20	FR4-ε_r =4.3, h =1.6	2.713, 2.729, 2.878, 3.175, 3.183 and 3.252	Yes	Yes

5 Conclusion

The fractal-based reconfigurable antenna is designed and analyzed for wireless applications. The S parameter results show better agreement for the numerical calculations obtained by substituting the capacitance value. The capacitance effect shifts the resonant frequency to a higher level and an average increase of return loss in dB to 50%. The SAR values are also analyzed for different diode-switching cases. The low SAR (0.149) is obtained for the diode 01 case operating at 3.183 GHz and the high SAR (0.648) for the diode 10 case operating at 2.729 GHz. The SAR values are well within the safety limits.

6 Conflict of interest

We, the authors, declare no conflict of interest

The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results

7 References

1. T. Alam, M. R. I. Faruque, M. T. Islam, Printed Circular Patch Wideband Antenna for Wireless Communication, Journal of Microelectronics, Electronic Components and Materials, Vol. 44, No. 3, 2014, 212 – 217.
2. Karthika K, Kavitha K (2021) Reconfigurable Antennas for Advanced Wireless Communications: a review. Wirel Pers Commun 120(4):2711–2771. https://doi.org/10.1007/s11277-021-08555-4
3. Ge, L.; Luk, K.M. Band-reconfigurable unidirectional antenna: A simple, efficient magneto-electric antenna for cognitive radio applications. IEEE Antennas Propag. Mag. 2016, 58, 18–27.
4. Chagharvand, S.; Hamid, M.R.; Kamarudin, M.R.; Kelly, J.R. Wide-to-narrowband reconfigurable Vivaldi antenna using switched-feed technique. Telecommun. Syst. 2016, 63, 711–717.
5. Chagharvand, S.; Hamid, M.R.; Kamarudin, M.R.; Kelly, J.R. Wide and multi-band reconfigurable Vivaldi antenna with slot-line feed. Telecommun. Syst. 2017, 65, 79–85.
6. Ojaroudi Parchin, N.; Jahanbakhsh Basherlou, H.; Al-Yasir, Y.I.A.; M. Abdulkhaleq, A.; A. Abd-Alhameed, R., "Reconfigurable Antennas: Switching Techniques—A Survey", Electronics 2020, 9, 336. https://doi.org/10.3390/ electronics9020336
7. Awan, W.A.; Naqvi, S.I.; Ali, W.A.E.; Hussain, N.; Iqbal, A.; Tran, H.H.; Alibakhshikenari, M.; Limiti, E. "Design and Realization of a Frequency Reconfigurable Antenna with Wide, Dual, and Single-Band Operations for Compact Sized Wireless Applications", Electronics 2021, 10, 1321. https://doi.org/ 10.3390/electronics10111321
8. Gençoğlan, D.N.; Çolak, ¸S.; Palandöken, M." Spiral-ResonatorBased Frequency Reconfigurable Antenna Design for Sub-6 GHz Applications", Appl. Sci. 2023, 13, 8719. https://doi.org/10.3390/ app13158719.
9. ICNIRP, "Guidelines for limiting exposure to time-varying electric, magnetic, and electromagnetic fields (up to 300 GHz)", 1998, Health Physiol. 74, pp. 494–552.
10. IEEE C95.1-1999, "Safety levels with respect to human exposure to radiofrequency electromagnetic fields: 3 kHz to 300 GHz", IEEE standard,1999.
11. Bahl, I.J, "A designer's guide to microstrip line. Microwaves", 1977, 16, 174–182.
12. Derneryd, "A Design of Microstrip Patch Antenna Elements", 1978.
13. H. Nishiyama and M. Nakamura, "Form and capacitance of parallel-plate capacitors," in IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part A, vol. 17, no. 3, pp. 477-484, Sept. 1994, https://doi.org/10.1109/95.311759
14. Lin, J. C., "A new IEEE standard for safety levels with respect to human exposure to radio-frequency radiation," IEEE Antennas and Propagation Magazine, Vol. 48, No. 1,pp. 157-159, Feb. 2006.
15. Asmalak, "Evaluation of SAR Distribution in Six-Layer Human Head Model", International Journal of Antennas and Propagation, 2015, vol.58, pp.40-47
16. H. Medkour, M. Cheniti, A. Narbudowicz, S. Das, E. Vandelle, and T. Vuong, "Coplanar waveguide-based ultra-wide band antenna with switchable filtering of WIMAX 3.5GHz and WLAN 5GHz signals," Microw. Opt. Technol. Lett., vol. 62, pp. 2398– 2404, Feb. 2020.
17. H. Ayadi, J. Machac, S. Beld, and L. Latrach, "Planar hexagonal antenna with dual reconfigurable notched bands for wireless communication devices," Radioengineering, vol. 30, no. 1, pp. 25-32, Apr. 2021.
18. R. Orugu and N. Moses, "Triangular fractal loaded reconfigurable antenna with notch band characteristics," Int. Journal of Numerical Modelling Electronic Networks Devices and Fields, vol. 34, no. 1, pp. 1-11, Sep. 2020.
19. A. Haider, M. Rahman, H. Ahmad, M. N. Jahromi, M. T. Niaz, and H. S. Kim, "Frequency-agile WLAN notch UWB antenna for URLLC applications," Computers, Materials & Continua, vol. 67, no. 2, pp. 2243-2254, 2021.

20. M. M. Ismail et al., "Multi-Beam Metasurface Control Based on Frequency Reconfigurable Antenna", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 54, No. 2,2024, pp. 77–85.

Arrived: 08. 06. 2024
Accepted: 01. 10. 2024

Original scientific paper
https://doi.org/10.33180/InfMIDEM2025.105

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
Vol. 55, No. 1(2025), 55 – 64

Design and Optimization of Multiple-Channel Double Dynamic Switching Biased Op-Amp for Switched Capacitor Integrator Using FinFET Technology

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Abstract: This paper presents the design and optimization of a parametric multiple-channel Double Dynamic Switching Biased Complementary Folded-Cascode Amplifier with switched capacitor integrator application in 32nm FinFET technology. The LTspice simulations demonstrate that the amplifier can attain an open-loop DC gain of 44.8dB, and a phase margin of about 87.8° with ±0.5V supply voltages. Moreover, the amplifier power consumption is measured 246µW including bias circuitry and a Gain-Bandwidth Product (GBW) of 77.45MHz under a 5pF load capacitor. The circuit's stability enables it to offer diverse design capabilities tailored to specific application needs. This novel design is capable of reducing supply voltages and power dissipation.

Keywords: 32nm FinFET Technology, Complementary Folded-Cascode Amplifier, Double Dynamic Switching Bias, Self-Cascode, Switched Capacitor

Načrtovanje in optimizacija večkanalnega dvojnega dinamičnega preklopnega optičnega ojačevalnika za stikalni kondenzatorski integrator z uporabo tehnologije FinFET

Izvleček: Članek predstavlja načrtovanje in optimizacijo parametričnega večkanalnega ojačevalnika z dvojnim dinamičnim preklopom, ki se opira na komponente z zloženo kaskodo, z uporabo integratorja s preklopnim kondenzatorjem v 32 nm tehnologiji FinFET. Simulacije LTspice kažejo, da lahko ojačevalnik doseže ojačenje z odprto zanko DC 44,8 dB in fazno rezervo približno 87,8° pri napajalnih napetostih ±0,5 V. Poleg tega je izmerjena poraba energije ojačevalnika 246 µW, vključno z napajalnim vezjem in GBW 77,45 MHz pri obremenitvenem kondenzatorju 5pF. Stabilnost vezja omogoča diverzno načrtovanje s prilagoditvami glede na potrebe aplikacije. Ta nova zasnova lahko zmanjša napajalne napetosti in porabo.

Ključne besede: 32nm FinFET tehnologija, komplementarni kaskodni ojačevalnik, Dvojno dinamično preklapljanje polarizacije, Preklopni kondenzator

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How to cite:
M. Babaeian Far et al., "Design and Optimization of Multiple-Channel Double Dynamic Switching Biased Op-Amp for Switched Capacitor Integrator Using FinFET Technology", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 55, No. 1(2025), pp. 55–64

1 Introduction

In semiconductor technology, the constant search for smaller, faster, and more energy-efficient transistors has driven technological innovation. Recent advances at the nanoscale level and the advent of multi-gate transistors have ushered in a new era of complexity in the design process. One such breakthrough technology that has attracted significant attention in the integrated circuit (IC) design industry is FinFET transistors. These transistors offer promising solutions to the challenges of shrinking device dimensions and enable performance and efficiency in modern semiconductor devices.

On the other hand, the relentless pursuit of miniaturization and performance improvement in electronic circuits extends beyond transistors to encompass various facets. Market demands and the push for advancements in portable electronics have compelled the industry to develop circuits with low voltage (LV) requirements and often restricted power consumption, presenting a significant challenge. Many emerging products must operate at voltages of 3V or lower to stay competitive in an industry characterized by rapid turnover [1]. Implantable medical electronic devices, especially those incorporating analog and digital circuits, are prime examples of this scenario.

In this competitive landscape, numerous proven techniques are used in innovative circuit design as essential for market viability. For instance, companies are increasingly utilizing CMOS switched capacitor (SC) methods for implementing analog signal processing integrated circuits (ICs) due to their effectiveness. Previous research has demonstrated the effectiveness of utilizing SC techniques with CMOS operational amplifiers (Op-Amps) to implement analog functions such as filters [2-4]. However, using multiple Op-Amps often creates significant power consumption, potentially leading to operational instability. To mitigate power dissipation associated with Op-Amps, various strategies including reduced supply voltages, bulk-driven topologies, floating-gate transistors, self-cascode structures, and subthreshold designs have been explored [1, 5].

In achieving high-speed operation, it is crucial to carefully address design considerations regarding distortion alongside the increase in power dissipation. This necessity arises from the intrinsic capability of Op-Amps to process analog signals. On the other hand, prior research has introduced a CMOS Folded-Cascode (FC) Op-Amp with a Double Dynamic Switching Biased (DDSB) in a simplified configuration to ensure minimal power consumption while maintaining switching capability [2]. This amplifier exhibits high power dissipation and occupies significant physical space. Operating with a supply voltage of 3V and consuming 9.2mW of power, it is suitable for signal processing applications. However, integrating it as an element in new-generation devices may pose challenges.

This study discusses the development of a Complementary Folded-Cascode (CFC) Op-Amp, designed to operate with a supply voltage of 1V (±0.5V) and achieve operational performance with a power consumption level of 246μW. PTM 32nm FinFET technology was chosen for the designs to leverage its advantages, including lower power consumption, higher density, improved scaling, enhanced reliability, and compatibility with future advancements in semiconductor technology. In line with FinFET technology, the self-cascode structure was employed, enabling both an increase in output resistance and the ability to design at lower voltages. This feature enables the design to have parametric flexibility. Moreover, integrating the DDSB circuit in [2] helps reduce undesirable phenomena such as noise and process variations, consequently enhancing the overall performance and stability. The stability and performance of the proposed circuit under various conditions were analyzed using the SC integrator application, yielding the expected triangle behavior.

In this paper, Section 2 elaborates on the FinFET, the integration of the self-cascode structure with FinFET, and the development of the CFC Op-Amp with DDSB. Section 3 provides details on the SC integrator topology and its FinFET-based design. Additionally, this section discusses the performance evaluation of the integrator, while Section 4 summarizes the conclusions. Results obtained reveal that the novel design employed in the present study can reduce the amount of supply voltages and power dissipation.

2 Design of CFC op-amp

2.1 FinFET

The inception of FinFET-like structures traces back to the introduction of a Fully Depleted Lean Channel Transistor (DELTA) by Hisamoto et al. in 1989 [6, 7], highlighting the longstanding pursuit of enhanced transistor architectures. The distinctive three-dimensional structure of FinFETs, with a thin silicon body formed perpendicular to the wafer plane, enables superior electrostatic control and reduced leakage compared to traditional planar MOSFETs [8]. FinFET transistors, operating at nanoscale dimensions, exhibit reduced Drain-Induced Barrier Lowering (DIBL) and mitigated

other Short-Channel Effects (SCEs), thereby enhancing overall performance and reliability [9]. This translates to higher on-state current, lower leakage, and faster switching speeds, making FinFETs an attractive option for many applications. Moreover, the fabrication process for FinFET transistors is compatible with conventional CMOS processes, enabling seamless integration into existing technologies.

Overall, FinFETs operate via three primary mechanisms: independent-gate (IG) connection, shorted-gate (SG) connection, and low-power (LP) mode [10]. As depicted in Fig. 1(a), the SG type features a three-terminal device. SG FinFETs present a promising alternative to MOSFETs, offering increased on-state current and faster transition speeds, thus enhancing performance. Moreover, robust gate control provides enhanced suppression against SCEs and gate-dielectric leakage. A thick masking oxide, T_{mask}, can be utilized to enable the operation of the devices as Double-Gate (DG) FinFETs, with sidewall gates providing electrical functionality exclusively.

The IG type eliminates the upper portion of the gate to create two separate gates, as shown in Fig. 1(b). Operating as a four-terminal device, this configuration allows the front and back gates to be coupled to distinct inputs. Consequently, the IG FinFET can function as a pair of parallel transistors, enhancing design flexibility and significantly reducing the number of transistors. LP mode is an exception to the typical behavior of the IG mode, effectively reducing threshold leakage by adjusting the back gate voltage, as noted in [8]. Further details on the operation modes can be found in [10].

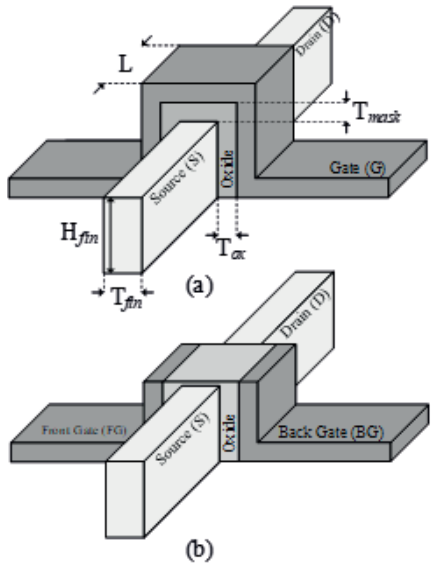

Figure 1: FinFET connection types: a): shorted-gate, b): independent-gate.

For a DG-FinFET, when the biasing condition is appropriate, current flows from the source to the drain under the influence of the corresponding sidewall gates, spanning the height H_{fn} of each fin. Consequently, the width (W) of the FinFET structure depends on the height of the fins. For a single-fin DG-FinFET, the total width can be determined as in equation (1).

$$W = 2H_{fin} \tag{1}$$

This study presents an Op-Amp design utilizing IG FinFETs operating in LP mode. The simulations are based on the Predictive Technology Model (PTM) for 32nm FinFETs. PTM is selected as the simulation model due to its comprehensive coverage of physical effects and excellent scalability. This approach enables precise predictions and enhances efficiency in circuit design. Overall, the combination of the Op-Amp design with the self-cascode structure for IG FinFETs in LP mode, supported by PTM, presents a promising approach for optimizing circuit performance in advanced semiconductor technologies [8].

2.2 Self-Cascode structure

The self-cascode configuration is depicted in Fig. 2 as a two-transistor setup, which can be viewed as an individual composite transistor. This composite structure exhibits a significantly extended effective channel length and output resistance. The lower transistor, referred to as F_{2a}, functions as an input-dependent resistor. To maintain optimal performance, the W/L ratio of F_{2b} is set more significantly larger than that of F_{2a}, denoted as C>1 [5].

Fig. 3 illustrates the results obtained by adjusting the structure using the parameters Composite (C) and Multiplier (M). One notable observation is the increased output resistance compared to configurations utilizing a single FinFET as expected. Increasing the value of C, which solely enlarges the size of F_{2b}, leads to elevated output resistance. Similarly, increasing the value of M

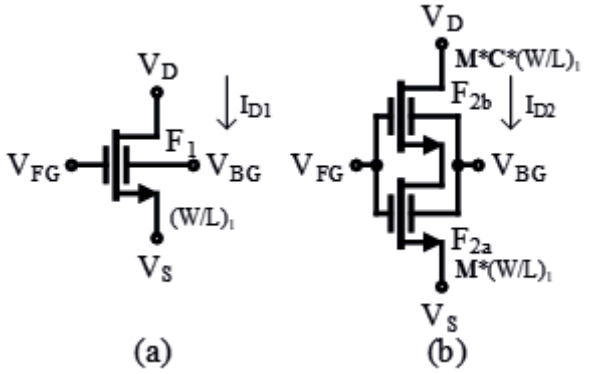

Figure 2: a) Single FinFET, b) Self-cascode structure.

enlarges both FinFETs within the self-cascode structure, thereby increasing the current.

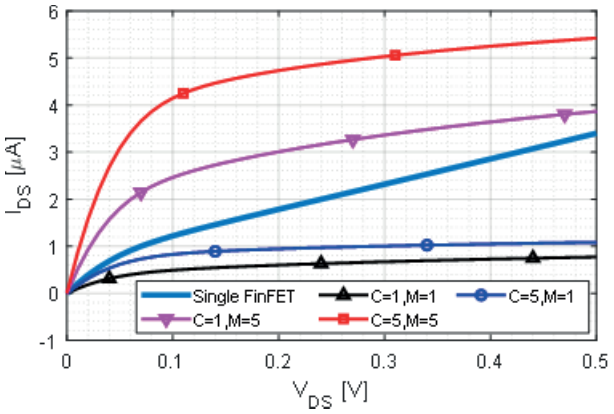

Figure 3: Operational outcomes for both single FinFET and self-cascode structures under various parameters (@V_{FG}=0.5V, @V_{BG}=V_S=GND, W_1/L_1=80nm/64nm).

2.3 Proposed CFC Op-Amp

Fig. 4 illustrates the proposed CFC Op-Amp configuration. The operational amplifier is biased with a DDSB circuit for low power consumption. To enhance input common mode voltage, a CFC is implemented, which consists of parallel-connected self-cascoded FinFETs F_{1Aa}-F_{1Ab}, F_{2Aa}-F_{2Ab} and self-cascoded FinFETs F_{1a}-F_{1b}, F_{2a}-F_{2b} differential input pairs. For the differential input, the current sources are self-cascoded FinFETs F_{3Aa}-F_{3Ab} and F_{3a}-F_{3b}. Instead of a traditional cascode current mirror, a wide-swing cascode current mirror is selected to ensure a broad dynamic range, even at reduced supply voltages [6].

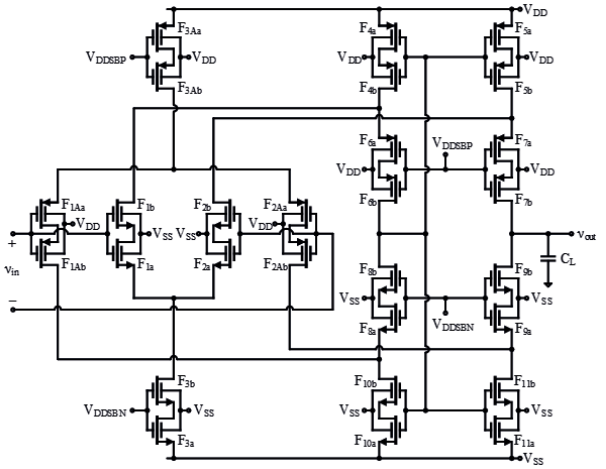

Figure 4: Proposed CFC Op-Amp configuration.

The low-frequency gain of the proposed circuit can be determined by $A_v = g_{mT}R_o$. Here g_{mT} is the total transconductance of the input stage, which is given in (2).

$$g_{mT} = g_{mN} + g_{mP} = g_{m(2a-2b)} + g_{m(2Aa-2Ab)} \quad (2)$$

The output resistance, R_o, which indicates the small-signal resistance seen from the drain of F_{7a}-F_{7b} and F_{9a}-F_{9b}, can be calculated using the parallel combination of (3a) and (3b) [6, 12].

$$R_{oN} = g_{m(9a-9b)} r_{o(9a-9b)} \left[r_{o(2Aa-2Ab)} r_{o(11a-11b)} \right] \quad (3a)$$

$$R_{oP} = g_{m(7a-7b)} r_{o(7a-7b)} \left[r_{o(2a-2b)} r_{o(5a-5b)} \right] \quad (3b)$$

Fig. 5 illustrates the configuration of the DDSB. In the circuit, the initial group of FinFETs F_{B1}-F_{B4} manages the activation state of self-cascoded current source (i.e., F_{3Aa}-F_{3Ab}) and self-cascoded FinFETs F_{6a}-F_{6b}, F_{7a}-F_{7b} within the CFC Op-Amp by regulating the bias voltage V_{DDSBP}. This modulation spans approximately –160mV to 320mV and is achieved through a designated control pulse, ϕ_{BP}. Similarly, the subsequent group F_{B5}-F_{B8} oversees the activation status of self-cascoded current source (i.e., F_{3a}-F_{3b}) and self-cascoded FinFETs F_{8a}-F_{8b}, F_{9a}-F_{9b} by adjusting the bias voltage V_{DDSBN} within a range of approximately –120mV to –380mV, controlled by pulse designated as Φ_{BN}.

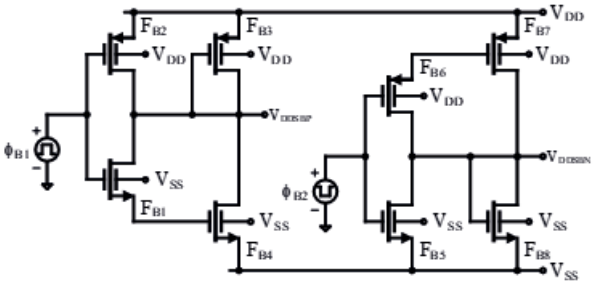

Figure 5: Configuration of the DDSB [2].

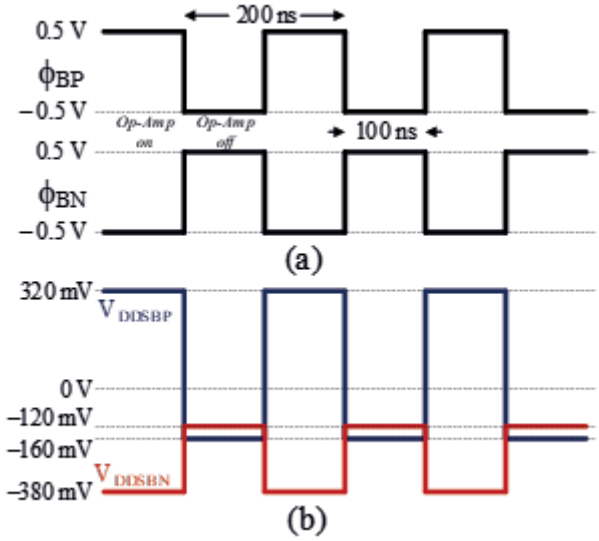

Figure 6: a) Operation waveforms of the DDSB clocks, b) DDSB outputs.

The operating waveforms of DDSB clocks are depicted in Fig. 6a, while the output voltages are shown in Fig. 6b. As indicated by their shape, the Op-Amp is designed to turn off at 100ns and then turn on again simultaneously. This integration helps mitigate side effects and provides better stability with low power consumption [2] for the proposed Op-Amp. The transistor dimensions utilized in the DDSB CFC Op-Amp are provided in Table 1.

Table 1: Transistors' aspect ratios.

FET	W/L (nm/nm)	FET	W/L (nm/nm)
F_{1Aa}	(1520*M)/64	F_{7a}	(800*M)/64
F_{1Ab}	(1520*M*C)/64	F_{7b}	(800*M*C)/64
F_{1a}	(1520*M)/64	F_{8a}	(450*M)/64
F_{1b}	(1520*M*C)/64	F_{8b}	(450*M*C)/64
F_{2Aa}	(1520*M)/64	F_{9a}	(450*M)/64
F_{2Ab}	(1520*M*C)/64	F_{9b}	(450*M*C)/64
F_{2a}	(1520*M)/64	F_{10a}	(500*M)/64
F_{2b}	(1520*M*C)/64	F_{10b}	(500*M*C)/64
F_{3Aa}	(420*M)/64	F_{11a}	(500*M)/64
F_{3Ab}	(420*M*C)/64	F_{11b}	(500*M*C)/64
F_{3a}	(650*M)/64	F_{B1}	200/64
F_{3b}	(650*M*C)/64	F_{B2}	200/64
F_{4a}	(500*M)/64	F_{B3}	64/64
F_{4b}	(500*M*C)/64	F_{B4}	180/64
F_{5a}	(500*M*C)/64	F_{B5}	250/64
F_{5b}	(500*M*C)/64	F_{B6}	80/64
F_{6a}	(800*M*C)/64	F_{B7}	200/64
F_{6b}	(800*M*C)/64	F_{B8}	300/64

M: Multiplier, C: Composit

2.4 Simulation results

The performance of the DDSB CFC Op-Amp was evaluated through simulations using the LTspice software. Increasing the C value results in elevated output resistances, as depicted in Fig. 3, subsequently boosting the circuit's gain. Likewise, increasing the M value enlarges both FinFETs within the self-cascode structure, thereby raising the current and consequently expanding the bandwidth. Thanks to the stability maintained by DDSB, this structure proposed in the paper enables the design to be tailored to different purposes and needs. It is important to note that increasing the values of C and M enhances the circuit's performance, but it also leads to an increase in layout size and power dissipation. For C=5 and M=5, the results reveal a gain of 44.88dB, a bandwidth of 42.1kHz, a Unity Gain Frequency (UGW) of 77.45MHz, and a phase margin of 87.8° with 5pF load capacitance. The AC response of the circuit for four different scenarios, based on variations in C and M, is illustrated in Fig. 7. The circuit's Common-Mode Rejection Ratio (CMRR) and comprehensive input-referred noise characteristics across a wide frequency band are presented in Fig. 8. When the parameters are set to C=1 and M=1, the CMRR reaches 50.62dB. Noise analysis at these dimensions indicates that the circuit exhibits input noise voltage densities of 3.6μV/√Hz at 100Hz and 161.5nV/√Hz at 1MHz. Specifically, the input-referred noise voltage density increases with the rise in the C coefficient, while it decreases with the increase in the M coefficient at frequencies close to DC. By analyzing the frequency response diagrams for voltage gain, phase margin, CMRR, and noise, as shown in Figs. 7 and 8, the performance of the designed amplifier for different values of C and M is compared in Table 2.

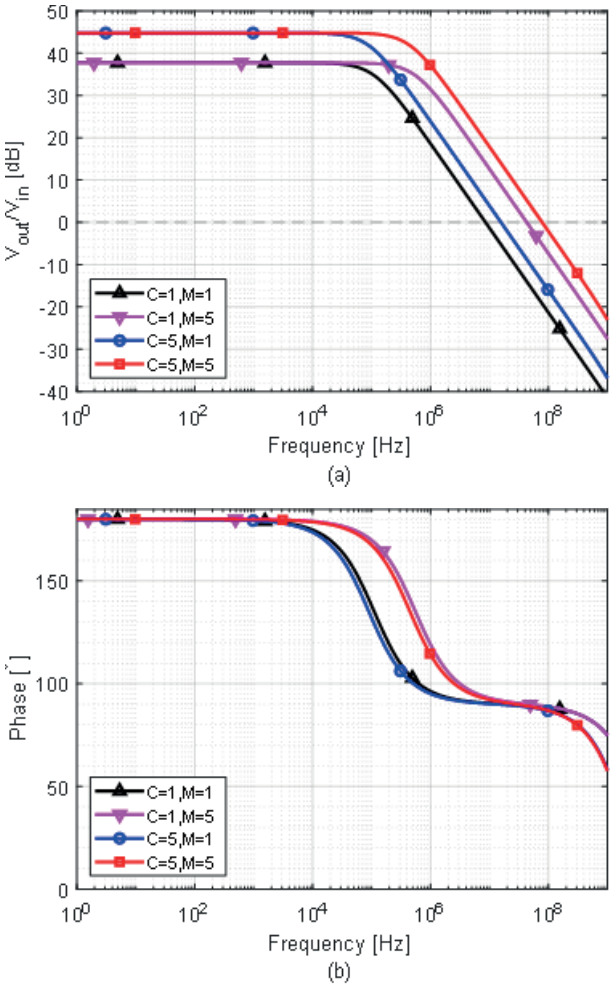

Figure 7: AC response of proposed Op-Amp: a) gain, b) phase.

Figure 9 illustrates the variation in the Gain-Phase characteristics of the circuit with respect to C_L and temperature. In Figure 9a, it is observed that for C=1 and M=1, increasing C_L from 0.5pF to 5pF results in a UGW of 87.1MHz with a load of 0.5pF, maintaining stability with a phase margin of 89.4°. Further analysis shows that

with C_L=10fF, the circuit achieves a UGW of 3.19GHz and a phase margin of 44.93°. When the parameters are set to C=5 and M=5, the circuit remains stable up to a load capacitance of approximately 220fF, providing a UGW of 1.38GHz and a phase margin of 45.5° for this load. The frequency response of the Op-Amp was analyzed over a wide temperature range from -40°C to 100°C, with simulations conducted at 20°C intervals as depicted in Fig. 9b. Under the conditions of C=1 and M=1, the gain and phase characteristics at -40°C are 39.8dB and 90.5°, respectively, while at 100°C they are 34.2dB and 90.1°. This indicates that the small-sized Op-Amp exhibits low sensitivity to thermal variations. This stability across the temperature range decreases as the Op-Amp size is increased.

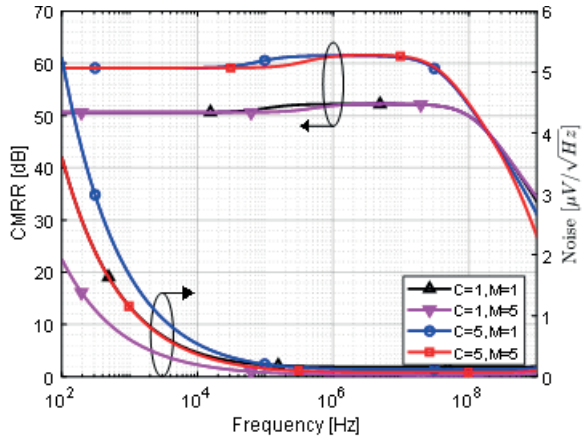

Figure 8: CMRR and input referred noise performance results of the proposed Op-Amp.

In this paper, the slew rate (SR) was determined by using an 800mV peak-to-peak input (–400mV to 400mV) employing a 10-90% threshold. Fig. 10 shows the step response of the Op-Amp under varying load capacitances (CL) from 1 pF to 5 pF. The simulation results indicate that the circuit provides a stable output due

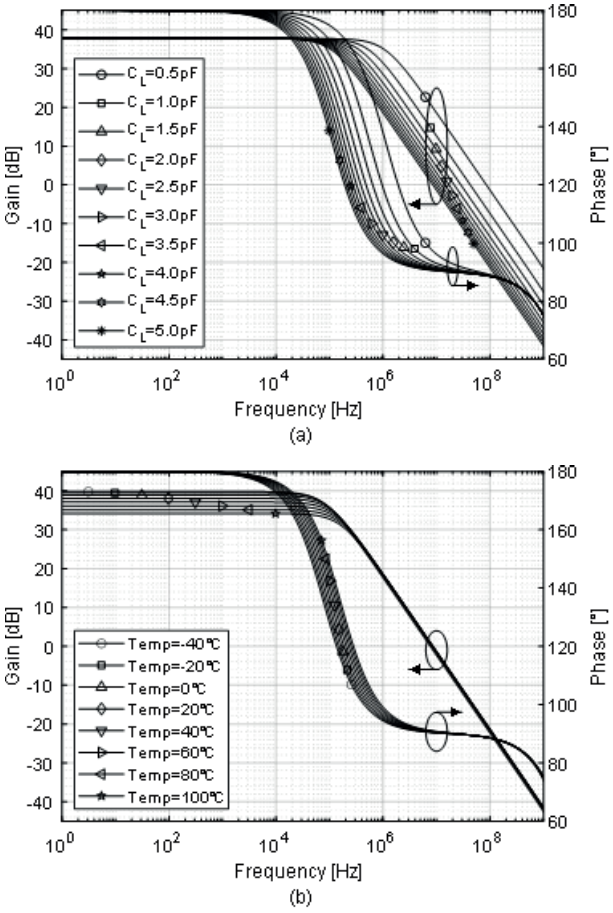

Figure 9: Gain-phase response variation (@C=1, M=1): a) with C_L, b) with temperature.

to the high phase margin. The fluctuations in the transition band are caused by the operation of the DDSB, which continuously switches the circuit on and off. This behavior is also observed during rising and falling transitions and presents a disadvantage by reducing the SR. For a 1pF load capacitor, the measured

Table 2: Performances of the DDSB CFC Op-Amp.

Parameters	Unit	C=1 M=1	C=5 M=1	C=1 M=5	C=5 M=5
Open Loop Gain (DC)	dB	37.42	44.80	37.72	44.88
Phase Margin	°	90.66	89.85	90.10	87.8
UGW	MHz	8.46	14.82	43.15	77.45
CMRR	dB	50.62	59.16	50.61	59.13
Input Ref. Noise (a/b)	$\frac{nV}{\sqrt{Hz}}$	3607/161.5	5246/128.9	1930/36.4	3605/79.4
Output Ref. Noise (a/b)	$\frac{\mu V}{\sqrt{Hz}}$	277.6/1.37	912.4/2.01	148.6/1.36	627/ 5.66
Power Dis.	mW	0.083	0.097	0.179	0.246

CL=5pF, (a): @100Hz, (b): @1MHz

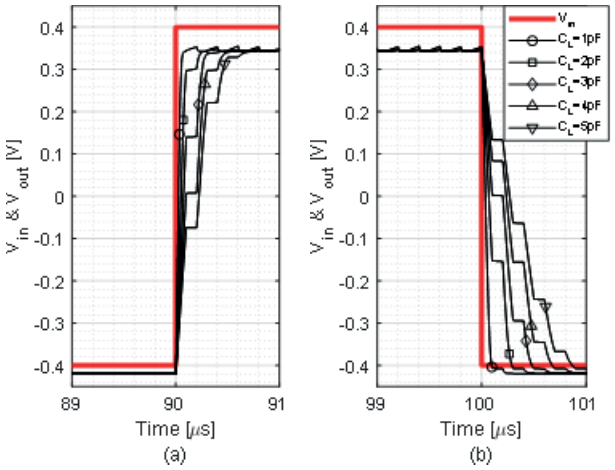

Figure 10: Step response of proposed Op-Amp for C=1, M=1: a) SR^+ b) SR^-.

SR^+ (SR^-) is 12.8 (9.3)V/μs for C=1, M=1, while for C=5, M=5, it increases to 97 (68.6)V/μs. When C_L is increased to 5pF, the SR^+ (SR^-) values decrease to 2.41 (1)V/μs for C=1, M=1, and to 32.2 (14.3)V/μs for C=5, M=5.

Monte Carlo (MC) analysis, conducted in LTspice over 50 iterations, investigated the impact of three key parameters on the circuit's performance: threshold voltage (V_{TH}), oxide thickness (t_{ox}), and supply voltages (V_{DD}, V_{SS}). The analyses are provided insight into how minor deviations in these parameters influence the overall behavior and stability of the circuit. The results are depicted in the Fig. 11 for C=1 and M=1.

Table 3 compares Op-Amps from the literature using CMOS and FinFET technologies with the proposed DDSB CFC Op-Amp configurations (@C=1, M=1 and @C=5, M=5). To facilitate a comparison of truly low-power structures, the two Figures of Merit (FoM1,2), as utilized in [13], have been employed regarding small-signal and large-signal power.

$$FoM_1 = \frac{GBW \cdot C_L}{P_{diss}} \tag{4a}$$

$$FoM_2 = \frac{SR_a \cdot C_L}{P_{diss}} \tag{4b}$$

Where SRa=(SR^++SR^-)/2 represents the average value of slew rates of rising and falling edges of the output. It should be noted that FoM_1 and FoM_2 relate small-signal gain bandwidth and slew rate to dissipation power.

When comparing the data in Table 3, it can be observed that the proposed circuit (C=5, M=5) outperforms other published circuits in terms of FoM1, providing 1574(MHz·pF)/mW. Regarding FoM2, the value of 1440(V·pF)/(μs·mW) from reference [14] stands out. The advantage of this study lies in its design, which includes a slew rate enhancement block aimed at achieving a high slew rate. However, the low phase margin value of 48.2° achieved by this circuit with 8pF load capacitance is a significant factor, and the likelihood of unstable operation increases with lower capacitive loads.

3 SC integrator application

Switched capacitor (SC) circuits are fundamental components in the construction of integrated circuits that

Table 3: Performance comparison of proposed Op-Amp with literature.

Performance Parameters	Unit	This Work(2)	This Work(3)	[2]	[6]	[14]	[15]	[16]	[17]
Process	N/A	32 nm (FinFET)	32 nm (FinFET)	1 μm (CMOS)	0.6 μm (CMOS)	0.18 μm (CMOS)	20 nm (FinFET)	55nm (FinFET)	45nm (FinFET)
Power Supply	V	±0.5	±0.5	±1.5	1.8	1.8	±0.5	1	1
Power Dissipation	mW	0.083	0.246	9.2	0.24	1.18	0.377	0.648	0.175
CL	pF	5	5	10	20	8	3	3	0.02
Open Loop Gain (DC)	dB	37.42	44.8	47.7	80.8	68	39.27	45.51	29.22
GBW	MHz	8.46	77.45	14.3	6.9	172.5	8.26	63	5.1
Phase Margin	°	90.66	87.8	47.9	71	48.2	45.05	60.1	90
Slew Rate (SR+/SR–)(1)	V/μs	2.41/1	32.2/ 14.3	106	2.2	212.5	2.3	41.34	1830/ 1120
FoM1	$\frac{MHz \cdot pF}{mW}$	509.64	1574	15.54	575	1169	65.72	291.66	0.582
FoM2	$\frac{V \cdot pF}{\mu s \cdot mW}$	103.01	472.56	115.21	183.33	1440	18.30	191.38	168.57

(1): For articles with a single SR, SRa=SR was considered, (2): C=1, M=1, (3): C=5, M=5.

find extensive application in a variety of domains, including voltage regulators, filters, and analog-to-digital converters. The principle behind SC circuits involves capacitors' periodic charging and discharging to perform specific signal-processing tasks. A SC circuit comprises a core network of capacitors, switches, and operational amplifiers. Switches control the connection and disconection of capacitors in the circuit and enable charge transfer between them. By opening and closing these switches at precise intervals, the circuit effectively mimics the behavior of resistors or other analog components. The history of SC circuits dates back to the middle of the 20th century, stemming from the need for more efficient analog signal processing methods. SC circuits use discrete components such as relays and mechanical switches to implement switching [18]. As discussed previously, the substitution of a resistor can be achieved by utilizing two FinFETs and a capacitor connected at a single node. The insensitive SC integrator, utilizing FinFETs as shown in Fig. 12An independent, non-overlapping clock signal controls each gate pin of the two FinFETs. This system operates under the assumption that the output is sampled at the conclusion of the ϕ_2 clock phase. Under this assumption, the transfer function of the integrator can be derived as given in (5) [19, 20].

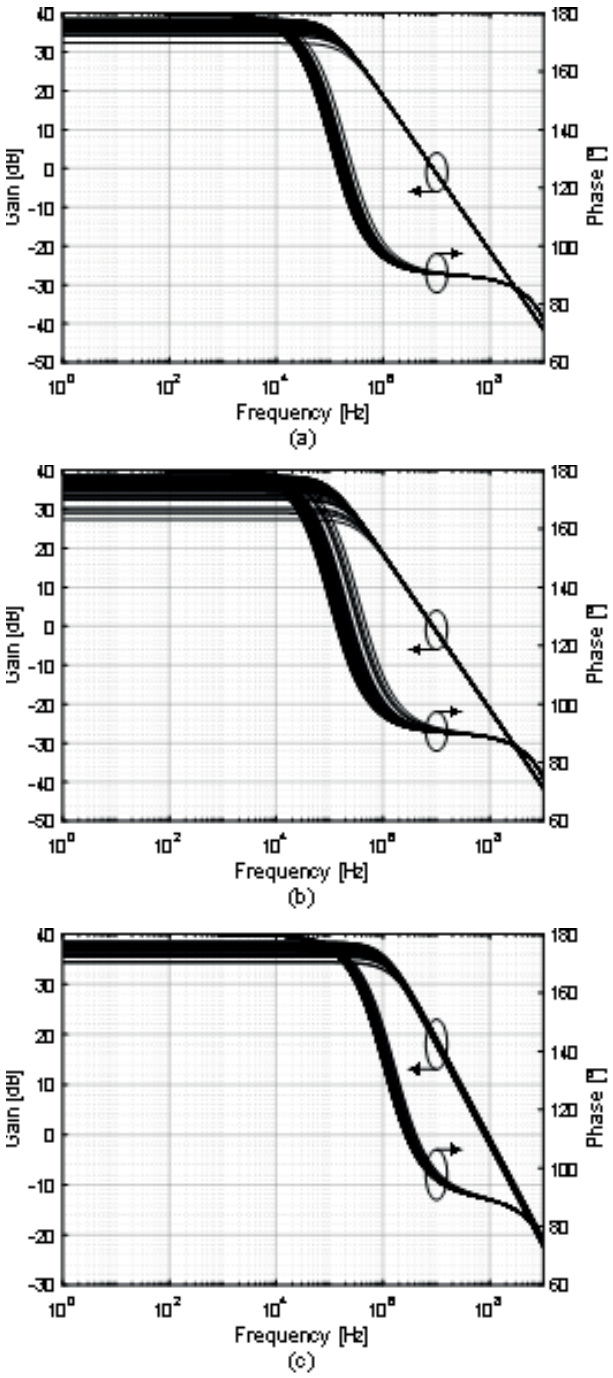

Figure 11: MC Analysis results: a) t_{ox} with 3% variation, b) V_{TH} with 1% variation, c) Power supplies (V_{DD}, V_{SS}) with 5% variation.

$$\frac{v_o}{v_i} = \frac{C_1 / C_2}{j\omega T}\left[\frac{\omega T}{2\sin\left(\frac{\omega T}{2}\right)}\right] \tag{5}$$

Here *T* represents the period of sampling. The operation waveforms of the SC clocks are depicted in Fig. 13.

The total equivalent resistance in the circuit is set to 250kΩ. The capacitors used in the circuit, C_1 and C_2, each have a capacitance of 40pF. The dimensions W and L of the FinFETs were chosen as 80nm and 32nm, respectively. The integrator receives a sinusoidal input signal with a frequency of 3.33kHz and a peak voltage of 50mV. As expected, the output displays a cosine waveform. The analysis of Total Harmonic Distortion (THD) was derived from the 20ms transient response of the integrator. The performance characteristics of SC integrators designed with two different Op-Amp configurations are provided in Table 4. The operating waveforms of the SC integrator designed with C=1 and M=1 Op-Amp are shown in Figure 14.

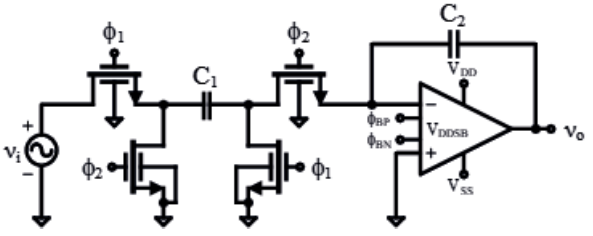

Figure 12: Configuration of the insenstive SC integrator utilizing FinFETs.

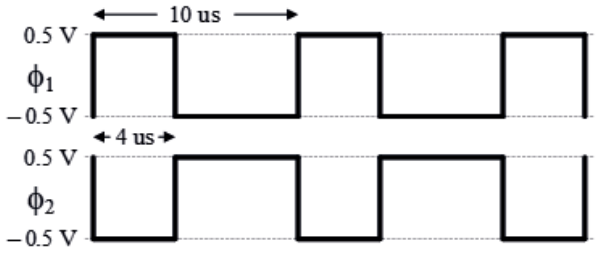

Figure 13: Operation waveforms of the switched capacitor clocks.

Table 4: Performance Comparison of SC Integrators.

Performance parameters	Unit	This Work(1)	This Work(2)
Power Supply Voltages	V	±0.5	±0.5
Switching Frequency	kHz	10	10
Input Signal Amplitude	mV	50	50
$THD_{(fin=3.33\ kHz)}$	N/A	0.336 %	0.251 %

(1): C=1, M=1, (2): C=5, M=5

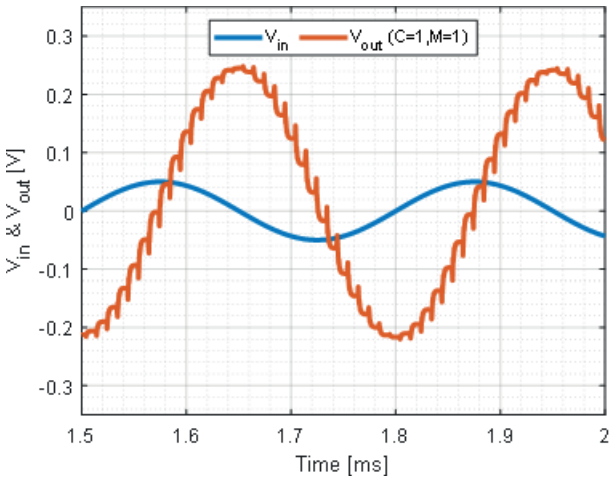

Figure 14: Input and output waveforms of the SC integrator (@C=1, M=1).

4 Conclusions

In this paper, a design of Complementary Folded-Cascode Op-Amp is presented using PTM 32nm FinFET technology. The circuit's stability at low voltages is achieved through the integration of DDSB and wide-swing cascode current mirror topologies. The dimensions of the circuit, parameterized by M and C, can be scaled down to nanoscale dimensions (C=1, M=1) according to application requirements, reducing power consumption to as low as 83µW. In this scenario, it can provide a DC gain of 37.42dB and a bandwidth of 8.46MHz. When C=5, M=5 the circuit simulations demonstrate a superior performance in terms of FoM1. In this case, with its provided 44.8dB voltage gain, 42.1kHz bandwidth, and 246µW power dissipation, it is highly suitable for low-power wide-band signal processing applications.

5 Conflict of Interest

The authors declare no conflict of interest

6 References

1. S. Yan and E. Sanchez-Sinencio, "Low voltage analog circuit design techniques: A tutorial," IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, vol. 83, no. 2, pp. 179-196, 2000.
2. H. Wakaumi, "A Switched-Capacitor Low-Pass Filter with Multiple-Channel Double-DSB OP Amplifiers," in 2021 International Conference on Electronics, Information, and Communication (ICEIC), 2021: IEEE, pp. 1-4.
3. J.-T. Wu, Y.-H. Chang, and K. L. Chang, "1.2 V CMOS switched-capacitor circuits," in 1996 IEEE International Solid-State Circuits Conference. Digest of TEchnical Papers, ISSCC, 1996: IEEE, pp. 388-389.
4. J.-f. Huang, J.-y. Wen, and Y.-j. Lin, "Chip design of a 10-MHz switched capacitor low-pass filter for wireless application," in 2014 Sixth International Conference on Wireless Communications and Signal Processing (WCSP), 2014: IEEE, pp. 1-5.
5. S. Rajput and S. S. Jamuar, "Low voltage analog circuit design techniques," IEEE Circuits and Systems Magazine, vol. 2, no. 1, pp. 24-42, 2002.
6. B. Song, O. Kwon, I. Chang, H. Song, and K. Kwack, "A 1.8 V self-biased complementary folded cascode amplifier," in AP-ASIC'99. First IEEE Asia Pacific Conference on ASICs (Cat. No. 99EX360), 1999: IEEE, pp. 63-65.
7. D. Hisamoto et al., "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," IEEE transactions on electron devices, vol. 47, no. 12, pp. 2320-2325, 2000.
8. N. Liao et al., "Low power adiabatic logic based on FinFETs," Science China Information Sciences, vol. 57, pp. 1-13, 02/01 2014, https://doi.org/10.1007/s11432-013-4902-x.
9. A. Kumar, B. Kaur, and M. Arora, "Evolution of Transistor Technology from BJT to FinFET–A study," in International Conference on Advanced Emerging Technology (ICAET), 2016.
10. S. K. Saha, FinFET devices for VLSI circuits and systems. CRC Press, 2020.

11. S. Kundra, P. Soni, and A. Kundra, "Low power folded cascode OTA," International Journal of VLSI design & Communication Systems, vol. 3, no. 1, p. 127, 2012.
12. B. Razavi, Design of analog CMOS integrated circuits. 2005.
13. T. Kulej and F. Khateb, "A 0.3-V 98-dB Rail-to-Rail OTA in 0.18 µm CMOS," IEEE Access, vol. 8, pp. 27459-27467, 2020.
14. J. Kim, S. Song, and J. Roh, "A high slew-rate enhancement class-AB operational transconductance amplifier (OTA) for switched-capacitor (SC) applications," IEEE Access, vol. 8, pp. 226167-226175, 2020.
15. M. Shirazi and A. Hassanzadeh, "Design of a low voltage low power self-biased OTA using independent gate FinFET and PTM models," AEU-International Journal of Electronics and Communications, vol. 82, pp. 136-144, 2017.
16. A. Hassanzadeh and S. Hadidi, "Systematic approach for IG-FinFET amplifier design using gm/Id method," Analog Integrated Circuits and Signal Processing, vol. 109, no. 2, pp. 379-385, 2021, https://doi.org/10.1007/s10470-021-01917-9.
17. R. A. Thakker et al., "A novel architecture for improving slew rate in FinFET-based op-amps and OTAs," Microelectronics Journal, vol. 42, no. 5, pp. 758-765, 2011.
18. T. Tanzawa, "Innovation of switched-capacitor voltage multiplier: Part 2: Fundamentals of the charge pump," IEEE Solid-State Circuits Magazine, vol. 8, no. 2, pp. 83-92, 2016.
19. B. J. Hosticka, R. W. Brodersen, and P. R. Gray, "MOS sampled data recursive filters using switched capacitor integrators," IEEE Journal of Solid-State Circuits, vol. 12, no. 6, pp. 600-608, 1977.
20. K. Martin, "Improved circuits for the realization of switched-capacitor filters," IEEE Transactions on Circuits and Systems, vol. 27, no. 4, pp. 237-244, 1980.

Arrived: 23. 05. 2024
Accepted: 14. 10. 2024

Original scientific paper
https://doi.org/10.33180/InfMIDEM2025.106

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 55, No. 1(2025), 65 – 72

A Low-Power and Low-Noise 4-12 GHz Buck CMOS Low-Noise Amplifier with Current-Reused Technique

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Abstract: In this paper, a wideband fully integrated low-power and low-noise amplifier (LNA) is presented. It features an 8 GHz (from 4 GHz to 12 GHz) bandwidth and an excellent noise figure (NF) using 65 nm CMOS technology. This LNA was designed utilizing a current-reused technique and a cascode gain boost technique. In addition, the interstage inductors use series peaking to reduce the roll-off of high frequency gain and achieve high broadband gain. The proposed LNA circuit achieved high and flat power gain of 23.5±1 dB with input return loss less than -8 dB within the bandwidth of interest (4-12 GHz). The flat NF is 3.3±0.5 dB and the NF_{min} is a staggering 2.8 dB. Achieving the above performance, the third-order input point (IIP3) also reached -10.78 dBm, which is considered excellent. The LNA consumes 6.07 mW from a 1.2 V supply and occupies a layout area of 0.53x0.55 mm^2.

Keywords: low-noise amplifier (LNA); noise figure (NF); Current-reused; CMOS

Ojačevalnik 4-12 GHz CMOS z nizko porabo energije in nizkim šumom s tehniko ponovne uporabe toka

Izvleček: V članku je predstavljen širokopasovni popolnoma integriran ojačevalnik (LNA) z nizko porabo energije in nizkim šumom. Ima 8 GHz (od 4 GHz do 12 GHz) pasovno širino in odlično šumno število (NF) z uporabo 65 nm tehnologije CMOS. LNA ojačevalnik je bil zasnovan z uporabo tehnike ponovne uporabe toka in tehnike kaskodnega povečanja ojačitve. Medstopenjske dušilke uporabljajo zaporedno ojačitev za zmanjšanje visokofrekvenčnega ojačenja in doseganje visokega širokopasovnega ojačenja. Predlagano vezje LNA je doseglo visoko ojačenje 23,5±1 dB z vhodno povratno izgubo, manjšo od -8 dB, znotraj pasovne širine (4-12 GHz). Ravna NF je 3,3±0,5 dB, NF_{min} pa je 2,8 dB. Pri doseganju zgornje zmogljivosti je vhodna točka tretjega reda (IIP3) prav tako dosegla -10,78 dBm. LNA porabi 6,07 mW pri napajanju z napetostjo 1,2 V in zavzema površino 0,53 × 0,55 mm^2.

Ključne besede: ojačevalnik z nizkim šumom (LNA); Vrednost šuma (NF); Ponovna uporaba toka: CMOS

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1 Introduction

With the rapid development of wireless communication, integrated wireless communication chip is widely used in the whole Ball positioning system, Internet of things, smart home, sensor and other industries, has been widely used and has penetrated into thousands of households and brought great and profound changes to the way of human work and life The development of integrated circuits [1-2]. Therefore, the LNA in UWB system has become a research hotspot. Because the performance of the first stage in the only communication system LNA amplifier directly affects the performance of the communication system, high gain and low noise figure become very important. In recent years, CMOS has become the mainstream of RF integrated circuit

How to cite:
J. Liu et al., "A Low-Power and Low-Noise 4-12 GHz Buck CMOS Low-Noise Amplifier with Current-Reused Technique", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 55, No. 1(2025), pp. 65–72

design. Its main advantages are low cost and easy integration [3-5].

As defined by the Federal Communications Commission (FCC), the frequency range 4-12 GHz is considered as UWB applications [6]. The low noise amplifier (LNA) is the first stage of the receiver system, and its performance affects the entire receiver system. Since it receives weak signals from the entire bandwidth range (4–12 GHz) and provides an adequate signal-to-noise ratio for subsequent signal processing, the LNA performance is crucial. If the noise is too large, the signal will be 'submerged' by the noise, thus affecting the performance of the entire receiving system. Therefore, it is critical for the LNA to have a low noise factor (NF), a high and flat power gain, and good input impedance matching performance. Several techniques have recently been proposed for research design of UWB LNA [6-8]. Additionally, with the wide application of UWB, a large number of excellent papers have been reported [9-10]. One of them is in [9], A two-stage LNA based on 90 *nm* CMOS is reported, with the first stage being a current reuse stage and the second stage being a cascode stage. Although a relatively low power consumption of 7.2 *mW* and a flat gain of 12.5 *dB* are achieved, NF 5.2 *dB* and low gain are still unsatisfactory. In [10], this paper reports a single-stage cascode topology fabricated in 0.13 *um* CMOS. Although the gain is relatively flat, it is too low to be acceptable for processing weak signals. What is more unsatisfactory is that only 4.25±0.4 *dB* NF is achieved with 30 *mW* power consumption.

In the process of analog integrated circuit design, designers need to follow the octagon principle of circuit design, and need to make a compromise between noise and gain, power consumption and matching, which requires constant debugging to achieve optimal performance. In order to compensate for the shortcomings of previous reports, this paper uses a two-stage topology. The first stage uses a Complementary common source stage and uses negative feedback to reduce gain sensitivity, the second stage uses a cascode stage to compensate for the lack of gain, and uses an inducer parallel peaking between stages to make up for the roll off of high-frequency gain. At the same time, the current multiplexing technology is used to effectively utilize the current to achieve low power design of the LNA, and all MOS are operating in the saturation region to achieve excellent performance.

The paper is structured as follows. The section 2 mainly focuses on circuit signal analysis including but not only input impedance and gain analysis. How do conventional structured small-signal analysis and matching devices affect input matching and noise figure. Section 3 introduces the proposed wideband LNA and the design process and current-reused technique. Section 4 is mainly devoted to the simulation results of the key indicators of LNA under different process voltage temperature (PVT). Finally, Section 5 draws the conclusions.

2 Circuit basic principle analysis

In the circuit design process, the designer may use the traditional common source stage as the first stage of the LNA. This is because the input matching and noise matching can be achieved by adding peripheral devices. Figure. 1(a) and Figure. 1(b) respectively are the traditional common source stage schematic diagram and small signal equivalent circuit whose gain expression is as follows:

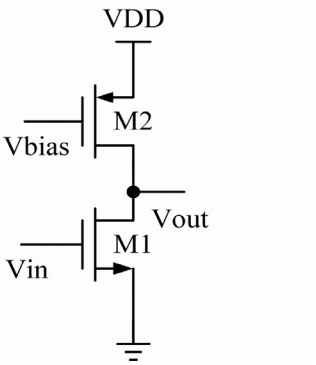

Figure 1(a): Common source stage circuit diagram.

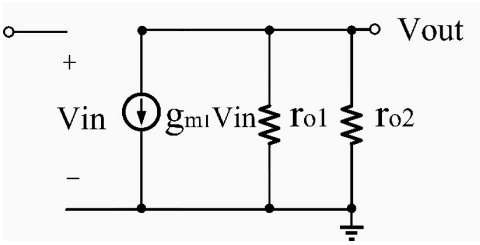

Figure 1(b): Common source stage small signal equivalent circuit.

$$A_V = -g_{m1}(r_{o1} \parallel r_{o2}) \tag{1}$$

Where gm_1 is the transconductance of the input transistor M_1, r_{o1} and r_{o2} are the small-signal equivalent resistances of the input transistor (M_1) and the current source transistor (M_2), respectively. From the gain expression, it can be seen that the traditional common source stage can improve the gain by increasing the small signal resistance, which is related to the current. Therefore, the small current can achieve high gain but will bring large noise, which is not consistent with the characteristics of LNA itself. Figure. 2(a) illustrates the noise equivalent circuit for noise analysis. The noise equivalent to the input is given by Expression (2) as follows:

$$\overline{V_{n,in}^2} = 4kT\gamma\left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2}\right) \quad (2)$$

Figure 2(a): Common source stage noise equivalent circuit.

Here k is Boltzmann's constant, T is the temperature and is the noise factor of the MOSFET. By observing Expression 2, it is not difficult to find that only the transconductance of gm_1 is small to achieve relatively low noise, The expression for g is given by (3) as follows:

$$g_m = \sqrt{2I\mu c_{ox}\frac{W}{L}\left(V_{gs} - V_{th}\right)} \quad (3)$$

Through expression (3), it can be proved that g_m will become smaller when the current decreases, and through expression (2), it is not difficult to find that the noise will become larger, which means that too small current will bring relatively large noise. Here μ and C_{ox} are the mobility and gate oxide capacitance of the MOSFET, V_{gs} and V_{th} are the gate-source voltage and threshold voltage of the MOSFET and $\frac{W}{L}$ is the aspect ratio usually determined by the designer.

The first stage of this paper adopts the complementary common source stage and the following is the principle analysis. Figure. 2(b) shows the first level circuit schematic diagram and Figure. 3(a) is the calculation of its input equivalent circuit used as the input impedance.

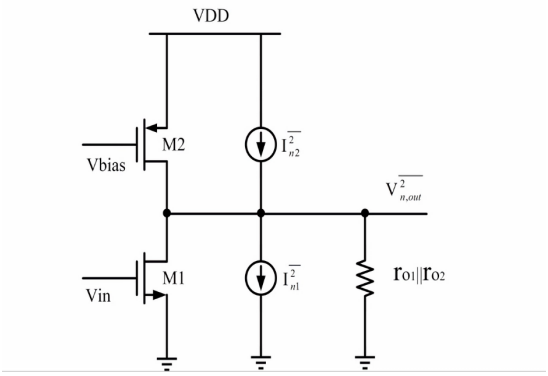

Figure 2(b): The first level of a circuit schematic.

The proposed of the LNA input impedance of the small-signal equivalent circuit according to Figure. 3(a) can be proved by Expression 3 as follows:

$$Z_{in} = \frac{s^2R_1C_{gs1}L_1 + R_1 + s^2C_1}{s^3R_1C_{gs2}C_{gs1}L_1 + s^2L_1C_{gs1} + sR_1\left(C_{gs1} + C_{gs2}\right) + 1} \quad (4)$$

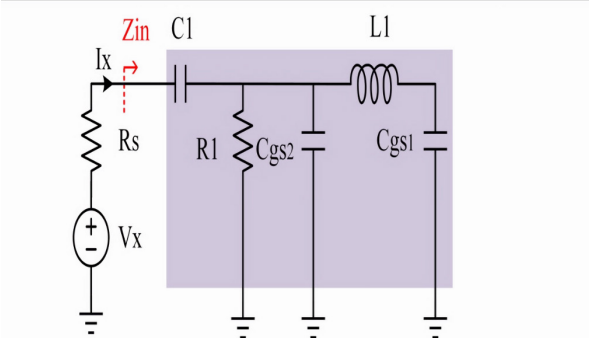

Figure 3(a): Input equivalent circuit of the LNA first stage.

Here are all the equivalent resistances seen by the node in Figure. 3(a), C_{gs1} and C_{gs2} are the MOSEFET gate-source parasitic capacitors of M_1 and M_2, respectively. Figure. 3(b) is the equivalent circuit of the first stage to analyze the gain of the first stage circuit, whose gain can be given by the following expression (5) by calculation.

$$A_{v1} = \frac{V_{out}}{V_{in}} = \frac{1 - g_mR_1 + s^2L_1\left(1 - g_{m1}R_1\right)}{\left(1 + s^2L_1\right)\left(1 + sR_1\right)} \quad (5)$$

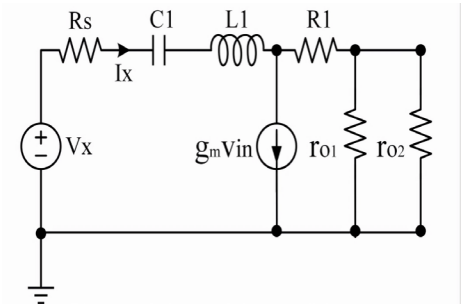

Figure 3(b): The first-stage small-signal equivalent circuit is used for gain analysis.

In order to maximize the transmission power of the receiving antenna, the LNA needs to design 50-ohm impedance matching. Figure. 4(a) shows the process of impedance matching. The matching process can be clearly seen from the Smith circle diagram. When the capacitor C_1 is added, the radius of the impedance circle is continuously reduced, as shown by the blue arrow in Figure. 4(a). When the inductor L_1 is added, the impedance curve is close to the center of the 50-ohm point circle, as shown by the green curve in the figure. The final circuit input impedance matching is shown by the red curve in the figure, achieving a good input matching.

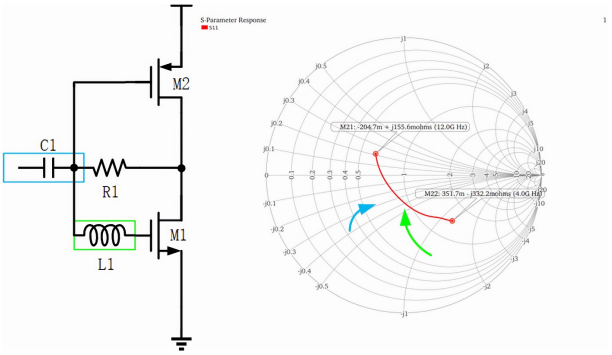

Figure 4(a): Smith Chart of impedance matching process.

3 Circuit design

With the continuous development of 5G millimeter-wave technology, the working frequency band is becoming higher, and the process requirements are also increasing. This demands MOSFETs with a higher cutoff frequency (f_t), faster speeds, and greater carrier mobility. After comprehensive consideration, this paper uses 65 *nm* CMOS technology to design a two-stage LNA applied to ultra-wide system, as shown in Figure. 4(b). The first stage uses a complementary common source stage which has a higher gain than the traditional common source stage. Because the first stage uses a feedback resistor to reduce the gain sensitivity, at the same time, it matched the noise with L1 to reduce the noise of the first stage, the second stage still uses a high gain cascode stage to improve the gain. The cascode stage not only has high gain but also has excellent input-output isolation characteristics which improve the isolation performance of the circuit. In essence, excellent isolation is achieved by negative feedback. When the output of M_4 fluctuates, it will also produce the same fluctuation at its source, which will cause the gate-source voltage of M_4 to change. Where to control the drain current. Therefore, the designed LNA achieves high gain and high linearity without passing through. Current reuse is reflected in the fact that the DC current flowing through M_4 and M_2 is multiplexed by M_1 and M_3 respectively so that no additional drive current is required to achieve lower power consumption.

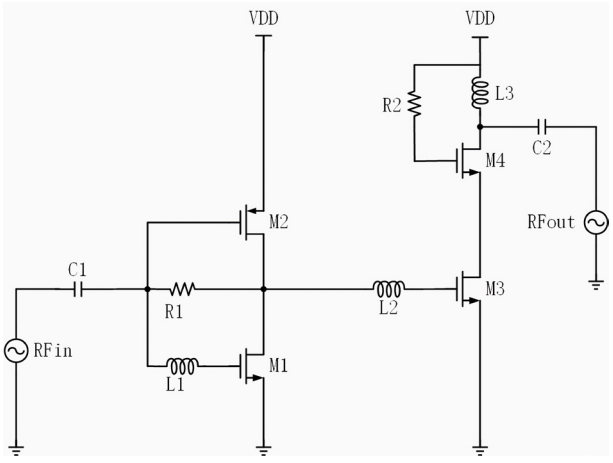

Figure 4(b): The Schematic of the proposed UWB LNA.

The wideband matching is not only reflected in the input impedance matching, but also in the frequency band of interest to avoid the attenuation of gain. In this paper, an inductor L_2 is added between the two stages. Using series inductive peaking can prevent the bandwidth degradation caused by the parasitic capacitor C_{gs3}, which is brought about by the large transistor M_3. By selecting a suitable inductance value for L_2 and resonating with the parasitic capacitance of the M_3 transistor, the high-frequency gain can be improved, and the bandwidth can be expanded. At the same time, the noise matching with the second stage can be realized to ensure the low noise characteristics of the LNA. Figure. 5 (a) shows that the LNA designed in this paper simultaneously achieves high and flat power gain and excellent noise characteristics within the frequency band of interest. In order to verify the effect of interstage inductance L_2, Figure 5(b) shows the results with and without series inductive peaking. It can be seen from Figure 5(b) that, with the series inductive peaking, the gain at the higher frequency increases from 12.4 *dB* to 23 *dB*, and the overall increase is nearly 11 *dB*. When there is no interstage inductance L_2, the gain will be greatly reduced in the high frequency part, which is the result we do not want to see. Therefore, the final choice of L_2 is equal to 2 *nH*. The former inductor L_3 and capacitor C_2 are designed to resonate with the parasitic capacitance of the leakage end of M_4 to achieve output matching, while the latter is a direct isolating capacitor to avoid the current of V_{DD} flowing to the output end of the amplifier.

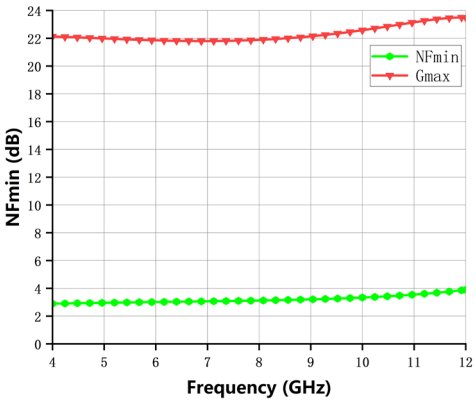

Figure 5(a): Verification of high and flat maximum gain and excellent noise characteristics in the frequency band of Interest.

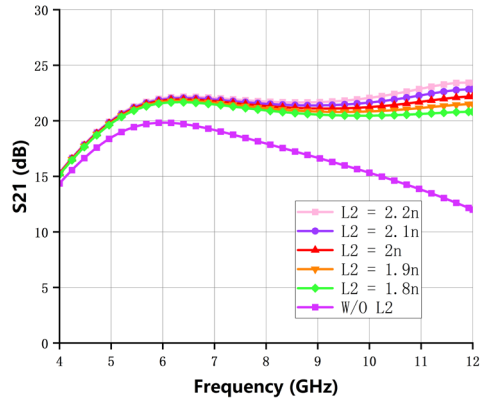

Figure 5(b): Comparison of simulation results of with or without inducer.

4 Performance summary

The proposed UWB LNA design has been implemented in 65 *nm* CMOS process, verified in Cadence Virtuoso platform, post-layout simulation of parasitic parameters extracted by Cadence Calibre, and imitation of netlist after import in Cadence Virtuoso, Figure. 6(a) shows the layout of the proposed LNA.

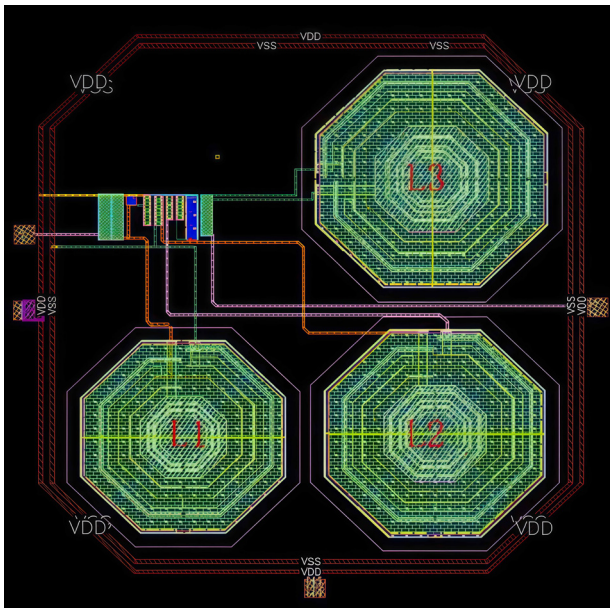

Figure 6(a): Layout of the proposed LNA

Figure. 6(b) shows the simulation results of the reflection coefficient of input return loss under different temperatures, different voltages and different process angles (PVT). The reflection coefficient of ff process Angle is the smallest and S11 is less than -10 *dB* in almost the whole frequency band. The minimum value of S11 is about -12 *dB*. Meet the impedance matching requirements. The simulation results of the UWB LNA under PVT conditions are illustrated in Figure. 7(a). The peak gain of 27 *dB* demonstrates exceptional performance compared to other published papers [11-16], while maintaining excellent S21 gain flatness across the entire UWB range with a minimal fluctuation range of only 1 *dB*. This characteristic enables effective amplification of in-band RF signals. Furthermore, even under the worst process angle (ss), it achieves a high gain ranging from 14-20 *dB*.

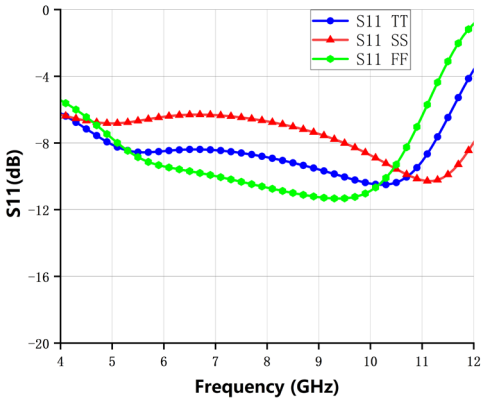

Figure 6(b): Simulated S_{11}.

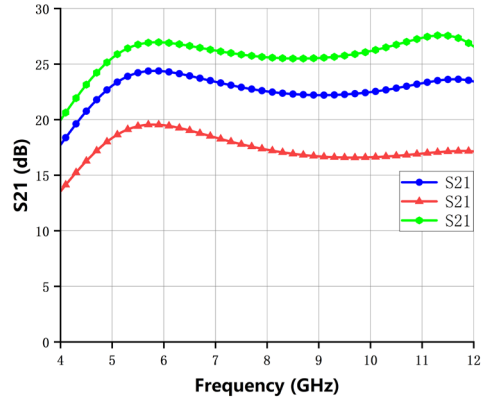

Figure 7(a): Simulated S_{21}.

The simulation curve of input-output isolation under PVT is depicted in Figure. 7(b). The reverse isolation exhibits a gradual increase across the entire frequency range, yet remains below -20 *dB*. within the UWB band. Notably, the reverse isolation index remains consistent across all three corners, indicating excellent performance of the UWB LN. Figure. 8(a) shows the noise characteristics of the proposed LNA. In the communication system, the LNA needs to deal with the energy from the antenna, so the output signal of the LNA is required to have a high enough signal-to-noise ratio NF to measure its performance. The proposed LNA exhibits an amazing 2 *dB* NF and achieves lower than 4 *dB*. NF over the entire frequency band even in the worst case, which is a very excellent result. The simulation results in Figure. 8(b) depict the third-order intermodulation

curve, which serves as an indicator of the linearity of UWB. Distortion arises from poor linearity in the output signal of an LNA, consequently leading to subpar performance of the entire communication system. In comparison with other research papers, this paper LNA exhibits exceptional linearity at approximately -10.78 *dBm* [17-19].

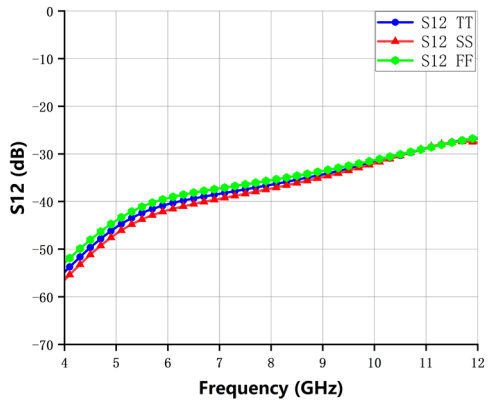

Figure 7(b): Simulated S_{21}.

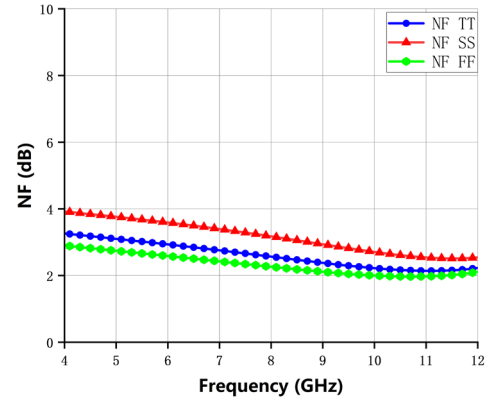

Figure 8(a): Simulated NF.

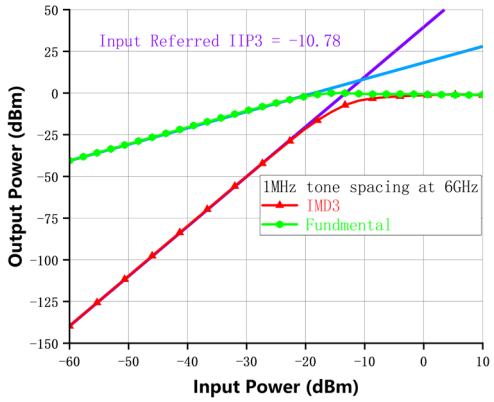

Figure 8(b): IIP3 of the proposed LNA

Figure. 9（a）shows the simulation results of the mismatch of NF. In the case of running 200 points, the mismatch of NF is very small and can almost be ignored. One value is 61 *m* and values are only 180 *m*, reflecting that the random mismatch of the device has very little influence on the LNA NF. The simulation results of S11 in Figure. 9(b) demonstrate a small mismatch ratio when running 200 points, primarily distributed around -8 *dB*. The value of one is 470 *m*, and the value of mismatch 1.4, indicating that the random device mismatch has a relatively negligible impact on the S11 performance of LNA. Its deviation remains within an acceptable range without affecting the overall UWB performance. Figure. 10(a) shows the simulated mismatch results for S21 gain. In the case of running 200 points, the mismatch of S12 is relatively small, with a value of 1, as the mismatch mainly concentrates on the gain greater than 23 *dB*. Even if there is a little mismatch, it is only a few points that have a minimal impact on the performance of the LNA. The minimum gain of the mismatched LNA is also greater than 20 *dB*, indicating that the LNA has excellent performance.

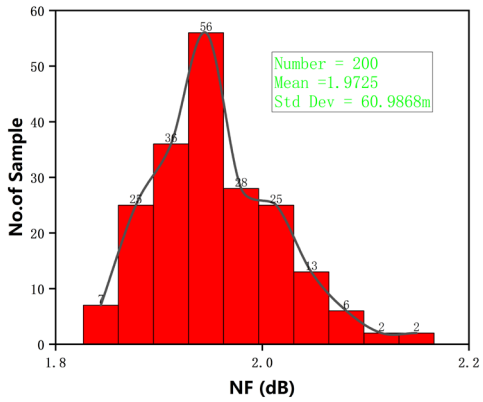

Figure 9(a): Monte Carlo results of NF

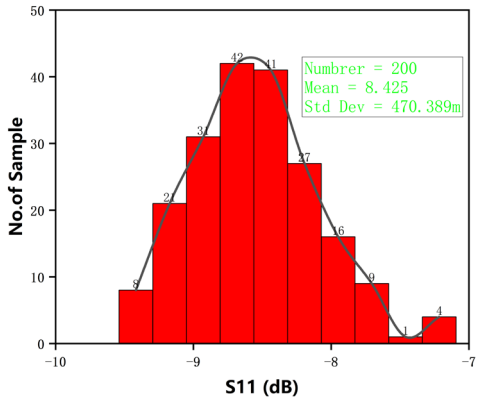

Figure 9(b): Monte Carlo results of S_{11}

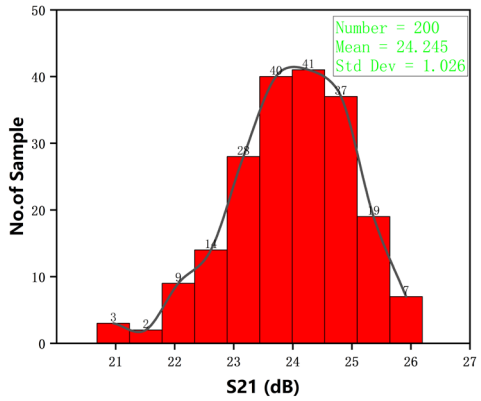

Figure 10(a): Monte Carlo results of S_{21}.

5 Conclusion

This article comprehensively describes the detailed analysis and design ideas of an LNA that adopts a two-stage structure implemented on 65 *nm* CMOS technology. The proposed two-stage LNA uses inter-stage matching to achieve broadband matching and high gain. Most importantly, noise matching is achieved to obtain a low NF, and at the same time, the current-reused technology is used to effectively reduce power consumption. Finally, the Monte Carlo and process-corner simulations confirm that the proposed design is suitable for the UWB system. The proposed LNA achieves a peak gain of 24.7 *dB*, with its 3- *dB* bandwidth ranging from 5 to 12 GHz and an NF of 2.8 *dB* at 11 GHz, while consuming 6.07 *mW* of DC power. The core area of the LNA is optimized to only 0.292 mm^2.

6 Conflict of interest

The authors declared no potential conflict of interest with respect to the research, authorship, and publication of this article.

7 References

1. J. Craninckx et al., "A Fully Reconfigurable Software-Defined Radio Transceiver in 0.13µm CMOS," 2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, San Francisco, CA, USA, 2007, pp. 346-607. https://doi.org/10.1109/ISSCC.2007.373436.
2. M. Brandolini, P. Rossi, D. Manstretta and F. Svelto, "Toward multistandard mobile terminals - fully integrated receivers requirements and architectures," in IEEE Transactions on Microwave Theory and Techniques, vol. 53, no. 3, pp. 1026-1038, March 2005. https://doi.org/10.1109/TMTT.2005.843505.
3. W. Wu, O. Novak, C. T. Charles and X. Fan, "A low-power 3.1–5GHz ultra-wideband low noise amplifier utilizing Miller Effect," 2009 IEEE International Conference on Ultra-Wideband, Vancouver, BC, Canada, 2009, pp. 255-259. https://doi.org/10.1109/ICUWB.2009.5288712.
4. R. -M. Weng, C. -Y. Liu and P. -C. Lin, "A Low-Power Full-Band Low-Noise Amplifier for Ultra-Wideband Receivers," in IEEE Transactions on Microwave Theory and Techniques, vol. 58, no. 8, pp. 2077-2083, Aug. 2010. https://doi.org/10.1109/TMTT.2010.2052404.
5. N. Li, W. Feng and X. Li, "A CMOS 3–12-GHz Ultrawideband Low Noise Amplifier by Dual-Resonance Network," in IEEE Microwave and Wireless Components Letters, vol. 27, no. 4, pp. 383-385, April 2017. https://doi.org/10.1109/LMWC.2017.2679203
6. S. Shekhar, X. Li and D. J. Allstot, "A CMOS 3.1-10.6 GHz UWB LNA employing stagger-compensated series peaking," IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2006, San Francisco, CA, USA, 2006, pp. 4 pp.-. https://doi.org/10.1109/RFIC.2006.1651088
7. P. Qin and Q. Xue, "Design of Wideband LNA Employing Cascaded Complimentary Common Gate

Table 1: Summarized performance and comparison with The-Starte-Of-The-Art.

Ref	Tech (nm)	Freq (GHz)	BW (GHz)	S_{21} (dB)	NF (dB)	Power (mW)	IIP3 (dBm)	Area (mm^2)
[3]	65	3.1-5	NA	13.8-14.6	5.4-6	1.49	-10.5	NA
[5]	130	3-12.3	NA	12-15	4-4.6	8.5	-7	0.86
[14]	180	0.4-10	9.6	12.4	4.4-6.5	12	-6	0.42
[15]	65	26-30	NA	13.68	3.84	11.6	-7.15	0.17
[16]	65	15.8-30.3	14.5	10.2	3.3-5.5	12.4	NA	0.185
[17]	65	0.5-7	NA	16.8	2.87-3.77	11.3	-4.5	0.044
[19]	180	3-10	7	12.2-15.2	2.2-2.4	18	-0.2	0.39
This Work	65	4-12	7	22.5-24.8	2.8-3.8	6.07	-10.78	0.292

and Common Source Stages," in IEEE Microwave and Wireless Components Letters, vol. 27, no. 6, pp. 587-589, June 2017. https://doi.org/10.1109/LMWC.2017.2701300
8. Y. -J. Lin, S. S. H. Hsu, J. -D. Jin and C. Y. Chan, "A 3.1–10.6 GHz Ultra-Wideband CMOS Low Noise Amplifier With Current-Reused Technique," in IEEE Microwave and Wireless Components Letters, vol. 17, no. 3, pp. 232-234, March 2007. https://doi.org/10.1109/LMWC.2006.890503
9. G. Sapone and G. Palmisano, "A 3–10-GHz Low-Power CMOS Low-Noise Amplifier for Ultra-Wideband Communication," in IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 3, pp. 678-686, March 2011. https://doi.org/10.1109/TMTT.2010.2090357
10. G. D. Nguyen, K. Cimino and M. Feng, "A RF CMOS amplifier with optimized gain, noise, linearity and return losses for UWB applications," 2008 IEEE Radio Frequency Integrated Circuits Symposium, Atlanta, GA, USA, 2008, pp. 505-508. https://doi.org/10.1109/RFIC.2008.4561487
11. A. R. A. Kumar, B. D. Sahoo and A. Dutta, "A Wideband 2–5 GHz Noise Canceling Subthreshold Low Noise Amplifier," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 7, pp. 834-838, July 2018. https://doi.org/10.1109/TCSII.2017.2719678
12. W. Wu, O. Novak, C. T. Charles and X. Fan, "A low-power 3.1–5GHz ultra-wideband low noise amplifier utilizing Miller Effect," 2009 IEEE International Conference on Ultra-Wideband, Vancouver, BC, Canada, 2009, pp. 255-259. https://doi.org/10.1109/ICUWB.2009.5288712
13. Chang-Wan Kim, Min-Suk Kang, Phan Tuan Anh, Hoon-Tae Kim and Sang-Gug Lee, "An ultra-wideband CMOS low noise amplifier for 3-5-GHz UWB system," in IEEE Journal of Solid-State Circuits, vol. 40, no. 2, pp. 544-547, Feb. 2005. https://doi.org/10.1109/JSSC.2004.840951
14. K. -H. Chen, J. -H. Lu, B. -J. Chen and S. -I. Liu, "An Ultra-Wide-Band 0.4–10-GHz LNA in 0.18-µm CMOS," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 54, no. 3, pp. 217-221, March 2007. https://doi.org/10.1109/TCSII.2006.886880
15. B. Bae, E. Kim, S. Kim and J. Han, "Dual-Band CMOS Low-Noise Amplifier Employing Transformer-Based Band-Switchable Load for 5G NR FR2 Applications," in IEEE Microwave and Wireless Technology Letters, vol. 33, no. 3, pp. 319-322, March 2023. https://doi.org/10.1109/LMWC.2022.3218001
16. P. Qin and Q. Xue, "Compact Wideband LNA With Gain and Input Matching Bandwidth Extensions by Transformer," in IEEE Microwave and Wireless Components Letters, vol. 27, no. 7, pp. 657-659, July 2017. https://doi.org/10.1109/LMWC.2017.2711524
17. H. Yu, Y. Chen, C. C. Boon, C. Li, P. -I. Mak and R. P. Martins, "A 0.044-mm2 0.5-to-7-GHz Resistor-Plus-Source-Follower-Feedback Noise-Cancelling LNA Achieving a Flat NF of 3.3±0.45 dB," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 1, pp. 71-75, Jan. 2019. https://doi.org/10.1109/TCSII.2018.2833553
18. J. -Y. Hsieh and K. -Y. Lin, "A 0.6-V Low-Power Variable-Gain LNA in 0.18- µ m CMOS Technology," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 1, pp. 23-26, Jan. 2020. https://doi.org/10.1109/TCSII.2019.2902301
19. Y. -S. Lin, C. -C. Wang, G. -L. Lee and C. -C. Chen, "High-Performance Wideband Low-Noise Amplifier Using Enhanced π-Match Input Network," in IEEE Microwave and Wireless Components Letters, vol. 24, no. 3, pp. 200-202, March 2014. https://doi.org/10.1109/LMWC.2013.2293666

Arrived: 09. 08. 2025
Accepted: 19.1 1. 2025

Informacije MIDEM
Journal of Microelectronics,
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Vol. 55, No. 1(2025), 73 – 73

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