SMART INTEGRATED MAGNETIC SENSOR CELL

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Abstract: The paper presents a design approach to an optimized integrated magnetic sensor cell. The cell is optimized for signal to noise ratio and for silicon area. A smart autocalibration is included to provide an output signal insensitive to process parameters variations, temperature variations, aging and stress caused by plastic packaging.

Celica pametnega integriranega magnetnega senzorja

Ključne besede: senzorji magnetni, senzorji pametni, senzorji integrirani, celice senzorske, celice magnetne, HALL elementi integrirani, šum električni, optimizacija šuma, kalibracija lastna, kalibracija občutljivosti

Izvleček: V članku je opisano načrtovanje optimizirane celice integriranega magnetnega senzorja. Celica je optimizirana glede razmerja signal šum in glede silicijeve površine. Pametna lastna kalibracija je vključena tako, da je izhodni signal neodvisen na variacije procesnih parametrov, variacije temperature, na staranje in na vplive pritiska zaradi zapiranja v plastično ohišje.

1 Introduction

Integrated Hall sensors offer very good offset voltage compensation. This is achieved by high frequency spinning of Hall element bias current.

The disadvantage of the Hall element is its relatively low sensitivity and consequently relatively poor signal to noise ratio. An improvement of signal to noise ratio was proposed /1/ by using N equal sensors. The signal to noise ratio is then improved by $\sqrt{N}$. For such optimization, a small silicon area of the sensor and the input amplifier is required.

The sensitivity of Hall sensor is linear function of its bias current. It is also temperature dependent and stress dependent. The stress introduced by packaging is changing both with temperature and time. To achieve the best results it is necessary to introduce a self calibration method.

2 Hall element spinning bias current and front end amplifier block

The aim of the proposed cell is to provide a maximum possible bias current for the given supply voltage. The other requirement is to design a block having a ratiometric sensitivity to the supply voltage. Additionally a design objective is to minimize the required silicon area, without loosing the performance of the block. This requirement is necessary to create a possibility to multiply the cell N times.

The schematic diagram of the described cell is shown in fig. 1.

The bias current of the spinned Hall element is determined simply by the ratio V_{dd}/R_h where V_{dd} is the supply voltage and R_h is the Hall element resistance, assuming that the R_{ON} resistance of the switches is very low compared to R_h.

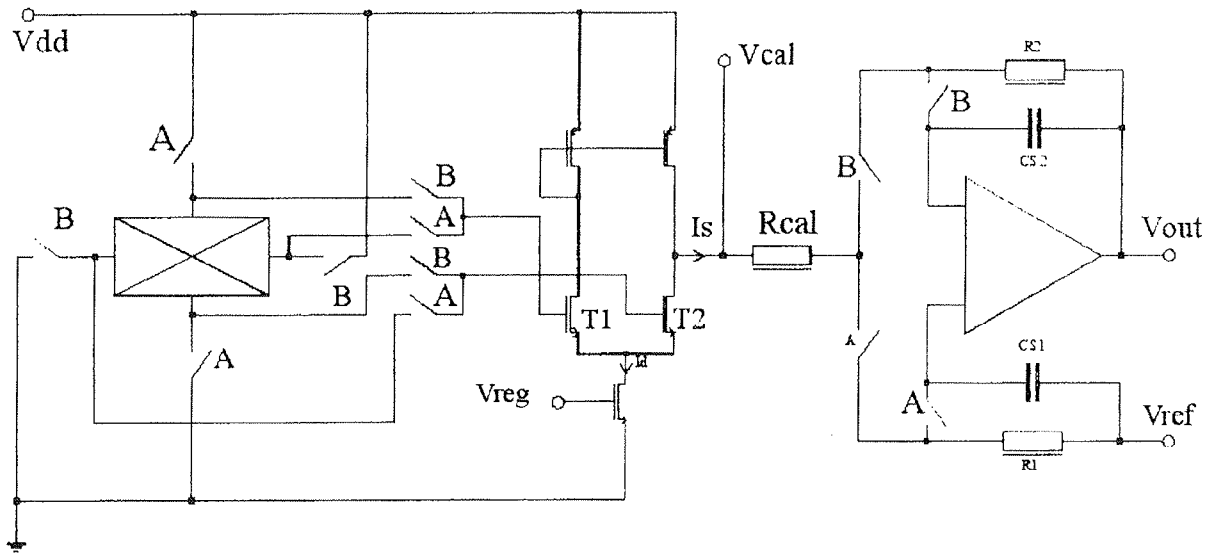

Fig.1: Hall element spinning bias current generation, front end amplifier and connecting amplifier.

The advantage of this approach is that all possible bias current for the given Vdd is flowing through Hall element. This advantage is quite substantial compared to constant bias current. When constant current bias is used it is usually only one third of total available current. This is caused by constant bias current electronic circuit which has to operate under all process corners and temperature variations.

The signal to noise ratio improvement of the proposed schematic is therefore up to three times.

The disadvantage of this approach is the fact that the bias current varies with the temperature coefficient of the well resistance. This temperature coefficient is very high and can not be easily compensated by autocalibration.

This temperature dependence is compensated by the arrangement shown in fig. 1. The resistors R1 and R2 are equal and realized as well resistors, i.e. having the same temperature dependence as R_h.

The Hall element voltage is given as:

$$V_h = B \cdot S_{h0} \cdot \frac{I_b}{I_0} = B \cdot S_{h0} \cdot \frac{k_0}{R_h} \qquad (1)$$

where B is magnetic field perpendicular to the surface of the chip, S_{h0} is Hall element sensitivity at constant bias current $I_o = 1/k_0$, and I_b is actual Hall element bias current.

The output current of the differential stage is given as:

$$I_S = g_m \cdot V_h = \sqrt{I_d \cdot k' \cdot \frac{w}{L}} \cdot V_h \qquad (2)$$

where g_m is transconductance of the differential transistors T1 and T2, I_d is bias current of the differential stage and w/L are the channel dimensions of transistors T1 and T2.

The output voltage V_{out} is:

$$V_{out} = I_S \cdot R1 + I_S \cdot R2 \qquad (3)$$

The resistors R1 and R2 are made equal and have the same temperature coefficient as Hall element resistance R_h so the output voltage is:

$$V_{out} = 2B \cdot S_{h0} \cdot k_0 \cdot \sqrt{I_d \cdot k' \cdot \frac{\omega}{L}} \cdot \frac{R}{R_h} =$$

$$= K(I_d, k') \cdot V_h = K(I_d, k') \cdot S_{h0}(T,P,t) \cdot B \qquad (4)$$

where K is a constant dependent on I_d and k' and S_{h0} is sensitivity of Hall element dependent on temperature (T), pressure (P) and time (t).

As seen from the equation 4 the most critical temperature and process dependence of the output voltage is replaced by constant ratio R/R_h which can be made very stable. The dependencies of the sensitivity due to mobility temperature coefficient and due to pressure variations are canceled by varying I_d in the selfcalibrating feed-back loop.

3 The offset voltage considerations

There are two most critical offset sources:

1. The offset of Hall element: V_{offh}
2. The offset of the front end differential stage: V_{offdif}.

The signal and the offset of Hall element seen at the input of the front end differential stage is:

$$V_A = V_{sig} + V_{offh}$$
$$V_B = -V_{sig} + V_{offh} \qquad (5)$$

where V_A and V_B denote the situation in spinning phases A and B.

This translates to the signal on resistors R1 and R2:

$$V_{R1} = K(V_{sig} + V_{offh} + V_{offdif})$$
$$V_{R2} = K(-V_{sig} + V_{offh} + V_{offdif}) \qquad (6)$$

In phase A the signal V_{R1} is sampled on capacitor C_{S1} and the operational amplifier is in voltage source configuration, i.e. the gain is +1.

In the spinning phase B the current S flows through resistor R2 and is sampled on capacitor C_{S2}. In this configuration the gain is -1 so the output is simply:

$$V_{out} = 2 \cdot I_S \cdot R \qquad (7)$$

where R = R1 = R2 and both offsets are subtracted. The efficiency of the subtraction is given by common mode rejection factor of the operational amplifier.

4 Autocalibration

The autocalibration is performed by generation of on board reference magnetic field /2/, /3/. This is done by integrated coils as shown in fig. 2.

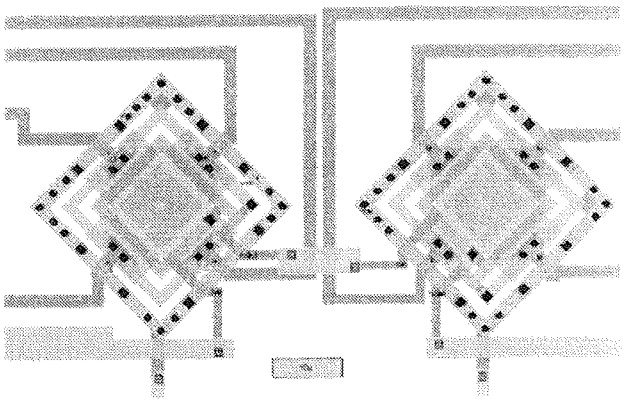

Fig. 2: Hall element pair with integrated coil for reference field generation.

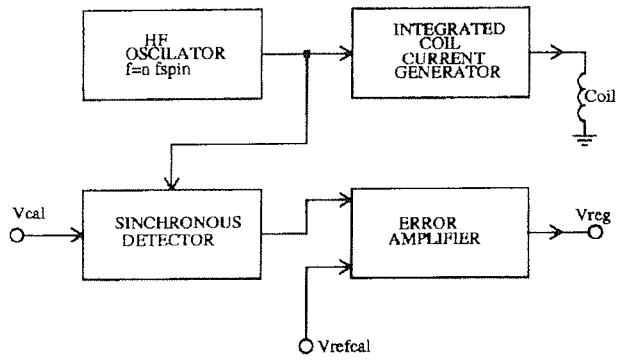

Fig. 3: Block diagram of magnetic sensitivity correction.

The block diagram of the autocalibration loop is shown in fig. 3.

The calibration current frequency is n times higher than the spinning frequency so it can not be seen on V_{out}.

The resistor R_{cal} is inserted to see high frequency signal V_{cal}. The phase of the reference field generation is inverted according to the spinning phase so no phase jump is seen on V_{cal}.

The signal V_{cal} is an AC signal which is effectively rectified by synchronous detector. An error amplifier compares this rectified signal and regulates the gain of the input differential stage by varying its bias current I_d.

5 Conclusions

An effective magnetic cell has been developed. It offers up to three times lower noise than the conventional approach.

The offset voltage is canceled by spinning and by introduction of a new differential sample and hold stage. The autocalibration is achieved by on board generation of the high frequency reference magnetic field.

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