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ON MICROELECTRONICS, DEVICES AND MATERIALS

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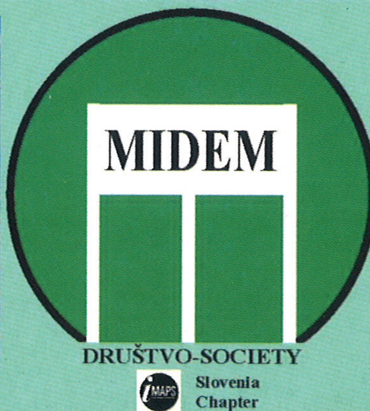

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Slika na naslovnici:
Letošnja konferenca, MIDEM 2001, se je odvijala v osrčju Triglavskega narodnega parka, v hotelu Zlatorog, katerega podoba se zrcali v kristalni vodi Bohinjskega jezera obdanega z vršaci Julijskih Alp.

Front page:
MIDEM 2001 Conference was held in hotel Zlatorog, mirrored in crystal waters of Lake Bohinj in the heart of Triglav National Park and surrounded by the peaks of the Julian Alps.

VSEBINA **CONTENT**

Conference MIDEM 2001 continued the tradition of annual international conferences organized by MIDEM, Society for Microelectronics, Devices and Materials. This issue of the Journal Informacije MIDEM brings seven invited papers presented at the Conference.

Main core of the Conference was devoted to the Workshop on OPTOELECTRONIC DEVICES AND APPLICATIONS, where distinguished guest speakers and other contributors presented valuable advanced information on lasers, light emitting devices, thin film transistors, optical fibre systems and non-linear optical devices. Basic physical principles, as well as actual and possible applications of these optoelectronic devices and systems were presented.

On 345 pages, Proceedings of the MIDEM 2001 conference contain invited, as well as 43 regular papers covering up-to-date topics on integrated circuits; device physics and modelling; optoelectronic devices and applications; thick and thin films and ceramics, metals and composites.

In addition, on the occasion of the 30th anniversary of the Laboratory for microelectronics at the Faculty of Electrical Engineering of the University of Ljubljana, Informacije MIDEM brings several research papers by the laboratory researchers, showing some of the present research activities of the Laboratory for microelectronics.

Presently the main activity of the Laboratory is the design of mixed signal integrated circuits and microsystems implemented by very efficient design tools that had been developed in the laboratory. These tools have been proved by successful design of several hundred of ICs for domestic and foreign customers.

Part of the Laboratory for microelectronics is an IC fabrication line, which is capable of processing 4" wafers down to submicron feature size enabling pilot production and high level student work.

Editor-in-chief

Iztok Šorli

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INTEGRATED HALL SENSOR / FLUX CONCENTRATOR MICROSYSTEMS

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INVITED PAPER
MIDEM 2001 CONFERENCE
10.10.01 - 12.10.01, Hotel Zlatorog, Bohinj

Key words: semiconductors, microelectronics, CMOS technologies, integrated microsystems, integrated magnetic sensors, HALL sensors, magnetic fields parallel to the chip surface, concentrated magnetic flux, planar magnetic flux concentrators, higher sensitivity, equivalent magnetic offset, equivalent magnetic noise

Abstract : The paper describes highly sensitive single-axis and two-axis integrated Hall magnetic sensors. They consist of an integrated combination of a CMOS Hall integrated circuit and a planar magnetic flux concentrator. The magnetic flux concentrator is made of a thick ferromagnetic layer bonded on the CMOS wafer. The CMOS part of the system contains two or more conventional Hall elements positioned under the periphery of the flux concentrator. The flux concentrator converts locally a magnetic field parallel with the chip surface into a field perpendicular to the chip surface. Therefore, a conventional Hall element can detect an external magnetic field parallel with the chip surface. The flux concentrator also provides a magnetic gain.

Integriran mikrosistem Hallov senzor / zgoščevalec magnetnega pretoka

Ključne besede: polprevodniki, mikroelektronika, CMOS tehnologije, mikrosistemi integrirani, senzorji magnetni integrirani, HALL senzorji, polja magnetna vzporedna površini chip-a, pretok magnetni zgoščeni, koncentratorji pretoka magnetnega planarni, občutljivost višja, offset magnetni ekvivalentni, šum magnetni ekvivalentni

Izvleček : V prispevku opisujemo zelo občutljive eno- in dvoosne integrirane Hallove magnetne senzorje. Dobimo jih z integrirano kombinacijo CMOS Hallovega integriranega vezja in ravninskega zgoščevalca magnetnega pretoka. Zgoščevalec magnetnega pretoka je izdelan iz debele feromagnetne plasti pritrjene na CMOS silicijevo rezino. CMOS del vsebuje dva ali nekaj konvencionalnih Hallovih elementov postavljenih pod obod zgoščevalca pretoka. Le-ta pretvori lokalno vzporedno magnetno polje v navpičnega glede na površino čipa. Zatorej lahko konvencionalni Hallov element zazna tudi zunanje magnetno polje vzporedno s površino čipa. Zgoščevalnik pretoka pa dodatno poskrbi tudi za ojačanje gostote magnetnega pretoka.

1. Introduction

The subject of this paper is a new class of magnetic sensor microsystems based on an integrated combination of Hall elements and ferro-magnetic structures. Such microsystems are members of emerging family of Hybrid Ferromagnetic - Semiconductor Structures /1/. The term "hybrid" here means: fabricated by dissimilar technologies, but the "hybridization" is now usually made at the semiconductor wafer level. Such hybrid structures are used as sensitive magnetic sensors and are also investigated as candidates for the information storage cells of novel magnetic random access memories /2/.

It is interesting to note that the idea of combining a semiconductor magnetic field sensor with ferromagnetic structures came to many researchers in the past. Probably the first report on the subject was published back in 1955 /3/. In order to amplify the magnetic field "seen" by an InSb Hall plate, the authors put the Hall plate in the air gap between two long ferromagnetic rods. In this way they considerably increased the effective sensitivity and the resolution of the Hall element and could measure quasi-static magnetic fields down to milli-gauss range. The operation of this device is based on the following well-known effect: if a ferromagnetic rod is placed in a magnetic field parallel with the long axes of the rod, the rod tends to collect the magnetic field lines in itself: it operates as a magnetic flux concentrator. Similar macroscopic systems Hall sensor - Magnetic concentrators, made of discrete components, were investigated also by other researchers /4/ - /6/. We developed a first hybrid micro-system Hall sensor - Magnetic concentrators /7/ which became a part of a commercially available product. The best reported detectivity limit of a combination Hall sensor - Magnetic concentrators is as low as 10 pT /5/.

In /5/ we find also a report of an attempt to incorporate ferromagnetic material into the package of a Hall device. This idea is also presented in /8/, and is now used in several commercially available Hall magnetic sensors.

To the best of our knowledge, the idea of using an integrated combination of a semiconductor magnetic micro-sensor and a thin ferromagnetic film was mentioned for the first time in a patent /9/.

In this paper we analyze integrated combinations of Hall elements and magnetic flux concentrators. As in the case of the conventional applications of magnetic concentrators /3/ - /7/, we use the integrated magnetic concentrators as passive magnetic amplifiers. However, the structure of our concentrators is different: it is planar, which allows an easy integration on a semiconductor wafer. We shall describe two basic structures, one with so-called twin magnetic flux concentrators and the other with a single magnetic flux concentrator. In both cases we shall estimate the relationships between the parameters of the structure and its magnetic gain and the saturation field.

2. TWIN magnetic flux concentrators

The idea of the integrated twin magnetic flux concentrators /10/ is illustrated in Figure 1. Obviously, the idea is inspired by the conventional configuration of the combination

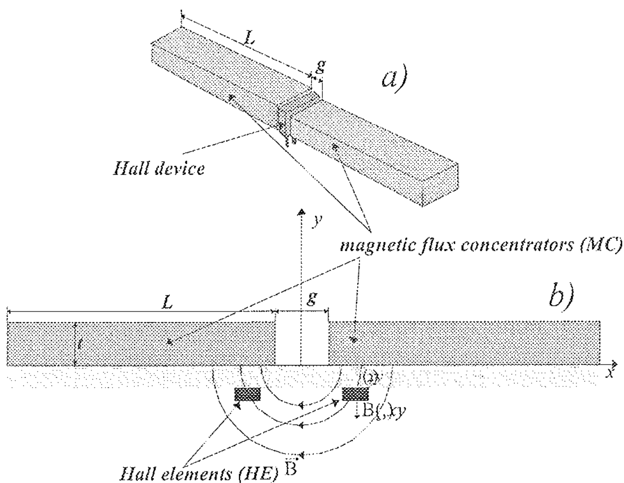

Figure 1: *Comparison of a conventional (a) and an integrated (b) combination Hall magnetic sensor - magnetic flux concentrators: a) the Hall device is placed in the air gap between the two flux concentrators; b) two Hall elements are placed under the planar magnetic concentrators /11/.*

Hall magnetic sensor - rod-like magnetic concentrators (MC). The key difference is, however, that the Hall element in (b) is placed not in, but near the air gap and under the concentrators. In this way, we can use conventional planar integrated Hall elements and we can define by photolithography the shape of MCs and the mutual positions in the system MCs - Hall elements.

The integrated magnetic flux concentrators consist of a high permeability and low coercive field (very soft) ferromagnetic layer bonded on the Hall sensor chip surface. The layer is structured so that a narrow air gap is created approximately in the middle of the chip. Figure 2 shows the distribution of the magnetic field lines around the MCs. The MCs "suck in" the magnetic field lines and convert locally the magnetic field parallel with chip surface into a magnetic field perpendicular to the chip surface. The perpendicular component of the magnetic field is the strongest near the gap. There we place the Hall elements. We use two Hall elements because two equivalent places are available and so we increase the signal to noise ratio. The Hall plates below the different concentrators see the useful magnetic field in opposite directions. So the system is insensitive to an external field component perpendicular to the chip surface /12/.

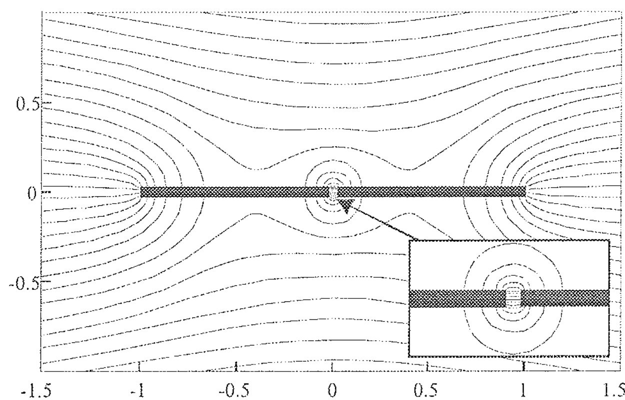

Figure 2: *The result of a two-dimensional simulation of twin planar MCs introduced into a homogenous magnetic field parallel with the MC-plane.*

In order to obtain an intuitive insight into the behavior of the magnetic concentrators, we shall perform here an appreciative two-dimensional analysis. We assume that integrated magnetic flux concentrators are layer-like (the planar dimensions of an MC are much larger than its thickness t). Moreover, since in practice we work only with very high-permeability materials, with $\mu_r > 10^5$, we assume $\mu_r \rightarrow \infty$.

2.1 Magnetic gain

We define the magnetic gain of an MC as the ratio

$$G_{XY} = B_{HE} / B_0 . \quad (1)$$

Here B_{HE} is the (perpendicular) component of the magnetic induction "seen" by the planar Hall element (HE) at a position (X, Y) (see Figure 1) and B_0 is the magnetic induction component parallel with the axis of the MC faraway from the MC.

Let us put the magnetic scalar potential difference (i.e. the equivalent excitation current I_{ex}) acting between the two adjacent MCs in the form

$$I_{ex} = KH_0(2L+g) \qquad (2)$$

Here H_0 is the magnitude of the magnetic field vector H_0 before introducing the MC, $H_0 = B_0/\mu_0$. K is a numerical factor defined by $K = \int H_g\,dl / H_0(2L+g)$, where H_g is the magnetic field in the gap and the integration is done over the gap. It tells which part of the theoretically available equivalent excitation current along the whole length of the MC we can rally use around the air gap. From physical arguments we estimate the limits for K in the two-dimensional case, with $L >> t$, as follows: when $g/t \rightarrow 0$, then $K \approx g/t \rightarrow 0$; when $L >> g >> t$, then $K \approx 1/2$. The values of K deduced from numerical simulations, Figure 3, supports these estimations.

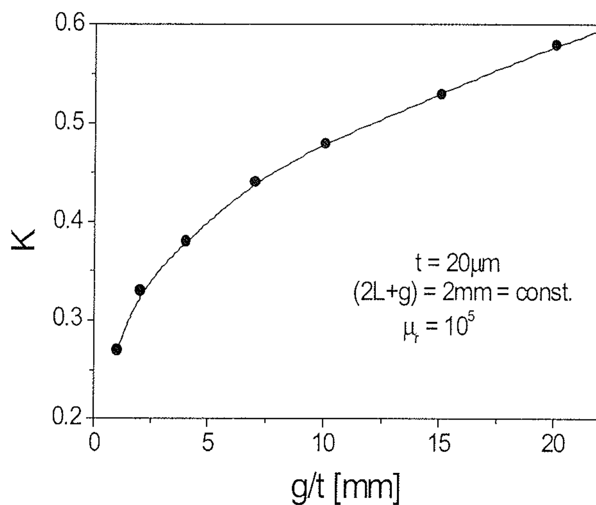

Figure 3. *The values of the factor K deduced from two-dimensional simulation of twin planar MCs.*

By inspecting Figure 2 we see that the magnetic field lines below the MC and close to the gap have approximately a circular form. This is always the case for high-permeability MCs and narrow gaps. Using this fact we find now the magnetic gain of a twin MC for a HE placed at (X,Y):

$$G_{XY} = \frac{K(2L+g)X}{\pi(X^2+Y^2)}$$

$$for \quad X > g/2,\ g \approx t \ and \ \mu_r >> 1 \qquad (3)$$

With an optimal layout of MC, for given t, L and g, one can increase K and so the magnetic gain G_{XY} up to a factor of 2 /13/. The realistic values of G_{XY} for an integrated sensor are between 5 and 10. But adding external MCs, this can be easily increased to about 100 /11/.

2.2 Saturation field

By inspecting Figure 2 we notice that the magnetic field lines have the highest density in the magnetic concentrators somewhere between the middle of each concentrator and the gap. We find the corresponding maximal magnetic flux density by calculating the total flux entering into an MC as follows:

$$B_{max} \approx \mu_0 \frac{KH_0(2L+g)}{g}\left(1+\frac{2}{\pi}\frac{g}{t}\ln(L/g)\right) \qquad (4)$$

When this induction reaches the saturation induction B_{sat} of the MC material, our magnetic sensor shows a strong decrease in its magnetic sensitivity. The external magnetic field induction at the onset of the saturation is given by

$$B_{0sat} \approx B_{sat}\, g\left[K(2L+g)\left(1+\frac{2}{\pi}\frac{g}{t}\ln(L/g)\right)\right]^{-1}$$

$$for \quad g \approx t \ and \ \mu_r >> 1 \qquad (5)$$

For a sensor with the MCs of the total length $2L + g = 2$ mm, $t = g = 20$ μm and $B_{sat} = 1$ T, we obtain $B_{0sat} \approx 10$ mT. By choosing an optimal form of the MC for given t, L and g, one can increase the saturation field up to a factor of 2 /12/.

2.3 Application

By integrating twin magnetic concentrators with Hall elements, we obtain a magnetic sensor system with the following combination of features: existence of a magnetic gain, which brings a higher magnetic sensitivity, lower equivalent magnetic offset, and lower equivalent magnetic noise than those in conventional integrated Hall sensors; and sensitivity to a magnetic field parallel with the chip surface, much as in the case of magneto-resistance sensors. Figure 4 shows one example of such an integrated magnetic sensor.

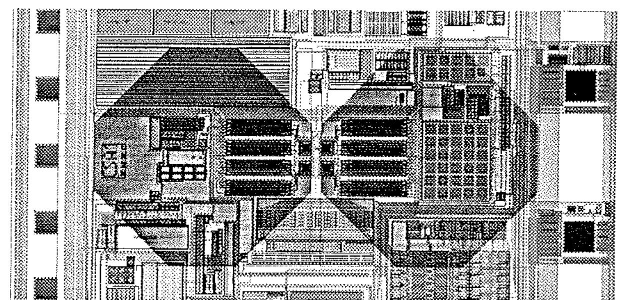

Figure 4: *The detail of the layout of an integrated magnetic sensor microsystem. The semiconductor part is a CMOS Hall ASIC. The twin magnetic concentrator has the form of the two octagons. The sensor responds to a magnetic field parallel to the in-plane symmetry axes of the two concentrators. The magnetic sensitivity is 300 V/T and the equivalent offset field is 0.05 mT. (Courtesy of SENTRON AG, Zug, Switzerland).*

3. Single magnetic FLUX concentrator

A single integrated magnetic flux concentrator is shown in Figure 5 /14/, /15/. Here again, the concentrator converts locally a magnetic field parallel with the chip surface into a magnetic field perpendicular to the chip surface. The strongest perpendicular component of the magnetic field appears under the concentrator extremities. The Hall elements are placed under the concentrator extremities and "see" this perpendicular component of the magnetic field much as in the case of twin magnetic concentrators.

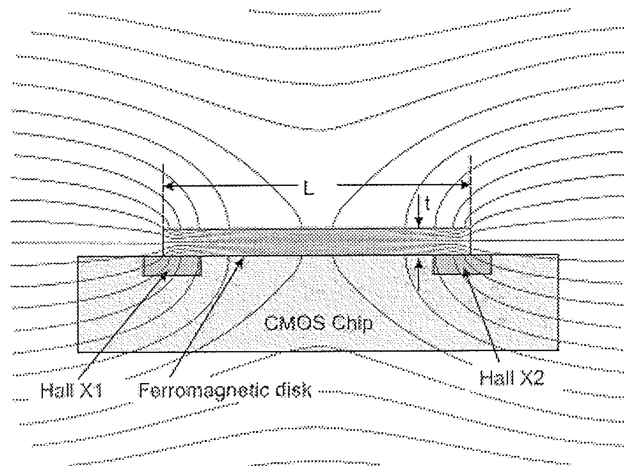

Figure 5: *Cross-section of a Hall chip combined with a single magnetic flux concentrator. The magnetic concentrator usually has the form of a disc /15/.*

3.1 Magnetic gain

We define the magnetic gain of a single magnetic field concentrator in the same way as above, Eq. (1). In order to estimate the magnetic gain, we model a disc-like magnetic concentrator with an oblate ellipsoid. For a very flat oblate ellipsoid magnetized parallel to a long axis, the demagnetization factor /16/ in our notation is

$$N \approx \frac{\pi t}{4L}(1-\frac{4t}{\pi L}) \qquad for \quad L/t >> 1 \tag{6}$$

In a very high-permeability and not very elongated structure, the internal magnetic induction is

$$B_i \approx \frac{\mu_0}{N} H_0 \tag{7}$$

Assuming that the external magnetic induction "seen" by the Hall elements $B_{HE} \approx B_i$, we obtain for the magnetic gain

$$G_E \approx 1/N \qquad for \quad \mu_r \to \infty \tag{8}$$

where N is given by Eq. (6). For a disc with $L / t = 10$, we calculate $G_E \approx 14.5$. Numerical simulations gave /15/ a similar value for the total magnetic gain, but only about 7 for the perpendicular field component.

3.2 Saturation field

From Eq. (7) we readily obtain

$$B_{0sat} \approx NB_{sat} \qquad for \quad \mu_r \to \infty \tag{9}$$

where B_{sat} is the saturation induction of the MC material. For a disc-like MC with $L / t = 10$ and $B_{sat} = 1$ T, this gives $B_{0sat} \approx 69$ mT.

3.3 Application

If used as a single-axes magnetic field sensor, the single MC system shown in this section may reach similar performance as the one with twin MC. The disc-like form of a single magnetic concentrator is very advantageous for contactless angular position sensing applications /15/. Figure 6 shows one example of such an integrated magnetic sensor microsystem.

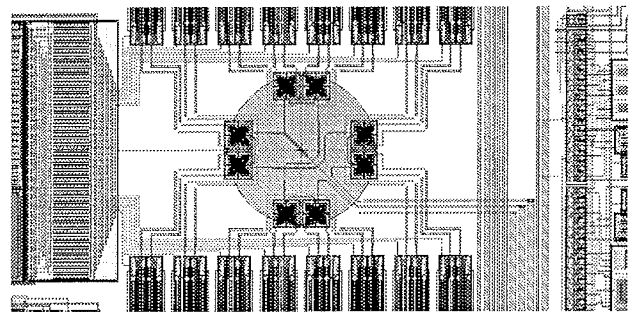

Figure 6: *Detail of the layout of an integrated 2-axes magnetic sensor microsystem. The semiconductor part is a CMOS Hall ASIC. The disc-like magnetic concentrator is deposited in a post-processing step. The sensor gives two component of an in-plane magnetic field and shall be used as an angular position sensor. (Courtesy of SENTRON AG, Zug, Switzerland).*

4. Conclusions

The Hall sensor microsystems described in this paper respond to a magnetic field parallel to the chip surface and not, as conventional Hall magnetic sensors, to a field perpendicular to the device surface. Thanks to the flux concentration effect, they also have higher magnetic sensitivity, lower equivalent magnetic offset, and lower equivalent magnetic noise than conventional Hall devices. Therefore, from the application point of view, these new integrated Hall sensors are similar to hypothetical low-offset and very linear magnetoresistive sensors (MR). Moreover, the structure of our new Hall sensors is fully compatible with conventional CMOS technology. This allows full system integration on a chip. Typical applications are sensitive position sensing and contactless angle measurement.

Assuming a state of the art realization of the CMOS part, the system performance of a magnetic sensor with a magnetic flux concentrator is determined by the characteristics of the concentrator. The magnetic gain is proportional to the ration length / thickness of the concentrator. The saturation magnetic field is inversely proportional to the magnetic gain. By and large, the maximal magnetic filed that could be concentrated on the Hall element is determined by thickness of the magnetic concentrator and the length of the sensor chip.

5. References

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HOT WIRE DEPOSITED MATERIALS FOR THIN FILM TRANSISTORS

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Key words: semiconductors, microelectronics, hot wire technologies, CVD, Chemical Vapour Deposition, HWCVD, Hot Wire CVD, Hot Wire Chemical Vapour Deposition, imaging devices, image sensors, image displays, scanners, X-ray imagers, TFT, Thin Film Transistors, a-Si:H TFT technologies, Hydrogenated amorphous Silicon Thin Film Transistor technologies, cost reduction

Abstract : Thin film transistors (TFTs) find widespread application as the switching element in active matrix (AM) liquid crystal displays (LCD), such as the TFT display used in lap top computers, but also in 2-dimensional imaging devices, such as document scanners or in digital X-ray imagers for medical applications.

This paper addresses the new challenges that exist in research and development of TFTs: 1) TFTs on plastic substrates, 2) low-temperature poly-silicon (LTPS) for the pixel TFTs and for row and column drivers on glass; 3) addressing of OLEDs (Organic Light Emitting Diodes) by silicon TFTs. For these advanced applications of TFTs the relevant issues are: (i) higher electron mobility, (ii) stability, and (iii) defect free, uniform deposition of thin silicon films and gate dielectrics at a high deposition rate (for reduced cost). Whereas a high deposition rate is generally needed to reduce the production cost, for novel high current applications the latter two issues have recently become more essential.

At Utrecht University, we are investigating Hot Wire (Catalytic) CVD as a deposition technique for novel TFTs that have a high potential to meet the above mentioned requirements. In Hot Wire CVD, the source gases are catalytically decomposed at heated tungsten or tantalum filaments (~1800 °C), whereas the substrate is kept at a low temperature. Hydrogenated amorphous silicon (a-Si:H) with device quality can be deposited at a high rate of 1-5 nm/s. Bottom gate, inverted staggered TFTs with Hot Wire CVD silicon films have been made with an electron mobility of 1.5 cm^2/Vs, and with field effect characteristics that are completely stable under operating conditions. Top gate, coplanar TFTs with polycrystalline silicon films have been made, showing a mobility of 4.7 cm^2/Vs, in agreement with the Hall mobility measured in individual thin films. This has been obtained without any post deposition treatment, and the Hot Wire technology can thus avoid expensive, time-consuming steps such as the laser recrystallization step that is currently used in the production of the latest poly-Si lap top displays. Hot Wire CVD is also suitable for the deposition of silicon nitride (SiN_x:H) gate dielectrics. TFTs with a Hot Wire silicon nitride gate dielectric, deposited below 400 °C, have reached a mobility of 0.6 cm^2/Vs and a threshold voltage of 2.9 V.

Nanos materialov z metodo vroče žice pri izdelavi tankoplastnih tranzistorjev

Ključne besede: polprevodniki, mikroelektronika, tehnologije žice vroče, CVD nanosi kemični s paro, HWCVD nanosi kemični s paro in žico vročo, naprave upodabljalne, senzorji slik, zasloni slikovni, skenerji, upodabljalniki X-žarkov, TFT transistorji tankoplastni, a-Si:H TFT tehnologije silicija amorfnega hidrogeniziranega za transistorje tankoplastne, zmanjšanje stroškov

Izvleček : Tankoplastni tranzistorji (TFT - Thin Film Transistors) se na široko uporabljajo kot stikalni elementi v aktivnih matrikah (AM - Active Matrix), prikazalnikih na tekoče kristale (LCD - Liquid Crystal Displays), kot npr. pri TFT zaslonih prenosnih računalnikov ali tudi pri dvodimenzionalnih slikovnih napravah kot so skenerji ali x žarkovni upodabljalniki v medicini.

V prispevku obravnavamo nove izzive v razvoju in raziskavah TFT tranzistorjev : 1) TFT tranzistorji na plastičnih substratih, 2) nizkotemperaturni nanos polisilicija (LTPS) za izdelavo točkovnih (pixel) TFT tranzistorjev, oz. za izdelavo krmilnikov vrstic in stolpcev na steklu , 3) krmiljenje OLED diod (OLED - Organic Light Emitting Diodes) s TFT tranzistorji. Za vse te naštete napredne uporabe TFT tranzistorjev so pomembne naslednje njihove lastnosti: i) visoka gibljivost elektronov, ii) stabilnost, iii) enakomeren nanos tankih plasti silicija in dielektrika za krmilno elektrodo brez napak pri visokih hitrostih nanašanja. Visoke hitrosti nanašanja so sicer potrebne za zmanjšanje proizvodnih stroškov, vendar zadnje čase postajata vse bolj pomembna zadnja dva dejavnika predvsem zaradi zahtev po visokih tokovih.

Na Univerzi v Utrechtu raziskujemo tehniko kemičnega nanosa silicija (CVD) z metodo vroče žice, s katero si obetamo doseči vse zgoraj naštete lastnosti TFT tranzistorjev. Pri tej metodi se plini katalitično razgradijo na greti tantalovi ali volframovi nitki (temperatura okoli 1800°C), med tem ko je substrat na nizki temperaturi. Ustrezno kvaliteten hidrogeniran amorfni silicij (a-Si:H) lahko nanašamo s hitrostjo 1 - 5 nm/s. S CVD nanosom z metodo vroče žice smo izdelali TFT tranzistorje z obrnjeno krmilno elektrodo z gibljivostjo elektronov 1.5 cm^2/Vs in z električnimi karakteristikami, ki so bile popolnoma stabilne. Koplanarni TFT tranzistorji iz polikristaliničnega silicija s krmilno elektrodo na vrhu pa so imeli elektronsko gibljivost 4.7 cm^2/Vs, kar je enako Hallovi gibljivosti merjeni v samostojnih tankih filmih. Omenjene lastnosti smo dosegli brez kakršnihkoli dodatnih obdelav, iz česar lahko sklepamo, da se pri CVD nanosu silicija z metodo vroče žice lahko izognemo dragemu in dolgotrajnemu postopku laserske rekristalizacije tanke plasti, ki je trenutno v rabi v proizvodnji najnovejših polisilicijevih zaslonov za prenosne računalnike.

CVD nanos z metodo vroče žice je primeren tudi za nanos dielektrika za krmilno elektrodo iz silicijevega nitrida (SiN_x : H). Tovrstni TFT tranzistorji nanešeni pri temperaturi pod 400°C so dosegli gibljivost elektronov 0.6 cm^2/Vs in pragovno napetost 2.9 V.

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1. Introduction

The application of Thin Film Transistors (TFTs) in image sensors and displays is very widespread. Amorphous silicon (a-Si:H) TFT technology has shown to be a mature technology and thus TFTs are widely used for individually switched display elements (pixels) in Liquid Crystal Displays (LCDs) /1/, primarily in portable laptop computers, but also in 2-dimensional imaging devices, such as document scanners or in digital X-ray imagers for medical applications.

In an LCD, the display elements comprise liquid crystals of which the transmissive or reflective optical properties can be altered by electrically charging or discharging them. These elements are arranged in large matrices along with their switching TFTs to form an Active Matrix Liquid Crystal Display (AMLCD). Although the mobility of a-Si:H TFTs is quite low (≈ 1 cm^2/Vs), these TFTs are very suitable as the pixel switches in AMLCDs, since they can be fabricated over large areas (so that displays with > 15" diameter are no longer an exception), with high yield, and showing very uniform performance, while the low mobility is amply sufficient to charge the pixels within the row addressing time. A possible drawback of a-Si:H TFTs is the threshold voltage shift after prolonged applied bias to the gate electrode. Given the high quality of the currently available gate dielectrics, this effect has been proven to be an intrinsic property of a-Si:H rather than charge trapping in the gate dielectric /2/. Nevertheless, the threshold voltage shift is not an issue in AMLCDs, since the total integrated duration of applied bias to each transistor ("ON time") over the life of a display is too short to produce any significant threshold voltage shift. The duty cycle is very short, because the pixels can be charged within a very short time and the TFT is switched back to the OFF condition once a pixel is charged.

2. Requirements to TFTs

2.1 Mobility

Although a-Si:H TFTs are used in mass-produced displays and sensor arrays, new challenges to this field have surfaced recently. The performance of very high-resolution displays is mainly determined by the electron mobility of the pixel TFTs. This is one reason why TFTs with higher mobility would have advantages. Further, one would like to avoid the need for external IC mounting of the row and column drivers. For on-glass peripheral driver circuitry integration, a higher carrier mobility of TFTs is required. For driver circuitry, n-channel and p-channel TFTs are required. This would enable Complementary Metal-Oxide-Semiconductor (CMOS) circuits, which would make low-power (< 1 mW) on-glass drivers possible and, consequently, the displays could become extremely flat. For row drivers a mobility of 10 cm^2/Vs is amply sufficient and for column drivers the mobility would need to be 100 cm^2/Vs /3/. Using multiplexed row and column drivers however, just a moderate improvement of the mobility of TFTs would already be sufficient /4/ while the number of interconnects could already be greatly reduced. For driver TFTs the stability, in addition to the mobility, becomes an issue.

2.2 Stability

The stability of the devices has again become an important issue in the following technology fields. *(i) Low-temperature deposited Thin Film Transistors on polymer substrates* /5,6/. Such low-temperature deposited matrices of TFTs could ultimately be made by roll-to-roll production and be used in curved consumer products, such as mobile phones, and in rollable "electronic paper". The maximum processing temperature that can be used on, e.g., transparent polyethylene terephthalate (PET) is ≈ 150 °C. *(ii) TFTs that are used in multiplexed drivers*. In such driver circuits, TFTs have a high duty ratio (i.e., the ON time is long compared to the OFF time) implying prolonged gate bias stress conditions. The threshold voltage shift that results from such prolonged gate bias conditions would lead to a too short life of the driver circuitry. *(iii) TFTs for the addressing of Organic Light Emitting Diodes (OLEDs)*. When OLED displays become large (i.e., laptop size), *active* matrix addressing (AMOLEDs) is required in order to reduce the power losses due to capacitive charging, which is a problem in *passive*-matrix addressed OLEDs. In contrast to the pixel switching scheme in *charge-driven* LCDs, the *current-driven* LED pixels have to be addressed in a *constant current* mode, which means that the switching transistors remain in the ON state as long as the pixel is required to be ON. Therefore, the TFTs have to be capable of enduring orders of magnitude longer durations of applied bias and should therefore be essentially stable.

2.3 Cost reduction

The solution to mobility and stability issues is often found by the introducing poly-Si TFTs. At present, these TFTs are already used in finer pitched displays, such as in the high quality segment of avionics products or in projection displays. In small size display panels, poly-Si TFTs are in use in the driver ICs as well as in the switching transistors /7/. These TFTs always have a top gate structure as this has the advantage that they can be structured using self-aligned photolithographic definition. The challenge in this segment is to produce poly-Si at a low temperature (LTPS; Low Temperature Poly-Silicon), so that inexpensive and larger substrate plates can be used.

One of the approaches to LTPS is to deposit amorphous or microcrystalline thin films that which are subsequently (re-)crystallized. The common crystallization techniques are furnace annealing (Solid Phase Crystallization; SPC) /8/, rapid thermal annealing (RTP) with lamps /9/, and excimer laser annealing /10/. For glass substrates, furnace annealing is restricted to temperatures < 600 °C due to the softening point of commonly used glass (Corning 1737) and is therefore a method that is very time consuming (in excess of 10 hours). In excimer laser annealing, the short

wavelength (308 nm for a XeCl laser) and the short pulse duration (20 -200 ns) promotes rapid melting and fast solidification. This, in principle, enables the use of substrates that are not resistant to high temperatures, such as glass and plastic foil.

The base materials for laser recrystallization are either made with Low Pressure Chemical Vapor Deposition (LPCVD) /11/ or with Plasma Enhanced CVD (PECVD) /12/. In the latter case, while PECVD allows for a lower deposition temperature, the recrystallization is actually a two-step process or even a three-step process. It is required to dehydrogenate the film (e.g., at 450 °C for 1 hour) in order to prevent explosive outgassing of hydrogen from the film leading to delamination. After completion of the TFTs, an rf hydrogen plasma (for several hours) is needed to passivate defects, reduce leakage currents, and to enhance the electron mobility. The multitude of complicated processing steps with a long duration that are associated with laser annealing is not straightforwardly compatible with the requirement of a throughput of one plate per minute in the single-substrate processing tools currently employed in the fabrication of AMLCDs /13/. Further, there are problems with the homogeneity of the performance of TFTs over large area substrates due to pulse-to-pulse energy fluctuations and the energy distribution in the beam /10/. This results in mobility and threshold voltage variations in the TFTs, which cause unacceptable non-uniformity in display brightness.

Direct deposition of poly-Si TFTs is of interest for obtaining uniformity over large area and for reducing the manufacturing costs. Early results obtained using catalytic chemical vapor dissociation (Cat-CVD) of SiH_4 gas at a hot tungsten wire and deposition of the reactants on a substrate held at 300 °C resulted in thin films with a Hall mobility of 10 cm^2/Vs /14/. Subsequently, a report appeared on TFTs that were deposited on a thermally-grown SiO_2 gate dielectric and had a remarkably high optimum in the field effect mobility of 70 cm^2/Vs /15/. Microcrystalline films can also be made using the Layer-by-Layer (LBL) variant of radio frequency (rf) Plasma Enhanced CVD (PECVD) /16/, leading to a mobility of 0.6 cm^2/Vs in TFTs. The Princeton group recognized that fluorinated silane promotes crystallization in PECVD of thin layers /17/ and produced 50 nm thick TFTs with an electron mobility of 10 cm^2/Vs /18/. Although the deposition rate is only 0.5 Å/s, the deposition time of the active layer could be limited to 15 min, because only a small thickness was required.

Recent results on large area deposition include the achievement of a thickness uniformity of +/- 2.5 % on 20 cm x 20 cm at the University of Kaiserslautern /19/ and a uniformity of +/- 7.5 % on substrates as large as 40 cm x 96 cm, using a novel showerhead design, at Anelva Corporation in Japan /20/.

3. Hot Wire CVD

At Utrecht University, we are investigating two deposition techniques for the fabrication of TFTs: Plasma Enhanced CVD in the Very High Frequency domain (VHFCVD) /18c/ and Hot Wire (Catalytic) CVD. This paper will discuss Hot Wire CVD only; for results obtained with VHFCVD we refer to Ref. 21.

In Hot Wire CVD, the source gases are catalytically decomposed at heated tungsten or tantalum filaments (~1800 °C), whereas the substrate is kept at a low temperature.

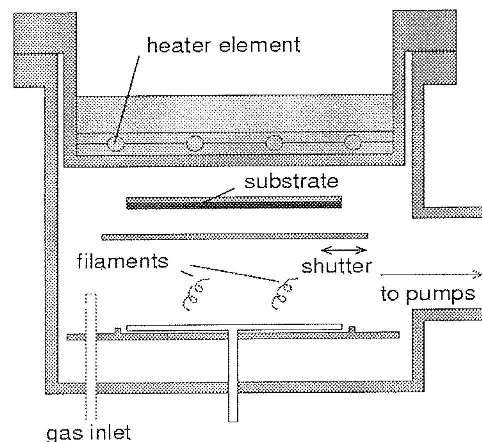

Fig. 1: Schematic cross section of a Hot Wire deposition chamber.

Figure 1 shows a schematic cross section of a Hot Wire deposition chamber at Utrecht University. It basically contains a substrate holder, a shutter, a hot wire assembly, a gas inlet, and a pump port. The substrate holder is optionally heated with an external heater. One or multiple filaments are located at 3 - 8 cm from the substrate. The gases flow perpendicular to the length of the filaments. In contrast to the conventional PECVD technique, no ions are created: though the hot filament emits a considerable electron current, the energy of these electrons is generally too low to cause impact ionization. At our laboratory, two Hot Wire deposition chambers are connected to one of our multichamber ultrahigh vacuum (UHV) systems. This offers the opportunity to create geometry and deposition parameters optimized for two types of intrinsic layers: amorphous and micro/polycrystalline silicon. Hydrogenated amorphous silicon (a-Si:H) films are obtained using 100 % silane (SiH_4), whereas polycrystalline silicon films are made using mixtures of hydrogen (H_2) and silane (SiH_4) gases with a flow ratio of 10 to 15. As a result of systematic and careful optimization procedures we have chosen different substrate-to-wire distances, different wire temperatures, and even different wire materials for a-Si:H and poly-Si:H deposition, respectively (see Table 1).

There are two issues of concern in HWCVD, which have been addressed recently: (1) *Breakage of the wires*. This can be avoided by preventing excessive silicide formation. This is prevented by avoiding high concentrations of silane near the points where the wire is relatively cool /20/. The life of the wire can be further lengthened by an appropriate annealing treatment with H_2 gas prior to deposition;

(2) *Metallic contamination of the films.* This is avoided under normal operating conditions. For instance, for depositions using a W wire at temperatures between 1800 - 2000 °C, it has been verified from SIMS measurements that the tungsten concentration in the deposited films is less than 10^{16} cm^{-3}.

Parameter	Poly-Si:H	a-Si:H
Wire material	W	Ta
$d_{substr-wire}$	40 mm	50 mm
T_{wire}	1800°C	1700°C
T_{sub}	500°C	250°C
Dilution ratio H_2/SiH_4	15	1
Pressure (mbar)	100	20
Deposition rate (Å/s)	5	10
Band gap (eV)	1,1	1,8
Activation energy (eV)	0,55	0,8
Photo-/dark conductivity ratio	10^2	10^6

Table 1: *Key deposition parameters and materials properties of the two intrinsic absorber layers*

At present, high quality amorphous silicon films can be deposited at a rate between 10 and 50 Å/s and micro- or polycrystalline silicon films at a rate between 5 and 20 Å/s. Using pure SiH_4 at a substrate temperature of 430 °C, our best material has an ambipolar diffusion length of 260 nm and is deposited at a rate of 18 Å/s. The hydrogen content is 8 at.-%, leading to an optical (Tauc) band gap of 1.70 eV. The first a-Si:H TFTs made with this material immediately showed that the HWCVD technique leads to very stable devices /22/.

Polycrystalline or microcrystalline silicon materials are typically obtained using dilution of the SiH_4 with H_2. We distinguish two main types of poly-Si:H. Type 1 has random oriented small crystals (denoted as *Poly1*) and type 2 has columnar, strongly oriented (220) crystals (denoted as *Poly2*). The random-oriented *Poly1* is obtained at high H_2 dilution of the silane. These layers are quite porous and are subject to bulk post oxidation if not shielded by a capping layer. They are useful because they typically show *immediate* nucleation on *any* kind of substrate. The deposition rate is relatively low (1 Å/s). The columnar-oriented Poly2 is obtained at moderate H_2 dilution and at a higher deposition rate (5 - 10 Å/s). This deposition rate is comparable to the highest deposition rates available for device quality µc-Si:H by VHFCVD /23,24/.

Poly2 has unique properties, such as a very intrinsic nature (oxygen levels down to 3 x 10^{18} cm^{-3}) and a very high compactness, due to good coalescence of the crystals /25/. The latter is illustrated by (i) SiH stretching mode IR absorption only at 2000 cm^{-1}, typical for isolated SiH bonds, (ii) H effusion only at 550-650 °C, (iii) low ESR spin density at 7 x 10^{16} cm^{-3}, and (iv) low activation energy of the Hall mobility (0.012 eV) /26/. The intrinsic nature of the material is also illustrated by the midgap position of the Fermi-level at 0.54 eV, as deduced from temperature dependent dark conductivity (σ_d) measurements. The value of s_d at room temperature is also low, at 1.5 x 10^{-7} $\Omega^{-1}cm^{-1}$. This helps in achieving low leakage currents in TFTs. The hydrogen content in *Poly2* films is only 0.5 at.-%. The compactness makes these films very suitable as capping layer against penetration of oxygen and water vapor. Typically, the *Poly2* growth regime shows an incubation time leading to amorphous or heterogeneous nature near the substrate interface during the first ≈ 50 nm.

3.1 Mobility

We applied the *Poly2* growth regime to the preparation of high quality bottom gate TFTs as well as top gate TFTs. The presence of an incubation layer, however, prevents the achievement of typical "polysilicon-like" behavior and therefore these TFTs behave predominantly "amorphous-like", along with the high ON/OFF ratio that is typical for amorphous silicon TFTs. Nevertheless, these TFTs showed an electron mobility of 1.5 $cm^2V^{-1}s^{-1}$ /27/, which is higher than that of conventional amorphous TFTs. Moreover, the I-V characteristics were remarkably stable /28/, which will be elucidated in the next subsection.

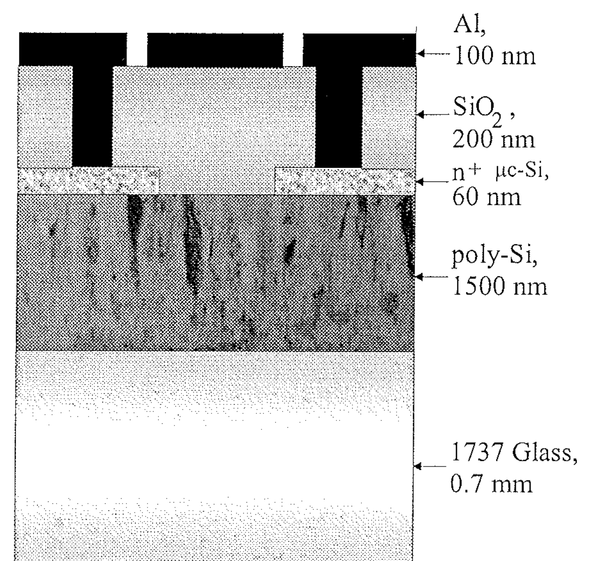

Fig. 2: *Schematic cross section of the top gate TFT structure.*

To investigate the mobility potential of as-deposited polysilicon layers made by HWCVD, Utrecht University and S. Wagner's group at Princeton University have fabricated *top gate* TFTs using the above *Poly2* layer. In the top gate configuration, the conducting channel is near the surface of the layer. Fig. 2 shows a cross section of the *top gate* structure. Since the crystals extend conically in the growth direction, the size of the crystals increases from the substrate to the film surface and hence it was expected that

the electron mobility at the top of the layer would be higher /29/ (for a film thickness of 1.5 μm).

The transfer characteristics at 0.1 V (linear regime) and 10 V (saturated regime) are shown in Fig. 3. It can be seen that at the lowest V_{ds} the drain currents are suppressed. This is possibly due to a small barrier at the source and drain contacts. At V_{ds} = 10 V, the currents are not limited by the contacts. Here, the ON current is 4.8 x 10^{-5} A and the OFF current is 7.5 x 10^{-11} A. Such a low OFF current is not usually obtained for poly-Si TFT. The subthreshold slope $S = \partial V/\partial(\log_{10} I_d)$ is 1.5 V/decade and the threshold voltage V_{th} is 8.0 V. The mobility in the saturated regime is calculated from the slope of the square root of I_d versus V_g measured at V_d = 10 V (for V_g < 15 V) and amounts to 4.0 $cm^2V^{-1}s^{-1}$. The maximum field effect mobility that was obtained is 4.7 $cm^2V^{-1}s^{-1}$.

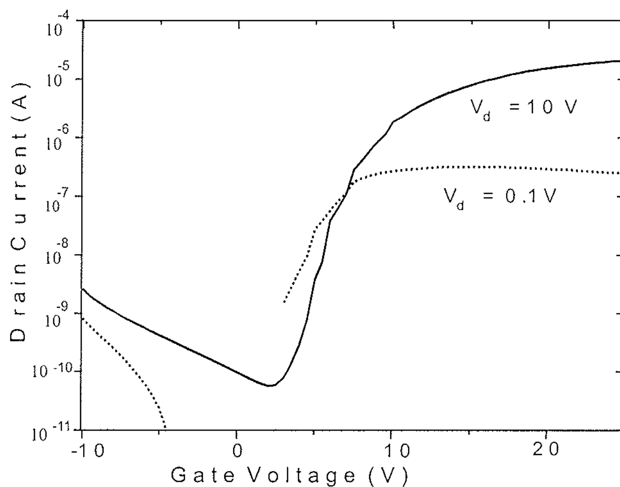

Fig. 3: *The transfer characteristics at 0.1 V (linear regime) and 10 V (saturated regime) of a HWCVD poly-Si:H TFT*

The transistor parameters are fully consistent with the individual thin film properties: the OFF current is in agreement with the dark conductivity of the *Poly2* layer and the field effect electron mobility is similar to the result of the Hall measurement, which was 5 $cm^2V^{-1}s^{-1}$. The mobility is also consistent with the mobility determined from Time-Resolved Microwave Conductivity (TRMC) measurements performed on the same layers, showing an electron mobility of 4 to 5 $cm^2V^{-1}s^{-1}$ /30/. In the TMRC technique, short wavelength pulsed laser illumination of the top surface was used to probe the mobility of the corresponding channel region of the TFT. The lateral current flow does not experience noticeable barriers due to crystal boundaries (consistent with the low activation energy of the Hall mobility of 12 meV).

In addition to this 1.5 μm film, we investigated the effect of a reduced thickness of the silicon film on the TFT characteristics. We employed 750 nm and 300 nm thick films. The results are shown in Table 2. *Top-gate* TFTs with films have reduced electron field effect mobility.

Thickness (nm)	V_{th} (V)	ON/OFF ratio	mobility ($cm^2V^{-1}s^{-1}$)
300	12	30	1.1 x 10^{-3}
750	6	2 x 10^5	1.5
1500	8	4 x 10^5	4.0
1500	9.5	6 x 10^5	4.7

Table 2: *Summary of the HWCVD poly-Si TFT characteristics for three thicknesses of the silicon film on Corning 1737 glass. The threshold voltages and mobilities are taken in the saturated regime. The ON and OFF current are taken at V_{ds} = 10 V, and V_g = 25 V and 0 V, respectively.*

For the thinnest film of 300 nm, the characteristics are very poor. It is interesting to note that the same thin films, implemented in *bottom gate* TFTs, yield an electron mobility of 1.5 $cm^2V^{-1}s^{-1}$. In those TFTs, the channel region is amorphous, due to the incubation stage that *Poly2* requires for the crystals to develop. Thus the reason for the poor mobility for the 300 nm thick *top gate* TFT is most likely the fact that the amorphous and crystalline phases at this stage of the growth are mixed in an unfavorable volume ratio, leading to local porosity, poor carrier transport between isolated grains (low mobility values) and a Fermi level that is pinned by the intergrain defect density (small ON/OFF ratio).

3.2 Stability

We studied the defect creation under prolonged bias voltage stress in TFTs based on silicon deposited by HWCVD and compared them with state-of-the-art devices prepared by PECVD. Purely amorphous as well as heterogeneous silicon conducting channel regions, incorporating a small fraction of crystallites, were exposed to the gate bias stress. A gate bias voltage of 25 V was applied at temperatures between 40 °C and 100 °C for periods between 10 s and 5 x 10^5 s. For the analysis of the data we used the thermalization-energy concept /31,32/ and we fitted stretched hyperbola functions to the relative threshold-voltage shift ΔV_{th}^{rel} versus the thermalization energy E_{th}

$$\Delta V_{th}^{rel} = (V_t - V_t^{ini})/(V_g - V_t^{ini}) = 1 - (\exp[(E_{th} - E_A)/k_B T_0] + 1)^{-1/(\alpha-1)}, \quad (1)$$

where

$$E_{th} = k_B T \cdot \ln(\nu t). \quad (2)$$

It is noteworthy that, although this concept was developed for a-Si:H TFTs, it appears to be equally well applicable to heterogeneous or microcrystalline silicon. Fig. 4 shows the relative threshold shift versus E_{th}.

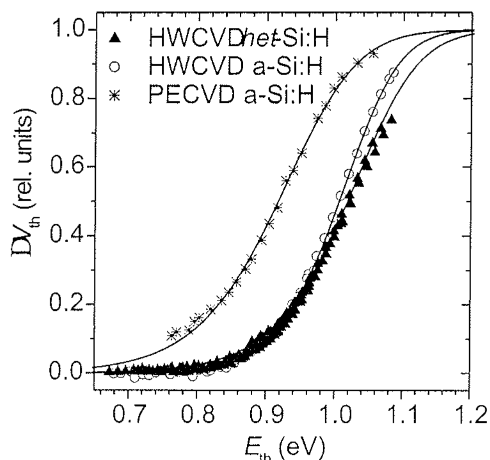

Fig. 4: Measured and fitted relative threshold voltage shift of PECVD a-Si:H and HWCVD silicon TFTs versus thermalization energy.

For HWCVD a-Si:H TFTs the fits resulted in E_A = 1.052 eV, which is high compared to the E_A value of 0.977 eV for the reference PECVD TFT. For the TFT with the heterogeneous material in the channel, which is the result of the initial growth under *Poly2*-type deposition conditions, the E_A value is even better than for the HW a-Si:H TFT, namely 1.073 eV. For this TFT the mobility was 1.18 cm^2/Vs. This demonstrates the superior stability of TFTs using HWCVD deposited silicon for the channel layer /33/.

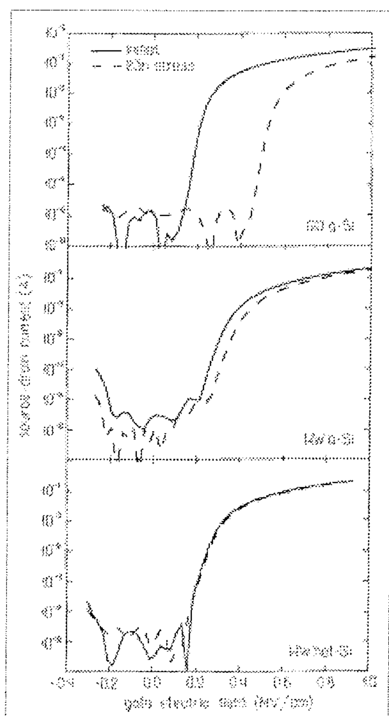

Fig. 5: Transfer characteristics of a PECVD a-Si:H TFT, a HWCVD a-Si:H TFT, and a HWCVD heterogeneous silicon TFT. The solid curves are the initial characteristics and the dashed curves are taken after 23 h of continuous stress at room temperature.

The improved stability is made more clearly visible by showing a snapshot of the I-V transfer characteristics for the three TFTs at an equal stressing dose of 23 h of continuous stress at room temperature. Fig. 5 shows the characteristics for initial and stressed conditions. Whereas the PECVD TFT shows a ΔV_{th} as high as 6.2 V, the HWCVD a-Si:H TFT shows a ΔV_{th} of only 0.9 V and the HWCVD with the heterogeneous silicon channel shows virtually no shift at all.

As all hot-wire TFTs have a better stability than state-of-the-art PECVD devices, these TFTs have the potential to fulfill the requirements for application as the pixel TFTs in AMOLEDs and as the driver TFTs in AMLCDs.

3.3 Cost reduction

The cost of manufacturing AMLCDs is determined, among others, by the thermal budget of the process (via the cost of heat-resistant substrates), the number and duration of processing steps (such as annealing and defect passivation steps), the complexity of the processes (which influences the yield), the cost of equipment (such as laser-annealing equipment), and the throughput. As Hot Wire CVD has already demonstrated that highly stable, high mobility TFTs can be produced, this technology, due to its large area capability, high deposition rates, and simplicity, can contribute greatly to cost-effective manufacturing of active matrices of TFTs. The potential contribution to cost reduction would even be large if both the channel material and the gate dielectric could be made with the same technique. For this reason we have also ventured the demonstration of "all-hot-wire" TFTs.

A HWCVD silicon nitride (SiN_x:H), that is suitable as the gate dielectric in bottom gate TFTs, has recently been developed in our lab /34/ as well as in Matsumura's lab /35/. For the deposition of HWCVD SiN_x gate dielectrics we used a mixture of ammonia (NH_3) and silane. The substrate temperature was kept below 400 °C.

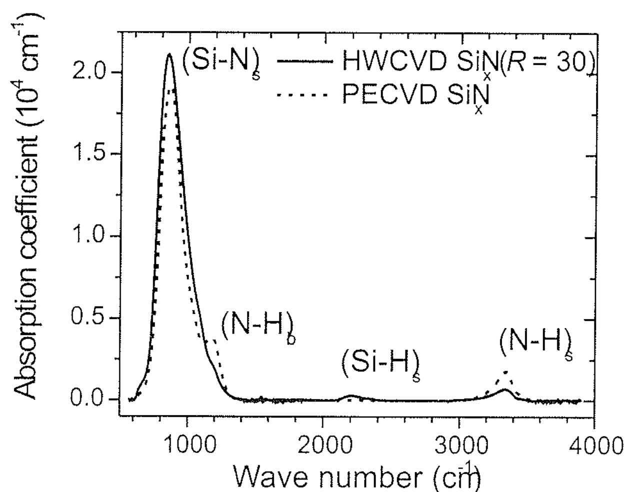

Fig. 6: Infrared absorption spectrum of a HWCVD and a PECVD SiN_x:H layer.

The composition can be tuned over a wide range by varying the SiH_4/NH_3 gas flow-rate ratio. We used a flow-rate ratio of R = 30 - 60 at a pressure of (8 - 15) x 10^{-3} mbar. The filament temperature was 1900 °C. The substrate temperature was 340 °C. A high breakdown field (> 5 MV/cm) and a high electrical resistivity (> 10^{15} Ωcm) have been achieved. Fig. 6 shows the FTIR absorption spectrum of HWCVD SiN_x deposited with R = 30. For comparison the spectrum of typical nitrogen-rich PECVD SiN_x deposited at a substrate temperature of 400 °C /34/ is also shown in this Figure. The composition of HWCVD SiN_x was measured with Elastic Recoil Detection (ERD). We determined x = N/Si = 1.35 ± 0.05, which is near to the value of x = 1.33 for stoichiometric Si_3N_4. In the semiconductor industry, Si_3N_4 is conventionally deposited by LPCVD at a high temperature of ~ 800 °C and therefore it cannot be applied to glass or plastic substrates. The hydrogen content of our films is (10 ± 1) at.-%. This is very low compared to the 22 at.-% present in the PECVD SiN_x sample. In the case of the PECVD SiN_x the hydrogen is bonded to N only, apparent in the N-H stretching mode at 3340 cm^{-1} and the N-H bending mode at 1180 cm^{-1}. The HWCVD layer, on the other hand, also shows a contribution from Si-H_x stretching at 2100 - 2300 cm^{-1}. A refractive index of 1.95 ± 0.02 and a band gap of E_{04} = 4.2 ± 0.1 eV (energy where the absorption coefficient is 10^4 cm^{-1}) was determined by spectroscopic ellipsometry. The relatively low bandgap (E_{04} ~ 5 eV for the PECVD SiNx) and the presence of the Si-H_x mode in the FTIR spectrum indicate that the SiN_x network contains a considerable fraction of Si-Si bonds and, thus, Si dangling bonds, may act as charge-trapping centers as in case of PECVD SiN_x /36/.

TFTs with a PECVD channel layer and a Hot Wire silicon nitride gate dielectric, have reached a mobility of 0.6 cm^2/Vs and a threshold voltage of 2.9 V. 'All-hot-wire' TFTs with both layers made by HWCVD have reached a mobility of 0.3 cm^2/Vs and a threshold voltage of 4.0 V /37/. Although more development work is needed to improve the compatibility between the two layers, it is thus demonstrated that the TFTs can in principle be made using a single process.

4. Conclusion

We have addressed the current issues in the development of TFTs for AMLCDs or AMOLEDs and grouped them in the categories mobility, stability, and cost. With reference to these issues we have discussed the potential of Hot Wire CVD for the fabrication of thin film amorphous, micro-, or polycrystalline silicon channel materials and silicon nitride dielectrics. Although there are still large challenges in the further development of the Hot Wire CVD technique, its simplicity makes it a very favorable technique for the formation of the active layers of TFT matrices and driver circuits.

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TAILORING FERROELECTRIC DOMAIN CONFIGURATIONS FOR NONLINEAR OPTICAL DEVICES

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Abstract : Ferroelectric domain engineering became an attractive and perspective tool for development of a new generation of diverse nonlinear optical and acoustic converters. Conventional one-dimensional engineered domain structure represents an array of strip-like domains of a micrometer width. These domains should possess vertical domain walls through the crystal bulk of a few millimeters depth. In fabrication of patterned domain configurations by electrical poling technique, the most critical point is a domain broadening effect. There are several fundamental processes, which play a crucial role in fabrication of domain configurations, such as bulk domain nucleation, domain shapes and anisotropic domain walls propagation

Oblikovanje feroelektričnih domen pri izdelavi nelinearnih optičnih komponent

Ključne besede: optika nelinearna, KTP $KTiOPO_4$ kristali feroelektrični, naprave optike nelinearne, pretvorniki akustični, pretvorniki optični, inženirstvo, elektrooptika, piezoelektrika, piroelektrika, viri svetlobe koherentne, viri svetlobe vidne koherentne, viri svetlobe UV ultravijolične koherentne, viri svetlobe IR infrardeče koherentne

Izvleček : Inženiring feroelektričnih domen je postalo privlačno in obetajoče orodje za razvoj nove generacije različnih nelinearnih optičnih in akustičnih pretvornikov. Konvencionalna enodimenzionalna domenska struktura je sestavljena iz polja podolgovatih domen z mikrometrsko širino. Omenjene domene imajo navpične stene, ki se širijo skozi telo kristala v globino nekaj milimetrov. Pri izdelavi domenskih struktur z izbrano predlogo z metodo selektivne električne polarizacije je najbolj problematičen pojav razširitve domen. Pri tovrstnem oblikovanju domen je pomembnih kar nekaj osnovnih procesov .To so predvsem : nukleacija domen v telesu kristala, geometrija domen in anizotropno širjenje domenskih sten.

1. Introduction

Fabrication of engineered domain structures allows observing new physical properties of a ferroelectric crystal. The physical origin of this phenomenon is changes in a macroscopic symmetry of the domain-patterned ferroelectrics. Many well-known properties of ferroelectrics such as electrooptical, nonlinear optical, pyroelectric, piezoelectric, etc., which are determined by tensors of the odd ranks, may be changed by means of tailoring specific domain-engineered configurations /1/. In nonlinear optics the domain-engineered structures allow satisfying quasi-phase-matching (QPM) conditions /2/. This method enables to develop coherent light sources in UV, visible and infrared regions where compact and efficient lasers are unavailable.

In this paper the principles of ferroelectric domain engineering, peculiarities of the spontaneous polarization reversal, ferroelectric domains nucleation problem, and the domain propagation in ferroelectric materials are discussed. $KTiOPO_4$ (KTP) ferroelectric crystals have been chosen for this study, because of their wide application in nonlinear optical conversions. These crystals possess high optical nonlinearity, high optical damage resistance, and broad optical transparency.

2. Ferroelectric domain engineering

Ferroelectrics are primary ferroic (twinned) crystals where twins are distinct in the orientation of spontaneous polarization P_S. These electrical twins (ferroelectric domains) differ in the signs of every polar property of the first, third and any other odd rank tensors. Tensors of the third rank describe several important physical effects such as piezoelectric, electrooptic and nonlinear optical. In ferroic crystals twins are reoriented by external driving force that is an electric field for ferroelectrics. Therefore, external electric field reversing spontaneous polarization $\boldsymbol{P_S}$ reverses the signs of coefficients of the corresponding tensors of the odd rank. For instance, two adjacent domains with opposite direction of $\boldsymbol{P_S}$ have opposite signs of the piezoelectric coefficients. Evidently, application of the operating voltage

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to this bi-domain ferroelectric crystal causes opposite strains for each of these domains via piezoelectric effect. It was shown that ferroelectric crystals with specifically tailored domain structures might have quite different and even new piezoelectric properties in comparison with monodomain ferroelectrics /3/,/4/.

The tensor of nonlinear optical coefficients is also of the third rank and its symmetry coincides with the tensor of piezoelectric coefficients. The sign of the nonlinear coefficient **d** of macroscopically polarized regions depends on the spontaneous polarization direction and it is opposite for ferroelectric 180°-domains. This enables to realize the idea of QPM proposed by Bloembergen /2/ by introducing into ferroelectric crystal bulk a specific domain configuration where the spontaneous polarization changes its direction alternatively. Several ideas were proposed to find another domain configurations for optical frequency tuning using ferroelectric domain engineering. Multi-grating domain design implemented in the works /5/,/6/ included fabrication of 25 domain grating sections ranged the domain grating period from 26 to 32 mm in 0.25 μm increments on one $LiNbO_3$ plate. This optical chip allowed generating OPO output tuned across the entire mid-IR transparency of $LiNbO_3$ from 1.98-1.36 mm in the signal branch and in the range 2.30-4.83 μm in the idler branch. In other work /7/ the continuous tuning was reached using fan-out grating design. Another approach where Fibonacci-based structures provided by aperiodic domain configurations /8/ were considered for simultaneously phase matching two interactions.

So far, ferroelectric domains, instead of deteriorating figures of merit, which occurs for instance in pyroelectric or electrooptic devices, demonstrate a unique ability to observe new and useful piezoelectric and optical properties based on specifically fabricated domain configurations. It paved the way for development of the new field-ferroelectric domain engineering /1/.

3. Domain broadening in ferroelectric domain structures

The most promising results in fabrication of the engineered domain structures were achieved by electrical poling technique, when pulsed electric switching field is applied to a monodomain ferroelectric crystal through a photolithographically patterned electrode /1/. The fabricated domain structure represents strip-like domains of a micrometer-scale width with straight, vertical domain boundary walls throughout the crystals bulk. However, despite of a strictly defined electrode pattern, the inverted domains are often wider than the deposited electrode strips. This unwanted domain broadening effect makes it especially difficult to tailor dense domain patterns with small periods. The conversion efficiency of SHG and OPO strongly depends on quality of the tailored domain grating structure. Various types of deviations from the perfect geometrical periodicity and changes of the duty cycle and their influence on the conversion efficiency of SHG were theoretically analyzed /9/.

The domain broadening is induced by propagation of the growing reversed domain to the region, which is beyond the region limited by the switching patterned electrodes. It may be caused by widening of the growing domains due to a high tangential field between electrode strips, by bulk domain nucleation or by anisotropy of the domain walls velocity. Tangential domain widening in KTP crystals has been studied in the work /10/. Two other mechanisms of domain broadening such as anisotropic domain walls propagation and bulk nucleation of ferroelectric domains are considered.

3.1 Anisotropy of domain wall velocity

The shapes of the domain strips in the domain-grated structures induced by applied electric field depend on shapes of domain nuclei and anisotropy of the domain wall velocity. It is clear, that both factors may cause a distortion of the fabricated domain structures especially for the dense domain gratings. Our experiments have shown that KTP and isomorphic crystals demonstrate extremely high anisotropic growth of the inverted ferroelectric domains /11,12/. Dynamic ferroelectric domain shapes of the KTP crystals were studied by partial polarization reversal of a sample with uniform silver paint solid contacts applied to both polar Z-faces. The reversed domains are strongly elongated in the Y-axis direction (Figure 1). This experiment confirms that orientation of the patterned electrode along the principal axis of the ferroelectric crystals plays a crucial role in tailoring the domain configurations in these crystals. In the case of orientation of the electrode strips along the Y-axis the perfect domain grating can be fabricated (Figure 2(a)). When the electrode strips are oriented along the X-axis, the reversed domain structure does not correspond to the switching electrode pattern (Figure 2(b)). The reversed domains grow in the direction of the Y-axis and coalesce under the dielectric layer. It leads to complete polarization reversal of the ferroelectric sample.

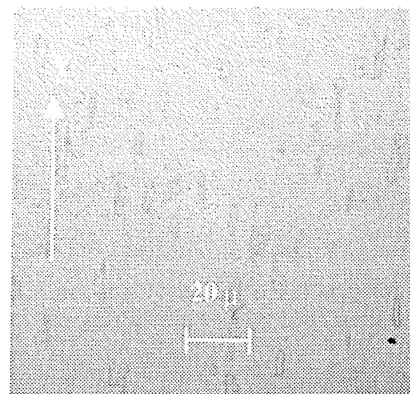

Figure 1: The optical microphotography of the etched Z-plane of KTP crystal after partial polarization switching

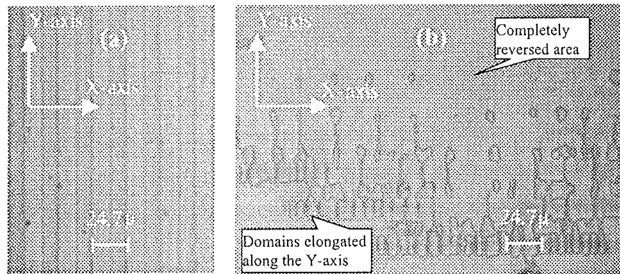

Figure 2: *The effect of the orientation of the patterned switching electrode on fabricated periodically poled structure: (a) - domain pattern obtained with the patterned electrode strips parallel to the Y-axis, (b) - domain pattern obtained with the patterned electrode strips parallel to the x-axis.*

The observed anisotropy of the domain wall velocity may be explained by a classic approach applied to the polarization reversal effect by Miller and Weinreich [/13/. They considered the mechanism of the sidewise motion of domain walls in weak fields as nucleation and subsequent growth of triangular reversed steps on 180^0 walls. The equation obtained by Miller and Weinreich for the domain walls velocity /13/ may be written in the form

$$v = v_{\infty} \exp(-\alpha b^{3/2}) \quad (1)$$

where b is the lattice constant and a is a constant depending on the parameters of the two-dimension nuclei, the applied field density and the temperature. The lattice constants in tetragonal $BaTiO_3$ are equal along the X and Y directions. As a result, the 180^0 domains observed by Miller in $BaTiO_3$ possessed rectangular forms /14/. In contrast, the crystal structure of the KTP crystals is extremely anisotropic. The lattice constant along X-axis is 12.814 Å, and it is twice less in the Y-direction: 6.404 Å /18/. According to the expression (1), reversed domains in KTP crystals should grow in the Y-axis direction, where the lattice constant is minimal. This leads to the anisotropic domain form in these crystals observed in our experiments (Figures 1, 2).

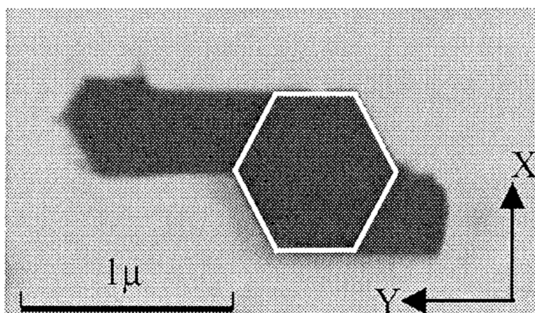

Figure 4: *Atomic Force Microscopy image of a reversed KTP micro-domain.*

Highly pronounced anisotropy of inverted domains makes KTP and its isomorphs especially attractive for fabrication of fine domain structures with periods of 1-2 micron. Our experiments using Atomic Force Microscopy demonstrated that domain nuclei of a sub-micron size in KTP crystals have a hexagonal form (Figure 3). The sidewise expansion of the reversed domains occurs by anisotropic motion of the hexagon sides in the Y-axis direction (Figure 3). Due to this extremely anisotropic motion of domain walls of sub-micron nuclei, domains with micron width oriented in the Y-axis direction could be tailored. The quasiperiodic structure for multiple nonlinear interactions with a minimal domain width 2 micron was successfully fabricated and showed good optical results. Hexagonal-shaped microdomains were observed by Dougherty *et al.* in $Pb_5Ge_3O_{11}$ ferroelectric crystals /15/.

3.2 Bulk domain nucleation

Another contribution to the domain widening is a bulk domain nucleation. According to the existing concepts /16/, compensation of the depolarization energy is a crucial condition for formation of domain nuclei with reversed spontaneous polarization. The depolarizing field may be screened by charges brought through the external circuit via switching electrodes or by the free charges existing in the crystal bulk.

Conventionally, most of ferroelectric materials are considered as ideal dielectrics with a very large dielectric relaxation time $\tau = \varepsilon\varepsilon_0/\sigma$ (e is the dielectric permittivity, and σ is the dc conductivity). TGS crystals ($\sigma \sim 10^{-18}\ \Omega^{-1}cm^{-1}$, $\tau \sim 10^6$ sec) provide a good example. In this case the polarization switching time τ_{sw} which may be several milliseconds, is much shorter than the time constant of the internal screening τ($\tau_{sw} \ll \tau$) and only the external compensation via switching electrodes process occurs. The dielectric film inserted between the switching electrode and a TGS sample totally prevents the external screening of the depolarizing field and as a result polarization switching /17/.

KTP crystals possess a very high room-temperature ionic conductivity as compared to classic ferroelectrics, due to the structure peculiarities of these crystals /18/. This conductivity is ascribed to hopping of highly mobile potassium ions through the channels existing along the polar axis. Our study of dielectric properties of these crystals shows /19/, that the cation mobility reduces with decrease of the temperature, and at the definite temperature region around T = 170 K the ionic conductivity is frozen. Measurement of the dc conductivity values of KTP crystals showed $\sigma = 5\times10^{-13}\ \Omega^{-1}cm^{-1}$ at the low temperature (T = 170 K) and $\sigma = 5\times10^{-6}\ \Omega^{-1}cm^{-1}$ at room temperature (T = 300 K).

Our experiment of polarization switching of KTP crystals with a single strip of Ti electrode (5-μm width) deposited on the +Z face of the sample confirmed that the bulk domain nucleation in these crystals is caused by their high ionic conductivity. The -Z face of the samples was coated uniformly by a silver paint electrode. The polarization switch-

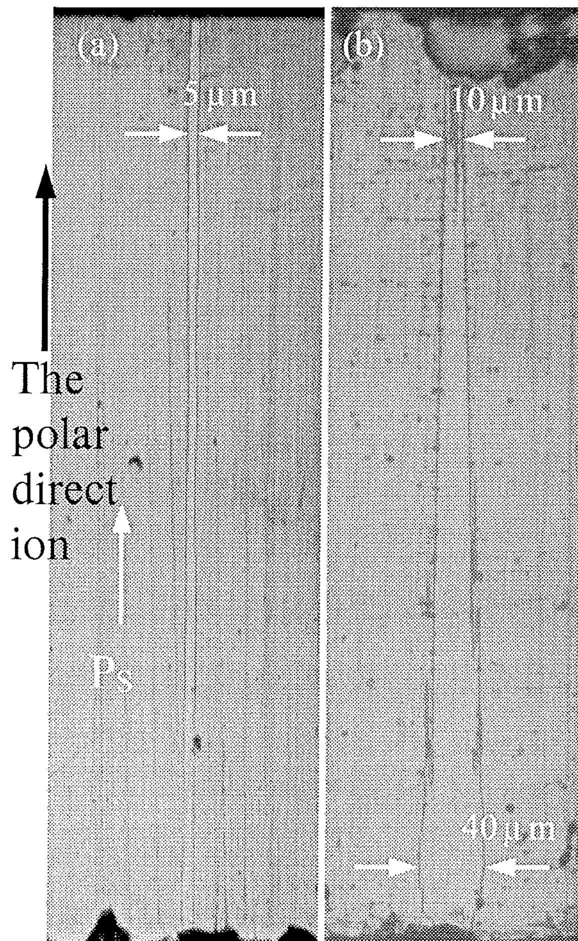

Figure 5: The view of the KTP sample polished at 45° to the z-plane and selectively etched after polarization reversal (a) at T = 170 K, (b) at T = 300 K.

ing was performed by application of square pulses of high voltage with amplitude exceeding the coercive field, where the switching time of KTP crystals is 0.1-10 ms /11,20/. At T = 170 K $\tau_{sw} << \tau = \varepsilon\varepsilon_0/\sigma \sim 1$ s. At this temperature, as could be seen from Figure 4(a), bulk nucleation does not take place. The domain propagates via the crystal bulk without any broadening preserving its initial width of 5 μm. The sample switched at room temperature ($\tau_{sw} >> \tau \sim 10^{-5}$ s) demonstrates a strong widening of the reversed domain (Figure 4(b)). In the lower part of this sample the width of the reversed domain is 40 μm, which exceeds by eight times the width of the electrode strip. In this case mobile K^+ cations contribute effectively to the internal screening of the depolarization field. Small nuclei, which were observed in the crystal bulk near the walls of the reversed domain, confirm the bulk nucleation origin of the domain broadening.

4. Conclusion

Fabrication of engineered domain structures allows observing new physical properties of ferroelectric crystals. The physical origin of this phenomenon is changes in a macroscopic symmetry of the domain-patterned ferroelectrics. It is shown that domains growing in KTP crystals in low electric field are highly anisotropic: they are elongated along the Y-axis direction. This could be explained by the difference in lattice constants along the X and Y principal axes. The shape of the micro-domains of KTP possesses a hexagonal form. A strong influence of the ionic conductivity on the polarization reversal in KTP crystals was observed. KTP crystals reversed at room temperature demonstrate strong domain broadening as a consequence of bulk domain nucleation.

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HIGH POWER SEMICONDUCTOR LASER DIODES

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Key words: semiconductors, power lasers, diode lasers, high powers, output powers up to 4 kW, edge emitting lasers, VCSEL, Vertical Cavity Emitting Lasers, COMD, Catastrophic Optical Mirror Damage, applications

Abstract : In the last decade the output power of semiconductor laser diodes has increased dramatically. Starting from a power range of several milliwatts, which is sufficient for a range of mass applications in the field of optical communication and optical storage systems, now semiconductor laser systems with an output power in the kilowatt range are available.

The progress in the development of high-power edge- and surface-emitting lasers emitting is described. The sophisticated design of large optical cavity lasers, the advanced production and mounting technology lead to usable cw-ouput powers in the range up to 70 W for a single laser bar. The concept of the monolithic vertical integration of several lasers leads to nanostack lasers with high power capabilities under short and long pulse operation. Vertical emitting lasers (VCSEL) also show promising high power performance.

The main advantage of diode lasers are the small volume, the high overall efficiency up to 60%, the availability of a wide spectral range and the high reliability. This combination together with the high output power opens a wide field of applications covering e. g. pumping of solid state lasers and amplifiers, transfer to printing plates, soldering and direct machining.

Polprevodniške laserske diode velikih moči

Ključne besede: polprevodniki, laserji močnostni, laserji diodni, moči velike, moči izhodne do 4 Kw, laserji sevajoči z roba, VCSEL laserji sevajoči s površine iz votline vertikalne, COMD poškodba zrcala optičnega uničevalna, aplikacije

Izvleček : Izhodna moč polprevodniških laserskih diod je v zadnji dekadi močno narasla. Od nekaj mW, kar zadostuje za množično uporabo na področju optičnih komunikacijah in optičnem shranjevanju podatkov, so dandanes na voljo polprevodniški laserski sistemi z izhodno močjo v kW območju.

V prispevku opisujemo napredek pri razvoju laserskih diod velikih moči z robno in površinsko emisijo. Inovativna sestava velikih optično votlinskih laserjev ter napredna proizvodnja in tehnike montaže so pripeljale do uporabnih CW laserskih izhodnih moči do 70W na lasersko palico. Koncept monolitne vertikalne integracije v laserske skladovnice pa pripelje do velikih izhodnih moči pri pulznem delovanju. Ravno tako laserji z vertikalno emisijo (VCSEL) kažejo obetajoče možnosti doseganja visokih izhodnih moči.

Glavne prednosti diodnih laserjev so majhen volumen, visok izkoristek, tudi do 60%, široko spektralno območje in visoka zanesljivost. Naštete lastnosti skupaj z visoko izhodno močjo odpirajo široka področja uporabe, kot so črpanje ojačevalnikov in laserjev iz trdne snovi, prenos slik na tiskalne plošče, spajkanje in direktno obdelovanje materialov.

1. Introduction

Laser diodes are attractive light sources due to the high conversion efficiency, the small volume, the high frequency modulation capability, the good beam quality, the wide wavelength range and the long lifetime. They find wide spread applications comprising especially optical data storage (CD, DVD) and optical communication over fibres. But also other fields are emerging like sensing, measurement and medical applications. The diode laser outperforms all other laser systems in the number of produced devices. Over the last years high power laser diodes steadily increased the performance in maximum output power and efficiency enabling new cost effective applications like pumping solid state lasers and amplifiers, transfer to printing plates and even direct machining.

2. Basics of high power laser diodes

For high power applications the semiconductor diode laser has to be specially designed to meet the specifications. The following items are common to all approaches:

- Maximum power in pulsed or cw-operation
- High overall efficiency
- Beam quality according to the application
- High reliability and long lifetime

A semiconductor laser diode is essentially a pn-diode in which the active zone is formed by a direct band gap material e.g. InGaAlAs or InGaAsP. Current is injected by forward biasing the pn-structure and leads to an excess carrier density, which is high enough to ensure optical gain by stimulated emission. In modern laser diodes the active zone consists of one or more very thin layers embedded in a material of higher bandgap forming a so-called double heterostructure. The thickness is in the range of a few nanometers and leads to quantum size effects in one direction. These quantum wells exhibit a high optical gain and the emission wavelength can be tailored by the alloy composition and the thickness. The kind of the optical resonator

divide the lasers in two principle categories, the edge- and the surface emitting lasers. Within each category a lot of different approaches have been realised in research and production leading to a wide variety of laser diodes whose description lies beyond the scope of this paper.

2.1 Edge emitting lasers

The edge emitting laser diode consists of a layer structure epitaxially grown on a substrate comprising the active zone providing the optical gain and a planar waveguide structure for the transversal confinement of the propagating optical mode. The resonator is formed by cleavage of the semiconductor along its crystal planes (Fig.1) and has a typical length from 200 to 2000 μm. In this type of laser the radiation propagates in the plane of the layers and is emitted through the mirrors perpendicular to the layers.

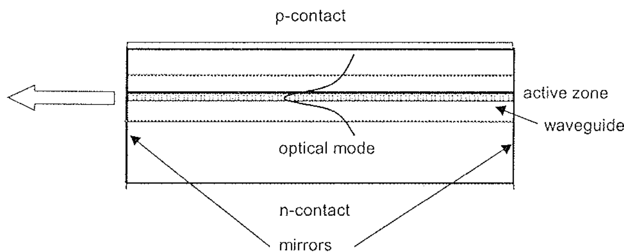


Fig. 1: Cross section of an edge emitting laser

The lateral confinement of the optical mode depends on the beam quality necessary for the application. Usually index guided structures are used for diffraction limited single mode applications e.g. for coupling into monomode fibres. For multimode operation gain guided structures are preferred due to a less demanding technology. The emission patterns for edge emitting lasers are usually characterised by an elliptical beam with different widths in the vertical and lateral direction.

2.2 Surface emitting lasers

In the VCSEL (**V**ertical **C**avity **S**urface **E**mitting **L**aser) the radiation propagates perpendicular to the layer structure. The partial reflecting mirrors are formed by layers with alternating composition and refractive index. Due to the small thickness of the active layer and the short cavity length in the order of several microns the available gain is small and the mirror reflectivities must be high close to 100 %.

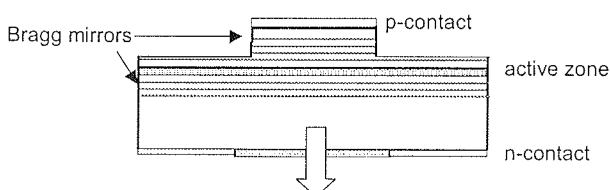


Fig. 2: Cross section of a bottom emitting VCSEL

Usually the emitting lateral aperture has a circular geometry leading to round emission patterns.

2.3 Physical limitations of the maximum output power

When a laser diode is driven by an increasing current there is a limitation of the maximum output power due different physical effects. The thermal limitation is characterised by an rollover of the power current relation and is usually reversible. The applied electrical power is not fully transferred to optical power in a laser diode, so electrical and optical losses lead to an increase of the chip temperature depending on the geometry and the thermal mounting of the device. With increasing temperature of the active zone the threshold current increases exponentially and the differential efficiency decreases. So with increasing current the output power will reach a maximum and will then decrease. Usually no permanent damage is introduced by this effect. To increase the rollover power, the internal efficiency has to be optimised by reducing the electrical and optical losses. The temperature rise can be reduced by increasing the chip area and by proper mounting of the device on heatsinks e. g. junction down where a minimum distance from the active zone to the heat removing body is achieved.

Especially in GaAlAs-based edge emitting semiconductor laser diodes another limitation occurs. At a certain level the optical power decreases suddenly and will not recover by reducing the operating current. Careful inspection of the mirror often reveal a crystalline damage due to melting in the area of the laser emission indicating a process where high temperatures occur. At the mirror surface the excess electron-hole pairs in the active zone recombine nonradiatively leading to heat generation at the surface. Due the induced bandgap shrinkage this region absorbs the generated laser radiation and the carrier density is increased. At a power density in the range of several MW/cm^3, which can easily be reached due to the strong confinement of the optical mode, there is a positive feedback leading to a thermal runaway. By that mechanism temperatures above the melting point are reached in a small volume of several cubic microns leading to permanent damage of the mirror. This so called catastrophic optical mirror damage (COMD) depends strongly on the surface recombination properties of the mirror, which can be improved by surface passivation.

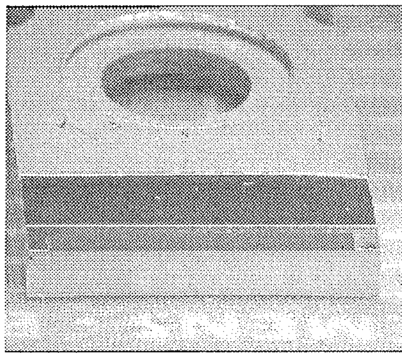
3. Techniques for increasing the maximum power

3.1 Wide aperture lasers and laser bars

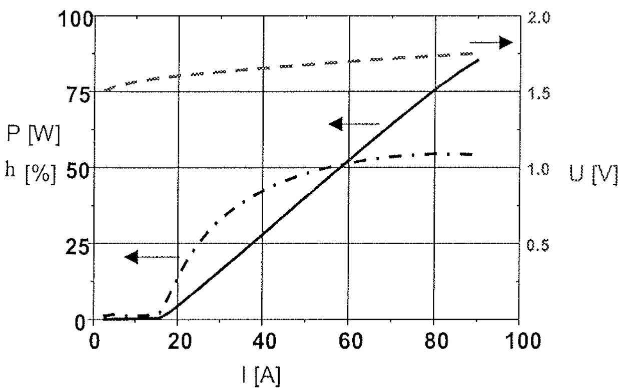
The COMD-effect depends on the optical power density at the mirror. So a straight forward strategy to increase to maximum output power of a laser diode is the increase of the emitting aperture in the lateral and transversal direction. The large optical cavity (LOC) design increases the transversal waveguide width and spreads the optical mode. This has an additional benefit in decreasing the width of the far-field distribution.

In the lateral direction the aperture is increased by array- or broadarea-configurations. In contrast to single mode laser with an aperture of several microns, the width in high power laser diodes ranges from 20 to approximately 500 µm. Due to the high mode volume several lateral modes will oscillate simultaneously and the incoherent superposition of these modes degrades the beam quality.

A further step is the monolithic integration of several broadarea or array lasers on one single bar. There is a quasi industry standard for 1cm long bars. In Fig. 3 such a bar is shown mounted on a water cooled heat sink.



a) mounted on a heatsink



b) CW-laser characteristics: Power P, wall-plug efficiency h and voltage drop U

Fig. 3: *InGaAlAs-laser bar (L=1cm)*

The characteristics of such a laser bar with an InGaAlAs double quantum well active zone for an emission wavelength of 808 nm is shown in Fig. 3b. The laser mirror are asymmetrically coated to enhance the front mirror power. The threshold current at room temperature is 18 A and the slope efficiency has a value of 1.1 W/A. Due to the low series resistance of 2.2 mΩ the wall-plug efficiency is 55 % at an output power of 60 W. The progress in the quality of the epitaxial growth process (MOVPE) and the incorporation of a single quantum well active zone led to a steady increase of the usable power of laser bars and values of 70 W with a reasonable operating time are available today.

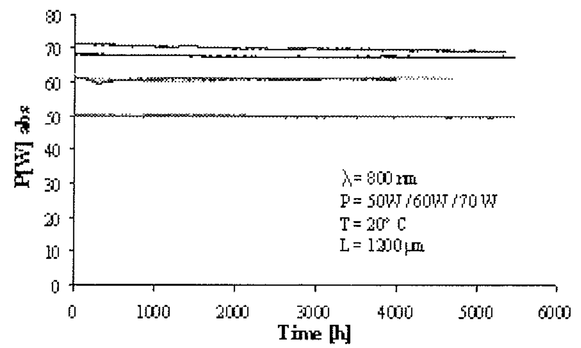


Fig. 4: *Degradation behaviour InGaAlAs-SQW laser bars at high power levels under constant current control*

Even at an output power of 70 W the degradation rate is only 0.5%/khr, which corresponds to an estimated lifetime of more than 40 khr.

Still higher output powers can be achieved by the assembly of laser bars mounted on heat sinks into modules resulting in two dimensional arrays. These modules can scale the power up to the kilowatt range. For many applications the beam quality is a crucial parameter and sophisticated combining optics have to be used to meet the specifications.

3.2 Nanostack Lasers

An unconventional way to increase the emission area of an edge emitting laser is the monolithic integration of several independent laser structures vertically /1/. The principle of the so-called nanostack laser is shown in the following Fig. 5.

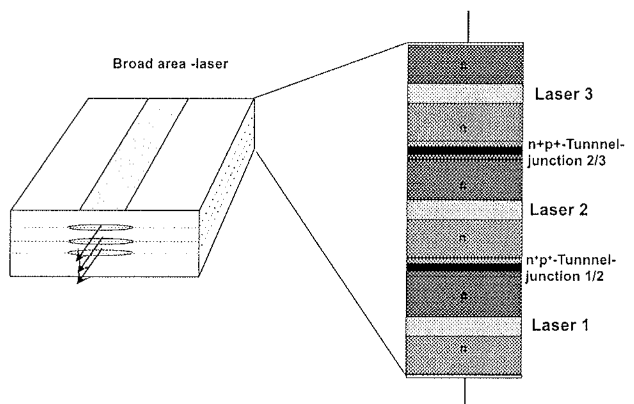


Fig. 5: *Principle of a triple-nanostack laser*

Each independent laser consists of a conventional LOC-structure with an AlInGaAs-double quantum well as active layer. In order to drive the lasers in series with high efficiency low-resistance tunnel-junctions have to be implemented. By optimizing the MOVPE growth process tunnel-junctions with a specific differential resistivity of 2.5×10^{-4} Ωcm^2 could be obtained. These junctions are suitable for the monolithic interconnection of the laser-structures.

Double and triple nanostack lasers with a specially designed transversal structure for low divergence angles have been developed. Single element broad area lasers with AR/HR-coating have been mounted junction up and tested under short pulse operation.

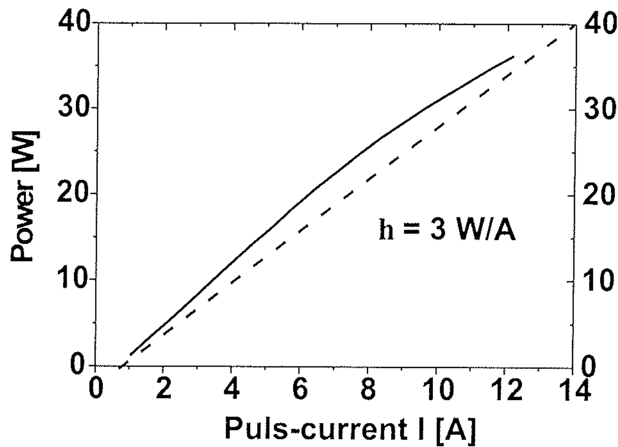


*Fig. 6: P/I-characteristic of a single broad area triple-nanostack laser (200*600 µm²) under short pulse operation (1 µs/10 kHz)*

The threshold current at room temperature is around 700 mA and the slope efficiency lies above 3 W/A. The slight bending of the P/I-curve comes from the thermal heating at high drive levels. The transversal farfield pattern has a FWHM of 23°. Under operation with short pulses (20 ns) even higher peak powers over 100 W can be obtained from a single chip. A comparison between test lasers with one, two or three integrated laser structures shows, that the slope efficiency and the turn-on voltage scales with the number of lasers. Due to the low-resistance tunnel-junctions there is no additional voltage drop which would decrease the overall efficiency. Double nanostack-lasers have been also successfully tested in the bar-configuration up to 250 W in QCW-operation with a pulse length of 200 µs and a duty cycle of 20 %.

3.3 High power VCSELs and Arrays

The benefit of VCSELs is the production and testing on a full wafer scale leading to low costs. In datacom field the VCSEL has found widespread application in single and parallel channel links. The VCSEL-concept is demanding with respect to high power applications /2/. Due to the short cavity- and gain-length high injection levels are necessary to reach threshold. On the other hand the high reflectivity Bragg-mirror introduce additional optical and electrical losses. The strategy is to minimise the series resistance and the optical absorption of the mirrors by tailoring the composition and the doping profile of the layers. For the lateral optical and electrical confinement several approaches are possible. The oxide confined structure implements an insulating aperture by lateral oxidation of an AlAs-layer /3/. In implanted VCSELs the region outside the active area is electrically and optically inactive due to a deep implantation of protons. Both versions have been tested as single VCSELs with circular apertures up to 135 µm and in arrays with a honeycomb structure of 19 elements with an aperture of 40 µm. As an example, data for an implanted bottom emitting array, mounted junction down on a TO-header, are given below. The VCSEL is realised in the InGaAlAs-system with an emission wavelength around 920 nm where the GaAs-substrate is transparent (Fig. 2).

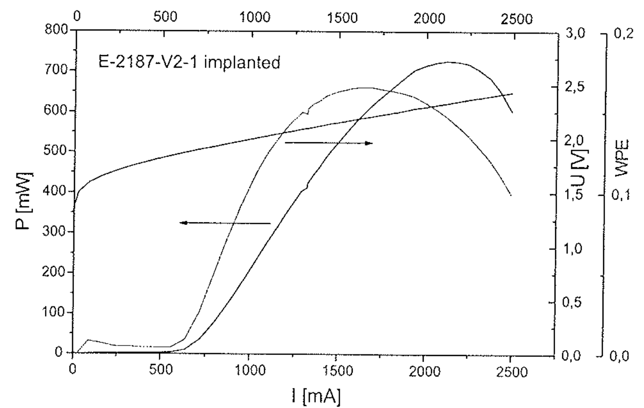
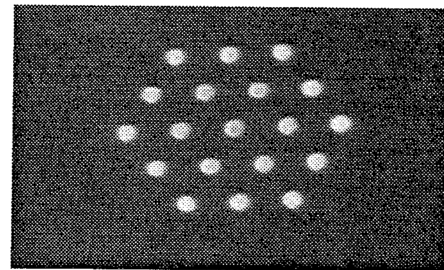
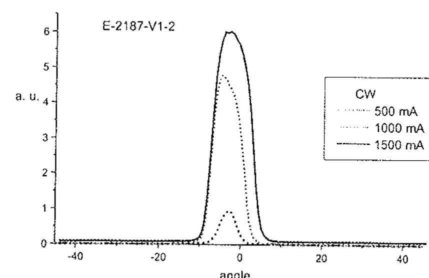


*Fig. 7: CW-laser characteristics of a 19*40µm-VCSEL-array P: output power, U: voltage drop, WPE: wall-plug efficiency*

The threshold current is 650 mA and a maximum power of 750 mW is achieved, which is limited by thermal rollover. COMD as described above is no problem for VCSELs because the active area is buried and no carriers interact with the radiation at the mirror surface. The wall-plug efficiency of 17 % is essentially lower than for an edge emitting laser, where values up to 60 % are possible.



nearfield



farfield

*Fig. 8: Emission patterns of a 19*40µm-VCSEL-array*

The nearfield pattern of the VCSEL-array shows an inhomogeneous distribution within each laser due to a high number of oscillating lateral modes. The farfield distribution at various currents is symmetric and has FWHM-values in the range between 7°-10°, which are substantially lower than typical values of 30°-40° for edge emitting lasers.

4. Applications of high power laser diodes

The attractive features of high power laser diodes like small volume, high efficiency, long lifetime and the availability of a wide spectral range open a wide field of application. The most prominent is the pumping of solid state lasers like Nd:YAG or Yb:YAG. Due to the high wall plug efficiency and the narrow spectrum laser diodes are ideally suited to replace the usually installed flashlamps, thus improving essentially the overall efficiency, the lifetime and the maintenance cost of the laser system. Today diode pumped solid state lasers with an output power of 4 kW are on the market. Due to the progress in beam combining of laser arrays the beam quality is high enough for direct application of diode lasers in industrial processes like soldering, welding, hardening or laser assisted turning of brittle materials like ceramics. The small volume of these laser system with output powers up to several kilowatts allows the integration on robotic arms for automated manufacturing processes. There are research efforts to use diode lasers directly, via solid state laser pumping and second harmonic generation to generate visible radiation with high beam quality for the application in laser television.

5. Conclusion

There is rapid progress in the development of high power edge- and surface emitting laser diodes. Due to the implementation of optimised transversal and lateral structures single laser bars with reliable powers up to 70 Wcw are available. The new approach of the monolithic integration of several lasers in a single chip leads to the nanostack-laser which has a high potential as pulsed light source for sensing applications. The high power VCSEL has a restricted maximum power and efficiency and will find niche applications where the symmetric low divergence farfield is required.

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COLOR ALIASING FREE DETECTORS

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Key words: semiconductors, microelectronics, image processing, colour images, CFA, Color Filter Array, color imagers, recording cameras, CMOS colour cameras, CCD colour cameras, colour aliasing free detectors, MOIRE effect, aliasing effect, colour separation, colour sensors, colour recognition

Abstract: Color images are commonly captured with sensor arrays covered with a mosaic of rgb-filters. Hence one-chip color imagers (CMOS and CCD color cameras) suffer from color aliasing or color moiré effects. In order to overcome these limitations color sensors based on vertically integrated diodes were realized. The complete color information of the color aliasing free sensor can be detected at the same spatial position without using additional optical filters. The color separation is realized by the wavelength dependent absorption of the incorporated material in the depth of the devices. A promising material for sensor application in the visible range is amorphous silicon and its alloys. Thin film systems based on amorphous two terminal and stacked multi terminal devices are fabricated by a low temperature CVD process. The spectral sensitivity of the sensors can be controlled by the optical and optoelectronic properties of the materials on one hand and the design of the devices on the other hand. The operation principle of the sensors will be presented and the different detection concepts will be compared regarding their application in the field of color recognition and digital imaging.

Detektorji barvne svetlobe brez motenj

Ključne besede: polprevodniki, mikroelektronika, procesiranje slik, slike barvne, CFA polje filtrov barvnih, upodabljalniki slik, kamere snemalne, CMOS kamere barvne, CCD kamere barvne, detektorji barv brez motenj, MOIRE efekt, ločevanje barv, senzorji barv, razpoznavanje barv

Izvleček: Barvne slike ponavadi zajemamo s senzorskimi polji, ki so pokrita z mozaikom RGB filtrov. Zaradi barvnega moire efekta prihaja do popačenj pri zajemu slik (CMOS in CCD barvne kamere). Izdelali smo barvne senzorje z vertikalno integriranimi diodami ravno z namenom izogniti se temu problemu. Popolno barvno informacijo brez popačenja lahko zajamemo na isti prostorski lokaciji brez uporabe dodatnih optičnih filtrov. Ločitev barv izvedemo z izbiro materialov, ki omogočajo absorpcijo v odvisnosti od valovne dolžine v različnih globinah detektorja. Obetajoči material za tovrsten senzor v vidnem področju so amorfni silicij in njegove zlitine. Z nizkotemperaturnim CVD nanašanjem smo izdelali tankoplastne strukture komponent z dvema izvodoma in večplastne strukture z večimi izvodi. Spektralno občutljivost senzorjev lahko na eni strani kontroliramo z optičnimi in optoelektronskimi lastnostmi uporabljenih materialov, na drugi pa z načrtovanjem komponente. V prispevku predstavimo princip delovanje takih senzorjev ter primerjamo različne koncepte detekcije glede na uporabo na področju zaznave barv in digitalnega upodabljanja.

1. Introduction

Color image processing is usually performed with the aid of CFA (color filter array) coated CCD or CMOS sensor arrays. However, color detection with a CFA leads to the color moiré or color aliasing effect, which is observed when structures with high spatial frequencies are captured. Furthermore, traditional sensor systems exhibit a rather limited resolution and low area fill factor, because one color pixel is split into several chromatic sub pixels. In order to overcome the color moiré effect, vertically integrated sensor structures have been proposed, which detect the color information in the depth of the sensor structure. Various sensor structures have been realized by using different materials, design concepts and contact configurations /1-12/. Nevertheless, the detection mechanism of all vertically integrated sensors can be basically described by a related operation principle. Due to the wavelength dependent absorption of the semiconductor material, photons are absorbed at various depths in the material so that the color information can be detected in the depth of the device.

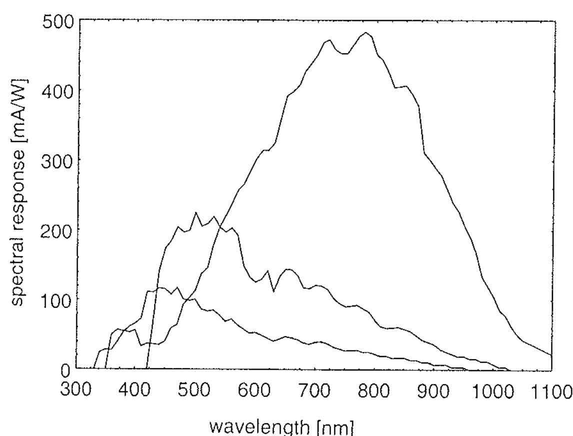

Fig. 1: Spectral sensitivity of three stacked crystalline p/n-junctions /1/.

Vertically integrated sensors based on CMOS/CCD processes were presented e.g. by Seitz et al. /1/ and Poenar et al. /2/. As example, the system of Seitz et al. consists of three vertically integrated pn-junctions fabricated by a BiCMOS process. The spectral response of the detector system is shown in Fig. 1. The color separation is limited

by the fixed optical band gap of the crystalline silicon material. To overcome this limitation and to improve the spectral sensitivity the optical band gap of the individual absorption regions has to be varied. Thus, thin film devices based on amorphous silicon (a-Si:H) and its alloys are favorable. Amorphous silicon alloys exhibit a high photosensitivity from the UVA (ultra violet A) to the near IR (infra red) part of the spectrum /13, 14/. In order to match the demand of different applications the optical band gap as well as the transport properties of the material can be controlled over a wide range by the deposition conditions. Additionally, a-Si:H multi-layer structures can be deposited on top of an amorphous, polycrystalline or crystalline active matrix array leading to significantly enhanced area fill factors of pixel-addressed sensors /15, 16/.

Several amorphous thin film detector concepts were proposed to separate the color information of the visible spectrum. The structures consist of pin-diodes with modified absorption layers /3-5/, pinip- or nipin-structures /6-8/ and more complex layer sequences /9-12/. a-Si:H thin film color sensors can be separated in two different classes. Sensors of the first class allow the separation of the color information by two terminal devices /3-9/. The color separation is realized by a shift of the collection region of the photo-generated carriers within the device due to the variation of the applied voltages. Two terminal devices are characterized by a simple structure but the sequential readout process limits the application of these devices. The second class contains color sensors based on vertically stacked diodes /10/. These sensors enable the advantage of a parallel detection of the chromatic color information at the same position, but require at least 4 interconnections between the sensor and the processing electronics. Additionally, a few combinations of these two classes (stacked diodes and detectors with a voltage controlled sensitivity) were also realized /11, 12/ resulting in devices with 3 and more terminals. In this paper different thin film sensors based on the two different sensor classes will be compared. The results of the developed structures will be presented and the advantages and disadvantages of the structure will be discussed.

2. Experiment

The samples have been deposited in a multi-chamber PECVD (plasma enhanced chemical vapor deposition) system at 210°C on glass substrates coated with flat TCO (transparent conductive oxide). The TCO layer has been realized by rf-magnetron sputtered ZnO /17/. In the case of stacked diodes, two additional TCO layers have been introduced to contact the individual diodes and to act as an etching stop during the patterning process. All detectors were patterned using photolithography and reactive ion etching. In the case of four terminal devices a simple 3-mask process was applied. For all samples, we use thermally evaporated aluminum as a back contact and the area of the test pixels ranges from 3 to 10 mm^2. In order to vary the optical band gap within the devices the amorphous silicon was alloyed with carbon or germanium using gas mixtures of silane and methane or mixtures of silane and germane, respectively. The optical band gaps of the i-layers increase with enhanced carbon content and decrease by alloying germanium. P- and n-type doped layers were realized by adding trimethylboron and phosphine, respectively. A detailed description of the deposition parameters is given elsewhere /14, 18/. The optical band gap of the a-Si:H layers was deduced from optical reflection and transmission measurements using separately prepared samples.

3. Results

3.1 Color detector based on a two terminal nipiin structure

Nipiin structures basically consist of two anti serial connected diodes. Applying different bipolar voltages generates the three color signals. The spectral response of a nipiin three color detector with modified band gaps and different $\mu\tau$-(mobility lifetime)-products in the i-layers of the top and bottom diode is shown in Fig. 2. The maximum of

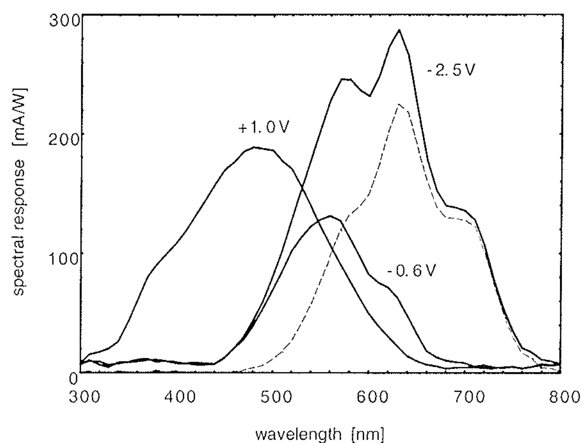

Fig. 2: *Measured spectral response of a nipiin three-color sensor at applied voltages of V = 1.0V, -0.6V and −2.5V (solid line) and the calculated difference between the sensitivity at V = -2.5V and V = -0.6V (dashed line).*

the voltage controlled spectral response of the sensor shifts in the bias range between V = -2.5V and V= 1.0V from red to green and blue. The spatial distribution of the band gap and the $\mu\tau$-product is given schematically in Fig. 3. A silicon carbon layer with an optical band gap of 2.0 eV and a thickness of 125nm defines the absorption region i^{I} in the top diode. The layer i^{II} is deposited by amorphous silicon. The optical band gap and the thickness, d_i, is 1.75 eV and 200nm, respectively. In order to get a high absorption for photons with low energy, region i^{III} was fabricated by a silicon germanium layer with an optical band gap of 1.65 eV.

The behavior of the color sensor can be explained as follows: The application of different voltages causes distinct band bending and changes the preferential collection region of the photo-generated carriers within the absorption regions of the device. For positive applied voltages the generated carriers in the reverse biased top diode are collected, while the photo generated carriers in the forward biased bottom diode recombine. Thus the photocurrent of the device is determined by the absorption within the top diode. The spectral response of the device exhibits blue sensitivity with a maximum at 480nm as a result of the high absorption coefficient of a-SiC:H for light with shorter wavelengths and low absorption for light with longer wavelength. An increase of the positive voltage enhances the spectral response only slightly, because wide band gap material with low defect density was employed in the top diode. Hence, in this region nearly all photo-generated carriers are extracted at low reverse bias (Fig. 2). At negative voltages the photocurrent is determined by the electrons and holes generated and collected in the bottom diode, whereas the photo-generated carriers in the top diode recombine.

To achieve a high linearity and linearly independent spectral response curves the band gap of the absorption layers must decrease from the front contact to the back contact, whereas the $\mu\tau$-product of the layers in the bottom diode increases from the n-layers to the p-layer (Fig. 3). For the

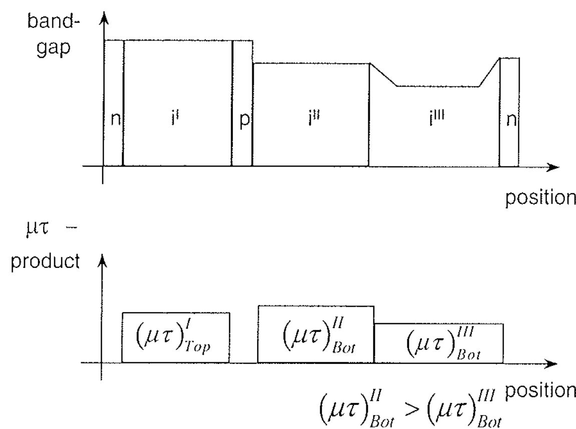

Fig. 3: Band gap and $\mu\tau$-product of a nipiin three-color sensor.

green/red separation at low negative voltages an a-SiGe:H-layer is introduced in the rear part of the absorption layer in the bottom diode, since a small amount of germanium alloyed to amorphous silicon increases the defect density and reduces the ambipolar diffusion length in the a-SiGe:H material /18/. Thus, the i-layer of the bottom diode consists of two regions with different $\mu\tau$-products. At low negative bias (-0.6 V) mainly the carriers generated in i^{II}-layer are extracted, while the carriers in the rear part of the bottom diode (i^{III}-layer) recombine. Thus, the device is sensitive to green light and the spectral sensitivity exhibits a maximum at 560nm. The recombination of carriers in the rear part is caused by the low $\mu\tau$-product combined with the low electric field within the i^{III}-layer. All carriers in the bottom diode are collected at high negative bias and the device yields a maximum of the spectral response for red illumination (630nm) at V = -2.5V. The spikes of the spectral response for longer wavelength, especially, at V = -2.5V can be attributed to interference effects within the whole layer stack. In this case the product of the absorption coefficient of the material and the layer thickness is smaller than the penetration depth of the photons for longer wavelengths.

At higher negative voltages the measured signal is determined by green and the red light. In order to separate the red signal from the measured signal at higher negative bias, the green response detected at low negative bias has to be subtracted. The dashed line in Fig. 2 indicates the difference between the two curves and demonstrates the good color separation of a nipiin color sensor. For accurate color recognition the measured spectral sensitivities can be converted into a standard color space (e.g. CIE) /19/. However, the subtraction and the transformation of the sensitivities into a standard color space assume that the spectral response curves are linear independent. For this device design three linear independent spectral response curves were achieved /20/.

Besides the separation of linear independent curves of the spectral response, a high dynamic and a good linearity are necessary to apply a detector for image processing. Since no saturation of the photocurrent is observed for realistic illumination conditions (< 10000 lx) the dynamic range of the device is defined as the ratio between the photocurrent under 1000 lx white light illumination and the dark current. A high dynamic can only be realized by using low color sensitive voltages, in order to avoid a distinct increase of the dark current /7/. The nipiin three-color detector optimized for low voltage color sensing exhibits a dynamic range exceeding 90 dB in the active color detection range from -2.5V to +1.0V (Fig. 4). The dark current increases

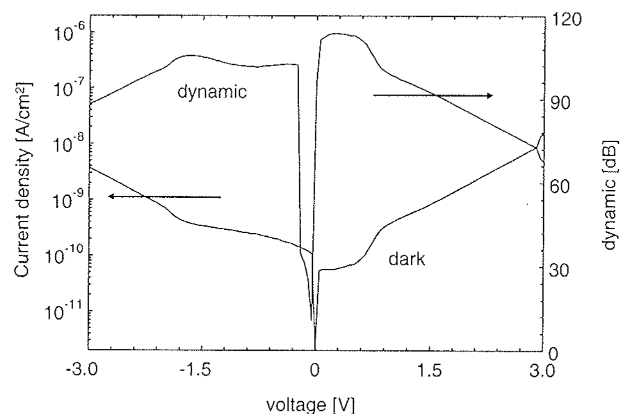

Fig. 4: Dynamic and dark current of a three-color nipiin sensor.

for higher voltages thereby limiting the dynamic performance of the color detector. Numerical modeling of the dark

I/V-curves reveals that for higher positive bias (V > 1.0V) the p-layer is flooded with electrons caused by the thin top diode. More insight into the transport and recombination model is given elsewhere /7/. The examination of the photocurrent as a function of the incident photon flux reveals that the nipiin sensor is highly linear over a wide range of intensity. The photocurrent can be described by a power law expression with an exponent close to one (0.95-0.98).

The delay time of the transient photocurrent after voltage switching is a further criterion of the detector performance, since a red/green/blue (RGB) signal can be generated sequentially after switching the applied voltages. The curves in Fig. 5 show the maximum frame rate for an optimized G-R-B-switching sequence as a function of the photon flux. The frame rate describes the reciprocal value of the sum of the photocurrent delay times t_d after switching from +1.0V to -0.6V, -0.6V to -2.5V and from -2.5V to +1.0V and an integration time of 1.5 ms of the signal (0.5 ms per color) using an additional read out electronic. A nearly linear relationship between the frame rate and the photon flux (ϕ) is observed for $\phi > 3{*}10^{11} cm^{-2}s^{-1}$, whereas a wavelength dependent hyper linear correlation is detected for lower ϕ. This hyper linear behavior is caused by the influence of the dark current and the recharging behavior in the dark, which is dominated for such low levels of intensity (moon light). A nearly linear correlation is found for high ϕ, since the integration time is much smaller than the total delay time of the sensor. Thus, color recognition is possible for frame rates above or equal to the curves in Fig. 5. For frame rates below the curves a color lag has to be considered, since the sum of the delay times and integration times is greater than the minimal requisite time to reach the steady state photocurrent.

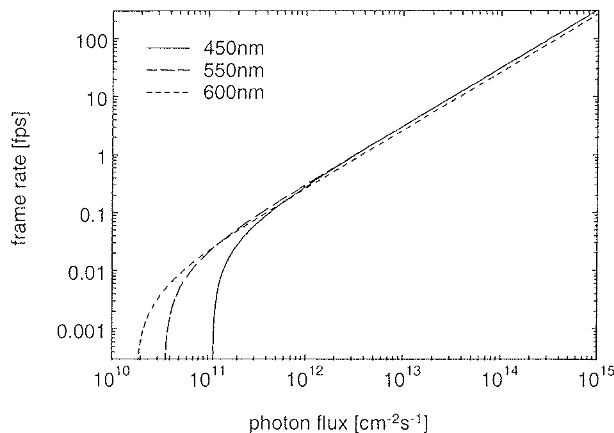

Fig. 5: Frame rate for an optimized RGB-switching sequence as a function of the photon flux for different wavelengths.

The strong illumination dependence of the transient response complicates the application of detector systems based on two anti serial connected diodes (as nipin or pinip-detectors) for color detection. Particularly, for low levels of illumination a deconvolution of the signal is necessary. A detailed analysis of the transient phenomena are discussed in detail elsewhere /21, 22/.

A 2-color detector array with 256x256 pixels was successfully demonstrated by Mulato and coworkers /23/, which combines pinip-structures with TFT read-out electronics. However, based on the previous discussed transient behavior real time imaging is restricted. In order to overcome these limitations, unipolar sensors based on a pin diode with modified absorption regions have been developed. Additionally, due to operating voltages of only one polarity, the structure is further on compatible to standard CMOS circuits.

3.2 Color detector based on a two terminal unipolar piiin structure

In Fig. 6 the schematic band diagram (a) and $\mu\tau$-product (b) of a piiin structure is shown. The optical band gap and

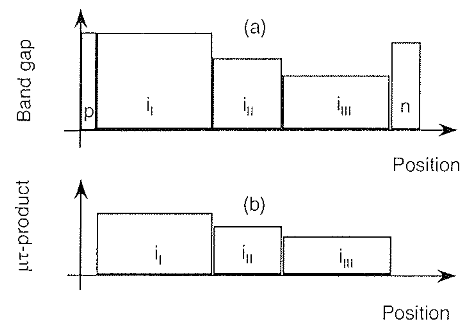

Fig. 6: Schematically spatial distribution of the band gap (a) and the $\mu\tau$-product (b) of a piiin structure.

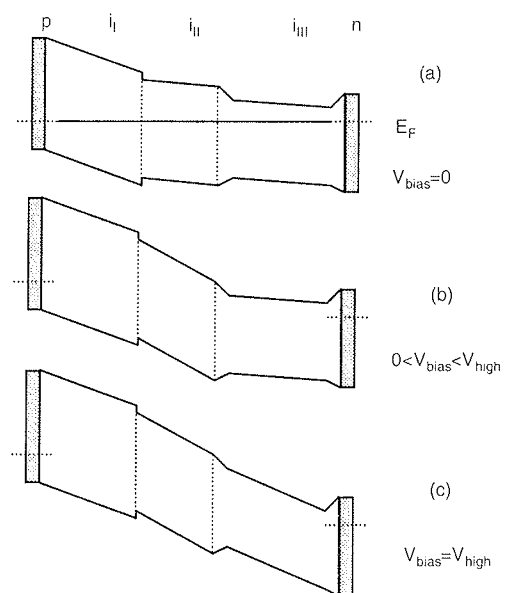

Fig. 7: Schematically band scheme of a pin structure according to Fig. 6 for short circuit (a), inter mediate reverse bias (b) and high reverse bias (c) conditions.

$\mu\tau$-product of the absorption layer decreases from the p- to the n-layer, to facilitate color separation. An amorphous silicon carbon layer with an optical band gap of 2.0eV and a thickness of 110nm was incorporated as absorption layer i^I. In region II material with an optical band gap of 1.8 eV and a thickness of 90nm is employed. For red light detection in the rear part (region III) an a-SiGe:H layer is introduced with an optical band gap of 1.65eV.

The schematic band structures for different applied voltages are shown in Fig. 7 to describe the electronic transport and the extraction of photo-generated carriers. Under short circuit conditions a strong band bending is observed only in the front part of the absorption layer (Fig. 7a). Thus, only the photo generated carriers in region I can be extracted, whereas the electric field in region II and III is not high enough to collect the photo-generated electrons and holes. In the case of intermediate reverse voltage the electric field in region II is enhanced and in addition to the extracted carriers from region I the carriers in region II are collected and contribute to the over-all photocurrent. The generated carriers in region III still recombine. In the case of a high reverse voltage applied to the piiin structure the electric field is high enough to extract nearly all photo-generated carriers. The spectral sensitivity of a piiin structure (solid lines) is shown in Fig. 8. The sensor exhibits a maximum of

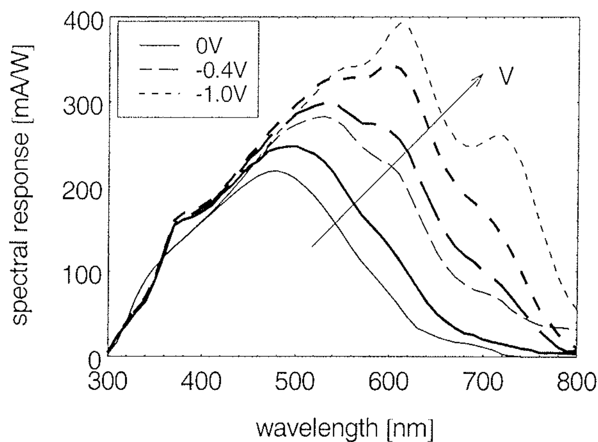

Fig. 8: Measured spectral response (bold lines) at 0V, -0.4V, -1.0V applied voltages and optically simulated data (thin lines) of a piiin diode.

the spectral response at 500nm measured under short circuit conditions. An increase of the reverse bias up to -0.4V leads to the extraction of photo-generated carriers out of region I and II and the maximum of the sensitivity shifts to 540nm. At high reverse bias (V = -1.0V) nearly all photo-generated carriers were extracted out of the whole i-layer. Consequently, the spectral response shifts to longer wavelengths detecting a maximum at 600nm.

To gain deeper insides into the behavior of the sensors we modeled the optical behavior of such a complex detector system, because all layers of the layer stack have an influence on the device characteristic. The program uses the complex refractive indices of each layer as input parameter. The calculated optical generation profiles have shown that mainly blue light is absorbed in region I, whereas green light is mainly absorbed in region I and II and red light in region III /4/. In order to compare the simulations with the measured spectral response data, we integrated the generation profiles in the three regions of the absorption layer. Neglecting the electronic losses (recombination) the spectral response determines the lower and the upper limit of the sensitivity. Under short circuit conditions the measured spectral response is higher than the simulated curve, which considers only the photo-generated carriers of region I. The higher photocurrent can be attributed to the extraction of generated carriers out of region II and III. At high reverse voltage the experimentally determined spectral response is smaller than the simulated curve. This difference can be explained by recombination losses of carriers especially generated in region III. The result indicates, that for blue and green illumination carriers generated in the middle and rear part of the structure contribute to the photocurrent. Since the collection efficiency of these carriers depends strongly on the applied voltages, the linearity of the device is resticted /4, 24, 25/. Especially, the linear independent spectral response curves at intermediate voltages complicate or prevent an accurate color acquisition /4/. However, linear independent curves can only be guaranteed by the application of one sensor for each individual chromatic signal.

3.3 Color sensors based on vertically stacked p-i-i-n diodes

3-channel sensors based on three vertically stacked pin diodes allow the simultaneous detection and read-out of the sensor signals. Furthermore, the spectral response curves are linear independent. A pre-processing electronic can perform the read-out process, which latches, processes and transfers the signals to a color-processing unit. In opposite to nipiin or piiin structures discussed above the photo-generated carriers can be stored within the diode and no additional pixel capacity is needed. This possibility reduces the required area for the pixel electronic and simplifies the shrinking of the pixel pitch. The multilayer system consists of three vertically integrated diodes (Fig. 9). After the deposition of the complete layer stack

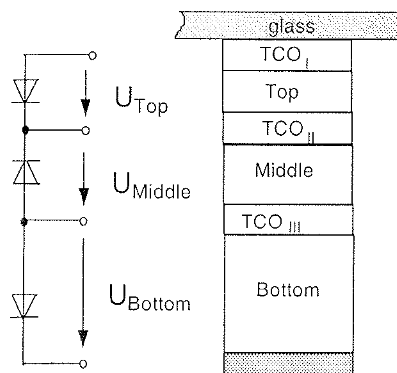

Fig. 9: Schematic configuration of a 3-channel sensor based on three vertically stacked diodes.

the diodes were patterned by a 3-mask process to contact the individual terminals. The sensor has been illuminated through the glass substrate. The spectral response curves of the 3-color detector (Fig. 10), measured under short circuit conditions, exhibit a maximum at 410nm, 535nm

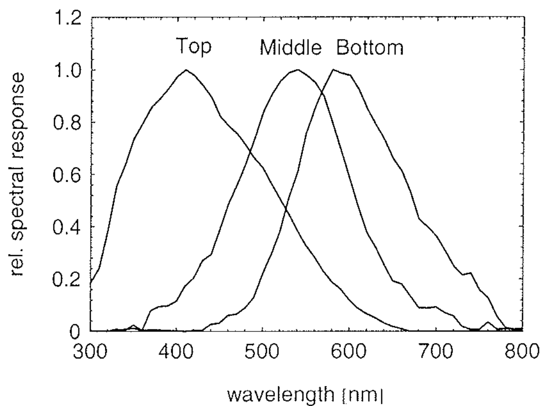

Fig. 10: Measured spectral response of a 3-channel sensor based on three vertically integrated pin diodes. The sensitivity is measured under short circuit conditions.

and 590nm and a Full Width at Half Maximum (FWHM) of 195nm, 147nm and 144nm, respectively. The preferential absorption of blue, green and red light is detected in the top, middle and bottom diode, respectively, by adjusting band gap and thickness of the absorption layers. The optical band gap of the absorption layers in the top, middle and bottom diode is 2.2 eV, 1.9 eV and 1.75 eV, respectively, by alloying carbon to the deposition gas silane. The amplitudes of the spectral response curves differ by less than a factor of 3. However, the color separation of green light in the different diodes is only moderate. The photocurrent of the top diode of the 3-channel detector under blue (λ = 450nm) and green (λ = 550nm) illumination differs only by a factor of around 2.5. In comparison, a CCD camera coated with optical filters has a separation ratio of more than 40 between blue (450nm) and green light (550nm) /26/. This effect is caused by the lack of optoelectronic materials with a high optical band gap and good electronic properties. A detailed analysis of the optical properties and colorimetric characterization of the sensor is given elsewhere /27/.

The dynamic range for all three diodes exceeds 80 dB in the bias voltage range from 0V down to -0.5V. For the middle and bottom diode, the dynamic is above 90 dB; since the dark current is lower than $2x10^{-10}$ A/cm^2 under reverse bias voltage of -0.5V.

3.4 Stacked color sensors comprising detectors with a voltage controlled sensitivity

One of the simplest ways to generate linear independent spectral response curves and to minimize the interconnections between the detector and the electronic based on the combination of a pinip or nipin system with a pin diode /11/. A different attempt is shown in Fig. 11. The sensor system consists of three stacked pinip diodes. A preprocessing electronic can perform the read-out process, which latches, processes and transfers the signals to a color-processing unit (Fig. 11). A reduction of the mismatch

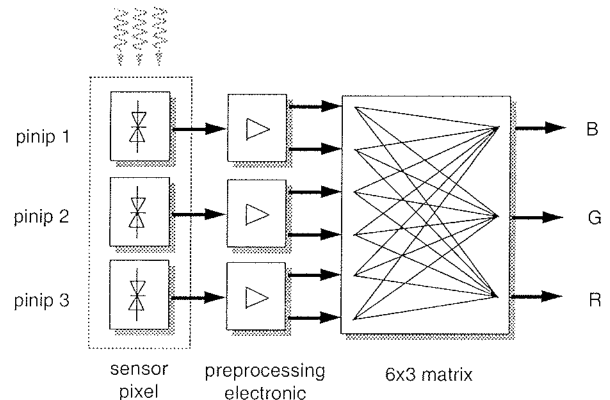

Fig. 11: Schematic configuration of a 6-channel sensor in combination with a preprocessing electronic and color processing unit.

between the spectral sensitivity of the color detector and the human eye can be achieved by the generation of more than three linearly independent spectral response curves. Thus, we have realized a 6-channel sensor, which can be read-out by two shots.

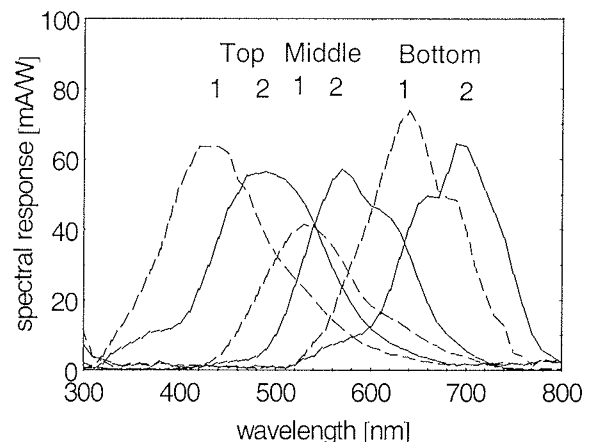

Fig. 12: Measured spectral response of 6-channel sensor. Curves 2 are measured applying 1.0V (solid lines) and curves 1 are measured applying -1.0V (dashed lines) bias voltages on the pinip-diodes of the different terminals.

Pinip structures show an operation principle similar to nipiin structures. At negative applied bias voltages, the top diode is reverse biased, whereas the back diode is forward biased. The photocurrent is determined by the reverse biased front pin diode. Changing the applied voltage from -1.0V to +1.0V shifts the preferential collection region of

the generated electron/hole pairs from the front to the bottom part of the individual pinip structures. The spectral response of the rear diode shifts to longer wavelengths, because the first part of the pinip structure acts as an optical filter. After transferring the sensor signal from the detector to the pre-processing electronic the signal is latched and the applied bias voltage is changed. Depending on the pre-processing electronic, the sensor signal can be either transferred sequentially or parallel to the color-processing unit. Afterwards a 6x3 matrix transforms the sensor signals into a standard color space like CIEXYZ. Fig. 12 shows the measured spectral sensitivity of the 4-terminal device with maxima at 430nm, 490nm, 530nm, 570nm, 640nm and 690nm. The spectral response curves with FWHM of 128nm, 133nm, 111nm, 120nm, 113nm and 116nm, respectively, can be taken by two shots, without using optical filters. A very good adjustment of the optical absorption for this device structures is achieved because the maxima of the spectral response vary by less than a factor of 1.8. The dynamic of the three pinip-structures exceeds 75dB in the bias range of +1.0V/-1.0V.

4. Discussion

In the following we discuss the different sensor concepts. We will focus only on voltage-controlled two terminal detectors and detectors based on three stacked p-i-n-diodes. The 6-channel sensor will not be discussed here, because the device combines the advantages and disadvantages of voltage-controlled two terminal and multi-terminal devices. The performance of the sensors is summarized in Tab. 1. The nipiin and piiin structures are specified by a simple contact configuration and a sequential read-out process, whereas the stacked sensors are stated by a more complex contact configuration. But in the latter case all channels can be read out at the same time. As a consequence of the different contact configurations, an additional pixel capacitor is required to store the photo-generated charge of the nipiin and piiin structures.

Device	nipiin	piiin	stacked p-i-n diodes
Color separation	moderate	moderate	good
Terminals	2	2	4
Dynamic	80-90dB	80-90dB	80-90dB
Linearity	good	good	very good
Processing	≥ 1 mask	≥ 1 mask	≥ 3 masks
Read out	External capacitor	External capacitor	Charge storage mode
Application	Color recognition	Color recognition	Digital Photography

Tab.1: *Comparison of the device performance of thin film color sensors.*

All presented sensors exhibit a dynamic range exceeding 4 orders of magnitude. The photosensitivity of the sensors deviates only by a factor of 2, so that the dark current of the devices mainly determines the dynamic. For the two terminal devices the material with the highest defect density primarily determines the dark current, which is typically employed in the rear part of the sensor. Furthermore, the dark current of the nipiin structure for higher voltages is influenced by the flooding of the central p-layer with electrons /7, 22/. In contrast to the limitation of the bottom diode of the nipiin structure, the dynamic of the stacked sensor is limited by the properties of the top diode. Due to the thin absorption layer of the top diode the current is influenced by micro shunts. Although the device design differs significantly, similar dark currents are measured for two terminal and stacked diode sensors. Therefore, the application of amorphous silicon based sensor is only limited for very low levels of intensity. A common feature of two terminal device structures is the distinct transient behavior, which limits real time imaging. A further aspect, which is of interest to compare different sensors, is the color separation. The spectral response curves of the piiin detector are very broad, which leads to noise problems when the RGB-signal is detected. Additionally, the spectral sensitivities depend on the illumination conditions. The linear independence of the color separation of the piiin sensor is significantly reduced in comparison to a nipiin and a stacked sensor structure. Especially, for intermediate bias voltages (green sensitivity) the sensor exhibits a linear dependence of the spectral sensitivity, which will hinder accurate color recognition.

In general, all color sensors or color sensor arrays (with and without optical filters) exhibit restrictions if the performance is compared with human vision. The mismatch between the human perception of color and the performance of technical sensors leads to metameric errors. Hence, the color space of the detector and the color space of the human eye represented by the colorimetric standard observer (CIE 1931) have to be matched /19/.

In contrast to sensors with color filters, which facilitates a reduction of the color error by the individual tuning of the filters for red, green and blue, the absorption within the individual i-layers of the presented color aliasing free sensors can not be independently optimized, because the sensor channels or absorption regions are vertically integrated. Hence, the color separation of the two terminal devices exhibit a moderate and the stacked color sensor a good color separation. Due to the detection of more than one color within one diode of the two terminal devices a special design of the diodes is required. As a result of these constraints the color separation of the sensors is limited by the optical and the transport properties of the material. Only certain materials fulfill the requirement to be employed in two terminal color sensors. The color sensors based on vertically integrated diodes are more or less only limited by the optical properties of the material. Thus, the device designer has higher flexibility in adapting the color separa-

tion to the required application in comparison to the two terminal devices. However, the spectral sensitivity of the top diode of the 3-channel sensor is mainly determined by the absorption within this diode. The spectral response of the middle and bottom diode is also influenced by the transmission properties of the layers arranged in direction of the incident light. For example: the sensitivity of the green and the red channel is determined by the design of the individual diodes and the absorption/transmission of the diode for blue and blue/green, respectively. As a consequence an individual modification of one sensor channel is only possible to a certain scope. In spite of this drawback, the color error of the stacked sensor system has been reduced to the level of commercial sensor arrays with optical filters /27/.

We have shown that nipiin and piiin structures are very good candidates for low cost applications, which require a moderate color separation and no real time imaging. The concept of vertically integrated pin diodes is more complex but the high flexibility in tuning the spectral sensitivity exhibits potential for high-end applications like multi spectral technology, digital photography or document archiving.

5. Conclusion

Novel amorphous silicon multi-spectral color detectors based on two terminal devices and stacked thin film structures have been developed and the optoelectronic properties of these devices have been discussed and compared. The thin film structures enable color aliasing free color detection. Accordingly, the complete color information can be detected at the same position without the aid of optical filters. The color separation is realized by the wavelength dependent absorption in the depth of the material. In order to match the demands of different applications the optical as well as the electronic properties of the individual regions of the device can be optimized due to the flexibility of the PECVD process. In combination with an amorphous or crystalline silicon active matrix read out electronic the color sensors permit the realization of imagers with a high area fill factor, reduced pixel pitch and a good color resolution. The nipiin and piiin structures are very good candidates for low cost applications, which require a moderate color separation and no real time processing of the sensor data. The multi-layer structure based on vertically stacked diodes is more complex but the high flexibility in tuning the spectral sensitivity reveals high-end applications like multi spectral technology or document archiving.

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OPTICAL-FIBER COMMUNICATIONS: COMPONENTS AND SYSTEMS

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Key words: optical communications, optical fibers, components, systems, state of the art, design, limitations, capacities, optical terminals, terminal equipment

Abstract: Optical-fiber communications brought a revolution to communication technology, outperforming other communication systems by several orders of magnitude in transmission capacity, unrepeated and repeated communication range and decreasing installation and operating costs. The optical-fiber revolution started approximately 30 years ago, when technology improvements decreased the optical-fiber loss to less than 20dB/km. The theoretical loss limit for silica (SiO_2) based fibers was reached only 10 years later, but the fiber handling and line-terminal technology was far from mature at that time.Even with primitive line-terminal technology, optical fibers immediately outplaced coaxial-cable systems and decreased the importance of microwave and satellite point-to-point radio links. In the last two decades, significant improvements have been made in the line-terminal technology, including narrow-spectrum solid-state lasers, wide-bandwidth modulators, laser optical amplifiers, fast and sensitive photodetectors and last but not least, high speed electronics. Although advanced laboratory experiments are quickly approaching the theoretical capacity offered by the >10 THz bandwidth of a single-mode optical fiber, several problems have yet to be solved to make high-capacity systems viable, including linear and nonlinear propagation effects in the optical fiber itself, high performance electro/optical and opto/electric converters, efficient high speed electronics and all-optical signal-processing components. The purpose of this presentation is to summarize the present status of optical-fiber communication technology, to discuss the basic components and the limitations of these devices, and to present the requirements and proposals for future systems.

Komunikacije po optičnih vlaknih : Gradniki in sistemi

Ključne besede: komunikacije optične, vlakna optična, komponente, sistemi, stanje razvoja, snovanje, omejitve, kapacitete, terminali optični, oprema terminalna

Izvleček: Zveze po optičnih vlaknih so prinesle revolucijo v tehnologijo telekomunikacij, saj omogočajo za več velikostnih razredov večjo zmogljivost, večji domet brez in z regeneracijo ter nižje nabavne in obratovalne stroške. Revolucija optičnih vlaken se je začela pred približno 30 leti, ko so izboljšave tehnologije znižale slabljenje optičnega vlakna pod 20dB/km. Teoretska meja slabljenja za vlakna iz kremenovega stekla (SiO_2) je bila dosežena že 10 let kasneje, toda rokovanje z vlakni in terminalna oprema sta bila zelo daleč od zrelosti v tistih časih. Celo s preprosto terminalno opremo so optična vlakna takoj zamenjala sisteme s koaksialnimi kabli in zmanjšala pomen mikrovalovnih in satelitskih zvez točka-točka. V zadnjih dveh desetletjih se je tehnologija terminalne opreme bistveno izboljšala, vključujoč ozkopasovne polprevodniške laserje, širokopasovne modulatorje, laserske optične ojačevalnike, hitre in občutljive fotodetektorje in nenazadnje hitro elektroniko. Čeprav se vrhunski laboratorijski poskusi hitro približujejo teoretski meji, ki jo omogoča pasovna širina >10THz enorodovnega optičnega vlakna, številna vprašanja okoli praktične uvedbe visokozmogljivih sistemov ostajajo odprta, vključujoč linearna in nelinearna popačenja prenosne poti po optičnem vlaknu, visokozmogljive elektrooptične in optično/električne pretvornike, učinkovito hitro elektroniko in gradnike za vseoptično obdelavo signalov. Namen te predstavitve je prikazati sedanje stanje komunikacij po optičnih vlaknih, razložiti osnovne gradnike in njihove omejitve ter prikazati zahteve in predloge za bodoče sisteme.

1. Optical fiber design

Optical fibers are members of a much broader group of dielectrical waveguides. Dielectrical waveguides potentially offer wide bandwidths and low insertion loss due to the absence of metals and related ohmic losses. Although the principles of operation of dielectric waveguides were known for a long time, practical low-loss optical fibers were only manufactured three decades ago.

The design of a low-loss, high-capacity optical fiber is shown on figure 1. The main dielectric material is pure silica (SiO_2) glass. Some germanium oxide is added to the core to raise its refraction index to allow the operation as a waveguide. The dimensions of the cladding (125um) and

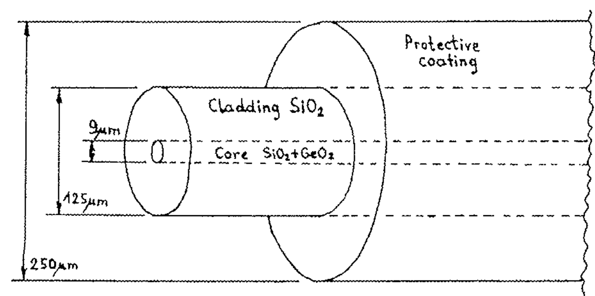


Figure 1: Optical fiber construction.

protective coating (250um) are standardized to allow interconnections among products from different manufacturers. The diameter and refraction index of the core are care-

fully selected for the required numerical aperture (NA) and single-mode operation at the desired optical wavelength.

The attenuation of a silica-based optical fiber is shown on figure 2. While the impurity content can be reduced by better manufacturing techniques and UV absorption only plays a secondary role, the attenuation of a silica-based optical fiber is mainly determined by the Rayleigh scattering and IR absorption. Silica fibers acheive their minimum insertion loss of about 0.2dB/km at optical wavelenghts of around 1.55um (194THz).

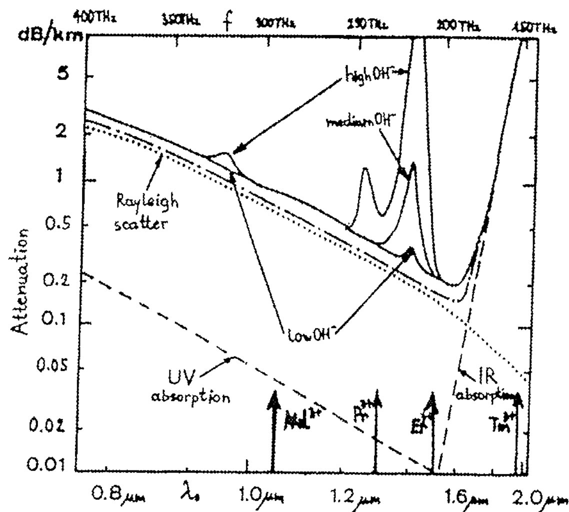


Figure 2: *Optical fiber attenuation.*

The attenuation of optical fibers is several orders of magnitude lower than competing metal cables, while their bandwidth is several orders of magnitude larger due to the carrier frequency in the optical region. Optical fibers therefore have several potential advantages over competing technologies.

2. Optical fiber limitations

Silica optical fibers also have a few limitations. Low-loss fibers acheive a low numerical aperture (NA around 0.1). The core size of single-mode optical fibers is very small (10um). It is therefore particularly difficult to couple light into an optical fiber as shown on figure 3. A large degree of spatial coherence is required from the light source.

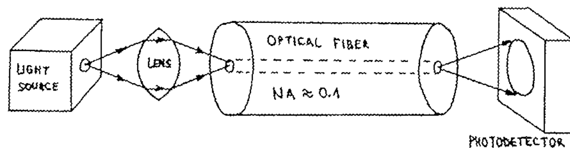


Figure 3: *Light source and photodetector coupling.*

Semiconductor lasers are usually used to acheive a high coupling efficiency of around 50% and a launched power up to a few hundred milliwatts into a singlemode fiber. Light-emitting diodes can also be used, but due to their incoherent nature, the coupled optical power into the fiber is very small, only a few microwatts into a singlemode fiber. The performance of optical-fiber links may be already limited by the insufficient power launched into the fiber as in the case of incoherent (LED) transmitters.

When a high coupling efficiency is obtained and sufficient light power is launched into a singlemode fiber, other effects may limit the link performance as shown on figure 4. When using broadband sources like (longitudinal) multimode, Fabry-Perot semiconductor lasers, the link performance may be limited by linear chromatic dispersion. Such links usually operate around 1.3um, where the linear chromatic dispersion is minimal for conventional singlemode fibers.

(A) Linear chromatic dispersion:

$$\Delta t = D_\lambda \cdot \Delta\lambda \cdot l$$

$$D_\lambda = -\frac{\omega^2}{2\pi c_0} \cdot \frac{d^2\beta}{d\omega^2}$$

D_λ [ps/(nm·km)]: 20, 10, 0, -10, -20; λ [μm]: 1.1, 1.2, 1.3, 1.4, 1.5, 1.6

(B) Nonlinear refraction coefficient (Kerr effect):

$$n(P) = n_0 + n_2 \cdot \frac{P}{A_{eff}}$$

$A_{eff} \approx 80\mu m^2$

$n_2 \approx 3.2 \cdot 10^{-20} m^2/W$

(C) Raman and Brillouin scattering:

Raman: mainly forward, $B \approx 4THz$, $\Delta f \approx 13THz$, $P_t \approx 300mW$

Brillouin: backward, $B \approx 10MHz$, $\Delta f \approx 11GHz$, $P_t \approx 3mW$

(D) Polarization mode dispersion:

l, t, Δt

$\Delta t = D_p \cdot \sqrt{l}$ $D_p = 0.1 \ldots 2\ ps/\sqrt{km}$

Figure 4: *Propagation effects in optical fibers.*

The optical power launched into a singlemode fiber is limied by different nonlinear effects including Raman and Brillouin scattering and the Kerr effect. The treshold power for the Brillouin scattering may be very low, but fortunately the latter is a narrowband effect. Raman scattering and the Kerr effect both limit the maximum signal power in a singlemode fiber to a few hundred milliwatts.

In the case linear chromatic dispersion is perfectly compensated and the signal power is kept low enough, the optical-fiber link performance may be limited by polarization mode dispersion. Polarisation mode dispersion is caused by small differences in the propagation velocities of the two orthogonally polarized, degenerated modes in a rotationally-symmetrical singlemode fiber. Unfortunately, high-birefringence, polarisation maintaining fibers are not practical for long-distance links for many reasons.

3. Optical fiber capacity

The capacity of a communication link depends on the available bandwidth and signal-to-noise ratio. In optical fiber communications, both optical (quantum) noise and electronics (thermal) noise are present. The noise spectral density for both noise types is shown on figure 5. Quantum noise is part of the optical signal and is further increased by the amplified spontaneous emission of optical amplifiers. Thermal noise is the main limitation in all terminal equipment electronics.

Noise power: $P_N = B \cdot N_0$

Thermal noise density: $N_0 = k \cdot T$ (Rayleigh-Jeans)

$k = 1.38 \cdot 10^{-23}$ J/K (Boltzmann)

Quantum noise density: $N_0 = h \cdot f$

$h = 6.624 \cdot 10^{-34}$ Js (Planck)

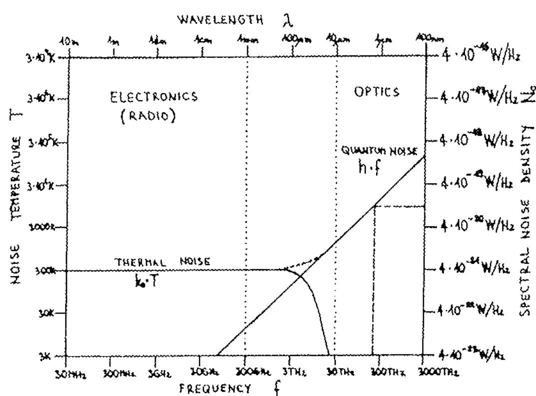


Figure 5: Electrical and optical noise.

In the case of a simple optical receiver as shown on figure 6, the predominant noise source is the thermal noise of the following electrical amplifier, in spite of the good quantum efficiency of a PIN photodiode. In such a simple receiver, electrical (thermal) noise is about 20dB stronger

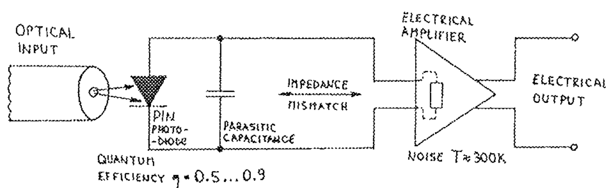


Figure 6: Noise in a simple optical receiver.

than optical (quantum) noise. In other words, while the quantum limit for a single logical "1" is 21 photons for a bit-error rate of 1.0E-9, a real receiver requires about 2000 photons for a logical "1" for the same bit-error rate. The main cause of the poor receiver performance is a large impedance mismatch between the photodiode and following electrical amplifier, further complicated by the always present parasitic capacitance.

The performance of optical-fiber links can be much improved by optical laser amplifiers. The best performance is currently acheived by erbium-doped fiber amplifiers as shown on figure 7. Erbium-doped fiber amplifiers may approach the quantum-noise limit to a few tenths of a dB. Like any laser amplifier, erbium-doped fiber amplifiers are bi-directional and require expensive optical isolators at both input and output.

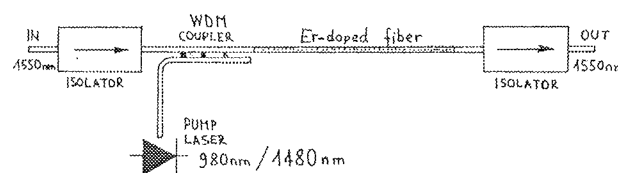


Figure 7: Erbium-doped fiber amplifier.

Before estimating the capacity of an optical-fiber link, the modulation coding loss should be estimated first. In the case of a simple optical link using intensity modulation and direct detection (IM-DD), the modulation coding loss is around -20.2dB as shown on figure 8. More efficient modulation schemes are very difficult to implement at optical carrier frequencies and the high data rates involved.

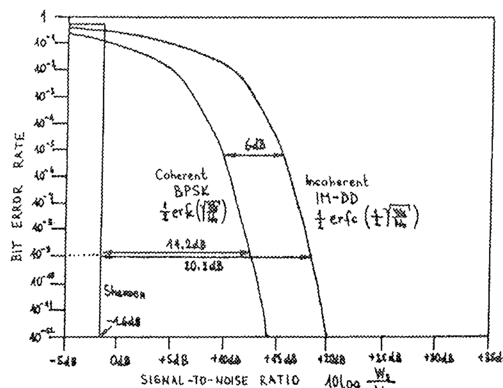
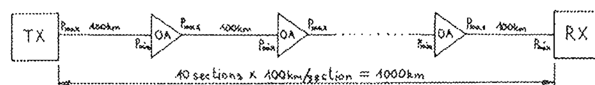


Figure 8: Simple modulation coding loss.

An estimation of the capacity of a high performance optical-fiber link covering 1000km is shown on figure 9. The link includes several erbium-doped amplifiers (usable bandwidth around 4THz) but there are no signal regenerators. The overall capacity of around 2.6Tbit/s is comparable to the bandwidth of the erbium-doped fiber amplifiers.



$B = 4$ THz (Er amp)

Coding loss = -20.2dB $= \alpha$

10 sections → $N_0 + 10$dB $= N_0'$

$P_{max} = 100$mW = $+20$dBm

$P_{min} = 0.3$mW = -5dBm

$$C = B \cdot \log_2\left(1 + \frac{\alpha \cdot P_{min}}{B \cdot N_0'}\right) = 2.6\,\text{Tbit/s}$$

Figure 9: Optical-fiber link capacity.

4. Terminal equipment design

Although still developing, the manufacturing of optical fibers is a relatively mature technology at least for silica fibers. There are only small improvements trying to tailor the linear chromatic dispersion, increase the core effective area to reduce the nonlinear effects and improve the fiber symmetry to reduce the polarisation mode dispersion.

There are many more open issues in the design of line terminal equipment for optical-fiber communications. First, line terminal equipment should consider all of the limitations of the optical-fiber transmisson path to fully utilize its capabilities. Second, due to the high data rates and wide bandwidths there are several technological constraints in designing the line terminal equipment itself.

Practically speaking, signal multiplexing from multiple sources is required both in the electrical domain as well as in the optical domain as shown on figure 10. Time-division multiplexing is used almost exclusively in the electrical domain with the rare exception of analog transmissions. Electrical time-division multiplexing is limited to about 40Gbit/s with the current semiconductor technology.

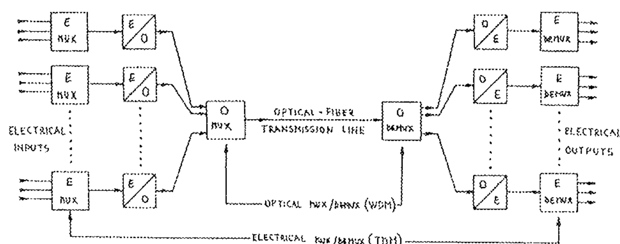


Figure 10: Electrical and optical multiplexing.

Although this figure may rise in the future, various propagation effects in the optical fiber, in particular linear chromatic dispersion and polarisation mode dispersion, also limit the maximum data rate for time-division multiplexing. In order to further increase the capacity of the optical transmission path, wavelength (frequency) division multiplexing has to be used in the optical domain.

The design of a high-capacity optical transmitter is shown on figure 11. The input electrical data is first processed in parallel form in a (silicon) VLSI ASIC, providing data formatting, framing and forward error correction if required. The data stream is then converted to serial form in a high-speed GaAs or InP circuit. Of course, the transmitter includes clock distribution and multiplication circuits.

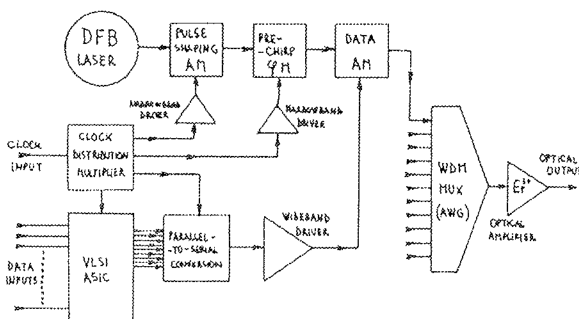


Figure 11: High-performance optical transmitter.

The optical signal source is usually a distributed feedback laser oscillating on a single longitudinal mode with a spectral linewidth of a few ten MHz. The laser feeds a chain of several different modulators. Although simple intensity (amplitude) modulation is used for transmitting data, the optical transmission path may require pulse shaping with an additional amplitude modulator as well as pulse prechirping with a phase modulator.

Many different technologies are used to build electro-optical modulators, but the most popular designs are based on lithium niobate ($LiNbO_3$) interferometric modulators and on electrooabsorption modulators built in semiconductor chips. Most modulator designs are polarisation dependent and require high-power and wide-bandwidth electrical drivers.

The outputs of several optical transmitters operating on different wavelengths can be combined together on a single optical fiber in a WDM multiplexer (a linear, passive combining network operating at optical frequencies). Finally, the optical signal power of all channels combined together is boosted with a single erbium-doped fiber amplifier.

Of course, a reverse signal processing has to be performed in a high-capacity optical receiver as shown on figure 12. The input optical signal level is first boosted with an optical amplifier before being fed to a WDM DEMUX (a bank of optical bandpass filters). Each signal wavelength is fed to a PIN photodiode, followed by a low-noise, wideband amplifier feeding the clock recovery and electrical demultiplexing circuits. High-capacity optical receivers may include an adaptive polarisation mode dispersion compensation.

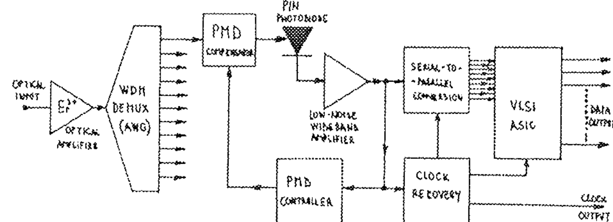
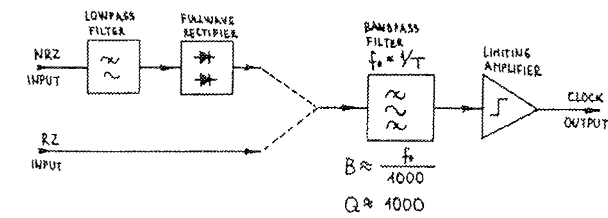


Figure 12: High-performance optical receiver.

One of the most critical functions of high-capacity receivers is the clock recovery, since it is responsible for jitter system. Electrical clock-recovery designs are shown on figure 13. In the case of a NRZ transmission, some signal processing (full-wave rectifier) is required to obtain a discrete spectral line at the clock frequency. Of course, little if any processing is required in the case of a RZ (soliton) transmission.



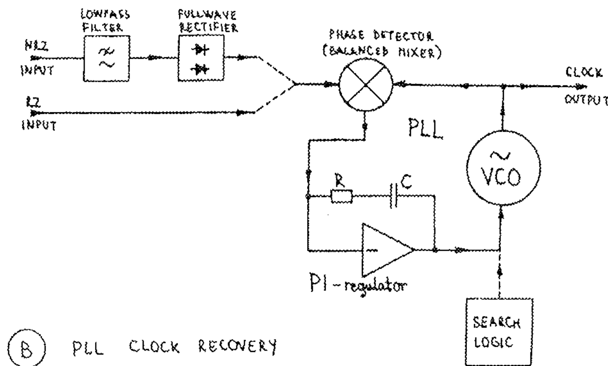


Figure 13: *Electrical clock-recovery designs.*

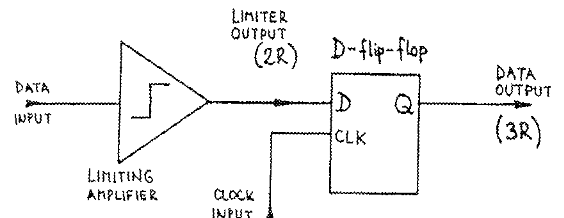
A bandpass filter is required to extract the clock line from the signal. A simple cavity filter as shown on figure 13A is not a very practical solution, since a high Q is required for the cavity. A PLL clock recovery as shown on figure 13B allows many more degrees of freedom including a second-order feedback network that keeps the static phase error independent of the clock-frequency offset. On the other hand, a PLL clock recovery usually requires a search logic to acquire an initial lock on the signal.

The performance of a digital communication system can be much improved using signal regeneration. At least one signal regenerator is required in the receiver, while additional signal regenerators may be inserted in the communication path. The regenerator design and operation is shown on figure 14. Full signal regeneration requires three steps: signal amplification, limiting (2R regeneration) and reclocking with a D-flip-flop (3R regeneration).

Currently most signal regenerators are built as electronic circuits, although there have been attempts to build optical 2R and 3R regenerators. An important drawback of optical WDM systems is that the signal regeneration has to be performed separately for each wavelength.

5. Conclusion

Since optical-fiber communications are an important and rapidly evolving tecnology, it makes sense to compare the evolution of optical communications with the evolution of radio communications almost one century ago. Radio started with spark-gap transmitters and rather primitive receivers. Optical-fiber communications started some 25 years ago with directly-modulated light-emitting diodes and lasers, whose optical signal spectrum was much broader than the information bandwidth just like in early radio systems.



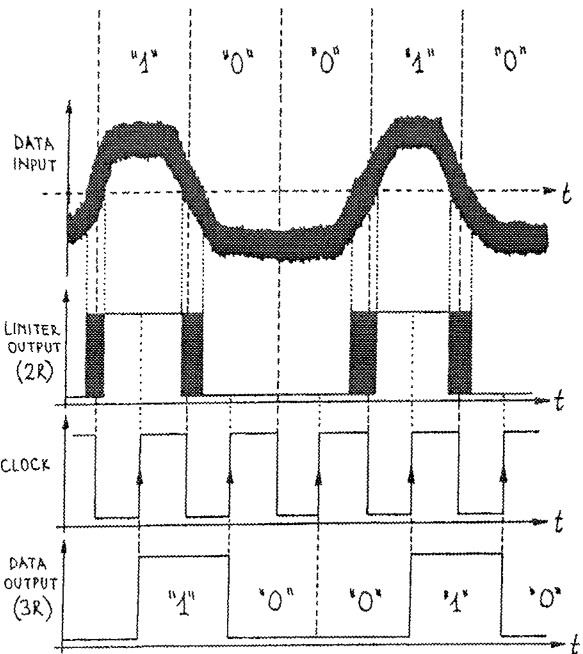


Figure 14: *Regenerator design and operation.*

An important breakthrough in radio communications was the vacuum-tube amplifier. The erbium-doped fiber amplifier brought a similar breakthrough to optical-fiber communications about one decade ago. Just like the vacuum-tube amplifier, the erbium-doped fiber amplifier finally allows at least some primitive signal processing in the optical domain. Unfortunately, the optical amplifier is still a complicated and expensive piece of equipment that can not be integrated easily, just like the vacuum-tube amplifier in the early days of radio communications.

The current needs of communication operators are to implement at least some low-level optical signal processing. In particular, since wavelength-division multiplexing is being used due to optical-fiber and terminal-equipment limitations, optical switching and routing is required in WDM systems as shown on figure 15. The most critical components, high-performance switching matrices, wavelength converters and optical 3R regenerators are still at a very early stage of developement.

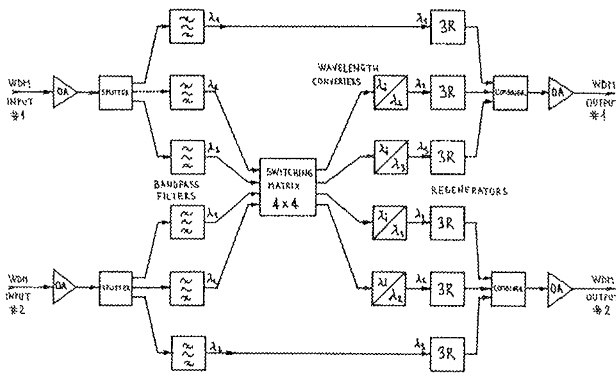


Figure 15: *Optical switching and routing*

At this point it is difficult to estimate the future developements of optical communication technology simply because the most important component, a simple unidirectional amplifier, like the transistor for radio frequencies, has not yet been invented for optical frequencies. All laser amplifiers are bidirectional amplifiers and require external isolators that can not be integrated easily. Finally, the linear dimensions of optical waveguides are two orders of magnitude larger than electrical interconnections inside modern integrated circuits.

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ORGANIC SEMICONDUCTORS AS CANDIDATES FOR ADVANCED OPTOELECTRONIC DEVICES

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Key words: OS, organic semiconductors, optoelectronic devices, ultrathin flexible multicolor displays, LED displays, Light-Emitting Diode displays, FET, Field Effect Transistors, OLED, Organic Light Emitting Diodes, Van der WAALS force, LONDON force, PTCDA, PeryleneTetraCarbox DiAnhydride

Abstract: Organic semiconductors are gaining an increasing attention due to their promise of novel optoelectronic devices. The main attraction of these materials stems from their potential integration with flexible materials, which would result in ultrathin flexible multicolor displays. Basic electronic properties of typical representatives of organic semiconductors are reviewed. The operation of a light-emitting device based on organic semiconductors is fundamentally different from its inorganic counterparts due to differences in electronic transport properties. The crucial component apart from the active material is represented by the metal-organic semiconductor contacts.

Organski polprevodniki - kandidati za napredne optoelektronske komponente

Ključne besede: OS polprevodniki organski, naprave optoelektronske, zasloni večbarvni fleksibilni ultratanki, LED zasloni z diodami svetlobo sevajočimi, FET transistorji z učinkom polja, OLED diode svetlobo sevajoče organske, Van der WAALS sila, LONDON sila, PTCDA perilentetrakarboksilni dianhidrid

Izvleček: Interes za organske polprevodnike se povečuje, saj gre za obetaven material, s pomočjo katerega bomo lahko izdelali nove optoelektronske elemente. Glavni čar teh materialov je njihova zmožnost integracije z upogljivimi materiali, kar bi omogočilo izvedbo izredno tankih upogljivih barvnih prikazovalnikov.

V prispevku predstavimo osnovne električne lastnosti tipičnih predstavnikov organskih polprevodnikov. Delovanje svetlečih elementov na osnovi organskih polprevodnikov se v osnovi razlikuje od delovanja njihovih neorganskih dvojnikov zaradi razlik v načinu transporta nabojev. Poleg materiala samega pa predstavlja kontakt kovina - organski polprevodnik naslednji pomemben faktor pri obnašanju komponente.

1. Introduction

Currently, two venues in material science of the organic semiconductors (OS) are being explored. The materials based on small molecules and polymers. The small-molecule materials are typically employed in thin-film-based devices and are synthesized by vacuum evaporation. These materials have relatively low molecular weight (~500 - 2000). Polymer films, on the other hand, are typically fabricated by dip-coating of the substrate, and have considerably higher molecular weight (~10 000 - 100 000). Since the excitation mechanisms are essentially the same for both classes of materials, the choice is a matter of preference of fabrication method. In what follows we will discuss only the small-molecule type of materials.

The most advanced OS-based devices to date are represented by field-effect-transistors (FETs) and organic light emitting diodes (OLEDs). In the early stage of development of OLEDs organic single crystals were employed. Relatively high dielectric constant of these materials forced the use of high voltages to achieve sufficiently high electric fields. High voltages coupled to poor reproducibility in material synthesis procedures and fabrication of metallic contacts caused extremely low reliability of the first devices. The use of the Langmuir-Blodgett technique yielded considerable improvement since it allowed the fabrication of OS layers with the thickness of well below of a micron.

The development in the OS thin-film fabrication techniques resulted in higher structural quality of the layers. The availability of novel materials resulted in better alignment of the electronic energy levels at the metal-OS interface. Consequently, in late eighties Tang *et al.* /1/ demonstrated OLEDs with efficiency and lifetime that promised the use in lighting and display applications. In by the end of nineties the OLEDs reached the commercialization stage. Further improvement in efficiency was achieved by the Princeton group through the use of fluorescent dye in the multilayer structure /2/.

2. Organic light-emitting devices

2.1 Basic material properties

OSs exhibit markedly different structural and electronic properties than their inorganic counterparts. The basic building blocks of OS are molecules instead of atoms. The

fundamental intramolecular interaction is Van der Waals or London force. Consequently organic molecular crystals reveal rather weak structure. The main advantage of such bonding is its relatively small modulus of elasticity, which allows the structure to adapt to a variety of different substrates. This is important when we consider the possibility of integrating optoelectronic devices with flexible structures such as plastics.

The main consequence of Van der Waals banding is small overlap between the electronic wave functions centered on atoms of neighboring molecules. This has profound implications on the transport of the electronic charge in OSs. The absence of extended delocalized states, results in the charge transport that is not coherent in energy bands but stochastic hopping from one localized state to another. Such transport is extremely sensitive to electrically active structural defect that typically act as traps for the carries, resulting in overall carrier mobilities in the range between 10^{-4} to 1 cm^2/Vs.

Many of the OSs currently under investigation are wide-gap materials with the energy separation between the highest unoccupied molecular orbital (HOMO) and the lowest occupied molecular orbital (LUMO) of 2-3 eV. This results in a very low concentration of thermally activated carriers. In addition to structural defects also impurities typically act as traps rather than sources of free carriers as in the case of inorganic semiconductors. Frequently oxygen and/or ambient water molecules affect the electronic transport in these materials.

There are several OSs that are employed in OLEDs,most frequently used is aluminum chelate complex (Alq) This is an electron conducting material where Al ion is surrounded by organic molecules-ligands where molecules are π-conjugated. Most studied OS material is 3,4,9,10-perylenetetracarboxyic dianhydride (PTCDA) whose

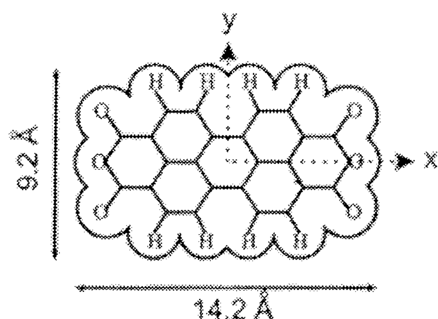

Figure 1: *Scematic representation of a single molecule of 3,4,9,10-perylenetetracarboxylic dianhydride.*

molecule is illustrated in Fig. 1. The core of the molecule represents perylene, at the sides are attached two dianhydride groups. The HOMO-LUMO energy separation is 2.2 eV and the maximum optical absorption occurs at ~ 550 nm. This is a hole-conducting material in which carriers are transported predominantly along the direction perpendicular to the molecular planes, where the overlap between p-orbitals of the perylene core and dianhydride groups is the greatest /3/.

PTCDA thin films are readily fabricated by vacuum evaporation. The molecules orient themselves parallel to the substrate surface and form monoclinic crystallites whose size depends strongly on the evaporation conditions. Under ultrahigh vacuum and low substrate temperature PTCDA grows almost epitaxially. High vacuum and elevated temperatures on the other hand yield grain size on the order of 50 nm.

2.1. Device physics

The electronic properties of OSs are characterized by molecular levels rather than by the extended bands of delocalized states. However, to illustrate the basic operating principles of and OLED we will use most of the concept derived from the inorganic physics, and keep in mind the peculiarities of OSs. In Fig. 2. we show schematically the basic steps involved in light generation from a single layer of OS by electrical excitation - electroluminiscence. The solid lines in the figure represent electronic energy levels although we stress again that typically no delocalized states are present in these materials. As we apply the bias on the structure consisting of a single OS layer sandwiched between two dissimilar metals several processes are underway. The carriers are injected from the electrode, transported along the organic material and captured. They recombine with the oppositely charged particles and consequently the light quantas are emitted

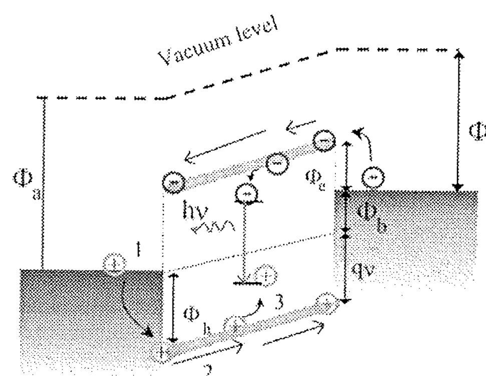

Figure 2: *Processes involved in light emission from an organic semiconductor sandwiched between two metallic layers. (1) charge carrier injection, (2) transport across the organic semiconductor, (3) exciton formation, (hν) radiative recombination. Indicated are Φ_a and Φ_b, workfunctions of the anode and cathode, respectively, Φ_h and Φ_e hole and electron injection barriers, respectively and $qv= qV-\Phi_b$,where Φ_b/q represents the built-in voltage as a consequence of dissimilar workfunctions of the two metals.*

The carrier injection proceeds via the metal/OS interface. If we neglect the interface dipole that my arise due to the charge distribution, and assume the alignment of the vacuum levels across the complete structure we could consider that the interface energy barriers for carrier transport are determined by the metal work functions. This approach is valid only as a first approximation. The metal/OS interface are frequently characterized by defects that stem from disordered growth and/or impure source materials. In addition relatively low-density structure of OS thin films facilitates diffusion of metal atoms yielding chemically intermixed interfaces. Consequently relatively large interface dipoles characterize metallic contacts on OSs, and present additional difficulties in quantitative description of electronic transport.

Injected carriers start their way across the sample under the applied electric field. The transport is markedly different than in the case of inorganic semiconductors. The principal characteristic of OS thin films is comparatively high degree of structural disorder which results in the loss of periodicity . Consequently, the electronic wave function become localized. The charge carrier transport is best described by hopping between these states that are arranged in a spatial array with a given energy distribution. Such transport mode is relatively slow and results in carrier mobilities that are several orders of magnitude lower than those in inorganic semiconductors. In addition, impurities within the OS may introduce energy levels that are lower than the levels in the manifold of hopping states. Such levels act as traps that can immobilize the carriers for longer periods of time.

When the injecting electrode forms Ohmic contact with OS layer and the applied bias is sufficiently high, the density of the injected carriers may exceed the density of the carriers that material can transport. The net charge resides within the OS forming a space-charge, which limits the current across the layer. The space-charge-limited (SCL) current is the maximum current that can flow across the OS layer at a given electric field, unless the opposite contact is capable of injecting the carriers of the opposite sign. The SCL current exhibits a power law dependence on the applied electric filed:

$$j \propto E^{l+1} / L^{l} \qquad (1)$$

where E is the electric field and L is the OS layer thickness. In the absence of deep traps l = 1, resulting in Child's law seen already in the vacuum tubes. In reality trapping is always present with a given energy distribution of trapping states. In this case the SCL current is best described with l>1, with typical values of 5.

In order to obtain light from the active OS layer the carriers of the opposite sign must recombine radiatively. Due to the low carrier mobility the the recombination of electron-hole pairs (excitons) is diffusion-limited and may exhibit radiative or non-radiative character. The probability and the multiplicity of radiative exciton decay is determined by its spin-symmetry. During electrical excitation approximately one singlet (total spin S=0) exciton is created for every three triplet (S=1) excitons /2/. Typically only relaxations of singlet excitons conserve spin and generate fluorescence. With disruption of symmetry triplets may slowly radiatively decay resulting in phosphorescence. Phosphorescence was considered inefficient mode of luminescence in OS. Recently the Princeton group demonstrated that the phosphorescence may be enhanced by doping the phosphorescent material with the fluorescent acceptor /2/. The result was an increase in quantum efficiency by a factor of three relative to the undoped material.

2.2. Metal-OS contacts

Metallic contacts on organic semiconductors (OS) are important due to their role in carrier injection in novel organic optoelectronic devices, and successful application of a given metal/OS contacts as a constituent of a device requires precise knowledge of its electrical properties. The alignment of the electronic energy levels across the metal/organic interface determine its transport properties. Electronic properties of the metal/OS interfaces have been examined on a case of prototypical OS 3,4,9,10-perylene-tatracaboxylic dianhydride (PTCDA) by Hirose *et al.* /4,5/ using synchrotron radiation photoemission (SRPES). Their findings show that the alignment of the electronic energy levels is strongly dependent on chemical and/or structural abruptness of the interface. Chemically abrupt interfaces are characterized by the interface energy barrier that is determined primarily by the position of Fermi level at the PTCDA surface. Chemically reacted interfaces, on the other hand, exhibit gap states that assist charge carrier transport across the interface and consequently yield ohmic contacts.

First ionization energy of the metal atom appears to be decisive parameter that determines whether a given metal/OS interface acts as a blocking contact or as an ohmic contact /4,5/. Indium is one of the metals with the lowest first ionization energy (5.79 eV) forming ohmic contact to PTCDA. The diffusion of In across the In/PTCDA interface has been thoroughly studied, albeit only for the case of In on highly ordered thin PTCDA layers /4, 8/. Upon arrival of In atoms onto PTCDA surface a formation of a coordination compound In_4PTCDA has been proposed /6,7/, and theoretical calculations of its molecular energy structure yielded the states in the gap of PTCDA acting as promoters of the charge carrier transport. Diffusion of In in PTCDA may be different in the case of reversed interface, i.e. PTCDA on In, which is interesting also from the applied standpoint. Also the stability of the interface relative to the increased temperature is of considerable interest for device processing.

We have employed transport measurements coupled to the SRPES experiments to examine the diffusion of In PTCDA at elevated temperatures. Our results show that

as the temperature of a Ag-PTCDA-In structure approaches the melting point of the In substrate the room-temperature rectifying current-voltage characteristics changes to ohmic. This process transformation is a result of strong In diffusion that is likely to be grain-boundary directed process.

2.2.1. Experimental

The samples for SRPES were synthesized in a vacuum chamber with the base pressure of 1×10^{-6} Torr. The source material was commercially available PTCDA that was purified by evaporating twice onto a collecting shutter that was placed above the Mo boat. We employed Si(001) substrates that were chemically cleaned using RCA etch, followed by dipping in 10% hydrofluoric acid to obtain atomically flat hydrogen-terminated Si(001) surface. Onto such surface we evaporated 1 μm-thick layer of In. During Indium evaporation the substrate was at room temperature (RT). Upon completion of In deposition 1 μm-thick PTCDA layers were grown using a growth rate of 1 nm/s. The layer thickness was monitored using an in-situ quartz thickness monitor. Upon completion of the OS growth we transferred the samples into the analysis chamber that was attached to the 6m-torroidal-grating monochromator beam line of the Synchrotron Radiation center storage ring in Stoughton, Wisconsin. Photoelectron spectroscopy was performed using a cylindrical-mirror analyzer and photon energy ranging from 20 to 130 eV, resulting in the overall resolution of the set-up (electrons+photons) better than 0.25 eV. The samples were mounted onto a sample holder that enabled heating and cooling of the sample in the range of temperatures between 80K and 673K.

The samples employed in transport measurements were identical to the samples investigated by SRPES with the exception of a 100 nm-thick Ag topmost contact, with the effective area of 4.9 mm^2. The current-voltage (I-V) characteristics measurements were performed using thin In tips attached to the contacts using precision manipulators. We used a Keithley 2400 SourceMeter as a voltage supply and as an ampere meter.

2.2.2 Results and discussion

Our electronic transport data on Ag/PTCDA/In heterostructures agree well with the findings by Hirose *et al* /4,5/.. Typical I-V characteristic for a structure comprising 1 μm-thick PTCDA layer grown on In-covered Si(001) and contacted with Ag layer is shown in Fig. 3. The forward current (filled circles) follows a linear dependence for voltages below 0.9V. Beyond that value a power-law dependence on the applied voltage was observed. The power increased from 3.2 to up to 5.9, indicating substantial effect of traps /9/ on the electronic transport. Relatively large reverse leakage current (open circles) may be due to image-charge lowering of the Ag-PTCDA interface energy barrier and/or tunneling through the barrier /10/. On the other hand, metals with low ionization potential such as In and Al form ohmic contacts on PTCDA. This is exemplified in Fig. 4(a) where we show an I-V characteristic of an In/PTCDA/In heter-

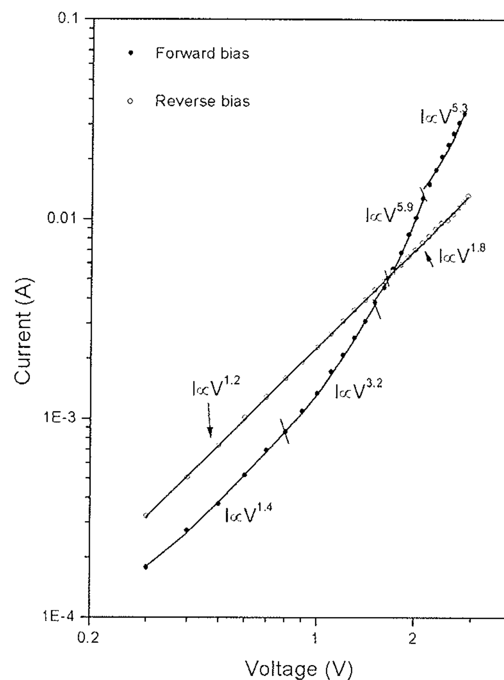

Figure 3: *Current voltage characteristic of a Schottky diode comprising 1 μm-thick PTCDA layer evaporated on In-covered Si(001) substrate and contacted to Ag layer. Open circles: reverse bias, filled circles: forward bias. The solid lines represent a least-squares fit to the function proportional to the power of applied voltage. The fitting parameters used in the fit were power exponent and the proportionality factor.*

ostructure that was synthesized by evaporation 1 mm-thick In layer onto PTCDA surface. We see a linear dependence that yields the resistance of a complete structure to be 9.4 Ω.

Ohmic character of the In/PTCDA interface is supposedly originating from the interface states that are a consequence of chemical reaction between In and carboxylic groups of PTCDA molecules. According to the recently published work by Ueno and coworkers[/8/, In atoms, presumably due to the low ionization potential, cede electrons to the PTCDA matrix and form In_4PTCDA coordination compound. Their calculations within the framework of hybrid Hartree-Fock/density functional theory indicate that In_4PTCDA complexes exhibit electronic energy states that lie above HOMO of PTCDA. Such states therefore, act favorably for the charge carriers crossing the In-PTCDA interface /4,5/. The linear I-V characteristic presented in Fig. 4(a) indicates that the chemical reaction leading to the formation of interface states takes place when free In atoms arrive onto the PTCDA surface, as well as when In atoms are bound in the metallic substrate. This results in the two interfaces characterized by a region where In diffusion determines their ohmic character.

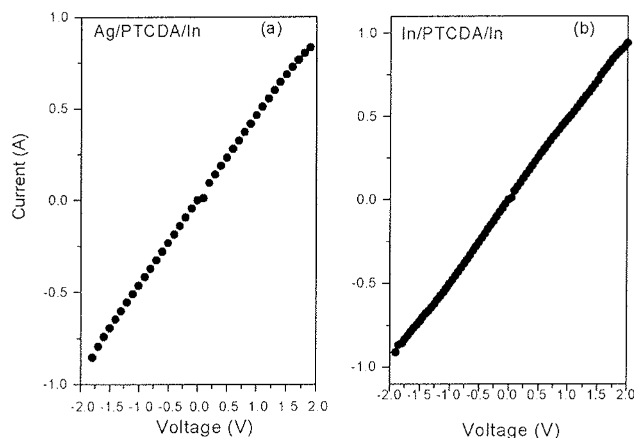

Figure 4: *(a)Current-voltage characteristic of a structure comprising 1 μm-thick PTCDA layer evaporated on In-covered Si(001) substrate and contacted to In layer. Both metallic layers form a conductive contact to PTCDA.*
(b)Current-voltage characteristic of a structure comprising 1 μm-thick PTCDA layer evaporated on In-covered Si(001) substrate and contacted to Ag layer, after heating to 120 °C.

Diffusion of In may assume drastic proportions if the sample is heated to 120 °C or above. The effect is illustrated by comparing Fig. 3 to Fig. 4(b), where we show the I-V characteristic of the sample used to obtain the data in Fig. 3, after heating to 120 °C. We see a dramatic change from rectifying to ohmic. Based on the I-V characteristic alone we can not rule-out the possibility that both In and Ag species diffuse into PTCDA, however our SRPES measurements indicate that In diffusion at elevated temperatures is extremely strong, resulting in In-related species diffusing through PTCDA layers as thick as 1 μm.

We demonstrate this by Fig. 5, which shows the photoelectron energy distribution curves (EDCs) measured on 1 μm-thick PTCDA layer grown on In-covered Si(001) substrate. Individual curves correspond to the sample at RT (bottom-most curve) and 150 °C (topmost curve).

The curves were obtained using photon energy of 80 eV. The binding energy scale is referenced to the position of the Fermi level that was determined from the photoemission cut-off of an in situ sputter-cleaned copper foil. We observed features in increasing binding energy that are pertinent to different energy levels of a PTCDA molecule /6-12/.

As the temperature of the sample increased to 150 °C we observed a strong emission of In 4d core level (topmost EDC). Room-temperature In diffusion can be ruled out based on the results illustrated in the inset, showing an EDC obtained with photon energy of 130 eV on 1 μm-thick PTCDA layer grown on clean Si(001) substrate. The feature at the binding energy of about 20 eV is present also in

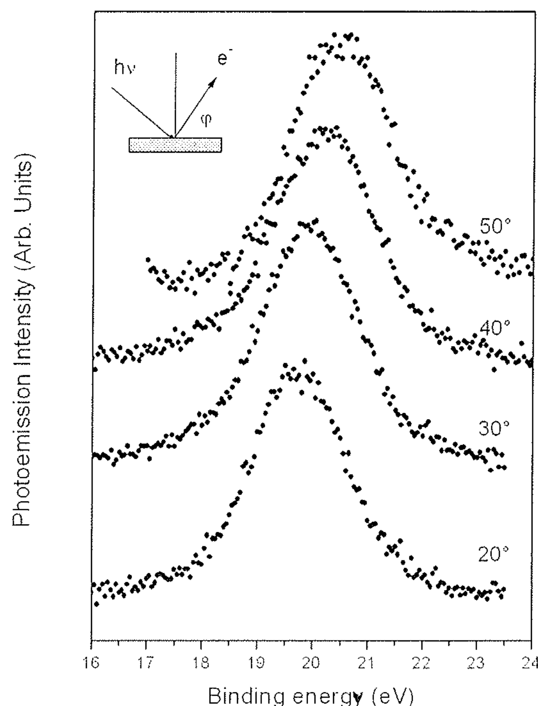

Figure 6: *Photoelectron energy distribution curves of a PTCDA/In/Si(001) structure indicating In diffusion as a consequence of sample heating. The photon energy employed was 80 eV. The curves represent emission from the sample at room temperature, and 150 °C, bottom to top, respectively. The narrow feature observed in the topmost curve corresponds to the emission from the In 4d core level. Inset: the photoelectron energy distribution curve from a PTCDA/Si(001) sample. The feature at 19.8 eV seen in this curve is originating from PTCDA and not from In*

this EDC and must therefore reflect the emission from the PTCDA-related energy states. From Fig. 5 we see that although the In-PTCDA chemical reaction takes place even if In atoms are bound in metallic In polycrystal, the room-temperature intermixing does not reach the surface of the 1 μm-thick PTCDA layer. When the sample temperature reaches or exceed the melting temperature of In however, substantial In-related photoemission is observed. From the position and lineshape analysis of the In 4d emission we can obtain the information on the chemical nature and consequently diffusion mechanism of In in PTCDA.

The emission from the In 4d core level presented in the topmost curve of Fig. 5 is relatively broad, which indicates a wealth of different chemical environment that In atoms may encounter upon diffusing towards the PTCDA surface. To check if the chemical environment of In atoms changes with the distance from the surface we have performed angular-dependent measurements, where we varied the emission angle (φ) from grazing towards normal. The incident angle of the photons also varied as ($\pi/2 - \varphi$). The results

are exemplified in Fig. 6, where we show the background-subtracted measurements as a function of emission angle (increasing bottom to top). The featureless lineshapes precludes reliable numerical analysis, although we have attempted to extract individual contributions to the observed emission. Note that the apparent binding energy of the feature presented in Fig. 6 deviates considerably form the published data for In 4d core emission in metallic In as well as for In 4d in compund semiconductors. For example, the positions of the In $4d_{5/2}$ and In $4d_{3/2}$ doublet components are reportedly 16.35eV, and 17.25 eV, respectively /16/ determined by SRPES on the polycrystalline film evaporated *in situ*. For the InSb these values are chemically shifted to 17.0 eV, and 17.8 eV, respectively /16/. Bermudez and Ritz /17/ observed by SRPES a 0.7 eV shift of the In 4d core-level emission centroid upon oxidation of the InSb(110) surface, and Sen *et al* report on the XPS-derived 1.1 eV chemical shift in In 4d centroid in In_2O_3 relative to the In 4d in polycrystalline film /18/. We attribute this variance to the final-state effects. Screening of the In core-hole is considerably less efficient for In atoms embedded in PTCDA matrix relative to that in In metal on In-compound semiconductors /4,5/. The centroid of the peak monotonically moves from 19.76 ±0.05 eV to 20.59±0.05 eV, for 20° and 50°, respectively. Coupled to this shift we observe an increase in FWHM of the peak from 1.9 eV to 2.18 eV for 20° and 50°, respectively. We interpret this behavior in a qualitative fashion in terms of multiple chemical environment of In atoms that vary with depth from the surface. The estimated photoelectron escape depth at these kinetic energies is ~4 Å /14/. Assuming that the photoemission signal is coming from roughly three times the escape depth, and taking into account that the molecules stack parallel to the substrate surface with the intermolecular separation of 3.21 Å /15/, we see that by changing the emission angle from 20 ° to 50 ° we have probed the region from the topmost molecular layer to the third molecular layer below the surface, respectively. At grazing emission the spectrometer detects photoelectrons only from the topmost molecular layer. The smallest FWHM of the peak indicates the presence of fewer In-related species; perhaps indium oxide and metallic In. As the emission angle increases towards normal the contribution of high-binding-energy component strongly increases, causing a high-binding-energy shift of the peak centroid coupled to the increase in FWHM. Large high-binding-energy shift (0.83 eV) suggests that the abundance of low-binding-energy component residing on the surface is relatively small. We can only speculate on the possible chemical environment of In atoms that contribute to the observed emission.

Apart of the metallic In and two common In oxides, InO and In_2O_3, In_4PTCDA comes to mind as possible candidate to explain the observed depth dependence of the In 4d core emission. We have evidence, however that the latter compound is not present at the PTCDA surface, when In atoms are subjected to diffusion through the layer of PTCDA. The signature for In_4PTCDA are the energy states above HOMO in PTCDA /6,7/. In Fig. 7 we show the EDCs obtained on the same sample as those in Fig. 5; this time with the photon energy of 50 eV. Focusing on the region near HOMO we see no emission Fermi energy and HOMO at the sample temperature of 150 °C, when we observed a strong In 4d core emission. Based of this evidence we can rule out the interaction of In with PTCDA in the form pro-

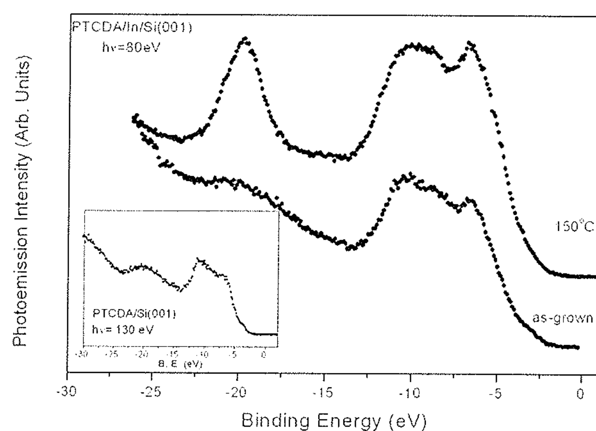

Figure 5: *In 4d core level photoelectron energy distribution curves obtained at different emission angles indicated at the left side of each curve. The binding energy scale is referenced to the spectrometer Fermi level. Inset: The emission angle in the figure is defined as the angle between the longer axis of the analyzer and the projection of this line on the sample surface.*

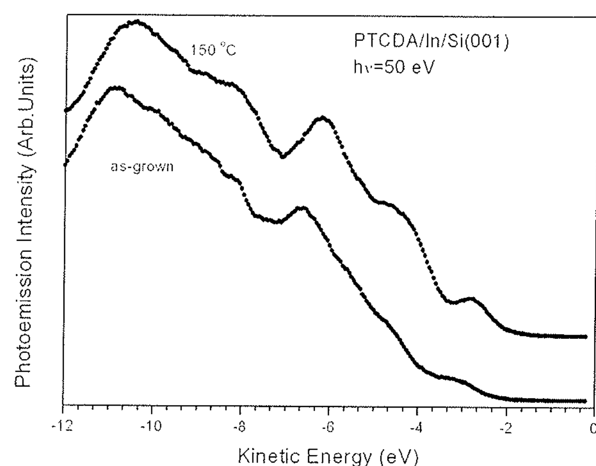

Figure 7: *Energy distribution curve taken at increasing temperatures of the 1 μm-thick PTCDA layer grown on In-covered Si(001). The energy scale is referenced to the spectrometer Fermi level. The bottommost curve was obtained on the as grown sample, to the bottommost curve in Fig. 5.. The topmost curve was obtained after heating of the sample to 150°C, and corresponds to the topmost curve in Fig. 5. The photon energy employed was 50 eV.*

posed by Ueno and co-workers /6,7/, when In is coming from In substrate.

The mechanisms connected to In diffusion are therefore different when PTCDA is evaporated onto In substrate than the mechanisms connected to In diffusion in the case of In evaporation onto ordered PTCDA surface. The tentative explanation assumes the formation of In_4PTCDA as the PTCDA molecules arrive onto In surface. The formation of the coordination compound is limited to the initial layer of thickness of few hundred Å /4,5/, and is determined by the room-temperature diffusion rate of In in PTCDA. Upon formation of sufficiently thick interface layer, the growth continues in the form of PTCDA. When the sample is heated the diffusion of In from the substrate is enhanced. The structure of the PTCDA overlayer is crucial for the diffusion.

Indium layer evaporated on Si(001) acts as structurally considerably different template for the PTCDA growth than the substrates employed in previous reports where atomically clean semiconductor /5-12/ or MoS_2 substrates were used /6,7/. Indium in thin film form is prone to three-dimensional island formation. Spicer and co-workers /19/ examined the growth of In on GaAs(110) substrates. Their SRPES results indicate that In forms atomic clusters for nominal coverage up to 8 monolayers, resulting in a discontinuous coverage. Ryu *et al.* /20/ examined In overlayers on hydrogen-terminated Si(001) substrates at different coverage by scanning tunneling microscopy (STM). After the thickness of In exceeds several monolayers (ML) the two-dimensional islands start to evolve into three-dimensional columns. Since the thickness of our In layers was 1 µm, we may safely assume that the surface exhibited increased roughness relative to the atomically flat hydrogen-passivated Si(001). In addition to the polycrystalline substrate, the PTCDA layer thickness and room-temperature of the substrate suggest that our PTCDA layer is polycrystalline /21/. High concentration of grain boundaries enhances a grain-boundary diffusion. Grain boundaries are also likely to contain embedded oxygen molecules, whereas the outermost layer of the film is oxygen-free due to oxygen desorption at elevated temperatures. Given the affinity of In to form oxides at temperatures that approach its melting point it is likely that the majority of In atoms remain immobilized as In_2O_3 and/or InO, and only few In atoms manage to reach the surface in atomic form, where they contribute to the low-binding-energy photoelectron emission presented in the bottommost curve of Fig. 6. The high-energy component of the EDCs shown in Fig. 6 might therefore represent the emission from In atoms in In_2O_3. Relatively fast decrease in intensity with the emission angle indicates low probability for In atoms to diffuse to the surface without forming an oxide.

3. Conclusion

In-PTCDA interface retains its ohmic character regardless the order of the layers, i.e. In on PTCDA or PTCDA on In. Diffusion of In in PTCDA at elevated temperatures, depends on the order of the layers and is likely to proceed via a grain-boundary network when polycrystalline PTCDA is grown on In substrates. Angular resolved photoemission reveals differences in chemical environment of In atoms that reside on the surface of thick PTCDA layers relative to the chemical environment of In atoms that reside in the molecular planes below the surface. Based on the binding energy of the In 4d core-level emission obtained at grazing-angle emission relative to the binding energy at high emission angle we suggest that small concentration of metallic In occupies sites on the PTCDA surface.

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SYSTEM DESIGN CONSIDERATIONS FOR LOW-POWER, BP Δ–Σ A/D CONVERTER USED FOR COHERENT DETECTION SYSTEMS

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Key words: BP Delta-Sigma A-D converters, BandPass Delta-Sigma A-D converters, coherent detection, power optimization, decimators, decimation filters, BW, Bandwidth, adders, running sum architecture

Abstract: Design considerations for low-power coherent detection system using BP Δ–Σ A/D converter are presented. Some optimization steps for reducing power consumption are explained together with some system and circuit level simulation results. A 6th order modulator design and corresponding 4th order running-sum decimator are presented. Suggestions are made for further reduction of power consumption, which is estimated to be less than 500μW for 6th order modulator with S-C loop filter implementation, oversampling ratio D=256, S/N=110dB at f_{ovs}=64kHz and bandwidth BW=260Hz.

Zasnova sistema za koherentno detekcijo z uporabo BP Δ–Σ A/D pretvornika z nizko porabo moči

Ključne besede: BP Delta-Sigma A-D pretvorniki pasovno propustni analogno-digitalni, detekcija koherentna, optimizacija moči, decimatorji, filtri decimacijski, BW širina pasovna, seštevalniki, arhitektura s seštevalniki

Izvleček: V članku je opisan postopek načrtovanja sistema za koherentno detekcijo z uporabo BP Δ–Σ A/D pretvornika na sistemskem nivoju. Predstavljeni so nekateri optimizacijski postopki na visokem hierarhičnem nivoju s pomočjo katerih lahko zmanjšamo porabo moči takega sistema ter rezultati nekaterih simulacij. Zasnovi BP Δ–Σ modulatorja šestega reda in pripadajočega decimatorja četrtega reda sta izbrani glede na postavljene zahteve in ostale pripadajoče kriterije. Podani so predlogi za zmanjšanje porabljene moči. Ocenjena poraba moči je približno 500μW za eno bitni modulator s filtrom šestega reda implementiranim s tehniko S-C, razmerjem vzorčevalne frekvence proti mejni D=256, razmerjem S/N=110dB pri vzorčevalni frekvenci f_{ovs}=64kHz in pasovno širino BW=260Hz.

1. Introduction

With down-scaling of integrated circuit technology in recent years analog signal processing circuits are more and more replaced by digital signal processing circuits because of several advantages: flexibility, programmability reliability, noise immunity, reduced power consumption, easier and more reliable design and test if automated procedures are used. The key operations in such systems are A/D conversion and for narrow band signals appropriate subsampling of correctly band-limited spectrum. In our case, simple coherent detection circuit and BP Δ–Σ modulator followed by simple and efficient digital decimation filters are used to transfer input double side band signal with suppressed carrier and limited bandwidth to a digital stream of data, which can be further processed by appropriate DSP algorithm. The technique has several advantages compared to traditional analog implementation: lower power consumption, easier integration and because of that higher reliability, better flexibility etc. It is essential to reduce power consumption as much as possible. The only way to do that is to perform optimization on each hierarchical level from the system to the layout.

We are trying to design a coherent detection system with as small power consumption as possible. The signal that must be down-sampled is double side band signal with suppressed carrier and with the bandwidth BW≤260Hz centered at 16kHz. The purpose of the system is to perform coherent detection of a low-frequency signal that causes modulation of the carrier, bring it down to the base-band and convert it to the digital domain using high resolution A/D converter with S/N>110dB. As usual this can be done in many different ways and it seems that most promising approach regarding silicon area and power consumption is BP Δ–Σ A/D converter and coherent detection.

In section II principles of coherent detection using BP Δ–Σ A/D converter are shortly explained and some system level simulation results are presented. Design steps for 6th order BP Δ–Σ modulator are shortly presented in section III with some key parameters regarding architecture, stability, speed, power consumption. Section IV deals with possible realisation of the decimator. Section V summarises simulation results and presents the conclusions.

2. System for coherent detection

Block diagram of possible system for coherent detection of narrow-band signals is presented on figure 1.

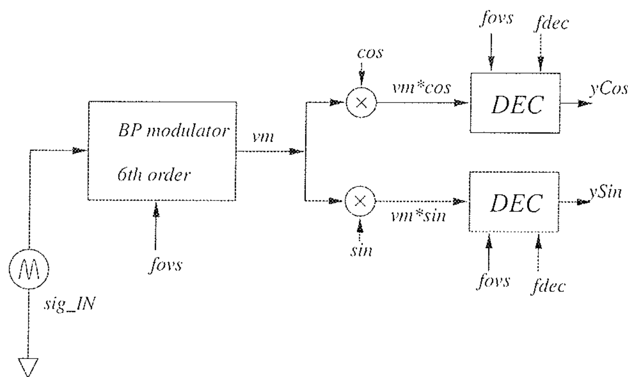

Fig. 1: Coherent detection system

BP modulator can be implemented with continuous time or S-C loop filter. Using S-C realisation makes A/D conversion more accurate and less sensitive to the process parameters and temperature variations compared to continuous time implementation, but requires additional filtering (anti-aliasing filter) to prevent folding of unwanted components to the base-band of the BP modulator. The continuous time gm-c loop filter reduces power consumption even further because it does not require anti-aliasing filter since all out-of-band components are attenuated efficiently by its loop filter. In addition the speed of the transconductance element needs to be smaller compared to the operational amplifier used in S-C implementation. Unfortunately CT approach it is less stable and less accurate. In this article S-C implementation is proposed for the reasons of accuracy. Sampling frequency of the BP modulator is selected as low as possible: $f_{ovs}=4f_{osc}$, thus a very simple method of coherent detection is available: multiplication of a bit-stream with coherent sine wave. It can be easily accomplished before the decimation filtering using frequency $f_{Cos}=f_{ovs}/4$ realised as another bit-stream with values taken from table 1 /4/. Coherent detection with defined relation among signal frequencies is reduced to the generation of simple streams of +1, 0 and -1 and 1 bit multiplication between bit-stream and Sin or Cos signal. Multiplying v_m by Cos or Sin signals is followed by filtering and down sampling. Some additional digital signal processing not described in this article gives further information about frequency and phase of demodulated signal: $x=v_mCos$ and $y=v_mSin$.

***Table 1:** Sin and Cos signal generation*

K	Cos	Sin
0	1	0
1	0	1
2	-1	0
3	0	-1
4	1	0

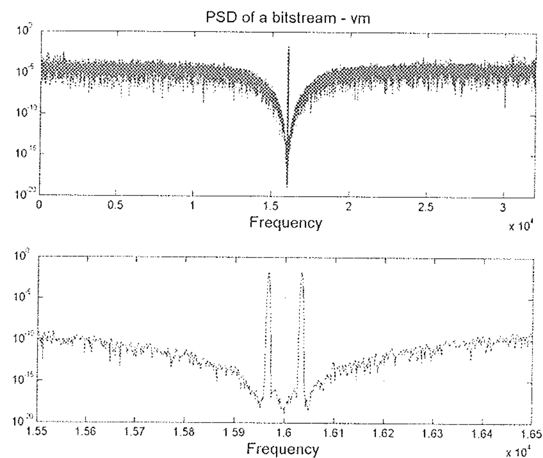

Fig. 2: Spectrum of a bit-stream v_m

The spectrum of a bit-stream v_m after BP Δ-Σ A/D converter is very rich and shown on figure 2 for the case of 2 spectral components of equal power with frequencies $f_{ovs}/4-f_x$ and $f_{ovs}/4+f_x$ (see detail on figure 2). Frequency f_x is a frequency of modulation signal that carries the information. The whole spectrum is composed of 2 spectral components in the band of interest, quantisation noise, thermal and 1/f noise and aliased crosstalk, which is much smaller than any other component if designed properly. Ideally the Cos or Sin signals are sine waves with only one spectral component with frequency f_x. Let us discuss the process of multiplication with our coherent signals. One can imagine that every spectral component in the v_m is multiplied by a sine wave with frequency $f_s/4$, which is in fact a stream of +1, 0 and -1. The band below $f_s/4$ is by multiplication reversed and placed to the same band and also translated to the band between $f_s/4$ and $f_s/2$. The band above $f_s/4$ is transferred between 0 and $f_s/4$ and $f_s/2$ and $3f_s/4$ and aliased back to the band $f_s/2$ to $f_s/4$. The spectrum after multiplication is shown on figure 3. 1/f noise and offset components are transferred around frequency f_s and are later attenuated by decimation filter. The noise power after multiplication with a coherent sine-wave is composed of all noise sources from the band below and above f_{osc} and are included in the simulation results presented on figure 3 /1/. The upper portion of the spectrum can not be seen because of the logarithmic scale. Similar spectrum exists for v_mSin. Frequency components above 125Hz must be attenuated using appropriate decimation filter.

Possible realisation of the decimation filter is $sinc^4$ characteristics with accumulate and dump architecture. Transfer function is presented on figure 5. A 4th order is used because in that case the slope of the decimation filter is bigger than the slope of quantisation noise produced by 6th order BP modulator. Short description of the implementation of the decimation filter is given in section IV. The spectrum y_{Cos} after $sinc^4$ decimator, down-sampled to $f_{dec}=f_{ovs}/R=250Hz$, with modulation frequency f_x=33Hz is presented on figure 4. Similar spectrum with different phase is obtained on the output y_{Sin}. Further digital signal processing of both signals can extract all necessary infor-

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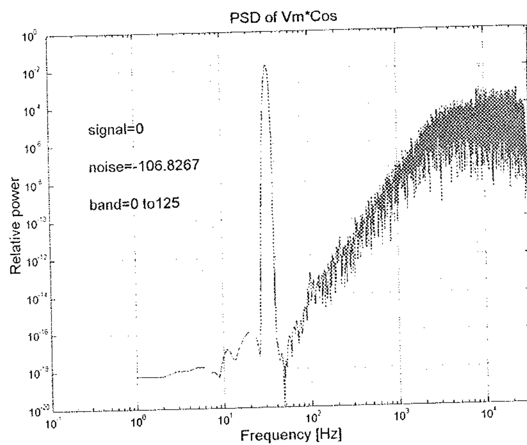

Fig. 3: Spectrum of v_mCos *for* f_x *=33Hz*

mation about frequency and phase of the rotation. Since all signals are very low frequency, serial digital signal processing can be used to save silicon area.

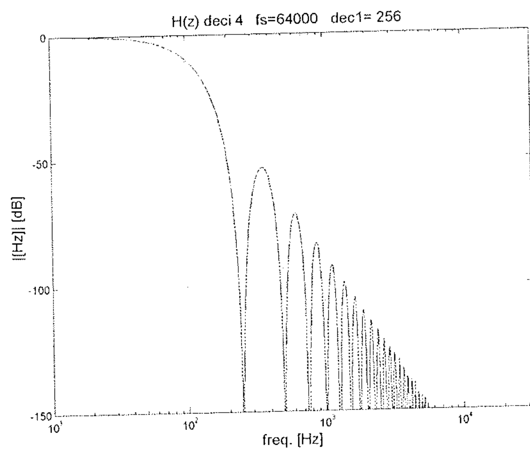

Fig. 4: Decimator frequency characteristics

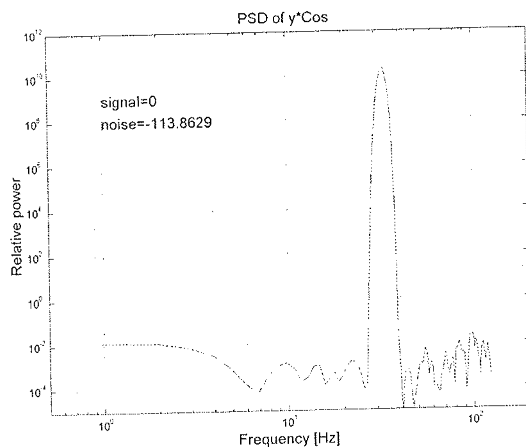

Fig. 5: Down-sampled spectrum of the rotation signal after decimator

3. 6th order modulator

A 6th order 1 bit BP modulator with oversampling ratio *R*=256 can fulfil the requirements: $S/N \geq 110$dB in a band of 125Hz. Figure 6 plots possible noise transfer function with poles and zeroes defined in table 2 and on figure 7. Signal transfer function (STF) depends on realisation, stability constraints, area and power consumption and will be presented in near future with special emphasise on power consumption optimisation and stability constraints. For S-C implementation the jitter does not present a problem, so normal comparator is used for one-bit A/D, while 1 bit D/A is implemented by non-return-to-zero S-C stage charged to the reference voltage and controlled by the outcome of the A/D conversion process or in other words by the bit-stream. The positions of poles and zeros are for the time being selected according to the Lee's rule of thumb /5/, which requires that the $|NTF(e^{j\omega})|<2$ for the whole band of interest. Since this condition is pessimistic and does not give insight into the real stability of the modulator it will be refined in the design and simulation steps that still needs to be implemented.

Table 2: *Poles/Zeros of possible Noise Transfer Function*

Poles	Zeros
-0.2151\pm j0.8333	-0.0048\pm j1.0000
+0.0000\pm j0.7499	+0.0000\pm j1.0000
+0.2151\pm j0.8333	+0.0048\pm j1.0000

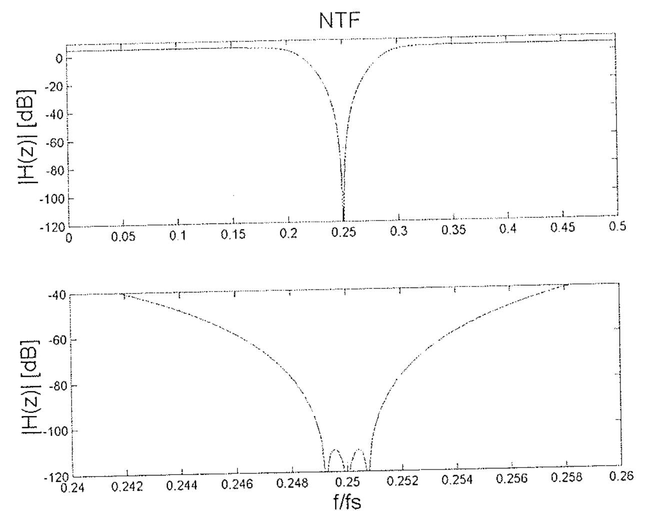

Fig. 6: Noise transfer function (NTF)

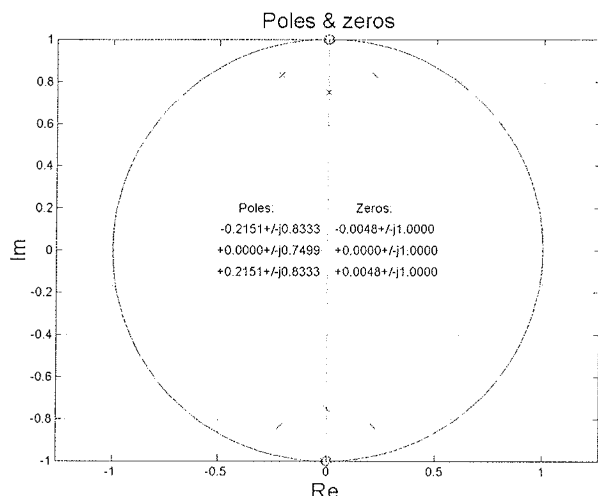

Fig. 7: Poles and zeros of noise transfer function (NTF)

4. Decimator

There are many possible realisations of the decimation filters. Efficient solution in terms of area and complexity is *sinc* decimator /3/, which does not need any multiplication and the only arithmetic operation needed is 2's complement addition. Here *sinc*^{4} (figure 8) is implemented because we have 6th order BP modulator with transfer function presented on figure 4. The slope of the frequency characteristics of the integrators before down sampling is bigger than the slope of the quantisation noise and thus guaranties enough attenuation of high frequency quantisation noise as well as other noise contributions. Very simple programmable accumulate-and-dump architecture has been implemented, so the oversampling ratio can be easily changed by simply taking every Rth sample from the IIR part and processed it by FIR low-frequency section of the decimator. Number of bits needed for correct operation is:

$$n_{bits} = \frac{\log_{10}\left(R^M r_i\right)}{\log_{10}(2)} = 32 bits$$

Where R is decimation ratio, M is decimator order, $r_i = 1$ is number of bits at the input and n_{bits} is number of bits needed for internal registers of the decimator, so that the overflow is correctly processed. IIR and FIR parts can be processed serially since the sampling frequency is rather low. Programming of the decimator is possible by changing the oversampling ratio from *R=2 to 256* and taking different bits from the last register of IIR to the first register of FIR every Rth oversampling clock cycles. Figure 5 is the result of processing the signal $v_m Cmos$ with real *sinc*^{4} decimator. If attenuation at 125Hz is not acceptable this can easily be corrected by simple digital all-pass filter following the decimator. The decimator realised in 0.6μm CMOS technology with f_{ovs}=64kHz consume approximately 20μA average current and the rest (80μA) are reserved for the modulator.

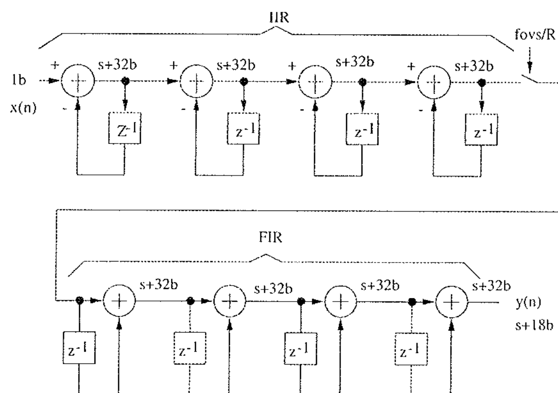

Fig. 8: Block diagram of sinc^4 *decimator*

5. Conclusions

A system design considerations and some important steps for the power consumption optimisation of a coherent detection system using 6th order BP modulator and 4th order *sinc*^{4} that can be used for mixed-signal processing of a narrow band double-side band signals with suppressed carrier are presented in the article. Possible architecture is evaluated and some system and circuit level simulations were performed to show the usefulness of the approach. Architecture of the BP modulator and decimator has been defined and important system level simulation results have been presented. The realisation of proposed architecture is feasible, so circuit design of a BP modulator will follow using S-C and gm-c implementation of the loop filter with big attention to the power consumption optimisation and stability constraints.

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SWITCHING NOISE IN DISTRIBUTED CLOCK SYSTEMS

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Key words: electronics, integrated systems, A-D integrated systems, analogue-digital integrated systems, mixed design, substrate noise, switching circuits, switching noise, distributed clock signal, noise optimization, design results

Abstract: Substrate noise is a serious limiting factor in the design of analogue-digital systems. Distributed clock systems can be used as an efficient method to solve the crosstalk and simultaneous switching noise associated with the data processing and clock distribution. In this paper we concentrate on the switching noise model for clock pipelines in order to find some interesting parameters for the circuit design. Expressions for clock transition time, switching current ripple and optimal clock symmetry are given. The comparison of an optimized clock pipeline, consisting of N stages with the central clock buffer shows that substrate noise due to the power bus voltage drops can be reduced approximately by $1.2 \cdot N$. Similarly, the reduction factor for substrate noise due to carrier injection from clock nodes can be as high as » $0.75 \cdot N$.

Preklopni šum v sistemih s porazdeljenim signalom ure

Ključne besede: elektronika, sistemi integrirani, A-D sistemi analogno digitalni integrirani, snovanje mešano, šum substrata, vezja preklopna, šum preklopni, signal ure porazdeljeni, optimizacija šuma, rezultati snovanja

Izvleček: Šum substrata je eden od pomembnih faktorjev ki omejujejo integracijo analogno-digitalnih sistemov. S porazdelitvijo signala ure lahko pomembno zmanjšamo presluhe in preklopni šum, ki je povezan z signalom ure in z obdelavo podatkov. V delu raziskujemo model preklopnega šuma v razvodu ure in poiščemo nekatere najbolj pomembne parametre za načrtovanje. Izvedeni so izrazi za čas prehoda signala ure, za stresanje toka napajanja in za optimalno simetriranje signala ure. Primerjava optimalno porazdeljenega signala s klasičnim pokaže, da v sistemu z N stopnjami lahko dosežemo zmanjšanje šuma v substratu za faktor »1.2·N zaradi zmanjšanih konic v napajalnem toku in za faktor » 0.75·N zaradi manjšega vpliva signala ure na substrat.

1. Introduction

In distributed clock systems the central clock is replaced by a large number of time-distributed signals, generated by a clock pipeline. In the simplest form the pipeline can be built as the chain of invertors integrated with the flip flops and logic gates /1/. If the system layout is done in such a way that pipeline stages are put close together with their loads, noise performance of the circuit as a whole can be improved significantly.

2. Switching properties of the distributed clock driver

The CMOS load is a combination of parasitic capacitances to V_{dd}, represented as C_p and parasitic capacitances to V_{ss}, represented by C_n. To analyze the circuit speed, all capacitances can be treated as one single load $C_l = C_p + C_n$ connected to V_{ss}. However, for the switching noise analyze the mode how the capacitances are connected with regard to power supply and the driving stage becomes important and the two capacitances must be treated separately. As presented on Fig.1, the power bus currents are different from the currents in the driving stage; they are smaller and different at the rising or falling edge of the signal.

Dynamic characteristic of the CMOS inverter becomes very complex if the slope of the input signal is comparable to the output signal slope. However, the influence of input signal waveform on the output is limited because of nonlinearities in the vicinity of the threshold voltage. If we apply a ramp function to the input of the chain of equally loaded inverters, such as presented on Fig.2, the responses converge rapidly to a 'characteristic' waveform /2/ that is independent from the initial signal slope. The most important measure for clock driver noise analyze are the slew rates of the rising and falling edges in the characteristic waveform, measured at their maximum value. These values are very close to slew rates measured at $V_{dd}/2$:

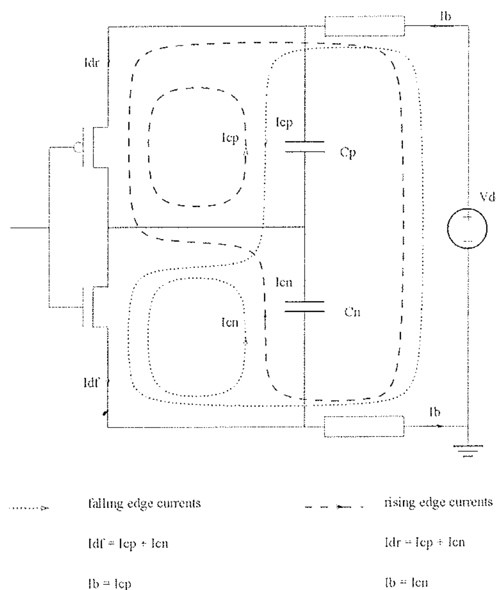

Figure 1: *Load currents in the CMOS buffer with local loads; power bus currents are different from the driving transistor currents*

$$s_r = \max\left(\frac{dv(t)}{dt}\right) \approx \frac{dv(t)}{dt}\Big|_{v(t)=vdd/2} \quad (1)$$

$$s_f = \max\left(\frac{-dv(t)}{dt}\right) \approx \frac{dv(t)}{dt}\Big|_{v(t)=vdd/2} \quad (2)$$

In general, s_r and s_f are not equal so that it is appropriate to define the *slew rate symmetry ss*

$$ss = \frac{s_r}{s_f} \quad (3)$$

Clock drivers are usually based on *equal slope* design ($ss \approx 1$) to achieve best noise immunity and waveform symmetry. For this type of characteristic, the threshold voltages and gain factors (K_p, K_n) for PMOS and NMOS transistors must be equal /3/.

Table 1: *Peak currents in the power bus and in the driving transistors*

I(peak)	Power bus	Driving transistor
Rising edge	$sr \cdot C_n$	$sr \cdot (C_n+C_p)$
Falling edge	$sf \cdot C_p$	$sf \cdot (C_n+C_p)$

Table 1 shows the difference between peak currents in the power bus and driving transistors in a single CMOS clock buffer. To achieve the symmetric characteristic, the P-transistor must be larger than the N transistor so that $C_p \approx 3C_n$. Under these conditions the difference between rising and falling edge bus current spikes becomes considerable. For purposes of noise analyze we will use

$$C_p = p \cdot C_n \quad (4)$$

The simplified presentation of switching currents in stage *i* and the neighboring stages is shown on Figure 3. The interaction of delay times and signal slopes determines how individual switching currents are summed in time to form the power supply current.

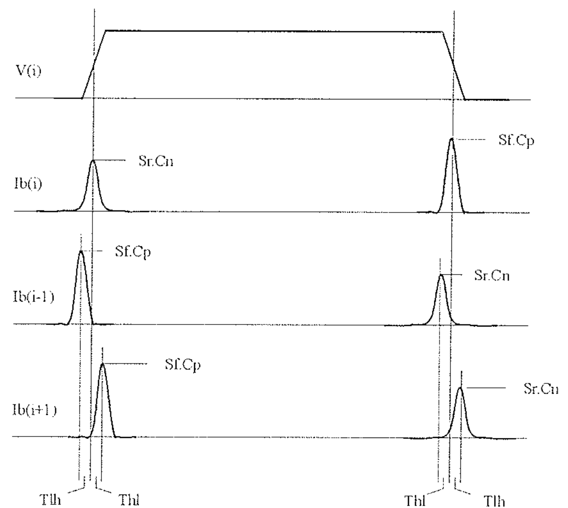

Figure 3: *Bus currents in the chain of inverting buffers with local loads*

Due to the serial signal passing across the buffer chain only a few stages are active at a given time. The sum of power supply currents in the chain depends on the interaction of delay times and the shape of the switching waveforms, but is independent of the chain length (Fig. 4).

If stage *i* is considered as reference stage in the clock pipeline, *neighbor activity* α_n can be defined as the ratio of slew rates in neighboring stages and the reference stage, measured when the reference output reaches $V_{dd}/2$:

$$\alpha_n = \frac{s_{i-1} + s_{1+1}}{2s_i}\Big|_{V_i=V_{dd}/2} \quad (5)$$

In the case when slew rate of the reference signal is larger than slew rates of it's neighbors, the switching point in stages with lower slew rates comes closer to $V_{dd}/2$ so that α_n increments. Neighbor activity in pipelines with non-symmetric switching characteristics is therefore different if measured at the rising edge or at the falling edge of the reference signal. However, as long as we are not too far from the symmetric case, values for both edges are close to each other so that an average value can be substituted.

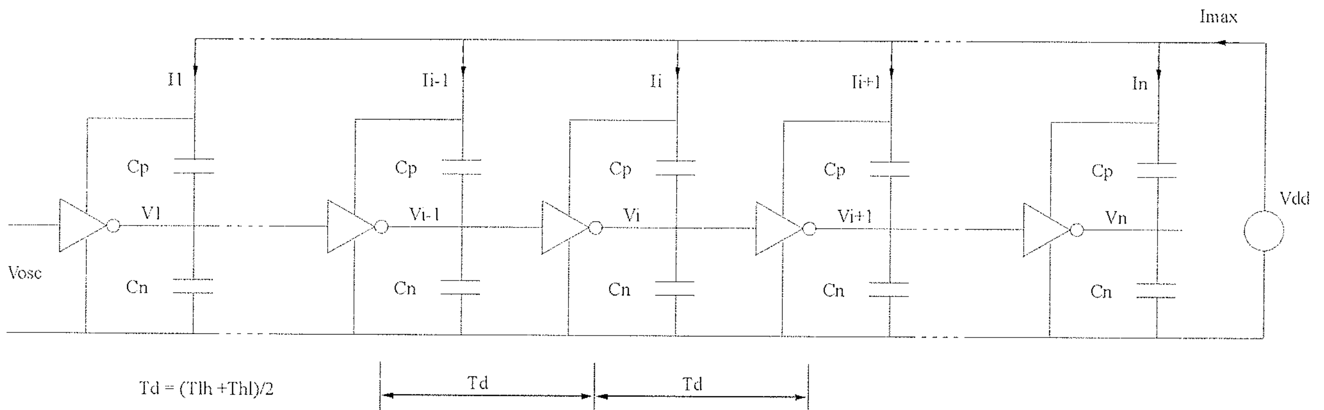

Figure 2: *The distributed clock driver as the chain of inverting buffers*

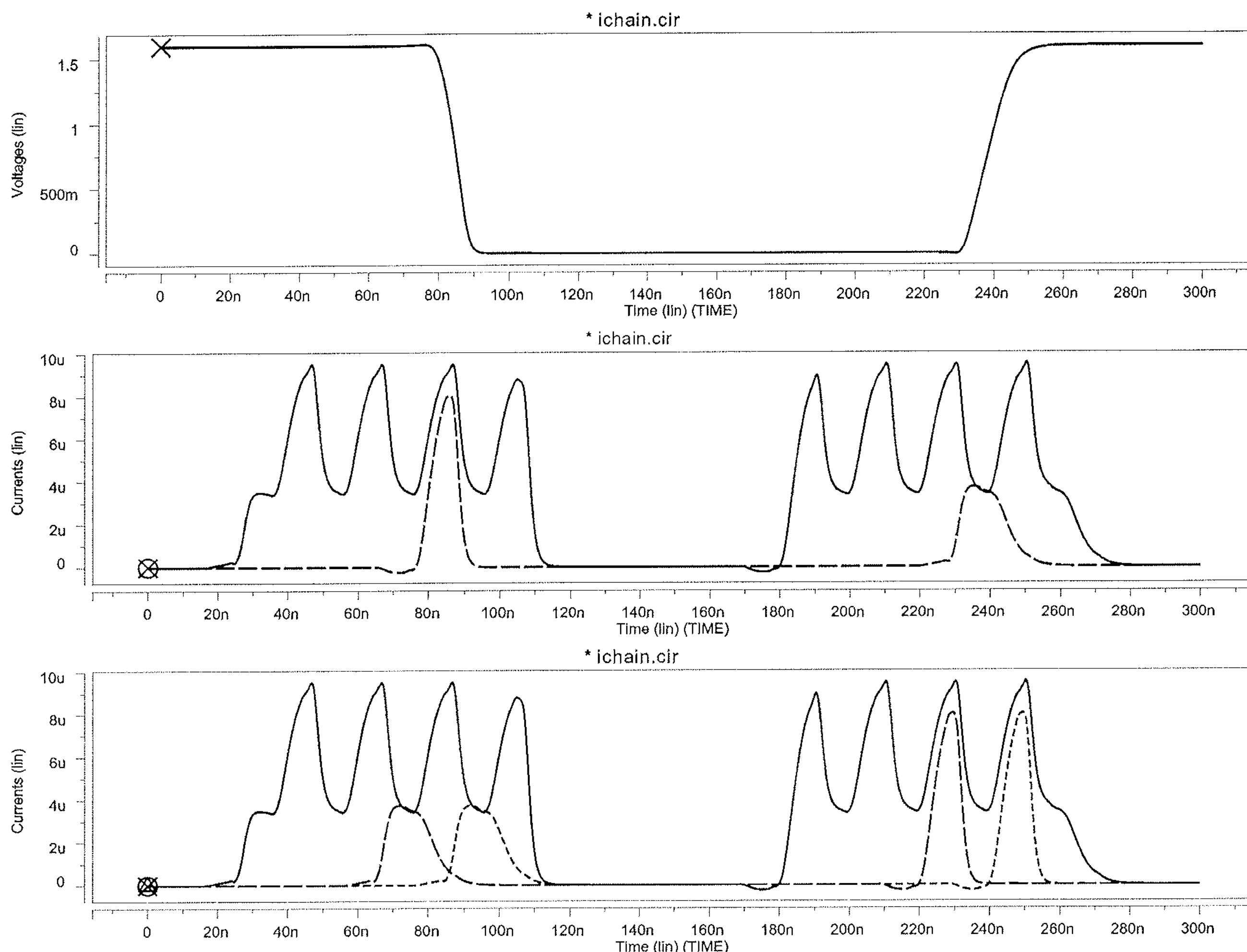

Figure 4: *Accumulation of local currents into the supply current for the case when $s_fC_p>s_rC_n$. Upper pane represents output signal in stage j; current contribution of stage j is shown by dashed line in the middle pane against the total supply current (solid line). Dashed lines in the lower pane represent current contribution of stages i, k against total supply current (solid line). On the rising edge, the supply current is dictated by currents in stages i, j that exhibit falling edges; on the falling edge, it is dictated by the current spike in stage i. The difference between solid line and the dashed lines (≈ 20%) is due to the activity of the neighboring stages. The circuit, based on Figures 1 and 2 with N = 8, was simulated at $V_{dd} = 2V_T$, $C_l = 10C_g$ and $s_fC_p = 2.5s_rC_n$.*

The average value in the range $K_p/K_n \approx 0.5...2$ is practically independent from K_p/K_n and load capacitances (Fig.5). With a series of simulations for circuits with equal absolute threshold voltages for P and N-type transistors we have found a satisfactory approximation for α_n as

$$\alpha_n = 0.555\frac{V_{dd} - V_T}{V_T} \tag{6}$$

If we take into consideration supply currents in the driving stage and in the closest two neighbors, the total supply current for rising edge signal is equal to

$$I_{dd,rise} = s_r C_n + 2s_f^{'} C_p$$

where $s_f^{'}$ stands for slew rate in the neighboring stages when s_r is maximal:

$$s_f^{'} = \alpha_n s_r$$

so that

$$I_{dd,rise} = s_r\left(C_n + 2\alpha_n C_p\right) \tag{7}$$

Current peak for the falling edge signal can be expressed in a similar way. Once both current peaks are known, we can define the *relative supply current ripple* as

$$r_r = \frac{I_{dd,rise}}{I_{dd,fall}} = ss\frac{C_n + 2\alpha_n C_p}{C_p + 2\alpha_n C_n} \tag{8}$$

For each signal transition on the input, active driver stages draw supply current $I_{dd}(t)$. As the signal travels along the pipeline, $I_{dd}(t)$ alternates between leading edge ($I_{dd,rise}$) and trailing edge ($I_{dd,fall}$) peaks. Signal transition time for the whole chain is given by

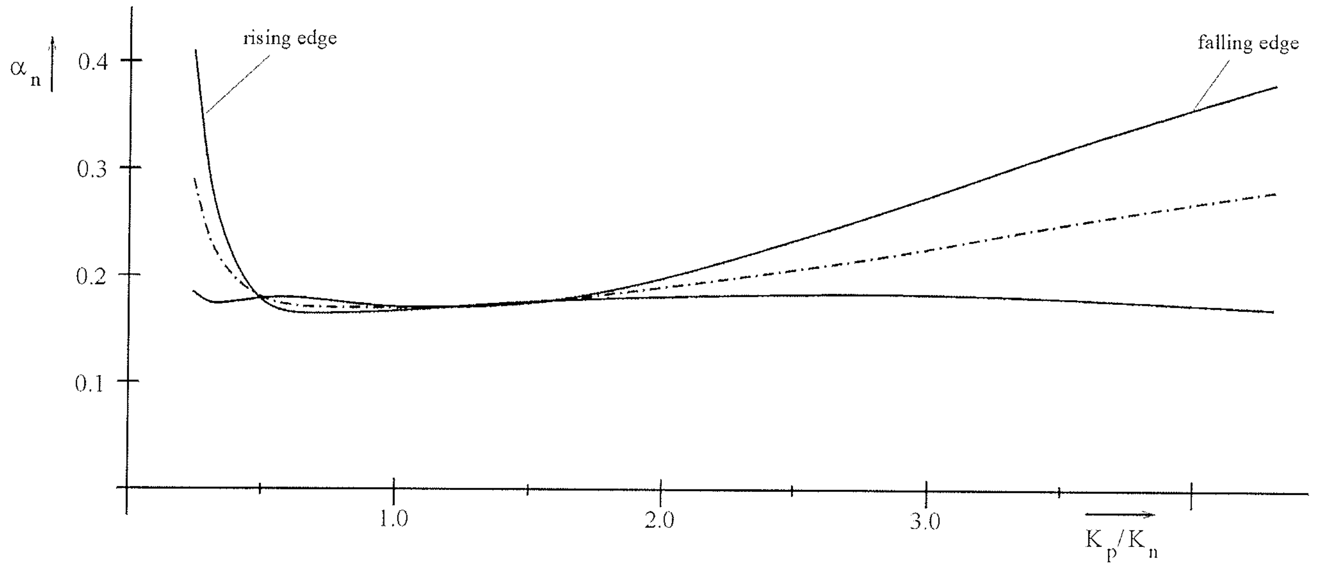

Figure 5: Activity of the first neighbors (stages i-1, i+1), measured when V_i in the reference stage reaches $V_{dd}/2$. Activity of stages next to the closest neighbors is practically equal to 0. The dashed line shows rising/ falling edge average.

$$T_t = N\frac{T_{lh} + T_{hl}}{2} \qquad (9)$$

Maximum supply current takes place in stages with rising edges if $r_r > 1$, or in stages with falling edges if the relation is opposite. Regardless of the case, maximum current occurs in every second stage so that the ripple period is equal to

$$T_{pair} = T_{lh} + T_{hl} \qquad (10)$$

3. Noise optimisation

The supply current ripple can be minimized if the rising and the falling edge peaks are made equal. By setting r_r = 1, equation 8 gives optimal clock symmetry

$$ss_{opt} = \frac{p + 2\alpha_n}{1 + 2\alpha_n p} \qquad (11)$$

If we now apply equation 6, we get optimal K_p/K_n ratio as

$$\left(\frac{K_p}{K_n}\right)_{opt} = 2ss - 1 = \frac{3 + (1-\alpha_n)(p-2)}{2(1+2\alpha_n p)} \qquad (12)$$

For purposes of noise analyze it is convenient to define the *pipeline activity* α_p as the ratio of switching currents of the entire driver chain and one single stage:

$$\alpha_p = \frac{I_{dd,rpipeline}}{I_{dd,stage}} \qquad (13)$$

In general, the entire switching event must be covered. Rising and falling edge currents are equal as long as we treat the optimized pipeline as a whole, but they can be different inside individual stages. For that reason the single stage current must be expressed by the average of rising/ falling edge values, so that α_p of a noise-optimized pipeline can be given by

$$\alpha_p = 2\frac{I_{dd,rise,pipeline}}{I_{dd,rise,stage} + I_{dd,fall,stage}} = 2\frac{I_{dd,fall,pipeline}}{I_{dd,rise,stage} + I_{dd,fall,stage}}$$

From the second expression we get

$$\alpha_p = 2\frac{s_f(C_p + 2\alpha_n C_n)}{s_r C_n + s_f C_p} = 2\frac{p + 2\alpha_n}{ss + p} \qquad (14)$$

Application of optimal symmetry from equation 11 gives

$$\alpha_p = 1 + \frac{\alpha_n p^2 + 4\alpha_n^2 p + \alpha_n}{\alpha_n p^2 + p + \alpha_n} \qquad (15)$$

In spite of quadratic form the pipeline activity α_p shows almost linear dependence from a_n and p in the range of common design conditions. Influence of p is very low because the pipeline is optimized. In most cases α_p evaluates to values around 1.4 ≈ 1.5.

4. Results

The power bus relaxation of a distributed clock system compared to the central clock system can be estimated by the ratio of peak supply currents. If C_L is the total load of a central clock buffer then the load of an equivalent N-staged clock pipeline would be given by

$$C_L = N(C_n + C_p)$$

We can assume that the central clock buffer has got symmetric switching characteristic, defined by $s = (s_r + s_f)/2$. In favor of fair comparisons we will consider only the last stage of the central clock driver. According to table 1, the switching current in that stage would reach $I_{dd,central} = s \cdot C_L$. The switching current of the distributed driver can be expressed by the average single stage current and α_p, so that we can define the *power bus relaxation factor* R as

$$R = \frac{I_{dd,central}}{I_{dd,pipeline}} = \frac{(s_r + s_f)N(C_n + C_p)}{\alpha_p(s_r C_n + s_f C_p)} \quad (16)$$

Application of equations 14 and 11 gives

$$R = N\frac{(p+1)^2(2\alpha_n + 1)}{2p + 4\alpha_n(p+1)^2} \quad (17)$$

For a typical design case with $p = 2$ and $a_n = 0.15$ we get $R = 1.24\ N$. Bus relaxation factor larger than N can be explained by optimal weighting of rising/falling edge currents and local load discharging in the pipeline, leading to a situation where discharge currents disappear from the power supply lines.

Substrate noise reduction has somehow different background. Since only one pipeline node is active at a given time, we can assume that the coupling capacitance of clock nodes is virtually reduced by N. If the pipeline activity is considered as well then a rough estimation for substrate noise reduction can be given by

$$S = \frac{N}{\alpha_p} \quad (18)$$

We see that substrate noise reduction is smaller than R, particularly because equation 18 is probably too optimistic. Typical values for S can be expected somewhere from 0.5 N to 0.75 N.

It has to be pointed out that above noise reduction assessments are valid for clock pipeline alone. Although being known as an important source of switching noise, the clock driver is not the only noise generator. Regular structure of the pipelined driver allows relative high values for R and S that cannot be achieved in other parts of the system.

5. Conclusion

One way to distribute activities of a synchronous digital system in time is to replace the central clock by a large number of equally delayed signals generated by a clock pipeline. The sum of switching currents in this case produces pulses with low amplitude and long duration, leading to substantial reduction of supply current spikes in comparison to systems with central clock. The resulting power bus relaxation and substrate noise reduction are beneficial for both pure digital and mixed projects.

Pipeline clocking has the potential to reduce three important noise sources: power bus bouncing, signal cross-talk and substrate noise. In order to find optimal design measures for noise reduction, switching properties of clock pipelines have been studied. Neighbor activity has been defined as the basis for calculation of a number of important parameters, among which supply current ripple, ripple frequency and length, optimal symmetry and the K_p/K_n ratio have been found. Assessment of power bus relaxation and substrate noise reduction have been given as well.

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PLACEMENT AND ROUTING OF HIGH VOLUME ICs

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Key words: semiconductors, microelectronics, IC, integrated circuits, high volume production, placement, routing, circuit area optimization, random logic layout, grid-less cell layout approach, density analysis tool

Abstract: A place and route tool is an integral part of a modern integrated circuit design environment. It is often that a custom circuit requires a large block of random glue logic for its operation. This paper introduces techniques for manual optimisation of area for blocks of random glue logic. An area reduction of 25 % to 40 % is achievable compared with the results of modern commercial place and route tools.

Nameščanje in povezovanje pri integriranih vezjih za množično proizvodnjo

Ključne besede: polprevodniki, mikroelektronika, IC vezja integrirana, proizvodnja množična, nameščanje, povezovanje, optimizacija površine vezja, geometrija logike naključne, geometrija celice brez mreže, orodje za analizo gostote

Izvleček: Orodje za nameščanje in povezovanje je običajno vključeno v moderno okolje za načrtovanje integriranih vezij. Pogosto vezja ASIC vsebujejo večje bloke povezovalne logike. Članek obravnava tehnike za ročno optimizacijo površine vezij povezovalne logike. Predstavljene metode omogočajo izdelavo blokov na 25% do 40% manjši površini kot moderna komercialna orodja za nameščanje in povezovanje.

1. Introduction

The area used for the interconnections in a large block of random glue logic designed for a traditional two level metallization process exceeds the effective area used by the cells. With the increased number of devices this ratio of channel area to cell area deteriorates. Ratios 2 to 3 in favour of the channel width are common. Assuming that the logic can not be optimised there are two common ways to decrease the block area: using a technology with better resolution and using a process with multiple levels of metallization. As the most cost-effective process was selected in the first place it is usually unacceptable to change the process during the layout design.

With the advent of dense processes and useful place and route tools integrated in the design environment a third solution does not seem obvious. With a convenient set of tools one can manually optimise the layout area better than the best place and route tools.

Gain in circuit area is the result of library optimisation, placement optimisation and routing optimisation. The task is labour intensive but for high volume ICs it is cost effective.

In the following text it is assumed that cells are placed in horizontal rows, metal1 (M1) is used for the horizontal wire segments and metal2 (M2) is used for the vertical wire segments as well as for wire segments connecting cell pins with the channel segments.

2. Library

Most commercial place and route tools require cells build with arbitrary grid. All pins must also be placed on the grid. With this constraints it is tedious to design cells and a couple of iterations required with a library conformance checking tool to complete a cell.

A faster grid-less approach is used in the design of optimised cells of the proposed method. Since each cell need not be expanded to the first grid point and less area is lost in on-grid placement of vias an average 10 % area gain is achieved in total area of all cells for a block. This may not look much with the channel area taking 2-3 times the cell area but the decreased width of the row of cells results in smaller width of the entire block.

The second advantage with the grid-less approach is the number of vertical passes through cells. This is increased by over 30 % for grid-less routing. This is a result of lesser constraints in via placement.

The third amelioration in the proposed library is a number of versions of each cell. The versions differ in the number of pins with via and M2, which are accessible from the channel. Observe a cell NAND2 on Figure 1, where all pins have vias (fig. 1a), on (fig. 1b) where only the output pin has vias, and a case with no vias (fig. 1c). As quite a few cells can be connected to the neighbouring cells using metal1 in the area used for the cells without wasting the space in the channel. This calls for some consideration in vertical placement of pins. Attention must also be paid to horizontal metal1 channels to as many pins of the cell as possible.

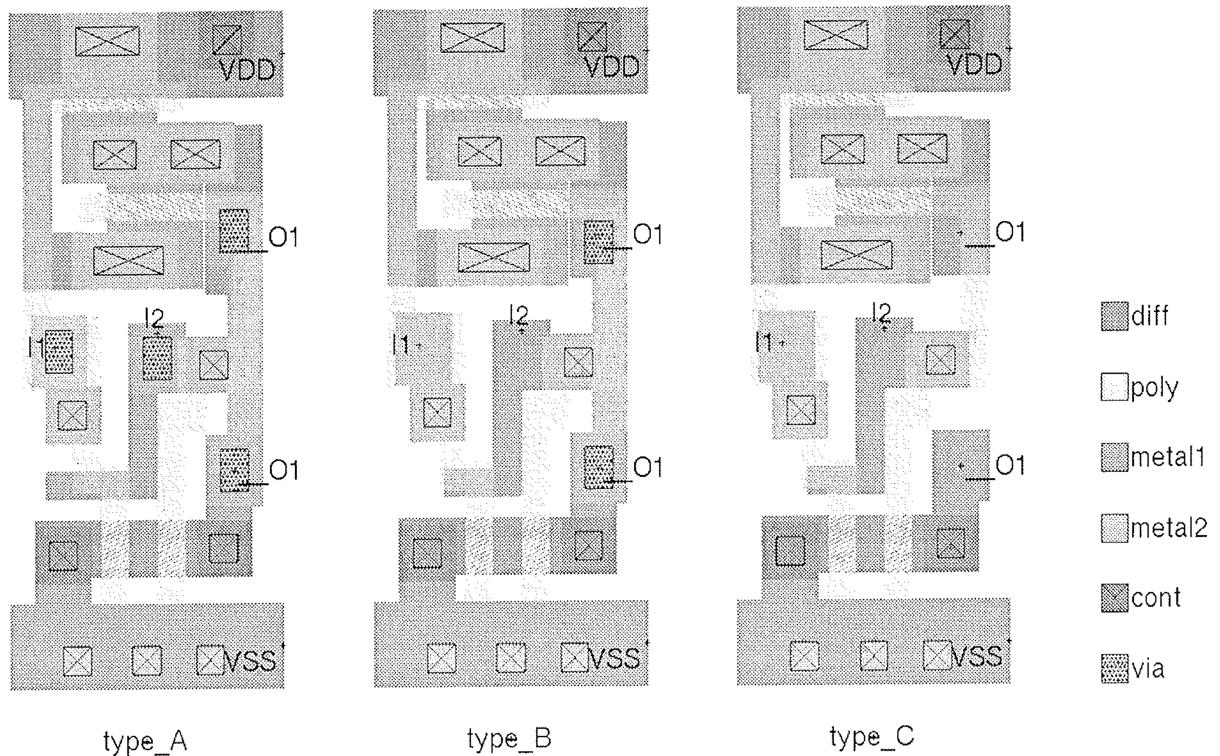

Figure 1: *Three versions of NAND2: (A) every pin is accessible from channel, (B) only output is accessible from channel, (C) all connections must be made in metal1. Well is omitted to improve readability.*

3. Placement

The placement is carried out in four phases: placement using some well known algorithms, visual placement evaluation, local optimisation with using alternative layouts of cells, and another visual placement evaluation.

A graphic density analysis tool (see fig. 2) displaying cell placement and the horizontal and vertical wire density used to evaluate both automatic phases. Entire block is split by a raster with grid spacing in both directions equal to the inter-row spacing. Various intensities of two colours are used to paint each segment depending on the number of wires passing. The number of passes through the row is evaluated for each segment and compared against the number of vertical wires that should pass this segment. The third colour is used to emphasise the segments which lack vertical passes through cells.

One can set a number of parameters with a typical placement tool /1/ to change optimise the placement according to the requirements of the task at hand. A configuration with an appropriate ratio between a small sum of horizontal tracks and a small number of vertical congestions is selected alternately using placer and density analyser. As the tool occasionally produces unacceptable results after minor changes to the set-up parameters the results of the global placement stage are evaluated with the density analyser.

In the local optimisation phase of placement a trade off between wire length increase and number of nets made of metal1 only is made. Converting a few nets to metal1 in the areas of horizontal congestion saves a number of tracks, which decreases the block size even though the overall wire length may not be optimal. Local optimisation is made by changing cell positions and swapping cells (type A) with versions where less metal2 is used (type B/C). Besides saving tracks (1.e. channel area) this increases the amount of vertical metal2 passes, which may cross the area thus improving the vertical congestions. This also decreases the number of feed-through cells, which need to be inserted to feasibility of routing.

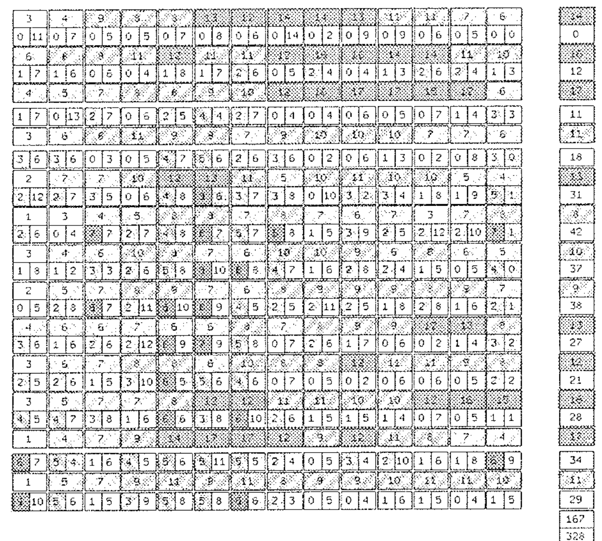

Figure 2: *Density of a circuit*

After placement evaluation with the density analyser manual optimisation of a few critical congestions can improve the placement in a reasonable amount of time to obtain another 5% gain in the block area.

4. Routing

Manual routing can be performed efficiently with a couple improvements in the wiring capabilities of the layout tool /2/. Starting or ending a wire on a label of the current net when a button is pressed close to the label and the obstacle avoiding ability when wiring through a row of cells are in need. A vertical grid is imposed on the channel to improve the quickness of routing.

The routing is started with sorted nets, which can be wired entirely in M1. The additional cells of type A are swapped for cells of type B/C to add vertical passes. Next, long horizontal segments are routed close to the supply rail of the cell rows. This improves compressibility of the channel. Lastly, all other nets a routed sorted by their length, longest first.

When all the nets are connected and the circuit proves to be LVS clean a channel optimisation is started. The horizontal congestions in each channel are identified and improved in the following ways:

- with large distributed nets a horizontal segments can be moved to other channels with no vertical passes used,
- by a horizontal segment being moved a couple of channels away to a non-congested area because of additional vertical passes resulting from metal2-less cell swap,
- by swapping the tracks and moving the contacts one can wire a net entirely in M2.

This actions decreases the worst number of tracks in a channel by 10% to 20%.

The channel compression is the last step in the routing process. This operation is also performed by most routers. Some tools also attempt contact moving to improve compression but manual inspection of critical areas with some track swapping can shrink the cannel an additional 3% to 5%.

5. Conclusions

Cell design in area optimal layout of digital integrated circuits with good metal1 inter-cell connectivity and without metal2 pins can improve block area in two ways: horizontal tracks are saved in the channel and fewer feed-through cells are needed for good vertical connectivity. The local placement optimisation for a metal1 inter-cell connection is more area efficient the minimum wire length. Interactive routing yields smaller block areas and is a valid alternative for very high volume ICs.

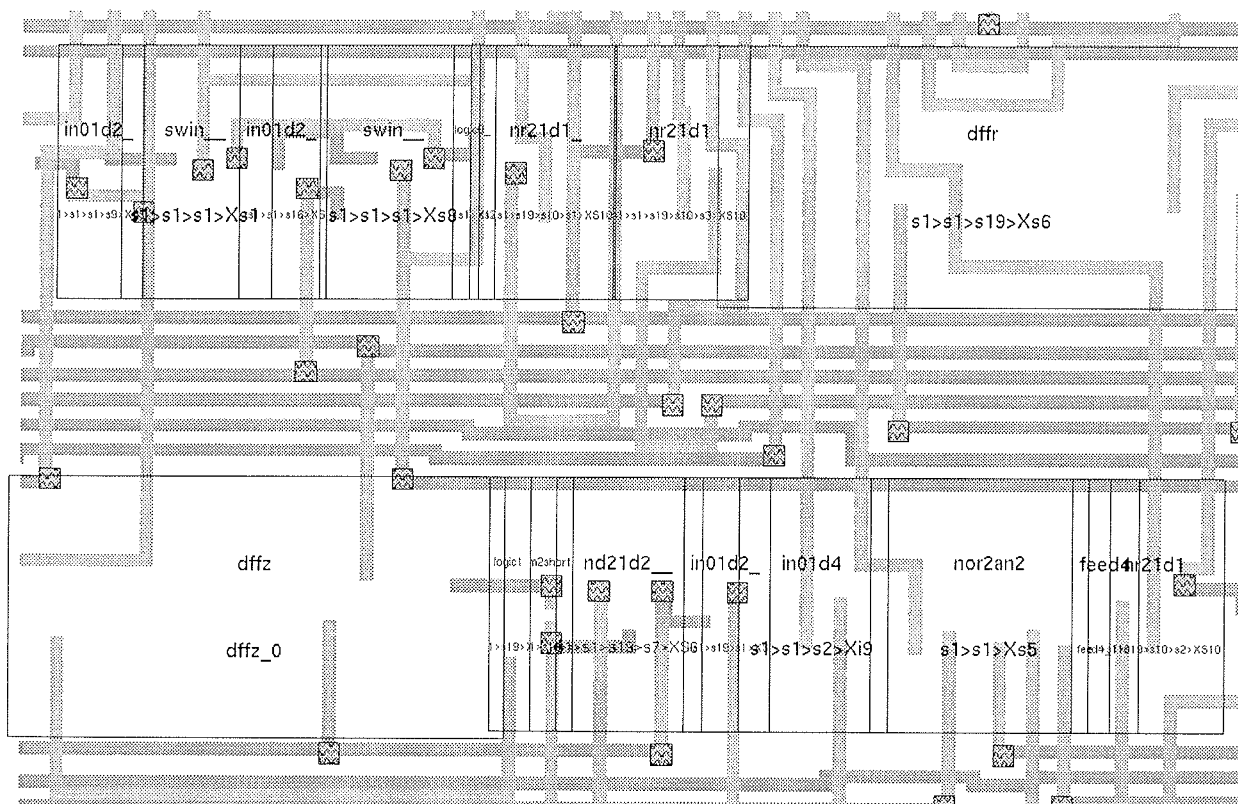

Figure 3: *A closer look at the manual wiring.*

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REVERSE VOLTAGE AND OVERVOLTAGE PROTECTION FOR A 5V CMOS TECHNOLOGY

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Key words: semiconductors, IC, integrated circuits, CMOS processes, CMOS technologies, reverse voltage protection, overvoltage protection, integrated protection, protection circuits, control circuits, simulation results, practical implementations

Abstract: In automotive applications the IC must withstand various hostile environments and still guarantee normal operation. One of the requests is the survival of the overvoltage and reverse supply voltage. For that usually a high-voltage process is used. In this paper a protection structure for a 5V CMOS process is presented. The proposed structure protects the internal circuit against up to +26V and down to -16V of the external supply voltage.

Vezje za zaščito pred nasprotno in previsoko napetostjo v 5V CMOS tehnologiji

Ključne besede: polprevodniki, IC vezja integrirana, CMOS procesi, CMOS tehnologije, zaščita pred napetostjo obrnjeno, zaščita pred prenapetostjo, zaščita integrirana, vezja zaščitna, vezja krmilna, rezultati simulacije, izvedbe praktične

Izvleček: Integrirana vezja, ki se uporabljajo v avtomobilskih aplikacijah, morajo biti odporna na razne sovražne vpliva okolja, kjer delujejo. Ena od takih zahtev je odpornost na previsoke napetosti in nasprotne napetosti na napajalnih priključkih. Za doseganje teh zahtev se ponavadi uporabi visoko-napetostna tehnologija in s tem elementi, ki so odporni na te napetosti. V članku je opisana zaščitna struktura v 5V CMOS procesu. Predlagana zaščita ščiti notranje napajanje integriranega vezja pred zunanjimi napetostmi v območju od -16V do +26V.

1. Introduction

The complexity and quantity of the embedded electronics in today's automotive products is steadily rising. It is expected that the value of the built in electronics will grow up to 5-10% of the total manufacturing cost of the car. Due to the large series of production the automotive electronics is usually integrated in a chip or chipset. Due to the safety and reliability requirements the IC must withstand hostile environments. The most common failures originate from various wiring problems. The most common wiring problems are shorted and disconnected lines. The IC must sense these problems, survive and signalise the existence of the problem. The IC usually operates with a regulated low-voltage supply (5V), but the supply lines can be shorted to the automotive car battery or reversed. In this article a standard CMOS technology protection structure against these overvoltage and reverse supply voltages is presented. A high-voltage CMOS technology is usually used in such applications, but the standard CMOS technology offers an advantage in the IC manufacturing cost.

2. Supply protection circuit

The supply protection circuit is made from two blocks. The first one is the actual protection structure made from four PMOS transistors, the gate controlling high-voltage NMOS transistors and from poly resistors. The second block is the control block, which monitors the supply voltage and controls the behaviour of the protection block. Each block is designed in such a way that it can also tolerate reverse supply voltages.

2.1 The PMOS protection structure

The supply protection structure is constructed from four PMOS transistors in series (the topology is presented in Figure 1.). Each gate of these PMOS transistors is controlled by a high-voltage NMOS pull-down transistor, which can tolerate drain voltages up to 35V. The series PMOS transistors are thereby switched on and off with the signal *con*, which is generated by the control circuit. In normal operation conditions the *con* signal is high, then the PMOS gates are pulled down and thereby the transistors are opened. The W/L ratio must be high and depends on the supply current of the IC. In this application the supply current is in the range of 5-10mA. The series resistance is approximately 20Ω. Because the IC also incorporates digital logic the internal supply is decoupled with a low-ohmic capacitor.

If the external supply voltage exceeds the allowed 7V, then the *con* signal goes low and the PMOS transistors are closed. The internal supply is shorted to the supply ground. The complete external supply voltage is divided between the four PMOS transistors. Because the maximum allowed PMOS drain-source voltage is 8V and the maximum expected external supply voltage is +26V four transistors have been used. If the supply voltage would stay below +24V only three transistors would be sufficient. With the use of series transistors the excessive voltage is divided between a number of devices and therefore preventing various break-

downs (gate, drain-source, diffusion to substrate ...) due to large voltages. The protection structure is made from devices available in standard CMOS processes (this also includes the high-voltage NMOS transistor).

If the IC is exposed to reverse supply voltages the numerous N-diffusion and N-well in the P substrate diodes are opened. The resulting current thermally destroys the IC. In the presented protection circuit all NP diode structures are protected by series poly resistors and thereby limiting the reverse voltage current. Special care was taken in the layout design to prevent the reverse current bipolar effects.

Figure 1: *The overvoltage protection structure*

2.2 The control circuit

The task of the control circuit is to monitor the supply voltage and detect overvoltage conditions. This is achieved with the comparison of a fraction of the external supply voltage with the reference voltage. The control circuit is made from a band-gap reference voltage source, comparator and the supply protection (Figure 2.). Because the control circuit must operate during the overvoltage condition it has its own supply protection. This protection is made from a series resistor and five transistor thresholds. If the supply voltage exceeds the 5*Vt voltage (which is process and temperature dependent) the transistors begin to conduct and therefore causing a voltage drop on the resistor. So the supply of the control circuit never exceeds the allowed maximum voltage. Because of the high resistance of the series resistor the current consumption of the control circuit must be kept low (in this case 50mA).

The band-gap voltage is compared to the fraction of the supply voltage and if this voltage exceeds the predefined voltage the control circuit outputs (*con* and *conb*) are changed. These signals are also used to set the IC output stage amplifier into a defined error signalising state, which can be detected by the IC readout electronics.

Figure 2: *The control circuit*

The high resistance of the supply protection resistor is also limiting the reverse voltage current.

2.3 Simulation results

Both conditions have been simulated to verify the various voltages and currents across the circuit to check if there are excessive values which could lead to the IC destruction.

In figure 3. the overvoltage condition simulation results are visible. The supply voltage is swept from 0 to 26V. At 7V the control circuit switches off the PMOS transistors. The voltage distribution across the transistors and the control signal behaviour is visible.

Figure 3: *Overvoltage condition; voltage distribution and control signal*

The reverse voltage condition simulation can be seen in Figure 4. The reverse voltage is swept from 0 to -16V. The voltages across the protection structure and the reverse current can be seen on the plot. The reverse current is limited to 1.6mA, which is sufficient to prevent damage of the IC.

Figure 4: *Reverse voltage condition; voltage distribution and reverse current*

2.4 Implementation

The proposed protection structure has been implemented in a double-metal, double-poly CMOS 0.8μm technology. A test IC was fabricated to measure the circuit behaviour. The measurements proved the protection capabilities of the structure in both overvoltage and reverse voltage conditions. The layout of the implemented protection structure is in Figure 5. The protection structure is on the upper side of the IC, the control circuit on the lower side.

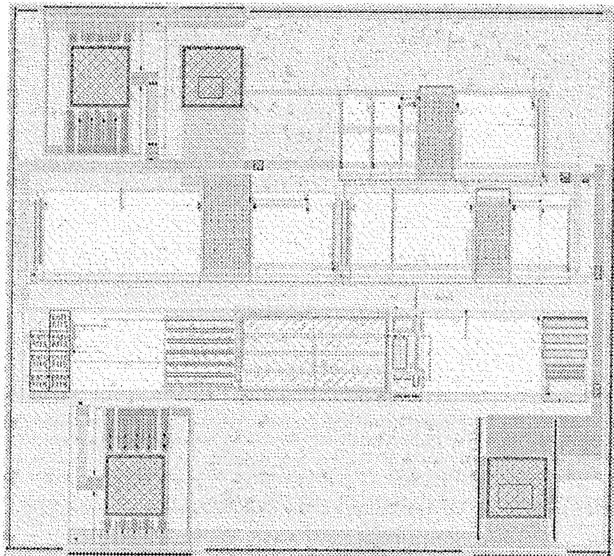

Figure 5: *The protection structure test chip layout*

3. Conclusion

The design and implementation of a supply protection structure was presented. It was shown that also low voltage (standard) CMOS processes can be used for IC's in applications, where the IC must withstand excessive voltages on the supply lines.

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INTELLIGENT SYSTEM FOR DECOUPLING MULTIPLE RFID TAGS

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Key words: informatics, ID, IDentification, RFID tags, Radio Frequency IDentification tags, electrical coupling, electrical decoupling, electrical crosstalk

Abstract: A novel approach to decoupling of multiple RFID tags has been presented. It consists of reducing the effective inductance of the tag resonant coil by switching on the part of coil to produce reverse mutual coupling. This happens when the tag is in inactive state. It has been shown that up to 50 tags positioned very close to each other can be accessed in one second without any crosstalk.

Inteligentni sistem za zmanjšanje sklopov med množico radiofrekvenčnih identifikacijskih kartic

Ključne besede: informatika, identifikacija, RFID kartice za identifikacijo s frekvencami radijskimi, sklop električni, razklop električni, presluh električni

Izvleček: Opisan je nov pristop za zmanjšanje sklopa med množico radiofrekvenčnih identifikacijskih kartic (RFID tag). Princip delovanja temelji na zmanjšanju inductivnosti resonančne tuljave kartice z vključitvijo dela tuljave na način, ki povzroči nasprotni znak sklopa. To se zgodi ker je kartica v neaktivnem stanju. Do 50 kartic, ki so zelo blizu skupaj je možno prebrati v eni sekundi, brez medsebojnega presluha.

1. Introduction

Tagging of articles for identification and/or theft protection is known. For instance, many articles are identified using a bar code comprising coded information, which is read by passing the bar code within view of a scanner. Many articles also include a resonant tag for use in theft detection and prevention. More recently, passive resonant tags which return unique or semi-unique identification codes have been developed. These tags typically include an integrated circuit (IC), which stores the identification code. Such "intelligent" tags provide information about an article or person that the tag is associated with and is detected in the zone of an interrogator or reader. The tags are desirable because they can be interrogated rapidly, and from a distance.

Radio frequency identification (RFID) tags or cards generally include a resonant antenna circuit electrically connected to the IC. The IC is essentially a programmable memory for storing digitally encoded information. The interrogator (transmit antenna) creates an electromagnetic field at the resonant frequency of the RFID tag. When the tag is placed into the field of the interrogator, an AC voltage is included in the resonant antenna circuit of the tag, which is rectified by the IC to provide the IC with an internal DC voltage. As the tag moves into the field of the interrogator, the induced voltage increases. When the internal DC voltage reaches a level that assures proper operation of the IC, the IC outputs its stored data. To output its data, the IC creates a series of data pulses by switching an extra capacitor across the antenna circuit for the duration of the pulses, which changes the resonant frequency of the tag, detuning the tag from the operational frequency. That is, the tag creates data pulses by detuning itself, which changes the amount of energy consumed by the tag. The interrogator detects the consumption of energy in its field and interprets the changes as data pulses.

Although such RFID tags or cards are known, there are still technical difficulties and limitations associated with the operation of such tags. One problem with attempting to read multiple RFID tags within an interrogation zone of the interrogator is that more than one tag may be activated by the interrogator at about the same time. When such tags are located proximate to each other, the fields generated by one tag can disturb the fields generated by another tag. This problem of mutual inductance is especially significant for RFID tags, which transmit their information by detuning, as described above. As a consequence, the reading distance drops and the modulation of the tag can become completely ineffective due to the fact that such modulation depends upon the tag being in resonance (or close to it). Thus, such detuning caused by other tags can make reading of stored information impossible or nearly impossible.

Yet another problem often encountered when reading intelligent tags or cards is a large variation in the received power, for instance, when the tag nears the power transmit antenna of the interrogator. As the tag approaches the transmit antenna, the received power increases, which can cause problems due to excessive voltage or power dissipation and, because of a decrease in tag Q, an inability to sufficiently modulate the tag with the data using the aforementioned detuning approach. Such detuning or modulation problems increase the difficulty of correctly reading the tag.

Accordingly, there is a need for a method of preventing RFID tags from generating fields, which disturb or affect other nearby resonant cards or tags. There is further a need

for a RFID tag whose operation is not adversely affected by large variations in received power. The present invention fulfils these needs.

2. Innovative solution for decoupling multiple RFID tags

The present solution is a radio frequency intelligent transponder. The transponder includes an integrated circuit for storing data and an inductor electrically connected to the integrated circuit. The inductor includes the first coil electrically connected to a second coil. A resonant capacitor is electrically connected to the integrated circuit and to at least one of the first and second coils, such that the resonant capacitor and the at least one connected coil have the first predetermined resonant frequency. A switch having a position A and a position B is provided for selectively allowing current to flow through the second coil. When the switch is in the first position, exposure of the transponder to an external field at or near the first resonant frequency induces a voltage in the inductor and causes the first current to flow through the inductor in the first direction, thereby generating a local field. When the switch is in the second position, exposure of the transponder to an external field at or near the first resonant frequency induces a voltage in the inductor and causes the first current to flow through the first coil in the first direction, thereby generating the first local field and the second current to flow through the second coil in the second, opposite direction, thereby generating a second local field. A sum of the first and the second local fields approaches zero.

The described solution is a radio frequency intelligent transponder comprising an integrated circuit for storing data and an antenna circuit. The antenna circuit comprises the first coil and a resonant capacitor having a predetermined resonant frequency electrically connected to the integrated circuit for providing power to the integrated circuit and for transmitting the data stored in the integrated circuit to a device reader. Exposure of the transponder to an external field at a frequency near the predetermined resonant frequency causes the first current to flow through the antenna circuit in the first direction, thereby producing the first local field, which couples the transponder with its environment. The transponder further comprises means for selectively generating the second local field, wherein a sum of the first and the second local fields approaches zero, for selectively decoupling the transponder from its environment.

Furthermore the present solution comprises an intelligent resonant tag comprising an integrated circuit for storing data and the first antenna circuit electrically connected to the integrated circuit. Exposure of the first antenna circuit to an electromagnetic field at the first predetermined radio frequency induces a voltage therein, which produces a current flowing in the first direction therethrough, thereby producing the first local field. The induced voltage also provides power to the integrated circuit such that the data stored therein is read therefrom and transmitted at the second predetermined radio frequency. The tag also comprises means for generating the second local field, which at least partially cancels the first local field generated by the first antenna circuit.

The complete solution is shown in figure 1. The resonant coil inductance in active state is the sum of inductances Lr and Lc as shown in figure 1. The series coil resistance is given by resistors Rs1 and Rs2 while switch resistance is "ON" position is given by Rs3.

Figure 2a shows the implementation of the tag. Again the total coil inductance in active state is given by the sum of LL and Lc, Rs1 is given by the quality of the resonance circuit, while resistance Rs is mainly the "ON" resistance of the integrated switch. Figure 2b shows the equivalent circuit of the tag in active state and figure 2c shows the equivalent circuit of the tag in the non-active, decoupled state.

3. Conclusions

A novel approach for decoupling of multiple RFID tags has been presented.. An ASIC has been designed to perform the described function. The photomicrograph of the ASIC is shown in fig. 3. The described system is widely used in various applications from supermarket product tags to warehouses and libraries inventory monitoring.

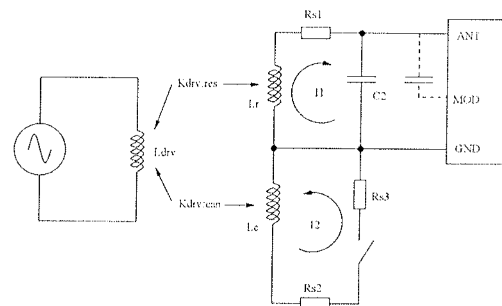

Figure 1: *An equivalent electrical circuit diagram of an interrogator and resonant frequency identification (RFID) device*

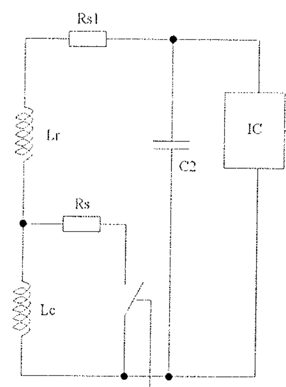

Figure 2a: *An equivalent electrical circuit diagram of the intelligent RFID tag*

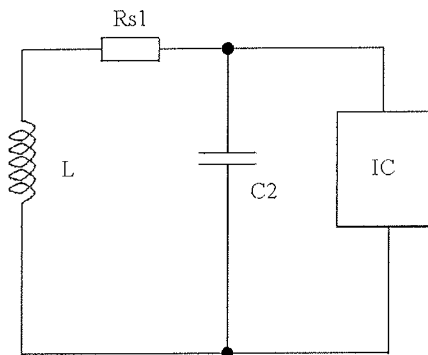

Figure 2b: *A schematic diagram of the equivalent electrical circuit of the RFID tag in an active state*

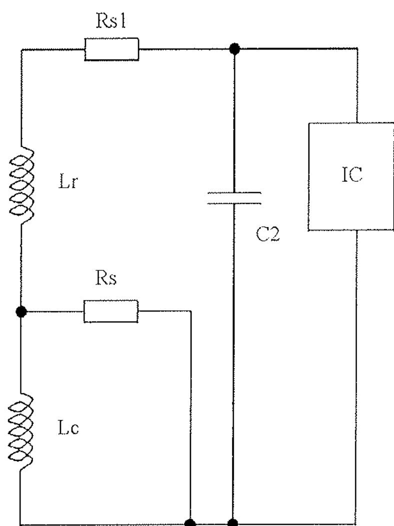

Figure 2c: *A schematic diagram of the equivalent electrical circuit of the RFID tag of fig. 2a in an inactive state*

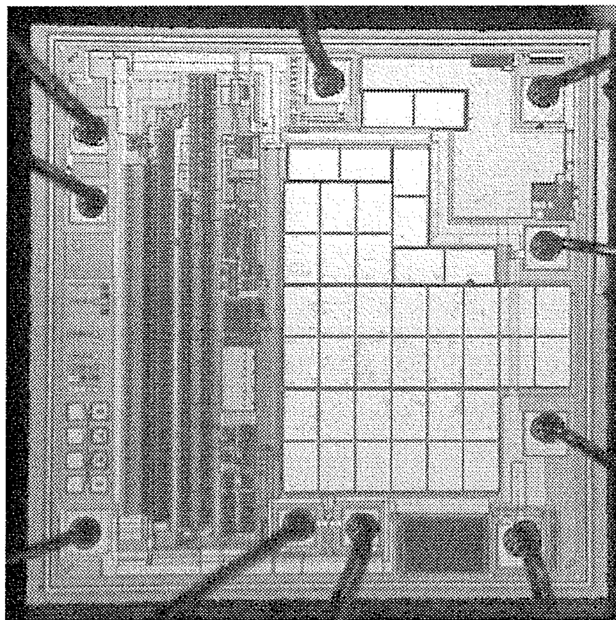

Figure 3: *The photomicrograph of the ASIC*

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MULTIDIMENSIONAL CAPACITANCE MEASURING SYSTEM

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Key words: position measuring, capacitance measuring, multidimensional capacitance measuring, patent applications, CMOS technologies, distance measurements, angular position measuring, linear position measuring, absolute positions, practical results

Abstract: A patent pending principle for multidimensional capacitance sensing system was developed and tested using standard CMOS technology. The described principle is suitable for a number of applications such as absolute angular or linear position , distance measurements, joystick pick-up or any position control in one or more axes. The test chip implementation comprised two dimensional sensing system which was used as absolute angular position sensor . The sensor resolution was limited only by external PCB limitations.

Večdimenzionalni kapacitivni merilni sistem

Ključne besede: merjenje položaja, merjenje kapacitivnosti, merjenje kapacitivnosti večdimenzionalno, prijave patentne, CMOS tehnologije, merjenje razdalj, merjenje položaja kotnega, merjenje položaja linearnega, položaji absolutni, rezultati praktičnii

Izvleček: Članek opisuje patentirani sistem za večdimenzionalno merjenje kapacitivnosti, ki smo ga razvili in preizkusili v standardni CMOS tehnologiji. Opisani sistem je primeren za številne aplikacije, kjer potrebujemo meritev razdalje ali položaja v eni ali več oseh. Testno vezje ki smo ga razvili smo uporabili za realizacijo absolutnega kotnega merilnika. Ta testni sistem je omogočal 8 bitno resulucijo, ki je bila omejena samo z tehnologijo izdelave tiskanega vezja za merilne elektrode.

1. Introduction

A number of capacitance based position measuring systems are known. The vast majority of them is based on differential principle where a ratio of two excitation signals having a 180 degree phase difference is used. Our system solution is unique since it uses two 90 degree shifted signals which are summed and subtracted to generate four excitation signals. These excitation signals are fed to 4 excitation plates on external PCB. The arrangement of these plates defines the position measurement system range (360 degree or any chosen angle).

The sensing plate is located on separate PCB which is placed over the excitation plates PCB and can be freely rotated. The electrical pick up from sensing plate is done using a capacitor between the excitation and sensing PCB. This capacitor can be realised as a metal rim on both plates. Such arrangement requires no wire connection to rotating sensing plate what makes the system very easy to use and robust.

In the chip the signal from sensing electrode is processed to determine the ratio of both excitation signals. Due to the fact that there are four excitation signals we can determine the amplitude and polarity of both basic excitation signals thus knowing the absolute position of the sensing plate in respect to four excitation quadrants.

Fig. 1 presents the basic layout of the two PCBs and the cross-section of mechanical system.

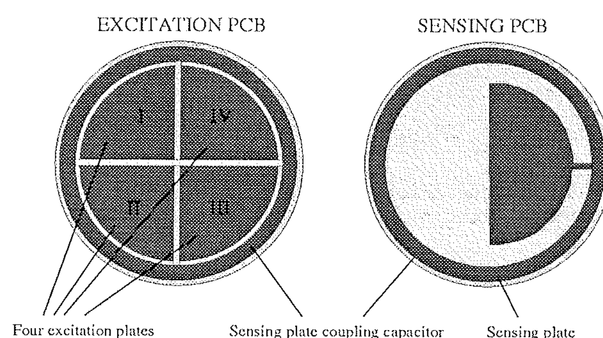

Fig. 1a: PCB layout for absulute 360 degree angle mesurement system

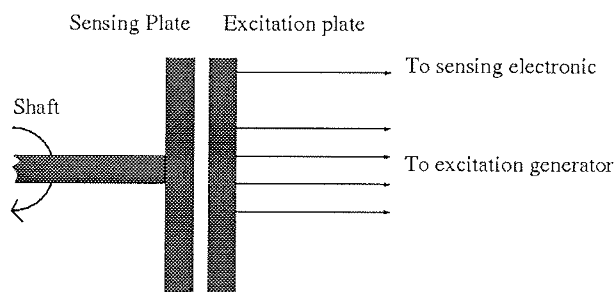

Fig. 1b: Cross-section of mechanical assembly

2. Electrical system

The system electronic can be divided in two main blocks . The excitation signals generation and the sensing signal processing.

The excitation signal generation uses internal RC oscillator to generate the basic frequency. This frequency is divided down to generate two 90 degree shifted signals. In case more than two dimensional system is required an additional pair of 90 degree shifted signals can be generated using a factor of two higher or lower frequency than the basic one. The two 90 degree shifted signals (called A and B) are fed to four summing points where the combinations A+B, A-B,-A+B,-A-B are generated. Those four combination present the four excitation signals needed for absolute position measurements.

The receive signal on sensing node is first amplified using a low noise amplifier having a capacitor in the feedback. To ensure correct DC potential a high ohm resistor (~10Meg Ohms) is needed. If the technology does not provide this possibility also so called "house keeping cycle" system can be used. In this case the DC potential is restored by discharging the feedback capacitor in a special clock cycle during which the measurement system is not operating. Since these cycles can be generated every 64 or 128 normal clock cycles they do not degrade the measurement system.

The amplified signal is fed to two phase selective rectifiers controlled by the two 90 degree shifted excitation signals. In case more dimensional system is used also the number of phase selective amplifiers is increased to match the number of basic excitation signals. The two (or more) phase selective rectifiers outputs directly present the level of each excitation signal content (which is used to control the rectifier) in the receive signal . The signal generated by the 90 degree shifted excitation signal is suppressed by further low pass processing of the rectifier output using integration.

To ensure perfect linearity the integrator output voltages of both channels are chopped by their excitation signals and fed back to the low noise amplifier input. There they are summed with the receive signal. This close loop configuration keeps the output of input amplifier and both phase selective rectifiers at zero signal level.

The signal representing the measurement value is displayed in the output voltages of the two integration blocks needed to keep the "zero signal state". Since there is always zero signal voltage in the most critical part of receive channel it quarantines perfect linearity.

Fig2. presents the basic schematic of excitation and receive block.

3. Conclusion

The described system was realised in 0.8μm standard CMOS technology. The test chip was evaluated both as stand alone electrical system and in combination with external PCB and mechanical assembly as absolute angle measurement system. The achieved resolution of angle measurement system was 8 bit. The limiting factor was not the electrical characteristic of measurement system but the precision of PCB manufacturing.

The electrical characterisation of capacitance measurement system yielded excellent results:

- measurement gain 1V/pF, 10V/pF, 20V/pF
- output spot noise 1.5μV/root(Hz) or 0.075aF/root(Hz)
- output offset <5mV
- output temperature drift <2μV/degree
- signal to noise ratio 110dB in 100Hz bandwidth

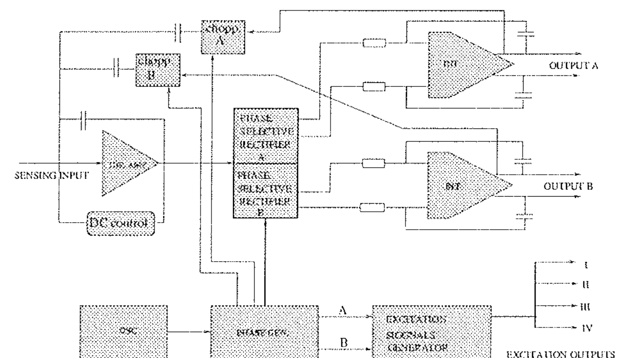

Fig. 2: Basic electrical shematic of test chip

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INTEGRATED OPTICAL POSITION MICROSYSTEM WITH PROGRAMMABLE RESOLUTION

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Key words: microelectronics, position meters, programmable interpolators, programmable resolution, optoelectronics, integrated optoelectronics, integrated microsystems, differential drivers, optical sensors, OMS, Optical MicroSystems, AFE, Analog Front End

Abstract: The paper describes an integrated optical microsystem for motion detection, which combines the following: an analog programmable interpolator, digital drivers, a differential analog front-end, signal monitoring outputs, error handling and an array of light-sensitive cells with a micro-strip raster.

The interpolator outputs are generated from orthogonal sinusoidal signals coming from illuminated integrated photo-sensors. The optical microsystem is composed of an autocalibration on an analog front-end to get proper interpolating signals. It consists of three symmetrical analog channels: *sine*, *cosine* and reference signal channel. Each channel combines a current-gain stage operating as a fully differential current-to-voltage converter and thus guarantees the best phase relation between the ordinary and the inverted analog signals. Integrated analog buffers are used for monitoring the processed analog signals. The signal bandwidth of the analog channels is designed to be large enough so as not to limit the system response and therefore maximize the useful signal range.

An ASIC was fabricated using standard in-house CMOS technology and three different types of photo-diodes having an area of 600um x 1500um each was integrated. The P+P/N substrate diode's responsivity of 0.52A/W and the 12uA typical diode current was the best result that was achieved by the motion detection system. Programmed interpolating factors of 4, 20 and 40 were realized (1, 2, 5, 10 in standard industrial notation Fig. 10).

Vezje za merjenje pozicije z integriranim optičnim senzorjem in nastavljivo ločljivostjo

Ključne besede: mikroelektronika, merilniki položaja, interpolatorji programljivi, ločljivost programljiva, optoelektronika, optoelektronika integrirana, mikrosistemi integrirani, gonilniki diferencialni, senzorji optični, OMS mikrosistemi optični, AFE analogni del čelni

Izvleček: Opisan integrirani merilni sistem sestavljajo programljiv A/D pretvornik, diferencialni vhodni ojačevalniki, svetlobno občutljivo polje senzorjev, testne strukture, digitalni procesor, detektor napak ter mikroraster.

Analogni signal (*sinusni* in *cosinusni* tokovni signal iz fotodiod) se pretvarja v napetostni signal ter ustrezno ojači. Vgrajena je kalibracija napetosti ničenja ter korekcija faze med vhodnimi kanali. Le-ti so trije: sinusni, kosinusni ter referenčni kanal. Procesiranje analognih signalov je diferenčno, kar zagotavlja visok rejekcijski faktor na spremembe napajalne napetosti ter na motnje. Vezje ima vgrajeno detekcijo faznih nepravilnosti izhodnih pravokotnih signalov A in B ter pozicije referenčnega impulza. Za kalibracijo in opazovanje so dodani hitri operacijski ojačevalniki.

Integrirano vezje je bilo proizvedeno v laboratoriju za mikroelektroniko na Fakulteti za elektrotehniko v Ljubljani, v standardni tehnologiji CMOS z uporabo dodatne maske za eleminacijo ekstremov v spektralnem odzivu integriranih P+P/N optičnih sensorjev, katerih največja izmerjena občutljivost je 0.52A/W pri valovni dolžini 820nm. Vezje ima tudi nastavljive interpolacijske faktorje: 1, 4, 10 in 40.

1. Introduction

The integrated optical microsystem (OMS) described here is an interpolating system combined with a solid-state optical sensor. The crucial requirements of an OMS are: photosensitivity, responsivity, dark current, dynamic range, and spectral response /3/. There are a number of ways to achieve optical-position detection. One method is to use a linear photodiode array to produce a signal that is a linear function of position. When the position has to be expressed incremental-digitally or absolute-digitally, the generation of orthogonal sine-wave signals is required /1/, and it is advisable to use a coded optical wheel or a linear glass scale and glass reticle (Fig.8 and Fig.9). To achieve high resolution and accuracy, the large dynamic range and wide bandwidth of an optical analog front end (OAFE) are required. In order to be able to use a large interpolating factor up to 1000, the *sine*-wave signals have to be generated very precisely. Therefore, the precision of the coded glass, the distance from the glass to diode's surface, the IR light source and the light cross-talk between the integrated diodes are most important. If we have accurate analog signals from the OAFE, the remaining difficulties related to high interpolating factors come from the analog-to-digital conversion (interpolator). To guarantee a motion measurement that is fast, the response of the overall system should also be fast.

The system presented in this paper acquires analog signals from four regular integrated diodes that are 200µm apart and a single reference diode. The optical part of the system is integrated with the electronic part for signal processing in the silicon area without peripheral structures. Integrated diodes in the micro-raster structure help to reduce the opto-electronic response time and can be used as an integrated glass reticle, -the first time this has been used in a completely integrated system. The AFE is capable of operating in either current or voltage mode.

An integrated programmable interpolator combines specially designed comparators and a single-level-delay *EXOR*

array. The interpolator exhibits high noise immunity and is highly insensitive to amplitude and the offset difference between channels. It converts the gained and converted, orthogonal photo-current signals to an orthogonal pulses sequence named A track and B track, and a reference-position signal that is counted in an external counter and gives an incremental linear position with a different resolution. The programmed interpolating factors of 1, 4, 20, and 40 are realized. The optical microsystem also combines a self-test feature and an error detection function, which is very important for dustrial use.

The dimensions in the stripped junction's area were chosen to achieve the minimum time constant and, therefore, a fast response. This guarantees a higher speed of position detection and reduces the higher harmonics. There are numerous important electrical and electro-optical parameters that we followed and measured.

Different junctions are available in standard p-well CMOS technology. We looked for the best sensitivity, the lowest possible diode capacitance, the minimum parasitic diode current and the proper reverse-current versus temperature behavior. The diodes inherent electrical and optical behaviors are well known and it was not necessary to evaluate them /1/. The following properties of the integrated systems were measured: the diode's capacitance versus reverse operating voltage, the reverse current versus temperature and the spectral response of the integrated light sensors.

The opto-electronic properties were first measured without any change of the protective nitride and the field oxide thickness. The ASIC were then fabricated again with diodes nitride and oxide modification to remove the peaks in the spectral response. The results of the measurements are reported along with the best selected junction structure. The OMS structure and the overall system is described in the paper as well as the system's remaining external components. The integrated micro-optics, together with the mixed analog/digital electronics, results in a useful miniaturization (Fig. 10), that made it easier to test and improved the reliability of the system for industrial use /4/.

2. Circuit architecture

A. Opto-electronic OAFE and calibration

A simplified block diagram of the system is shown in Fig.1. It consists of the AFE, an optoarray, analog output buffers, an analog/digital programmable interpolator and a digital output structure.

The analog channel, as part of the AFE, is shown in Fig. 2. An orthogonal sinusoidal current or voltage enters the gain stage where the analog signal ground is used as an output balance signal. In current-mode operation the signal-ground also stabilizes the input operating point (i.e. diodes). This means that the variations in the reverse-operating diode's

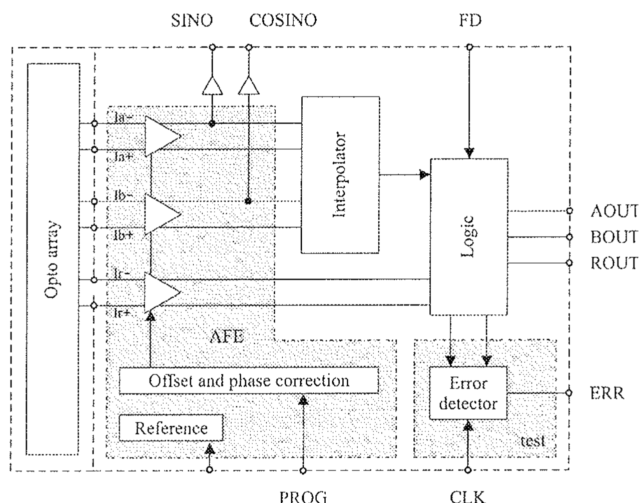

Figure 1: *Block diagram of the integrated OMS microsystem*

voltage are a few milivolts, with a maximum signal current of 20µA (with the diode illuminated).

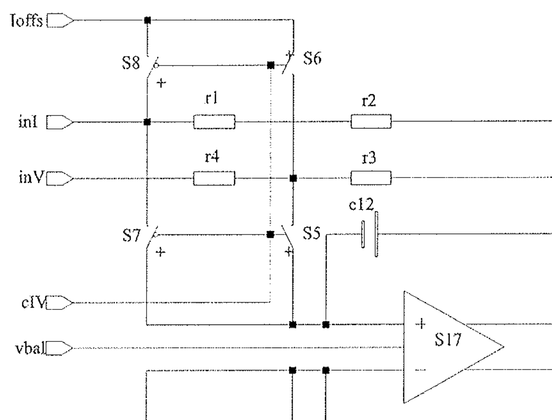

Figure 2: *The AFE signal-channel half of the symmetrically-balanced stage. The current input inI or the voltage input inV is selected by the cIV signal. The Ioffs input current is selected for the offset correction of the AFE. Integrated diodes are connected from inI inputs to the substrate (VDD) in reverse polarity. Each channel has two photodiodes.*

Measuring the phase shift between the two AFE channels provides us with the signal for phase compensation. A part of a *sine* signal is used as a phase correction for the *cosine* signal. This principle has no effect on the signals' amplitude. The small *sine* signal is converted into a differential current by means of temperature tracking with current gain and is fed back to the input terminal of the *cosine* gain stage.

The phase adjustment is digital with a minimum step size of 0.2 angle deg. Therefore the principle looks like an aligning process between two analog channels. It is important

to note that the phase-aligning process aligns the signal phases to 90 deg. This means that aligning two orthogonal signal phases may include the overall system, i.e. it may include the external-mechanical components, too. Fig.3 shows a simplified schematic of the *cosine* phase-correction circuit.

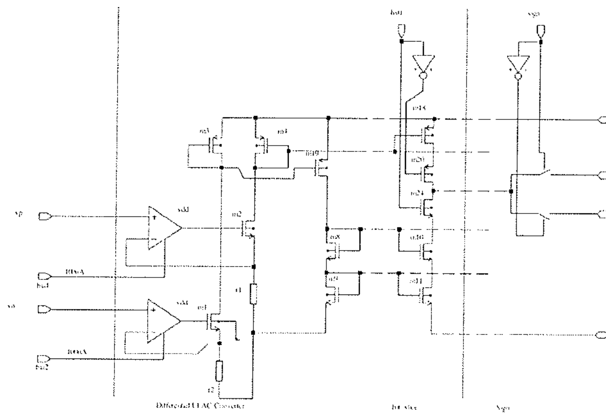

Figure 3: *Detail from the phase-correction circuit*

A very similar adjustment is used for the system-offset correction. As the analog signal-ground is used for balancing the signals going to the interpolator inputs, a part of the constant DC signal is converted into a current and feeds back into the virtual ground of the gain stage. Therefore, one analog channel is selected to be the reference, and the second channel's offset is adjusted to the first channel's offset. This is sufficient for proper operation of the analog/digital interpolator. The interpolator handles only four sinusoidal signals and does not require a signal-ground.

The corrected phase and offset stability over temperature is guaranteed by a proper design technique. The signal voltage is converted into a phase or offset current-signal error via a polysilicon resistor, which is matched with the gain-setting resistor in the AFE, where the error signal is converted back into phase or offset voltage information.

B. Interpolator

The programmable interpolator combines a novel design of comparators, a resistor chain and an *EXOR* array to process the comparators' output signals into two orthogonal pulses: A and B. Comparators have built-in hysteresis in such a way that their inputs remain high ohmic. The amplitude of the hysteresis tracks the photodiode signal on AFE output with temperature and process.

The A and B signals are generated using a 4-transistor *EXOR* logic to generate a single-level delay function and include the N-channel device of a multiple input *NOR* gate. Instead of P-channels, a simple current source is used. Because there is just one event at a time a larger DC current can be used. With more than 200 comparators and a 50μA pull-up current, the logic converter's overall delay of 1nsec is achieved. Fig. 5 shows a detail from the schematic.

C. Error detection and testing

The photosensitive elements act as good protection diodes to the substrate due to the large diode area. As a result, extra protection is not needed when the diode's anode (amplifier inputs) is routed to the PAD. External access is useful to inject the signal current for test purposes. When operating in voltage mode an externally generated differential voltage is required. It is also enough to generate a single-ended input signal and to connect one input to the generated voltage signal-ground (buffered output). In current mode, one input terminal may stay unconnected. Using a single driving input signal the AFE output is reduced by 6dB. The AFE output voltage can be monitored on external pins via integrated analog output buffers.

The sequence of the generated orthogonal pulses named A track and B track can be monitored at the output and verified in terms of position in two different ways.

The first one requires synchronization between the analog input signal and the sampling square wave, which samples the A and B tracks. The sampled tracks can trigger the counter, the contents of which can be verified at the end of *sine* wave period. For a low input sinusoidal frequency this test procedure is simply realizable in the LabVIEW environment.

The second principle is more or less completely integrated. All that is need is an external clock, which, for precise testing, needs to be synchronized with the sinusoidal frequency and requires "n" periods per one *sine* wave period. Fig.4 shows the measuring principle and the appropriate period relations with respect to the division factor and the absolute interpolation error for n=4. The resolution of the error detection is increased when a larger "n" is used. Two principles are used: error is not detected if there is a clock edge inside two tracks' edges (Fig.4a) or at least one positive and one negative clock edge is required between tracks' edges (Fig.4b).

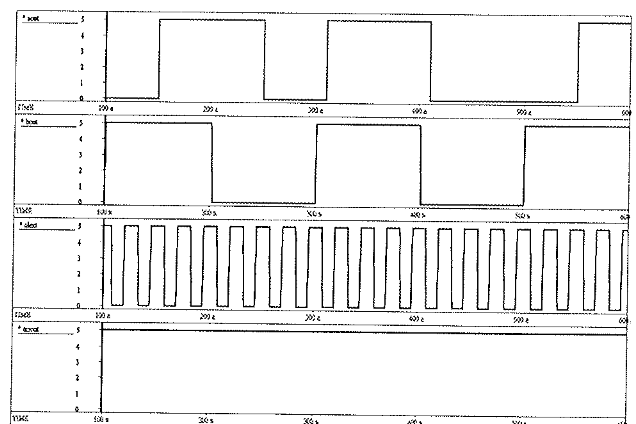

Figure 4a: *Error function: principle of operation. External clock frequency is f_ext>4FD.f_sin. Error is not detected if there is clock edge between track A and track B.*

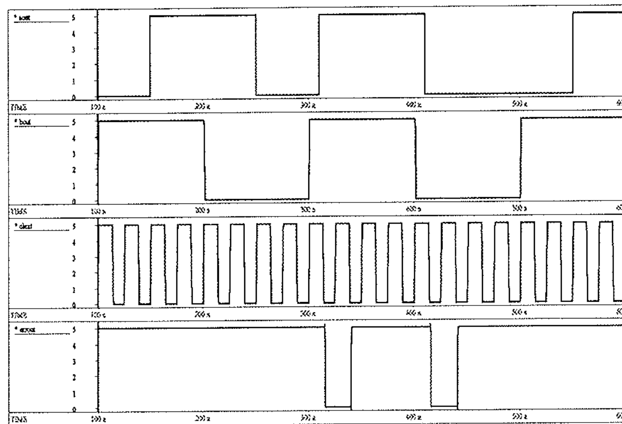

Figure 4b: *Error detected (errout = LOW), edge separation is less than a half clock period.*

3. Considerations for a large dynamic range

The integrated system dynamics is limited by a number of factors. The first important limitation comes from an integrated optical array related to its size, resistivity, capacitance and noise performances. The second limitation is imposed by the noise characteristic of the analog front-end channels. Let us first consider the integrated electronics, where the current mode is active.

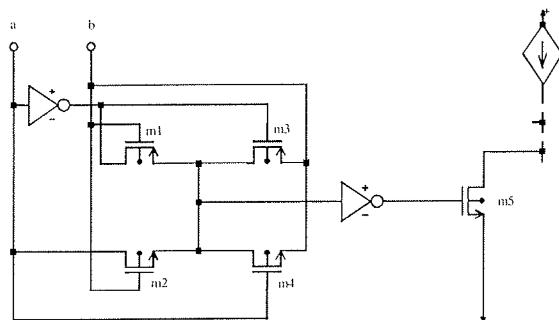

Figure 5: *EXnOR logic*

The feedback resistor has a nominal value of 100kΩ and is used as a current-to-voltage conversion element. It largely determines noise and bandwidth as well as gain. Resistor acts as an important wide-band noise source (4$\sqrt{R}$) in nV/$\sqrt{Hz}$, and appears directly at the output of the current-to-voltage converter without amplification (where R is the resistivity in kΩ). The fully differential amplifier in a typical application (e.g. AFE) including a biasing circuit has the voltage noise shown in fig.6. Most of the noise power is concentrated in the frequency band at low frequency and where the gain peaking occurs.

If we choose only the 100kHz bandwidth, the 50pF diode capacitance and the $1/g_m$=100kΩ, than the *rms* spot noise voltage of the AFE is 20µV. To achieve a 9-bit resolution of the AFE channel, the minimum output voltage on the AFE

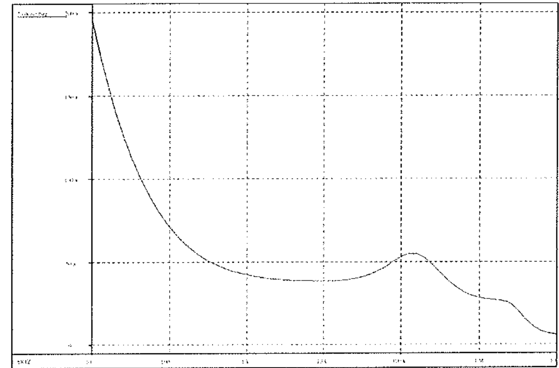

Figure 6: *Output noise voltage on the AFE channel*

channel should be 0,1024V_p, which requires at least a 1,024µA_p photocurrent. This means the *rms* photodiode current noise level must be below 2nA. For the above calculation, only the electronic noise was counted. But there is also an edge effect from the coded plate, a light modulation effect, light bends on the patterns' edges of the measuring plate (small hole dimensions), a non-constant dark current, a leakage current, etc. Taking into account all these effects, a margin of 4 is estimated to be sufficient. To calculate the minimum comparator's hysteresis and therefore the minimum required photodiode signal current, the expected comparator's offset voltage has to be considered, too. For an interpolation factor of 40, an additional margin is not required and a 4uA_p photodiode current is sufficient.

4. Opto-electronic system characteristics

The photodiode operating reverse voltage is always mid supply level, that increases the diode capacitance and slightly reduces the diode noise. Separate optical measurements were done using reverse diode voltage of 5V (P+P/N) /3/.

- Supply voltage: 3V (min), 5V (nom)
- Supply current: 6mA
- Photodiode current: 1mA (min), 20mA (max)
- Photodiode responsivity 0.52A/W
- Photodiode peak wavelength 820nm
- Photodiode capacity @ -5V 19pF
- Photodiode Q.E. 80%
- Photodiode reverse current @-5V 200pA
- Operating frequency range: DC to 200kHz
- S/N ratio: 62dB (AFE)
- Common-mode signal rejection: -64dB
- Resolution: 9 bit(AFE)
- Technology: 2µm, p-well CMOS
- Programmable division factors: 2, 4, 8, 20, 40
- Balance voltage internally generated requires external capacitor, min 100nF.

- Max internal delay: 20nsec
- Absolute interpolator error: below 0.5°

5. OAFE transimpedance channel characteristics

- Fully differential topology
- Low noise
- Short recovery time
- Large dynamic range
- Operating point control
- Upper corner frequency independent on optosensor capacitance
- Offset regulation
- Phase control
- Programmable gain
- DC and DARK current compensation

6. Layout constrains

The geometry of the combined *ASIC* has the *PAD*s for the external connection placed away from the optodevices' area. Fig.7 shows the microphotograph of the chip. Only test pads may be placed close to or in the illuminated area. This separation is also good for better positioning of the external mask patterns.

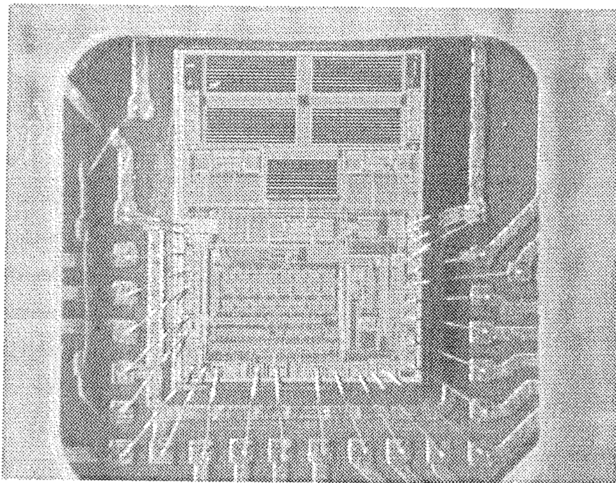

Figure 7: *ASIC die including opto-array*

The photodiodes' structure that we used was a P/N diode (p-well/n-substrate). P+ diffusion strips with narrow *metal1* and *metal2* aluminum layers were also used to reduce the surface resistivity of the diode. The same was done for better substrate conductivity. P+ diffusion therefore reduces the response time, while the sensitivity versus wavelength remains unchanged (P+ mostly covered by aluminum). The stripped diodes (*1500μm long*) and the movement of the external mask have the same orientation. This means that all stripped diodes are illuminated simultaneously and the generated current is an integral over *dx* along the diodes.

7. Conclusions

The proposed system needs to be optimized on high common mode rejection on input. Due to P+P/N substrate diodes and conversion to differential output signal, the effective generated signal is reduced by 6dB.

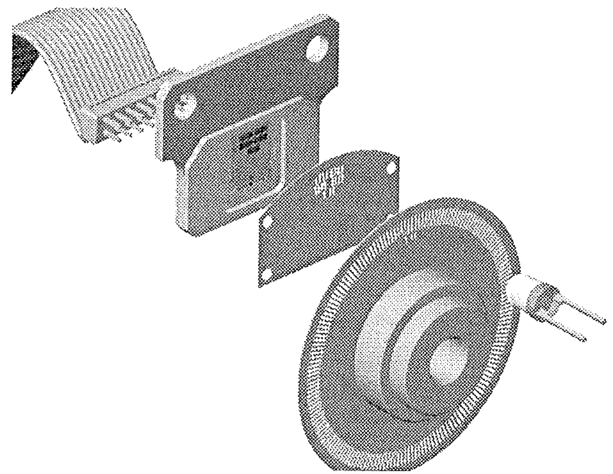

Figure 8: *Opto-ASIC in rotary-incremental application*

Optical shielding is used between the diodes (polysilicon, metal layers). Because there are no bonds on the optical area the minimum distance (*d*) of the monitoring pattern plate (glass) to the *ASIC* surface can be expressed as:

$d \leq \frac{1}{2} \cdot P/\lambda$ where P is the period size (pattern to pattern) and λ is the wavelength (820nm).

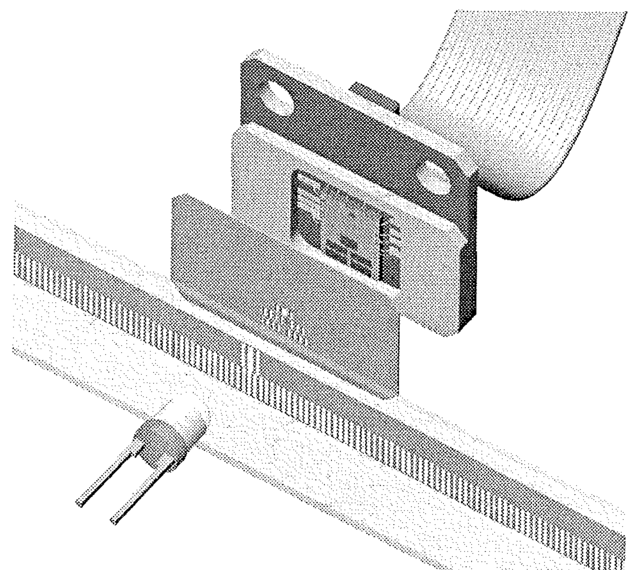

Figure 9: *Opto-ASIC in linear-incremental-position application*

The test using a microstrip raster formed by both aluminum layers was expected to be used instead of a receiving coded plate. The advantages of the integrated diodes and the proposed PAD position are that the distance (d) of the patterned glass from the *ASIC* surface can be reduced almost to zero. Using patterned glass above the die overrides the integrated strips, which makes the system more flexible.

The next important result is the noise figure for the overall integrated electro-optical system. This was measured with different illumination (LED diodes). If this noise is evaluated and calculated as a noise current to the diode terminals, the possible minimum illumination can be found. This value is close to the expected 3nA peak on input. The larger measured value is due to the noise contribution of the analog output buffer. The measured results printed in chapter IV showed behavior of the integrated system and of the opto-elements separately.

The temperature characteristics of the photoeffect are not so important as the dark current of the P+P/N integrated diodes /3/. This current increases rapidly with temperature. In our case, the voltage on the diode is not close to zero and therefore the increasing leakage with temperature is not negligible. A possible solution could be a continuous offset cancellation using a *dummy DARK* optochannel. As can be clearly seen from Fig.2, the *DARK* and the *common-mode DC* components are canceled out by means of a floating input common-mode level. All the diodes need to be matched. Along with the phase matching this is a big advantage of the designed analog front end (AFE).

Figure 10: *Opto-ASIC microsystem and application*

All the designed ASICs are used in RLS incremental linear and rotary encoders (Fig. 10). They are available also as modular COB component.

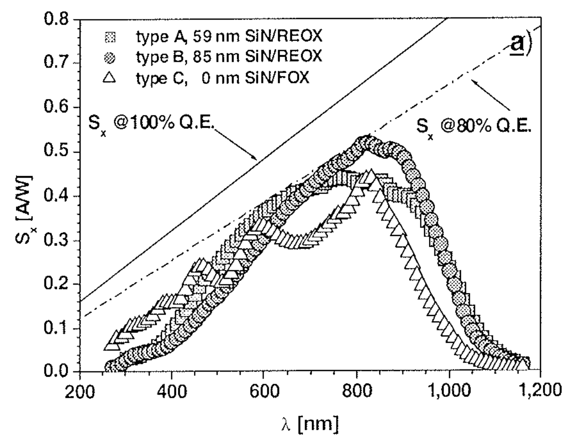

Figure 11: *Measured spectral response of the diodes*

Only one additional mask for the antireflection coating of 85nm of the Si_3N_4 with refracted index of 1.98-2.02 was finally added to the standard CMOS process. The size of the integrated diode is *600μm x 1500μm* with a peak responsivity of *0.52A/W* at *820nm* (Fig. 11).

Acknowledgements

The author would like to thank Janez Novak, director of the *RLS* company, for useful suggestions, the engineers at *RLS* for doing the *ASIC* test in applications and to Marijan Maček for diodes characterization and processing.

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FUNCTIONALITY TEST FOR MAGNETIC ANGULAR POSITIONING INTEGRATED CIRCUIT

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Key words: angle measuring, integrated hall sensors, magnetic sensors, HALL sensor array, integrated coils, semiconductors, microelectronics, silicon wafers, magnetic fields, ASIC, Application Specific Integrated Circuits, functionality test, testing devices, wafer probers, automatic testing

Abstract: A description of the low cost, fully automated on silicon wafer testing procedure of the magnetic angular positioning integrated sensor is presented. The problem to be solved is, how to implement repetitive and rotating magnetic field around the silicon wafer. This must be done while testing integrated circuits on the wafer prober. Such magnetic field is needed for proper measurements of the integrated hall sensor array functionality.

Testiranje integriranega magnetnega senzorja za merjenje kota

Ključne besede: merjenje kotov, HALL senzorji integrirani, senzorji magnetni, polje HALL senzorjev, tuljave integrirane, polprevodniki, mikroelektronika, rezine silicijeve, polja magnetna, ASIC vezja integrirana za aplikacije specifične, preskušanje funkcionalnosti, naprave preskusne, naprave preskusne za rezine silicijeve, preskušanje avtomatsko

Izvleček: Predstavljen je način avtomatskega testiranja silicijevih rezin z integriranim magnetnim senzorjem za merjenje kota. Potrebno je bilo rešiti problem, kako zagotoviti ponavljajoče in vrteče se magnetno polje okoli silicijeve rezine med testiranjem na testni napravi. Takšno magnetno polje je namreč potrebno za meritev integriranega polja Hall-ovih senzorjev.

Introduction

Positioning systems are very common devices in modern machinery. There is strong demand for inexpensive, accurate magnetic angular positioning device - monolithic CMOS circuit. Such devices can be used for example in automotive industry for reliable throttle position sensor or drive by wire implementations. Cost of such sensors can be further reduced by fast, on silicon wafer functionality testing. This enables us to skip expensive die bonding, wiring and packaging of bad dices.

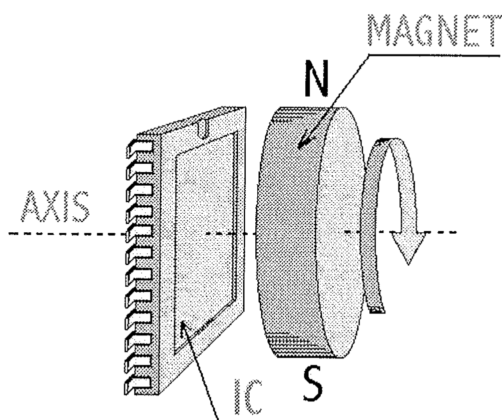

Figure 1. *Rotating magnet above the chip*

Description of the magnetic angular positioning integrated circuit

The magnetic angular positioning circuit determines the absolute angular position of the magnet rotating above the chip. Such magnet produces a rotational magnetic field as shown in figure 1. This can be done with an array of Hall magnetic sensors, positioned around the circle with the same center as the axis of the rotating magnet. Outputs of these sensors are connected to two adders, whose output defines signals S (1) and C (2). The signals S and C are orthogonal and have function of sinα and cosα, where α is actual angle of the magnet rotation. Such array of Hall magnetic sensors is shown on figure 2.

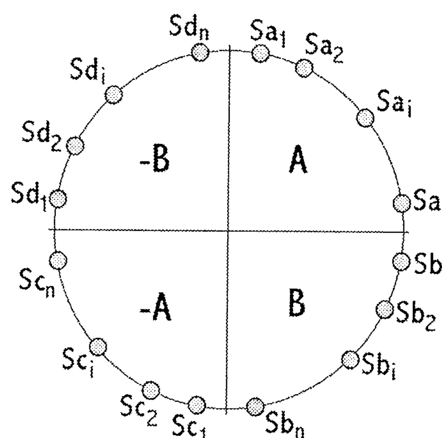

Figure 2. *Structure of the sensors*

$$S=\sum_{i=1}^{n} Sa_i+\sum_{i=1}^{n} Sb_i-\sum_{i=1}^{n} Sc_i-\sum_{i=1}^{n} Sd_i \qquad (1)$$

$$C=-\sum_{i=1}^{n} Sa_i+\sum_{i=1}^{n} Sb_i+\sum_{i=1}^{n} Sc_i-\sum_{i=1}^{n} Sd_i \qquad (2)$$

As we mentioned before, the problem to be solved is, how to test the chip without implementing the mechanical environment as shown on figure 1. Such environment is almost impossible to realize on the silicon wafer test level.

Implementation of the functionality test

Instead of building a special mechanism for fixing and rotating the magnet above the chip, it is possible to generate magnetic field with on-chip integrated coils as shown on figure 3. Here we can see a layout of the magnetic Hall sensor in the middle of the coil with six turns. For that purpose two metal layers are used.

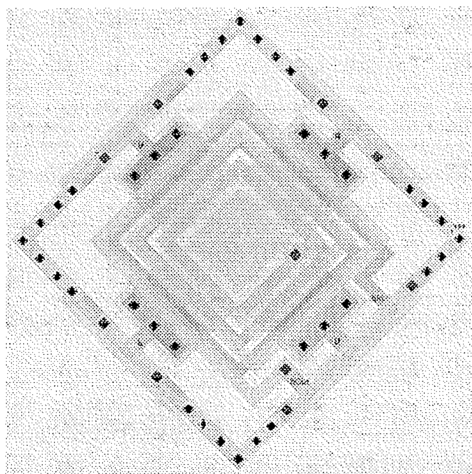

Figure 3. *Layout of the integrated coil*

Figure 4 demonstrates the structure of all sensors with coil. All coil turns are in the same direction. We can also see, how the coils are connected together. N coils have one input and one output terminal.

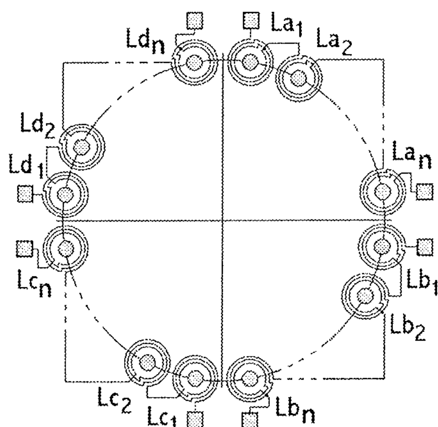

Figure 4. *Structure of the integrated coils*

As we can see on figure 4, it is also possible to reverse the sign of magnetic field by reversing the coil terminals. When applying the same current I_A through the sensor coils La_i and through reversed coils Lc_i the signal **S** corresponds to $+2nI_A$, due to the current I_A and when applying the same current I_B through the coils Lb_i and through reversed coils Ld_i, the signal **C** corresponds to $+2nI_B$, due to the current I_B.

However, according to (1) and (2) the contribution of current I_B to signal **S** is $+2nI_B$ and the contribution of current I_A to signal **C** is $-2nI_A$. Therefore we have:

$$S=2nI_A+2nI_B \qquad (3)$$

$$C=2nI_B-2nI_A \qquad (4)$$

This is shown on figure 2. If we use current **A** equal to $I_A=I_A\sin\omega t$ and current **B** equal to $I_B=I_B\cos\omega t$ signals **S** and **C** become orthogonal functions with the amplitude:

$$\sqrt[2]{(2nI_A)^2+(2nI_B)^2} \qquad (5)$$

This shows, that properly controlled, on chip integrated coils can actually replace the rotating magnet while testing the functionality of the sensors on the magnetic angular positioning integrated circuit.

In our test environment we have wafer prober, semiconductor parametric test system HP-4062B with switching matrix, multifunction card DAQ-1200 with analog output capability from National Instruments and two personal computers. One of them is equipped with HP-IB (Hewlett Packard Interface Bus) card. This card is used to control wafer prober and Hewlett-Packard test system. Figure 5 represents our test configuration.

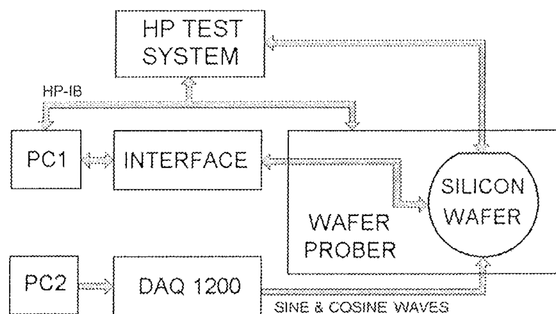

Figure 5. *Test environment*

Conclusion

By adopting and properly controlling on chip integrated coils, we transformed mechanical rotation α into measurable harmonic function $j\omega$ of selected integrated coil currents. The equivalence between actual signal from the rotating magnet and the signal generated from the properly controlled integrated coils has been also determined.

Figure 6 presents the photograph of the integrated circuit for angular positioning. On this picture we can see, how

magnetic sensors with amplifiers are distributed on the circle within the chip surface.

Diagram on figure 7 presents an example of measuring results compared with reference angular positioning device. We can easily determine that the absolute error is about ±1bit. Since measured chip has nine bits for absolute angular positioning, it is capable to determine 512 different angular positions. In this case absolute error of ±1bit means actual error of ±0.7 angular degree.

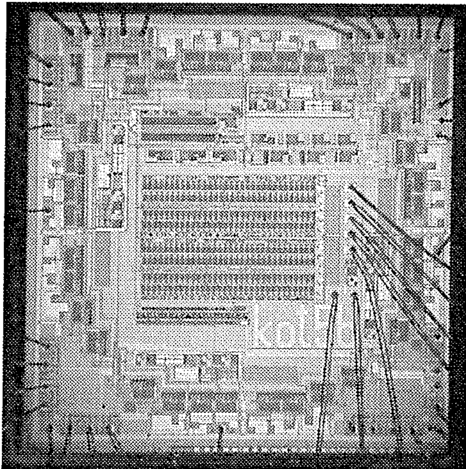

Figure 6. *Integrated circuit for magnetic angular positioning*

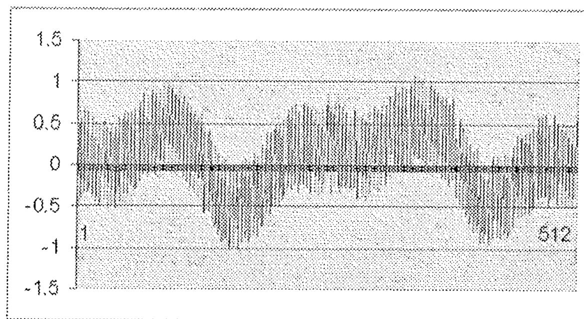

Figure 7. *Diagram for absolute error while rotating 360 degrees.*

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KONFERENCA MIDEM 2001 - POROČILO
CONFERENCE MIDEM 2001 - REPORT

37th International Conference on Microelectronics, Devices and Materials - MIDEM 2001

with the WORKSHOP on

OPTOELECTRONIC DEVICES AND APPLICATIONS

10.10.2001 - 12.10.2001
HOTEL ZLATOROG, BOHINJ

REPORT

37th International Conference on Microelectronics, Devices and Materials, MIDEM 2001, continued the tradition of annual international conferences organised by MIDEM, Society for Microelectronics, Devices and Materials, Ljubljana, Slovenia. These conferences have always involved a large number of Slovene and foreign experts working in these fields as well as attracted distinguished guest speakers. Once a year our scientists have the opportunity to present their activities and research results to domestic audience and to discuss news, trends and problems related to their fields of work with colleagues from abroad.

This year 43 papers and eight invited presentations in five sessions during three days, from Wednesday to Friday, were presented. On 345 pages, Proceedings of the MIDEM 2001 conference contain all invited, as well as 43 regular papers covering up-to-date topics on integrated circuits; device physics and modelling; optoelectronic devices and applications; thick and thin films and ceramics, metals and composites.

Workshops were added to the programme of the MIDEM Conferences in 1998. The workshops are dedicated each year to the selected specific topic.

For the year 2001 we organised **Workshop on Optoelectronic Devices and Applications**. Selected topics associated with advanced aspects within lasers, light emitting devices, thin-film transistors, optical fiber systems, nonlinear optical devices, etc. were presented, covering the basic physical principles, as well as actual and possible applications of these optelectronic devices and systems. Seven invited speakers presented the chosen topic from different aspects, thus offering the audience valuable information.

The work of the Conference was divided into five sessions: Integrated Circuits; Optoelectronics; Device Physics and Modelling; Thick and Thin Films; and Ceramics, Metals and Composites.

This year, distinguished guest speakers presented the following invited papers:

Prof.Dr.Radivoje S.Popović
EPFL-Swiss Federal Institute of Technology Lausanne, Switzerland
Christian Schott and Robert Racz
SENTRON AG, Zug, Switzerland
Integrated Hall Sensor/Flux Concentrator Microsystems

Prof. Dr. Martin Stutzmann
Walter Schottky Institut, Technische Universität München, Germany
The Status of GaN-based LEDs and Laser Diodes

Prof. Dr. R. E. I. Schropp, B. Stannowski, J.K. Rath
Debye Institute, Physics of Devices, Utrecht University, The Netherlands
Hot Wire Deposited Materials for Thin Film Transistors

Prof.Dr.Gil Rosenman, P. Urenski
Department of Electrical Engineering-Physical Electronics, Tel Aviv University, Israel
Tayloring Ferroelectric Domain Configurations for Nonlinear Optical Devices

Dr. Christian Hanke
Corporate Research Photonics, Infineon Technologies, Munich, Germany
High Power Semiconductor Laser Diodes

Dr. Helmut Stiebig, D. Knipp, H. Wagner
Institut für Photovoltaik, Forschungszentrum Jülich, Germany
Color Aliasing Free Detectors

Dr. Matjaž Vidmar
Faculty of Electrical Engineering, University of Ljubljana, Slovenia
Optical-fiber Communications: Components and Systems

Dr. Gvido Bratina, R. Hudej
Nova Gorica Polytechnic, Slovenia
Organic Semiconductors as Candidates for Advanced Optoelectronic Devices

Some statistical data:

Number of participants: 65, 14 from abroad

Number of published papers in the Proceedings: 51, 15 from abroad

Number of presented papers: 51, 15 from abroad

Participating countries: Slovenia, Italy, Poland, Slovakia, Switzerland, Germany, Israel, Hungary, The Netherlands and Croatia.

For MIDEM 2001 Programme Committee
F.Smole, M.Topič and I.Šorli

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We are a non-profitable institution established by interested production enterprises and research institutions of Slovenia in conformance with regulations and laws prescribed by Ministry of Science and Technology, Republic of Slovenia, **with the aim to better use existing knowledge and equipment and create new knowledge in joint operation - vertical and horizontal cooperation in the field of electrical and electronic components and to assure the participants competitive advantages in joint and coordinated work.**

The cooperation between members is not new. It started decades ago on bilateral basis or while the enterprises were members of big industrial system. Now they realized that by help of technology center, the flow and level of information and cooperation can be higher.

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TC has established **The research group for materials, electronic components and technologies**, where researchers from various production enterprises and research institutions work together on the projects of common interest.

In their strategic plans **the members allocate considerable funds for innovation of the products**- to adopt them to the specific requirements of the customers and develop new products, technologies and equipment. Use of synergy effects makes the realization of the goals easier.

The result of cooperation can be seen in the business results of participants. Researchers publish their results on various research work presentations and conferences. Majority of researchers are members of Professional Society for Microelectronics, Electronic Components and materials - MIDEM and publish their results in the professional-scientific publication Informacije MIDEM.

First half year of activities (second half-year of 2000)

Exchange of information about, new events, national and international tenders, knowledge needs and availability.

All the members receive Obvestila S-xy (=Information) in which their attention is directed to new events and opportunities. They are informed of the following meetings of the group and get the minutes of them.

Seven presentations in R&D departments and laboratories of our members have been done to co-members. A lot of information have been exchanged and new cooperation opportunities have been discovered. The existing knowledge can be used for new purposes after small additional research.

Many interested thematic of common interest have been discussed at the meetings and local experts have been invited to answer the questions. Besides the technology problems we discussed the Project proposals preparation, Conditions to present proposals for 5-th frame program, Access to the information bases, Quality management and testing, products and systems assessment and certification, measurements and instrumentation calibration, possibilities of getting venture capital for new investments, Possibilities of joint presentation of new research results, joint participation on fairs, etc.

Presentation of project proposals for national and international R&D project subsidy

In year 2000 ten of our members presented their project proposals (23 in total) to Ministry of Science and Technology. Sixteen projects were awarded subsidy by the ministry for the next two years.

The policy of Zavod TC SEMTO is to help to its members at preparation of proposals. In accordance with the rules and procedure the industrial enterprises are the project proposers. Enterprises that have their oven registered R&D departments are also the R&D performers. Those, whose

development departments are not registered, delegate their researchers to work in mixed groups in the frame of Zavod TC SEMTO, who acts in these cases as R&D performer.

In 2000 we prepared two Exploratory award proposals sent to CORDIS to be included in 5-th frame program and to be followed by CRAFT proposals.

Tradition of electronic components and materials research and development and production in Slovenia

The development and production of electronic components in Slovenia started after the second world war, when the development of electronic was considered as strategic goal of Yugoslavia. The University of Ljubljana produced big number of good trained engineers who were stimulated to follow the most up to date development in the world.

Yugoslav market was closed and the foreign currency scarce. The local marked required all types of products. As the Yugoslav marked was too small to enable series that would justify automation and enable competitive prices, the sales and production were oriented to European markets and the production has been enlarged. The products had to correspond to valid standards and specific customers' wishes. The quality was essential. Contacts with customers research groups were established.

Iskra group within Slovenia became the main Yugoslav electronic components producer. Its products were well accepted in the European market. Mainly passive components were produced (film and wire resistors, potentiometers, nonlinear resistors, ceramic, foil and electrolytic capacitors, technical ceramic, ferrites, strip wound cores and inductive components, filters, over-voltage and EMI protection, Si diodes, relays, switches, printed circuits boards, antennas, batteries, automotive components etc.).

When the marked was opened after separation from Yugoslavia, the Slovene components producers were prepared for the open competition. The production program has been revised and narrowed. The R&D has been intensified and oriented to some fields. Slovene components producers are important, well accepted European producers and partners to many European and American groups.

Electronics and material science is well established in Slovene universities and R&D institutes, who are cooperating with industry in joint development projects and providing the needed R&D specialists.

Igor Pompe

Umrl je prof.dr.Janez Dobeic, častni predsednik društva MIDEM

V 87.letu starosti je umrl prof.dr.Janez Dobeic, častni predsednik društva MIDEM in dolgoletni profesor na Fakulteti za elektrotehniko v Ljubljani.

Objavljamo poslovilni govor prof.dr.Tadeja Bajda, dekana Fakultete za Elektrotehniko:

Danes se poslavljamo od našega kolega profesorja Janeza Dobeica. Bil je vsestranski strokovnjak, odličen pedagog in ustvarjalen umetnik.

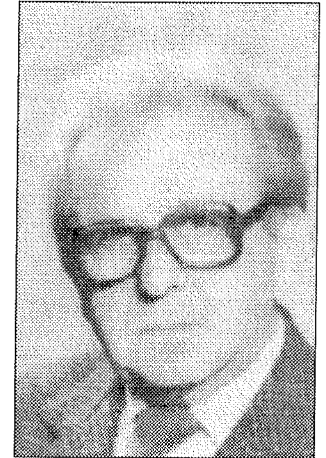
Rodil se je v Kranju leta 1914, maturiral leta 1932 na Poljanski gimnaziji v Ljubljani in leta 1940 diplomiral na elektrotehniškem oddelku tedanje Tehniške fakultete na Univerzi v Ljubljani. O njegovem vizionarstvu priča že diplomsko delo z naslovom »Motoelevator«. Pred več kot šestdeset leti je podal teoretično in praktično zamisel v prostoru lebdeče lokomotive brez nosilnih in pogonskih koles.

Med vojno se je vključil v delovanje OF in bil zaprt v zloglasnih Begunjah.

Kmalu po vojni je bil imenovan za asistenta na oddelku za elektrotehniko. Zdi se, da je bila štipendija francoske vlade, ki ga je popeljala na izpopolnjevanje na pariško Sorbonno, tisti pomembni življenski vzgib, ki je profesorja Dobeica za vselej zaznamoval kot elektrotehnologa. Od tedaj je bil razpet med dva pola. Po eni strani je snoval nove in nove izboljšave in izume za potrebe slovenske industrije, po drugi strani pa se je izdatno posvečal pedagoškemu delu.

Zasnoval je domač način izdelave tiskanih vezij, izboljšal postopek za naparevanje silicijevega oksida in razvil steklene skale za prve radijske sprejemnike. Še bi lahko našteval njegove izvirne zamisli, vendar naj na tem mestu omenim samo še en, posebno imeniten dosežek. Profesor Dobeic je skonstruiral nekaj ton težko makrovezje za potrebe železarne Štore.

Kot pedagog je predvsem ustvaril predmet Elektrotehnologija. Odlično pripravljene vsebine predmeta so po profesorju Dobeicu povzeli še na petih elektrotehniških fakultetah tedanje Jugoslavije. Predaval je tudi na Fakulteti za gradbeništvo, na vojni akademiji v Šentvidu, ter na univerzah v Mariboru in Splitu.



Bil je prodekan Fakultete za elektrotehniko in dolga leta predstojnik katedre za Uporabo električne energije in tehnologijo. Bil je častni član več nacionalnih in mednarodnih zvez in društev in večkrat je bil za svoje izvirno delo odlikovan.

Profesor Dobeic je bil tudi moj profesor. V spominu sta mi ostali predvsem dve stvari. Naprej moram omeniti njegov obsežen učbenik Elektrotehnologija. Pred več kot 30 leti študentje nismo bili navajeni, da bi nas profesorji pri svojih predmetih razvajali z učbeniki, zato smo prizadevanje profesorja Dobeica še posebej cenili. Spominjam se tudi, da je bil učbenik napisan v izbrani slovenščini. V spominu pa mi je ostal tudi profesor sam, kako v delovni halji stoji ob stružnici in z lastnimi rokami uresničuje svojo zamisel. Ni mu bilo dovolj, da je tehnološke probleme razumel, vse je želel tudi sam izdelati in preizkusiti.

Ob vseh teh pomembnih tehničnih dosežkih smo na Fakulteti manj poznali njegove umetniške stvaritve. Vedeli smo, da ima fotolaboratorij in da odlično obvlada postopke barvne fotografije. Manj pa nam je bilo znano, da je bil tudi večkrat nagrajen za svoje umetniške fotografije. To pa še ni vse, profesor Dobeic je bil tudi avtor operet in lutkovnih igric za otroke.

Profesor Dobeic je bil miren, prijeten in skromen človek. Bili smo srečni, da smo lahko bili njegovi študentje in sodelavci.

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Slika na naslovnici:
Letošnja konferenca, MIDEM 2001, se je odvijala v osrčju Triglavskega narodnega parka, v hotelu Zlatorog, katerega podoba se zrcali v kristalni vodi Bohinjskega jezera obdanega z vršaci Julijskih Alp.

Front page:
MIDEM 2001 Conference was held in hotel Zlatorog, mirrored in crystal waters of Lake Bohinj in the heart of Triglav National Park and surrounded by the peaks of the Julian Alps.

Informacije MIDEM
Strokovna revija za mikroelektroniko, elektronske sestavine dele in materiale

NAVODILA AVTORJEM

Informacije MIDEM je znanstveno-strokovno-društvena publikacija Strokovnega društva za mikroelektroniko, elektronske sestavne dele in materiale - MIDEM. Revija objavlja prispevke domačih in tujih avtorjev s področja mikroelektronike, elektronskih sestavnih delov in materialov, ki so lahko:
izvirni znanstveni članki, pregledni znanstveni članki, predhodne objave, strokovni članki ter predavanja in povzetki s strokovnih posvetovanj.
Strokovni prispevki bodo recenzirani.

Revija objavlja tudi aplikacijske članke, poljudne članke, novice iz stroke, vesti iz delovnih organizacij, inštitutov in fakultet, obvestila o akcijah društva MIDEM in njegovih članov ter druge prispevke.

Strokovni prispevki morajo biti pripravljeni na naslednji način:

1. Naslov dela, imena in priimki avtorjev brez titul, imena institucij in firm.
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3. Naslov dela v angleščini.
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Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials

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original scientific papers, review scientific papers, prelemiinary communications, professional papers, conference papers and abstracts.
All professional contributions are subject to reviews.

Applications articles, scientific news, news from the companies, institutes and universities, reports on actions of MIDEM Society and its members as well as other relevant contributions are also welcome.

Each professional contribution should include the folowing specific components:

1. Title of paper, authors names, name of the institution/company.
2. Key Words and Abstract (not more than 250 words).
3. Introduction, maintext, conclusion, acknowledgements, appendix and references following the IMRAD scheme (Introduction, Methods, Results and Discussion).
4. Full authors' names, titles and complete company or institution address including Tel./Fax/E-mail.

COMMENT: Slovenian authors who write in English language must submit title, abstract and key words also in Slovene language.

General informations

1. Authors should use SI units and provide alternative units in parentheses wherever necessary.
2. Illustrations should be in black on white paper. Their width should be up to 7.5 or 15 cm. Each illustration table or photograph should be numbered and with legend added. Illustrations tables and photographs are not to be placed into the text but added separately. However, their position in the text should be clearly marked.
3. Contributions may be written and will be published in Slovene language.
4. Papers will not be accepted unless two copies are recived.
5. Authors may send their files on formated diskettes (3.5"/1.44 mb/) in ASCII or Word for Windows 6.0 format as text will be formatted in Ventura 5.0. Graphic files may be in TIFF, EPS, PCX, GEM or JPG formats.

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Contributions are to be sent to the address:

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