EFFICIENT IMPLEMENTATION OF A THREE-CHANNEL ECG DIGITAL ACQUISITION MODULE

Uroš Platiše[1], Matej Cvikl[2], Andrej Žemva[3]

[1] Andeuros, Kranj, Slovenia; [2] Konel d.o.o., Šenčur, Slovenia;
[3] Fakulteta za elektrotehniko, Ljubljana, Slovenia

Key words: ECG, PSoC, mixed-signal array, microcontroller, analog signal acquisition, quantization, sampling, holter monitor

Abstract: ECG signal acquisition has to deal with small signal measuring. The amplitude of the ECG signal is only a few mV and the signal frequency ranges from a few mHz to a few hundred Hz. The signal baseline drift caused by respiration or variable contact between the electrode and the skin, signals generated because of power line interference from power mains, and noise often obstruct otherwise simple ECG signal measurements. In this paper, one of the possible ECG signal acquiring systems that overcome these problems is shown. The developed system is a three-channel signal acquiring device easily comparable to some of the commercially available holter monitors. The specialty of the device acquisition part is that it is realized with only two active components, i.e. an instrumentation amplifier and a PSoC mixed-signal array.

Učinkovita implementacija digitalnega modula za trikanalen zajem EKG signala

Kjučne besede: EKG, PSoC, mikrokrmilnik, zajem analognega signala, vzorčenje, holter

Izvleček: Merjenje EKG signalov je merjenje signalov nizke amplitude. Amplituda EKG signala je le nekaj mV, njegov frekvenčni razpon pa je med nekaj mHz in nekaj sto Hz. Merjenje EKG signala otežujejo motnje kot so neprenehno spreminjanje enosmerne referenčne napetosti elektrod, ki jo lahko povzroči dihanje ali pa spreminjanje upornosti med kožo in elektrodami, motnje zaradi napetosti, ki se v merilnih priključkih inducirajo zaradi elektromagnetnega polja električnega omrežja, in pa nenazadnje šum. V članku je opisana ena od možnih izvedb sistema za zajemanje EKG signala, ki lahko, ne glede na moteče dejavnike, kakovostno meri EKG signal. Razviti trikanalni merilni sistem lahko brez težav primerjamo s komercialno dobavljivimi holterji. Posebnost merilnega dela je, da je sestavljen le iz dveh aktivnih elementov; instrumentalnega ojačevalnika in PSoC mikrokrmilnika, ki je prilagojen za delo z analognimi in digitalnimi signali.

1. Introduction

Polarization and depolarization of the heart muscle mass creates a three-dimensional electrical field that changes with time. As a result, voltages can be measured on the surface of the body. They represent the pumping cycle of the myocardium. The most widely used three differential voltages that represent the heart activity are: from the right arm (RA) to the left arm (LA), from LA to the left leg (LL), and from LL to RA. These voltages are known as ECG leads I, II, and III. The right leg electrode (RL) acts as the neutral pole in this system. This configuration is known as the Einthoven triangle.

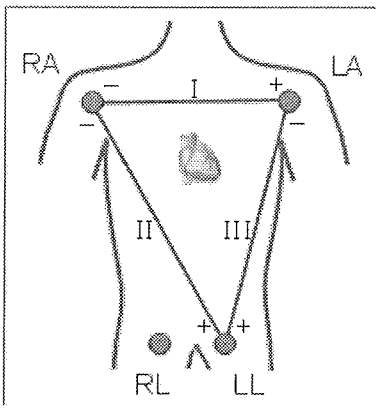

Figure 1-1: Einthoven Triangle

It is clearly seen that the three leads are defined as:

$$\text{Lead I: } V_I = V_{LA} - V_{RA} \quad (1)$$

$$\text{Lead II: } V_{II} = V_{LL} - V_{RA} \quad (2)$$

$$\text{Lead III: } V_{III} = V_{LL} - V_{LA} \quad (3)$$

This three-lead voltage system is the basis of ECG signal measuring.

The amplitude of the ECG signal as measured on the skin ranges from 0.1 mV to 5 mV and its frequency approximately extends from 0.05 Hz to 300 Hz. However, according to /1/ and /7/, ECG signal measuring in the frequency range of 0.5 Hz to 100 Hz is sufficient to do the basic analysis while a lot of devices on the market only cover the 0.5 Hz to 50 Hz frequency range which is still sufficient for monitoring applications. Since the ECG signal has a very low voltage, the average amplitude of the signal is only around 1 mV, and its frequency is low, too, there are several problems preventing its efficient measurement. One of them are large DC offset voltages resulting from electro-

chemical processes between the electrode attached to the patient and the patient's skin. These voltages can be as high as +/-500 mV. Also, the contact resistance between an electrode and the body surface can vary very much. The presence of 50 Hz (60 Hz in USA) power line noise is one of the major problems to be copped with, because common-mode voltages as high as several volts peak-to-peak can be superimposed on the body. Signals originating from muscle contraction are present in the ECG signal as well. Eliminating this source of noise is one of the major tasks of an ECG amplifier.

When one encounters health problems that indicate there is something wrong with her/his heart activity, one's ECG is usually measured. In case problems come up irregularly, usually a holter recorder is used to record heart activity over a longer period of time, usually through 24 or 48 hours. The data is stored on a removable memory media such as audio cassette or CompactFlash card. During the recording time, the person wearing the holter recorder can live her/his normal everyday life and as soon as the holter recorder is returned to the hospital, the recorded data is transferred to a PC running ECG analysis software. Doctors can now make an exact diagnosis of the problem. 24-hour holter recorders usually offer one to three-channel ECG recording with 100 to 300 samples per second at eight to ten-bit sample resolution.

The main goal of our research work was to design a low-cost ECG signal acquisition module operating as a holter recorder or an event monitor and having characteristics similar to the ones of commercially available holter recorders. We also wanted the device to consist of inexpensive, widely used and commercially available electronic components. We found it important that only components with low power consumption are used since the device is powered from battery cells. The acquired data is either saved to a SecureDigital memory card or sent to a wireless instrumentation network providing real-time global powerful data processing capabilities. Moreover, the applied wireless instrumentation network allows also on-line diagnostics of any human being under investigation, alarming, heart-attack detectors, etc.

This paper focuses on the device's acquisition part and the pertaining communication interface composed of just two different types of active components and some passive components. Differential signals of each of the three measurement channels are amplified by INA118 precision low-power instrumentation amplifiers (IA). They were chosen because of their good electrical characteristics described in /5/, they have high CMR of 120 dB, their gain is set with an external resistor and their power consumption is low.

For general processing and signal filtering, a PSoC from Cypress MicroSystems is used. This is a low-power 8-bit microcontroller designed with a different approach compared to other microcontrollers on the market. The microcontroller comprises an 8-bit core processor, eight digital

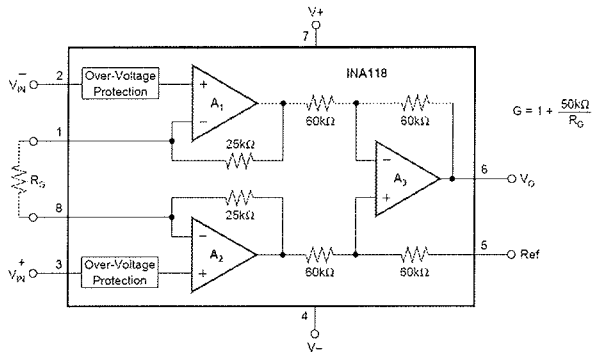

Figure 1-2: INA118 Instrumentation Amplifier

blocks and twelve analog blocks. Digital blocks provide all communication peripherals, counters, timers and PWMs while analog blocks consist of digital-to-analog converters (DAC), analog-to-digital converters (ADC), programmable gain amplifiers, programmable filters and comparators. A more detailed description can be found in /6/. A PSoC top level block diagram is shown in *Figure 1-3*.

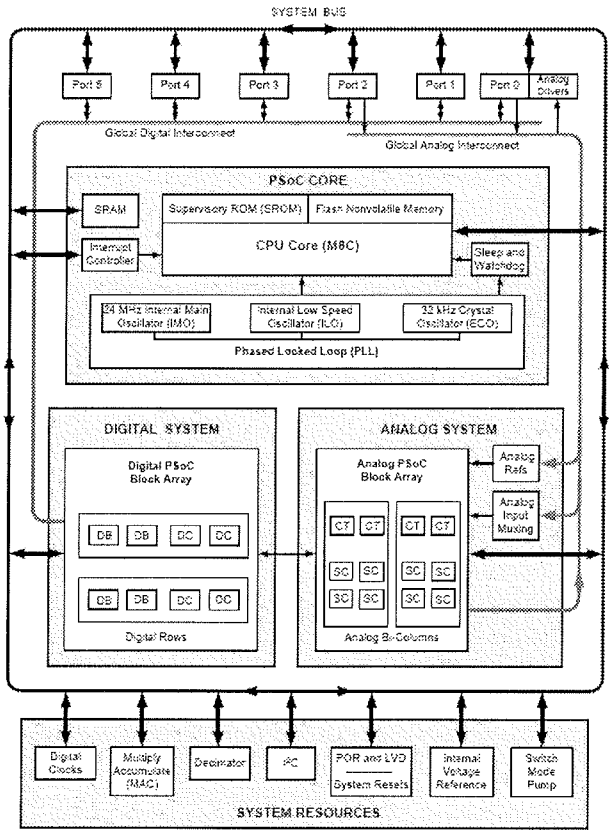

Figure 1-3: PSoC Top Level Block Diagram

2. ECG Measurement Loop

From the nature of the ECG signal and problems that interfere with the quality signal measurement, it can be seen that the overall system must protect the patient and filter out disturbing signals. As one of the most important fac-

tors is DC offset voltage elimination, the system must act as a high-pass filter that passes all signals of the frequency greater than 0.05 Hz (or at least greater than 0.5 Hz) and at its input compensates any signals of a lower frequency. The basic idea of signal acquisition is to amplify the input signal, filter it, digitize it, and store the samples. Problems caused by the DC offset voltage are detected and eliminated by a feedback loop.

Input Stage and Active Driving of Body Reference

One of DAC in PSoC is used to generate a 1.3 V signal named the body reference. This signal is used as the right leg drive signal RA shown in *Figure 1-1* and sets the patient's body to a virtual potential of 1.3 V against the measurement system which is this way placed at a virtual potential of 0 V. The ECG signal is led to the INA118 IA through high-resistance series resistors (R_{PROT}) used to prevent either possible quick discharges of IA input capacitors through the patient's body or high-current flows through the patient's body in case of device malfunction. The same kind of resistor is used on the body reference signal as well. IA gain K_{IA} is set to 16 meaning the input differential signal voltage is multiplied by 16 at the IA output. At the same time, the IA's common-mode rejection ratio (CMRR) of 120 dB assures that only one millionth of the input common mode signal voltage passes to the output of the amplifier.

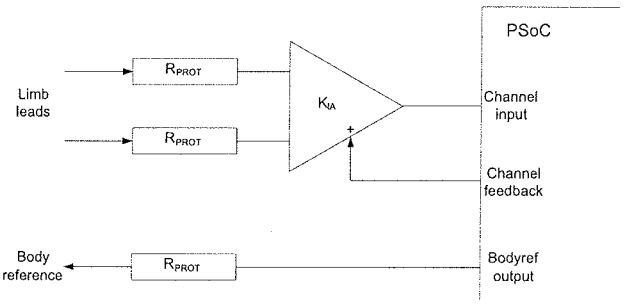

Figure 2-1: Input/Output Stage

This CMRR assures that almost no common-mode interference voltages (usually inducted in wires because of the power line electromagnetic field) pass the IA. Once the signal is amplified, it is acquired by the PSoC where it is again amplified by one of the programmable gain amplifiers (PGA). Here, too, the gain is set to 16 (K_{CHIA}). A simple diagram of the PGA block is shown in *Figure 2-2*.

Analog-to-Digital Conversion

After amplification, the signal is digitized with integrating ADC represented with a block named H_{AD}. H_{AD} is an ADC converter transfer function which can be derived from the equation characteristic for integration:

$$V_{OUT}=\frac{\int_{t-T_{int}}^{t} V_{IN}}{T_{int}} \qquad (4)$$

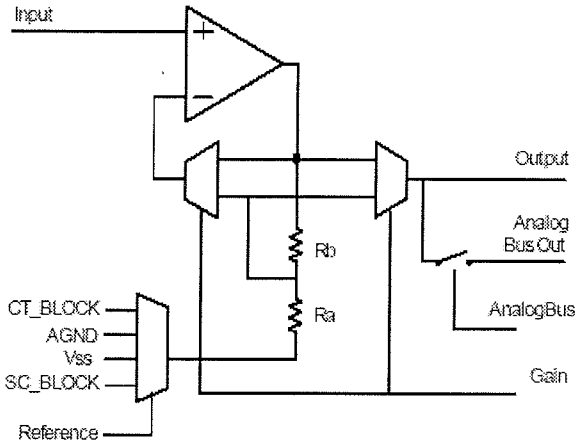

Figure 2-2: PSoC PGA Block (K_{CHIA})

which after Laplace transformation becomes:

$$V_{OUT}(s)=V_{IN}(s)\cdot\frac{1}{T_{int}\cdot s}\Rightarrow H_{AD}=\frac{1}{T_{int}\cdot s} \qquad (5)$$

T_{int} (integrating time) can be calculated according to instructions in the PSoC datasheet. In our case, T_{int} is 6.8267 ms. But as there is also delay to perform the above calculation within the PSoC, the total time spent for integration is 10 ms. Since the function of integration is not active all the time, but rather at short time intervals, the integrating part can be omitted and the transfer function can be written in a completely different way. We can say that its value depends on the input voltage range and number of output bits (resolution).

$$H_{AD}=\frac{N}{V_{ADC}}=\frac{256}{2.6} \qquad (6)$$

An important benefit of the ADC used is that it consists of three separate ADCs which can all operate simultaneously. A simplified block diagram of this triple ADC is shown in *Figure 2-3*. Although their resolution ranges from 7 to 13-bits per sample and the sample rate can go as high as 10,000 samples per second, 8-bit resolution at 100 samples per second was chosen. Samples are stored in a 24-bit register to enable further signal processing. ADC default reference voltage V_{ref} is set to 1.3 V and can therefore efficiently digitize voltages that range between 0 V to 2.6 V (V_{ref} ± 1.3 V). V_{ref} is the reason for setting the body reference to 1.3 V. As already mentioned, the peak-to-peak voltage of the ECG signal is approximately 10 mV. In order to stretch these 10 mV to the entire 2.6 V scale of the ADC, the signal is amplified.

$$V_{ADC}=K_{IA}\cdot K_{CHIA}\cdot V_{ECG} \qquad (7)$$

With V_{ECG} = 10 mV and K_{IA} = K_{CHIA} = 16, V_{ADC} as an input voltage to the ADC equals 2.56 V which almost covers the entire ADC input range.

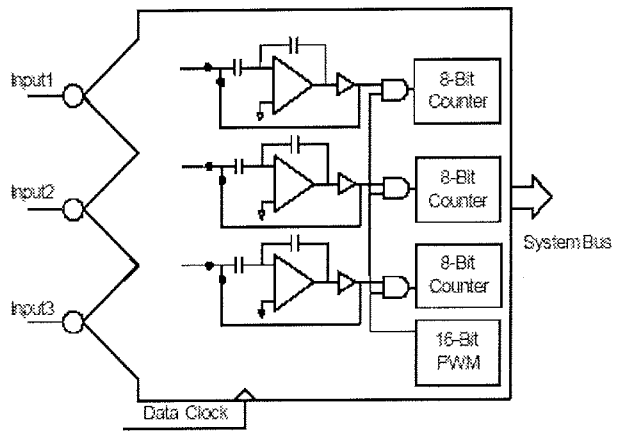

Figure 2-3: PSoC Triple Input ADC - Simplified

Though the signal is now ready to be stored to the memory card, there is still one more problem to be solved.

Feedback Loop – Integrator and Pole Positioning

As the first step in the DC component detection and elimination, an integrator is used to continuously integrate the digitized ECG signal.

An important detail of the design is also a correct system transfer function pole placement. The pole defines which frequencies will be attenuated and which not. In order to get the desired effect and place the pole near to 0.05 Hz or 0.1 Hz, the signal is multiplied by 16 (K_P).

Feedback Loop – Digital-to-Analog Conversion

Conversion back to the analog signal is necessary to provide offset voltage compensation to the input IA. Digital-to-analog conversion is done with an 8-bit pulse-width modulator (PWM) and a low-pass RC filter. Voltage conversion using just an 8-bit PWM usually gives satisfying result in low-precision systems, whereas in our case any minor integrating change would immediately result in DC offset voltage modification at the low-pass filter. Since this is not desired, the precision was improved with a software delta-sigma modulator placed in front of the PWM.

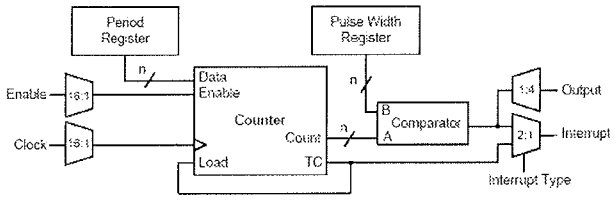

Figure 2-4: PSoC PWM Block Diagram

A software delta sigma modulator upon 8-bit PWM hardware enhances resolution for additional 7-bits, yielding a 15-bit DAC. Eight most significant bits are actually used as an input signal to the PWM, while seven less significant bits are used as its decimal value. Although an 8-bit PWM is used, together with a delta-sigma modulator the overall performance increases as if a 15-bit PWM was used. Because of the nature of digital-to-analog conversion a conversion factor K_C of 3.3/256 has to be taken in consideration. The PWM output is connected to a low-pass RC filter with components R=6.8 kΩ and C=22 μF.

$$H_{RC}(s)=\frac{1}{1+s\cdot R\cdot C} \tag{8}$$

The output voltage generated on the filter is finally inverted by PSoC (K_{REF}) and to IA where it is added to the input ECG signal.

Other Overall System Design Considerations

A possible problem that arises with digital-to-analog transformation is noise generation. It reflects itself in a noisy feedback offset voltage which is consequently inserted into the ECG signal. This problem is minimized in two ways. Noise is at first very much reduced by a low-pass RC filter placed after the IA and is again reduced by integrating ADC. Integrating time (T_{int}) of ADC and PWM pulse period (T_{PWM}) are set in such way that T_{int} is a wholenumber multiple of T_{PWM}.

$$T_{int}=k\cdot T_{PWM};\ k\in N \tag{9}$$

This relation maximizes rejection of noise generated by the PWM, while other high-frequency (stochastic) noise is also much reduced with ADC signal integration.

AC Filter

Using the blocks mentioned above, a first order AC-filter eliminating the DC voltage at the input is constructed. We can briefly describe the process that is hiding behind the system. Although the body reference voltage potential is set to 1.3 V, it is not necessary that this is also a reference or offset voltage for each ECG channel. It is more likely that each channel differential voltage will have its own offset voltage drifting around 1.3 V value. This deviation can cause incorrect ECG signal measurement because an incorrect offset voltage can cause the ADC input range to be exceeded. Any DC or very low frequency components must therefore be removed from the signal being taken care of by the feedback loop. The integrator in the loop detects this error which is then converted back to the analog signal and subtracted from the source ECG signal by the IA.

Offset Compensator

The offset compensator is an additional part to the overall AC filter design. Its position in the system can be seen in the lower right part of the overall system block diagram shown in *Figure 2-6.* The offset compensator is responsi-

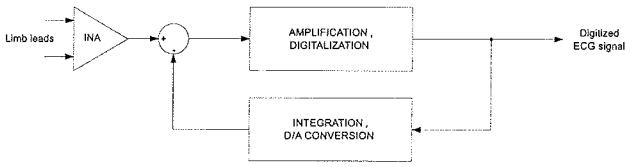

Figure 2-5: Basic System Loop

ble for setting the ECG signal to the centre of the ADC input voltage range when certain conditions are not met. The AC filter integrator located in the upper branch (INT) operates all the time while the integrator in the lower branch (INT_{OC}) is only active when the signal reaches the upper or lower ADC limit. The part of the design that enables or disables the second integrator is shown as a block with a non-linear transfer function. This offset compensator continuously monitors sampled values and centers the signal to $V_{PP}/2$, where V_{PP} is the ECG signal peak-to-peak voltage. When the values are within a preset range, the second integrator is disabled, but when the values fall out of the preset range, the second integrator is enabled.

System Transfer Function Calculation

After having described the system, we can show a complete block diagram for one of the three measurement channels (one lead). The remaining two channels are designed in a similar way, except for the body reference which is common for all the three channels.

The *Figure 2-6* shows which functional blocks are realized in PSoC and which are realized with external components. It can be seen that only input IA (K_{IA}) and low pass filter (H_{FILT}) are placed outside the PSoC boundary and therefore realized with external components.

The following transfer function can be written for the system presented in the *Figure 2-6*:

$$H(s)=K_{INA}\cdot\frac{K_{CHIA}\cdot H_{AD}}{1-K_{INT}\cdot K_P\cdot H_{DA}\cdot K_C\cdot H_{FILT}\cdot K_{REF}} \quad (10)$$

After all values are entered in this equation, the result is:

$$H(s)=\frac{1616\cdot\frac{256}{2.6}}{1-\frac{100}{s}\cdot 16\cdot\frac{1}{2^{16}}\cdot\frac{3.3}{256}\cdot\frac{1}{1+0.15\cdot s}\cdot(-1)}=$$

$$=\frac{25206.15\cdot(0.15\cdot s+1)\cdot s}{(0.15\cdot s+1)\cdot s+0.5} \quad (11)$$

Both poles of the transfer function are negative which is common to absolutely stable systems. One of the transfer function poles is at -0.544 and the other at -6.122. After recalculation from the s domain to the frequency domain this means the poles are at -0.087 Hz and -0.974 Hz. The pole that is closer to zero has a dominant influence on the system transfer function. It is therefore expected that signals of frequency lower than 0.087 Hz will be attenuated.

For testing purposes, the system response to the unit step can simply be calculated by multiplying H(s) with 1/s which is Laplace transformation of the unit step. Using the Mathcad tool, we performed inverse Laplace transformation of the response and got a result shown in *Figure 2-7*. It can be seen that soon after the input signal goes high at t=0 s and stays high, the system detects this as a DC offset and starts with compensation. After two seconds, the signal already drops by 63%.

This is the expected response. At the beginning, there is no input signal to the system. Once the unit step is present, the system samples the change and outputs it. But as the input voltage does not change with time, the system treats it as a large DC offset. Input DC offset should not be a part of the desired ECG signal measurement, therefore the PSoC starts compensating it. Consequently, the output voltage starts falling towards 0 V.

3. Communication interface

Processed ECG data samples are sent to the second processor that handles wireless data transfer or data storage to removable media. Data exchange is done via both proces-

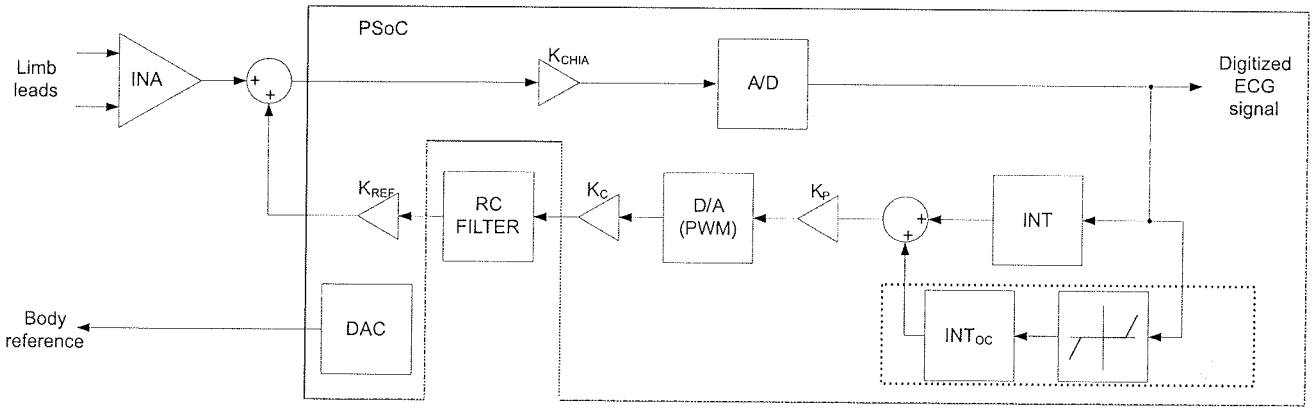

Figure 2-6: Complete Measurement Loop

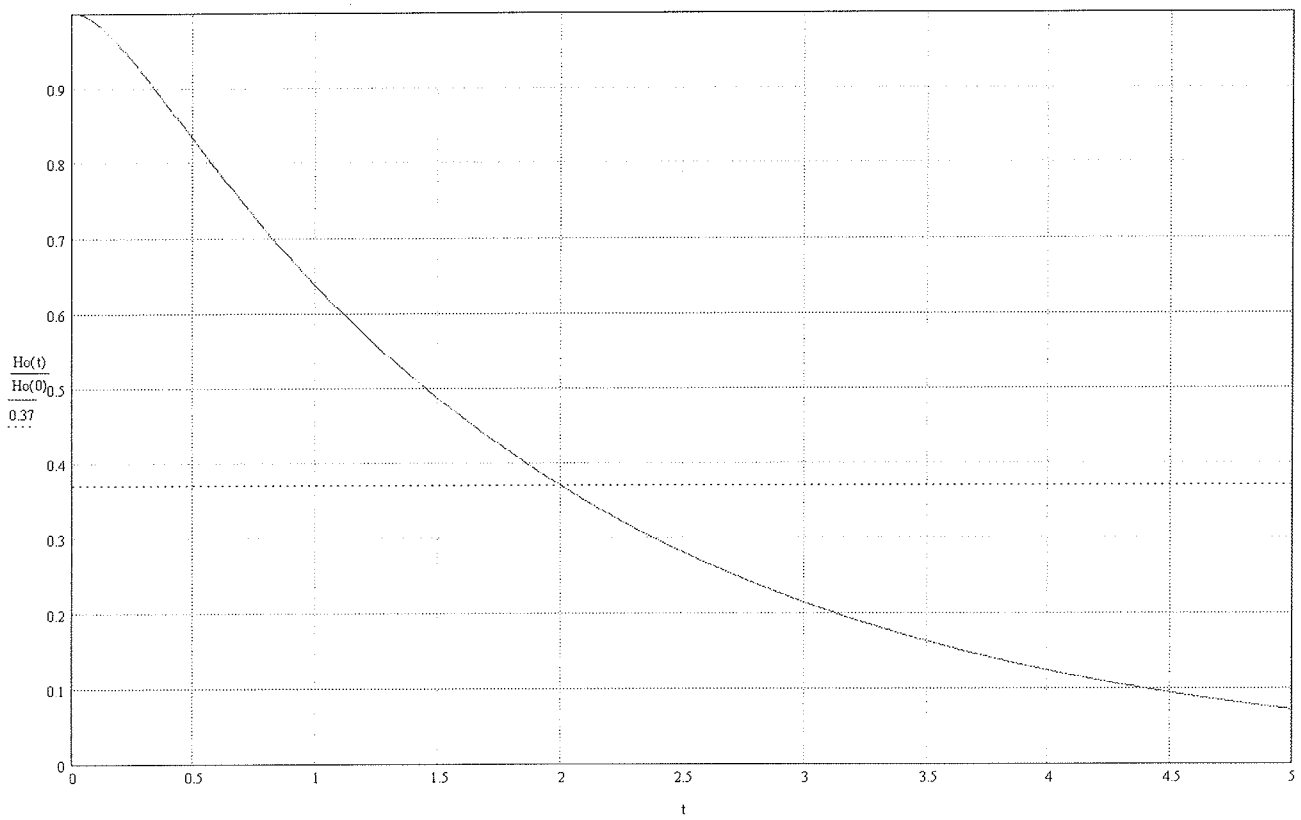

Figure 2-7: Calculated System Response to Input Unit Step

sors' I2C interfaces. As the design is battery powered, it is crucial that ECG data is sent as infrequently as possible in order to save power. For making this possible, data compression is done in the PSoC. For this purpose we implemented Huffman variable length coding (VLC). This is an entropy encoding algorithm that finds the optimal system of encoding strings based on the relative frequency of each symbol. Fixed 8-bit size binary symbols are replaced with variable length codes of an optimal length in such a way that the most common symbols are presented in the shortest way possible. The larger is the probability of a symbol to occur, the shorter is its code.

Because of the dynamic nature of the ECG signal, the range of different values it can take is relatively large. *Figure 3-1* shows how often individual 8-bit sampled values of the ECG signal are repeated over a certain period of time.

The number of different values can be significantly reduced if the ECG signal is represented with differences between adjacent signal values. Distribution of such signal representation is shown in *Figure 3-2*.

We can see that this kind of signal representation is more concentrated around one value and is less dispersed over the whole range. A system with less different values can more easily and efficiently be encoded, therefore the second signal representation was chosen. As an offset value of the signal must be known, the first data sample needs to have its real sampled value. All other ECG signal values

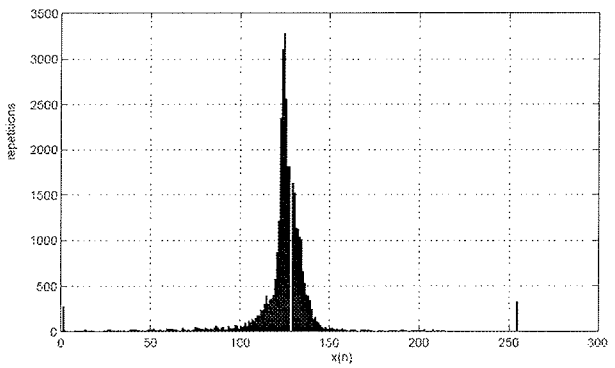

Figure 3-1: Value Distribution of a Sampled ECG Signal

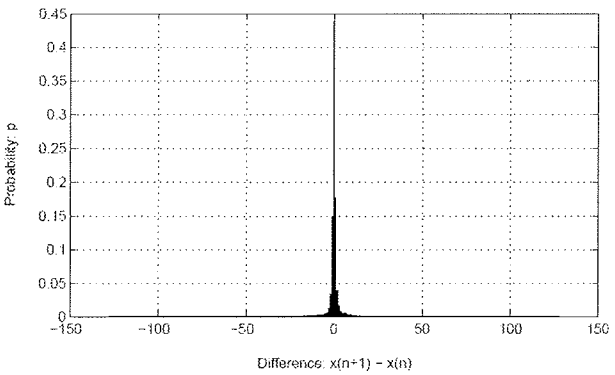

Figure 3-2: Distribution of Differential Values Between Adjacent ECG Samples

are derived from the given differences. The resulting ECG signal vector would thus be:

$$X=[x(1), d_{1,2}, d_{2,3}, \ldots, d_{n-1,n}] \quad (12)$$

where x(1) is the first data sample and $d_{i,j}$ is the difference between sample x(i) and x(j). This kind of data stream can be efficiently encoded at this point. A set of Matlab/Octave dedicated functions was used in order to generate the Huffman codes from the distribution shown in *Figure 3-2*. Because of power saving, the encoded ECG signal data needs to be sent out of the PSoC microcontroller in bursts of packets. A calculation of the compression ratio versus the packet size was used to find an optimal packet length. To find the optimum packet size, an N bytes long input vector was compressed and repacked to P bytes long output packets. The compression ratio is represented as:

$$\text{Compression\_Ratio}=\frac{\text{Input\_Packets}}{\text{Output\_Packets}}=\frac{N}{P} \quad (13)$$

Results are shown in *Figure 3-3* where it can be seen that the packet size greater than 10 bytes should be sent to the second microcontroller.

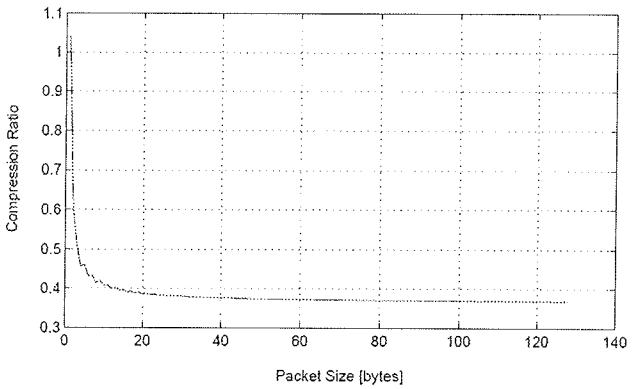

Figure 3-3: Compression Ratio vs. the Packet Size

4. Results

Hardware implementation was verified using a sine generator to scan the frequency response function. Measurements showed that the system started to attenuate input signals of the frequency lower than approximately 0.4 Hz. Attenuation of $\sqrt{2}$ was achieved at approximately 0.075 Hz which is very near to one of the calculated poles of the system transfer function.

In the next step we measured how the system responds to a unit step input signal. *Figure 4-1* depicts this measurement performed on the third channel. As the other two channels were short circuited, they are not shown. The markings in the figure are used for a quicker orientation. It can be noted that the response is very similar to the calculated response depicted in *Figure 2-7*, meaning that implementation results overlap with theoretical results.

After verifying characteristics of each channel, the ECG signal was measured using the placement as described for a popular holter manufactured by Spacelabs Burdick, Inc. The lead placement and placement description according to /4/ are shown in *Figure 4-2* and *Table 4-1*.

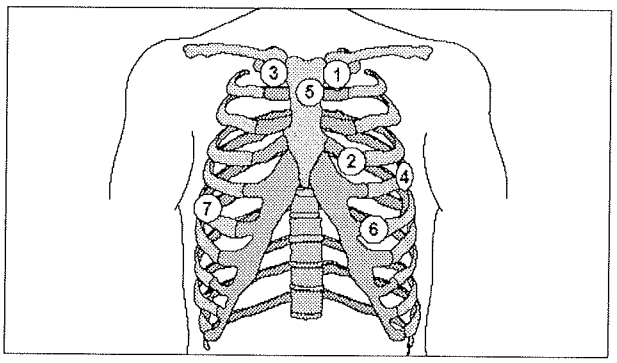

Figure 4-2: ECG Lead Placement

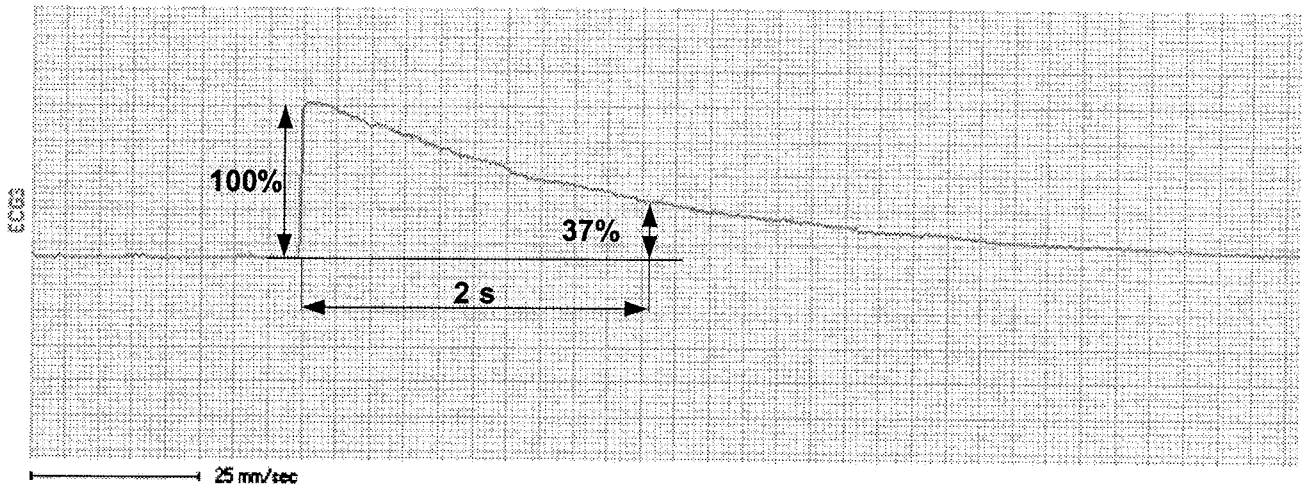

Figure 4-1: Response to Low-frequency Square-wave Input Signal on Channel 3

Table 4-1: Lead Placement Description

#	Channel	Color	Lead	Placement
1	1 (-)	white	LA	Below left clavicle, just lateral to the midclavicular line.
2	1 (+)	red	Mod V5	At the fourth rib to the left of the sternal border.
3	2 (-)	brown	RA	Below right clavicle, just lateral to the midclavicular line.
4	2 (+)	black	Mod V6	Fifth rib at anterior axillary line.
5	3 (-)	blue	Sternum	At manubrium sterni.
6	3 (+)	orange	Mod V4	At the sixth rib on the midclavicular line.
7	Bodyref	green	Reference	Lower right chest wall, rib.

Measurement results according to the above lead placement:

Figure 4-3: 3-channel ECG Measurement

5. Conclusion

One of the possible ways of implementing an ECG signal acquiring unit was discussed in this paper. We have decided to design a device similar to the commercially available ECG holter monitors with as little electronic components as possible. In fact, only instrumentation amplifiers, passive RC filters and a PSoC microcontroller were used for our implementation. We started by identifying the problems present at ECG signal measurements, then we defined a model eliminating these problems and at last calculated its response to the input signal.

The design in hardware and software proved to work in the same way as the theoretical model. Measurements showed that the input DC voltage and common mode voltage are successfully reduced and therefore do not have any major influence on the ECG signal measurement quality. Our design samples and records the input signal at the rate of 100 samples per second with 8-bit resolution. The input signal frequency range is between 0.1 Hz and 50 Hz. Signals of the frequency out of this range are either attenuated or not sampled correctly.

In the next step we shall investigate the possibilities of increasing both the sampling frequency and the number of bits per sample. The microcontroller is loaded as little as 30%. The theoretical limitations show the maximum sampling frequencies to be up to 800 Hz @ 9 bits and maximum resolution 12 bits @ 100 Hz. Some of the possible limitations will surely be additional tasks the microcontroller shall have to perform in a target system. Also to be investigated is the allowed power consumption of the target system.

Acknowledgement: This work was supported by Ministry of Education, Science and Sport of Republic of Slovenia as part of Research Program P2-0246 "Algorithms and Optimization in Telecommunications"

References

/1/ J. Enderle: *Introduction to Biomedical Engineering*, San Diego, Calif.: Academic Press, 2000.

/2/ F. Bergelj: *Meritve 2. del*, Založba FE in FRI, Ljubljana 1996

/3/ B. Zupančič: *Zvezni regulacijski sistemi - I. Del*, Založba FE in FRI, Ljubljana 1996

/4/ Spacelabs Burdick, Inc. Compact Digital Recorders (6722 / 6732 / 92512 / 92513) Operating Instructions Part No. 070-0860-00 Revision B

/5/ INA118 Precision, Low Power Instrumentation Amplifier, Burr-Brown Corporation, April 1998

/6/ PSoC™ Mixed Signal Array Final Data Sheet, Cypress Microsystems, 2004

/7/ ACC/AHA Guidelines for Ambulatory Electrocardiography, American Heart Association, 1999

Uroš Platiše
Andeuros, Kranj, Slovenia

Matej Cvikl
Konel d.o.o., Šenčur, Slovenia

Andrej Žemva
Fakulteta za elektrotehniko, Ljubljana, Slovenia

Prispelo (Arrived): 04.01.2005 *Sprejeto (Accepted): 15.03.2005*