A STUDY OF HIGHLY DOPED LAYERS FOR BICMOS COLLECTOR INSERTS

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Abstract: In order to develop a BiCMOS IC fabrication module based on implantation and diffusion of dopants for the collector insert layers for the vertical npn bipolar transistors, we performed a detailed comparison of simulations of such a process and results of actual fabrication of the layers. We conclude that the thickness and half—width of the collector insert layers can be simulated accurately (within 4% of measured values, on average), which satisfies the requirements for developing the process module. However, for process control purposes simulations seem to have to be augmented by a direct measuring method.

Študija močno dopiranih plasti za BiCMOS kolektorske vložke

Ključne besede: mikroelektronika, IC vezja integrirana, BiCMOS CMOS vezja bipolarna, izdelava vezij, profil koncentracije dopantov, plasti tanke, vložki kolektorski transistorjev, simulacije računalniške, postopki tehnološki

Izvleček: Z namenom, da bi za razvili modularni tehnološki postopek za izdelavo integriranih vezji tipa BiCMOS, na osnovi implantirane in difundirane dopirane plasti za kolektorski vložek vertikalnih, bipolarnih npn tranzistorjev, smo izvedli natančno primerjavo računalniške simulacije izdelave takšnih plasti in fizikalnih karakteristik izdelanih plasti. Ugotovili smo, da se simulacije in meritve debeline plasti in njene polovične širine ujemajo v povprečju na 4 %. To zadošča za potrebe razvoja procesa, medtem ko je za procesno kontrolo simulacije dopolnjevati z neposrednimi meritvami fizikalnih lastnosti plasti.

1. Introduction

BiCMOS technology integrates both CMOS and bipolar device structures on the same chip. This capability can be exploited in a number of ways to produce integrated circuits (IC) with performances that exceed those that are possible when only one of the device types is used. These benefits are attained at the expense of a more complex fabrication technology, including development and chip manufacturing tasks, however, in many high performance digital applications and in mixed analog/digital systems the benefits often exceed these extra costs. The key feature of a BiCMOS technology is fabrication of the collector inserts for the bipolar npn vertical transistors. In high performance BiCMOS ICs the fabrication of the insert is usually based on epitaxial layers. However, if one wishes to augment an existing CMOS technology by adding bipolar devices (e.g. in I/O drivers), an improvement of IC performance can still be achieved by a simpler, and relatively low cost BiCMOS technology, involving essentially only additional implantation and diffusion processing steps /1/. A serious limitation in developing such a process is that there exists no reliable nondestructive method for characterizing the insert layers, in addition to the fact that lack of a reliable measuring method makes tight control the fabrication process difficult. However, computer process simulation is sometimes a viable alternative to characterization measurements required by the development and production. In this contribution we present an attempt to correlate a destructive layer characterization method, Spreading Resistance Analysis (SRA), with results of a detailed simulation of a 1.2 μm IC fabrication process, extended to BiCMOS capability, and comment on the applicability of simulation for development and production needs.

2. Experimental

Test processing in our study was designed as an extension (i.e. insertion module) in an existing 1.2 μm CMOS process. (This is a standard, although proprietary 17 layer process defined and used by the IMP, San Jose, Ca., USA.) /2, 8/ It was executed on p-type, <1-0-0> silicon wafers, nominally 25-50 Ωcm, selected for uniformity. The fabrication of the collector insert layer consisted of doping in a two-step process: a phosphorus implantation followed by a deposition of a layer of phosphorus-doped poly-Si. The implantation was performed at 150 keV, at the dose of $8 \cdot 10^{12}$ ions/cm^2. The poly-Si layer was the dopant source for diffusion of phosphorus into silicone during the deposition itself and in subsequent processing step. In a preliminary study it has been determined that the

required insert layer properties can be achieved only by a modification of the standard process: doped poly-Si layer was deposited at 1150 °C in N_2 atmosphere, followed by oxidation at 1130 °C. At this stage the poly-Si layer was removed from the wafer surface and further diffusion performed at 1000 °C for 240 min. This processing results in a thick (approximately 5 μm), low resistivity (1.5 to 2.5 Ωcm) layer that is adequate for fabrication of the collector inserts. For convenience, the details of the process parameters of short loop are summarized in Table 1.

Tab. 1: Process parameters of key process steps in fabrication of the collector insert layer.

process step	process parameters
P implantation	dose: 8 x 10^{12} ions/cm^2; voltage: 150 keV
poly-Si deposition	temp: 1150 °C dep. time (diffusion 1): 32, 24.5, 22, 20 min
oxidation	temp: 1130 °C time (diffusion 2): 14.5, 11, 8.5, 8.5 min
diffusion	temp: 1000 °C time: 240 min

Finally the experimental run was split in two parts: one was analyzed by the SRA method and the other further processed (metallization, etching) to allow standard C-V analysis. The poly-Si deposition and diffusion steps was performed in a Thermco diffusion furnace /3/.

A C-V characterization of the insert layers with a parametric tester, Hewlett Packard model HP 4062B, was attempted. From the numerical analysis of the C-V data the dopant profile can in principle be determined /4,5/ if certain limitations of the method, concerning the size of the capacitor, dopant concentration and inversion layer depth are not exceeded. However, in our study precisely this was the case; the method yielded reasonable data for surface dopant concentrations but the insert layer thickness could not be determined by this method.

Spreading Resistance Analysis (SRA) allows for an accurate and relatively simple determination of the dopant profile /6/ by a 2-point method. However, it is destructive. A bevel, inclined approximately 0.5 deg to the wafer surface, is ground into the wafer with 5 μm grit. Knowing the angle of the taper gives the distance from the surface as a function of displacement along the bevel. The shallow taper allows an accurate probing of the profile in over 100 steps of 10 μm each. The probe contact force was 7.5 x 10^{-2} N. SRA measurements were performed at Solecon Laboratories Inc, Ca., USA, according to their standard procedures. Having the SRA measurements performed at a commercial laboratory was deemed necessary as no reliable calibrated dopant profile standards are available which would insure the required precision of measurements.

For simulations of the collector insert fabrication steps the well known 2 dimensional program package SUPREM 4, with capability of generating data for the 2-D IC simulator PISCES 2B, (7), run on s Sun workstation, was used.

3. Results and discussion

The simulations program package that we have used is usually applied for simulations and analysis of standard IC fabrication steps for which processing parameters are, to a certain extend, generic. However, fabrication of collector inserts involves parameters that exceed the standard ones and it was not obvious from the outset that the mathematical models used in the simulations package are adequate for modeling the formation of very thick, highly doped films. A detailed, point by point comparison of simulation results and SRA profile measurements was therefore performed. 4 different processing sequences (each involving 5 wafers) were studied, the relevant details of which are given in Table 2, and the results of measurements and simulations in Table 3.

Tab. 2. Details of the 4 different processing sequences studied.

#	p_B (cm^{-3})	diffusion 1	diffusion 2	bevel angle (rad)
1	8 . 10^{14}	32 min	14.5	0.0099
2	8	24.5	11.0	0.0103
3	8	22	8.5	0.0107
4	8	20	8.5	0.0107

Tab. 3. Results of SRA measurements and simulations for the 4 different processing sequences studied

#	SRA measurements			simulation		
	n_S (cm^{-3})	$d_{½}$ (μm)	d_i (μm)	n_S (cm^{-3})	$d_{½}$ (μm)	d_i (μm)
1	9.0 10^{19}	3.7	4.8	4.5 10^{19}	3.6	4.8
2	9.5	3.8	4.5	3.8	3.8	4.9
3	7.0	3.8	4.6	4.0	3.7	4.8
4	6.5	3.6	4.5	4.3	3.9	4.7

It has been determined that some of the features of the profiles can be simulated quite accurately while the surface concentrations of the treated wafers less so. Even though over-all agreement was deemed sufficient for proces development purposes, it has

been attempted to reduce these differences by varying the simulation parameters, but no significant improvement could be achieved.

The resulting shape of the concentration profiles resulting from fabrication steps employed in our study is quite similar to those of the standard processing steps, which have been well studied and are understood /2, and References therein/. Therefore it is sufficient to characterize our profiles with 4 parameters only: concentration of dopants in untreated wafer p_B (bulk concentration; for our study wafers with the same $p_B = 8 . 10^{14}$ cm^{-3} were selected), surface concentration of the treated wafers (i. e. on top of the fabricated collector insert) p_s, half-width of the distribution $d_{1/2}$, conveniently defined as the depth at concentration

$c_{1/2} = sqrt(n_s \times p_B)$,

and the depth of the inversion layer d_i. Comparison of measured and simulated values shows that the differences in $d_{1/2}$ and d_i in no case exceeds 8 %, the average vale of the difference being less than 4 %. Our data demonstrate that the doped poly-Si layer is not depleted as a source during the deposition and subsequent oxidation. Thus the details and possible variations during processing of these two steps are not critically reflected in the properties of the final insert layer. The layer profile and its thickness (depth of the inversion layer) are primarily determined by the final diffusion step, which insures reliability and repeatability of the fabrication module, as was intended.

The relatively large discrepancy between the measured and simulated values of n_S (largest difference 60 %, average over the 4 sequences 45 %) could not be traced to a single cause with any degree of certainty. The measured values are in all cases larger than the simulated ones and it seems probable that the actual thermal balance of the processing is not faithfully reflected by the simulation, and thus the effect of the depletion of dopants in the poly-Si exaggerated. However, the integrated concentrations of the dopants in a fabricated layer, which largely determine its bulk properties and have been calculated from the measuring and simulations data, differ only slightly and are not significantly effected by the differences in n_S obtaint via the two routes. From the production standpoint the discrepancy is a point of only minor concern as the over-all properties of the collector insert are satisfactory and the developed production module has been proven to yield working ICs with the required properties. However, it demonstrates the limitations of simulations for process control and the need for a physical measuring method for such purposes.

4. Conclusion

On the basis of over-all and reasonable agreement between the results of measurements and simulations, we conclude that computer simulations of processing steps required for fabrication of the collector inserts are a reliable tool in developing BiCMOS technologies in which such layers are fabricated by implantation and diffusion of dopants. In particular, the thickness of the collector insert layer and its resistance can be simulated accurately. It seems that with some care such an approach, combined with a direct measuring method (e.g. C-V measurements), can be used in process control, and possibilities in this direction are presently being explored in our laboratory.

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