INTEGRATED OPTICAL POSITION MICROSYSTEM WITH PROGRAMMABLE RESOLUTION

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Abstract: The paper describes an integrated optical microsystem for motion detection, which combines the following: an analog programmable interpolator, digital drivers, a differential analog front-end, signal monitoring outputs, error handling and an array of light-sensitive cells with a micro-strip raster.

The interpolator outputs are generated from orthogonal sinusoidal signals coming from illuminated integrated photo-sensors. The optical microsystem is composed of an autocalibration on an analog front-end to get proper interpolating signals. It consists of three symmetrical analog channels: *sine*, *cosine* and reference signal channel. Each channel combines a current-gain stage operating as a fully differential current-to-voltage converter and thus guarantees the best phase relation between the ordinary and the inverted analog signals. Integrated analog buffers are used for monitoring the processed analog signals. The signal bandwidth of the analog channels is designed to be large enough so as not to limit the system response and therefore maximize the useful signal range.

An ASIC was fabricated using standard in-house CMOS technology and three different types of photo-diodes having an area of 600um x 1500um each was integrated. The P+P/N substrate diode's responsivity of 0.52A/W and the 12uA typical diode current was the best result that was achieved by the motion detection system. Programmed interpolating factors of 4, 20 and 40 were realized (1, 2, 5, 10 in standard industrial notation Fig. 10).

Vezje za merjenje pozicije z integriranim optičnim senzorjem in nastavljivo ločljivostjo

Ključne besede: mikroelektronika, merilniki položaja, interpolatorji programljivi, ločljivost programljiva, optoelektronika, optoelektronika integrirana, mikrosistemi integrirani, gonilniki diferencialni, senzorji optični, OMS mikrosistemi optični, AFE analogni del čelni

Izvleček: Opisan integrirani merilni sistem sestavljajo programljiv A/D pretvornik, diferencialni vhodni ojačevalniki, svetlobno občutljivo polje senzorjev, testne strukture, digitalni procesor, detektor napak ter mikroraster.

Analogni signal (*sinusni* in *cosinusni* tokovni signal iz fotodiod) se pretvarja v napetostni signal ter ustrezno ojači. Vgrajena je kalibracija napetosti ničenja ter korekcija faze med vhodnimi kanali. Le-ti so trije: sinusni, kosinusni ter referenčni kanal. Procesiranje analognih signalov je diferenčno, kar zagotavlja visok rejekcijski faktor na spremembe napajalne napetosti ter na motnje. Vezje ima vgrajeno detekcijo faznih nepravilnosti izhodnih pravokotnih signalov A in B ter pozicije referenčnega impulza. Za kalibracijo in opazovanje so dodani hitri operacijski ojačevalniki.

Integrirano vezje je bilo proizvedeno v laboratoriju za mikroelektroniko na Fakulteti za elektrotehniko v Ljubljani, v standardni tehnologiji CMOS z uporabo dodatne maske za eleminacijo ekstremov v spektralnem odzivu integriranih P+P/N optičnih sensorjev, katerih največja izmerjena občutljivost je 0.52A/W pri valovni dolžini 820nm. Vezje ima tudi nastavljive interpolacijske faktorje: 1, 4, 10 in 40.

1. Introduction

The integrated optical microsystem (OMS) described here is an interpolating system combined with a solid-state optical sensor. The crucial requirements of an OMS are: photosensitivity, responsivity, dark current, dynamic range, and spectral response /3/. There are a number of ways to achieve optical-position detection. One method is to use a linear photodiode array to produce a signal that is a linear function of position. When the position has to be expressed incremental-digitally or absolute-digitally, the generation of orthogonal sine-wave signals is required /1/, and it is advisable to use a coded optical wheel or a linear glass scale and glass reticle (Fig.8 and Fig.9). To achieve high resolution and accuracy, the large dynamic range and wide bandwidth of an optical analog front end (OAFE) are required. In order to be able to use a large interpolating factor up to 1000, the *sine*-wave signals have to be generated very precisely. Therefore, the precision of the coded glass, the distance from the glass to diode's surface, the IR light source and the light cross-talk between the integrated diodes are most important. If we have accurate analog signals from the OAFE, the remaining difficulties related to high interpolating factors come from the analog-to-digital conversion (interpolator). To guarantee a motion measurement that is fast, the response of the overall system should also be fast.

The system presented in this paper acquires analog signals from four regular integrated diodes that are 200μm apart and a single reference diode. The optical part of the system is integrated with the electronic part for signal processing in the silicon area without peripheral structures. Integrated diodes in the micro-raster structure help to reduce the opto-electronic response time and can be used as an integrated glass reticle, -the first time this has been used in a completely integrated system. The AFE is capable of operating in either current or voltage mode.

An integrated programmable interpolator combines specially designed comparators and a single-level-delay *EXOR*

array. The interpolator exhibits high noise immunity and is highly insensitive to amplitude and the offset difference between channels. It converts the gained and converted, orthogonal photo-current signals to an orthogonal pulses sequence named A track and B track, and a reference-position signal that is counted in an external counter and gives an incremental linear position with a different resolution. The programmed interpolating factors of 1, 4, 20, and 40 are realized. The optical microsystem also combines a self-test feature and an error detection function, which is very important for dustrial use.

The dimensions in the stripped junction's area were chosen to achieve the minimum time constant and, therefore, a fast response. This guarantees a higher speed of position detection and reduces the higher harmonics. There are numerous important electrical and electro-optical parameters that we followed and measured.

Different junctions are available in standard p-well CMOS technology. We looked for the best sensitivity, the lowest possible diode capacitance, the minimum parasitic diode current and the proper reverse-current versus temperature behavior. The diodes inherent electrical and optical behaviors are well known and it was not necessary to evaluate them /1/. The following properties of the integrated systems were measured: the diode's capacitance versus reverse operating voltage, the reverse current versus temperature and the spectral response of the integrated light sensors.

The opto-electronic properties were first measured without any change of the protective nitride and the field oxide thickness. The ASIC were then fabricated again with diodes nitride and oxide modification to remove the peaks in the spectral response. The results of the measurements are reported along with the best selected junction structure. The OMS structure and the overall system is described in the paper as well as the system's remaining external components. The integrated micro-optics, together with the mixed analog/digital electronics, results in a useful miniaturization (Fig. 10), that made it easier to test and improved the reliability of the system for industrial use /4/.

2. Circuit architecture

A. Opto-electronic OAFE and calibration

A simplified block diagram of the system is shown in Fig.1. It consists of the AFE, an optoarray, analog output buffers, an analog/digital programmable interpolator and a digital output structure.

The analog channel, as part of the AFE, is shown in Fig. 2. An orthogonal sinusoidal current or voltage enters the gain stage where the analog signal ground is used as an output balance signal. In current-mode operation the signal-ground also stabilizes the input operating point (i.e. diodes). This means that the variations in the reverse-operating diode's

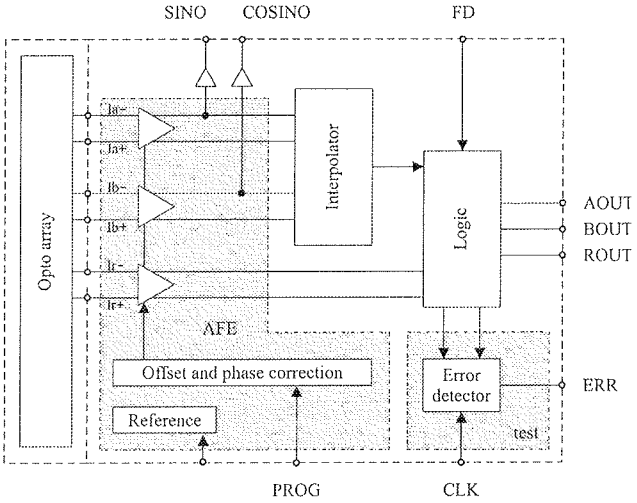

Figure 1: Block diagram of the integrated OMS microsystem

voltage are a few milivolts, with a maximum signal current of 20μA (with the diode illuminated).

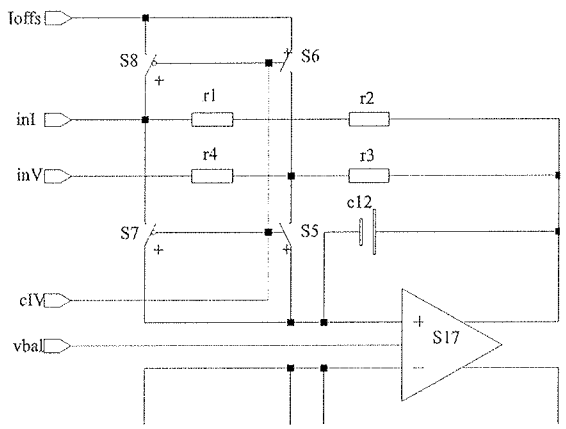

Figure 2: The AFE signal-channel half of the symmetrically-balanced stage. The current input inI or the voltage input inV is selected by the clV signal. The Ioffs input current is selected for the offset correction of the AFE. Integrated diodes are connected from inI inputs to the substrate (VDD) in reverse polarity. Each channel has two photodiodes.

Measuring the phase shift between the two AFE channels provides us with the signal for phase compensation. A part of a *sine* signal is used as a phase correction for the *cosine* signal. This principle has no effect on the signals' amplitude. The small *sine* signal is converted into a differential current by means of temperature tracking with current gain and is fed back to the input terminal of the *cosine* gain stage.

The phase adjustment is digital with a minimum step size of 0.2 angle deg. Therefore the principle looks like an aligning process between two analog channels. It is important

to note that the phase-aligning process aligns the signal phases to 90 deg. This means that aligning two orthogonal signal phases may include the overall system, i.e. it may include the external-mechanical components, too. Fig.3 shows a simplified schematic of the *cosine* phase-correction circuit.

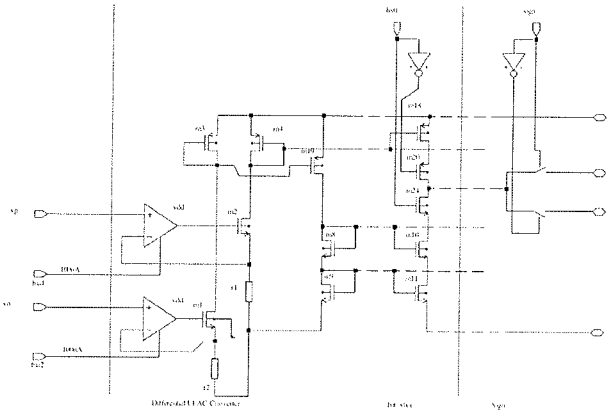

Figure 3: *Detail from the phase-correction circuit*

A very similar adjustment is used for the system-offset correction. As the analog signal-ground is used for balancing the signals going to the interpolator inputs, a part of the constant DC signal is converted into a current and feeds back into the virtual ground of the gain stage. Therefore, one analog channel is selected to be the reference, and the second channel's offset is adjusted to the first channel's offset. This is sufficient for proper operation of the analog/digital interpolator. The interpolator handles only four sinusoidal signals and does not require a signal-ground.

The corrected phase and offset stability over temperature is guaranteed by a proper design technique. The signal voltage is converted into a phase or offset current-signal error via a polysilicon resistor, which is matched with the gain-setting resistor in the AFE, where the error signal is converted back into phase or offset voltage information.

B. Interpolator

The programmable interpolator combines a novel design of comparators, a resistor chain and an *EXOR* array to process the comparators' output signals into two orthogonal pulses: A and B. Comparators have built-in hysteresis in such a way that their inputs remain high ohmic. The amplitude of the hysteresis tracks the photodiode signal on AFE output with temperature and process.

The A and B signals are generated using a 4-transistor *EXOR* logic to generate a single-level delay function and include the N-channel device of a multiple input *NOR* gate. Instead of P-channels, a simple current source is used. Because there is just one event at a time a larger DC current can be used. With more than 200 comparators and a 50µA pull-up current, the logic converter's overall delay of 1nsec is achieved. Fig. 5 shows a detail from the schematic.

C. Error detection and testing

The photosensitive elements act as good protection diodes to the substrate due to the large diode area. As a result, extra protection is not needed when the diode's anode (amplifier inputs) is routed to the PAD. External access is useful to inject the signal current for test purposes. When operating in voltage mode an externally generated differential voltage is required. It is also enough to generate a single-ended input signal and to connect one input to the generated voltage signal-ground (buffered output). In current mode, one input terminal may stay unconnected. Using a single driving input signal the AFE output is reduced by 6dB. The AFE output voltage can be monitored on external pins via integrated analog output buffers.

The sequence of the generated orthogonal pulses named A track and B track can be monitored at the output and verified in terms of position in two different ways.

The first one requires synchronization between the analog input signal and the sampling square wave, which samples the A and B tracks. The sampled tracks can trigger the counter, the contents of which can be verified at the end of *sine* wave period. For a low input sinusoidal frequency this test procedure is simply realizable in the LabVIEW environment.

The second principle is more or less completely integrated. All that is need is an external clock, which, for precise testing, needs to be synchronized with the sinusoidal frequency and requires "n" periods per one *sine* wave period. Fig.4 shows the measuring principle and the appropriate period relations with respect to the division factor and the absolute interpolation error for n=4. The resolution of the error detection is increased when a larger "n" is used. Two principles are used: error is not detected if there is a clock edge inside two tracks' edges (Fig.4a) or at least one positive and one negative clock edge is required between tracks' edges (Fig.4b).

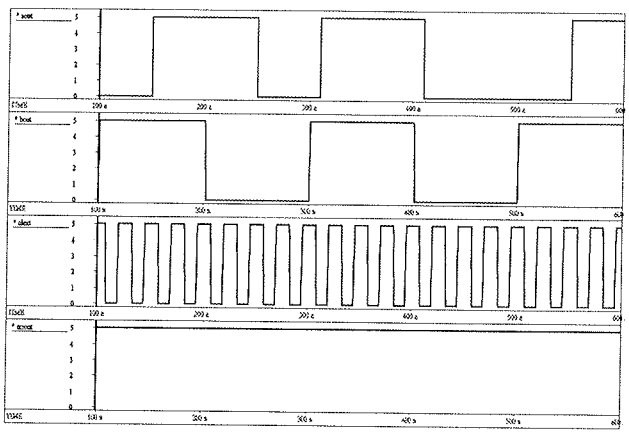

Figure 4a: *Error function: principle of operation. External clock frequency is f_ext>4FD.f_sin. Error is not detected if there is clock edge between track A and track B.*

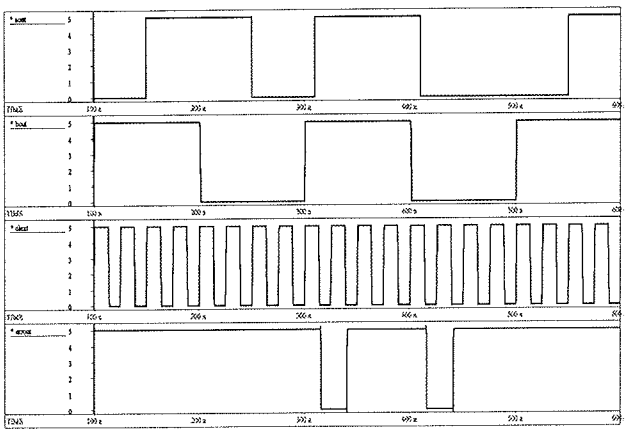

Figure 4b: Error detected (errout = LOW), edge separation is less than a half clock period.

3. Considerations for a large dynamic range

The integrated system dynamics is limited by a number of factors. The first important limitation comes from an integrated optical array related to its size, resistivity, capacitance and noise performances. The second limitation is imposed by the noise characteristic of the analog front-end channels. Let us first consider the integrated electronics, where the current mode is active.

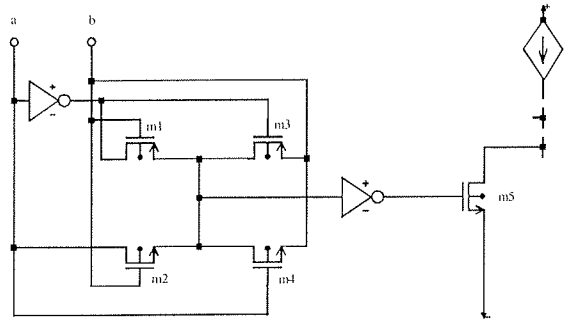

Figure 5: EXnOR logic

The feedback resistor has a nominal value of 100kΩ and is used as a current-to-voltage conversion element. It largely determines noise and bandwidth as well as gain. Resistor acts as an important wide-band noise source ($4\sqrt{R}$) in $nV/\sqrt{Hz}$, and appears directly at the output of the current-to-voltage converter without amplification (where R is the resistivity in kΩ). The fully differential amplifier in a typical application (e.g. AFE) including a biasing circuit has the voltage noise shown in fig.6. Most of the noise power is concentrated in the frequency band at low frequency and where the gain peaking occurs.

If we choose only the 100kHz bandwidth, the 50pF diode capacitance and the $1/g_m = 100k\Omega$, than the *rms* spot noise voltage of the AFE is 20μV. To achieve a 9-bit resolution of the AFE channel, the minimum output voltage on the AFE

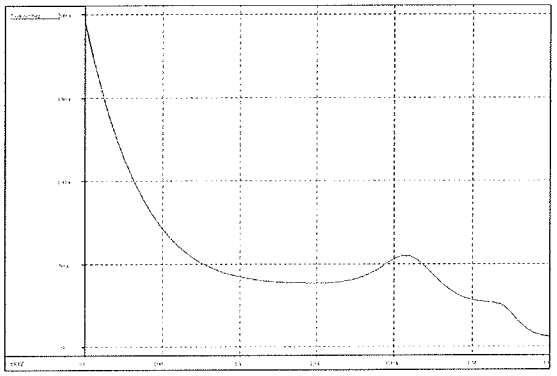

Figure 6: Output noise voltage on the AFE channel

channel should be $0{,}1024V_p$, which requires at least a $1{,}024\mu A_p$ photocurrent. This means the *rms* photodiode current noise level must be below 2nA. For the above calculation, only the electronic noise was counted. But there is also an edge effect from the coded plate, a light modulation effect, light bends on the patterns' edges of the measuring plate (small hole dimensions), a non-constant dark current, a leakage current, etc. Taking into account all these effects, a margin of 4 is estimated to be sufficient. To calculate the minimum comparator's hysteresis and therefore the minimum required photodiode signal current, the expected comparator's offset voltage has to be considered, too. For an interpolation factor of 40, an additional margin is not required and a $4uA_p$ photodiode current is sufficient.

4. Opto-electronic system characteristics

The photodiode operating reverse voltage is always mid supply level, that increases the diode capacitance and slightly reduces the diode noise. Separate optical measurements were done using reverse diode voltage of 5V (P+P/N) /3/.

- Supply voltage: 3V (min), 5V (nom)
- Supply current: 6mA
- Photodiode current: 1mA (min), 20mA (max)
- Photodiode responsivity 0.52A/W
- Photodiode peak wavelength 820nm
- Photodiode capacity @ -5V 19pF
- Photodiode Q.E. 80%
- Photodiode reverse current @-5V 200pA
- Operating frequency range: DC to 200kHz
- S/N ratio: 62dB (AFE)
- Common-mode signal rejection: -64dB
- Resolution: 9 bit(AFE)
- Technology: 2μm, p-well CMOS
- Programmable division factors: 2, 4, 8, 20, 40
- Balance voltage internally generated requires external capacitor, min 100nF.

- Max internal delay: 20nsec
- Absolute interpolator error: below 0.5°

5. OAFE transimpedance channel characteristics

- Fully differential topology
- Low noise
- Short recovery time
- Large dynamic range
- Operating point control
- Upper corner frequency independent on optosensor capacitance
- Offset regulation
- Phase control
- Programmable gain
- DC and DARK current compensation

6. Layout constrains

The geometry of the combined *ASIC* has the *PADs* for the external connection placed away from the optodevices' area. Fig.7 shows the microphotograph of the chip. Only test pads may be placed close to or in the illuminated area. This separation is also good for better positioning of the external mask patterns.

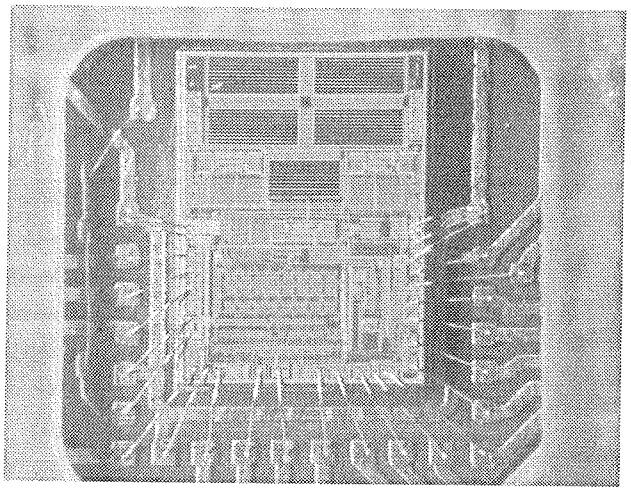

Figure 7: *ASIC die including opto-array*

The photodiodes' structure that we used was a P/N diode (p-well/n-substrate). P+ diffusion strips with narrow *metal1* and *metal2* aluminum layers were also used to reduce the surface resistivity of the diode. The same was done for better substrate conductivity. P+ diffusion therefore reduces the response time, while the sensitivity versus wavelength remains unchanged (P+ mostly covered by aluminum). The stripped diodes (*1500μm long*) and the movement of the external mask have the same orientation. This means that all stripped diodes are illuminated simultaneously and the generated current is an integral over *dx* along the diodes.

7. Conclusions

The proposed system needs to be optimized on high common mode rejection on input. Due to P+P/N substrate diodes and conversion to differential output signal, the effective generated signal is reduced by 6dB.

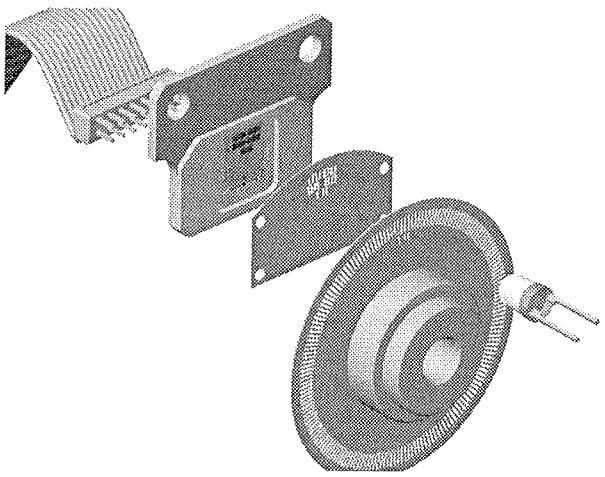

Figure 8: *Opto-ASIC in rotary-incremental application*

Optical shielding is used between the diodes (polysilicon, metal layers). Because there are no bonds on the optical area the minimum distance (*d*) of the monitoring pattern plate (glass) to the *ASIC* surface can be expressed as:

$d \leq \frac{1}{2} \cdot P / \lambda$ where P is the period size (pattern to pattern) and λ is the wavelength (820nm).

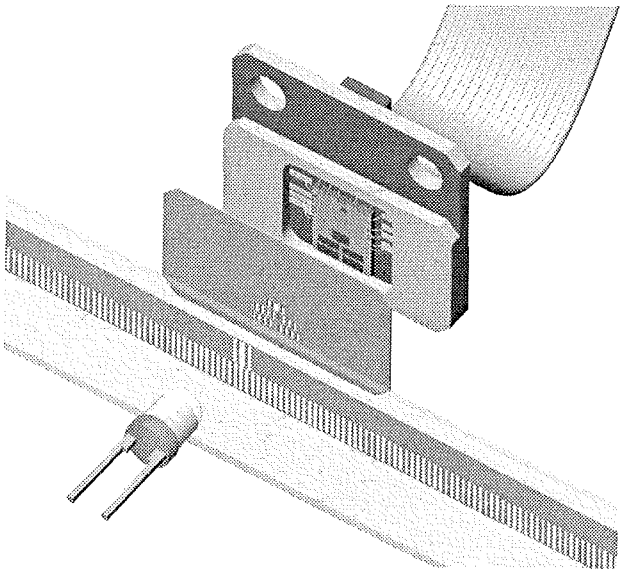

Figure 9: *Opto-ASIC in linear-incremental-position application*

The test using a microstrip raster formed by both aluminum layers was expected to be used instead of a receiving coded plate. The advantages of the integrated diodes and the proposed PAD position are that the distance (d) of the patterned glass from the *ASIC* surface can be reduced almost to zero. Using patterned glass above the die overrides the integrated strips, which makes the system more flexible.

The next important result is the noise figure for the overall integrated electro-optical system. This was measured with different illumination (LED diodes). If this noise is evaluated and calculated as a noise current to the diode terminals, the possible minimum illumination can be found. This value is close to the expected 3nA peak on input. The larger measured value is due to the noise contribution of the analog output buffer. The measured results printed in chapter IV showed behavior of the integrated system and of the opto-elements separately.

The temperature characteristics of the photoeffect are not so important as the dark current of the P+P/N integrated diodes /3/. This current increases rapidly with temperature. In our case, the voltage on the diode is not close to zero and therefore the increasing leakage with temperature is not negligible. A possible solution could be a continuous offset cancellation using a *dummy DARK* optochannel. As can be clearly seen from Fig.2, the *DARK* and the *common-mode DC* components are canceled out by means of a floating input common-mode level. All the diodes need to be matched. Along with the phase matching this is a big advantage of the designed analog front end (AFE).

All the designed ASICs are used in RLS incremental linear and rotary encoders (Fig. 10). They are available also as modular COB component.

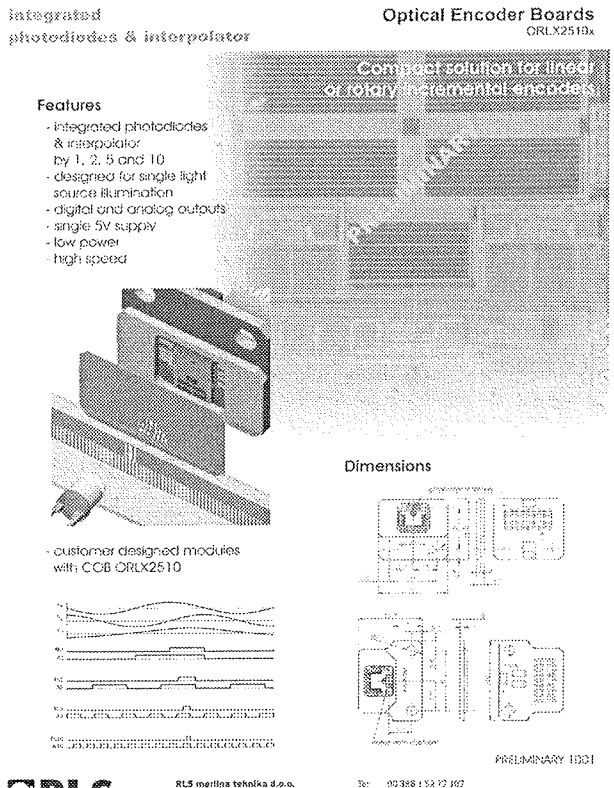

Figure 10: *Opto-ASIC microsystem and application*

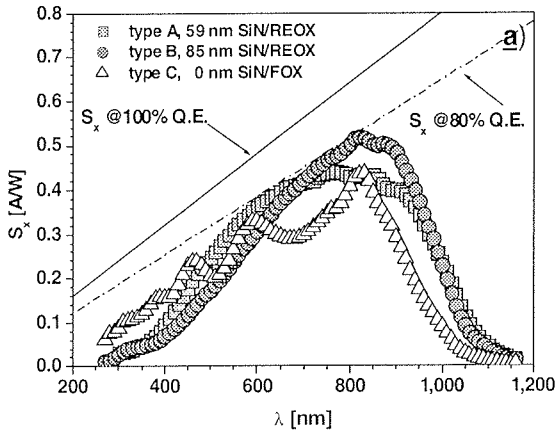

Figure 11: *Measured spectral response of the diodes*

Only one additional mask for the antireflection coating of 85nm of the Si_3N_4 with refracted index of 1.98-2.02 was finally added to the standard CMOS process. The size of the integrated diode is *600μm x 1500μm* with a peak responsivity of *0.52A/W* at *820nm* (Fig. 11).

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References

/1/ P.Aubert, H.J.Ogney, R.Vuilleumier, "Monolithic Optical Position Encoder with On-chip Photodiodes", *IEEE Journal of Solid State Circuits, Vol.23, No.2*, April 1988, pp465-473

/2/ R. Kanert, W.Budde, A.Kalz, "A Monolithic Field Segment Photo Sensor System", *IEEE Journal of Solid State Circuits, Vol.30, No.7*, July 1995, pp 807-811

/3/ M. Maček, "On-Chip Photodiodes for Monolithic Optical Position Encoder", *Proceedings of the 37th International Conference on Microelectronics, Devices and Materials*, pp 225-230, 2001

/4/ A. Pleteršek, J. Trontelj, "Integrated Optical Motion Detection Microsystems with Programmable Resolution", *Proceedings of SPIE, MOEMS and Miniaturized Systems*, Santa Clara, USA, pp 403-410, 2000

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