

# Application of Direct Current Control in a Three-phase Parallel Active Power Filter

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**Abstract.** The paper presents application of a direct current control (DCC) method in a three-phase parallel active power filter. The shunt active power filter is employed to compensate the fundamental reactive power and harmonic distortion of non-linear loads. Due to its inverter-like topology with known parameters in the filter branch, the predictive DCC method was implemented to reduce the filter commutation frequency. Consequently, the filter branch losses are decreased. Experimental setup based on a TMS320F2407A DSP showed that the DCC variant without modulation within the sampling interval yields even better results than the DCC variant, which modulates the active and zero voltage vectors within the sampling interval. A comparison between the DCC and the synchronized on-off control method indicates that the DCC improves the filter performance.

**Keywords:** shunt active power filter, current control, harmonics, modulation, reactive power

## Uporaba neposredne regulacije toka pri trifaznem paralelnem aktivnem močnostnem filtru

**Povzetek.** V članku je predstavljena uporaba metode neposredne regulacije toka (angl. Direct Current Control – DCC) pri trifaznem paralelnem aktivnem močnostnem filtru. Paralelni aktivni močnostni filter je namenjen kompenzaciji osnovne jalove moči in harmonskega popačenja, ki nastaja kot posledica nelinearnih bremen. Po topologiji je filter podoben razsmerniku in ker so parametri vezja v filtrski veji znani, lahko filter vodimo s prediktivno metodo neposredne regulacije toka (DCC), s čimer se zniža preklopna frekvenca, posledično pa se zmanjšajo tudi izgube v filtrski veji. Poskuse smo opravili na laboratorijskem modelu filtra, ki je voden z DSP krmilnikom TMS320F2407A. Glede dosežene stikalne frekvence in harmonskega popačenja so rezultati meritev, pridobljeni z uporabo različice DCC brez dodatne modulacije, celo boljši kot pri različici DCC, pri kateri se izbrani aktivni in ničelni napetostni vektor modulirata znotraj vzorčnega časa. V primerjavi s klasičnim časovno-diskretnim načinom regulacije toka pa pri delovanju aktivnega močnostnega filtra obe različici DCC izkazujeta boljše rezultate.

**Ključne besede:** paralelni aktivni močnostni filter, regulacija toka, harmonsko popačenje, modulacija, jalova moč

### 1 Introduction

The wide use of power electronics, e.g. rectifiers in home and office appliances as well as in industrial devices, gives rise to the reduced power factor and

harmonic distortion in the supply grid. The applicable standards lay down rigorous limits for harmonic distortion, thus trying to provide quality of electrical power to consumers.

A solution to meet the quality requirements, besides proper design of power electronics devices, is active power filter. When connected in parallel with a load, an active power filter can compensate – not only the fundamental reactive power due to the lag between the phase voltage and phase current – but the load current harmonic distortion as well [1-3]. It can also provide a balanced load in three-phase systems [4, 5].

A topology similar to the one in the voltage-source inverter can be used for an active power filter, thus providing proper compensating currents in the filter branch. The filter current reference can be established according to the compensation requirements in many different ways [6-10]. Their advantages are in features like data acquisition and processing simplicity, dynamic response to load current variation, sensitivity to line voltage disturbances, etc. Consequently, various current control approaches are possible, like synchronized on-off principle [2] and space vector modulation – SVM [11].

Current control should provide good tracing of the filter current to its reference value, with minimal ripple and the lowest possible commutation frequency to minimize the switching losses. The requirements are contradictory. Since the filter current waveform consists of high-order harmonics, an attempt was made to

implement a direct current control (DCC) method. Previously, the DCC method was successfully tested in a classical VSI-based AC current source [12] and later, with some upgrade, in induction motor control [13], where the method faces the back-EMF phenomenon.

Preliminary results of the DCC method application in active power filters were reported [14], therefore in this paper, after a brief explanation of the active power filter 3-phase 3-wire topology and the applied method of filter current reference determination, a summary of the DCC principle will be presented. After a description of the experimental setup, the obtained compensation results will be shown and discussed.

## 2 Parallel Active Power Filter

### 2.1 Topology and Principle

A configuration of a parallel active power filter for three-phase three-wire loads is shown in Figure 1.

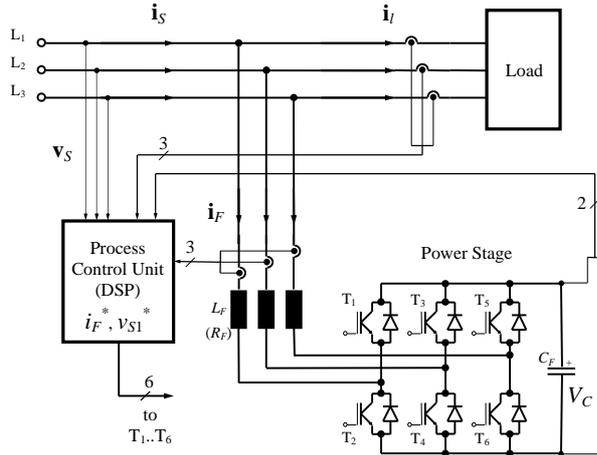


Figure 1. Three-phase three-wire parallel active power filter.

According to the selected compensation strategy, the filter can compensate the fundamental reactive power and/or load current harmonic distortion by enforcing an appropriate current into the filter branch:

$$i_{F(1,2,3)} = i_{S(1,2,3)} - i_{L(1,2,3)}. \quad (1)$$

The inverter-like topology in the filter power stage can provide the required filter current only when the filter capacitor voltage  $V_C$  exceeds the instantaneous value of supply line voltage  $v_S$ . Consequently, the capacitor voltage has to be controlled, as well. Also, if there is no capacitor voltage control, the capacitor voltage might decrease or increase due to an inevitable unbalance in the active power flow from the supply grid to the load. On the other hand, the capacitor voltage affects the filter current ripple; for a constant capacitor voltage the highest ripple is expected when the line voltage crosses zero. Therefore, the capacitor voltage is an important issue in filter design and some approaches try to avoid

this effect by varying the capacitor voltage in accordance with the line voltage [15].

### 2.2 Filter Current Reference

There have been several methods of current reference determination developed for the parallel active power filters. Some of these methods can be applied in single-phase filters. Others are suitable only for three-phase systems, and some can be used both for single-phase and three-phase topologies. An advantage of the method can be its ability to perform various compensation strategies, i.e. separate compensation of the fundamental reactive power and/or the harmonic distortion. The methods can be further estimated through a number of quantities required to be sensed and processed (load currents, line voltages, line currents, phase shifts, etc.). Another important issue is the dynamics of the method. It is the response of the filter current reference to variations in the load parameters. The methods can be also valued by their sensitivity to various disturbances, especially those of the line voltage. They are decisive for the filter synchronization to the line voltage.

In this paper, a three-phase three-wire topology of an active power filter is considered. The aim is to compensate both the fundamental reactive power and the harmonic distortion. Furthermore, line currents are required to be sinusoidal, so the filter-load system should behave like a resistive load with resistance

$$R_{(1,2,3)}^* (t) = \frac{v_{S1(1,2,3)}(t)}{i_{S(1,2,3)}(t)}, \quad (2)$$

with  $v_{S1(1,2,3)}$  being the line voltage fundamental for each phase, which provides the sinusoidal waveform of the line current. This line voltage fundamental can be calculated as

$$v_{S1}^* (t) = A_1^* (t) \sin(\omega^* t) + B_1^* (t) \cos(\omega^* t), \quad (3)$$

where the fundamental Fourier coefficients are

$$A_1^* (t) = \frac{2}{T^*} \int_{t-T^*}^t v_S(\tau) \sin(\omega^* \tau) d\tau, \quad (4)$$

and

$$B_1^* (t) = \frac{2}{T^*} \int_{t-T^*}^t v_S(\tau) \cos(\omega^* \tau) d\tau. \quad (5)$$

The assumed line cycle given above is denoted with  $T^*$ . It has been proved, that sine and cosine in (3)–(5) do not need any special synchronization to the line voltage when the assumed supply grid frequency  $\omega^*$  differs from the actual supply grid frequency  $\omega$  for less than 0.5 % [2]. In this case, synchronization is provided by calculated line voltage fundamental  $v_{S1}^*$ .

If the power losses are neglected, there should be no active power in the filter branch:

$$P_{F(1,2,3)} (t) = \frac{1}{T} \int_{t-T}^t v_{S(1,2,3)}(\tau) \cdot i_{F(1,2,3)}(\tau) \cdot d\tau = 0. \quad (6)$$

With an additional requirement for balanced line currents, symmetrical substitutive resistance can be calculated:

$$R^*(t) = R_{(1)}^*(t) = R_{(2)}^*(t) = R_{(3)}^*(t), \quad (7)$$

$$R^* = \frac{\int_{t-T^*}^t v_{S(1)}^2 d\tau + \int_{t-T^*}^t v_{S(2)}^2 d\tau + \int_{t-T^*}^t v_{S(3)}^2 d\tau}{\int_{t-T^*}^t v_{S(1)} i_{l(1)} d\tau + \int_{t-T^*}^t v_{S(2)} i_{l(2)} d\tau + \int_{t-T^*}^t v_{S(3)} i_{l(3)} d\tau}. \quad (8)$$

The sinusoidal line current reference can now be easily obtained from (2), (3) and (8):

$$i_{S(1,2,3)}^*(t) = \frac{1}{R^*(t)} v_{S(1,2,3)}^*(t). \quad (9)$$

This finally leads to the filter current reference by using (1):

$$i_{F(1,2,3)}^*(t) = i_{S(1,2,3)}^*(t) - i_{l(1,2,3)}(t). \quad (10)$$

Therefore, the presented method of filter current reference determination requires on-line measurements of the line voltages, load currents and filter currents. As mentioned above, the filter current reference has to be also controlled to provide the constant filter capacitor voltage. Consequently, the filter capacitor voltage has to be measured, too.

### 3 Direct Current Control (DCC)

In voltage-source inverters with the topologies similar to the presented active power filter, various current control principles can be applied. The aim of current control is to generate appropriate triggering pulses for the power stage transistors ( $T_1$ – $T_6$ ). Consequently, the actual filter currents  $i_{F(1,2,3)}$  should follow their reference values  $i_{F(1,2,3)}^*$  with the smallest possible error. Besides the small current ripple, a low commutation frequency of the power stage transistors is required to minimize the switching losses.

In the previous work, the synchronized on-off current control principle was used in the active power filters, since its implementation on slower microcontrollers was easier than the space vector modulation and its commutation frequency is a bit lower. On the other hand, a drawback of the synchronized on-off approach in the three-phase topology hides in its incapability to impress a zero voltage vector, yielding to higher current ripple.

A solution to this issue is the proposed predictive approach to current control [12]. It enables impressing a zero voltage vector for the entire sampling interval  $\Delta t$  or, in its more sophisticated variant, for a precalculated subinterval  $t_{on} < \Delta t$ . This method, called the Direct Current Control (DCC) method, gives some encouraging results in AC sources and in induction motor control. It might also be advantageous in active

power filters, since the relevant parameters in the filter branch ( $L_F$ ,  $R_F$ ) are known.

In the first DCC variant, for each sampling interval either an active voltage vector or a zero voltage vector can be impressed. The decision is based on the lower predicted filter current error. The predicted filter current vector  $\mathbf{i}_F$  at the end of the sampling interval  $\Delta t$  can be written as

$$\mathbf{i}_F(n+1) = \mathbf{i}_{F0}(n+1) + \mathbf{v}_F(n) \cdot \frac{\Delta t}{L_F} \quad (11)$$

where

$$\mathbf{i}_{F0}(n+1) = \mathbf{i}_F(n) \left( 1 - \frac{R_F \Delta t}{L_F} \right) + \mathbf{v}_S(n) \cdot \frac{\Delta t}{L_F} \quad (12)$$

represents the predicted filter current at the end of the sampling interval, without applying any filter active voltage vector  $\mathbf{v}_F$ , but taking into account the line voltage vector  $\mathbf{v}_S$  at the beginning of the sampling interval.

After impressing the filter active voltage vector  $\mathbf{v}_F$  ( $\mathbf{v}_F$  is one of the six possible active vectors  $\mathbf{v}_1 - \mathbf{v}_6$ )

$$\mathbf{v}_F(n) = V_C \cdot \begin{bmatrix} K_{va}(n) \\ K_{vb}(n) \end{bmatrix} = V_C \cdot \begin{bmatrix} \frac{2}{3} & \frac{1}{3} & \frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \cdot \begin{bmatrix} s_1(n) \\ s_3(n) \\ s_5(n) \end{bmatrix}, \quad (13)$$

where  $s_1$ ,  $s_3$  and  $s_5$  are the corresponding transistor states (0 or 1), the predicted filter current error at the end of the sampling interval is

$$\boldsymbol{\varepsilon}_V(n+1) = \mathbf{i}_F^*(n+1) - \mathbf{i}_{F0}(n+1) - \mathbf{v}_F(n) \cdot \frac{\Delta t}{L_F}. \quad (14)$$

On the other hand, the predicted filter current error for a zero voltage vector is

$$\boldsymbol{\varepsilon}_0(n+1) = \mathbf{i}_F^*(n+1) - \mathbf{i}_{F0}(n+1) \quad (15)$$

Both predicted errors (14) and (15) have to be calculated and their magnitudes compared. A practical criterion for applying an active voltage vector is:

$$\frac{2 V_C \Delta t}{9 L_F} < \boldsymbol{\varepsilon}_{0a}(n+1) \cdot K_{va}(n) + \boldsymbol{\varepsilon}_{0b}(n+1) \cdot K_{vb}(n), \quad (16)$$

where  $\boldsymbol{\varepsilon}_{0a}(n+1)$  and  $\boldsymbol{\varepsilon}_{0b}(n+1)$  are the components of predicted current error  $\boldsymbol{\varepsilon}_0(n+1)$  in the stationary reference frame.

The example shown in Figure 2 indicates both current errors with superscript  $I$ . In this particular case, the magnitude of the predicted filter current error for a zero voltage vector ( $\boldsymbol{\varepsilon}_0$ ) is smaller than the magnitude of the predicted error for an active voltage vector ( $\boldsymbol{\varepsilon}_V$  for  $\mathbf{v}_3$ ), therefore a zero voltage vector should be selected.

The second DCC approach requires impressing an active voltage vector for a subinterval  $t_{on}$  within the sampling interval  $\Delta t$ ; a zero voltage vector is impressed for the remaining time of the sampling interval. Thus, the predicted filter current error at the end of the sampling interval can be written as (11):

$$\boldsymbol{\varepsilon}_V(n+1) = \mathbf{i}_F^*(n+1) - \mathbf{i}_{F0}(n+1) - \mathbf{v}_F(n) \cdot \frac{t_{on}}{L_F} \quad (17)$$

The expression for the duration of the "active" subinterval  $t_{on}$  is obtained by minimizing this error (17):

$$t_{on} = \frac{9L_F}{4V_C} (\varepsilon_{0a}(n+1) \cdot K_{va}(n) + \varepsilon_{0b}(n+1) \cdot K_{vb}(n)) \quad (18)$$

If the calculated  $t_{on}$  exceeds the sampling interval  $\Delta t$ , then  $t_{on}$  is set to  $\Delta t$  thus providing a simple overmodulation.

For this DCC approach, the minimized filter current error in Figure 2 is shown with superscript *II* with the active voltage vector  $v_3$  impressed for  $t_{on}$  only. Compared with the first DCC variant, a lower current ripple and increased average commutation frequency are expected. On the other hand, the dead-time compensation can be implemented easily.

#### 4 Experimental Setup and Results

The active power filter with DCC was tested on a laboratory model. It was built with Semikron SKM75GB123D IGBT modules and  $C_F = 1000 \mu\text{F}$ ,  $L_F = 2.6 \text{ mH}$ ,  $R_F = 90 \text{ m}\Omega$ . During the experiments, the supply grid line-to-neutral voltage  $V_S$  was 230 V (RMS) and the filter capacitor voltage  $V_C$  was controlled to 720 V. The Process Control Unit (Figure 1) is based on a TMS320F2407A DSP controller with six additional fast two-channel AD converters (MAX 1314, conversion time 1.2  $\mu\text{s}/2 \text{ ch}$ ).

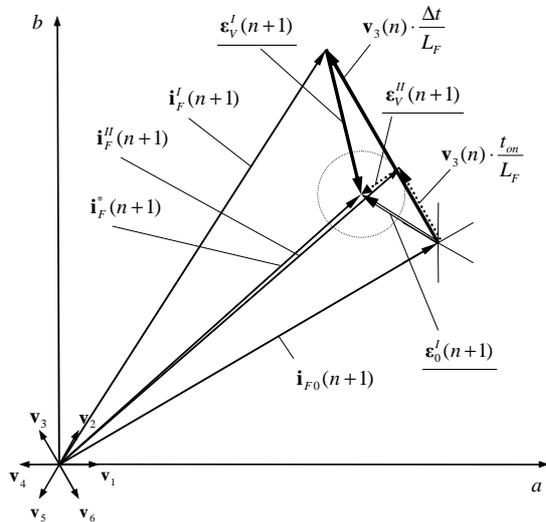


Figure 2. Comparison between predicted filter current errors for both DCC approaches (denoted with superscripts *I* and *II*)

The DSP performs all the calculations for filter current reference determination (10) and filter capacitor voltage control for 256 samples per grid cycle (20 ms); therefore the sampling interval for these tasks is 78.125  $\mu\text{s}$ . In a halved sampling interval ( $\Delta t = 39.06 \mu\text{s}$ ), it samples all the signals, executes the routines for the DCC algorithm ((16), (18)) and

consequently generates the triggering pulses for the power stage transistors ( $T_1$ – $T_6$ ).

During the tests, a single-phase thyristor rectifier was used as a nonlinear load. It was connected between two phase terminals so as to simulate unbalanced circumstances. In Figure 3, the relevant line voltage and load current signals for load transient (after 20 ms) are shown. Compensation results for the filter, controlled by synchronized on-off method, are presented in Figure 4. A fast response of the line current to the load transient is obvious as well as its sinusoidal form, but the comparison with similar results for the other control methods (DCC I: Figure 5, DCC II: Figure 6) can be better seen from the frequency spectra in Figure 7. The first diagram (Figure 7 a) shows the load current spectrum. In the second diagram (Figure 7 b), the spectrum for the line current, obtained with the DCC I method (grey), is superimposed to the spectrum for the synchronized on-off method (black). In general, the DCC I method yields lower harmonic contents. From Figure 7 c it can be seen that the DCC II method contains even less harmonics. The line current THD was calculated, also for all the tested methods in steady state (Table I), by taking into account 25 harmonics. Surprisingly, the first DCC method shows better performance than the second one. Namely, the latter causes a sort of an asymmetric filter current ripple [12] that decreases compensation capabilities for the fifth and the seventh line current harmonic.

Considering the switching losses, an additional objective was minimization of the actual switching frequency. Classical SVM control in the same three-leg VSI topology would have two commutations (state changes) per sampling interval for each transistor, regardless of the load conditions. With the applied sampling frequency of 25.6 kHz ( $\Delta t = 39.06 \mu\text{s}$ ), this would result in the transistor commutation frequency of 51.2 kHz.

In the synchronized on-off method and in both DCC methods, the actual switching frequency depends on the load conditions. Therefore, the number of all transistor commutations during the 100 ms load transient, presented in Figures 3-6, was evaluated. Results obtained with the various investigated current control methods are shown in Table II.

As expected, the transistor commutation frequency takes the highest value with SVM. That is why SVM usually operates at a lower sampling frequency. For both DCC methods, further efforts were made in the algorithm to reduce the number of commutations by optimal zero voltage vector selection (either  $v_0$  or  $v_7$ ). Consequently, the advantage in the reduced commutation frequency of the first DCC variant over the synchronized on-off method is evident. A higher commutation frequency for the second DCC variant was foreseen, but it does not help reducing the line current THD.

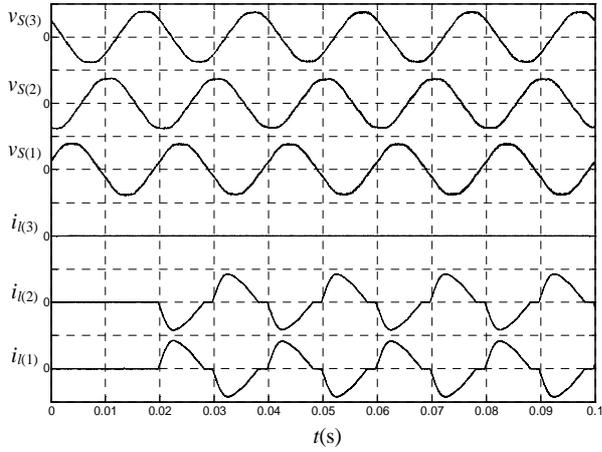


Figure 3. Line voltages ( $v_{S(1)}$ ,  $v_{S(2)}$ ,  $v_{S(3)}$ ) and load currents ( $i_{l(1)}$ ,  $i_{l(2)}$ ,  $i_{l(3)}$ ) during the load transient ( $k_v = 400$  V/div,  $k_i = 50$  A/div).

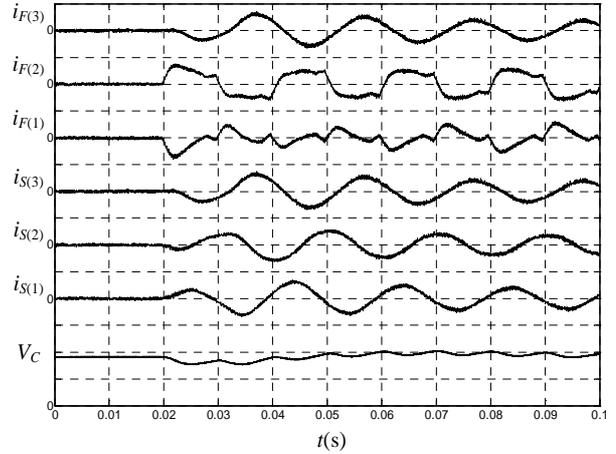


Figure 5. First DCC method: filter currents ( $i_{F(1)}$ ,  $i_{F(2)}$ ,  $i_{F(3)}$ ), compensated line currents ( $i_{S(1)}$ ,  $i_{S(2)}$ ,  $i_{S(3)}$ ) and filter capacitor voltage ( $V_C$ ) during the load transient ( $k_v = 400$  V/div,  $k_i = 50$  A/div).

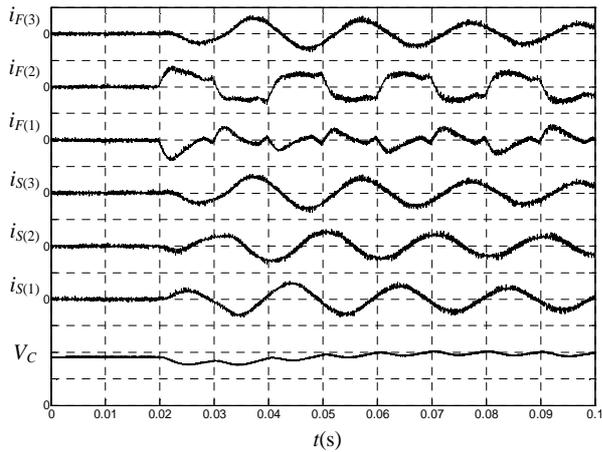


Figure 4. Synchronized ON-OFF method: filter currents ( $i_{F(1)}$ ,  $i_{F(2)}$ ,  $i_{F(3)}$ ), compensated line currents ( $i_{S(1)}$ ,  $i_{S(2)}$ ,  $i_{S(3)}$ ) and filter capacitor voltage ( $V_C$ ) during the load transient ( $k_v = 400$  V/div,  $k_i = 50$  A/div).

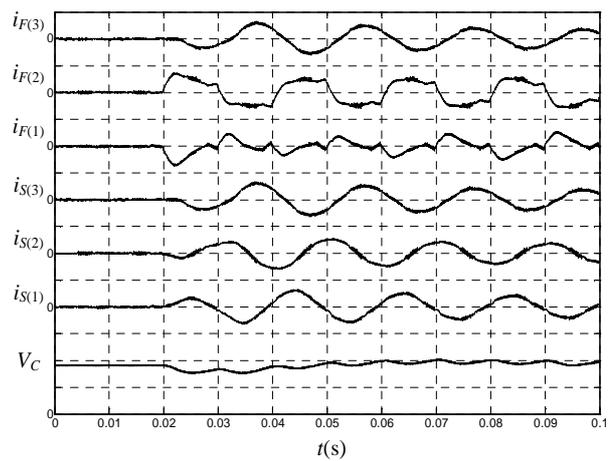


Figure 6. Second DCC method: filter currents ( $i_{F(1)}$ ,  $i_{F(2)}$ ,  $i_{F(3)}$ ), compensated line currents ( $i_{S(1)}$ ,  $i_{S(2)}$ ,  $i_{S(3)}$ ) and filter capacitor voltage ( $V_C$ ) during the load transient ( $k_v = 400$  V/div,  $k_i = 50$  A/div).

TABLE I. TOTAL HARMONIC DISTORTION OF STEADY STATE LINE CURRENT

Current control method	THD
No compensation (i.e. load current)	21.3 %
Synchronized on-off	5.0 %
DCC I	3.9 %
DCC II	5.3 %

TABLE II. TRANSISTOR COMMUTATION FREQUENCY

Current control method	Number of all commutations during 100 ms transient	Commutation frequency for each transistor
Synchronized on-off	7386	12310 Hz
DCC I	6224	10373 Hz
DCC II	9592	15987 Hz
SVM	30720	51200 Hz

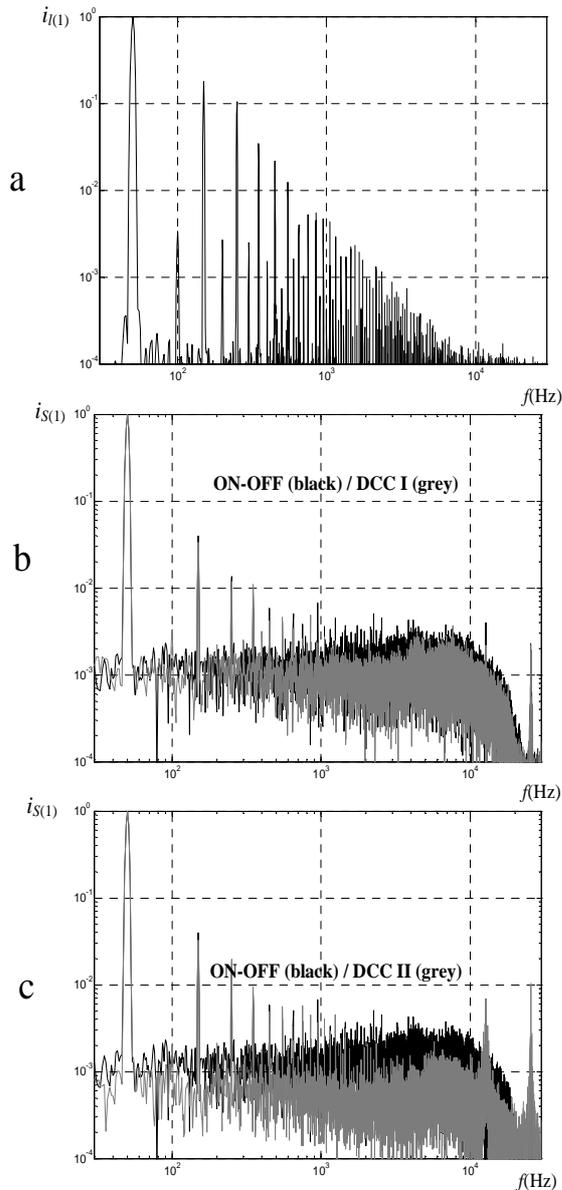


Figure 7. Compared frequency spectra for normalized load current ( $i_{l(1)}$ ) and for normalized line current ( $i_{s(1)}$ ) obtained with the synchronized on-off method and with both DCC methods (I and II).

## 5 Conclusion

The proposed direct current control (DCC) method was successfully implemented in an active power filter. Due to its predictive approach, the consequent line current ripple was reduced. Its commutation frequency for the first DCC approach is lower than in the synchronized on-off current control principle. The commutation frequency in the second DCC approach with modulation is higher but still lower than in SVM. Despite assuring outstanding performance in AC drive applications, the main drawback of the second DCC method in active

power filters remains its immanent asymmetric current ripple. The main focus of our further research will be on this issue. Also to be considered is the DCC application in the methods of filter current reference determination with a reduced number of current sensors. Also, solutions with a variable filter capacitor voltage will be investigated, to reduce the current ripple when the line voltage crosses zero.

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