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Editorial | Uvodnik

Dear reader,

Year 2018 almost ran out and this editorial brings up some statistics about manuscripts submitted. In 2018 we have received more than 180 manuscripts, out of which only 23 have been accepted for publication and more than 140 manuscript were rejected. The number of manuscripts that are out of our journal's scope has been drastically reduced. In 2018 we published 26 original scientific papers. The success rate remains below 15% in 2018 and reflects determination for quality that will path long-term quality growth. Citation metrics (JCR IF-2017=0.476, SNIP-2017=0.265 and CiteScore-2017=0,61) is one of the performance indicators. I sincerely thank all reviewers and Editorial Board Members for their valuable contribution to the journal quality growth.

In light of quality growth, we introduce a digital object identifier (DOI) to all papers in this issue for the first time. We sincerely hope that DOI will help us in wider dissemination and path to the open access publishing, which is planned already for the next volume, starting with the first issue of the volume 49.

December is time for recognition and celebration, not only in Slovenian science arena but also elsewhere. We are happy to congratulate Dr. Tadej ROJAC to be honoured with the "Zoisovo priznanje" – the Zois Certificate of Recognition as the second highest Award of the Republic of Slovenia for Scientific and Research Achievements – that he received for important achievements in research of the synthesis and characterization of high-temperature piezoelectric ceramics based on bismuth ferrite.

Let the festive days bring joy and peace in each home, office or research laboratory. It is the time to look ahead and make plans for the coming year. This brings me to editorial wishes for 2018. As a part of your success we look forward to receiving your future manuscript(s) on our submission page (http://ojs.midem-drustvo.si/).

Merry Christmas and a Happy, Healthy and Prosperous New Year!

Prof. Marko Topič
Editor-in-Chief

P.S.
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Proficient Static RAM design using Sleepy Keeper Leakage Control Transistor & PT-Decoder for handheld application

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Abstract: Due to their large storage capacity and small access time static random access memory (SRAM) has become a vital part in numerous VLSI chips. Low power adequate memory configuration is a standout among the most challenging issues in SRAM design. As the technology node scaling down, leakage power utilization has turned into a noteworthy issue. In this paper a novel power gating technique, namely sleepy keeper leakage control transistor technique (SK-LCT) is proposed for a handheld gadget application. The SRAM architecture has two primary components, specifically SRAM cell and sense amplifier. The proposed SK-LCT technique is applied in both SRAM cell and sense amplifier for a new low power high speed SRAM architecture design. The outline of SRAM architecture utilizing pass transistor decoder (PT-Decoder) gives better outcomes in term of power. Simulation is done using Tanner EDA tool in 180nm technology and the results demonstrate a noteworthy change in leakage power utilization and speed.

Keywords: SRAM; SK-LCT Technique; sense amplifier; Tanner EDA; Leakage Power

Načrtovanje učinkovitega statičenega RAMa z uporabo tranzistorja za kontrolo uhajalne moči z ohranjanjem stanja in PT dekoderja za ročne aplikacije

Izvleček: Zaradi visoke pomnilne kapacitete in kratkih dostopnih časov so statični pomnilniki z naključnim dostopom (SRAM) postali bistveni del VLSI čipov. Nizka moč zadostne konfiguracije pomnilnika je ena od najzahtevnejših problemov v zasnovi SRAM. V članku je predstavljena nova tehnika uporabe tranzistorja za nadzor uhajanja moči z ohranjanjem stanja (SK-LCT) za uporabo v ročnih aplikacijah. Arhitektura SRAM ima dve primarni komponenti, SRAM calico in tipalni ojačevalnik. Predlagana tehnika SK-LCT se uporablja tako v celici SRAM kakor v tipalnem ojačevalniku za novo zasnovano arhitekturo SRAM z nizko močjo. Okvir arhitekture SRAM, ki uporablja prehodni tranzistorski dekoder (PT-dekoder), ki daje boljše rezultate v smislu moči. Simulacija se izvaja z orodjem Tanner EDA v tehnologiji 180 nm, rezultati pa kažejo na opazno spremembo v kontroli uhajanja in hitrosti.

Ključne besede: SRAM; SK-LCT tehnika; tipalni ojačevalnik; Tanner EDA; uhajalna moč

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1 Introduction

Very Large Scale Integration (VLSI) is the way towards incorporating a million of transistors inside a single microchip. Quick advancement in the VLSI design process brings about the expansion of densities of the integrated circuit [1]. With the progression of innovation that are occurring in the universe, the demand for large storage of data is increasing in a way that needs to be faster than the current advancement [2]. At the same time, increment of power dissipation has ended up the major impediment against the further advancement of VLSI circuits. In a computing framework, power utilization because of the memory gets to frequently constitute a prevailing part of the aggregate power utilization [3].

Static Random Access Memory (SRAM) is a critical part in the vast majority of the VLSI chips; it regularly expends a prevailing part of power in each chip. By decreasing the power of SRAM, the overall power of chips can be diminished. Because of the quadratic connection amongst power and supply voltage of transistors [4]; one of the most compelling strategies to diminish the power utilization is by lessening the supply voltage. The strong demand of SRAM memory in handheld gadgets, system on-chip (SoC) & high performance VLSI circuits, the reduction of power utilization is imperative. Owing to high bit-line swing requirement, the leakage power utilization of memory circuit is high. Sleep technique, stack technique, sleepy stack technique, sleepy keeper technique, lector technique, foot switch technique & double switch technique are probably the most regularly utilized power gating for leakage power reduction. To overcome the drawback of the above existing method, a novel strategy is recommended. In computerized frameworks, instructions are conveyed by means of binary levels. The decoder is broadly utilized in memory framework to change over n-bit twofold input code into m yield lines. The address input code from the central processor is utilized to trigger the memory storage location assigned by address code [5].

Low power consumption is essentially crucial parameter, so pass transistor based decoders have been used due to the low leakage and dynamic switching currents. Among the overall power consumption of memory circuit, static power dissipation plays an predominant role. (2) A novel power gating technique, namely SK-LCT technique (Sleepy keeper Leakage Control Transistor Technique) is proposed in order to reduce the static power dissipation. SK-LCT technique is the combination of sleepy keeper and LECTOR technique which is employed in the design of SRAM cell and sense amplifier. The SRAM architecture using a SK-LCT method and pass transistor decoder (PT-decoder) has several advantages over the ordinary SRAM's design with high speed and low power consumption. (1)

2 Literature survey

During standby mode, a large portion of the power is squandered in SRAM design; since leakage power maneuvers an overwhelming part in SRAM power utilization. SRAM cell, sense amplifier & decoder are the indispensable portion of memory design. Improper design of these elements contributes to influence the robustness of the memory device. Both memory access time and memory power dissipation are emphatically affected by a sense amplifier circuitry. The power gating technique such as sleep technique, stack technique, sleepy stack technique, sleepy keeper technique & lector technique are utilized to shrink the static power of the SRAM cell. In order to diminish leakage power & delay of sense amplifier; latch-type sense amplifier is designed using a foot switch technique & double switch Technique.

In sleep technique, "PMOS-S" sleep transistor is embedded between VDD & pull up network and "NMOS-S BAR" sleep transistor is embedded between the pull down network & ground. The wake up time of the sleep method has a considerable impact on the competence of the circuit [6]. Stack technique is state maintenance technique with the detriment of increased delay and area [7]. The divided transistor of sleepy stack technique increases the delay drastically & also limits the convenience of this technique [8]. In Sleepy Keeper Technique parallel connected PMOS and NMOS transistor is embedded between pull up network & VDD and pull down network & ground. Lector technique has two leakage control transistors (LCT1 &LCT2) which are inserted between the pull up & pull down network. It has a very low leakage power which results in a delay penalty [9]. The data retention issue occurs in the circuit, which can be minimized by placing sleep transistor [10].

The footer switch voltage latch sense amplifier (FS-VLSA) senses the voltage difference between the bit line voltage & bit line bar voltage and amplifies it to rail yield voltages. The footer switch current latch sense amplifier (FS-CLSA) senses the current difference produced by ΔVBL and amplifies it. By introducing an extra head switch (i.e. Double Switch PMOS Access & Double Switch NMOS Access) the invalid current paths in FS-VLSA can be expelled which introducing a complementary sense enable signal. Double switch transmission access-voltage latch sense amplifier (DSTA-VLSA) is used to remove the sensing dead zone of the memory [11].

Based on the specific combination of input levels, the decoder is initiated. The most commonly utilized decoders in the design of SRAM architecture are AND decoder, NOR decoder, pseudo NMOS decoder. The speed of the AND decoder is more proficient than other decoders with the disadvantage of high power consumption. The design of decoder using NOR gate prompts low power consumption with increased time lag. In pseudo-NMOS decoder static power dissipation dominates the circuit.

There is an indigence of a novel power gating technique & the decoder circuitry to overcome the disadvantages of the above issue in SRAM architecture. By

appropriate outline of SRAM cell, sense amplifier & decoder; the general execution of memory design can be advanced.

3 SK-LCT technique & PT decoder

SRAM architecture comprises of SRAM cell, sense amplifier, precharge circuit, row/ column decoder and write driver circuit. A novel sleepy keeper leakage control transistor technique (SK-LCT Technique) is proposed in order to design SRAM cell and sense amplifier circuitry. The decoder using pass transistor gives better outcomes in terms of static power. The SRAM architecture for handheld gadget application is designed using the SK-LCT method and pass transistor decoder (PT-decoder) has a few favorable circumstances over the conventional SRAM's outline with high speed and low power consumption.

3.1 Sleepy Keeper Leakage Control Transistor Technique (SK-LCT Technique)

To overcome the problem in SRAM architecture, a novel SK-LCT Technique is applied. The delay & power of the SRAM architecture can be further scaled down and the data retention can be preserved using this novel technique. (3)

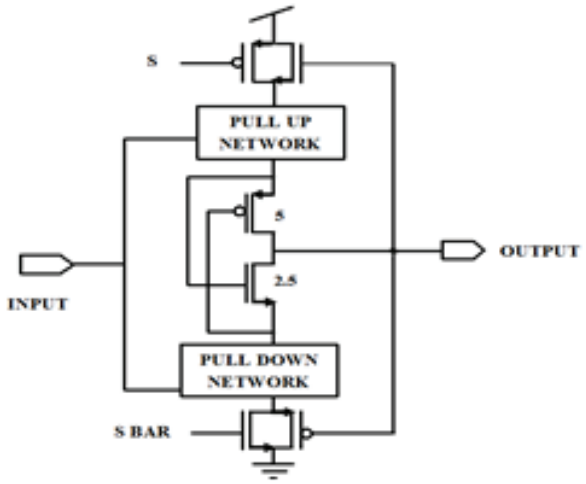

Figure1: SK-LCT Technique

Fig.1 illustrates the sleepy keeper leakage control transistor technique (SK-LCT Technique). Here, leakage control transistor (PMOS-LCT & NMOS-LCT) is placed in between pull up & pull down network. Both PMOS and NMOS are tied up parallel to preserve the stable retention in standby mode. The PMOS-LCT gate is associated with the drain of pull down network and NMOS –LCT gate is associated with the drain of pull up network. Hither, the sleep PMOS (S) transistor is put beneath VDD and sleep NMOS (S BAR) transistor is set over the ground. In sleep mode, parallel connected NMOS is the only terminal between pull up network & VDD and parallel connected PMOS is the only terminal between pull down network & ground. Sleep transistors cutoffs the power rails when the circuit is not in use while the state of circuit is saved by keeper transistors. This leads to the reduction of static power dissipation of memory circuit. The SRAM cell and sense amplifier are the two main fundamental components of SRAM Architecture; by outlining SRAM cell and sense amplifier using sleepy keeper-leakage control transistor (SK-LCT) technique low power high speed memory architecture can be obtained.

3.2 Pass Transistor Decoder (PT-Decoder)

Pass transistor decoder frequently requires less power consumption, runs faster and utilizes fewer transistors than a similar function implemented in complementary CMOS logic. The leakage power dissipation of PT-decoder is completely arrested. Fig. 2 demonstrates the pass transistor decoder.

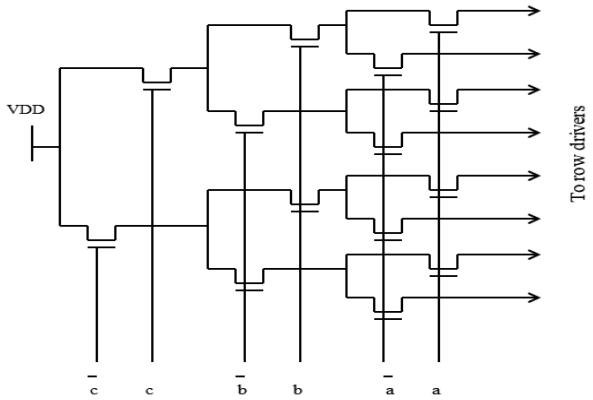

Figure 2: PT-Decoder

In memory design, the decoder is used to translate the given address and enable the particular row & column of the memory cluster. Row and column pass decoder is utilized to enable word line and write enable of a SRAM array. Based on the address line, specific memory cell is chosen and the data is read and written in the memory array.

4 Proficient static ram architecture

The low power and high speed SRAM architecture is outlined using sleepy keeper leakage control transistor (SK-LCT Technique) & pass transistor decoder. Fig. 3 illustrates the block diagram of SRAM architecture using the SK-LCT Technique & PT decoder. Initially, precharge

both the bit lines (BL & BLB) by using a precharge circuit. The storage location inside the memory devices are selected by the pass transistor decoder. By enabling the word line (WL) of the SRAM cell using PT-decoder, the data either '0' or '1' is stored. If data '1' is written in SRAM cell, BLB automatically discharges to '0' & BL remains high and vice-versa. Sense amplifier boosts the data in SRAM cell and acts as a read part circuitry. No change in the memory cell takes place during hold operation.

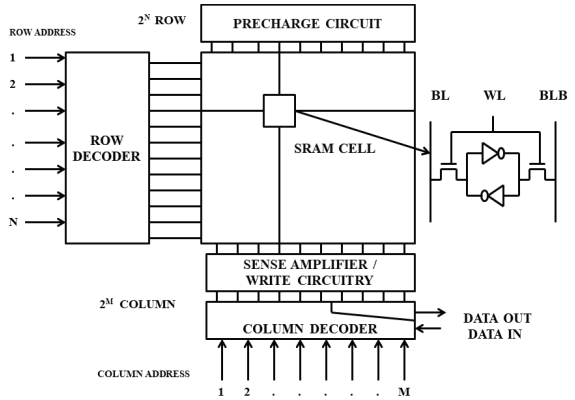

Figure 3: SRAM Architecture

Table 1 demonstrates the read and write operation of SRAM architecture. When word line (WL) and write enable circuitry (WE) is enabled, previous data is modified and new data is written in the memory. When either word Line (WL) or write enable circuitry (WE) is disabled, the previous data is hold in the memory. No change in the memory takes place during hold operation.

Table 1: Read and Write operation of SRAM

WRITE OPERATION		READ OPERATION	
WRITE '1'	Q=0, Q-bar=1 Word Line=1 Bit bar=0 Bit =1	READ '1'	Precharge both the bit lines Word line=1 Bit bar=0 (discharges to 0) Bit=1
WRITE '0'	Q=1, Q-bar=0 Word Line=1 Bit bar=1 Bit =0	READ '0'	Precharge both the bit lines Word line=1 Bit bar=1 Bit =0 (discharges to 0)

4.1 Design of SRAM cell using the SK-LCT Technique

SRAM cell is designed using the SK-LCT Technique to reduce the leakage power dissipation of memory. Fig. 4 illustrates SRAM cell the using the SK-LCT Technique. When word line (WL) is asserted high, access transistors are turned 'ON' for write operation. This connects the cell to two complementary bit lines columns (BL &BLB) and the data either '1' or '0' is written in the memory cell. When WL=0, SRAM cell is being inaccessible from both bit lines; keeping it in standby mode. This keeps prior stored value in the cell unchanged.(5)

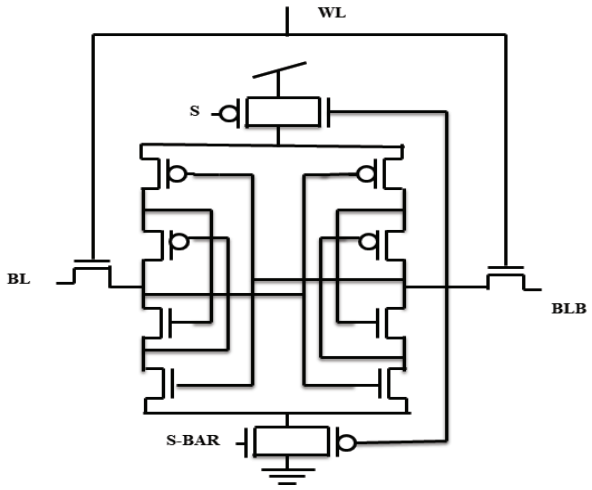

Figure 4: SRAM cell using SK-LCT Technique

4.2 Design of Sense Amplifier using the SK-LCT Technique

The power and delay of the voltage latch sense amplifier (VLSA) is reduced using SK-LCT Technique. Here, the additional transmission gate is inserted along with bit lines. During read mode, the PMOS sleep transistor(S) is activated to high and the NMOS sleep transistor(S-BAR) is activated to low; thus turning on the transmission gate and switching off the PMOS transistor whereas in standby mode the transmission gate is turned off and PMOS transistor turns on. Fig.5 illustrates voltage latch type sense amplifier using SK-LCT Technique.(6)

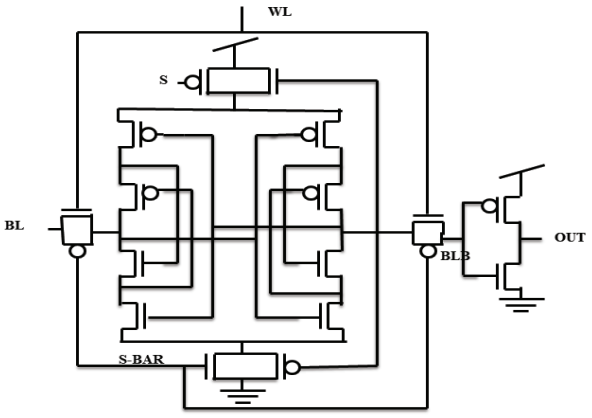

Figure 5: Sense Amplifier using SK-LCT Technique

4.3 Design of SRAM architecture using the SK-LCT Technique & PT-decoder

Fig:6 illustrates 4 bit SRAM architecture using the SK-LCT Technique and PT-decoder for handheld gadget application. Each column has a single precharge circuit in the memory array to precharge both bit lines (BL & BLB) to VDD during read and write operation. The address line of the memory is activated using row/column PT-decoder. SRAM cell using the SK-LCT Technique diminishes the leakage power dissipation of memory. When the word line (WL) is high, NMOS access transistors are turned 'ON' for write operation. This interfaces the cell to two complementary bit lines and the data either '1' or '0' is written in the memory cell. When WL=0, SRAM cell is inaccessible from both bit lines (BL & BLB). The write enable (WE) signal is turned on; when the write operation is intended. Otherwise, the WE signal isolates the bit lines from write drivers. The voltage difference between both the bit lines (BL&BLB) of voltage latch sense amplifier (VLSA) is sensed and amplifies the small voltage signal in the bit lines to conspicuous logic levels.

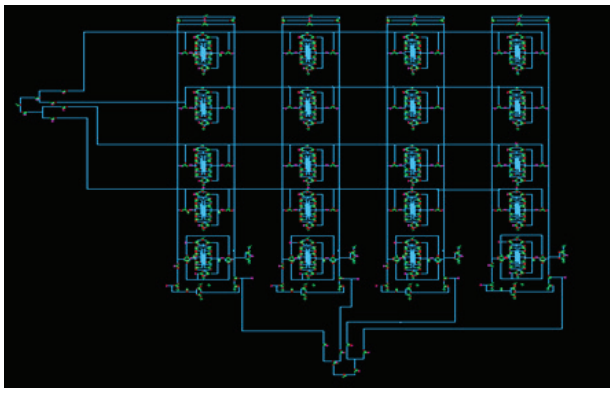

Figure 6: 16 bit SRAM architecture using SK-LCT Technique & PT-decoder

5 Results & discussion

The low power, high speed SRAM architecture is outlined using sleepy keeper leakage control transistor (SK-LCT Technique) & PT-decoder. The entire work is conveyed using Tanner EDA 180nm technology. The simulation result indicates the examination of various parameters like power consumption, leakage power and delay.

5.1 SRAM cell using the SK-LCT Technique

SRAM cell is designed using the SK-LCT technique to diminish the leakage power and improve the speed of the memory. If WL=1 and bit lines BL=1 (remains high, i.e. '1') & BLB=0 (remains low, i.e. '0'), data '1' is written in the SRAM cell. If WL=1 & bit lines BLB=1(remains high, i.e. '1') & BL=0 (remains low, i.e. '0'), data '0' is written in the SRAM cell. Fig.7 illustrates the simulation waveform of SRAM cell using the SK-LCT Technique

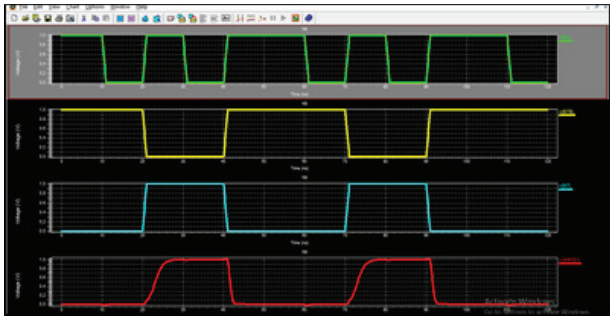

Figure 7: Simulation waveform for SRAM cell using SK-LCT Technique

Table 2 demonstrates the correlation of SRAM cell with power gating technique and without power gating technique. By utilizing the existing technique the static power and delay of the SRAM cell can be upgraded. A new power gating technique, namely SK-LCT Technique is proposed which saves 57.53% of **static power (7)** and 44.70% of delay compared to SRAM cell without power gating.

Table 2: Performance comparison of the SRAM cell

SRAM CELL		POWER	DELAY
WITHOUT POWER GATING		106.7 nW	1.0934ns
WITH POWER GATING	Sleep Technique	45.83 nW	0.7924ns
	Stack Technique	95.86nW	0.9556ns
	Sleepy stack Technique	68.58nW	1.0019ns
	Sleepy keeper Technique	89.18nW	1.0575ns
	LECTOR Technique	57.04nW	0.7069ns
	SK-LCT Technique	45.33nW	0.6041ns

5.2 Sense amplifier using the SK-LCT Technique

The voltage difference between both the bit lines (i.e. BL & BLB complement to each other) of the voltage latch sense amplifier (VLSA) is sensed and amplifies the small voltage signal in the bit lines to conspicuous logic levels. The data in memory cluster are greatly diminished & unstable, which can be boosted by using the amplifier circuitry. The simulation waveform for voltage latch sense amplifier using the SK-LCT Technique is illustrated in Fig.8

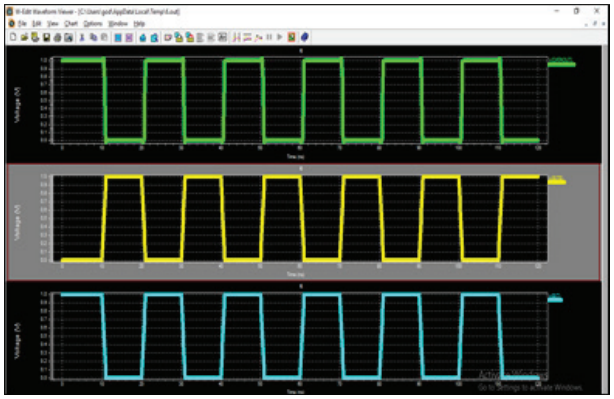

Figure 8: Simulation waveform for sense amplifier using the SK-LCT Technique

The Table 3 demonstrates the correlation of sense amplifier with power gating technique and without power gating technique. By using the existing technique the power and delay of the sense amplifier can be reduced. A novel technique, namely SK-LCT Technique is proposed which saves 93.65% of **static power (7)** and 95.26% of delay contrasted to a differential sense amplifier.

Table 3: Performance comparison of the Sense amplifier

SENSE AMPLIFIER		POWER	DELAY
WITHOUT POWER GATING	Differential Sense Amplifier	0.9034µW	4.2953ns
WITH POWER GATING	Footer Switch-VLSA	0.1556µW	0.25325ns
	Footer Switch-CLSA	0.8592µW	0.25328ns
	DSPA -VLSA	0.1708µW	0.25325ns
	DSNA -VLSA	0.6003µW	0.25325ns
	DSTA -VLSA	0.1401µW	0.23605ns
	SK-LCT Technique(VLSA)	0.0573µW	0.20328ns

5.3 PT-decoder

Based on the address line, particular memory cell is chosen and the data is read and written in the memory cluster. In memory design, the decoder is used to decode the given address and enable the particular row or column of the memory array. Row and column decoder is used to enable word line (WL) and write enable (WE). The speed of the PT–decoder is more proficient than other decoders with the advantage of low power consumption. The simulation waveform of pass transistor decoder is illustrated in Fig. 9.

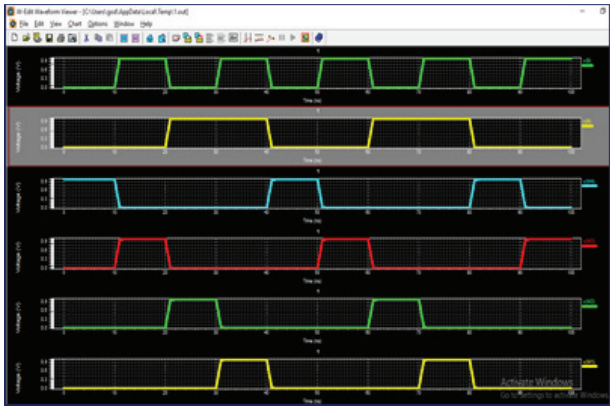

Figure 9: Simulation waveform for PT-decoder

Table 4 demonstrates the comparison of 2:4 decoder. The PT-decoder is more efficient both in power consumption & speed compared to other decoder.

Table 4: Performance comparison of Decoder

DECODER (2:4)	POWER	DELAY
AND Decoder	0.95229 mW	8.5113ps
NOR Decoder	0.23732 mW	29.990ns
Pseudo NMOS Decoder	11.1572 mW	25.206ps
Pass Transistor Decoder (PT-decoder)	8.33171 nW	1.9717ns

5.4 SRAM architecture using SK-LCT technique & PT-decoder

Figure 10: Simulation waveform for SRAM architecture

4 bit, 16 bit & 64 bit SRAM architectures are designed using the proposed SK-LCT technique & PT-decoder provides considerable reduction in leakage power and delay. Fig.10 illustrates the simulation waveform of SRAM architecture using write and read mode. By enabling the PT-decoder, data is written in any one of the memory cell (SRAM cell) and remaining SRAM cell is in hold mode (shut down mode). (4) The data is read by sense amplifier circuitry.

Table 5: Performance comparison of SRAM architecture

SRAM architecture	Without SK-LCT Technique & PT-Decoder		With SK-LCT Technique & PT-Decoder	
	POWER	DELAY	POWER	DELAY
4bit	37.422µW	25.458ns	9.7465µW	11.794ns
16 bit	53.526µW	46.736ns	13.615µW	22.571ns
64 bit	94.63µW	92.219ns	29.607µW	47.383ns

Table 5 demonstrates the performance comparison of 4 bit, 16 bit & 64 bit SRAM architecture using sleepy keeper leakage control transistor & PT decoder. The power & delay of memory architecture are limited using this novel technique. About, 68.71% of **static power (7)** & 44.83% of delay is reduced, which is more attractive than conventional SRAM architecture design.

6 Conclusion

SRAM cell design using the novel SK-LCT technique saves 57.53% of power and 44.70% of delay. Similarly, the sense amplifier design using the novel SK-LCT technique saves 93.65% of power and 95.26% of delay compared to conventional method. SRAM architecture using PT-Decoder is effective compared to other decoders. 4 bit, 8 bit & 64 bit memory architecture save 68.71% of power & 44.83% of delay and are intended for low power application such as handheld gadget. Therefore, from the simulation results it is observed that low power, high speed SRAM architecture for low power application is obtained using SK-LCT technique & PT-decoder.

7 References

1. Andrea Calimera, Alberto Macii, Enrico Macii & Massimo Poncino (2012), "Design Techniques and Architectures for Low-Leakage SRAMs", IEEE Transactions on Circuits and Systems, Vol. 59, No. 9, Sep 2012, pp.1992-2007
2. Yeap G. K. et al (1998), "Practical Low Power Digital VLSI Design', Kluwer Academic Publishers", Norwell, MA, ISBN: 0792380096, pp-233.
3. F. Catthoor, S. Wuytack, E. DeGreef (1998), "Custom Memory Management Methodology Exploration of Memory Organization for Embedded Multimedia System Design", Kluer Acadamic Publishers, Boston.
4. J. M. Rabaey, A. P. Chandrakasan (2003), "Digital Integrated Circuits: A Design Perspective", Upper Saddle River, NJ, USA: Prentice-Hall.
5. A. Anand Kumar, "Fundamentals of Digital Circuits" Second Edition, Prentice Hall of India, pp. 337-340, 2006.
6. Hina Malviya and Sudha Nayar (2013), "A new Approach for Leakage Power Reduction Techniques in Deep Submicron Technologies in CMOS circuit for VLSI Application", IEEE Int. Solid State Circuits Conf. (ISSCC) Dig. Tech, Vol.3 Mar 2013, pp. 11–16.
7. Anu Tonk and Shilpa Goyal (2015), "A Literature Review on Leakage and Power Reduction Techniques in CMOS VLSI Design", International Journal of Advanced Research in Computer and Communication Engineering, Vol.3, Issue.2, pp.554-558.
8. J. Park (2014), "Sleepy Stack: a New Approach to Low Power VLSI and Memory", Ph.D. Dissertation, School of Electrical and Computer Engineering, Georgia Institute of Technology, May 2014.
9. Narender Hanchate (2011), "LECTOR: A Technique for Leakage Reduction in CMOS Circuits", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol.12, No. 2, Feb 2011, pp.198-205
10. M. Geetha Priya, Dr. K. Baskaran and D. Krishnaveni (2012), "Leakage Power Reduction Technique in Deep Submicron Technologies for VLSI Applications", Elsevier-Sciverse Science Direct, Procedia Engineering, Vol. 30, Dec 2012, pp.1163-1170
11. Taehui Na, Seung-Han Woo, Jisu Kimg, Hanwool Jeon, and Seong-Ook Jung(2013), "Comparative Study of Various Latch-Type Sense Amplifiers", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 12, No. 6, Sep 2013, pp.1-5

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Implementation of VIP for bus interface logic of 32-bit processor using System Verilog

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Abstract: A verification environment to verify an ARM-based SoC is proposed in this work. This work introduces the design of a Verification Intellectual Property (VIP) of Advanced Microcontroller Bus Architecture (AMBA). AMBA protocols are today the best standards for 32-bit processor because they are well documented and can be used without royalties. The VIP provides Coverage Driven Verification (CDV) which significantly reduces the design verification time. The code coverage verification of the AHB bus master, Icache controller, Dcache controller and APB peripherals such as APB bridge, timer, UART, and ACE is done in this work. The test cases done for the APB peripherals are ACE with the mil_std_protocol, Timers for generation of interrupt and watchdog reset, UART for transmitting and receive messages, and interrupt registers for Reading and Write. The functional verification of AMBA is carried out using the Mentor Graphics Questasim tool with the system Verilog language.

Keywords: Verification Intellectual Property; AMBA; Coverage Driven Verification; timer; ACE; UART; system Verilog

Uporaba VIP za vmesnik logičnega vodila 32-bitnega procesorja s uporabo System Verilog

Izvleček: V članku je predlagano okolje preverjanja SoC na osnovi ARMa. Struktura uvaja verifikacijo intelektualne lastnine (VIP) na napredni arhitekturi vodila mikrokontrolerja (AMBA). AMB protokoli so danes najbolj standardni protokoli na 32- bitni procesorjih, saj so dobro dokumentirani in brez avtorskih zaščit. VIP uporablja CVD, ki močno zmanjša čas verifikacije. V tem delu je predstavljena verifikacija AHB master vodila, Icache in Dcache kontrolerjev ter APB perifernih enot, kot so časovnik, UART in ACE. Testni primeri za APB periferne enote so ACE z mil_std_protocol, časovniki za generacijo prekinjanj in resetiranja kontrolne enote (watchdog), UART za pošiljanje in sprejemanje sporočil in prekinitveni registri za zapis in branje. Funkcionalno preverjanje je izvedeno s pomočjo orodja Mentor Graphics Questasim v jeziku Verilog.

Ključne besede: verifikacija intelektualne lastnine; AMBA; verifikacija; časovnik; ACE; UART; Verilog

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1 Introduction

With the continued progression of chip geometries to ever smaller sizes, designers are finding themselves with a wealth of available gates in which to create their latest designs [1-4]. With design from scratch entirely out of the question, designers now build these systems with off-the-shelf IP blocks that are pre-designed and verified, helping them meet their goals of differentiation, cost control and time to market.VIP blocks are well-tested simulation models of industry-standard buses and protocols that generate and respond to stimulus and check protocol rule adherence. VIP reduces system verification time and improves quality.

VIP design of AMBA AXI bus is done in the previous works [5-9][11], But the VIP for Dcache controller, Icache controller and APB peripherals such as APB bridge, timer, UART, and ACE is done for the first time. The implemented VIP finds application in the realization of onboard computers for navigation, guidance,

and control processing in-flight applications as well as for general purpose processing applications.

The verification environment is managed with Questa Sim Simulator ver.10.0, test bench and SVA in System Verilog HDL and DUT in VHDL. Separate assertion files in system Verilog are bound with the corresponding test benches to validate design specifications.

2 Proposed system design

2.1 AMBA Bus

The Advanced Microcontroller Bus Architecture specification defines an on-chip communications standard regarding bus protocols for communication between various system devices and peripherals. AMBA is a registered trademark of ARM Limited and is an open standard, on-chip interconnect specification for the connection and management of functional blocks in a System-on-Chip (SoC) [2]. This work provides Coverage Driven Verification (CDV) for the implementation of Verification Intellectual Property (VIP) for the AMBA bus. In this paper, the verification of the APB peripherals such as APB Bridge, timer, UART, and ACE is done.

2.2 AMBA Architecture

An AMBA based microcontroller typically consists of a high-performance system backbone bus (AMBA AHB or AMBA ASB), able to sustain the external memory bandwidth, on which the CPU, on-chip memory, and other Direct Memory Access (DMA) devices reside. A typical AMBA Architecture is shown in figure 1[2].

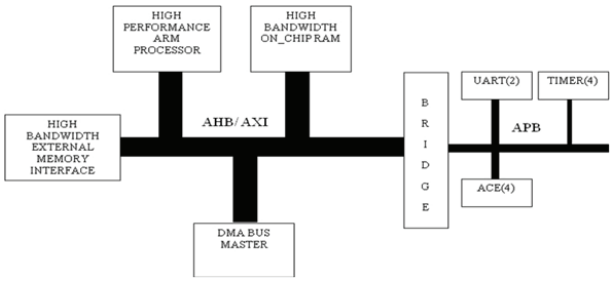

Figure 1: AMBA Architecture

2.3 AHB Master

AHB_master generates chip select signals, the external memory address for instruction and data memory. The FSM of AHB_master is shown in figure 2.

The FSM works on clk_x2_pos. Wait states are added for external instruction and data memory access. They are selected from the Memory Configuration Register depending on the memory bank accessed.

Instr_state: It is selected when instruction access is requested by fetch stage of the pipeline when instruction cache is disabled. Chip select signals and address for external memory access are generated. The instruction read from external memory is sent to the fetch stage of the pipeline. FSM waits in the instr_state till the specified wait states are over and transitions back to idle state.

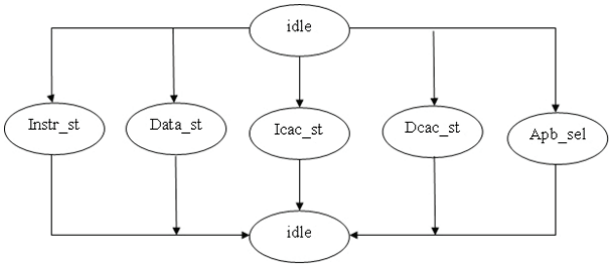

Figure 2: FSM of AHB_master

Data_state: It is selected when data memory access is requested by the memory stage of the pipeline when data cache is disabled. Chip select signals for load/store and address for external memory access are generated. For load, the data read from external memory is sent to the memory stage of the pipeline. For the store, the data from the memory stage of the pipeline is sent to the external memory. FSM waits in the data_state till the specified wait states are over and transitions back to idle state.

ICache_state: This state is selected if Icache is enabled and a cache miss occurs. FSM2 handling miss in icache_controller.vhd is active here. The chip select signals are generated when fsm2 in icache_controller. vhd is in wait_for_mfc (wait_for_mfc_icache = 1) state. FSM transitions to idle when icache access is complete (icache_access_complete=1, from icache_controller. vhd)

DCache_state: This state is selected if Dcache is enabled and a cache miss occurs. FSM2 handling miss in dcache_controller.vhd is active here. The chip select signals are generated when fsm2 in dcache_controller. vhd is in wait_for_mfc (wait_for_mfc_dcache = 1) state. FSM transitions to idle when dcache access is complete (dcache_access_complete=1, from dcache_controller. vhd).

APB_sel: If a memory mapped peripheral is selected apb_sel state is encountered. FSM transitions to idle when hready_apb = '1' from apb_bridge.vhd, the external memory address for instruction access, is generat-

ed in instr_state or icache_state. The external memory address for data access is generated in data_state or dcache_state.

2.4 Icache controller

The instruction cache controller is used to cache copies of frequently accessed instructions, thus eliminating the program memory access bottleneck. The cache controller receives instruction read request an address from the Fetch stage. Depending on hit/miss the cache controller supplies instruction from the on-chip cache or reads from external program memory via AHB and provides instruction to the pipeline. Till external memory access is complete, the pipeline is stalled.

- 32KB size.Can store 8K instructions
- Two way set associative
- Uses Least Recently Used (LRU) algorithm for block replacement
- Block size: 4 words

LRU Replacement Algorithm

The LRU (Least Recently Used) algorithm is implemented for the two-way associative cache conFigure uration. This algorithm selects a block for replacement based on its usage, thus benefiting from the temporal locality principle. A single bit is added as part of the tag entry in the tag ram. Whenever a tag match is found in a block, the LRU bit of that block is cleared and the LRU bit of the second block in the set is made '1'.When a block is to be evicted, the tag entry in the set which has its LRU bit set to 1 is selected.

2.5 Dcache controller

The data cache controller caches frequently used data items. The data cache implements copy back with write allocate on a write miss. The dirty blocks are written back to external memory only when they need to be evicted.

- Size = 32KB
- Cache line size = 4words
- Uses an LRU replacement algorithm
- Copy back policy
- Write allocate on a write miss
- Two way set associative

Hardware Organization: Data cache is identical to the instruction cache, except that each tag ram location has an additional bit called the dirty bit, which indicates whether the cache block had been modified during its cache residency. Thus each tag ram array has 23 bits * 1024 locations.

Address Decoding: This is identical to two-way associative instruction cache implementation. The 10-bit address is used to index the tag ram arrays. The two-word locator bits are appended to the 10-bit set address to address the cache ram arrays.

Copy Back Architecture: When there is a store request from the memory stage of the pipeline, the corresponding cache array entry is updated in the cache if it already exists in the cache. If it is a cache miss, the block which includes the address requested by the store operation is brought into the cache from the external memory (write allocate on a write miss) and the required location is updated. This policy is especially beneficial when frequent writes to a memory location (store instruction) occur since there is no need to access external memory once the word is in the cache. This policy uses the memory bandwidth more efficiently compared to the write through policy wherein each store location writes to the external memory.

Data Cache Parity Error detection of cache tags and data is implemented using two parity bits per tag and 4-byte data sub-block. The tag parity is generated from the tag value, LRU, dirty and the valid bits. The data parity is derived from the sub-block data. The parity bits are written simultaneously with the associated tag or sub-block and checked on each access. The two parity bits corresponding to the parity of odd and even data (tag) bits.

2.6 APR Bridge

APB bridge acts as the master for the APB slaves – four ACE, two UART, interrupt registers and four timers. The APB bridge converts the AHB signals from the bus master to corresponding signals in APB. Memory configuration register specifies the no. of wait states for different memory banks and internal RAM.

Select signal for selecting a memory mapped register is generated by decoding the address (haddr). Hwrite=1 indicates a register write operation. Hwrite=0 indicates a register read operation. The ACE, UART, timer, interrupt, and processor configuration registers are read or written in a single clock cycle, and hready_apb is asserted. For ace access hready_apb is asserted when already signal is asserted. The Processor Configuration Register is shown in table 1.

Table.1: Processor Configuration Register

Bit	Description
31:13	Unused
12	Interrupt Enable
11	Watchdog enable
10	SECDED enable for Internal RAM

9	SECDED enable for external memory bank 6
8	SECDED enable for external memory bank 5
7	SECDED enable for external memory bank 4
6	SECDED enable for external memory bank 3
5	SECDED enable for external memory bank 2
4	SECDED enable for external memory bank 1
3	SECDED enable for external memory bank 0
2	SECDED enable for Internal Registers
1	Instruction Cache Enable
0	Data Cache Enable

2.6 AMBA Advanced Peripheral Bus

The APB Bridge is the only bus master on the AMBA APB. Also, the APB Bridge is also a slave on the higher-level system bus (for example AHB). The bridge unit converts system bus transfers into APB transfers and performs the following functions:

- Latches the address and holds it valid throughout the transfer.
- Decodes the address and generates a peripheral select, PSELx. Only one select signal can be active during a transfer.
- Drives the data onto the APB for a write transfer.

2.7 Code Coverage Analysis

Code coverage is a verification technology is used to recognize what code has been executed (figure 3). It has to be checked only after the simulation part. If the design may look like a good design, but the problem is that it can contain unknown bugs. It is hardly possible to know the verification is functionally correct, with cent percent certainty and all of the test benches simulate successfully. The main objective of the code coverage is to find out which code has to forget to exercise in the design.

The term *"test bench"* specifies the stimulus used to initiate a predestined input sequence for the design and to examine its response. The test bench describes the stimulus for the DUT along with its responsibility for the outputs. Here, the test bench is written in SystemVerilog with a preset input sequence, and they may be included with external data files. The main task of the test bench is that to verify what input patterns to provide to the design and what is the anticipated throughput of a properly working design. If the test bench was not exactly executed, it should be returned in the design. So, code coverage technology is used for the 100% certainty. It can be classified into four categories. They are Statement coverage, Path coverage (Branch and Toggle coverage), Expression coverage, FSM coverage.

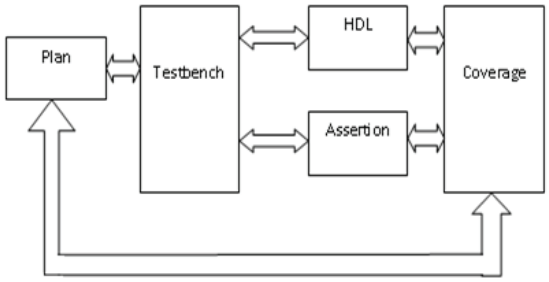

Figure 3: Verification plan

Statement coverage: It is also known as Block coverage, where the block is series of statements. If a single statement is executed, all of the statements in the block will be executed. By the verification suite, it measures how much of the total line of code was executed. Figure 4 shows the analysis window for the statement coverage verification. It will be generated after the simulation part. The tick (√) mark indicates that statement code which includes in the DUT are functionally correct. If shows (x) mark, indicate that design is functionally incorrect. It will quickly identify, and we can browse which statements that were not executed.

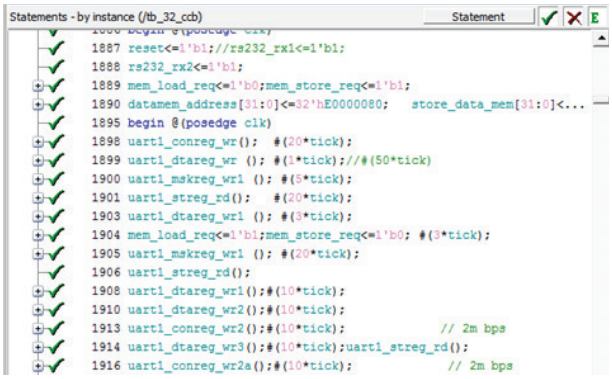

Figure 4: Statement coverage

FSM: It is usually, coded using a choice in a case statement, the unvisited state identified with uncovered statements. During the verification time, it clearly or correctly identifies the state transitions. Figure 5 shows the bubble diagram for FSM. It indicates that state transitions of decoder sections.

Branch and Toggle coverage: A signal is considered to have fully toggled when it has experienced at least one rising edge and at least one falling edge during the simulation. It has been found from the simulated results that the coverage windows, which indicate all the branch and toggles present in the design of AMBA was functionally, correct.

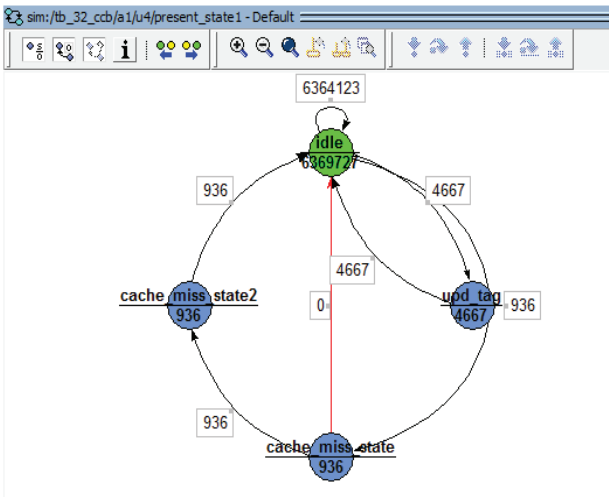

Figure 5: FSM coverage

Transition Coverage: Transition coverage measures the presence or occurrence of sequences of values. Transition coverage can involve more than two consecutive values of the same coverage point. However, the number of possible bins grows factorially with the number of transition states. Mechanically, transition coverage is identical to coverage points. Specific values are sampled at specific locations at specific points in time with specific bins. Table 2 and 3 show the Assertions for the Timer module and the UART module.

Table.2: Assertions for the Timer Module

3 Results and discussion

The functional verification of AMBA is carried out using the Mentor Graphics Questasim tool in the code coverage mode with the SystemVerilog language. The SystemVerilog simulation is performed to verify the AMBA design by using the VIP. Functional integrity of DUT is checked by using Assertions and cover groups along with necessary test inputs.

Figure 6 shows the instance coverage analysis of the AMBA peripherals. The instance analysis is done a state of the peripherals during each instance. It provides the coverage of the individual modules in the AMBA peripherals. This window analyzes coverage statistics for each instance in a flat and non-hierarchical view. The window contains the same code coverage statistics columns as in the Files and Structure windows.

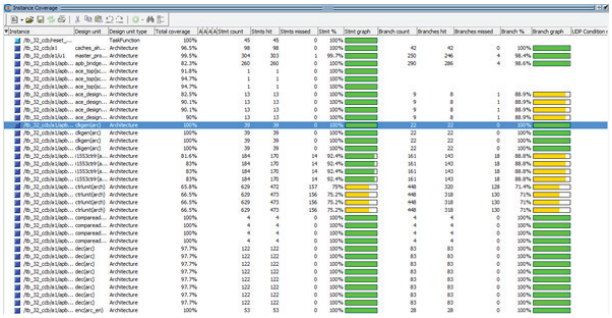

Figure 6: Instance coverage

Assertion	Description
Timer_hreset_prdata	prdata_timer=32'h00000000 when hreset is asserted
Timer_hreset_intr	Intr_timer1, Intr_timer2, Intr_timer3, Intr_timer4=0 when hreset is asserted
Timer1 underflow	When prdata_timer<=32'h00000000 and haddr <= 32'hE0000048 then intr_timer1=0
Timer2 underflow	When prdata_timer<=32'h00000000 and haddr <= 32'hE0000054 then intr_timer2=0
Timer3 underflow	When prdata_timer<=32'h00000000 and haddr <= 32'hE0000060 then intr_timer3=0
Timer4 underflow	When prdata_timer<=32'h00000000 and haddr <= 32'hE000006c then intr_timer4=0
Timer1_disable	When prdata_timer<=32'h00000000 and haddr <= 32'hE0000040 then intr_timer1=1
Timer2_disable	When prdata_timer<=32'h00000000 and haddr <= 32'hE000004c then intr_timer2=1
Timer3_disable	When prdata_timer<=32'h00000000 and haddr <= 32'hE0000058 then intr_timer3=1
Timer4_disable	When prdata_timer<=32'h00000000 and haddr <= 32'hE0000064 then intr_timer4=1

Table.3: Assertions for the UART Module

Assertion	Description
Uart1_transmit enable	When hreset is asserted and haddr==32'hE0000020 && hwdata==24'h0000A5 then rs232_tx1==1'b1
Uart1_recieve enable	When hreset is asserted and haddr==32'hE0000024 && rs232_rx1==1'b1 then hrdata_apb==32'h000000A5
Uart2_transmit enable	When hreset is asserted and haddr==32'hE0000080 && hwdata==24'h0000A5 then rs232_tx2==1'b1
Uart2_recieve enable	When hreset is asserted and haddr==32'hE0000084 && then rs232_rx2==1'b1 then hrdata_apb==32'h000000A5

Figure 7 shows the coverage aggregation analysis of the AMBA peripherals. The coverage aggregation analysis shows, the state of the toggle graph, state graph, and the transition graph during the coverage analysis.

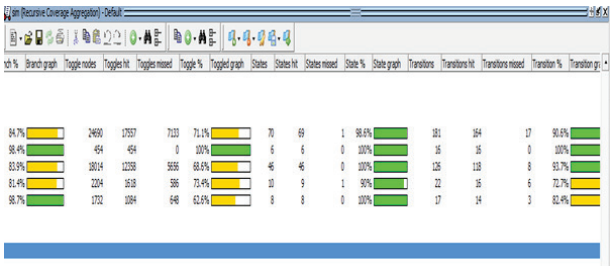

Figure 7: Coverage aggregation

The Assertion Coverage of the AMBA peripherals is also analyzed using a simulation tool. Assertion/properties provide a clear indication to the VIP module. The assertions can be set as true or false throughout the VIP module. It has been found from the simulated results that, the total of 17 assertions are used for the analysis and each of them has been satisfied throughout the analysis. Hence, the assertion coverage of the proposed VIP module is 100 %.

Figure 8 and 9 shows the coverage analysis report of the AMBA peripherals. The coverage analysis depicts the coverage obtained by the proposed VIP module for each of the AMBA peripherals. For the coverage analysis, the VIP considered seven aspects for each module, and they are the statement, Branches, FEC condition trees, FEC expression trees, States, transition, and toggle bin. In total, proposed VIP has achieved coverage value of 91.4%, for each AMBA peripherals. Besides, the total 17 assertions provided for the analysis has never failed throughout the process,

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Coverage Report Summary Data by file

File: 32UP_V4/32_sep14/Bus Interface/vhdl/ahb_master.vhd

Enabled Coverage	Active	Hits	Misses	% Covered
Stmts	284	284	0	100.0
Branches	209	205	4	98.1
FEC Condition Terms	0	0	0	100.0
FEC Expression Terms	0	0	0	100.0
States	6	6	0	100.0
Transitions	16	16	0	100.0
Toggle Bins	1464	1464	0	100.0

File: 32UP_V4/32_sep14/Bus Interface/vhdl/apb_bridge.vhd

Enabled Coverage	Active	Hits	Misses	% Covered
Stmts	177	177	0	100.0
Branches	189	184	5	97.3
FEC Condition Terms	0	0	0	100.0
FEC Expression Terms	0	0	0	100.0
States	0	0	0	100.0
Transitions	0	0	0	100.0
Toggle Bins	2752	2330	422	84.6

File: 32UP_V4/32_sep14/Bus Interface/vhdl/caches_ahb_top.vhd

Enabled Coverage	Active	Hits	Misses	% Covered
Stmts	61	61	0	100.0
Branches	43	25	0	100.0
FEC Condition Terms	0	0	0	100.0
FEC Expression Terms	0	0	0	100.0
States	0	0	0	100.0
Transitions	0	0	0	100.0
Toggle Bins	2372	1888	484	79.5

File: 32UP_V4/32_sep14/Bus Interface/vhdl/decoder_uart.vhd

Enabled Coverage	Active	Hits	Misses	% Covered
Stmts	34	34	0	100.0
Branches	7	7	0	100.0
FEC Condition Terms	0	0	0	100.0
FEC Expression Terms	0	0	0	100.0
States	0	0	0	100.0
Transitions	0	0	0	100.0
Toggle Bins	12	12	0	100.0

File: 32UP_V4/32_sep14/Bus Interface/vhdl/uart.vhd

Enabled Coverage	Active	Hits	Misses	% Covered
Stmts	229	217	12	94.7
Branches	221	204	17	92.3
FEC Condition Terms	0	0	0	100.0
FEC Expression Terms	0	0	0	100.0
States	3	3	0	100.0
Transitions	7	7	0	100.0

Figure 8: Coverage report

File: 32UP_V4/32_sep14/Bus Interface/vhdl/uart_apb_iface.vhd

Enabled Coverage	Active	Hits	Misses	% Covered
Stmts	8	8	0	100.0
Branches	6	6	0	100.0
FEC Condition Terms	0	0	0	100.0
FEC Expression Terms	0	0	0	100.0
States	0	0	0	100.0
Transitions	0	0	0	100.0
Toggle Bins	232	166	66	71.5

File: ace_top.vhd

Enabled Coverage	Active	Hits	Misses	% Covered
Stmts	1559	1380	179	88.5
Branches	1237	1073	164	86.7
FEC Condition Terms	0	0	0	100.0
FEC Expression Terms	0	0	0	100.0
States	5	5	0	100.0
Transitions	14	13	1	92.8
Toggle Bins	6269	4489	1780	71.6

File: dcache.vhd

Enabled Coverage	Active	Hits	Misses	% Covered
Stmts	347	306	41	88.1
Branches	276	225	51	81.5
FEC Condition Terms	0	0	0	100.0
FEC Expression Terms	0	0	0	100.0
States	9	8	1	88.8
Transitions	20	14	6	70.0
Toggle Bins	2990	2098	892	70.2

File: icache.vhd

Enabled Coverage	Active	Hits	Misses	% Covered
Stmts	186	176	10	94.6
Branches	150	135	15	90.0
FEC Condition Terms	0	0	0	100.0
FEC Expression Terms	0	0	0	100.0
States	8	8	0	100.0
Transitions	17	14	3	82.3
Toggle Bins	2348	1818	530	77.4

File: timer_new.vhd

Enabled Coverage	Active	Hits	Misses	% Covered
Stmts	125	117	8	93.6
Branches	201	193	8	96.0
FEC Condition Terms	0	0	0	100.0
FEC Expression Terms	0	0	0	100.0
States	0	0	0	100.0
Transitions	0	0	0	100.0
Toggle Bins	492	444	48	90.2

NEVER FAILED: 100.0% ASSERTIONS: 17

Figure 9: Coverage report (Continued)

4 Conclusion

In this work, verification environment for Caches AHB_ Top, AHB Master, Instruction cache, Data cache the free running counters/timers of APB, ACE Controller, UART and APB Bridge is done. The verification scenario includes Read and Write transfer phases of the APB which are verified with the values of the count and reset. The test cases done for the APB peripherals are ACE with the mil_std_protocol, Timers for generation of interrupt and watchdog reset, UART for transmitting and receive messages, and interrupt registers for Reading and Write. From the simulation results, the state of operation of the AMBA is obtained. The overall coverage obtained for the AMBA peripherals is 91.4%, and the Assertion Coverage is 100%. This work can be extended by creating the verification environment for AMBA with the UVM library. Questasim collects all coverage data, code coverage, assertions, formal, and functional

coverage into a single highly efficient Unified Coverage Database (UCDB) and makes them available in real-time within the test bench.

5 Reference

1. "AMBA AHB"- specification by ARM limited.
2. AMBA timer data sheet, http://www.arm.com/.
3. ARM, "AMBA specification overview," http://www.arm.com/
4. Chris spear, SystemVerilog for Verification A Guide To Learning the Test Bench Language Features, 2nd edition.
5. Golla Mahesh, Sakthivel S M "Verification IP for an AMBA-AXI protocol using system Verilog", International Journal of Applied Engineering Research, Vol.12, No.17, pp. 6534-6541,November 2017.
6. Golla Mahesh and Sakthivel.S.M, "Verification IP for an AMBA-AXI Protocol using System Verilog" International Journal of Engineering Research and General Science, vol.3, no.1, pp.792-799, February, 2015.
7. Han Ke, Deng Zhongliang, Shu Qiong "Verification of AMBA bus model using SystemVerilog" The Eighth International Conference on Electronic Measurement and Instruments ICEMI' 2007. https://doi.org/10.1109/ICEMI.2007.4350567
8. Heli Shah P, Chinmay modi P, Bhargav Tarpara P "Design & Implementation of Advance Peripheral Bus Protocol," International journal of scientific engineering and applied science (IJSEAS) vol.1, no.3, June 2015.
9. Manu B, Prabhavathi P, "Design and Implementation of AMBA ASB APB bridge" Proceedings of 2013 International conference on fuzzy theory and its application national Taiwan University of science and technology, pp. 6-8, December 2013. https://doi.org/10.1109/iFuzzy.2013.6825442
10. Questa sim user's manual, by Mentor Graphics.
11. Richa Sinha, Akhilesh Kumar, and Archanakumari Sinha "Verification analysis of AHB-LITE protocol with coverage," International Journal of advances in Engineering & technology, Vol.2, No.1, pp.121-128, January 2012.

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Temporary Bonding Using Paper Inserted PPC Layer

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Abstract: Temporary bonding using paper inserted polypropylene carbonate (PPC) layer is demonstrated. The inserted paper layer can absorb photo acid generator (PAG)-induced acid and protect the substrate. Large improvements of bonding strength are achieved using paper inserted PPC layer. Especially, the bonding strength is much higher than that of PPC/PAG-PPC bonding for tissue paper. The results show that the paper fibers can absorb decomposed PPC and PAG-induced acid, thus protecting the substrate.

Keywords: temporary bonding; debonding; polypropylene carbonate

Začasno bondiranje z uporabo s papirjem vnesene PPC plasti

Izvleček: Prikazano je začasno bondiranje z vnosom plasti polipropilen karbonata (PPC) s pomočjo papirja. Vložena papirna plast lahko absorbira kislino generatorja fotokisline (PAG), s čimer zaščiti substrat. Uporaba PPC plasti omogoča velike izboljšave vezne trdnosti bonda. Zlasti je vezna trdnost precej višja kot pri uporabi PPC/PAG-PPC tkanine. Rezultati kažejo, da lahko papirna vlakna absorbirajo razgrajeno kislino, ki jo povzroča PPC in PAG, s čimer se zaščiti substrat.

Ključne besede: začasno bondiranje; debondiranje; polipropilen karbonat

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1 Introduction

Silicon wafer is the fundamentals of semiconductor industry [1-3]. Particular, the application of thin silicon wafers is an enabling technology for modern electronics as reduced wafer thickness integration enables shorter processing times and less cost [4-6]. All of this is advantageous for a low package height for chip cards, the requirement for higher power, and the search for System-in-a-Package (SiP) using chip stack methods.

Temporary bonding and debonding are essential for fabricating thin wafers [7, 8]. On the one hand, the bonding strength should be high in order to endure the mechanical polishing/thinning. On the other hand, debonding process is required to be simple, low cost and of high reliability. To achieve the above requirements, we propose photo acid generator (PAG) loaded polypropylene carbonate (PPC) debonding at room temperature without any solvent based or ultraviolet (UV) treatment [9]. Subsequently, PPC/PAG-PPC bonding structure is proposed [10]. The inserted PPC layer serve as the passivation layer, which can absorb the PAG-induced acid. The bonding layer loses adhesion to the substrate and automatic debonding is achieved when center region of the PPC layer is decomposed. The PAG-induced acid is separated from the bonding substrate, which improve the bonding strength and protect the substrate. Application of PPC as temporary adhesive for fabrication of sensor chip has also been demonstrated [11].

The main aim of this work is to develop a method to further increase the PPC temporary bonding strength. Herein, we propose temporary bonding using paper inserted PPC layer. Further improvement of bonding strength is achieved.

2 Experimental

Temporary bonding and debonding using paper inserted PPC layer is proposed to protect the substrate and improve the bonding strength. The bonding structure is shown in Fig. 1a. The PPC polymers (QPAC 40) used in this work were obtained from Empower Materials and have a molecular weight of 196 kg / mol. The PPC solution was prepared by dissolving pure PPC in acetone under constant stirring to form a 20 wt% solution. Tetrakis(penta-fluorophenyl) borate-4-methylphenyl [4-(1-methylethyl)-phenyl] iodonium tetrakis (pentafluorophenyl) borate is used as the PAG and obtained from tokyo chemical industry Co. The PAG-PPC solution was prepared by adding PAG (about 1 wt% of the PPC) to the PPC solution. Printer paper, tissue paper and silicone paper are used as the paper insertion layer. The main chemical compositions of the paper insertion are cellulose, hemicellulose, lignin, calcium carbonate, etc. The paper fiber can interlace with PPC polymer and absorb PAG-induced acid. Silicon paper is fabricated by treating printer paper with silicone, so it is nonstick and heatproof. The glass substrates (10mm×10mm) are obtained from Dongsheng Corporation with density of 2.2 g/cm^3, tensile strength of ~50 MPa and inflection resistance of 60-70 MPa. The PPC solution was poured onto the glass substrate facade. The acetone was then removed by baking the specimen for 10 min at 60 °C. Subsequently, paper layer is attached on PPC surface, followed by dropping of PAG-PPC solution and solvent evaporation. Bonding of the fabricated samples is achieved using a hot press (Carver, Inc.) at bonding pressure of 0.2MPa. The bonding temperatures for thermal bonding 1 and 2 are 100°C and 200°C, respectively. The morphology of the substrate surface is examined using Hitachi TM3000 scanning electron microscope (SEM).

3 Results and Discussions

The decomposition products of PPC include cyclic propylene carbonate (cPC), propylene glycol, and CO_2, which indicates that decomposed PPC is liquid at room temperature. The (SEM image of typical paper fiber is shown in Fig. 2. It is obvious that the cellulose fiber of paper can absorb decomposed PPC and PAG-induced acid. Thus, PPC is less consumed and there is PPC remained beneath the paper layer, the substrate is protected and the bonding strength is improved. Under high bonding temperature (＞170°C, represent as thermal bonding 2 in Fig. 1a1), sufficient PAG-induced acid is produced, consuming the entire PPC layer between paper layer and achieving automatic debonding at room temperature without any solvent based or UV treatment. Under low bonding temperature (＜130°C, represent as thermal bonding 1 in Fig. 1a2), a portion of PAG is activated and less PAG-induced acid is produced, and a considerable portion of acid is also absorbed by paper fiber. Thus, a subsequent UV irradiation or heating is required to achieve complete debonding.

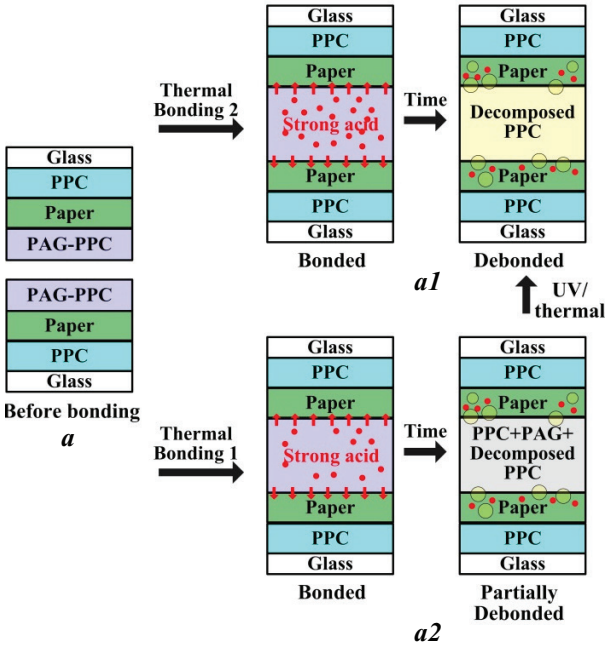

Figure 1: Schematic of temporary bonding and debonding process
a PPC/Paper/PAG-PPC bonding structure
a1 Bonding at high temperature(＞170°C) and subsequent automatic debonding for PPC/Paper/PAG-PPC structure
a2 Bonding at low temperature(＜130°C) and subsequent debonding for PPC/Paper/PAG-PPC structure

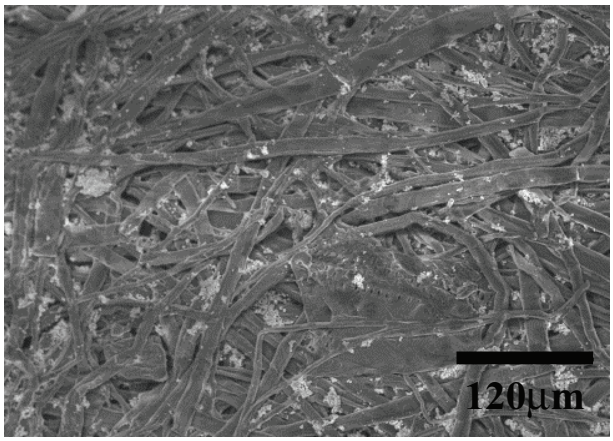

Figure 2: SEM image of typical paper fiber

Glass substrates are used to demonstrate and compare the bonding results. The results are shown in table 1. It

can be seen from table 1 that large improvements of bonding strength are achieved using paper inserted PPC layer. This effect is especially obvious for tissue paper, which absorb more PAG-induced acid. For printer paper and tissue paper, the bonding strength decrease significantly when bonding temperature increases to 200°C, which is probably caused by damage of fiber structure. On the contrary, there is no significant decrease of bonding strength of silicone paper inserted PPC layer, which can be attributed to the heat resistance property of silicone paper.

In order to adjust the debonding time, heating or UV irradiation processes after bonding is used. All the bonded samples fabricated in this work are successfully debonded.

Table 1: Comparison of the bonding strength of different methods demonstrated using glass substrates

Ref.	Bonding strength (MPa)	
	Thermal bonding 1	Thermal bonding 2
Printer paper in this work	3.9±0.45 MPa	1.7±0.33 MPa
Tissue paper in this work	4.1±0.29 MPa	2.3±0.12 MPa
Silicone paper in this work	3.5±0.19 MPa	3.2±0.43 MPa
PAG-PPC bonding in [9]	3.0±0.34 MPa	2.1±0.18 MPa
PPC/PAG-PPC bonding in [10]	3.3±0.26 MPa	2.7±0.25 MPa

The surface morphologies of debonded samples were observed by SEM. Fig. 3 shows the SEM image of typical surface morphology of debonded samples for PAG-PPC bonding under thermal bonding 2. PPC residue was observed. The results correspond well with the bond mechanism which state that under high bonding temperature, excessive PAG-induced acid is produced, consuming the PPC protection layer at multiple locations and and leaving PPC residue. The PAG-induced acid can cause damage to the substrate and decrease the reliability of circuit where PPC protection layer is consumed.

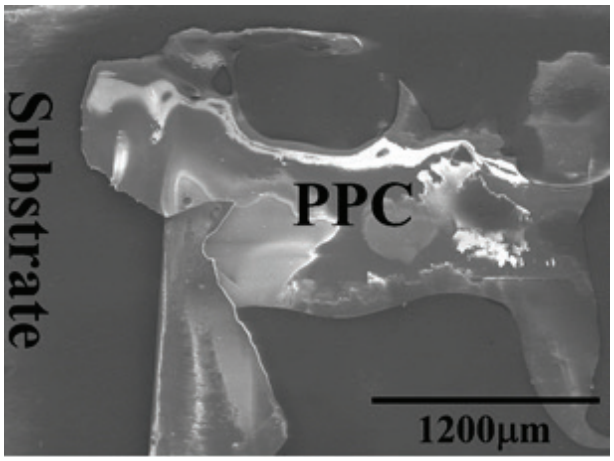

Figure 3: SEM image of typical surface morphology of debonded samples for PAG-PPC bonding under thermal bonding 2

Fig. 4 shows the SEM image of typical surface morphology of debonded samples for PPC/silicone paper/PAG-PPC under thermal bonding 2. The results show that the upper surface of paper is the debonding interface, which indicate that the PPC layer beneath paper insertion is hardly decomposed. This corresponds well with the bond mechanism which state that paper fibers can absorb decomposed PPC and PAG-induced acid. Thus, PPC is less consumed and there is PPC remained beneath the paper layer, the substrate is protected and the bonding strength is improved. The improvements of bonding strength have also been demonstrated in Table 1.

Figure 4: SEM image of typical surface morphology of debonded samples for PPC/silicone paper/PAG-PPC under thermal bonding 2.

4 Conclusion

This letter proposes temporary bonding and debonding using paper inserted PPC layer. The paper insertion can absorb PAG-induced acid and increase bonding strength. In order to adjust the debonding time, heating or UV irradiation processes after bonding is used.

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6 References

1. B. Tunaboylu, Space transformer connector characterisation for a wafer test system, *Informacije MIDEM,* 47[4] (2017) 255-260.
2. B. Tunaboylu, Performance of Ni-alloy MEMS-probes coated with PdCo films in semiconductor wafer test, *Informacije MIDEM,* 46[2] (2016) 80-90.
3. X. S. Zhang, Fabrication and characterization of squama-shape micro/nano multi-scale silicon material, Science China Technological Sciences, 55[12] (2012) 3395-3400. https://doi.org/10.1007/s11431-012-4853-2
4. S. L. Ma, et al., Fabrication and characterization of a tungsten icroneedle array based on deep reactive ion etching technology, *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena,* 34[5] (2016) 052002. https://doi.org/10.1116/1.4960715
5. R. N. Fang, et al., Characteristics of coupling capacitance between signal-ground TSVs considering MOS effect in silicon interposers, *IEEE Transactions on Electron Devices,* 62[12] (2015) 4161-4168. https://doi.org/10.1109/ted.2015.2494538
6. X. Sun, et al., Measurement-based electrical characterization of through silicon vias and transmission lines for 3D integration, *Microelectronic Engineering,* 149[5] (2016) 145-152. https://doi.org/10.1016/j.mee.2015.10.010
7. Y. Guan, *et al.*, Fine-pitch through-silicon via integration with self-aligned back-side benzocyclobutene passivation layer, *IET Micro & Nano Letters*, 11[10] (2016) 619. https://doi.org/10.1049/mnl.2016.0267
8. P.Garrou, Handbook of 3D integration (Wiley-VCH), 2008.
9. Z. Zhu, *et al.*, Temporary Bonding/Debonding of Silicon Substrates Based on Propylene Carbonate, *Journal of Electronic Packaging*, 137[4] (2015) 044501. https://doi.org/10.1115/1.4031750
10. Z. Zhu, *et al.*, PPC-based bilayer temporary bonding and debonding, *Microelectronic Engineering*, 180[5] (2017) 5-7. https://doi.org/10.1016/j.mee.2017.05.029
11. X. Xue, *et al.*, Heat-Depolymerizable Polypropylene Carbonate as a Temporary Bonding Adhesive for Fabrication of Flexible Silicon Sensor Chips, *IEEE Transactions on Components Packaging & Manufacturing Technology*, 7[11] (2017) 1751-1758. https://doi.org/10.1109/TCPMT.2017.2742554

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Reliability evaluation of buck converter based on thermal analysis

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Abstract: The design, which is based on the concept of reliability, is impressive. In power electronic circuits, the reliability design has been shown to be useful over time. Moreover, power loss in switches and diodes plays a permanent role in reliability assessment. This paper presents a reliability evaluation for a buck converter based on thermal analysis of an insulated-gate bipolar transistor (IGBT) and a diode. The provided thermal analysis is used to determine the switch and diode junction temperature. In this study, the effects of switching frequency and duty cycle are considered as criteria for reliability. A limit of 150°C has been set for over-temperature issues. The simulation of a 12 kW buck converter (duty cycle = 42% and switching frequency = 10 kHz) illustrates that the switch and diode junction temperature are 117.29°C and 122.27°C, respectively. The results show that mean time to failure for the buck converter is 32,973 hours.

Keywords: Reliability; Mean time to failure; Buck converter; Junction temperature.

Ocena zanesljivosti buck pretvornika na osnovi termične analize

Izvleček: V prispevku je predstavljena ocena zanesljivosti buck pretvornika na osnovi termične analize bipolarnega tranzostorja z izoliranimi vrati (IGBT) in diode. Termična analiza je uporabljena za določitev temperature spoja diode in stikala. Kriterij zanesljivosti je vpliv frekvence preklopa in obratovalnega cikla. Zgornja temperaturna meja je 150 °C. Simulacije 12 kW buck pretvornika (obratovalni cikel = 41%, frekvenca preklopa = 10 kHz) pokažejo temperaturo stikala 117.29 °C in spoja diode 122.27 °C. Povprečen pričakovani čas do okvare je 32,973 ur.

Ključne besede: zanesljivost; srednji čas do okvare; buck pretvornik; temperatura spoja.

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1 Introduction

In recent years, the use of renewable energy has become more popular because of the negative impacts of fossil fuels and the environmental pollution they cause. Nowadays, various methods and topologies for extracting energy from different renewable sources are being introduced. Solar energy, which can be harnessed using photovoltaic panels, is one of the alternative sources of energy and offers many advantages (such as less negative environmental effects and affordability) in comparison with other sources. As renewable energy sources continue to be used more often, more attention is now being paid to power electronics. A converter frequently used for photovoltaic panels in power electronics, as well as in several wind turbine energy conversion systems, is the dc–dc converter. In the last few decades, there have been many dc-dc converter topologies introduced, which have been generally classified based on the ratio of voltage output to input (also known as gain) into three fundamental groups: buck, boost, and buck-boost. This paper focuses on the buck converter type, often used in small or low power systems as a simple, remarkably efficient way to reduce the input voltage to a regulated dc voltage [1].

More efficient use of any device has always been a goal of manufacturers. In power electronics, the proper functioning of converters encompasses high output quality, a long lifespan, and less energy consumption. Due to the increase of power electronic converters in different devices, an especially important factor for optimizing converters is power quality, which can be described in terms of its thermal characteristics. Indeed,

previous researches have clarified the relationship of converter performance and quality in terms of heat loss [2–4]. Furthermore, Usui and Ishiko presented a simple approach for the thermal design of an IGBT module practised only in steady state operation [5].

In recent decades, different approaches for thermal analysis have also been introduced, including the highly accurate method of computational fluid dynamics (CFD), based upon how airflow conditions determine heat transfer coefficients [6].

Converter lifespan is another significant factor with a direct relationship to reliability, which represents the probability of failure in a system at a specific time [7]. The reliability of a system depends on various parameters; for this reason, identifying the indicators and calculation of the reliability parameters of the system's parts is required. Usually, two parameters are used to assess the reliability of the system. The first parameter is failure rate explained by failure distribution, and the next parameter is mean time to failure (MTTF) which presents the average operation time before the first failure of a component [8].

There are different researches related to the reliability assessment of various circuits and power converters. These circuits include multilevel inverters [9, 10], DC-DC converters [11], and AC-AC converters [12].

Khosroshahi et al. [13] evaluated the reliability of two conventional and interleaved DC-DC boost converters based on the MIL-HDBK-217 procedure. They found that the interleaved boost converter performs better in terms of reliability in comparison with the conventional boost converter. Perhaps, the most crucial weakness of this article is using approximate relations for calculating power dissipation in the switch and diode, which are based on their internal resistances.

Rashidi-Rad et al. [14] performed a reliability analysis of modular multilevel converters (MMCs) with the presence of half and full-bridge cells. Their examination illustrated that the modular converters that used half-bridge cells have more reliable performance than other state.

Arifujjaman and Chang [12] compared the reliability of three ac-ac converter namely intermediate boost converter (IBC), intermediate buck-boost converter (IBBC), and back-to-back converter (BBC) with the well-known matrix converter. They concluded that the intermediate boost converter exhibits more reliable than other ones.

In [15], the reliability of a buck converter was assessed in the presence of N-channel and P-channel MOSFET drivers. They showed that the considered buck converter has more reliability when an N-channel MOSFET is used as switch. However, they ignored some portions of the power losses in switch and diode, thus the obtained results may not be referred.

Ranjbar et al. [16] carried out a reliability assessment of single/two stage power factor correction (PFC) converters. The MIL-HDBL-217 was considered as reliability estimation procedure in this analysis. The outcomes demonstrated that the lifespan of a single-stage converter is about 1.6 times longer than the two-stage converter. In this study, for simplicity of calculations, the case temperature was intended to be a fix value of 35°C. This leads to an inaccuracy in the results.

The main purpose of this paper is to estimate the reliability of a buck converter based on the MIL-HDBK-217 standard. Although this standard has been criticized for being obsolete, it is still extensively used in military and aerospace industries to provide a basis for comparison between two or more different circuits [17]. For this reason, several previous literatures have employed this standard for predicting the reliability of power electronic converters (e.g., [18-22]). To investigate the reliability of semiconductor devices, there is a need for determining the junction temperature in these types of components, and in this study, the selected approach is based on information from manufacturer's datasheet. A one-cell Cauer thermal model was utilized in order to provide a precise relationship between the power losses and the junction temperatures in the presence of a heatsink. This approach has an acceptable result as well as suitable speed in calculations. Additionally, this is the first time that the simultaneous impact of switching frequency and duty cycle on the power losses and the junction temperature has been analyzed.

The rest of this paper is structured as follows: Section 2 describes the buck converter as a case study. The reliability principals employed for the analysis are discussed in Section 3. In Section 4, the accurate thermal analysis for the buck converter is discussed. In Section 5, the results and reliability evaluation are presented. Finally, conclusions are drawn in Section 6.

2 The buck converter

The buck converter circuit shown in Figure 1 is a highly efficient step-down dc-dc converter which is commonly used in switched-mode power supply circuits (SMPS). Generally, the dc input voltage of the buck converter

is derived from the output of a rectifier through a dc-link. In this paper, an IGBT is used as a switch for the converter. Also, the thermal analysis has been performed considering the effect of temperature on the voltage drop between the collector and emitter junctions of the diode and the transistor, because practically this voltage should be estimated by the means of both collector current and temperature, $V_{CE}(i_C, T_j)$.

The voltage drop for an IGBT can be experimentally measured by sensing the current of switch. Typically, a low-ohmic resistor is placed between the ground and emitter, and by flowing the current through this sensing resistor, the occurred voltage drop can be identified by another monitoring circuit. An improved sensing method is based on four external connection nodes for finding R_{DS}(on) of the switching power MOSFET, or V_{CE}(on) of an IGBT. The drawback of these methods is need for protection circuits and expensive discrete components against high voltage [23]. But, the employed approach in this paper will provide us the opportunity to identify the voltage drop indirectly.

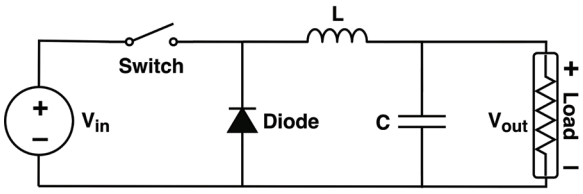

Figure 1: Topology of a buck DC-DC converter.

When the buck converter operates in continuous conduction mode (CCM), the current through the inductor (I_L) will never fall to zero during the cycle. Assuming the steady state operation for this converter, it can be concluded that the energy stored in each of circuit components at the end of a cycle is equal to energy stored at the beginning of the cycle. Therefore, the input and output voltages in the buck converter have a direct relationship with the duty cycle of the pulses, which can be shown as follows:

$$V_{out} = DV_{in} \tag{1}$$

where V_{out}, V_{in}, and D are the output voltage, the input voltage, and the converter duty cycle, respectively. With regard to the value of $0<D<1$, as a consequence, the output voltage is always lower than the input voltage. The basic characteristics of the converter are summarized in Table 1.

Table 1: Rated parameters for the desired buck converter.

Characteristic	Value
Rated output active power Po	12 kW
Input voltage Vin	300 V DC
Output voltage Vout	125 V DC ± 1.2%
Switching frequency fs	10 kHz
Inductor L	3 mH
Capacitor C	1 µF

A buck converter with parameters based upon Table 1 is simulated in MATLAB/Simulink. An open-loop controller is used for the simulation. Furthermore, a value of 42% is considered the duty cycle in this state. The results of the simulation are shown in Figure 2:

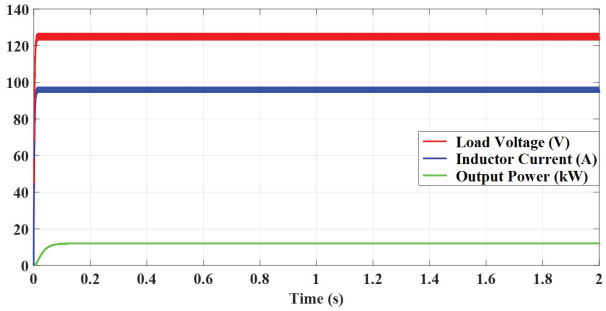

Figure 2: The simulation results of basic characteristics of the converter.

3 The reliability principle

Reliability means the ability of an item to perform a specific function under given conditions over a specific time period, which is expressed as a probability or failure frequency [24]. The importance of reliability in space and in the arms industry is more prominent than that of other industries because in these significant instruments, detecting or replacing a failed part is very difficult. Different methods have been introduced to improve the reliability of a system. One of these methods involves adding redundancy to parts of the converters, thereby increasing the global reliability of a system. Reliability is improved by adding more parts for redundancy, but cost is a deterrent to increasing the number of redundancy circuits [25].

One of the factors influencing reliability is failure rate. Failure rate can be expressed as the probability of failure per unit time occurring in the interval $[t,t+\Delta t]$, and there is no failure before time t. Usually, Δt is a very small value, and it is close to zero [26].

If we present a failure rate with λ, the probability distribution function for failure can be expressed as a relationship in terms of failure rate, and can be obtained using the exponential distribution. Equation (2) presents the distribution function:

$$f(t,\lambda) = \lambda e^{-\lambda t} \tag{2}$$

Also, the reliability function can be expressed as follows [8]:

$$R(t,\lambda) = e^{-\lambda t} \tag{3}$$

where in the above equations, λ is the component's failure rate. Another influential factor of reliability is mean time to failure (MTTF). MTTF is the average length of time before the first failure of a component or device occurs after it starts to work, after which the device is no longer able to continue with its normal operation. MTTF is expressed by the integral of reliability as follows:

$$MTTF = \int_0^{+\infty} R(t)\,dt \tag{4}$$

A simple equation for the expression of MTTF is derived by substituting Equation (3) with Equation (4):

$$MTTF = \frac{1}{\lambda} \tag{5}$$

In the last decades, various procedures have been introduced by different organizations to estimate the reliability. Some of the most popular procedures, such as RAC's PRISM [27], Telcordia SR-332 [28], SAE's PREL [29], CNET's reliability prediction method [30], Siemens SN29500 standard [31] and British Telecom's HRD-4 [32], are described and discussed according to the organization's strategies. A comprehensive comparison has been made among these procedures in [33]. Today, the MIL-HDBK-217F handbook is used as a suitable reference for estimating reliability. This paper also used a calculation based on the MIL-HDBK-217F procedure [34].

Two methods that include parts stress and parts count are discussed in the handbook. In the parts count method, less information is required, such as number of parts, quality level and environmental situation [35].

According to the series structure of the buck converter, the failure rate can be calculated using the summation of all failure rates of the circuit components, as shown in Equation (6) [36]:

$$\lambda_{System} = \sum \lambda_{Components} \tag{6}$$

where $\lambda_{Components}$ is the failure rate of each circuit component.

With the increasing complexity of the studied system, the overall system should be divided into subsystems so that the reliability evaluation becomes simpler and more concise [37].

3.1 The Reliability of Components

The buck converter consists of various components, including switch, diode, inductor and controller. In related studies on the reliability of electronic components (switches, diodes, capacitors and inductors), specific relationships for determining the failure rate for each component are expressed as follows [25, 34, 35, 38]:

$$\lambda_p(Capacitor) = \lambda_b \pi_{CV} \pi_Q \pi_E \tag{7}$$

$$\lambda_p(Inductor - Transformer) = \lambda_b \pi_C \pi_Q \pi_E \tag{8}$$

$$\lambda_p(Switch) = \lambda_b \pi_T \pi_A \pi_R \pi_S \pi_Q \pi_E \tag{9}$$

$$\lambda_p(Diode) = \lambda_b \pi_T \pi_C \pi_S \pi_Q \pi_E \tag{10}$$

In Equations (7)–(10), λ_b is the base failure rate, which is different for each component. Additionally, π_i is pi factor related to each component, and should be determined accurately. The controller failure rate can be considered 0.88 (failures/10^6 h) [35].

Due to the sudden progress of IGBTs, field data and reliability model related to this component are not available. Furthermore, one drawback of the employed standard is the lack of relationships for estimating the reliability of IGBT devices, because the latest update of the standard was before the comprehensive introduction of this kind of switch. In prior studies, some researchers preferred to use MOSFET equations for calculating IGBT failure rate [37], and alternatively, several papers claimed that using the reliability formulas of bipolar power transistors instead of IGBT would provide appropriate results [38]. In this paper, it is assumed that the IGBT modules have the same factors of high-power bipolar transistors. Another assumption is the fact that the value of base failure for an IGBT can be easily obtained by knowing the module's field data, and according to [38], its value for a medium-power IGBT is equal to 100 FIT ($\lambda_{b\,(S)}$ = 0.1 failures/10^6 h).

The factors π_Q and π_E, represent quality and environmental, respectively. The quality and environmental factor values can be assumed to be equal to one, although the effects of these two factors were eliminated [25]. Another factor is the application factor, π_A, and for switching application is equal to 0.7. The power rating factor, π_R, is directly related to the rated power which is equal to 10 for a 500 W IGBT module. The voltage stress factor for IGBT ($\pi_{S(S)}$) can be calculated by

$$\pi_{S(S)} = 0.045 \times \exp(3.1 \times V_{S(S)}) \tag{11}$$

where $V_{S(S)}$ is the ratio of applied collector-emitter voltage to rated voltage.

Diodes are usually used as power rectifiers in power electronic converters. In the industry, the diodes with a reverse recovery rate of 500 nanoseconds or less (approximately 0.1 of standard rectifiers) are categorized as fast rectifiers. If this period is reduced to 100 nanoseconds or less, they will be named as superfast rectifiers [39]. Given that the diodes within the IGBT modules are classified as fast recovery power rectifier, they must be set to the appropriate level according to the standard, and the base failure rate for the diodes will be equal to 0.025 failures/10^6 h.

In the following equation, $\pi_{S(D)}$ is the stress factor for diodes:

$$\pi_S = \left(V_{S(D)}\right)^{2.43} \tag{12}$$

where $V_{S(D)}$ is the ratio of operating voltage to nominal voltage.

π_C explains the contact construction. Considering it is metallurgically bonded, the contact construction leads to the value of 1 for π_C [35].

In the capacitor failure rate, π_{CV} is the capacitor factor which can be calculated as follows:

$$\pi_{CV} = 0.34 \times C^{0.12} \tag{13}$$

where C is the capacitance in microfarad.

The inductor base failure rate can be expressed as follows:

$$\lambda_{b(L)} = 0.000335 \times \exp\left(\frac{T_{HS} + 273}{329}\right)^{15.6} \tag{14}$$

where T_{HS} is the hot spot temperature in degree Celsius, which can be determined using Equation (15):

$$T_{HS} = T_A + 1.1 \times \Delta T \tag{15}$$

In Equation (15), T_A expresses the device ambient operating temperature in degree Celsius. Also, ΔT is the average temperature rise above the ambient [34, 35]. The inductor failure rate is much lower than other circuit components, so it can be omitted from the analysis.

The capacitor failure rate can be described by the following equation:

$$\lambda_{b(C)} = 0.00254\left[\left(\frac{S}{0.5}\right)^3 + 1\right]\exp\left(5.09 \times \left(\frac{T_A + 273}{378}\right)^5\right) \tag{16}$$

where S is the ratio of operating voltage to nominal voltage.

π_T is the temperature factor that, for the switch and diode, can be expressed as follows [35]:

$$\pi_{T(S)} = \exp\left(-2114 \times \left(\frac{1}{T_j + 273} - \frac{1}{298}\right)\right) \tag{17}$$

$$\pi_{T(D)} = \exp\left(-3091 \times \left(\frac{1}{T_j + 273} - \frac{1}{298}\right)\right) \tag{18}$$

where T_j is the junction temperature.

One of the major concerns regarding reliable power electronics is the operating temperature. Thus, it seems that the precise determination of the junction temperature results in a more accurate analysis of the reliability. There are five different approaches introduced by Reliability Analysis Center (RAC) to predict the junction temperature for semiconductor devices. In this study, Method IV was used. This method is utilized when a heatsink is mounted on the device, and the exact value of the case temperature is also available [40].

According to the used approach, the junction temperature can be calculated from Equation (19):

$$T_j = T_C + \theta_{jc} \times P_{loss} \tag{19}$$

In Equation (19), T_C is the heat sink temperature, θ_{jc} is the thermal resistance of the diode or switch, and P_{loss} is the total power losses of switch or diode.

In fact, Equation (19) exhibits a scheme of the one-cell Cauer thermal network. Figure 3 shows this modeling.

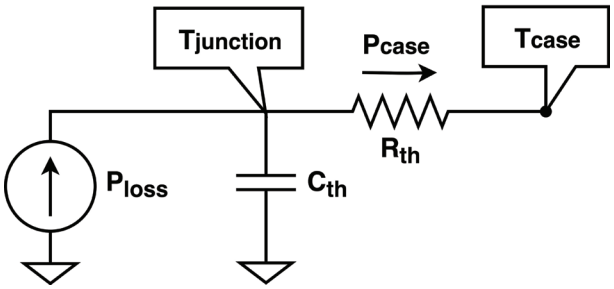

Figure 3: One-cell Cauer thermal network model.

In Figure 3, R_{th} and C_{th} are the thermal resistance and capacitance from junction-to-case, respectively, and these indicators should be selected from the datasheet of the used IGBT module (both diode and IGBT). Also, by similarity of thermal modeling and electrical modeling, the junction temperature can be found easily from the total power losses.

Foster and Cauer thermal network models are commonly used for dynamic thermal modeling, and both models use thermal resistance (*R*) and thermal capacitance (*C*), which are joined together as ladders and form multiple layers. Although many manufacturers of power modules typically offer the Foster model limited to four layers [41], the others only provide the transient thermal impedance curve (Z_{th}) within the datasheet; and the values for each layer should be obtained by curve fitting tools [42, 43] or algorithms [44]. Here, the particle swarm optimization (PSO) algorithm was used [45] to identify four RCs related to the four different layers.

Due to the need for a high number of simulations in this paper, a one-layer Cauer model has been employed for thermal analysis between junction and case. In addition to having the suitable precision, this model improves the simulation speed significantly. One issue for modeling thermal networks is the conversion of a Foster model to a Cauer model, and vice versa (for more details about these two thermal networks, refer to [46]). Considering that the four-layer Foster model is a four-order system, a circuit software is required to convert it to the first-order Cauer model. In this study, we used the LTspice software to find the values of R_{th} and C_{th} for the one-cell thermal model. The resistance of the single-layer model is equal to the sum of the four resistances of the four-layer model, which is the same as the peak of the thermal impedance curve. In order to determine the value of capacitance, a curve fitting on the outputs of the LTspice software was performed. Thus, the obtained values of the thermal resistance and capacitance for the Cauer network are 0.25 K/W and 0.18 J/K, respectively. Similarly, the extracted values for the diode are 0.46 K/W and 0.1 J/K, respectively.

To complete the thermal model, the heat transfer from the case to the ambient through the heatsink should also be added. Modeling of this part is shown in Figure 4.

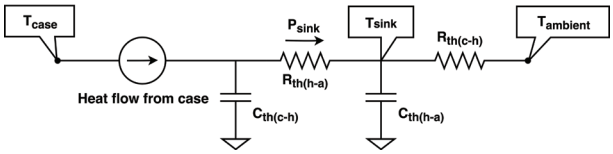

Figure 4: Thermal modeling from case-to-ambient.

In order to implement this part, the thermal and physical elements of MATLAB/Simulink have been used. The case-heatsink thermal resistance value ($R_{th(c-h)}$) is driven from the datasheet, and is equal to 0.05 K/W for the module under study. A 10-inch aluminum heatsink manufactured by the Wakefield-Vette under forced air cooling (500 feet per minute) is considered as the cooling system. According to the described circumstances, the value of $R_{th(h-a)}$ will be equal to approximately 0.1 K/W. For simplicity, we consider the case-heatsink thermal capacitance to be 0.25 J/K. The heatsink thermal capacitor is also assumed to be 0.01 J/K, based on [47].

Finally, as mentioned earlier, the determination of semiconductors' failure rate depends on their power losses. The utilized approach in this paper is based on calculating both conduction and switching losses for the diode and switch using lookup tables. Detailed explanation of this process is given in [48].

4 Thermal analysis of buck converter

In order to determine the thermal analysis of the converter, a Fuji 2MBI150U2A-060 600V/150A IGBT module is selected as the switch. The features of this module include high speed switching, voltage drive, and low inductance [49].

Figure 5 shows the IGBT on-state characteristics in 25°C and 125°C, based on Collector current versus Collector-Emitter voltage.

The rated current distributions for the switch and diode are shown is Figure 6, which this figure clearly demonstrates the summation of switch and diode currents can produce the inductor current (when the switch is on, the diode is off). Conversely, when the diode is on, the switch is off. The inductor current will be a triangular waveform when its voltage analogue is pulsating in a rectangular form

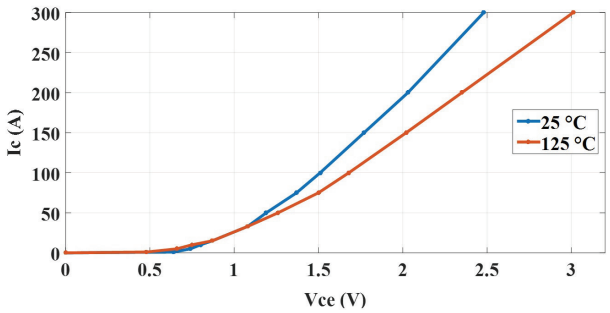

Figure 5: IGBT's Collector current in terms of Collector-Emitter voltage [49].

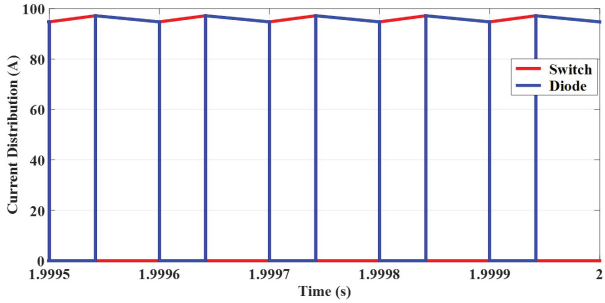

Figure 6: Current distributions of the switch and diode.

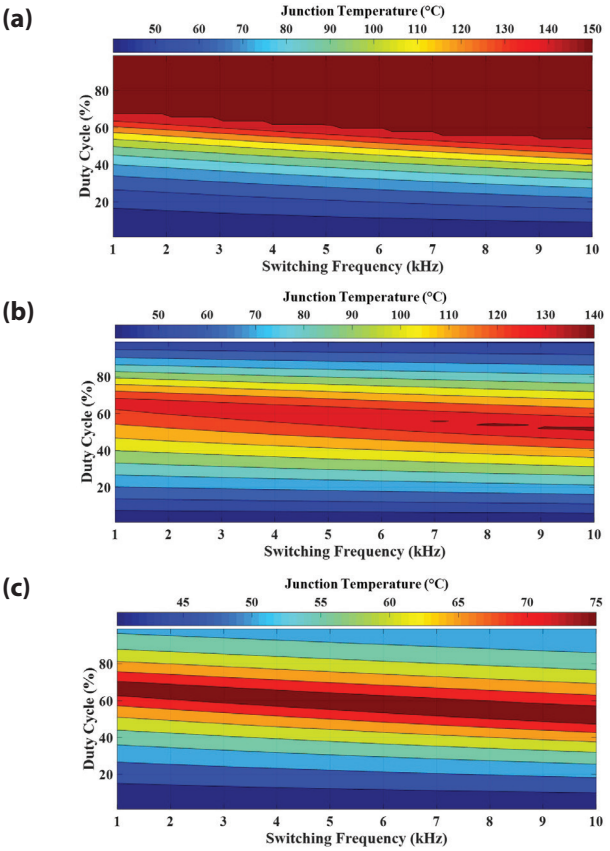

Figure 7: 2D plots for showing effects of duty cycle and switching frequency on (**a**) the switch junction temperature, (**b**) the diode junction temperature, (**c**) the heat sink temperature.

The most important factor in the evaluating converter reliability is temperature, which is directly related to power losses of the switch and diode. Thus, the calculation of the junction temperature is a sure way to assess reliability. Various elements can influence the junction temperature and its value will change with variations in component's power losses; increasing the switching frequency can lead to more power losses in the switch and diode. Another important factor for power losses in the buck converter is the modulation index or duty cycle. By setting a different duty cycle for the converter, the gain of the output voltage will change. An analysis is undertaken to show the effects of the switching frequency and the duty cycle on the junction temperature and the heat sink temperature. Figures 7 and 8 represent the items that can affect temperatures in the form of two-dimensional and three-dimensional diagrams.

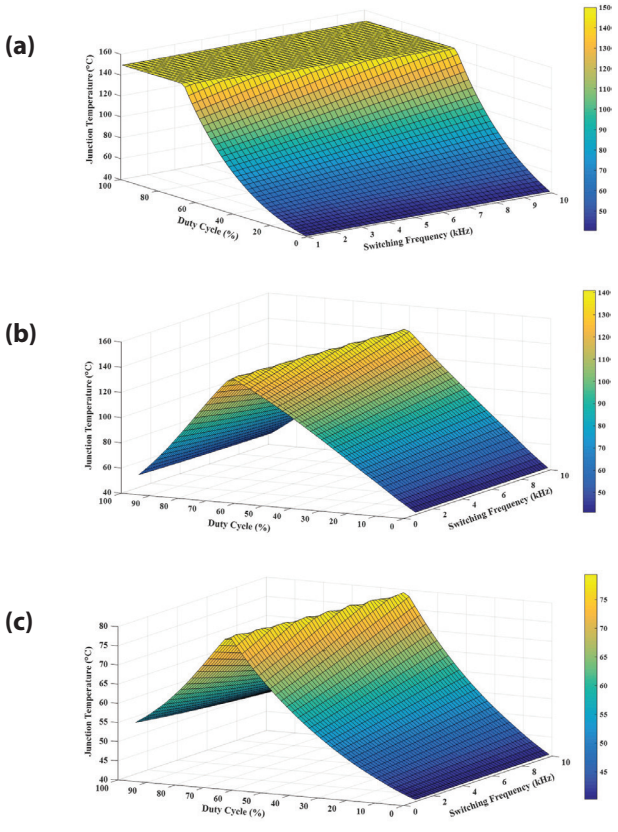

Figure 8: 3D plots for showing effects of duty cycle and switching frequency on (**a**) the switch junction temperature, (**b**) the diode junction temperature, (**c**) the heat sink temperature.

It is evident from Figures 7 and 8 that a lower duty cycle corresponds to a better performance in terms of temperature because of the decrease in the output voltage level. Therefore, it is possible to change the duty cycle to its desired value by changing the basic

characteristics of the converter. Increasing switching frequency from 1 to 10 kHz has a negligible impact on the temperature, but switching frequencies higher than 10 kHz will increase the temperature. The over-temperature is limited to 150°C, so the converter ceases to operate beyond this temperature. For duty cycles higher than 51%, the junction temperature of the switch rises beyond the over-temperature. This shows the weakness of heatsink for cooling the module under thermal pressure. Using a more efficient heatsink will result in a decrease in the junction temperature and the extension of authorized period for increasing the duty cycle. The calculated power losses for the switch and diode (based on the rated parameters) are 145.02 W and 89.69 W, respectively. Also, the results illustrate that the switch junction temperature for a duty cycle of 42% and f_s = 10 kHz is 117.29°C. The junction temperature of the diode is 122.27°C, and it has a higher value than the switch's temperature.

Although the diode power losses are less than the switch, due to the greater diode thermal resistance in comparison with the switch (0.46 compared to 0.25 K/W), the diode junction temperature would be higher. This issue can also be deduced from the physical structure of the IGBT module, because the cross-section of the diode chip is smaller than the switch, and with the same heat flux applied to the both chips, the smaller chip will experience higher temperature increase. This shows that greater thermal resistance can produce higher junction temperatures.

Typically, the heat sink temperature is much lower than that at the junction of other components, and in reliability designs, a temperature of 40°C is considered a stable value for the temperature of the heat sink [50]. However, the structure and design of the heat sink can affect its operating temperature. The simulation results showed that the heat sink temperature measured with the parameters rated was 69.32°C.

5 The reliability evaluation of buck converter

Estimated failure rates for each component under identical conditions are shown in Tables 2-5. Due to the application of the switch, a value of 0.7 is considered to be the application factor. Values of π_Q and π_E were set for the components according to [34].

A value of 0.88 was considered to be the failure rate of the controller, similar to [35], and the failure rate of the converter can be estimated by summing all of the failure rates (we only have one from each component). The failure rate of the entire system was calculated at 30.328 (failures/10^6 h) by the following equation:

$$\lambda_{System} = \sum n_i \lambda_i = \left\{ \begin{matrix} \lambda_{P\,(S)} = 27.188 \\ \lambda_{P\,(D)} = 2.014 \\ \lambda_{P\,(C)} = 0.197 \\ \lambda_{P\,(L)} = 0.049 \\ \lambda_{P\,(Controller)=0.88} \end{matrix} \right\} + \quad (20)$$

By reversing the failure rate, MTTF can be calculated as follows:

$$MTTF = \frac{1}{\lambda_{System}} = \frac{10^6}{30.328} = 32,973\,\text{hours} \quad (21)$$

Table 2: The estimated base failure rate for the switch.

P_{Loss} (W)	T_j (°C)	π_T	π_A	π_R	π_S	π_E	π_Q	λ_b	λ_P (failures/10^6 h)
145.02	117.29	5.35	0.7	10	0.22	6	5.5	0.1	27.188

Table 3: The estimated base failure rate for the diode.

P_{Loss} (W)	T_j (°C)	π_T	π_C	π_S	π_E	π_Q	λ_b	λ_P (failures/10^6 h)
89.69	122.3	12.85	1	0.19	6	5.5	0.025	2.014

Table 4: The estimated base failure rate for the capacitor.

Value	T_A (°C)	π_{CV}	π_E	π_Q	λ_b	λ_P (failures/10^6 h)
1 µF	40	0.34	2	10	0.029	0.197

Table 5: The estimated base failure rate for the inductor.

T_A (°C)	T_{HS} (°C)	π_C	π_E	π_Q	λ_b	λ_P (failures/10^6 h)
40	69.32	1	4	20	6.22×10^{-4}	0.049

6 Conclusion

A new approach to reliability assessment based on thermal analysis of the switch and diode was presented. The thermal analysis of a buck converter with the basic characteristics shown in Table 1 was conducted by calculating the temperature at the switch and diode junction. The total failure rate of the converter was expressed by summing the failure rate of the components using the parts count method. The procedure employed for the reliability analysis was that given in the MIL-HDBK-217F handbook. The results of the simulation using MATLAB Simulink showed that the buck converter analyzed will operate reliably for 3.8 years, which is an acceptable performance.

7 References

1. Huangfu Y, Ma R, Liang B, Li Y. "High power efficiency buck converter design for standalone wind generation system". *International Journal of Antennas and Propagation*, 1, 1-9, 2015. https://doi.org/10.1155/2015/751830
2. Stupar A, Bortis D, Drofenik U, Kolar JW. "Advanced setup for thermal cycling of power modules following definable junction temperature profiles". *Power Electronics Conference (IPEC)*, Sapporo, Japan, 21-24 June 2010. https://doi.org/10.1109/IPEC.2010.5542179
3. Zhang MT, Jovanovic M, Lee FC. "Design and analysis of thermal management for high-power-density converters in sealed enclosures". *Applied Power Electronics Conference and Exposition*, Atlanta, Georgia, 23-27 Feb 1997. https://doi.org/10.1109/APEC.1997.581482
4. Bašić M, Vukadinović D, Polić M. "Analysis of power converter losses in vector control system of a self–excited induction generator". *Journal of Electrical Engineering*, 65(2), 65-74, 2014. https://doi.org/10.2478/jee-2014-0010
5. Usui M, Ishiko M. "Simple approach of heat dissipation design for inverter module". *Proc. of International Power Electronics Conference (IPEC 2005)*, Niigata, Japan, 4-8 April 2005.
6. Lee TT, Mahalingam M. "Application of a CFD tool for system-level thermal simulation". *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A*, 17(4), 564-572, 1994. https://doi.org/10.1109/95.335043
7. Lee Y, Hwang D. "A study on the techniques of estimating the probability of failure". *Journal of Chungcheong Mathematical Society*, 21(4), 573-583, 2008.
8. Stapelberg RF. *Handbook of reliability, availability, maintainability and safety in engineering design*. 1st ed. London, UK, Springer Science & Business Media, 2009.
9. Ding Y, Loh PC, Tan KK, Wang P, Gao F. "Reliability Evaluation of Three-Level Inverters". *Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Palm Springs, USA, 21-25 February 2010. https://doi.org/10.1109/APEC.2010.5433438
10. Alavi O, Hooshmand-Viki A, Shamlou S. "A comparative reliability study of three fundamental multilevel inverters using two different approaches". *Electronics*, 5(2), 1-18, 2016. https://doi.org/10.3390/electronics5020018
11. Dhople SV, Davoudi A, Domiínguez-Garciía AD, Chapman PL. "A unified approach to reliability assessment of multiphase DC–DC converters in photovoltaic energy conversion systems". *IEEE Transaction on Power Electronics*, 27(2), 739-751, 2012. https://doi.org/10.1109/TPEL.2010.2103329
12. Arifujjaman M, Chang L. "Reliability comparison of power electronic converters used in grid-connected wind energy conversion system". *3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Aalborg, Denmark, 25-28 June 2012. https://doi.org/10.1109/PEDG.2012.6254021
13. Khosroshahi A, Abapour M, Sabahi M. "Reliability evaluation of conventional and interleaved DC-DC boost converters". *IEEE Transactions on Power Electronics*, 30(10), 5821-5828, 2015. https://doi.org/10.1109/TPEL.2014.2380829
14. Rashidi-rad N, Rahmati A, Abrishamifar A. "Comparison of reliability in modular multilevel inverters". *Przeglad Elektrotechniczny (Electrical Review)*, 88(1), 268–272, 2012.
15. Javadian V, Kaboli S. "Reliability assessment of some high side MOSFET drivers for buck converter". *International Conference on Electric Power and Energy Conversion Systems*, Istanbul, Turkey, 2-4 October 2013. https://doi.org/10.1109/EPECS.2013.6713092
16. Ranjbar AH, Abdi B, Gharehpetian GB, Fahimi B. "Reliability assessment of single-stage/two-stage PFC converters". *Compatibility and Power Electronics Conference*, Badajoz, Spain, 20-22 May 2009. https://doi.org/10.1109/CPE.2009.5156043
17. Harb S, Balog RS. "Reliability of candidate photovoltaic module-integrated-inverter (PV-MII) topologies—A usage model approach". *IEEE Transactions on Power Electronics*, 28(6), 3019-3027, 2013. https://doi.org/10.1109/TPEL.2012.2222447

18. Parvari R, Zarghani M, Kaboli S. "RCD snubber design based on reliability consideration: A case study for thermal balancing in power electronic converters". *Microelectronics Reliability*, 88, 1311-1315, 2018. https://doi.org/10.1016/j.microrel.2018.06.072
19. Ristow A, Begovic M, Pregelj A, Rohatgi A. "Development of a methodology for improving photovoltaic inverter reliability". *IEEE Transactions on Industrial Electronics*, 55(7), 2581-2592, 2008. https://doi.org/10.1109/TIE.2008.924017
20. Gupta N, Garg R, Kumar P. "Sensitivity and reliability models of a PV system connected to grid". *Renewable and Sustainable Energy Reviews*, 69, 188-196, 2017. https://doi.org/10.1016/j.rser.2016.11.031
21. Kadwane SG, Kumbhare JM, Gawande SP, Mohanta DK. "Reliability evaluation of BLDC drive in refrigeration systems". *42th Industrial Electronics Society Conference*, 23 October, pp. 6645-6650, 2016. https://doi.org/10.1109/IECON.2016.7793538
22. Memon HH, Alam MM. "Reliability, maintainability, availability and failure rate analysis of IGBT triggering system designed for marine environment". *13th International Bhurban Conference on Applied Sciences and Technology (IBCAST)*, 12 January, pp. 295-299, 2016. DOI: https://doi.org/10.1109/IBCAST.2016.7429893
23. Chen J. A Smart IGBT Gate Driver IC with Temperature Compensated Collector Current Sensing. PhD [dissertation]. University of Toronto, 2018.
24. Wang H, Ma K, Blaabjerg F. "Design for reliability of power electronic systems". *38th Annual Conference on IEEE Industrial Electronics Society*, Montreal, Canada, 25-28 October 2012. https://doi.org/10.1109/IECON.2012.6388833
25. Richardeau F, Pham TT. "Reliability calculation of multilevel converters: Theory and applications". *IEEE Transactions on Industrial Electronics*, 60(10), 4225-4233, 2013. https://doi.org/10.1109/TIE.2012.2211315
26. Lyu MR. *Handbook of software reliability engineering*. 1st ed. New York, NY, USA, IEEE computer society press, 1996.
27. Denson WA. "Tutorial: PRISM". *RAC Journal*, 1-6, 1999.
28. Telcordia Technologies. "Special Report SR-332: Reliability Prediction Procedure for Electronic Equipment (Issue 1)". Telcordia Customer Service, Piscataway, USA, 2001.
29. SAE G-11 Committee. "Aerospace Information Report on Reliability Prediction Methodologies for Electronic Equipment AIR5286". Draft Report, 1998.
30. Union Technique de L'Electricité. "Recueil de données des fiabilite: RDF 2000. Modèle universel pour le calcul de la fiabilité prévisionnelle des composants, cartes et équipements électroniques". 2000.
31. Siemens AG. "Siemens Company Standard SN29500 (Version 6.0). Failure Rates of Electronic Components". Siemens Technical Liaison and Standardization, 1999.
32. British Telecom. "Handbook of Reliability Data for Components Used in Telecommunication Systems". London, UK, 1987.
33. Pecht MG, Nash FR. "Predicting the reliability of electronic equipment [and prolog]". *Proceedings of the IEEE*, 82(7), 992-1004, 1994. https://doi.org/10.1109/5.293157
34. "MIL-HDBK-217F (Notice 2). Military handbook: Reliability prediction of electronic equipment". Department of Defense, USA, 1995.
35. Abdi B, Ranjbar AH, Gharehpetian GB, Milimonfared J. "Reliability considerations for parallel performance of semiconductor switches in high-power switching power supplies". *IEEE Transactions on Industrial Electronics*, 56(6), 2133-2139, 2009. https://doi.org/10.1109/TIE.2009.2014306
36. Rausand M, Hoyland A. *System reliability theory: Models, statistical methods, and applications*. 2nd ed. New York, NY, USA, Wiley, 2004.
37. Aten M, Towers G, Whitley C, Wheeler P, Clare J, Bradley K. "Reliability comparison of matrix and other converter topologies". *IEEE Transactions on Aerospace and Electronic systems*, 42(3), 2006. https://doi.org/10.1109/TAES.2006.248190
38. Chen G, Burgos R, Liang Z, Lacaux F, Wang F, Van Wyk JD, Odendaal WG, Boroyevich D. "Reliability-oriented design considerations for high-power converter modules". *35th Annual Power Electronics Specialists Conference*, pp. 419-425, 2004. https://doi.org/10.1109/PESC.2004.1355782
39. Walters K. *Rectifier Reverse Switching Performance*, Microsemi, 1998.
40. Chan F, Calleja H. "Reliability estimation of three single-phase topologies in grid-connected PV systems". *IEEE Transactions on Industrial Electronics*, 58(7), 2683–2689, 2011. https://doi.org/10.1109/TIE.2010.2060459
41. Ma K, He N, Liserre M, Blaabjerg F. "Frequency-domain thermal modeling and characterization of power semiconductor devices". *IEEE Transactions on Power Electronics*, 31(10), 7183-7193, 2016.
42. Pandya KL, McDaniel W. "A simplified method of generating thermal models for power MOSFETs". *18th Annual Symposium on Semiconductor Thermal Measurement and Management*, pp. 83-87, 2002. https://doi.org/10.1109/STHERM.2002.991350

43. Ram SS, Vijayakumari A. "Thermal modeling of wide bandgap semiconductor devices for high frequency power converters". *IOP Conference Series: Materials Science and Engineering*, 2018. https://doi.org/10.1088/1757-899X/310/1/012133
44. Fraisse G, Souyri B, Pinard S, Ménézo C. "Identification of equivalent thermal RC network models based on step response and genetic algorithms". *12th Conference of International Building Performance Simulation Association*, Sydney, 2011.
45. Chen TY, Kuo SL, Hsu JM, Pan CW. "Dynamic compact thermal modeling of package-on-package by thermal resistor-capacitor ladder". *15th Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, pp. 223-229, 2016. https://doi.org/10.1109/ITHERM.2016.7517554
46. Stout R. "How to Use Thermal Data Found in Data Sheets. ON Semiconductor Application Note AND8220", *ON Semiconductor Products Inc.*, Phoenix: Arizona, 2006.
47. Schonberger J. "Thermal Simulation of a Buck Converter". Plexim GmbH, 2010.
48. Graovac D, Purschel M. "IGBT Power losses calculation using the data-sheet parameters". Infineon Application Note, Neubiberg, Germany, 2009.
49. Fuji Electric Device Technol. Co. Ltd. "Fuji 2MBI150U2A-060 600V/150A IGBT module datasheet". Fuji IGBT Modules Application Manual. Application Note, Feb 2004.
50. Ma K, Munoz-Aguilar RS, Rodriguez P, Blaabjerg F. "Thermal and efficiency analysis of five-level multilevel-clamped multilevel converter considering grid codes". *IEEE Transactions on Industry Applications*, 50(1), 415-423, 2014. https://doi.org/10.1109/TIA.2013.2266391

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Elliptically polarized frequency agile antenna on ferroelectric substrate

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Abstract: A low-profile, compact and frequency-tunable antenna made on ferroelectric substrate is presented. It is designed as a planar dipole antenna with an IDC varactor integrated in the signal line. Antenna is fed through a coplanar waveguide matched to 50 Ω. The center frequency can be tuned from 6.895 GHz to 7.050 GHz. It exhibits elliptical polarization and omnidirectional radiation pattern.

Keywords: Frequency-tunable antenna; ferroelectric thin films; $(Ba,Sr)TiO_3$

Eliptično polarizirana in frekvenčno nastavljiva antena na feroelektrični podlagi

Izvleček: Predstavljena je frekvenčno nastavljiva planarna antena z majhnim profilom izdelana na feroelektrični podlagi. Zasnova antene temelji na planarnem dipolu z interdigitalnim varaktorjem, ki je integriran v signalni liniji. Napajana je skozi koplanarni valovod z imedanco 50 Ω. Resonančna frekvenca antene je prilagodljiva v območju med 6.895 GHz in 7.050 GHz. Antena ima eliptično polarizacijo in omni-smerni diagram sevanja.

Ključne besede: Frekvenčno nastavljiva antena; feroelektrične tanke plasti; $(Ba,Sr)TiO_3$

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1 Introduction

Nowadays Earth and space communication modules provide multiple services on different frequencies with constant demand for reduced dimensions of the communication devices. Reduced dimensions of the chassis often result in either compact antennas with narrow bandwidth or in complex multiband design. Frequency-agile antennas, on the other hand, are attractive as they are small and can at the same time seamlessly cover a wide frequency range [1, 2].

A simple way to tune antenna is to load it with varactors. In the past years thin-film ferroelectric varactors have been extensively studied for possible use in frequency-agile microwave devices [3, 4]. Lumped-element microwave circuits based on ferroelectrics are advantageous over the competing technologies, i.e., semiconductor varactors and micro-electro-mechanical systems (MEMS), in terms of space-radiation stability, reliability and their rapid response [5, 6]. High-density integrated circuits based on ferroelectric thin films with thicknesses below 1 μm can be produced on a single substrate, which increases the fabrication output and reduces the cost.

This paper presents a novel antenna architecture with integrated ferroelectric varactor, which was designed to manufacture a simple yet efficient tunable antenna

for satellite communications at frequencies between 6.875 and 7.050 GHz. In addition to tunable center frequency it is characterized also with elliptical polarization and good cosmic irradiation hardness [7]. Antenna is fed through a coplanar waveguide (CPW) loaded with an interdigital (IDC) varactor made on $Ba_{0.3}Sr_{0.7}TiO_3$ thin-film substrate. Biasing of the varactor is achieved through the CPW signal line, with RF signal and bias separated with 1 MΩ resistor.

2 Antenna fabrication and design

Resonant frequency of the antenna can be effectively changed by adding a variable capacitor (varactor) at its feed point. Polycrystalline ferroelectric film, with the composition of $Ba_{0.3}Sr_{0.7}TiO_3$, was deposited by cost-efficient Chemical Solution Deposition on ~250 µm-thick polished polycrystalline Al_2O_3 substrate (CoorsTek Inc., Golden, USA, ε = 9.9). Thickness of the film was increased by several deposition-heating steps to 240 nm and the final annealing was performed at 900 °C [8]. Dielectric permittivity ε and losses tanδ of the films were measured at 9.6 GHz using split-post dielectric resonators (QWED, Warsaw, Poland) and were found to be 640 and 0.02, respectively.

Dipole antenna fed by a coplanar waveguide with integrated BST varactor was found to give the best compromise between the requirements, i.e., working frequency range, and its characteristics, i.e., dimensions and efficiency. The structure was patterned by lift-off photolithography and top Cr/Cu electrodes with 15 nm of Cr and 2 µm of Cu were deposited by DC sputtering (Balzers Sputron, Oerlikon Balzers, Liechtenstein). Its configuration is shown in Fig. 1. Width and spacing of the 50 Ω CPW feed line are 1050 µm and 250 µm, respectively. The IDC fingers are 185 µm long, 10 µm wide and have a 5 µm gap between them. Magnified view of the 12-fingered IDC varactor is shown in the inset of Fig. 1.

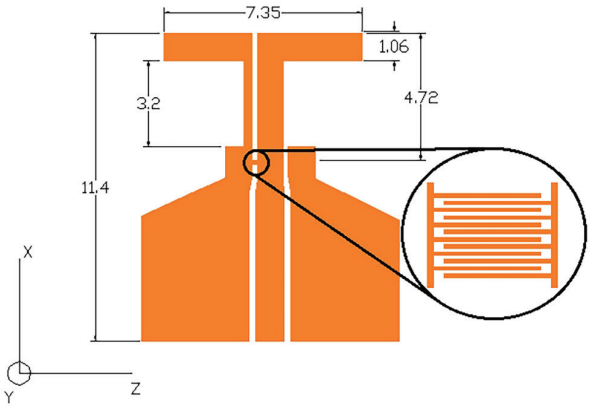

Figure 1: Configuration of the proposed tunable dipole antenna. Dimensions are given in mm.

To facilitate the measurement, an SMA connector was mounted at the edge of the CPW. The photography of the fabricated antenna and the optical micrograph of the IDC varactor are shown in Fig. 2(a) and (b), respectively.

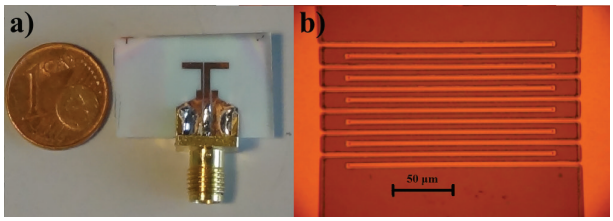

Figure 2: (a) fabricated tunable dipole antenna and (b) IDC varactor.

3 Measurement results and comparison with existing solutions

Return loss S_{11} of the tunable dipole antenna measured at applied bias voltage up to 50 V is shown in Fig. 3. The resonant frequency changes between 6.875 GHz for 0 V bias and 7.050 GHz for 50 V bias, which translates into tuning range of approximately 3 %. Higher voltages detune the antenna to the point where it is no longer viable for space communication.

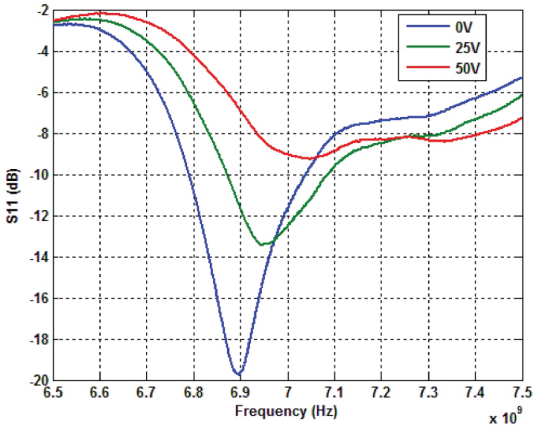

Figure 3: Measured return loss S_{11} of the tunable dipole antenna.

Far-field radiation patterns were measured in the MVG Satimo StarLab (MVG Industries, Villebon-sur-Yvette, France) near field measurement chamber (Fig. 4). Currents flowing on the outside of the coaxial cable shield were suppressed as much as possible with the use of ferrite chokes, which can be seen as white cylinders near the antenna in Fig. 4. The radiation patterns at 6.875 GHz under 0 V bias are presented in Fig. 5, while the Axial Ratio (AR) is shown in Fig. 6. In X-Y plane antenna has an almost omnidirectional

pattern. In the Z-X plane antenna has maximum gain in X axis and minimum in Z axis, which is typical for dipole antenna radiation pattern, although it is not perfect. It has a higher gain in -X direction compared to +X direction (Fig. 5a) and higher gain in X-axis compared to Y-axis. This can be explained with the current flowing on the antenna between the horizontal arms and ground plane shown in Figure 7. Maximum gain is 1.6 dBi. AR measurement shows that antenna is linearly polarized in Z-X plane but has a significantly lower AR in X-Y plane, i.e. it is elliptically polarized in Y axis (Fig. 6).

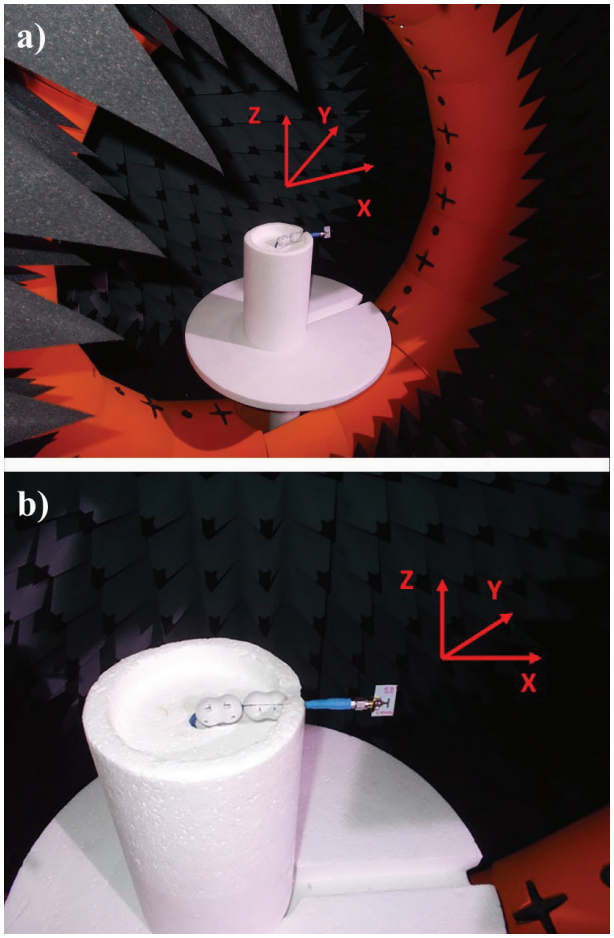

Figure 4: a) Measurement set-up for far-field radiation measurements with mounted antenna. b) Detailed view of the same set-up.

Elliptical polarization and irregular radiation pattern can be explained by examining the current distribution on the antenna, which was simulated with Sonnet Software 3D planar high-frequency electromagnetic software and is shown in Fig. 6. Vertical parts of the antenna between horizontal dipole and ground plane are electrically far apart. Consequently, currents flowing into the antenna though the signal line and out of the antenna through the ground plane do not cancel each other out. Antenna is therefore radiating not only from its horizontal parts, as could be expected for a dipole antenna, but also from its vertical parts. This induces vertical component into the radiated electromagnetic field.

Compared to the existing literature data on tunable antennas based on BST-film varactors, the 3 % tuning of resonant frequency at 50 V exceeds the values reported for slot loop antennas, for which either 3 % or 1 % tuning was achieved with 200 [9] and 40 V bias

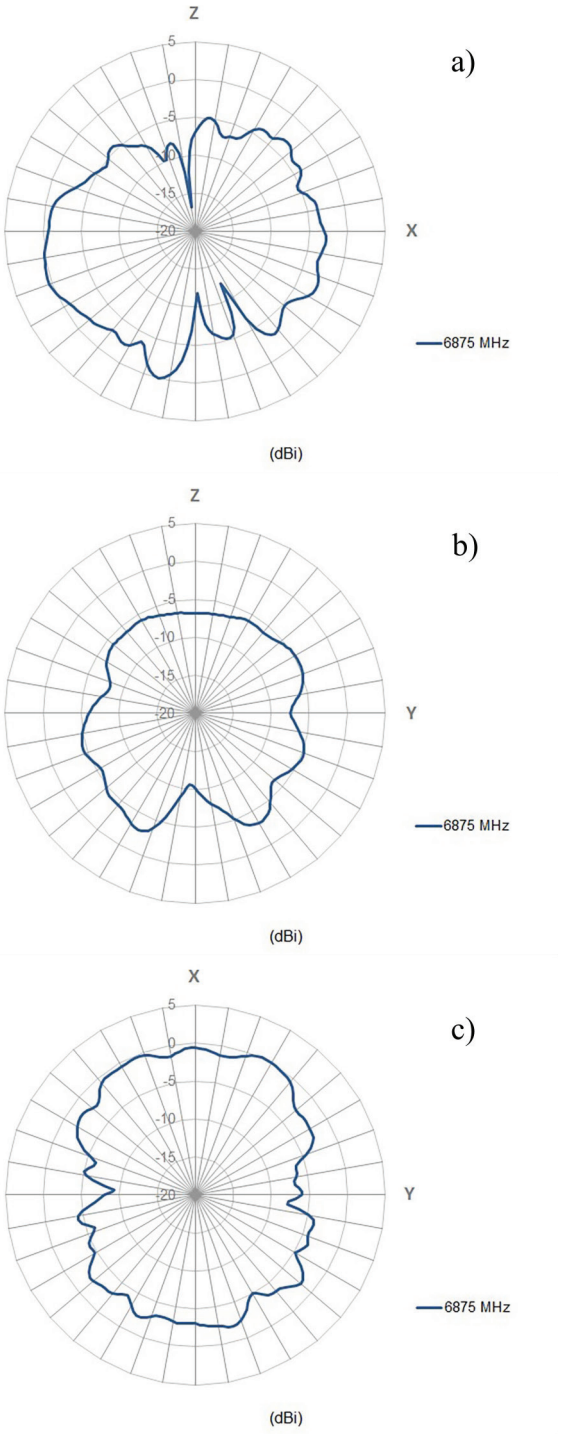

Figure 5: 2D radiation patterns measured at 6.875 GHz. a) Z-X plane, b) Z-Y plane and c) X-Y plane.

[10], respectively. However, it is inferior to the 8 % tuning achieved with 10 V in Bowtie antenna with three IDC varactors integrated in the feed line [11].

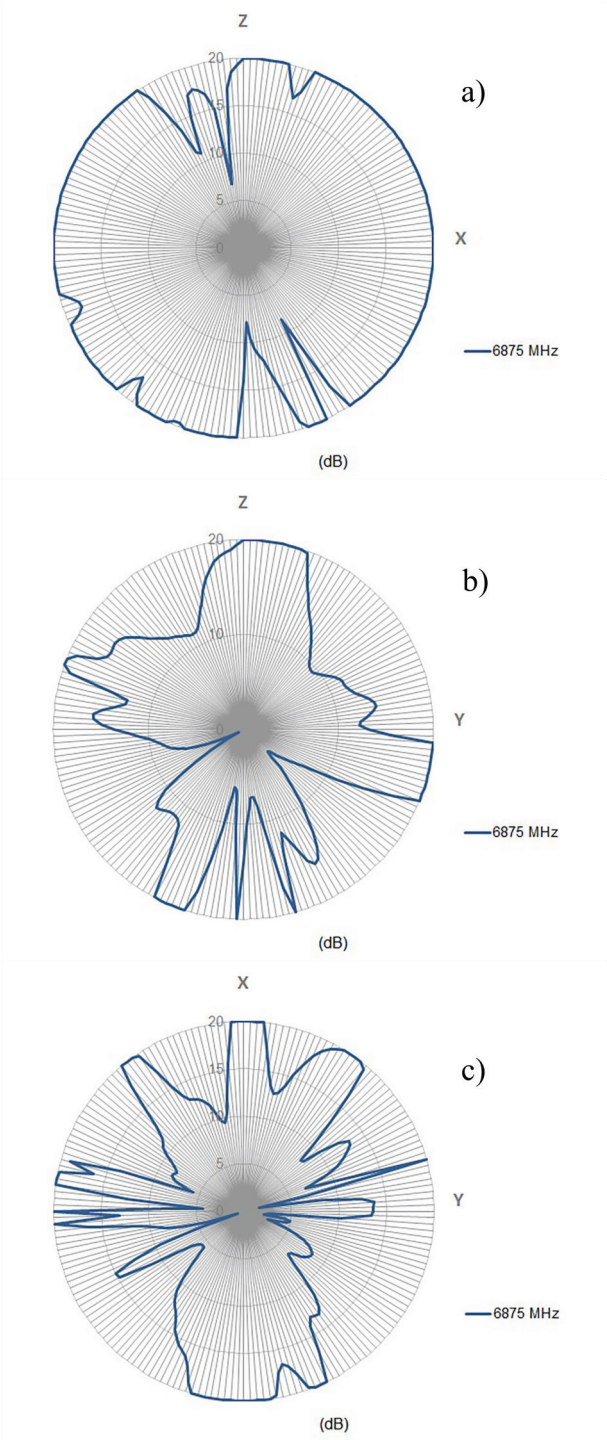

Figure 6: Axial Ratio diagrams measured at 6.875 GHz. a) Z-X plane, b) Z-Y plane and c) X-Y plane.

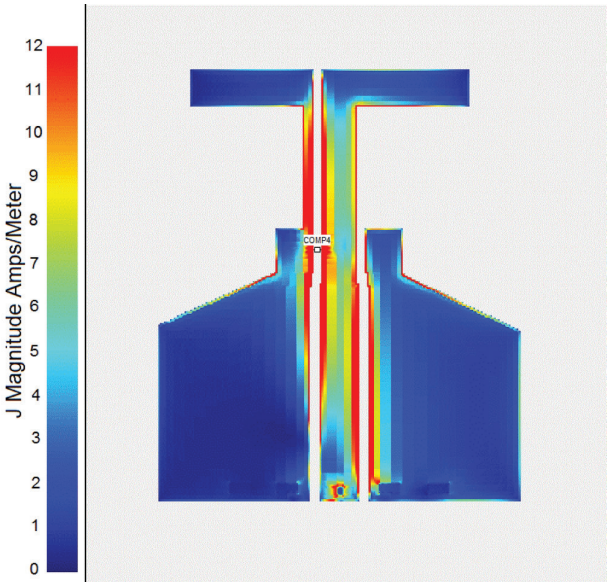

Figure 7: Tunable dipole antenna current distribution at 6.875 GHz.

4 Summary

A low-cost and compact frequency agile antenna on ferroelectric substrate was made and measured. An IDC varactor integrated in the antenna can shift its resonant frequency by 3 % when bias voltage of 50 V is applied. In Y-axis antenna exhibits elliptical polarization with low axial ratio, which is desirable in Earth and satellite communication as it reduces fading of the signal. Design allows a compact, lightweight and low cost manufacturing, which is anticipated for space applications.

5 Acknowledgments

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6 References

1. J. M. Carrere, R. Staraj, G. Kossiavas, "Small Frequency Agile Antennas", Electronics Letters, vol. 37, no. 12, June 2001, pp. 728-729, 2001. https://doi.org/10.1049/el:20010529
2. R. T. Cutshall, R. W. Ziolkowski, "Performance Characteristics of Planar and Three-Dimensional Versions of a Frequency-Agile Electrically Small Antenna", IEEE Antenn. Propag. M., vol. 56, no.

6, pp. 53-71, 2014. https://doi.org/10.1109/MAP.2014.7011020
3. Y. Zheng, A. Hristov, A. Giere, R. Jakoby, "Suppression of harmonic radiation of tunable Planar Inverted-F Antenna by ferroelectric varactor loading", IEEE MTT-S Microwave Symposium Digest, pp. 959–962, 2008. https://doi.org/10.1109/MWSYM.2008.4632993
4. H. Jiang, M. Patterson, C. Zhang, G. Subramanyam, "Frequency tunable microstrip patch antenna using ferroelectric thin film varactor", Proceedings of the IEEE 2009 National Aerospace & Electronics Conference, pp. 248–250, 2009. https://doi.org/10.1109/NAECON.2009.5426620
5. S. Gevorgian, "Ferroelectrics in microwave devices, circuits and systems: physics, modeling, fabrication and measurements", Springer, London, 2010.
6. R. Sayyah, T. C. Macleod, F. D. Ho, "Radiation-hardened electronics and ferroelectric memory for space flight systems", Ferroelectrics, vol. 413, no. 1, pp. 170-175, 2011. https://doi.org/10.1080/00150193.2011.554145
7. S. Glinšek, T. Pečnik, V. Cindro, B. Kmet, B. Rožič, B. Malič, "Role of the microstructure in the neutron and gamma-ray irradiation stability of solution-derived $Ba_{0.5}Sr_{0.5}TiO_3$ thin films", Acta Mater., Vol. 88, pp. 34-40, 2015. https://doi.org/10.1016/j.actamat.2015.01.028
8. T. Pečnik, S. Glinšek, B. Kmet, B. Malič, "Combined effects of thickness, grain size and residual stress on the dielectric properties of $Ba_{0.5}Sr_{0.5}TiO_3$ thin films", J. Alloy. Compd., vol. 646, pp. 766-772, 2015. https://doi.org/10.1016/j.jallcom.2015.06.192
9. V. K. Palukuru, M. Komulainen, T. Tick, J. Perantie, H. Jantunen, "Low-Sintering-Temperature Ferroelectric-Thick Films: RF Properties and an Application in a Frequency-Tunable Folded Slot Antenna", IEEE Antenna and Wireless Propagation Letters, vol. 7, pp. 461-464, 2008. https://doi.org/10.1109/LAWP.2008.2001120
10. H. Y. Li, H. P. Chen, S. C. Chen, C. H. Tai, J. S. Fu, "A tunable slot loop antenna using interdigitated ferroelectric varactors", IEEE Antennas and Propagation Society Symposium, 2012. https://doi.org/10.1109/APS.2012.6348537
11. K. C. Pan, H. Jiang, D. Brown, C. H. Zhang, M. Patterson, G. Subramanyam, "Frequency tuning of CPW bowtie antenna by ferroelectric BST thin film varactors", Proceedings of the 2011 IEEE National Aerospace and Electronics Conference, 2011. https://doi.org/10.1109/NAECON.2011.6183066

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Electrochemical acetylcholinesterase biosensor for detection of cholinesterase inhibitors: study with eserine

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Abstract: Cholinesterase inhibitors are widely used as pesticides, as chemical warfare agents and as drugs to treat symptoms of Alzheimer's disease. Therefore, it is a high need to develop methods for their detection which are fast, sensitive, and reliable. This paper reports a preliminary work in the development of an electrochemical biosensor based on acetylcholinesterase (AChE) which is constructed by immobilization layers – cysteamine/glutaraldehyde/AChE on thin layer gold electrode for detection of cholinesterase inhibitors. Eserine (physostigmine) was used as a test inhibitor. The enzyme immobilization efficacy was evaluated by measuring activity of immobilized enzyme via Ellman's method. The enzyme activity of the initial reduction of 33% in five days remained after that stable for at least one week. Chronoamperometric response to substrate acetylthiocholine chloride (ATCl) was assumed to follow Michaelis-Menten kinetics. After exposure biosensor to 25 μM eserine for 10 min, 70% inhibition of enzyme was detected. Reactivation factor of inhibited AChE was determined as 0.016 min^{-1}.

Keywords: Electrochemical biosensor; Acetylcholinesterase; Eserine; Ellman assay; Chronoamperometry; Cyclic voltammetry

Elektrokemijski acetilholinesterazni biosenzor za detekcijo holinesteraznih inhibitorjev: raziskava z eserinom

Izvleček: Holinesterazni inhibitorji se pogosto uporabljajo kot pesticidi, kot kemična bojna sredstva ali kot zdravila za zdravljenje simptomov Alzheimerjeve bolezni, zaradi česar je razvoj hitrih, občutljivih in zanesljivih metod za njihovo zaznavanje izrednega pomena. Članek podaja rezultate začetnih raziskav v razvoju elektrokemijskega biosenzorja za detekcijo inhibitorjev acetilholinesteraze (AChE). Biosenzor je zgrajen na steklenem substratu, na katerem je strukturirana tankoplastna zlata elektroda. Na njej so imobilizirani cisteamin/glutaraldehid/AChE. Kot testni inhibitor je uporabljen eserin (fizostigmin). Učinkovitost imobilizacije encima smo spremljali z merjenjem aktivnosti imobiliziranega encima z Ellmanovo metodo. Po petih dneh od izdelave biosenzorja se je aktivnost encima stabilizirala. Kronoamperometrični odziv na substrat acetiltioholin klorid (ATCl) je predpostavljeno sledil kinetiki Michaelisa in Mentenove. Po 10 minutni izpostavljenosti biosenzorja 25 μM eserinu smo detektirali 70% inhibicijo encima. Reaktivacijski faktor inhibiranega AChE je bil 0.016 min^{-1}.

Ključne besede: elektrokemijski biosenzor; acetilholinesteraza; eserin; Ellmanova metoda; kronoamperometrija; ciklična voltametrija

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1 Introduction

In 1962, Clark and Lyons proposed the initial concept of glucose enzyme electrodes which led to a powerful analytical instrument for the detection of glucose in samples from patients with diabetes. This resulted in popularization of biosensors [1, 2]. In comparison with the conventional analytical techniques (such as chromatography and mass spectrometry), biosensors are typically easy to use, suitable for *in situ* measurement, and low cost [3]. Biosensors are remarkably diverse,

comprising a wide range of combinations of biorecognition and transduction elements [4, 5]. Enzymes are the most often used bio-recognition elements, whereas the most widely applied biosensors are based on electrochemical transduction method [6].

Enzyme-based biosensors are implemented in direct or indirect form [5]. One example of indirect form option is cholinesterase (ChE) biosensors which are based on enzyme inhibition [7, 8]. They are useful tools for detection of ChE inhibitors. The most widespread applications of such biosensors are detection of pesticides (organophosphates and carbamates) and warfare nerve agents (sarin) [6]. ChE inhibitors are also recognized as prevailing choice (galantamine, rivastigmine, donepezil) in the treating of Alzheimer's disease symptoms [9]. For these applications, the inhibitors detection and analysis are of great importance. Eserine has been used by many researchers as a reference standard in the evaluation of new ChE inhibitors [10]. Eserine can be found naturally in the Calabar bean. Eserine binds at both the anionic and esteric sites of acetylcholinesterase (AChE), forming a drug-enzyme complex. The mechanism is not completely reversible [11].

This paper reports construction of an AChE biosensor based on immobilization layers of cysteamine, glutaraldehyde, and AChE, which are chemically bound to the thin gold electrode layer. Cyclic voltammetry (CV) and chronoamperometry (CA) were applied to demonstrate the fasibility of fabricated biosensor structure for the detection of one well-known and important neurotransmitter inhibitor eserine.

2 Materials and methods

2.1 Chemicals

Following compounds were purchased from Merck (Germany): 95-98% H_2SO_4, 30% H_2O_2, 100 mM cysteamine, glutaraldehyde 5% (v/v), AChE from electric eel (50 U/mL), 100 mM K-P buffer solution with pH = 8.0 (47 mL 1 M K_2HPO_4 + 3 mL 1 M KH_2PO_4 + 450 mL miliQ water), 5 mM (if not specified differently) substrate acetylthiocholine chloride solution (ATCl), and 10 mM eserine. 0.1 M KCl containing 2 mM ferri/ferro-cyanide were prepared and purchased from Merck and Fluka (Belgium), respectively.

2.2 Instruments

Spectrophotometry was carried out by microplate reader Cytation 3 from BioTek (Germany).

CV and CA measurements were carried out using potentiostat EmStat3+ Blue equipped with PSTrace 5.3 software from PalmSens BV (The Netherlands). Miniature Ag/AgCl, 3 M KCl reference electrode, model ET073 was from eDAQ Pty Ltd (Australia).

2.3 Biosensor structure

Electrodes. Replaceable chip, containing an array of 6 thin layer gold working electrodes (Figure1a) was manufactured. Gold electrodes were applied on glass substrate using microfabrication processes – sputtering of Cr/Au with thicknesses 30 nm/120 nm, photolithography patterning and wet etching. The diameter of the working electrodes was 0.3 cm, resulting in an apparent geometric area of 0.07 cm^2. As counter (or auxiliary) electrode, platinum wire was used, and it was wrapped around the external reference electrode (Figure 1b). All three electrodes were installed in an originally designed electrochemical cell with reservoir volume of 5 mL (Figure 1c). Chip with working electrodes in electrochemical cell was connected to potentiostat (Figure 1d) with spring tips.

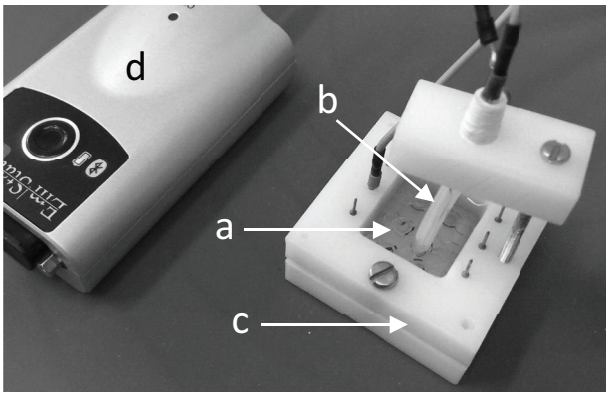


Figure 1: Experimental setup of biosensor.

AChE immobilization. Gold electrode chip was first cleaned with piranha solution (H_2SO_4:H_2O_2 in volume ratio 3:1), for 10 minutes. Thereafter, the electrode chip was well rinsed with ultrapure water and imme-

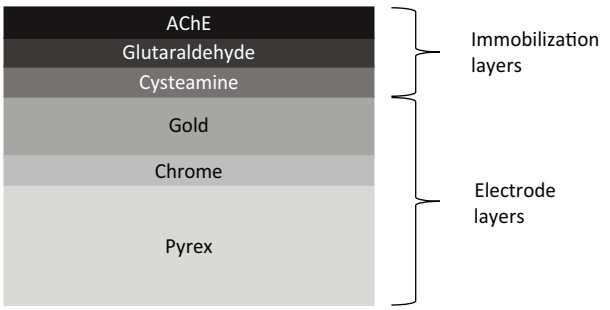


Figure 2: AChE immobilized gold electrode.

diately immersed in cysteamine, glutaraldehyde aqueous solution and in AChE solution as described in [12]. Schematic description of resulting sample structure is shown in Figure 2.

2.4 Measurement procedure

AChE activity measurement. AChE hydrolyses ATCl to acetate and thiocholine chloride (TChCl) which can be further measured spectrophotometrically [13]. Standard spectrophotometric Ellman colorimetric assay [14] was used to check the efficacy of the enzyme immobilization procedure on the gold surface. Test gold plated glass with 0.2 cm^2 had AChE immobilized as described previously. The absorbance of yellow product 5-thio-2-nitrobenzoate (TNB) was measured after reaction time of 10 minutes and the product quantity was evaluated using the Lambert-Beer law as Eq. 1 [15]:

$$Product\ quantity = \frac{AV}{\varepsilon l} \tag{1}$$

where A is absorbance at 405 nm, V is volume of the sample (products TChCl, Ellman's reagent, K-P buffer), ε known molar extinction coefficient of TNB (ε = 14,150 $M^{-1}cm^{-1}$ [16] and l is the beam length in the sample, respectively. In our case parameters were: V = 250 µL, l = 0.75 cm.

CV and CA techniques [17] were applied to measure enzyme activity on immobilized gold electrode chip. In the case of measurement by CV, the input voltage

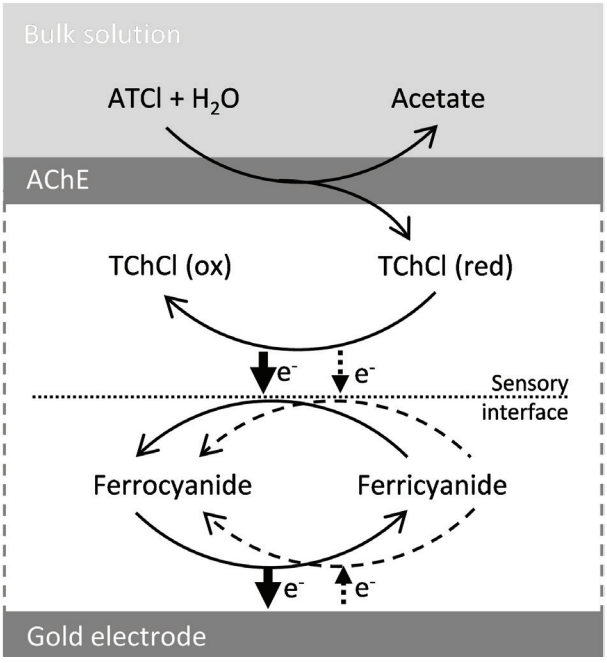


Figure 3: Sequence of reactions occurring at AChE biosensor.

was scanned from -0.1 V to +0.6 V, with potential step of 0.01 V and scan rate of 0.06 V/s. CA measurement was carried out at DC potential of 0.4 V. Measurements, if not specified differently, were performed 10 minutes after exposure substrate ATCl to AChE enzyme. Substrate was dissolved in K-P buffer and solution of ferricyanide with KCl. Sequence of reactions occurring at an AChE biosensor is shown schematically in Figure 3. The result of the ATCl hydrolysis is the electrochemically active TChCl, which exchanges an electron with an electrochemical mediator ferricyanide when passing from reduction to oxidation state. Mediator transfers the electron to the electrode via redox reactions. Oxidation and reduction process on cyclic voltammogram are referred to solid and dashed lines in Figure 3, respectively [18, 19]. Electrons on the electrode are detected by external electrical circuit (potentiostat).

AChE inhibition measurement. AChE biosensor is based on enzymatic inhibition mechanism. Eserine as analyte inhibits the normal enzyme function. The enzyme inhibition is therefore determined by the difference in measured electric currents in the absence (i_0) and presence (i_i) of eserine. The inhibition is calculated as Eq. 2 [20]:

$$Inhibition = \left(i_0 - i_i\right) / i_0 \tag{2}$$

Measuring protocol of AChE inhibition was performed in three steps. The biosensor was immersed in the substrate ATCl solution and solution of ferricyanide with KCl, for 10 min and the signal i_0 was measured (step 1). Then, the AChE biosensor was rinsed three-times with the K-P buffer solution (step 2) and immersed in a new substrate and ferricyanide solution with eserine addition for reaction and incubation time of 10 min, then residual activity i_i was measured (step 3).

3 Results and discussion

Activity of the immobilized enzyme was evaluated spectrophotometrically by measuring the quantity of produced thiocholine chloride product. The activity was monitored in time period of 12 days (Figure 4).

From Figure 4 it can be seen that after 33% initial decrease of enzyme activity in five days, the activity remained steady for at least one week. The reason for large initial loss of activity can be attributed to stabilization of biostructure or incomplete covalent binding of the enzyme, surface defects and impurity of enzyme.

After confirming immobilized enzyme activity by Ellman's method, AChE biosensor performance was investigated by CV and CA measurements on biosensor

electrode structure. Figure 5 shows CV response obtained in absence and in presence of ATCl.

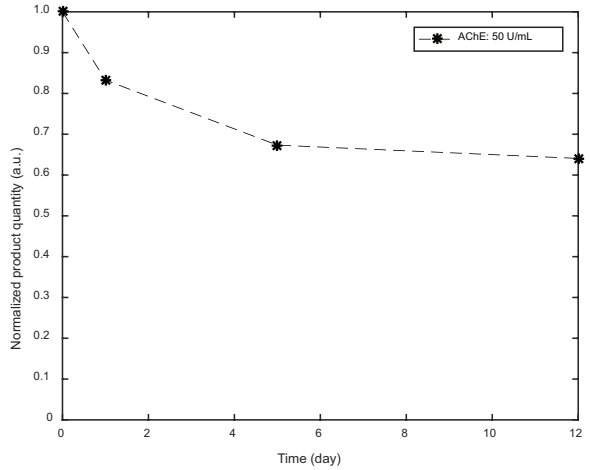


Figure 4: Spectrophotometrical measurement of time dependent AChE activity.

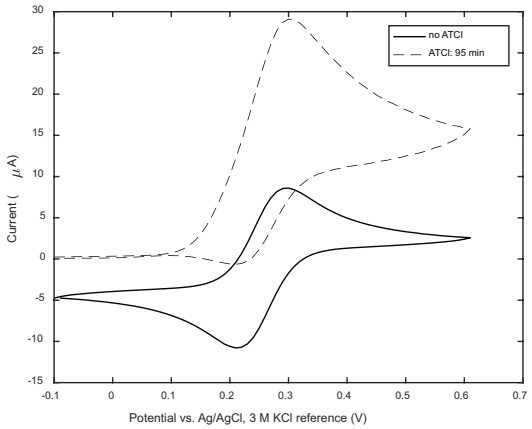
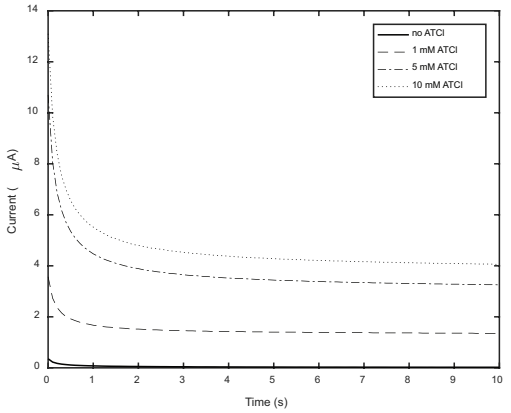


Figure 5: Cyclic voltammogram obtained in absence (solid line) and in presence of substrate ATCl (discontinuous line) in the presence of redox couple ferri/ferro-cyanide. The reaction with substrate refer to ATCl hydrolysis, catalysed by the enzyme AChE.

Addition of ATCl causes an increase in concentration of TChCl and consequently of the ferrocyanide, resulting in an increase of the anodic peak current. On the contrary, the cathodic peak current is proportional to the amount of ferricyanide that decreases after the addition of ATCl. This can be seen in Figure 5, where anodic peak current I_{pa} increases and cathodic peak current I_{pc} decreases with time of TChCl present. Therefore, we can determine a ratio I_{pa}/I_{pc}. The ratio of the peak currents is equal to one for reversible system of ferro/ferri-cyanide, shown by solid line in Figure 5. Larger peak current difference is obtained for reaction with ATCl, shown by dashed line in Figure 5, for the reaction time of 95 min. The corresponding ratio of the peak currents was therefore determined as 3.1. This confirms higher rate of oxidation and consequently concentration of produced TChCl.

Figure 6 shows measured current by CA technique and fitted result (solid line) versus ATCl concentration.

(a)



(b)

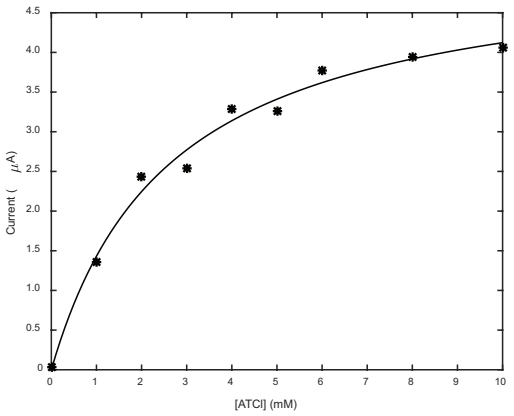


Figure 6: Selected chronoamperometric curves (a) from which (at 10 s) calibration plot of ATCl using the AChE biosensor is constructed (b).

Relation between electrical current and concentration of substrate ATCl was assumed to follow Michaelis-Menten kinetics (Eq. 3) [21], being aware that many other factors can affect the results [22]:

$$V_0 = \frac{V_{max}[S]}{K_M + [S]} \tag{3}$$

where V_0 is initial velocity, V_{max} is maximum velocity, [S] is substrate concentration, and K_M is Michaelis constant. According to the curve fit of measured points in Figure 6 (solid line), the calculated apparent Michaelis constant $K_M^{app} = 2.6 \pm 0.9$ mM was determined.

Finally, after determining production of TChCl by AChE biosensor, AChE inhibition was chronoamperometricaly detected by using well-established commercially available AChE inhibitor eserine. The inhibition of AChE was determined by measuring the decrease of the CA signal, which is consequence of eserine addition to the ATCl substrate solution. Result of inhibition for 25 μM of concentration of eserine is presented in Figure 7.

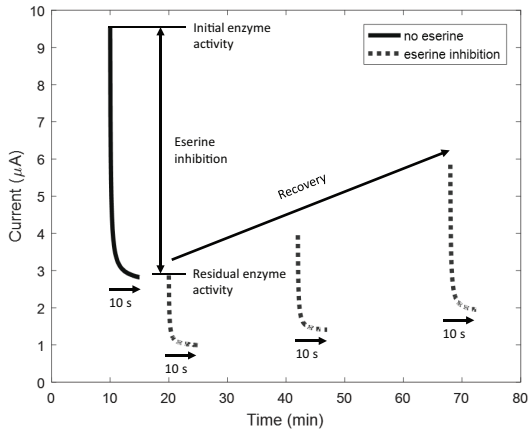


Figure 7: Study of AChE inhibition by eserine.

Both, initial enzyme inhibition in value of 70% and recovery of AChE activity are presented in Figure 7. After 10 minutes of inhibition by eserine, samples were repeatedly rinsed and re-measured, noting the significant recovery of the signal. Note that each measurement, presented in Figure 7, lasted only 10 s, while time on x-axis shows the total time of experiment duration. It can be seen that recovery of AChE activity increases almost linearly with time (20 to 68 min) when system was not exposed to eserine, recovering to 59% and 39% of inhibition at 42 and 68 min, respectively.

An important kinetic parameter of inhibited AChE is the reactivation factor K_{react}. By applying Perola's equation (Eq. 4), the reactivation factor K_{react} was calculated from the inclination of the linear plot obtained by monitoring the inhibition as a function of time [23]:

$$\ln\left(\frac{Inhibition_t}{Inhibition_0}\right) = -K_{react}t \quad (4)$$

where $Inhibition_0$ is the first measured current after inhibitor addition, which corresponded to $t = 0$ of the decarbamoylation phase, and $Inhibition_t$ is the inhibition determined as a function of time during the enzyme activity recovery phase. K_{react} of 0.016 min^{-1} was determined, and it is in good agreement with the literature data [24].

4 Conclusions

The AChE electrochemical biosensor is presented. It is successfully applied for detection of eserine as an example of choline inhibitor in water.

Spectrophotometric measurements have shown that five days after AChE immobilisation on gold surface activity of an enzyme decreased for 33% and then remained stable an extended period of time.

Biosensor was evaluated via CV and CA measurements. CV measurement of enzyme activity resulted in asymmetric cyclic voltammogram, i.e. increase of anodic peak current and decrease of cathodic peak current (ratio 3:1). This confirms higher rate of oxidation and consequently concentration of produced TChCl. Moreover, relation between electrical current and concentration of substrate ATCl up to 10 mM were assumed to follow Michaelis Menten kinetics. Apparent Michaelis constant was determined as 2.6 ± 0.9 mM.

Our results have shown that 25 μM eserine inhibits the activity of AChE for 70%. Reactivation factor of 0.016 min^{-1} was determined, showing reversibility of AChE inhibition by eserine.

Presented work is to be further extended to determine biosensor sensitivity, reliability and concentration dependent inhibition of eserine and other AChE inhibitors.

5 Acknowledgments

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6 References

1. A. P. F. Turner, 'Biosensors: sense and sensibility', *Chemical Society Reviews*, vol. 42, no. 8, p. 3184, 2013. https://doi.org/10.1039/c3cs35528d
2. L. C. Clark and C. Lyons, 'Electrode systems for continuous monitoring in cardiovascular surgery', *Annals of the New York Academy of Sciences*, vol. 102, no. 1, pp. 29–45, Oct. 1962. https://doi.org/0.1111/j.1749-6632.1962.tb13623.x
3. A. Amine, S. Cinti, F. Arduini, D. Moscone, and G. Palleschi, 'How to extend range linearity in enzyme inhibition-based biosensing assays', *Talanta*, vol. 189, pp. 365–369, Nov. 2018. https://doi.org/10.1016/j.talanta.2018.06.087
4. D. R. Thévenot, K. Toth, R. A. Durst, and G. S. Wilson, 'Electrochemical biosensors: recommended definitions and classification1', *Biosensors and Bioelectronics*, vol. 16, no. 1–2, pp. 121–131, 2001. https://doi.org/10.1081/AL-100103209
5. D. G. Rackus, M. H. Shamsi, and A. R. Wheeler, 'Electrochemistry, biosensors and microfluidics: a

convergence of fields', *Chemical Society Reviews*, vol. 44, no. 15, pp. 5320–5340, 2015. https://doi.org/10.1039/C4CS00369A
6. Š. Štěpánková and K. Vorčáková, 'Cholinesterase-based biosensors', *Journal of Enzyme Inhibition and Medicinal Chemistry*, vol. 31, no. sup3, pp. 180–193, Nov. 2016. https://doi.org/10.1080/14756366.2016.1204609
7. L. Matějovský and V. Pitschmann, 'New Carrier Made from Glass Nanofibres for the Colorimetric Biosensor of Cholinesterase Inhibitors', *Biosensors*, vol. 8, no. 2, p. 51, May 2018. https://doi.org/10.3390/bios8020051
8. V. Dhull, A. Gahlaut, N. Dilbaghi, and V. Hooda, 'Acetylcholinesterase Biosensors for Electrochemical Detection of Organophosphorus Compounds: A Review', *Biochemistry Research International*, vol. 2013, pp. 1–18, 2013. https://doi.org/10.1155/2013/731501
9. W. Hussein *et al.*, 'Synthesis and Biological Evaluation of New Cholinesterase Inhibitors for Alzheimer's Disease', *Molecules*, vol. 23, no. 8, p. 2033, Aug. 2018. https://doi.org/10.3390/molecules23082033
10. T. J. Petcher and P. Pauling, 'Cholinesterase Inhibitors: Structure of Eserine', *Nature*, vol. 241, p. 277, Jan. 1973. https://doi.org/10.1038/241277a0
11. L. -G. Zamfir, L. Rotariu, and C. Bala, 'Acetylcholinesterase biosensor for carbamate drugs based on tetrathiafulvalene–tetracyanoquinodimethane/ionic liquid conductive gels', *Biosensors and Bioelectronics*, vol. 46, pp. 61–67, Aug. 2013. https://doi.org/10.1016/j.bios.2013.02.018
12. F. Arduini, S. Guidone, A. Amine, G. Palleschi, and D. Moscone, 'Acetylcholinesterase biosensor based on self-assembled monolayer-modified gold-screen printed electrodes for organophosphorus insecticide detection', *Sensors and Actuators B: Chemical*, vol. 179, pp. 201–208, Mar. 2013. https://doi.org/10.1016/j.snb.2012.10.016
13. F. Arduini, A. Amine, D. Moscone, and G. Palleschi, 'Biosensors based on cholinesterase inhibition for insecticides, nerve agents and aflatoxin B1 detection (review)', *Microchimica Acta*, vol. 170, no. 3–4, pp. 193–214, Sep. 2010. https://doi.org/10.1007/s00604-010-0317-1
14. G. L. Ellman, K. D. Courtney, V. Andres, and R. M. Featherstone, 'A new and rapid colorimetric determination of acetylcholinesterase activity', *Biochemical Pharmacology*, vol. 7, no. 2, pp. 88–95, Jul. 1961. https://doi.org/10.1016/0006-2952(61)90145-9
15. G. L. Ellman, 'Tissue sulfhydryl groups', *Archives of Biochemistry and Biophysics*, vol. 82, no. 1, pp. 70–77, May 1959. https://doi.org/10.1016/0003-9861(59)90090-6
16. M. Pohanka, M. Hrabinova, K. Kuca, and J. -P. Simonato, 'Assessment of Acetylcholinesterase Activity Using Indoxylacetate and Comparison with the Standard Ellman's Method', *International Journal of Molecular Sciences*, vol. 12, no. 4, pp. 2631–2640, Apr. 2011. https://doi.org/10.3390/ijms12042631
17. N. Elgrishi, K. J. Rountree, B. D. McCarthy, E. S. Rountree, T. T. Eisenhart, and J. L. Dempsey, 'A Practical Beginner's Guide to Cyclic Voltammetry', *Journal of Chemical Education*, vol. 95, no. 2, pp. 197–206, Feb. 2018. https://doi.org/10.1021/acs.jchemed.7b00361
18. P. Abad-Valle, H. Y. Aboul-Enein, J. Adrian, and S. Alegret, 'Contributors to Volume 49', vol. 49, p. 1308.
19. Faculty of Chemical Technology, University of Pardubice, Studentska 95, Pardubice, Czech Republic and A. Kostelnik, 'Electrochemical Determination of Activity of Acetylcholinesterase Immobilized on Magnetic Particles', *International Journal of Electrochemical Science*, pp. 4840–4849, Jun. 2016. https://doi.org/10.20964/2016.06.39
20. S. Kurbanoglu, C. C. Mayorga-Martinez, M. Medina-Sánchez, L. Rivas, S. A. Ozkan, and A. Merkoçi, 'Antithyroid drug detection using an enzyme cascade blocking in a nanoparticle-based lab-on-a-chip system', *Biosensors and Bioelectronics*, vol. 67, pp. 670–676, May 2015. https://doi.org/10.1016/j.bios.2014.10.014
21. R. F. Boyer, *Concepts in Biochemistry*, 3 edition. Hoboken, NJ: Wiley, 2005.
22. M.-P. Bucur, B. Bucur, and G.-L. Radu, 'Critical Evaluation of Acetylthiocholine Iodide and Acetylthiocholine Chloride as Substrates for Amperometric Biosensors Based on Acetylcholinesterase', *Sensors (Basel)*, vol. 13, no. 2, pp. 1603–1613, Jan. 2013. https://doi.org/10.3390/s130201603
23. M. Vandeput *et al.*, 'Flow-through enzyme immobilized amperometric detector for the rapid screening of acetylcholinesterase inhibitors by flow injection analysis', *Journal of Pharmaceutical and Biomedical Analysis*, vol. 102, pp. 267–275, Jan. 2015. https://doi.org/10.1016/j.jpba.2014.09.012
24. E. Perola, L. Cellai, D. Lamba, L. Filocamo, and M. Brufani, 'Long chain analogs of physostigmine as potential drugs for Alzheimer's disease: new insights into the mechanism of action in the inhibition of acetylcholinesterase', *Biochimica et Biophysica Acta (BBA) - Protein Structure and Molecular Enzymology*, vol. 1343, no. 1, pp. 41–50, Nov. 1997. https://doi.org10.1016/S0167-4838(97)00133-7

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Orthodox Theory Monte-Carlo Simulation of Single-Electron Logic Circuits

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Abstract: In the past decades MOS based digital integrated logic circuits have undergone a successful process of miniaturisation eventually leading to dimensions of a few nanometres. With the dimensions in the range of a few atomic radii the end of conventional MOS technology is approaching. Amongst the prospective candidates for sub 10nm logic are integrated logic circuits based on single-electron devices. In our contribution we present the use of MOSES (Monte-Carlo Single-Electronics Simulator) as a method for simulation of complementary single-electron logic circuits based on the orthodox theory. Simulations of single-electron devices including a single-electron box, a single-electron transistor and a complementary single-electron inverter were carried out. Their characteristics were evaluated at different temperatures and compared to measurement results obtained at other institutions. The potential for room-temperature operation was also assessed.

Keywords: single-electron logic circuits; single-electron transistor; Monte-Carlo; simulation; MOSES; voltage-state logic

Monte-Carlo simulacija enoelektronskih logičnih vezij na podlagi Ortodoksne teorije

Izvleček: V preteklih desetletjih je MOS tehnologija uspešno prestala proces miniaturizacije, kar je privedlo do dimenzij struktur v rangu nanometrov. Dimenzije, ki obsegajo le še nekaj atomski polmerov, bi lahko napovedovale konec konvencionalne MOS tehnologije. Kot eden izmed glavnih kandidatov za logična vezja, ki bodo delovala pri dimenzijah okoli 10nm in manj, se omenjajo logična vezja na osnovi enoelektronskih gradnikov. V našem prispevku bomo predstavili uporabo simulacijskega orodja MOSES (Monte-Carlo Single-Electronics Simulator), kot metode za simulacijo komplementarnih enoelektronskih digitalnih logičnih vezij na podlagi Ortodoksne teorije. Izvedli smo simulacije enoelektronskih struktur vključno z enoelektronsko škatlo, enoelektronskim tranzistorjem in komplementarnim enoelektronskim inverterjem. Njihove karakteristike smo ovrednotili pri različnih temperaturah in primerjali z izmerjenimi karakteristikami z drugih raziskovalnih ustanov. Ocenili smo tudi možnost delovanja enoelektronskih vezij pri sobni temperaturi.

Ključne besede: enoelektronska logična vezja; enoelektronski tranzistor; Monte-Carlo; simulacija; MOSES; logika stanj napetosti

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1 Introduction

In the last 50 years since the invention of CMOS technology in 1963 the aforementioned technology has gained a huge advantage mainly due to its small power dissipation. Through the continuous process of miniaturisation the reduction of device dimensions from 5 µm to 14 nm was achieved [1]. Conventional CMOS technology is bound to reach its limits in the near future and in order to sustain device miniaturisation other technological options should be employed.

One of the prospective candidates for the implementation of sub-10 nm digital logic circuits are digital logic circuits based on single-electron Coulomb blockade devices [2]. The possibility to manipulate electrons one by one should reduce the power dissipation and enable higher integration densities. Up to this point two implementation abilities have been explored. Voltage-state logic as a direct transfer of CMOS topology to single-electron devices [3] and charge-state logic in the form of binary decision diagram – BDD [4] circuits and quantum cellular automaton – QCA [5][6] circuits.

In our contribution we explore the possibility of voltage state logic circuits design and analysis using the MOSES [2] Monte-Carlo simulator. Our focus will be mainly on

the implementation of logic functions with means of complementary single-electron logic circuits based on the Orthodox theory briefly described in Section 2.

2 Orthodox theory and monte-carlo simulation

In order for single-electron charging effects to become observable and for orthodox theory to apply two conditions should be met. Firstly charging energy should be much greater than thermal energy as depicted in equation (1).

$$E_C \gg E_T \tag{1}$$

This condition requires either feature sizes to be in the range of nanometres to minimise capacitances of the structure, or the operating temperature to be near the absolute zero. The second condition to be met is the condition of tunnel resistance R_t in equation (2).

$$R_t = \frac{\hbar}{q^2} \approx 4.2\,k\Omega \tag{2}$$

Satisfying these conditions, one can analyse single-electron circuits according to the orthodox theory. Applying the theory, the tunnel rate Γ through an individual junction can be expressed by means of equation (3).

$$\Gamma = \frac{\Delta E}{q^2 R_t \left(1 - \exp\left(-\frac{\Delta E}{k_B T}\right)\right)} \tag{3}$$

As the orthodox theory assumes independence between individual tunnelling events and only one tunnelling event possible at a certain time, it is possible to describe the macroscopic behaviour of such circuit through a stochastic series of such tunnelling events. The process takes into account probabilities that a tunnelling event will occur at a certain point in time and the probabilities are weighted by the tunnelling rate Γ. Such a process is suitable for implementation within the Monte-Carlo method and is implemented in the MOSES simulator.

3 Simulation of single-electron structures

Within our work we have analysed circuits of a single-electron box, single-electron transistor and a complementary single-electron inverter. Wherever possible we compared our results to measurements of a physical device with similar parameters taken at other institutions.

3.1 Single-electron box

A single-electron box is the simplest single-electron structure. It consists of a single tunnel junction, coupled through a capacitance to a voltage source. The circuit is shown in Fig. 1 and circuit parameters used for simulation are given in the Table 1 below.

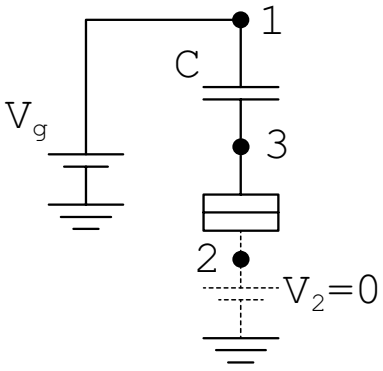

Figure 1: Circuit of a single-electron box used for simulation.

Table 1: Single-electron box circuit parameters used for simulation.

Element	Value
C	9 aF
C_{TJ}	1 aF
R_{TJ}	100 kΩ
V_g	0-50 mV

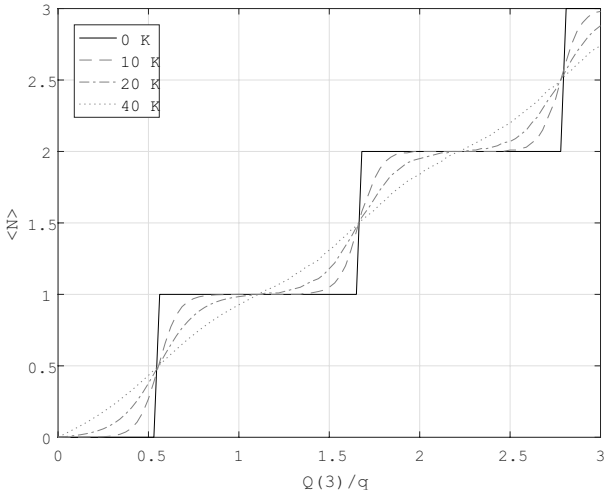

Figure 2: Simulation results of a single-electron box at 25 mK.

Varying the voltage V_g from 0 to 50 mV, we observed a characteristic response of the circuit – Coulomb staircase, predicted by the orthodox theory. Simulation results are shown in Fig. 2.

We could not find a real structure measurement to compare the results to, but we have found them comparable to an identical structure simulated by MUSES [7], which is another Monte-Carlo simulator.

The characteristic Coulomb staircase is temperature dependent, since the thermal energy should not exceed the charging energy. Simulation of the temperature dependence of a Coulomb staircase is depicted in Fig.3.

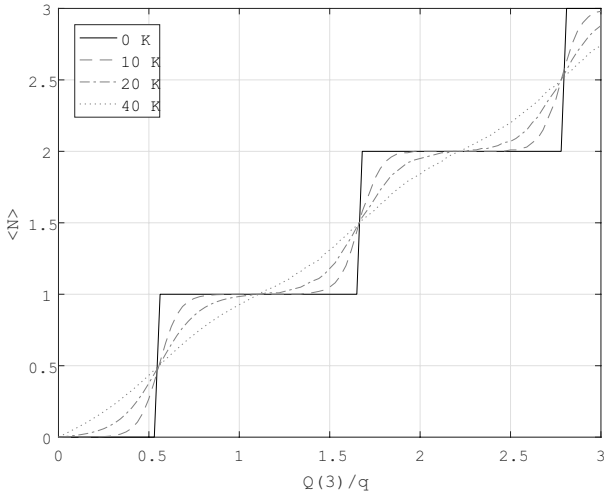

Figure 3: Temperature dependence of the Coulomb staircase.

3.2 Single-electron transistor

A single-electron transistor (SET) is a modification of a single-electron box. Adding another tunnel junction and a supply voltage source, we get the circuit presented in Fig. 4. In Table 2 element values used for simulation are presented.

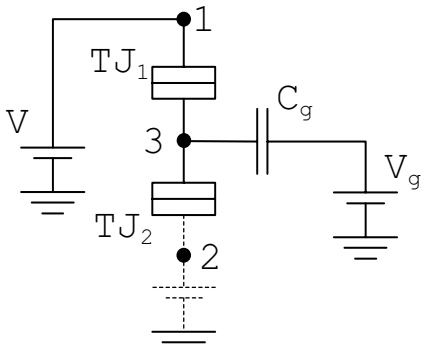

Figure 4: Circuit of a single-electron transistor used for simulation.

Values for the simulation were chosen according to the measurements in [8]. Varying the gate voltage V_g and supply voltage V as given in Table 2, we were able to obtain a stability diagram for the given transistor. The simulation was performed at 25 mK and a background charge at the central island of 0.3 electrons as observed in [8]. The addition of background charge was necessary to achieve agreement between simulations and measurements, since it shifts the stability diagram of a single-electron transistor. The obtained stability diagram is given in Fig. 5. Fig. 6 presents a measured stability diagram of a real single-electron transistor [8] with the same parameters.

Table 2: Single-electron transistor circuit parameters used for simulation.

Element	Value
C_{TJ1}	57.14 aF
C_{TJ2}	53.94 aF
Cg	3.2 aF
R_{TJ1}, R_{TJ2}	100 kΩ
V_g	0-80 mV
V	0-2 mV

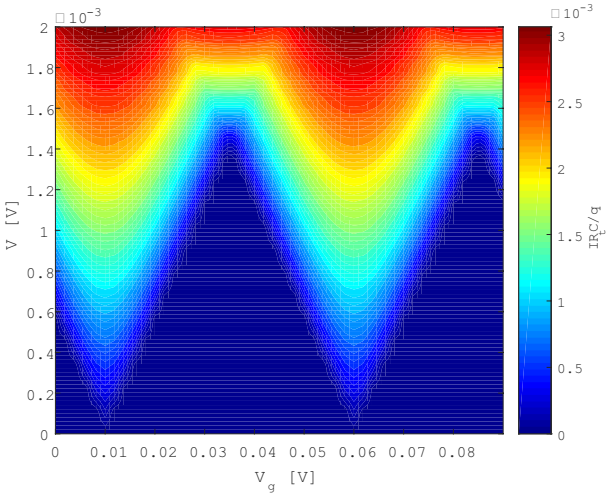

Figure 5: Simulation of a SET stability diagram at 25 mK.

3.2.1 Temperature dependence

As a single-electron transistor is just a variation of a single-electron box, its characteristics should also be temperature dependent. Taking 114.28 aF as a cumulative capacitance of the circuit in Fig. 4 towards the environment C_Σ, we were able to estimate the temperature, up to which Coulomb oscillations would be noticeable, according to equation (4).

$$T \ll \frac{q^2}{k_B C_\Sigma} \approx 16\,K \tag{4}$$

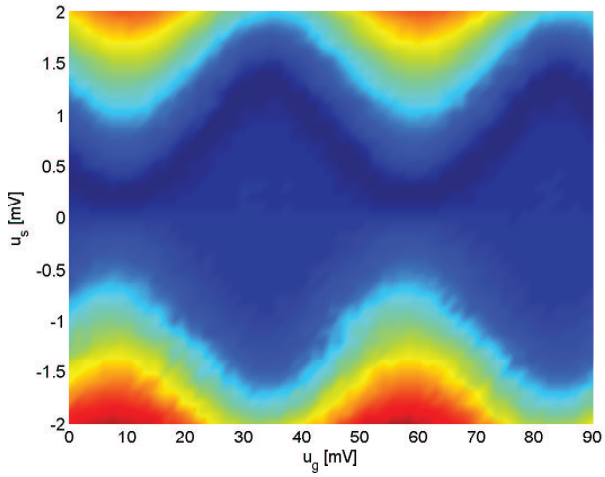

Figure 6: Mesurement of a SET stability diagram at 25 mK [8].

To get a sense of the relation 'far less' in equation (4), we made a simulation of Coulomb oscillations at different temperatures and a supply voltage *V* of 1 mV. It was observed, that Coulomb oscillations become negligible at temperatures 3 times smaller as calculated. The results of the simulations are given in Fig. 7.

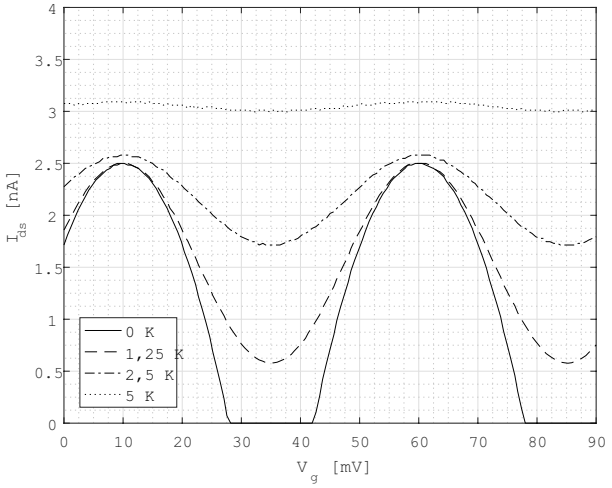

Figure 7: Simulation of Coulomb oscillations at different temperatures. *V* = 1 mV.

As the temperature dependence of the observed Coulomb oscillations may not pose a serious problem at this point, their impact of the characteristics of complementary single-electron logic circuits is quite significant.

3.3 Complementary single-electron inverter

A complementary single-electron inverter is comprised of two single-electron transistors much as a conventional CMOS inverter. The two identical SETs with an additional controlling capacitance at the gate, act as a p-MOS or n-MOS equivalent, depending on the operating point set by the controlling electrodes. The schematic of a single-electron inverter circuit is shown in Fig. 8. The elements' values were once again taken from a real implementation of the device from [8] for easier comparison of the results. The parameters are given in Table 3.

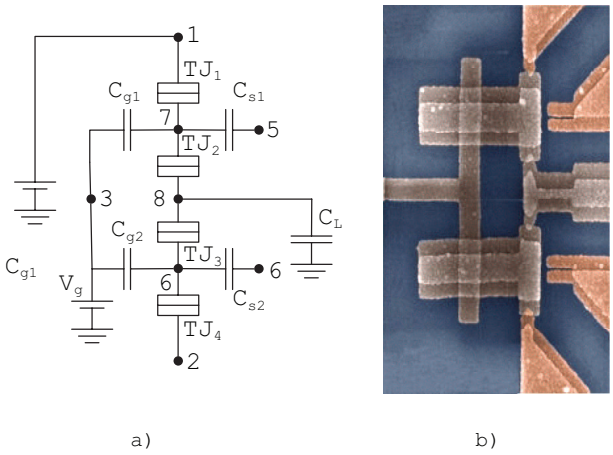

Figure 8: Complementary single-electron inverter a) and an electron microscope image of the realisation from [9] b).

Table 3: Single-electron inverter circuit parameters used for simulation.

Element	Value
C_{TJ1} - C_{TJ4}	100 aF
C_{g1}, C_{g2}	800 aF
C_{s1}, C_{s2}	686 aF
R_{TJ1} - R_{TJ4}	100 kΩ
V_g	0-80 μV
V_s	65 μV

The simulation was performed at 25 mK and with no background charge at any of the nodes, since none was reported originally. Fig. 9 shows simulation results of a DC transfer characteristics compared to the measurement and SPICE simulation results obtained in [8].

Our simulated characteristic shows some deviations from the measured one and more closely corresponds to the characteristics obtained by SPICE. The difference is thought to be due to second-order effects namely cotunneling, since it is not simulated by MOSES and could result in a steeper characteristic than in reality. Second-order effects are most prominent near or in the Coulomb blockade region [10], where standard tunneling is negligible. Additional electron transmission

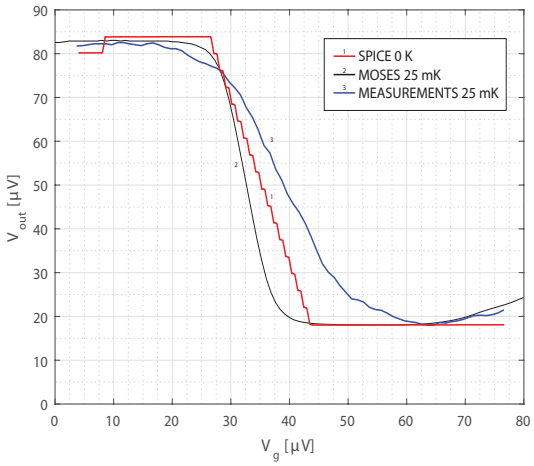

Figure 9: Simulated SET inverter characteristics at 25 mK from MOSES, SPICE [8] and the measurement of the device [8].

through the single-electron transistor induced by the cotunneling effect in the Coulomb blockade region could account for the gentler slope, since it inhibits charging and discharging of the load capacitor. Nearly perfect agreement between simulations and measurements outside of the transition region of the inverter, on the other hand, lets us believe that simulations at higher temperatures should show similar or even better agreement with real structures, due to the diminishing of the cotunneling effect with increasing temperature as observed in [11-12].

3.3.1 Temperature dependence of DC transfer characteristic

The temperature dependence of the inverter's transfer characteristic was evaluated using equation (4) where the cumulative capacitance towards its surroundings 1686 aF was taken as the value of C_{Σ}. Taking into account the factor 'far less' derived in the previous section, the maximum operating temperature was estimated to be around 360 mK. The simulation of the temperature dependence of the inverter's DC transfer characteristic is shown in Fig. 10.

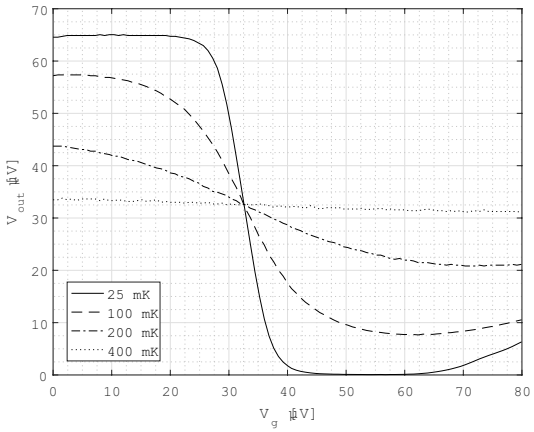

Figure 10: Temperature dependence of SET inverter characteristics.

From Fig. 10 one can clearly see a continuous degradation of logic levels with increasing temperature, as well as a decrease in the absolute differential gain at the switching point. An inverter with such characteristics is clearly an inappropriate building block for larger logic circuits even at temperatures close to absolute zero, let alone at room temperature.

3.3.2 Single-electron inverter at room temperature

The main goal in developing single-electron circuits is room temperature operation. According to the simulations from previous sections we have proposed a structure that when implemented, should exhibit single-electron effects even at room temperature. Using equation (4) and a factor 1/5 for the criterion 'far less' we have estimated the value of C_{Σ} to less than 1.2 aF.

To meet the criterion we have scaled the values in Table 3 2000 times. The element values of the scaled inverter are given in Table 4 and the simulation of the DC transfer characteristics at different temperatures is given in Fig. 11.

Table 4: Single-electron inverter circuit parameters used for simulation.

Element	Value
C_{TJ1} - C_{TJ4}	0.05 aF
C_{g1}, C_{g2}	0.4 aF
C_{s1}, C_{s2}	0.343 aF

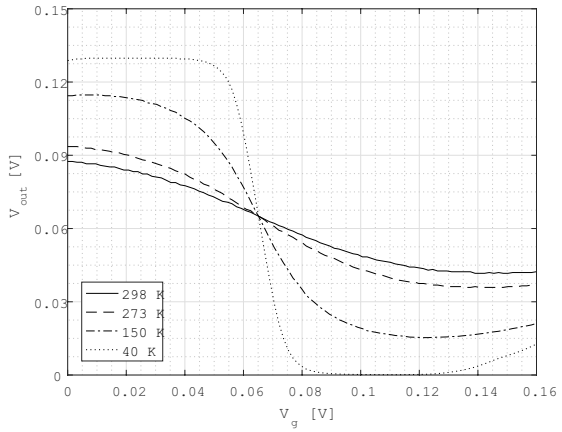

Figure 11: Temperature dependence of SET inverter characteristics.

From Fig. 11 it is clearly visible, that the inverter characteristic is still observable at room temperature, even

though the differential gain at the switching point is already below 1. A strong degradation of logic levels is also visible. Despite the observable inverter characteristics at room temperature, the inverter would still not be capable to drive further logic stages. For that to become possible, the dimensions of the features composing the inverter would need to drop into the sub-nanometre region as predicted in [13].

The dimensions of a fabricated device with parameters from Table 4, where each island is shaped as a cube for simplicity, are given in Table 5. Fig. 12 presents a simplified layout of the device.

Table 5: Dimensions of the single-electron inverter structure for parameters in Table 4 and Table 3.

Dimension	Length Table 4	Length Table 3
a	1 nm	1 nm
b	2.38 nm	106 nm
c	0.12 nm	0.12 nm
d	0.15 nm	0.15 nm

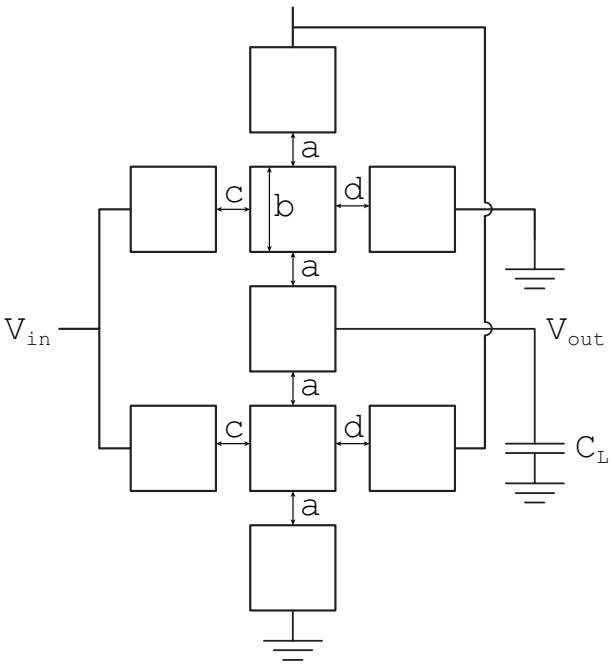

Figure 12: Proposed simple layout of a room temperature operable single-electron inverter.

4 Conclusions

From the performed simulations it is clear, that single-electron circuits could be the next step in the integration and miniaturisation of logic circuits. One of the setbacks of complementary single-electron logic is the small dimension of the features comprising the single-electron circuits to achieve room temperature operation. Another possible setback is the degradation of the logic levels and thus the inability to drive further stages. The solution of the problem could be found in single-electron charge state logic, which defines logic levels with the presence of an electron and not with the voltage level as do complementary single-electron circuits. Two of the possible approaches already in development are the use of QCA (Quantum Cellular Automaton [5][6] and the BDD (Binary Decision Diagram) [4].

5 References

1. V. K. Khanna, "Single Electronics," in *Integrated Nanoelectronics*, Pilani, India, Springer, 2016, pp. 247-269. https://www.doi.org/10.1007/978-81-322-3625-2
2. A. N. Korotkov, "Single-electron logic and memory devices," *International Journal of Electronics,* vol. 86, no. 5, pp. 511-547, 1999. https://www.doi.org/10.1080/002072199133256
3. K. Uchida, J. Koga, R. Ohba, et al., Programmable Single-Electron Transistor Logic for Future Low-Power Inteligent LSI: Proposal and Room-Temperature Operation," *IEEE T. Electron Dev.*, vol. 50, no. 70, pp. 1623-30, July 2003. https://www.doi.org/10.1109/ted.2003.813909
4. S. Kasai in H. Hasegawa, "A single electron binary-decision-diagram quantum logic circuit based on schottky wrap gate control of a GaAs nanowire hexagon," *IEEE Electron Device Letters*, vol. 23, no. 8, pp. 446–448, 2002. https://www.doi.org/10.1109/led.2002.801291
5. A. N. Bahar, S. Waheed, N. Hossain in M. Asaduzzaman, "A novel 3-input xor function implementation in quantum dot-cellular automata with energy dissipation analysis," *Alexandria Engineering Journal*, 2017. https://www.doi.org/10.1016/j.aej.2017.01.022
6. S. Banerjee, J. Bhattacharya, R. Chatterjee, P. Bagchi, S. Mondal, R. Bandyopadhyay, R. Dutta in P. Das, "A novel design of 3 input 8 output decoder using quantum dot cellular automata," in *Information Technology, Electronics and Mobile Communication conference (IEMCON), 2016 IEEE 7th Annual*, pp. 1- 6, IEEE, 2016. https://www.doi.org/10.1109/iemcon.2016.7746340
7. A. A. Elabd, A.-A. T. Shalaby in E.-S. M. El-Rabaie, "Monte carlo simulation of single electronics based on orthodox theory," in *Radio Science conference (NRSC), 2012 29th National*, pp. 581–591, IEEE, 2012. https://www.doi.org/10.1109/nrsc.2012.6208569

8. R. van de Haar in J. Hoekstra, "Spice simulation of single-electron electronics compared to measurement results," in *STW-ProRISC-IEEE Workshop*, pp. 190–194, 2003.
9. C. P. Heij, P. Hadley, and J. E. Mooji., "Single-electron inverter," *Applied Physics Letters,* vol. 78, no. 8, pp. 1140-1142, 2001. https://www.doi.org/10.1063/1.1345822
10. C. Wasshuber, *Computational Single-Electronics*. Springer-Verlag Wien, 2001. https://www.doi.org/10.1007/978-3-7091-6257-6
11. S. De Franceschi, S. Sasaki, J. M. Elzerman, et al., "Electron cotunneling in a semiconductor quantum dot," *Physical review letters,* vol. 86, no. 5, pp. 878-881, 2001. https://www.doi.org/10.1103/PhysRevLett.86.878
12. R. Scheibner, E. G. Novik, T. Borzenko, et al., "Sequential and cotunneling behavior in the temperature-dependent thermopower of few-electron quantum dots," *Phiysical Review B,* vol. 75, no. 4, pp. 041301, 2007. https://www.doi.org/10.1103/PhysRevB.75.041301
13. K. K. Likharev, "Single-electron devices and their applications," *Proceedings of the IEEE*, vol. 87, no. 4, pp. 606–632, 1999. https://www.doi.org/10.1109/5.752518
14. R. H. Chen, D. M. R. Kaplan in O. Turel, *Monte-Carlo Single-Electronics Simulator 1.2 USERS'S GUIDE*, 2001.
15. MOSES. Monte-Carlo Single-Electronics Simulator, available from R. H. Chen (rchen@felix.physics.sunysb.edu)

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Digitally Adjustable Differential Gain Stage

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Abstract: Most ASIC's demand signal conditioning sub-circuits to modify various signal parameters; one of the important parameter is the gain. The presented configuration is based on the conventional R-2R structure which mainly suffers from the mismatch imperfections. The study shows possible approach to improve mismatch characteristic or enables us to take the advantage to increase bit resolution without mismatch deteriorations. The approach could be used to even further improve accuracy of the numerous previously described approaches [1], [2] which already eliminate high resolution mismatch imperfections. Paper presents the implementation of the gain stage with digital gain adjustment, in the range from 0.9 to 1.1 in 128 equidistant monotonous steps, nevertheless the approach could be implemented even for higher resolution stages. For robust design in terms of the fabrication process and harsh environment operation, a fully differential amplifier was designed in standard 0.18µm CMOS technology. Designed amplifier in combination with resistive network is presented together with simulation results including the parasitic capacitances.

Keywords: digitally adjustable gain; resolution improvement; R-2R stage; deferentially balanced structure

Digitalno nastavljiva diferencialna ojačevalna stopnja

Izvleček: Večina namenskih integriranih vezij potrebuje podsklope vezij, ki skrbijo za obdelavo signalov in njihovih parametrov; pomemben parameter je ojačenje. Predstavljena konfiguracija bazira na konvencionalni R-2R strukturi, ki je znana po nezanemarljivem vplivu neidealnosti ujemanja elementov vezja. Študija predstavlja možen pristop za izboljšavo teh karakteristik oziroma nam omogoča povečanje ločljivosti ne da bi se pri tem poslabšale karakteristike ujemanja. Pristop se lahko uporabi na že znanih rešitvah za odpravo neidealnosti [1], [2] in tako še dodatno izboljša ločljivost. Delo predstavlja implementacijo ojačevalne stopnje z digitalno nastavljivim ojačenjem od 0.9 do 1.1 v 128 ekvidistančnih monotonih korakih, vendar bi se lahko podoben pristop uporabil tudi za stopnje z večjo ločljivostjo. Robustno delovanje glede na proces izdelave in obratovale pogoje je dosežen z diferencialnim ojačevalnikom dizajniranim v standardni 0.18µm CMOS tehnologiji. V članku je predstavljen načrtan ojačevalnik v kombinaciji z uporovnim vezjem skupaj s simulacijskimi rezultati vključujoč parazitne kapacitivnosti.

Ključne besede: digitalno nastavljivo ojačenje; izboljšanje ločljivosti; R-2R stopnja; diferencialno uravnotežena struktura

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1 Introduction

Common part of numerous analog ASIC's (Application Specific Integrated Circuits) incorporate circuits for signal conditioning. Modification of signal amplitude through gain adjustment presents one of the most frequently used approach. Several implementations are possible. In analog implementations the gain is changed using some nonlinear element in the feedforward or feedback path; the problem of such implementations is large distortions of the signal. In narrow band systems, this is acceptable, however, in our case, the system is wide band and thus analog nonlinear gain adjustment is not acceptable because we would like to achieve the distortions in the range of 0.01%. Thus, the only possibility is digital gain adjustment [3]. Each approach has associated advantages and disadvantages shortly described above. The important characteristics of the digital gain adjustment stage are: the resolution of gain steps, the responsivity, the distortions, the bandwidth, the area, and the final product cost.

The paper investigates a possible approach for digital gain adjustment using the similar circuit as known from the R-2R DA converters. The implementation is based on the conventional R-2R ladder structure to adjust the gain through the binary weighted currents. Com-

pared to other structures it has some advantages (for example small area and fast switching) and some disadvantages (for example non-monotonicity) [4], where non-monotonicity is more evident at higher number of bits. The monotonicity performance of a higher resolution stages could be improved by a numerous approaches as a resistor laser trimming procedure, binary LSB and unary MSB algorithmic segmentation [2], ordered element matching [1] and others. Some of them contributes to more complex digital logic with interconnection considerations taking into account wiring placement as a result of on-chip gradients, while some others enlarge inevitable die area as a result of inability of analog component accuracy at shrunk dimensions [2]. Mismatch suppression could be achieved with increased dimensions of the unit resistors as described with the Pelgrom's Law [5]. Nevertheless monotonicity could be improved even without increment of the resistor dimensions at the expense of additional R-2R structure presented in this work. Approach take the advantage of the fully-differential interconnection of both structures which yields higher robustness [6]. A method which maintains monotonicity of the gain stage with higher number of bits in the ASICs with two anti-phase shifted input signals is proposed.

The paper is organized as follows. Section 1 introduces the problem and explains why the R-2R structure is preferable. Section 2 describes the principle of operation, while Section 3 presents simulation results. Section 4 presents the layout and Section 5 concludes the article.

2 Circuit description

2.1 Principle of operation

The principle schematics of a fully differential, digitally adjustable gain stage is shown in the Fig. 1. It consists of a resistive network composed of two R-2R ladder structures and feedback resistors. The adjustable gain stage provides the gain in the range from 0.9 to 1.1. R-2R determined adjustable gain (Gain=±0.1) is superpositioned to the constant one (Gain=1) determined by feedback resistors R_{FB1} and R_{FB2}. To take the advantage of the proposed approach of doubling gain range, input signals ***inp*** and ***inn*** should be anti-phase shifted as differential structure suppresses in-phase signals. In the case when multiplexer directly translates the portion, determined by the bits, of the signal ***inp*** to the upper amplifier feedback resistor $\boldsymbol{R_{FB2}}$, the absolute amplitude of the output signal ***outn*** is increased and in contrary decreased in a case when the portion of the ***inn*** is crossed through a multiplexer and tied to the upper resistor $\boldsymbol{R_{FB2}}$. In this manner multiplexer with its switches permutates in-between two R-2R ladder structures and thus control whether the gain is increased or decreased. The proposed approach with differentially connected R-2R structures yields higher resolution compared to single-ended structure at the expense of increased die area. The stage has gain resolution equivalent to 7 bits. According to the desired gain, determined by the six bits $\boldsymbol{b_i}$ (i=0,1,…5) plus additional one $\boldsymbol{b_6}$ for multiplexer (sign bit), the portion of the current from the R-2R structure is connected either to the signal ground or to the summing point at the input node of a differential amplifier. Resistor $\boldsymbol{R_{FB2}}$ in combination with differential TIA (trans-impedance amplifier) serves as a current to voltage converter. Two differential output signals are kept around the signal ground with a help of common mode feedback circuit (***CM*** block in the Fig. 1). Output common signals are assured by a help of additional amplifier which compares the voltage $\boldsymbol{V_{CM}}$ to the reference voltage (i.e. signal ground) and provides error correction through the feedback biasing signal $\boldsymbol{V_{CMB}}$ (Fig. 2).

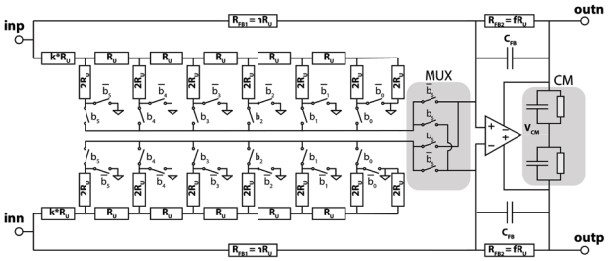

Figure 1: Simplified schematic of a fully differential, balanced, R-2R adjustable gain stage.

2.2 Resistive network

The gain of the stage is composed of two super-positioned contributions. The constant one is determined by the ratio ***f/n*** of resistors $\boldsymbol{R_{FB1}}$ and $\boldsymbol{R_{FB2}}$ while the variable one is based on the adjustable R-2R stage determined by binary weighted currents delivered to the virtual ground of the TIA from the R-2R stage. Values of resistors are determined in a way to achieve a desired gain range from 0.9 to 1.1 in 128 equidistant monotonous steps. Desired gain steps can be realized according to (1) by setting unit resistors multiplication factors to ***k***=153, ***n***=16 and ***f***=16 (see (1)).

$$Gain = -\left(\sum_{i=0}^{5} \frac{R_U}{(k+1)R_U 2^{5-b_i}} \frac{b_i}{2R_U} (-1)^{b_6} + \frac{1}{nR_U} \right) fR_U \qquad (1)$$

Unit resistance is selected appropriately to provide on one side sufficient accuracy and bandwidth, and on the other side to maintain low noise and low current con-

sumption. The resistors should exhibit high linearity (low voltage coefficient), small temperature coefficient, acceptable noise, small parasitic capacitance and good matching properties. This is accomplished by appropriate size of the unit resistor and appropriate layout. Considering mentioned parameters, high resistive poly resistor is used [4]. Unit resistance $\boldsymbol{R_U}$ is composed of foundry minimal recommendation of five squares. Used high resistive poly resistor with sheet resistance of approximately 350 Ω/W yields $\boldsymbol{R_U} \cong 1.836$ kΩ.

2.3 Switches

In order to realize high accuracy of gain adjustment, it is essential to properly construct the switches as well. Weighted currents in the R-2R branches call for scaled switches from the one with a minimum conduction resistance for b_5 to the switch with maximum resistance for b_0, which has 32 times larger resistance compared to the switch b_5. Nevertheless, maximum resistance of each switch should be much smaller than the unit resistance $\boldsymbol{R_U}$. To meet the switch conduction requirements, they should be adequately dimensioned. For the same reason, multiplexer switches should be properly designed as well. In general, large switches have relative large parasitic capacitance that affects the speed and stability. However, R-2R switches in the proposed approach do not experience any voltage change as they are tied to the signal ground node. This is convenient in terms of the system bandwidth. R-2R and multiplexer switches are constructed as transmission gates with complementary MOSFETs with different dimensions to maintain approx. linear resistance over different voltages. In addition, dummy MOSFETs are added to the nodes, to reduce the clock feedthrough effect and off channel charge injection during switching and to ensure the same loading of all driving lines, thus to mitigate the gain transition glitches. Remaining imperfections during gain adjustment are empirically determined by simulations and solved with time delayed control lines through buffered inverters.

2.4 Differential trans-impedance amplifier

Fully differential TIA with feedback resistances $\mathbf{R_{FB2}}$ converts currents out of the resistive R-2R network and $\mathbf{R_{FB1}}$ to two differential output signals. Since closed loop configuration impact overall system bandwidth and stability, the TIA is based on the folded cascode architecture (Fig. 2). Sufficient unity-gain bandwidth is needed to overcome the gain variations at the frequency of the signal. Poorly designed TIA, in terms of bandwidth, can at high frequencies cause large gain variations. TIA is composed of a PMOS differential pair (M3, M4) with tail current of 200μA, which is distributed between two NMOS transistors (M5, M6). Each of them drains additional current of 40 μA from PMOS load (M7, M8). To clearly present configuration, additional cascode transistors for performance improvement are missing in the simplified schematic. Output stage is based on the common source configuration with Miller compensation.

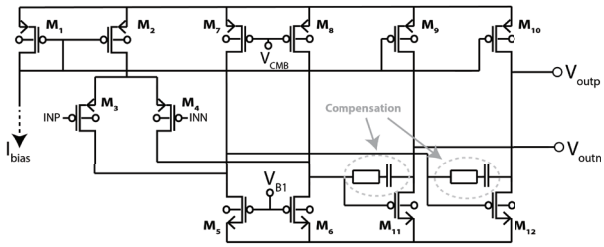

Figure 2: Transimpedance amplifier based on the folded cascade architecture.

TIA must be stable under all conditions, therefore a differential and common mode stability is assured using appropriate frequency compensation circuitry. It should be properly designed using appropriate feedback capacitor C_{FB} (Fig. 1), which implements low pass filtering characteristics. This capacitance compensates influence of the parasitic capacitance of the switches in the R-2R ladder structure.

3 Simulation results

The circuitry is designed in TSMC 180nm CMOS technology and characterized using Cadence Virtuoso environment. Process verification includes all process corners: typical, low-slow, slow-fast, fast-slow, fast-fast and/or statistical variations: MC, MM; complete temperature range from -40°C to 150°C and supply voltage range from 3V-5V.

Principle of operation of gain adjustment is presented in the Fig. 3. The gain is equal to 1 when the bits b_5-b_0

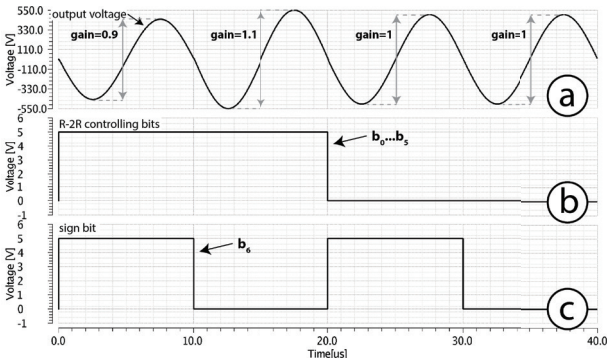

Figure 3: Gain adjustment: (a) signal at the output of the amplifier, (b) status of controlling bits b_0 to b_5, (c) status of multiplexer bit b_6.

are set to low independently of the multiplexer bit b_6. When b_6 is low, enabled b_0-b_5 bits increase the gain up to 1.1 and when b_6 is high the gain is decreased from 1 down to 0.9 in 127 equidistant steps.

Figure 4 shows transient response to 500 kHz input square signal. The system settles 2µs after power-on.

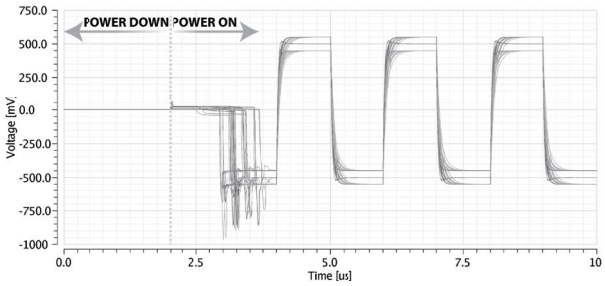

Figure 4: Transient response at gain: 0.9, 1 and 1.1 for 500 kHz square-wave input signal.

Implementation with two 6-bit R-2R ladder structures yields better accuracy as one with single 7-bit R-2R structure. In the Fig. 5, the matching accuracy of two 7-bits R-2R ladder based structures are presented. Fig. 5(b) shows LSB gain variations for proposed approach with two 6-bit R-2R structures and multiplexer which implements the b_6 compared to the previous design [4] with one 7-bit R-2R structure presented in Fig. 5(a). One 6-bit R-2R structure provides adjustable gain range of 0.1 which is doubled over constant gain of 1 with a help of an additional 6-bit R-2R and multiplexer, while 7-bit R-2R have to provide an adjustable gain range of 0.2 above the constant gain of 0.9. Distribution of the LSB gain shows improvement of the standard deviation of the proposed approach compared to the previous one for approximately 40%.

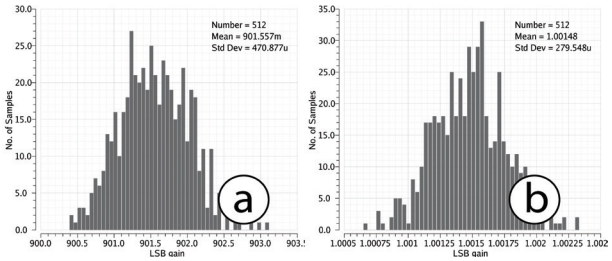

Figure 5: LSB gain variation: (a) mismatch of the previous design and (b) mismatch for proposed approach.

Closed loop AC characteristics of the amplifier with digital gain adjustments are presented in the Fig. 6, for gains set to 0.9, 1 and 1.1. At higher frequencies, the gain characteristics starts to distort as a result of process influence to the gain bandwidth of the TIA. Nevertheless, closed-loop gain characteristics at low frequencies are mainly affected by the mismatch contribution of the R-2R structure [7]. It is evident in the case when an ideal amplifier is used and R-2R mismatch is the main contributor to the overall gain variations, which are listed in the Table 1.

Table 1: Influence of process and mismatch variations on the LSB gain using real and ideal TIA.

	Real amplifier		Ideal amplifier	
	Std. dev. @ 100kHz	Std. dev. @ 500kHz	Std. dev. @ 100kHz	Std. dev. @ 500kHz
Process	8.20E-05	1.83E-03	1.42E-07	3.46E-06
Mismatch	2.90E-04	4.58E-04	2.82E-04	2.82E-04

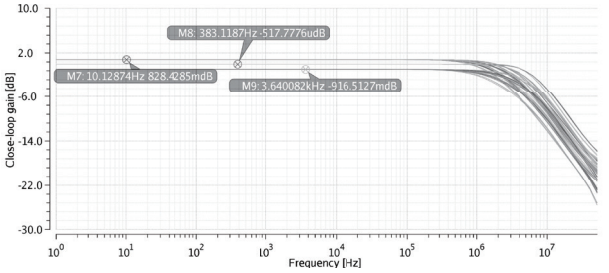

Figure 6: Closed-loop characteristic for the gain stage with gain variations 0.9, 1 and 1.1.

Figure 7 shows open loop differential AC characteristics. Most critical phase margin of 53° is met at 12.7MHz for 3V power supply, fast-fast corner and at temperature of 150°C. Fig. 8 shows AC characteristics for common mode feedback signal ($\boldsymbol{V_{CM}}$). It shows stable behavior and provides the appropriate output common signal.

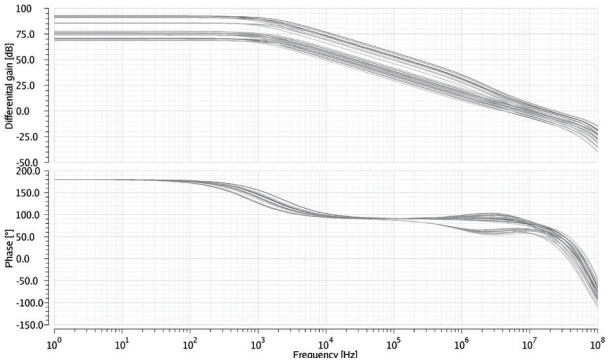

Figure 7: Differential open-loop gain and phase characteristics.

The offset of the complete gain stage is generated inside the TIA, as a result of the mismatch of the MOSFETs in the input differential stage. Offset distribution based on Monte-Carlo simulation is shown in the Fig. 9. The maximum input offset is 3mV and is included in the evaluation of the system performance.

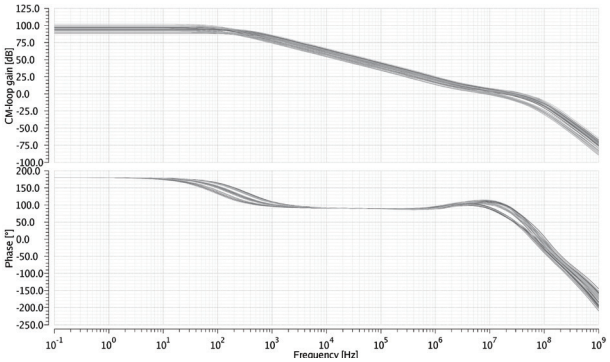

Figure 8: Open-loop gain and phase characteristics of the common mode feedback signal V_{CM}.

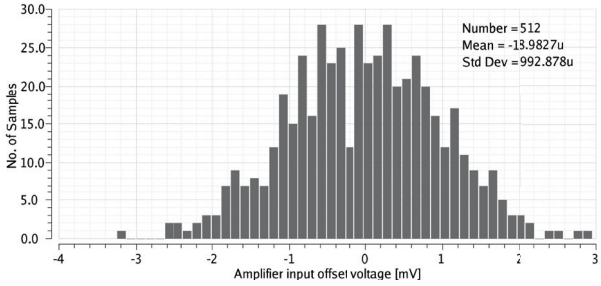

Figure 9: TIA input offset for mismatch variations.

The CMRR behavior of the gain stage with added input offset voltage of 3mV is shown in the Fig. 10. The presented characteristics show that the amplifier input offset deteriorate CMRR performance as it is proportional to the invert value of the offset [8].

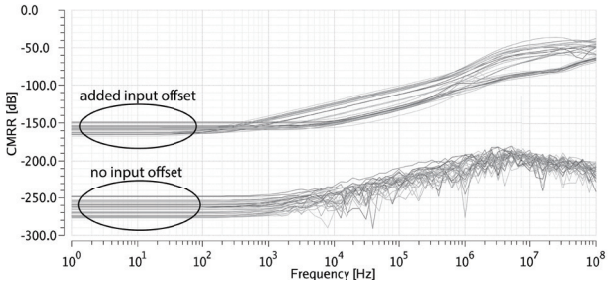

Figure 10: CMRR with and without added offset.

The important parameter is also a phase shift at the highest frequency of 500 kHz. The worst phase shift of 14° happens as expected at the largest gain, for supply voltage of 5.5V, at 150°C and max process variation of the R-2R structure. This deviation could be trimmed in the separate process of the phase shifting. Typical power consumption is 660 µA at 3.3V supply voltage, typical process parameters and 25°C. It is increased to 860 µA at 5.5V supply voltage, fast-fast process parameters corner and at 150°C.

4 Layout

The layout of the stage is presented in the Fig. 11. It is symmetrical. As already mentioned, the R-2R implementations are prone to glitches during gain switching. Appropriate control logic is realized in a way to equalize digital control signals delay. The resistors mismatch is improved by using the optimum width of the resistors (R_U dimensions 4µmx20µm). In addition, the surrounding of all resistors must be the same, which is achieved using appropriate dummy resistors that reduce the edge effects. Analog inputs are shielded from the digital signals. For higher accuracy, sensitive current mirrors and differential stage of the TIA are protected with additional dummy devices. Signal ground tracks are wide enough to minimize voltage drops across the gain stage. Overall silicon area occupies approximately 0.2 mm^2.

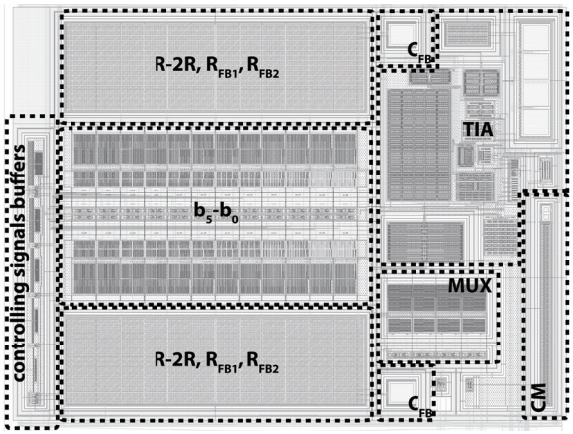

Figure 11: Layout of adjustable gain ratio cell.

5 Conclusions

This paper presents design, optimization and implementation of a digitally adjustable gain stage, based on R-2R structure. Proposed approach yields performance improvements in terms of the accuracy compared to the previous realizations. Designed TIA is implemented in a way to provide sufficient bandwidth of the system together with the parasitic contributions of the resistive network and switches. The characteristics of the amplifier are verified in terms of process and mismatch variations as well as supply voltage and temperature.

6 References

1. You Li, Tao Zeng, and Degang Chen, 'A high resolution and high accuracy R-2R DAC based on ordered element matching', in *2013 IEEE*

International Symposium on Circuits and Systems (ISCAS2013), Beijing, 2013, pp. 1974–1977. https://doi.org/10.1109/ISCAS.2013.6572256
2. G. Radulov, P. Quinn, H. Hegt, and A. H. M. van Roermund, *Smart and Flexible Digital-to-Analog Converters*. Dordrecht: Springer Netherlands, 2011. https://doi.org/10.1007/978-94-007-0347-6
3. W. Xu, R. Zhang, and C. Shi, 'Research of segmented 8bit voltage-mode R-2R ladder DAC', 2015, pp. 1–4. https://doi.org/10.1109/ASICON.2015.7517105
4. Miha Gradišek, Janez Trontelj, and Drago Strle, 'High precision adjustable gain stage', *Conference proceedings 2017*, pp. 102–107, 2017.
5. M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, 'Matching properties of MOS transistors', *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct. 1989. https://doi.org/10.1109/JSSC.1989.572629
6. A. Abba, A. Manenti, F. Caponio, and A. Geraci, 'High Performance Analog Front-End for Digital Spectroscopy', *IEEE Transactions on Nuclear Science*, vol. 57, no. 4, pp. 2173–2177, Aug. 2010. https://doi.org/10.1109/TNS.2010.2049658
7. M. P. Kennedy, 'On the robustness of R-2R ladder DACs', *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 47, no. 2, pp. 109–116, Feb. 2000. https://doi.org/10.1109/81.828565
8. Jian Zhou and Jin Liu, 'On the measurement of common-mode rejection ratio', *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 1, pp. 49–53, Jan. 2005. https://doi.org/10.1109/TCSII.2004.838332

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Multiparameter miniature fiber-optic sensor: design and signal interrogation

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Abstract: Miniature, all-silica, fiber-optic sensors capable of independent measurement of at least two different parameters are presented. Sensors were produced by a micromachining process based on the selective etching of specially designed phosphorous-doped optical fibers and an assembly-procedure that included fiber cleaving, fiber splicing and etching of fiber-micro-assemblies. Furthermore, an efficient method for independent readout of parameters in sensors that are composed of multiple resonators was also developed. The method utilizes a discrete Furrier transform of sensor's optical spectrum and allows for simultaneous, crosstalk-free and highly sensitive readout of individual resonators' path length changes.

Keywords: Optical sensors; micromachinin; microstructures; discrete Fourier transform.

Večparametrični miniaturni optični vlakenski senzorji: načrtovanje in signalno razločevanje

Izvleček: V članku so predstavljeni miniaturni, optični, vlakenski senzorji, ki lahko neodvisno zaznavajo najmanj dva različna parametra. Senzorji so izdelani s postopkom mikroobdelave na osnovi selektivnega jedkanja posebnih z fosforjem dopiranih optičnih vlaken. Ti postopki so združeni s standardnimi postopki rezanja, varjenja in jedkanja. Poleg tega je predstavljena učinkovita metoda za neodvisno branje parametrov senzorja, ki združuje več zaporedno nanizanih resonatorjev. Metoda vključuje diskretno Fourierjevo transformacijo optičnega spektra, ki omogoča simultano in zelo občutljivo razločevanje sprememb posameznih optičnih dolžin resonatorjev.

Ključne besede: Optični senzorji; mikroobdelava; mikrostrukture; diskretna Fourierjeva transformacija.

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1 Introduction

Optical fiber-based sensors have received a great deal of attention over the past several decades for increased sensitivity over existing techniques, geometric versatility, immunity to harsh environments, and inherent compatibility with optical fiber communication systems. The rising complexity of sensor systems, methods often require sensing of more than one physical or chemical parameter. In particular, multi-parameter fiber-optic sensors that monitor physical, chemical, and biological parameters are of great importance in numerous areas including structural health monitoring, environmental pollution control, biochemical and biomedical applications [1-4]. Miniaturization brings additional challenges in cases of small sensing devices designs, as those devices are more sensitive to oxidation and other degradation processes. A variety of multi-parameter sensors have been proposed recently including Fiber Bragg grating [5], Fabry-Perot interferometer (*FPI*) [6], higher-order-mode fiber based modal interferometer sensors [7], evanescent field sensors [8], surface plasmon resonance sensors [9] and combination between them [10]. Beside them, there are also some other techniques involving multicore fibers, that have high potential for multiparameter sensing [11].

In this paper we present all-silica multiparameter miniature fiber-optic Fabry-Perot (*FP*) sensors for measuring at least two parameters simultaneously. Sensor design, signal interrogation and achieved performance is presented and discussed for following multiparameter sensors:

- sensor for pressure and temperature [12]
- sensor for pressure and refractive index [13]

- sensor for refractive index and temperature [14]
- sensor for relative humidity and temperature [15]
- sensor for pressure, temperature, thermal conductivity and refractive index [16]

All sensors demonstrated high measurement resolution with negligible cross-talk among measured parameters. We successfully demonstrated simultaneous measurement up to four very different physical parameters. In addition, efficient method for independent readout of different parameters of multiple resonators was also presented. The method base on discrete Furrier transform of sensor's back reflected optical spectrum that allows simultaneous, crostallk-free and highly sensitive measurements of resonators' path length change.

2 Mathematical model and signal processing of fabry-perot multiparameter sensor

The model of the multiparameter sensor, which was used in simulations to illustrate the cross-talk between different frequency components and effect of applied Gaussian window, will be presented below.

Sensor is composed from three semi reflective surfaces, which forms three *FP* resonators. The first two are shown in the Fig.1 as L_1 and L_2, while the third resonator L_3 represents their sum. The basic principle of the operation of an individual *FP* resonator or interferometer can be explained by the light wave that enters the resonator, where it is reflected or interfered between the two surfaces. The magnitude of the light current or the shape of the spectral characteristic is effected by: the distance *L* between mirrors, the wavelength of light *λ* and the refractive index *n* of the transmission medium. Because in our case we have several *FP* resonators in the series, we can use one-dimensional space, where the superposition of the optical wave can be presented with a trigonometric approach.

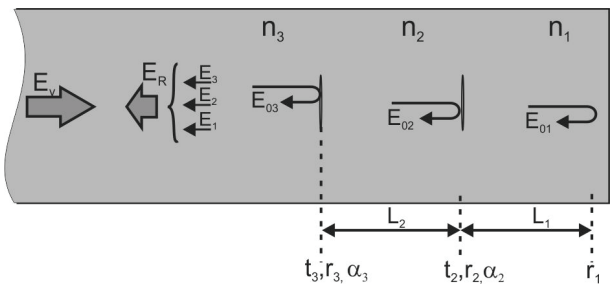

Figure 1: Model of FPI.

In general, the optical wavelength in some point can be described as a function of time:

$$E = E_0 \sin(\omega t \pm \varphi) \tag{1}$$

This can be written in the complex space as:

$$E = E_0 e^{j(\omega t \pm \varphi)} \tag{2}$$

First, three waves overlapping in space of the same frequency and speed must be add together.

The following waves are summed up after the reflection from the mirrors in the lead-in fiber:

$$\begin{aligned} E_{03} &= E_V r_3 \cdot e^{j\omega t} \\ E_{02} &= E_V t_3 r_2 \sqrt{1-\alpha_3} \cdot e^{j(\omega t+\varphi_1)} \\ E_{01} &= E_V t_3 t_2 r_1 \sqrt{1-\alpha_3}\sqrt{1-\alpha_2} \cdot e^{j(\omega t+\varphi_2)} \end{aligned} \tag{3}$$

Where E_{03}, E_{02}, and E_{01} are individual components of the electrical field strength, that are reflected from individual semi-reflective surfaces, *Ev* is the input amplitude of the electric field strength, r is coefficient of reflectivity and *t* is transmission coefficient, and the coefficient *α* is reserved for describing the optical losses on the splice.

The phase changes corresponded to the interferometer's optical path length variations: φ=kn=2πLn/λ, in our case, we have already defined it as a phase change due to a reflection from a distant mirror, which doubling the optical path, and thus the phase of the wave.

$$\begin{aligned} \varphi_1 &= \frac{4\pi n_2 L_2}{\lambda} \\ \varphi_2 &= \frac{4\pi\left(n_2 L_2 + n_1 L_1\right)}{\lambda} + \pi \end{aligned} \tag{4}$$

When optical waves travels cross the glass / air boundary, or vice versa, an additional phase shift occurs for *π* / 2, so in our example, when we observe the reflected wave, this is taken into account with the phase delay *π* (equation 4).

The current description covers only electric field strengths that do not include transmission coefficients t of individual mirrors on the way back. This is supplemented by the following terms:

$$\begin{aligned} E_3 &= E_{03} = E_v r_3 \cdot e^{j\omega t} \\ E_2 &= E_{02} t_3 \sqrt{1-\alpha_3} = E_v t_3^2 r_2 (1-\alpha_3) \cdot e^{j(\omega t+\varphi_1)} \\ E_1 &= E_{01} t_3 t_2 \sqrt{1-\alpha_3}\sqrt{1-\alpha_2} = \\ &= E_v t_3^2 t_2^2 r_1 (1-\alpha_3)(1-\alpha_2) \cdot e^{j(\omega t+\varphi_2)} \end{aligned} \tag{5}$$

Where E_3, E_2 and E_1 represent the total electrical field strength, which is reflected from the individual semi-reflective mirror, as shown in Fig. 1. Furthermore, the total electrical field strength can be written as the sum of all three components:

$$\begin{aligned} E_R &= E_3 + E_2 + E_1 \\ E_R &= E_v r_3 \cdot e^{j\omega t} + E_v t_3^2 r_2 (1-\alpha_3) \cdot e^{j(\omega t+\varphi_1)} + \\ &\quad + E_v t_3^2 t_2^2 r_1 (1-\alpha_3)(1-\alpha_2) \cdot e^{j(\omega t+\varphi_2)} \end{aligned} \tag{6}$$

Since the reflected-light intensity I_R is proportional to the square of the electric field strength, the following can be written as:

$$I_R \propto {E_R}^2 \tag{7}$$

When squaring, the conjugated complex value of the electric field strength must be taken into account:

$$\begin{aligned} I_R &\propto E_R E_R^* \\ I_R &\propto \left[\begin{array}{l} E_v r_3 \cdot e^{j\omega t} + E_v t_3^2 r_2 (1-\alpha_3) \cdot e^{j(\omega t+\varphi_1)} + \\ \quad + E_v t_3^2 t_2^2 r_1 (1-\alpha_3)(1-\alpha_2) \cdot e^{j(\omega t+\varphi_2)} \end{array} \right] \\ &\quad \cdot \left[\begin{array}{l} E_v r_3 \cdot e^{-j\omega t} + E_v t_3^2 r_2 (1-\alpha_3) \cdot e^{-j(\omega t+\varphi_1)} + \\ \quad + E_v t_3^2 t_2^2 r_1 (1-\alpha_3)(1-\alpha_2) \cdot e^{-j(\omega t+\varphi_2)} \end{array} \right] \end{aligned} \tag{8}$$

For more understandable presentation, the product will be written by combining individual coefficients into groups:

$$I_R \propto {E_V}^2 \left(\begin{array}{l} A + B\left(e^{-j\varphi_1} + e^{+j\varphi_1}\right) + \\ +C\left(e^{-j\varphi_2} + e^{+j\varphi_2}\right) + D\left(e^{-j(\varphi_2-\varphi_1)} + e^{+j(\varphi_2-\varphi_1)}\right) \end{array} \right) \tag{9}$$

$$\begin{aligned} A &= r_3^2 + r_2^2 t_3^4 (1-\alpha_3)^2 + r_1^2 t_3^4 t_2^4 (1-\alpha_3)^2 (1-\alpha_2)^2 \\ B &= r_3 r_2 t_3^2 (1-\alpha_3) \\ C &= r_3 r_1 t_3^2 t_2^2 (1-\alpha_3)(1-\alpha_2) \\ D &= r_2 r_1 t_3^4 t_2^2 (1-\alpha_3)^2 (1-\alpha_2) \end{aligned} \tag{10}$$

Taking into account the Euler's equation $e^{\pm jx} = \cos x \pm j \sin x$, we obtain:

$$I_R \propto {E_R}^2 \left[A + 2B\cos\varphi_1 + 2C\cos\varphi_2 + 2D\cos(\varphi_2 - \varphi_1) \right] \tag{11}$$

Since we calculate the reflected-light intensity, the reflective and transmission coefficients can be replaced by the reflectance R and the transmission T:

$$R = r^2, \quad T = t^2 \tag{12}$$

To reduce the set of unknowns of equations (4.11), by applying the law R + T = 1, the transmission can be replaced by the reflection and the group of coefficients can be written as follows:

$$\begin{aligned} A &= R_3 + R_2 (1-R_3)^2 (1-\alpha_3)^2 + \\ &\quad + R_1 (1-R_3)^2 (1-R_2)^2 (1-\alpha_3)^2 (1-\alpha_2)^2 \\ B &= \sqrt{R_3 R_2} (1-R_3)(1-\alpha_3) \\ C &= \sqrt{R_3 R_1} (1-R_3)(1-R_2)(1-\alpha_3)(1-\alpha_2) \\ D &= \sqrt{R_2 R_1} (1-R_3)^2 (1-R_2)(1-\alpha_3)^2 (1-\alpha_2) \end{aligned} \tag{13}$$

If we take into account the individual values of the phase angles and the fact that the reflected light intensity depends on the input light intensity, the final equation can be written as:

$$I_R = I_V \left[\begin{array}{l} A + 2B\cos\dfrac{4\pi n_2 L_2}{\lambda} + \\ \quad + 2C\cos\left(\dfrac{4\pi\left(n_2 L_2 + n_1 L_1\right)}{\lambda} + \pi \right) + \\ \quad + 2D\cos\left(\dfrac{4\pi n_1 L_1}{\lambda} + \pi \right) \end{array} \right] \tag{13}$$

We have shown that the total reflected-light intensity I_R of *FPI* with three semi-reflective surfaces can be described as a linear superposition of three cosine spectral components with distinctive spectral frequencies, which are determined by the length of the resonator, the refractive index (*RI*) of the transmission medium and the wavelength of light.

Further presented interrogation method involve straightforward solution for independent readout of individual *FP* resonators path length variations. Method based on discrete Furrier transform (*DFT*) of sensor's optical spectrum followed by phase tracking of corresponded frequency component. Basic definition of *DFT* is:

$$X_k = \sum_{n=0}^{N-1} x_n e^{-j\frac{2\pi}{N}nk}, \quad \mathrm{k} \in \{0,1,...,N-1\} \tag{14}$$

Where X_k is Fourier transform at k-th frequency component, N is the number of samples, and x_n is the n-th sample, which is then multiplied by a complex matrix of real and imaginary values. The method is especially useful because it enables us to calculate a complex matrix in advance, which depends only on the number of input samples. If we are interested only in changing the phase of a predefined frequency component, it is sufficient to calculate only the k-th component of the complex matrix, which additionally saves the processor time. When multiplying the input data with the k-th component, we obtain a complex number x+jy from which the value of the phase is calculated:

$$\varphi = \arctan\frac{\mathrm{Im}}{\mathrm{Re}} = \arctan\frac{y}{x} \tag{15}$$

The spectral characteristic in the wavelength space does not have a pure cosine characteristic, as the distance between the adjacent peaks is not constant regarding wavelength axis. To get a clean periodic cosine characteristic, the wavelength should be replaced by frequency taking into account basic law $\lambda=c/f$, where c presents speed of light in vacuum and f frequency. The mathematical model from equation (13) is transformed into the following form in the frequency domain:

$$I_R = I_V\left[\begin{array}{l} A+2B\cos\dfrac{4\pi n_2 L_2 f}{c}+ \\ \quad +2C\cos\left(\dfrac{4\pi\left(n_2L_2+n_1L_1\right)f}{c}+\pi\right)+ \\ \quad +2D\cos\left(\dfrac{4\pi n_1 L_1 f}{c}+\pi\right) \end{array}\right] \tag{16}$$

To show significance of frequency domain and of applying a Gaussian window, we simulated dual cavity *FPI*, calculate *DFT* in wavelength and frequency domain, once with and once without Gaussian window. One example of simulated spectrum is shown on Fig.2.

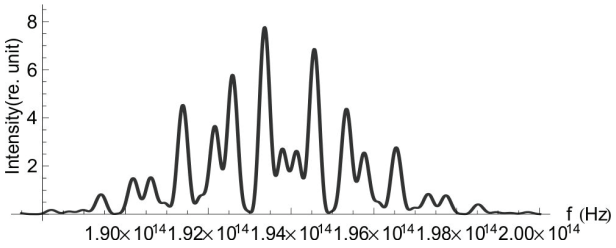

Figure 2: Typical back-reflected spectrum of dual FPI (L_1=100 μm, L_2=160 μm, n=1.45) with applied Gaussian window.

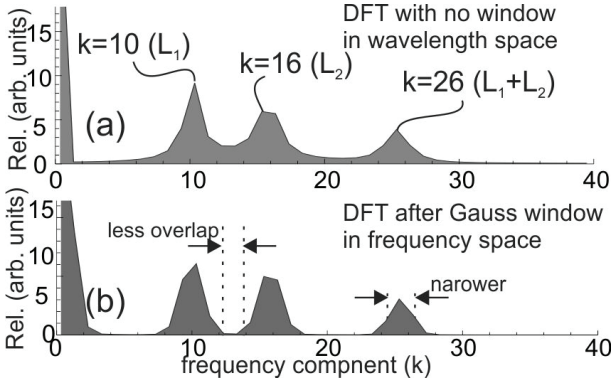

Figure 3: Simulated *FP* sensor with dual cavity length L_1=100 μm, L_2=160 μm, n=1.45, wavelength sweep was from 1510 to 1590 nm: (a) *DFT* in wavelength space with no applied window, (b) *DFT* in frequency space with Gaussian window.

The simulation results show that *DFT* in frequency domain with Gaussian window helps to isolate the individual frequency component to minimize crosstalk between them. The crosstalk between both components was reduced from few degrees to less than ±0.01 degree, when varying L_1 and observing phase change of L_2.

3 Multiparameter fiber optic sensors

Multiparameter fiber optic sensors are created by using micromachining technique based on selective etching [17]. Selective etching is a highly effective tool for realization of various optical sensors and microdevices. In general, the creation of a microdevice

based on selective-etching requires the design and manufacturing of a specially doped structure forming fiber (*SFF*). A short section of *SFF* is then spliced at the tip or in-between the lead-in single mode fibers (*SMF*) and then etched into the final structure. The tip of the *SFF* can also be directly etched into the desired microphotonic structure when the *SFF* incorporates a waveguide structure.

One example produced by selective etching is shown in Fig. 4.

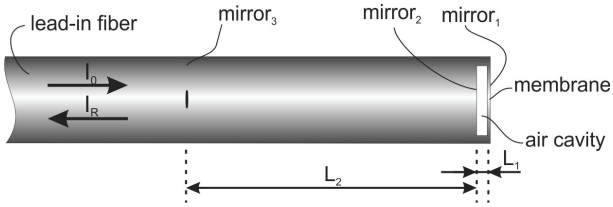

Figure 4: Dual parameter pressure-temperature sensor.

The sensor's design utilized dual all-fiber *FP* resonators with distinctive lengths that permitted straightforward spectrally-resolved interrogation of the sensor [12]. First shorter pressure sensitive *FP* resonator (L_1) is located on the fiber tip and consists of thin silica membrane and inner reflective surface. Temperature is measured by observing the optical path length change of the second *FP* resonator (L_2), which is mainly temperature dependent due to the silica's *RI* dependence on the temperature (i.e. *dn/dT* of silica corresponds to about 10^{-5} K^{-1}) Temperature measurements with all-silica structure positioned between two reflective surfaces is involved almost at all further presented sensors.

The temperature and pressure were efficiently and unambiguously determined by signal processing of the reflected optical-spectra. Reflected optical spectra of typical sensor is presented in Fig. 5.

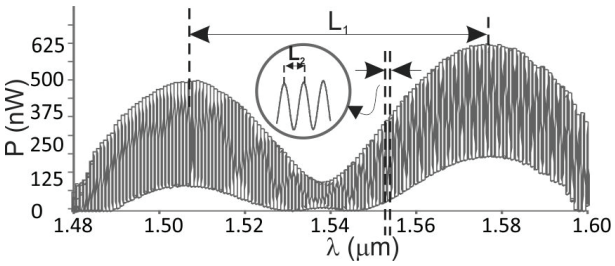

Figure 5: Output spectral characteristic of temperature pressure sensor (L_1=17 μm, L_2=1000 μm).

The sensor can be easily modified to cover different pressure and temperature ranges. In particular, its all-silica design and miniature size provides potential opportunities for its usage in high-temperature, biomedical and micro-fluidic systems.

Another example of multiparameter sensor is shown in Fig. 6, and present a miniature, all-silica, dual-parameter *FP* sensor for simultaneous measurement of surrounding fluid's *RI* and temperature [14]. Sensor consists of two stacked *FPI*, first *FPI* is U-shaped microcell for *RI* change measurements and second *FPI* is temperature sensitive segment. This sensor permits a full temperature-compensated high resolution *RI* measurement in range of 10^{-7} refractive index unit (*RIU*) as is shown on Fig. 7. High resolution measurement can be used to determine very small changes in fluid structure or composition. All-silica design provides high chemical and thermal inertness, while the miniature size provides opportunities for measuring very small (*nL*) fluid volumes.

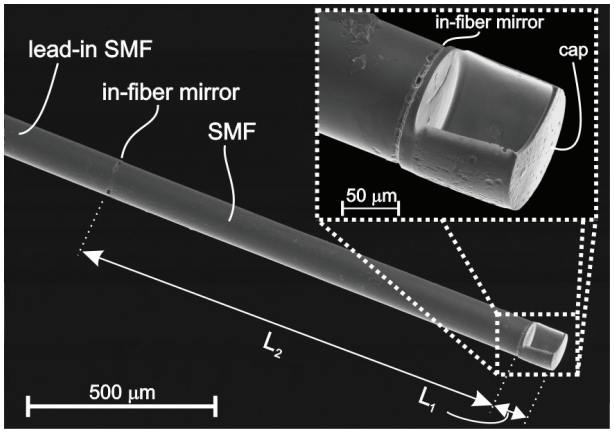

Figure 6: Dual parameter RI-temperature sensor.

Next example in Fig. 8 shows one more complex multiparameter *FP* sensor for simultaneous measurement of pressure and refractive index [13]. Sensor consists of microcell that allows surrounding fluid to freely enter inside to provide the detection of fluid's *RI* through the measurement of the microcell's optical path length.

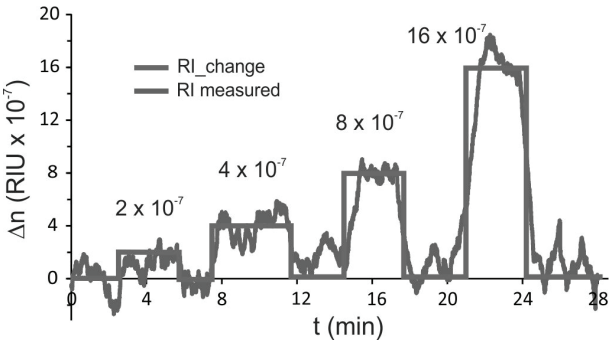

Figure 7: Demonstration of system RI resolution under varying temperature conditions.

Pressure measurements is realized by *FPI* created between thin silica diaphragm and inner reflective surface.

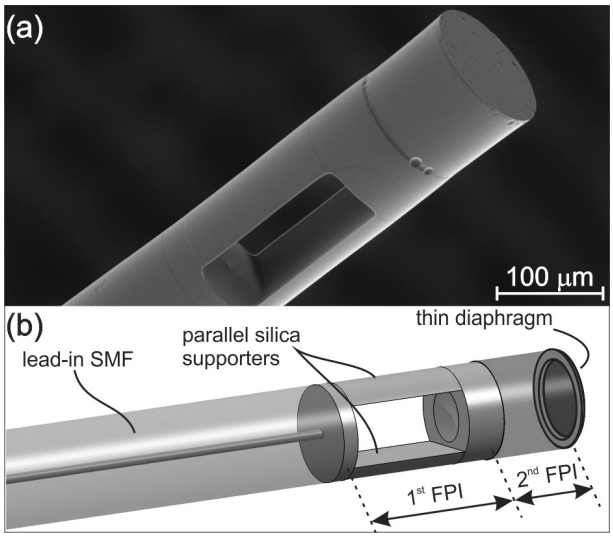

Figure 8: Pressure-refractive index sensor, (a) SEM photo, (b) proposed sensor design.

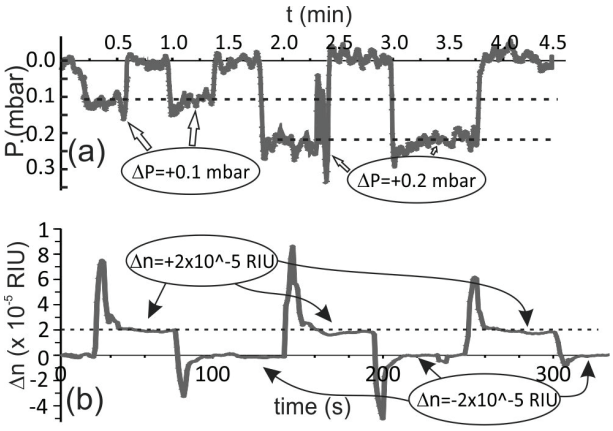

Figure 9: Sensor's response to P and *RI* change: (a) pressure resolution demonstration, (b) *RI* resolution demonstration.

High measurement resolutions better than 0.1 *mBar* and 2x10^{-5} *RIU* can be achieved by using spectral interrogation and a *DFT*-based measurement algorithm.

Another example of multiparameter sensor is shown in Fig. 10, and present a miniature, all-silica, dual-parameter *FP* sensor for simultaneous measurement of relative humidity (*RH*) and temperature [15].

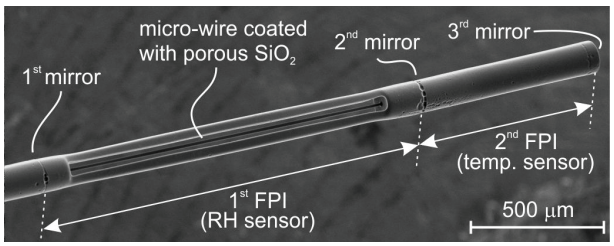

Figure 10: SEM image of RH sensor.

The sensor is composed of two cascaded *FPI*. The first *FPI* consists of a short silica micro-wire (diameter is cca. 13 μm) "sandwiched" in-between two semi-reflective in-fiber mirrors (mirrors 1 and 2 in Fig. 10).

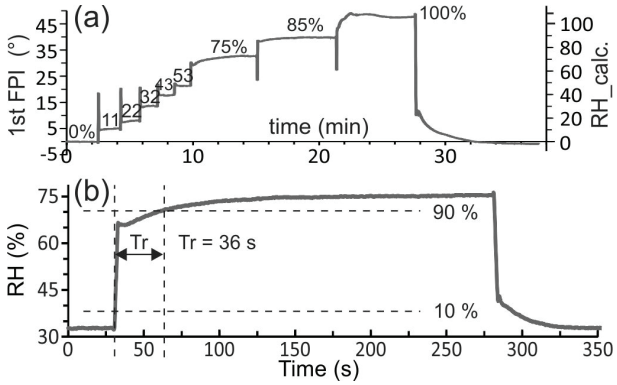

Figure 11: (a) Response of produced sensor to humidity change using about a 600 *nm* thick porous SiO_2 layer, (b) Dynamic response of *RH* sensor.

Micro-wire is coated by a thin layer of porous silica, and forms a *RH* sensing part. The second *FPI* consists of section created on the sensor tip that forms a temperature measuring part. The typical total length of produced sensor is less than 2 mm, while diameter doesn't exceed 125 μm. The sensor has good dynamic performances and covers broad *RH* measuring range as shown in Fig. 11. Sensor has also linear characteristics for both measurement parameters with sensitivity of 0.48 degree/%RH and 3.7 degree/°C.

The last and the most complex device is multiparameter all-silica fiber optic sensor for simultaneous measurement of pressure, *RI*, temperature and thermal conductivity of gases [16]. It is one of the few truly fiber solutions that allows measuring more than three parameters simultaneously.

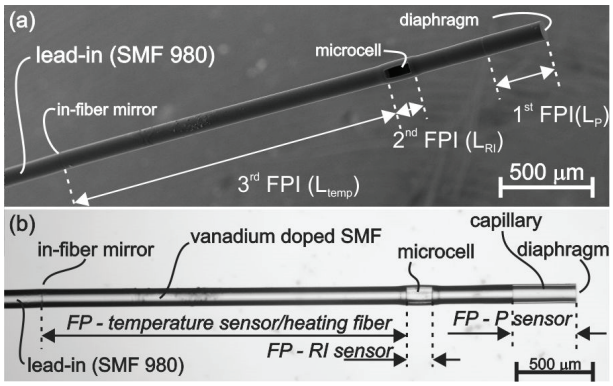

Figure 12: Fabricated multiparameter sensor: (a) *SEM* image; (b) optical microscope image.

The sensor utilizes three different *FPI* stacked on the tip of a lead-in optical fiber. The first *FPI* is made of a thin-wall glass capillary and thin silica diaphragm located on the top of the sensor structure. The *2nd FPI* is open path U-shaped all-silica microcell, which allows for free access of the surrounding gas in-between the *FPI's* semi-reflective surfaces and, thus, for gas *RI* measurements. A short section of Vanadium-Doped Fiber placed in between an in-fiber mirror and semi-reflective surface defines the *3rd FPI*. Vanadium doping induces high optical absorption at shorter wavelengths (i.e. 980 *nm*), while the increase in absorption near 1550 *nm* remains limited/low [18]. This *3rd FPI* performs two functions: Temperature sensing and thermal conductivity measurement. Temperature is measured by observing the optical path length change of the *3rd FPI*. On the other hand, the thermal conductivity is measured by application of active heating of this temperature sensitive segment.

Sensor has high repeatability and high resolutions of all four sensed parameters (a temperature resolution of 2 *mK*, pressure resolution of 1 *mbar*, *RI* resolution of 5x10^{-7} *RIU* and thermal conductivity of better than 1x10^{-3} *W/mK* were achieved).

4 Conclusions

This paper presented design and interrogation of many multiparameter Fabry-Perot sensors that are all capable of measuring at least two parameters simultaneously. Experimental results regarding crosstalk confirmed that independent and simultaneous readout of stacked *FP* resonators on the optical fiber is possible, which is consistent with simulated results obtained from a mathematical model.

In the future, sensors could be produced with even more *FP* resonators (more than 3), which is entirely feasible with this kind of micromachining technology and with this kind of signal interrogation, but it however increases the complexity of the sensor and hence also the price efficiency in compared to using multiple individual sensors.

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6 References

1. P. Lutzow, D. Pergande, and H. Heidrich, "Integrated optical sensor platform for multiparameter biochemical analysis," Opt Express 19, 13277-13284 (2011). https://doi.org/10.1364/Oe.19.013277
2. Y. P. Xu, P. Lu, S. Gao, D. Xiang, P. Lu, S. Mihailov, and X. Y. Bao, "Optical fiber random grating-based multiparameter sensor," Opt Lett 40, 5514-5517 (2015). https://doi.org/10.1364/Ol.40.005514
3. V. Bhatia, "Applications of long-period gratings to single and multi-parameter sensing," Opt Express 4, 457-466 (1999). https://doi.org/Doi 10.1364/Oe.4.000457
4. Y. Chamorovskiy, "Specialty Optical Fibres for a Sensing Application," Inform Midem 40, 285-290 (2010).
5. H. Y. Meng, W. Shen, G. B. Zhang, C. H. Tan, and X. G. Huang, "Fiber Bragg grating-based fiber sensor for simultaneous measurement of refractive index and temperature," Sensor Actuat B-Chem 150, 226-229 (2010). https://doi.org/10.1016/j.snb.2010.07.010
6. S. Pevec and D. Donlagic, "Miniature fiber-optic Fabry-Perot refractive index sensor for gas sensing with a resolution of 5x10−9 RIU," Opt Express 26, 23868-23882 (2018). https://doi.org/10.1364/OE.26.023868
7. M. Boerkamp, Y. Y. Lu, J. Mink, Z. Zobenica, and R. W. van der Heijden, "Multiple Modes of a Photonic Crystal Cavity on a Fiber Tip for Multiple Parameter Sensing," J Lightwave Technol 33, 3901-3906 (2015). https://doi.org/10.1109/Jlt.2015.2448763
8. R. Biswas, "Low-cost wavelength-selective evanescent fiber optic temperature and refractive index sensor," Eur Phys J Plus 132(2017). https://doi.org/ARTN 207 10.1140/epjp/i2017-11509-6
9. W. Luo, S. Chen, L. Chen, H. L. Li, P. C. Miao, H. Y. Gao, Z. L. Hu, and M. Li, "Dual-angle technique for simultaneous measurement of refractive index and temperature based on a surface plasmon resonance sensor," Opt Express 25, 12733-12742 (2017). https://doi.org/10.1364/Oe.25.012733
10. M. M. Ali, M. R. Islam, K. S. Lim, D. S. Gunawardena, H. Z. Yang, and H. Ahmad, "PCF-Cavity FBG Fabry-Perot Resonator for Simultaneous Measurement of Pressure and Temperature," Ieee Sens J 15, 6921-6925 (2015). https://doi.org/10.1109/Jsen.2015.2468065
11. A. Samir and B. Batagelj, "A seven-core fibre for fluorescence spectroscopy," Inform Midem 47, 49-54 (2017).
12. S. Pevec and D. Donlagic, "Miniature all-fiber Fabry-Perot sensor for simultaneous measurement of pressure and temperature," Appl Optics 51, 4536-4541 (2012). https://doi.org/10.1364/Ao.51.004536
13. S. Pevec and D. Donlagic, "Miniature fiber-optic sensor for simultaneous measurement of pressure and refractive index," Opt Lett 39, 6221-6224 (2014). https://doi.org/10.1364/Ol.39.006221
14. S. Pevec and D. Donlagic, "High resolution, all-fiber, micro-machined sensor for simultaneous measurement of refractive index and temperature," Opt Express 22, 16241-16253 (2014). https://doi.org/10.1364/Oe.22.016241
15. S. Pevec and D. Donlagic, "Miniature all-silica fiber-optic sensor for simultaneous measurement of relative humidity and temperature," Opt Lett 40, 5646-5649 (2015). https://doi.org/10.1364/Ol.40.005646
16. S. Pevec and D. Donlagic, "MultiParameter Fiber-Optic Sensor for Simultaneous Measurement of Thermal Conductivity, Pressure, Refractive Index, and Temperature," Ieee Photonics J 9(2017). https://doi.org/10.1109/JPHOT.2017.2651978
17. S. Pevec, E. Cibula, B. Lenardic, and D. Donlagic, "Micromachining of optical fibers using the selective etching of doped silica glass," Micro-Optics 2012 8428(2012). https://doi.org/10.1117/12.922045
18. Z. Matjasec, S. Campelj, and D. Donlagic, "All-optical, thermo-optical path length modulation based on the vanadium-doped fibers," Opt Express 21, 11794-11807 (2013). https://doi.org/10.1364/Oe.21.011794

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Najvišja priznanja v slovenski znanosti v letu 2018

Odbor za nagrade, ki mu predseduje prof. dr. Janez Plavec, je 27. 11. 2018 v Cankarjevem domu v Ljubljani podelil najvišja priznanja za dosežke na znanstveno raziskovalnem in razvojnem področju. Slavnostni govornik na prireditvi je bil predsednik Republike Slovenije Borut Pahor.

Zoisovo nagrado za življenjsko delo sta prejela dr. Milica Kacin Wohinz in akad. prof. dr. Boštjan Žekš, Puhovo nagrado za življenjsko delo pa prof. dr. Franc Vodopivec. Zoisovo nagrado za vrhunske dosežke v znanosti so prejeli prof. dr. Marko Noč, prof. dr. Matjaž Perc in prof. dr. Robert Dominko. Puhovo nagrado za vrhunske dosežke na razvojnem področju je prejel univ. dipl. ing. Marjan Pipenbaher. Zoisova priznanja so prejeli **izr. prof. dr. Mojca Benčina, prof. dr. Saša Prelovšek Komelj, izr. prof. dr. Andreja Kutnar, prof. dr. Nina Gunde Cimerman, prof. dr. Janez Košmrlj in doc. dr. Tadej Rojac,** Puhovo priznanje pa Leon Kralj. Priznanje ambasador znanosti Republike Slovenije je prejel prof. dr. Bogdan Povh.

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