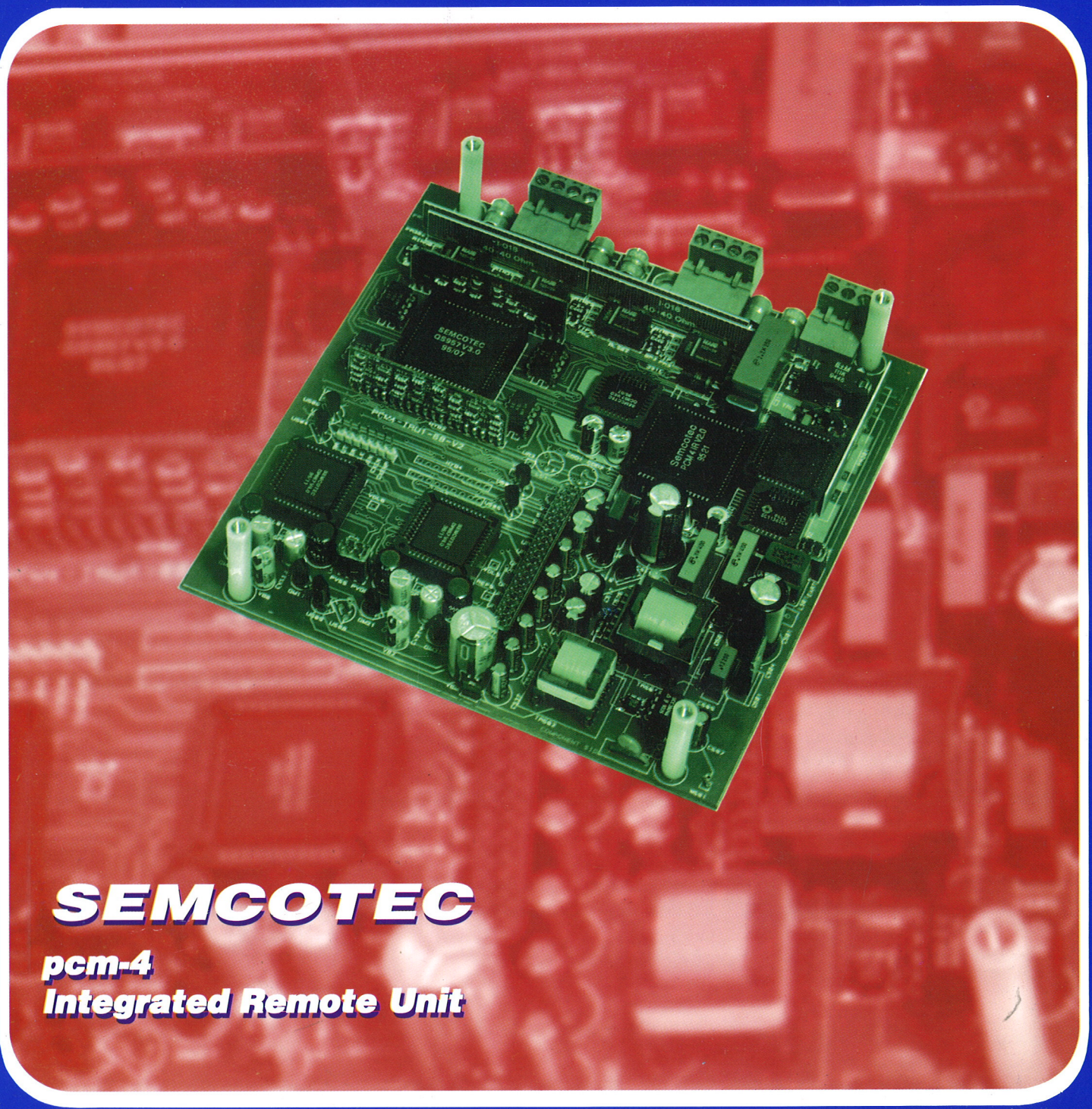
UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

INFORMACIJE MIDEM 3·1995

Strokovno društvo za mikroelektroniko elektronske sestavne dele in materiale

Časopis za mikroelektroniko, elektronske sestavne dele in materiale
Časopis za mikroelektroniku, elektronske sastavne dijelove i materijale
Journal of Microelectronics, Electronic Components and Materials

INFORMACIJE MIDEM, LETNIK 25, ŠT. 3(75), LJUBLJANA, september 1995



INFORMACIJE MIDEM 3 ° 1995

INFORMACIJE MIDEM	LETNIK 25, ŠT. 3(75), LJUBLJANA,	SEPTEMBER 1995
INFORMACIJE MIDEM	GODINA 25, BR. 3(75), LJUBLJANA,	SEPTEMBAR 1995
INFORMACIJE MIDEM	VOLUME 25, NO. 3(75), LJUBLJANA,	SEPTEMBER 1995

Izdaja trimesečno (marec, junij, september, december) Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale.
Izdaja tromjesečno (mart, jun, septembar, decembar) Stručno društvo za mikroelektroniku, elektronske sastavne dijelove i materiale.
Published quarterly (march, june, september, december) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

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Scientific Council for Technical Sciences of Slovene Ministry of Science and Technology has recognized Informacije MIDEM as scientific Journal for microelectronics, electronic components and materials.
Publishing of the Journal is financed by Slovene Ministry of Science and Technology and by Society sponsors.

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Grafična priprava in tisk
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Printed by
BIRO M, Ljubljana

Naklada
Tiraž
Circulation
1000 izvodov
1000 primjeraka
1000 issues

UDK621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 25(1995)3, Ljubljana

VSEBINA **CONTENT**

Volitve v organe društva MIDEM

V Portorožu, oktobra 1992, smo izvolili organe društva v sedanji sestavi. Leta so se hitro zavrtela in zopet smo pred novimi volitvami, saj je v skladu s statutom društva mandatna doba vseh organov in funkcij tri leta z možnostjo ponovne izvolitve.

*Glede na to, da je MIDEM mednarodno društvo (okoli 30% članov **ni** državljanov Republike Slovenije), in ker Izvršilni odbor želi tudi tujim članom omogočiti aktivno udeležbo na volitvah, se je na svoji seji dne 26.10.1995 odločil izvesti pisne volitve.*

Volili bomo člane naslednjih organov društva MIDEM:

- *Predsednika društva*
- *Izvršilni odbor (15 članov)*
- *Nadzorni odbor (3 člani)*
- *Častno razsodišče (3 člani)*

Na strani 249 pričujočega izvoda revije "Informacije MIDEM" boste našli volilni listič s seznamom imen kandidatov za posamezne funkcije in člane organov društva MIDEM. Prosimo, da listič izpolnite in ga vrnete na naslov društva.

Obveščamo tudi vse tiste člane, ki želijo prebrati STATUT društva MIDEM, da je le-ta na vpogled pri Iztoku Šorliju (MIKROIKS d.o.o., Dunajska 5, Ljubljana, tel. 061 312 898), oz. je bil v celoti objavljen v reviji "Informacije MIDEM" 22(1992)4.

Elections of MIDEM Society Bodies Members

In Portorož, in October 1992, the present members of MIDEM Society Bodies were elected. Years pass and again, new elections are to be held before the end of this year. According to MIDEM Statute all functions and mandate duration is being 3 years by the possibility of reelection.

MIDEM is an international Society (about 30% of its members are from abroad) and since Executive Board wishes to give the opportunity of vote also to the foreign members, it decided to perform written elections.

The following MIDEM Bodies Members will be elected:

- *MIDEM Society President*
- *Executive Board (15 members)*
- *Supervisory Board (3 members)*
- *Court of Honour (3 members)*

On page 249 of this issue of Journal "Informacije MIDEM" You can find electoral leaf with the list of candidates for MIDEM Bodies. Please, return the leaf to MIDEM address.

Those who want to read the STATUTE of MIDEM Society are welcome to call Iztok Šorli (MIKROIKS d.o.o., Dunajska 5, 61000 Ljubljana, tel.+386 61 312 898) who will make it available for You. As well, in Journal "Informacije MIDEM" 22(1992)4, full text in Slovene and English language was published.

MIDEM Society President

Dr. Rudolf Ročak

UDK621.3:(53+54+621+66), ISSN 0352-9045 Informacije MIDEM 25(1995)3, Ljubljana

RADIATION EFFECTS IN SILICON COMPONENTS FOR SPACE APPLICATIONS

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Keywords: semiconductors,radiation effects, silicon components, space applications, device physics, radiation hardness, material science, MOS devices, CMOS devices, submicron CMOS, bipolar components, CCD, Charge Coupled Devices, SOI, Silicon-On-Insulator, JFET transistors, defect engineering, gettering, noise performance, ionization damages, displacement damages, semiconductor technologies, bipolar technologies, bipolar devices, Si-SiO_2 interfaces, threshold voltage, silicon technologies, burnout, SEB, Single Event Burnout, MOSFET deficiencies, JFET transistors, TEOS, Tetra-Ethil Ortho-Silicate glass

Abstract: Radiation effects are of crucial importance for space applications, which are a growing niche market of microelectronics. This paper reviews the impact of both ionising and bulk damage effects on the electrical performance of microelectronic silicon components, including Silicon-on-Insulator technologies (SOI), Charge Coupled Devices (CCDs), submicron CMOS, and standard and advanced bipolar components. Beside an overview of the general device characteristics, information will also be given on the underlying physical models. Some measures for obtaining radiation-hard devices are briefly addressed.

Učinki sevanja na silicijeve elektronske sestavne dele namenjeni uporabi v vesolju

Ključne besede: polprevodniki, učinki sevanja, deli sestavni silicijevi, uporaba v vesolju, fizika naprav, odpornost proti sevanju, znanost o materialih, MOS naprave, CMOS naprave, CMOS submikronski, deli sestavni bipolarni, CCD naprave, SOI tehnologije silicij-na-izolantu, JFET transistorji, inženiring hib, getranje, zmogljivost šumna, poškodbe ionizacijske, poškodbe premestitve v mreži atomski, tehnologije polprevodnikov, tehnologije bipolarne, naprave bipolarne, Si-SiO_2 plasti vmesne, napetost pragovna, tehnologije silicija, izgoretje, SEB izgoretje posamično, MOSFET poškodbe, JFET transistorji, TEOS steklo

Povzetek: Učinki sevanja na silicijeve elektronske sestavne dele so bistvenega pomena za uporabo komponent v vesolju, kar postaja vse bolj rastoči trg uporabe mikroelektronike. V prispevku pregledno opisujemo efekte ionizirajočih in notranjih poškodb na električne karakteristike mikroelektronskih sestavnih delov na siliciju vključujoč tehnologije SOI (Silicon-on-Insulator), CCD (Charge Coupled Devices), submikronski CMOS ter standardne in napredne bipolarne tehnologije. Poleg pregleda splošnih električnih karakteristik komponent podajamo tudi ustrezni opis fizikalnih mehanizmov. Na kratko opišemo korake, s pomočjo katerih lahko izdelamo komponente, ki so odporne proti sevanju.

1. INTRODUCTION

About 25% of the Military/Aerospace integrated circuit market is taken by radiation-hard devices, with an increasing importance of the space applications. Major microelectronics applications in a spacecraft are related to telecommunications, scientific instrumentation, data handling, imaging, earth observation, and teledetection. The general microelectronic trends to increase the packing density, to enhance the circuit functionality, and to reduce the power consumption are also becoming important in this field. However, it is well-known that advanced processing steps used in submicron silicon technologies make these technologies more vulnerable to radiation effects so that the required hardness levels can only be obtained by both the implementation of radiation hard process modules and the optimisation at the design level. This paper will mainly focus on the impact of the technological parameters on the radiation hardness.

The space environment consists of a large variety of particles such as electrons, neutrons, protons, heavy particles, X-rays, γ-rays ... with energies ranging from a few keV to GeV. The amount of irradiation encountered by the devices depends on a variety of parameters such as the amount of shielding, the altitude of the polar orbit in combination with the influence of well-known space phenomena such as the Von Allen belts, solar flares, and the South Atlantic Anomalies /1/. Therefore the on-earth simulation of the space environment remains very difficult and is mainly restricted to the simulation of the impact of some dedicated irradiation particles.

Depending on the type of the irradiating particles one has to differentiate between respectively ionising irradiation (e.g. γ irradiations), mainly causing irradiation damage in the silicon dioxide layer and at the Si-SiO_2 interface, and irradiation resulting in displacement damage (e.g. protons, neutrons and electrons) in the semiconductor lattice. In general, the impact of irradiation on the electrical performance will be revealed by a change of the threshold voltage, a reduction of the mobility, a degradation of the transconductance, a reduction of the charge transfer efficiency, a degradation of the current gain, an increase of the leakage current, a reduction of the carrier minority lifetime, single event upsets, latch-up, and an increase of the low frequency noise. Extensive information on these topics is published in the proceedings of the annual IEEE Nuclear and Space Radiation Effect Conference and of the bi-annual European RADECS Conference. A comprehensive compilation of the relevant literature in this field till 1992 can be found in /1/.

This paper will briefly discuss some basic physical phenomena, before discussing more in detail the radiation hardness of different technologies such as Silicon-on-Insulator (SOI), Charge-Coupled Devices (CCD), submicron CMOS, and bipolar technologies. Some alternative technologies will also be briefly addressed. It is an update and extension of a previous review paper by the authors on this topic /2/. Due to space limitations only general trends and some special phenomena will be discussed. Some challenges and future trends will also be highlighted.

2. PHYSICAL IRRADIATION MODELS

Ionising irradiations lead to the formation of defects in the silicon dioxide and at the Si-SiO_2 interface resulting into the generation of the oxide trapped charge and of the interface trap density. This damage will cause a shift in the threshold voltage of MOS devices. A huge amount of publications are dealing with a possible explanation for the involved defect creation mechanism. Presently, two different schools exist /3-4/. On one hand it is believed that due to the irradiation electron-hole pairs are formed in the oxide, whereby the electron is very mobile and the hole moves towards the interface. It is generally accepted that interface traps are trivalent silicon atoms with a dangling bond. After device processing these dangling bonds are saturated due to the hydrogen passivation, so that for modern technologies the interface trap density is very low and in the 10^9-10^{10} cm^{-2} eV^{-1} range. The irradiation-generated holes will lead to broken bonds once they reach the interface, thereby increasing the interface trap density. The oxide traps are believed to be trivalent silicon atoms with an oxygen vacancy and have been identified by electron spin resonance studies. This model is called the trapped-hole model. Another theoretical model, called the hydrogen diffusion model, is based on the fact that during irradiation hydrogen ions throughout the oxide are formed which under positive gate bias may diffuse to the interface and thus creating interface traps according to the following radiochemical reaction /5/

$$\equiv Si\text{-}H + H^+ + e^- \Leftrightarrow \equiv Si\text{-}H + H^0 \Leftrightarrow \equiv Si\text{-} + H_2 \qquad (1)$$

Due to the electron tunneling from the substrate through the oxide, the hydrogen ion is transformed into a hydrogen atom. The hydrogen atom is very reactive and reacts with a saturated silicon bond in order to form an interface trap (dangling bond) and a hydrogen molecule that diffuses away. Although there still exists a lot of controversy about the exact model, more and more experimental evidence is given for the validity of the hydrogen diffusion model.

Detailed studies by Fleetwood and co-workers /6-7/ resulted into a generally accepted nomenclature for the irradiation induced oxide defects. Dependent on the location of the generated traps, distinction is made between bulk oxide traps, border traps and interface traps. This is schematically illustrated in Fig. 1. The reaction time of the generated traps allows a further classification into 'fixed' and 'switching' states. The switching states are those which have an impact on the dynamic operating conditions (e.g. low frequency noise) of the devices. Both states will have an influence on the threshold voltage. Special measurement techniques have been proposed to separate the influence of the oxide and interface trapped charge.

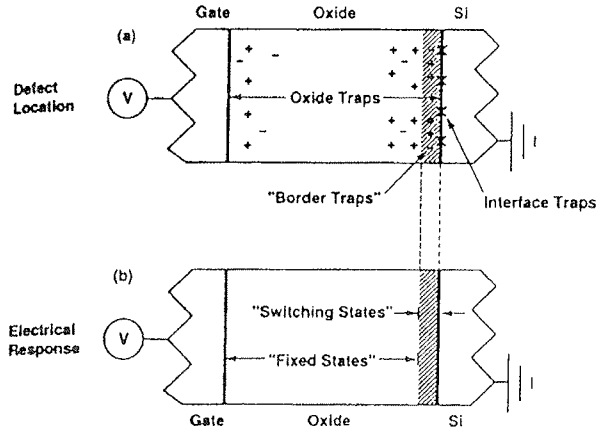

Figure 1: Schematic illustration of the used nomenclature to differentiate between the physical location and the electrical response of the irradiation induced charges, after Fleetwood et al. /7/. 'Border traps' are located in the oxide near the interface and can exchange charge with the Si substrate on the time scale of the measurement.

Dependent on the irradiation conditions a certain amount of energy will be deposited into the silicon material and may therefore result into so-called displacement damage, as reviewed recently /8/. The displacement damage will mainly consist of a variety of defects such as isolated intrinsic defects (self-interstitials and/or vacancies) and defect complexes and defect clusters. In recent years, the authors have used a large variety of electrical and structural analysis techniques (such as TEM, DLTS, infrared spectroscopy, laser scattering tomography, photoluminescence, electrical I-V and C-V measurements, lifetime measurements, low frequency noise spectroscopy) in order to identify and to characterize the electrical behavior of these defects after proton, electron and neutron irradiations /9-11/. Special attention has been given to the impact of the quality of the starting silicon material, i.e. Czochralski (Cz) Si with different interstitial oxygen concentrations - Float Zone - Epitaxial wafers - high resistivity silicon, on the hardness against displacement damage. This study also included the influence of the implementation of gettering treatments, originally intended to reduce the amount of process-induced defects.

3. IRRADIATION HARDNESS OF SILICON TECHNOLOGIES

This section is intended to give an overview of some general features of the radiation hardness of different silicon technologies. Although the irradiation behaviour of several electrical parameters has been extensively studied during the last decade, less attention has been given to the low frequency noise behaviour of devices in a space environment. This topic has recently been reviewed by the authors /12-13/ and will also briefly be mentioned here.

3.1 Silicon-on-Insulator (SOI) Technologies

To improve the total dose irradiation hardness of MOS technologies, Silicon-on-Sapphire (SOS) technologies were introduced around the mid-sixties. The thin silicon film on the insulating substrate (Al_2O_3), in which mesa transistors are fabricated, has a reduced carrier lifetime due to the interfacial lattice mismatch. Although these technologies still have a beneficial irradiation behaviour from a viewpoint of single event upset (SEU) and resistance against so-called gamma-dot upsets caused by solar flares or nuclear explosions, for many space applications SOI technologies have gained a larger market share. It is even so that at the annual IEEE SOS/SOI Technology Workshop only a few papers are still dealing with SOS. For SOI wafers the thin silicon film, which is separated from the silicon substrate by a buried insulator layer, can be obtained by oxygen implantation (SIMOX), wafer bonding and etch back (BESOI) and zone melting recrystallisation (ZMR). The main advantages of using a thin silicon film are latch-immunity, reduced leakage currents, increased SEU thresholds, and the elimination of leakage currents associated with parasitic transistors /14/. For space applications radiation levels between 50 and 100 krad(Si) are sufficient. In addition to several microprocessors, radiation hardened 256k and 1 Mbit SRAMs have also successfully been fabricated on SIMOX material. The trend in device scaling is surely making SOI a winner compared to SOS as for the latter the end-of-life is mentioned to be around the 1.2 μm level.

In SOI devices the irradiation sensitivity is mainly related to the different Si-SiO_2 interfaces associated with the gate oxide, the buried oxide and the isolation oxides respectively. Therefore attention has been given to the impact of both the gate oxide temperature and the isolation scheme used /15/. Hardened devices are obtained by lowering the gate oxidation temperature and by implementing a MESA-LOCOS isolation, whereby a deep trench is etched in the Si film before the sidewalls are oxidized, instead of a standard LOCal Oxidation of Silicon (LOCOS). This is clearly illustrated in Fig. 2, showing that for hardness levels up to 100 krad(Si) a maximum threshold voltage shift of 100 mV is obtained. Also the post-irradiation low frequency noise behaviour is strongly influenced by the isolation scheme as can be seen in Fig. 3 /16/. In strong inversion no difference is observed, while in the subthreshold region the noise strongly increases for the LOCOS device. For the MESA-LOCOS device the noise increase is much smoother. The observed noise spectra are $1/f^n$ like with

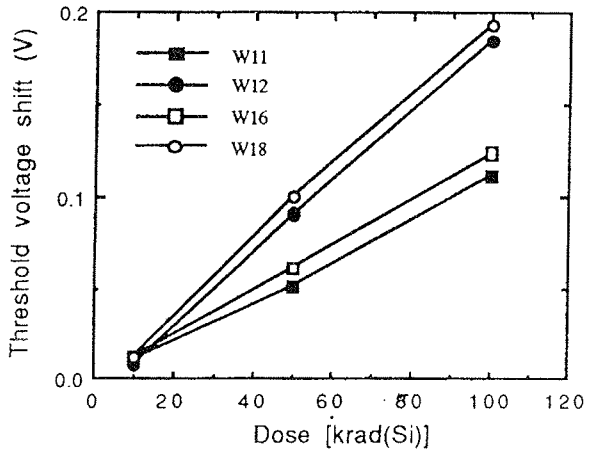

Figure 2: Threshold voltage shift of a SOI nMOST as a function of the total irradiation dose for different isolation schemes and gate oxidation temperatures (W 11: MESA-LOCOS/850°C; W 12: MESA-LOCOS/975°C; W16: LOCOS/850°C: W18: LOCOS/975°C). Irradiations are done for worst case biasing conditions.

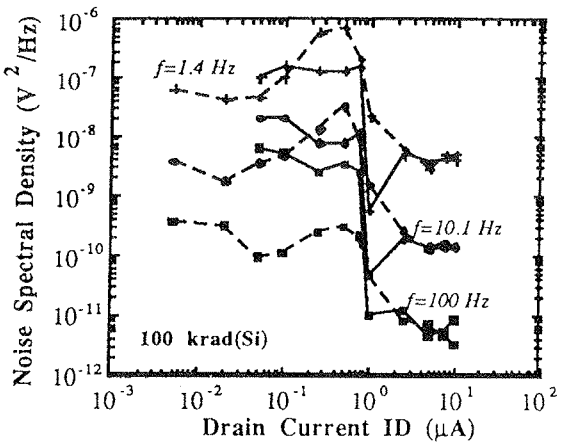

Figure 3: Low frequency noise spectral density of irradiated MESA-LOCOS (dashed lines) and LOCOS nMOSTs for three different frequencies.

n slightly larger than 1. Investigations also pointed out that irradiations have a negligible impact on the excess noise in the kink region of the devices. Hardened SOI technologies are often using an additional boron implantation at the bottom of the silicon film in order to compensate for the irradiation-induced positive charge build-up in the buried oxide as otherwise an inversion layer would be formed /15/. This can only be done for partially depleted devices as fully depleted devices are processed on rather thin silicon films which implies that there is a coupling between the front- and back interfaces.

Other measures to increase the irradiation hardness of SOI devices are either design related, such as e.g. the use of body ties and/or edgeless transistors, or modifying the transistor concept. An example of the latter is to use Gate-All-Around (GAA) or dual gate MOSTs, whereby there is a thin oxide all around the gate /17/. These GAA devices allow total dose levels up to 30 Mrad(Si) /18-19/. An interesting feature is that while the threshold voltage shows a serious rebound after Mrad(Si) irradiations, the low frequency noise has a turn-around behaviour for increasing irradiation doses. The maximum transconductance is a decreasing function of the total dose. The rebound effect is associated with a compensation of the near-interface oxide traps by the interface traps and can be reduced by optimizing the radiation hardness of the gate oxide /19/.

3.2 Charge Coupled Devices (CCD)

CCDs are frequently used for imaging purposes on board of spacecrafts and orbital satellites, so that extensive research has been performed during the last decade. For these devices not only ionizing irradiation but also irradiation-induced bulk damage have a strong impact on the electrical performance and reliability of the devices. In Europe extensive research in this field has been performed by EEV (UK), Thomson (F), IMEC (B) and research groups such as e.g. SIRA, Brunell and Leicester University (UK). For reducing the dark current a dithering technique, a multiphase pinned (MPP) or a virtual phase CCD technology are often used. The ionization damage causes charge build-up in the gate oxide layers resulting in a shift of the threshold voltage, while the generation of interface traps leads to an increase of the surface dark current. In addition transient effects may be observed. Displacement damage produces trapping centres in the silicon substrate, which in turn leads to a reduction of the charge transfer efficiency and the production of dark current spikes and a Random Telegraph Signal (RTS) behaviour.

Systematic studies have been performed in order to investigate the impact of technological parameters on the total dose radiation hardness /20-22/. The standard IMEC n-type buried channel, triple poly and double metal 3 μm CCD technology was evaluated up to 73 krad(Si) and it was observed that i) there is a 3x increase of the dark current density, ii) a high hole trapping factor of 0.6, iii) a high subthreshold leakage, and iv) severe reverse annealing effects after irradiation /20/. By technological modifications such as replacing the solid-source doping at 950°C by an ion implantation, reducing the thermal budget after gate oxidation by restricting the maximal temperature to 800°C, and changing the plasma enhanced CVD reflow oxide in the back end by a tetra-ethyl ortho-silicate glass (TEOS), the radiation hardness level has been increased to 100 krad(Si) /21/. Some typical results are shown in Fig. 4. The modified process is characterized by a threshold voltage shift of 14 mV/krad(Si), a hole trapping factor of 0.04, a dark current increase of less than 2 times, and an increase in interface trap charge of about 2×10^9 cm^{-2} eV^{-1}. A different behaviour of the storage and image region of a Frame Transfer CCD has also been observed /22/. Due to the presence of a metal light shield on the

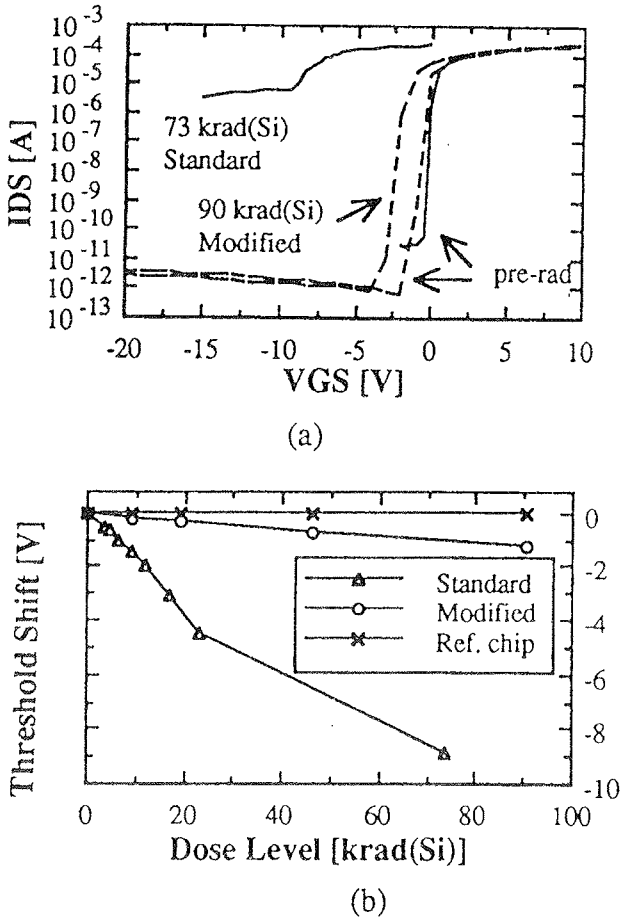

Figure 4: Typical subthreshold (a) and threshold voltage shift (b) as a function of irradiation dose level for the standard and the radiation-hardened CCD process.

storage region, the sintering step in forming gas leads to a large amount of active hydrogen-containing species in the oxide layers. The latter results in a pre-irradiation reduction of the interface trap density, but is at the same time responsible for a higher interface trap density build-up during ionizing irradiation, in agreement with the hydrogen model discussed in section 2 and characterized by eq. (1). This phenomenon is illustrated in Fig. 5, giving the evolution of the average interface trap density during irradiation and subsequent annealing for a CCD device with the sintering step before or after etching the Al light shield.

As already mentioned, CCDs are also very sensitive to irradiation-induced bulk damage. Therefore the authors have studied in detail the impact of the quality of the substrate material and some technological parameters on the radiation hardness of the devices /9-11/. A variety of proton, ^{252}Cf and electron irradiations resulted into the following main conclusions. The oxygen content of the starting material has a strong impact on the radiation resistance, and the best results are obtained for low oxygen wafers and epitaxial material. The degrading impact of the oxygen content has been confirmed by

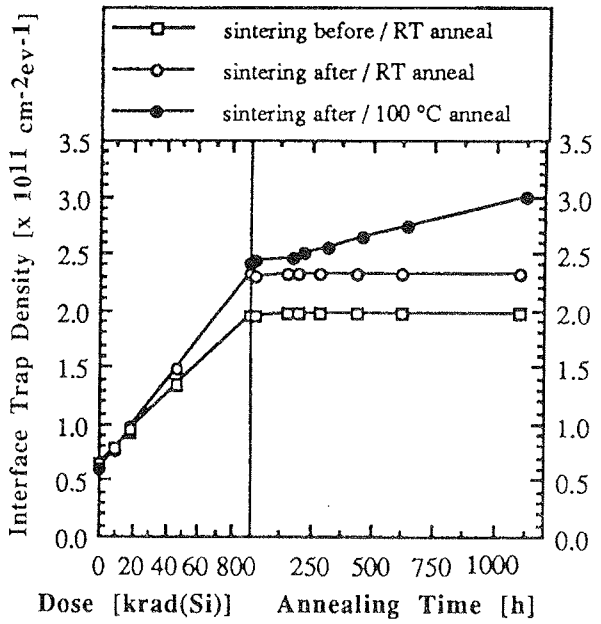

Figure 5: Average interface trap density determined from charge pumping measurements on gate oxide transistors of the radiation hardened CCD process as a function of the accumulated dose level and the subsequent annealing time. A difference is made between a sintering step before or after etching of the Al light shield.

electrical characterizations of diodes, TEM analysis, photoluminescence measurement, and DLTS analysis. The SiO_x precipitates and their associated dislocations are responsible for minority carrier traps in p-type silicon, characterized by two deep levels at E_C-0.17 and E_C-0.43 eV, leading to an increase of the leakage current. While in irradiated p-type silicon the majority traps related with carbon (interstitial carbon-substitutional carbon C_iC_s or interstitial carbon-interstitial oxygen C_iO_i complexes) dominates the leakage current, in n-type irradiated silicon this is the case for majority traps associated with vacancies (E-centres or di-vacancies). The implementation of an internal gettering step may also have a beneficial impact on the radiation hardness. The technological importance of these conclusions are for the moment being validated by evaluating the radiation hardening of a 1024x1024 CCD processed in a 1.25 µm CCD-CMOS technology.

Reduction of the bulk damage is important for the use of CCDs in a near-Earth space environment. A systematic study by Hopkinson /23/ concerning the radiation-induced dark current increase points out that the surface dark current increase due to ionization damage is bias dependent and shows a large reverse annealing effect, while the bulk damage generates dark current spikes and may introduce temporal fluctuation similar as RTSs. These RTSs, which have time constants up to 1 hour, are believed to be due to bistable lattice defects, i.e. defects with two stable configuration, corresponding to a different charge state.

It is also important to mention that beside technological modifications the radiation hardness can further be improved by optimizing the design. In addition, the radiation sensitivity also depends on the device operating conditions (e.g. operating bias, operating temperature, in-situ annealing affects).

3.3. Submicron CMOS Technologies

Bulk CMOS technologies are inherently more radiation sensitive than SOI technologies. However, typical features of commercial bulk CMOS devices are: total dose hardness >1 x 10^6 rad(SiO_2), dose rate upset hardness to 1 x 10^9 rad(Si)/sec, dose rate survivability to 1 x 10^{12} rad(Si)/sec, SEU hardness for flip-flops and SRAMs to 1 x 10^9 -1 x 10^{10} upsets/bit/day, and neutron fluence hardness to 1 x 10^{14} cm^{-2} /24/.

A further scaling of the devices to the deep submicron region requires the implementation of several advanced processing steps which will have an impact on the radiation hardness. Some of these technological process modifications are briefly discussed. The switching to so-called ultraclean processing in order to maintain the stringent material specifications concerning defects and contamination of the starting silicon has a beneficial impact on the radiation hardness. The use of thinner gate oxides results in a strong improvement of the radiation hardness as in general the irradiation-induced threshold voltage shift ΔV_t follows a power law with the gate oxide thickness t_{ox} /1/:

$$\Delta V_t \approx t^n_{ox} \qquad (2)$$

with n ranging between 1 and 3, depending on the oxide growth conditions. Ultrathin oxide (10-30 nm) have been reported to be harder than predicted by eq. (2), which

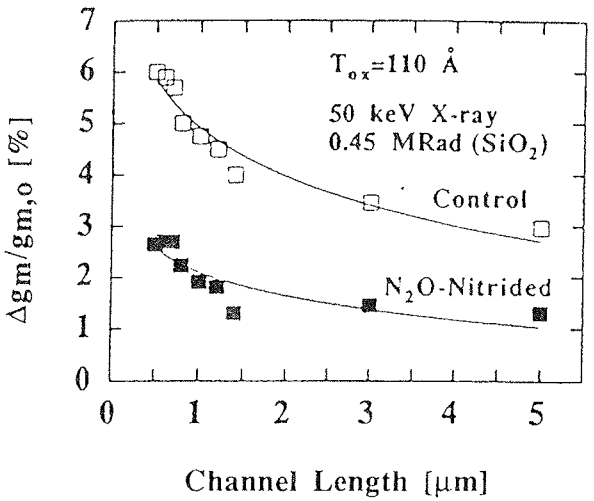

Figure 6: Comparison of the X-ray irradiation sensitivity of a standard and a N_2O-nitrided oxide. The normalized degradation of the peak transconductance is shown as a function of the effective device length /26/.
(dose rate 10 krad(SiO_2)/min).

might be due a compensation of the oxide trapped holes by tunnel electrons. For a complete picture one also has to take into account the impact of additives to the oxide growth ambient (e.g. Cl, F, Ar, N ...), the oxide growth temperature and the post-oxidation anneal conditions. Recent work even seems to indicate that threshold voltage shift due to oxide trapped charge is less oxide thickness dependent (n = 2.8) than the shift caused by the interface trapped charge (n = 4.3) /25/. Another beneficial influence on the radiation hardness of the gate oxides is the use of N_2O-nitrided (NO) /26/ or reoxidised nitrided (RNO) structures /27/, as illustrated in Fig. 6 for a NO oxide. Field oxides can be hardened by sandwich structures such as a P- or As-doped deposited oxide on a thin thermal oxide /28/. Modern transistors concepts such as Lowly Doped Drain (LDD) surely impacts the radiation hardness. Especially in the spacer regions irradiation-induced charge can be trapped.

3.4 Bipolar Devices

Irradiations degrade the common emitter current gain β of bipolar junction transistors by increasing the base current without significantly impacting the collector current This is caused by either displacement damage in the bulk reducing the minority carrier lifetime or by ionizing irradiation of the oxide covering the emitter-base junctions, whereby the oxide trapped charge results in a spreading of the field induced depletion layer in the base region and the interface traps increase the minority carrier surface recombination velocity /29/. The decrease in effective doping of the base of NPN transistors will be less pronounced for relatively heavy base doping as well as a very narrow base width. The effective surface recombination velocity versus the ionizing dose rate is illustrated in Fig. 7 /30/, showing very clearly that the surface recombination velocity not only increases with the total dose but also depends on the dose rate. While the highest values are observed for a low dose rate, there is a tendency to level off at high dose rates. A similar behaviour is noticed for the excess base current. Fig. 8 gives a typical behaviour of the current gain characteristics for various total dose levels /31/.

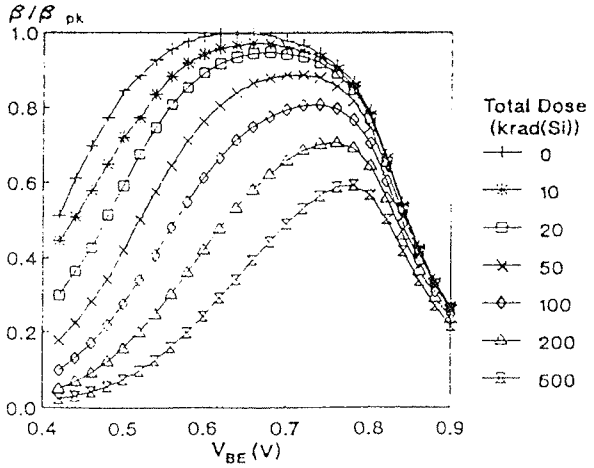

Figure 8: Typical common emitter current gain characteristics for various levels of total dose. The post-irradiation current gain is normalized to the peak pre-irradiation current gain β_{pk}, after Nowlin et al. /31/.

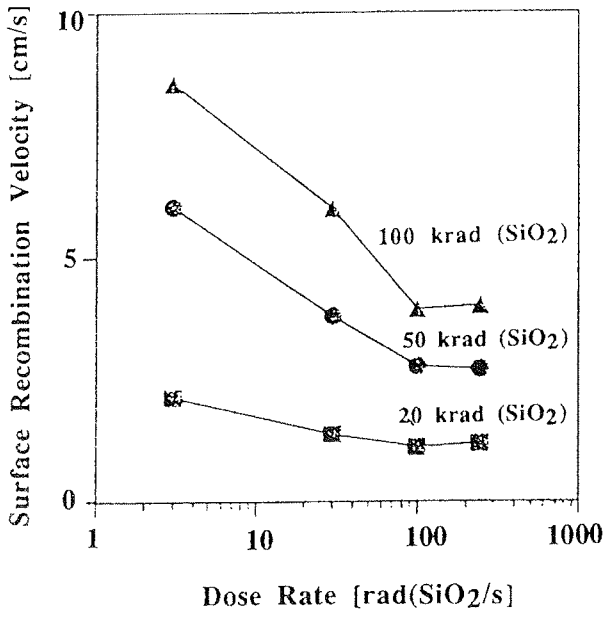

Figure 7: Variation of the effective surface recombination velocity calculated at a 0.6 V base emitter voltage versus the dose rate and for various total dose levels, after Wei et al. /30/.

A systematic study of different modern bipolar technologies leads to the following conclusion /31/: i) NPN transistors degrade more severe than PNP transistors, due to the build-up of positive charge in the oxide covering the base region, ii) devices with small emitter perimeter-to area ratios are less radiation sensitive than devices with a larger ratio, iii) the collector bias has no impact on the gain degradation, iv) the worst case irradiation condition is with a reverse bias on the emitter, v) large base-emitter voltages give a smaller increase in base current, and vi) poly emitter devices are initially harder than standard emitter devices, but are becoming worse at larger total doses. During the last years there is also a strong interest in SiGe HBTs because of their excellent electrical behaviour and their potential for cryogenic applications /32/. Recently, initial irradiation studies have been reported, indicating that up to a total dose of 1 Mrad(Si) these devices are radiation hard both at room temperature and at liquid nitrogen temperature /33/. However, at 77 K the behaviour of the base current is influenced by Poole-Frenkel trap assisted tunneling. Irradiations initially increase the tunnel base current, while there is a decrease for higher dose levels. Irradiations only have a limited influence on the low frequency noise behaviour by a slight increase of the generation-recombination centres resulting in a Lorentzian hump on the 1/f noise.

The authors have performed a systematic study of the impact of the quality of the starting silicon on the radiation hardness of junction diodes after a variety of proton, ^{252}Cf, electron, and neutron irradiations (see e.g./9-11, 34-36/). Some important conclusion have already been mentioned in section 3.2. The impact of different kinds of irradiation on the gated diode characteristics of one particular type of Cz n^+p junction diode is illustrated in Fig. 9. The shift of the gated diode step towards more negative gate voltage indicates a shift in the flatband voltage of the 100 nm thick gate oxide, due to the creation of ionization damage, i.e., trapped holes. The increase in the reverse current step after irradiation indicates the creation of interface traps, while the increase in the back-ground reverse current is mainly due to displacement damage in the substrate. From this figure, one can conclude that γ-irradiations predominantly cause ionization damage and negligible bulk damage, while the high energy particle irradiations (e^-, H^+) cause both.

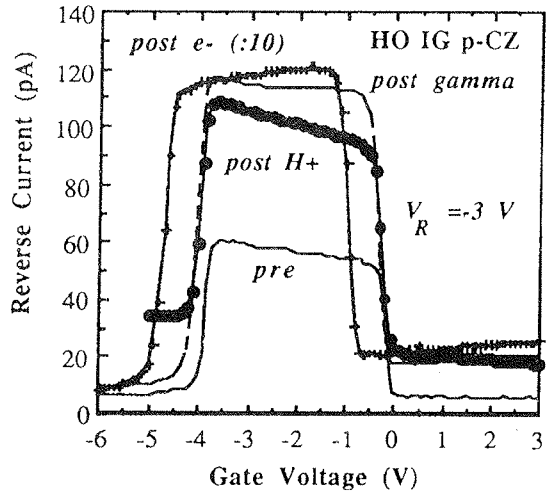

Figure 9: Gated diode characteristics before (full line) and after irradiation with:14 krad(Si) γ- (dash); 10 MeV 2x10^{10} H^+/cm^2 (circle) and 2 MeV 10^{13} e^-/cm^2. The reverse diode bias is -3 V.

In addition it can be stated that ^{252}Cf irradiations have a much higher defect generation efficiency than proton irradiations, but for the interpretation of the data one has to take into account the defect profile in silicon substrate. Detailed noise studies pointed out that the pre- and post-irradiation low frequency noise spectra can be described by a semi-empirical model

$$S_I = C\frac{I_F^B}{f^\gamma} \qquad (3)$$

with for proton irradiations $1.5 < B < 2$ and $0.65 < \gamma < 1.2$ for the diode current noise S_I. More information on the correlation between the irradiation-induced bulk damage and the LF noise performance can be found in /12/. It has to be remarked that the observed noise behaviour can not be explained by the standard available noise models.

The LF noise characteristics of electron irradiated diodes are somewhat peculiar as for FZ material the LF noise at low forward current levels decreases after irradiation. A theoretical model is under development and will take into account the relative importance of the surface G-R noise component and the noise associated with oxygen-related bulk G-R centres.

3.5 Other Technologies

There are still other silicon based technologies which are used for space applications and which have not been discussed here due to page restrictions. Junction field-effect transistors (JFETs) are less sensitive than MOSFETs as it is a bulk type device, with current conduction based on majority carriers. They are less sensitive to ionization bulk damage than bipolars. These devices are of special interest for detector front-end electronics in colliders as they are radiation tolerant and allow monolithic integration. Gamma irradiation levels up to 100 Mrad(Si) and neutron fluences in the range 4x10^{14} n/cm^2 have been reported /37/. Another promising approach for the fabrication of fully integrated pixel detectors is the use of high-resistivity (5-10 kΩcm) SOI wafers whereby the detector diodes are fabricated in the high resistivity substrate, while the CMOS read-out and amplification electronics are located in the thin silicon top layer /38/. A schematic cross-section of such a device is shown in Fig.10.

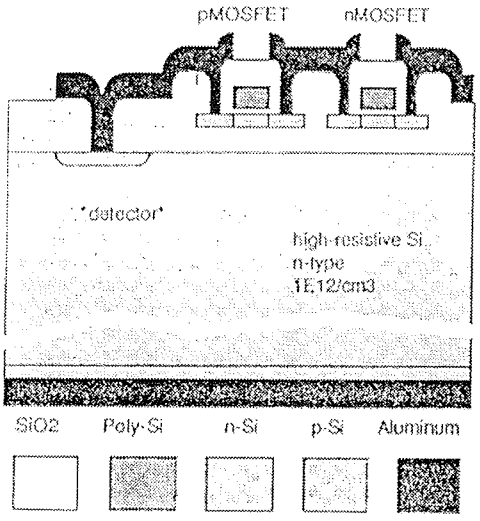

Figure 10: Schematic cross-section of the monolithic integration of CMOS electronics and particle diodes in high-resistiviy SOI wafers.

Special attention should be paid to the use of Power MOSFETs in radiation environments. Beside the standard MOSFETs deficiencies, an important phenomenon is the occurrence of Single Event Burnout (SED) result-

ing in a drain-source and drain-gate short. Important parameters to control are the operating voltages, the operating frequency, the applied voltage in the off state, and the operating temperature. It is essential to differentiate between the static and the dynamic operation of the devices and to take into account the irradiation parameters (e.g. type of particle, energy, stopping power, incident angle ...).

Finally it should be mentioned that there exists an increasing interest in the radiation hardness of sensor and/or microsystems due to their increasing functionality and fields of applicability. A discussion of that topic is out of the scope of the present paper.

4. CONCLUSIONS

It may be stated that silicon components remain the key electronic elements for space applications. This is mainly due to a better understanding of the physical mechanisms underlying the radiation hardness so that radiation resistant devices can be fabricated. This paper has only discussed the impact of technological parameters, but also on the design side there are plenty of measures that can be implemented. Only for dedicated applications, II-VI and III-V technologies are a competitor of the silicon technologies. During the last years the research efforts concerning radiation hardened technologies has been triggered and Europe is playing a more important and leading role.

ACKNOWLEDGMENTS

Part of this work has been performed with financial support from ESTEC, under contract No. 8515/90/NL/PM(SC). Although a large number of people have to be thanked for many stimulating discussion, special acknowledgment is given to J.P. Colinge, I. Debusschere, B. Dierickx, B. Johlander and L. Adams for their input and for the use of co-authored results.

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Prispelo (Arrived): 05.09.95 *Sprejeto (Accepted): 03.10.95*

OSNOVE RAČUNALNIŠKEGA MODELIRANJA PROCESNEGA KORAKA PLANARIZACIJE

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Ključne besede: polprevodniki, IC vezja integrirana, tehnologije mikroelektronske, osnove fizikalne, modeliranje računalniško, modeliranje numerično, modeliranje procesov, simulacije procesov, simulacije korakov procesnih, procesi planarizacije površine, planarizacija topografije, plasti planarizacijske, BPSG stekla boro-fosfo-silikatna, SOG steklo tekoče nanešeno centrifugalno, difuzija površinska, metode fizikalne, metode tekočinske, Navier-Stokes enačbe, oprema programska

Povzetek: V preglednem članku so predstavljene fizikalne osnove različnih modelov za simulacijo procesnega koraka planarizacije pri proizvodnih postopkih izdelave integriranih elektronskih vezij. Podrobneje sta opisana modela planarizacije s tanko plastjo močno dopiranega silicijevega dioksida in tanko plastjo tekočega stekla.

Physical Foudations of Computer Modeling of Planarization Processes

Keywords: semiconductors, IC, integrated circuits, microelectronic technologies, physical foundations, computer modelling, numerical modelling, process modelling, process simulations, process step simulations, planarization processes, topography planarization, planarization layers, BPSG, Boro-Phospho-Silicate Glasses, SOG, Spin-On Glass, surface diffusion, physical methods, liquid methods, Navier-Stokes equations, software

Abstract: In this review paper physical foundations of planarization process computer models are discussed. As planarization is becoming of crucial importance for processes with small lateral dimensions (i. e. <1,2 μm), the need for a reliable computer model of this process is increasing. One approach to process modelling is to start from "the first principles"; at later stages of modelling this, approach usually requires extensive simplifications and omissions of the relatively small terms in the equations in order to keep the model within computing power of present day computers. The other approach is to fit parameters of a model as to match the result of simulation to experimental data.

One of the possible classifications of planarization techniques is to physical and to liquid methods. Based on our experimental investigations described elsewhere we focused on finding a model for planarization with borophosphosilicate glass (BPSG) layer among physical methods, and for planarization with spin-on glass (SOG) among liquid methods, therefore the two are treated in more detail. Different models of planarization are compared and evaluated with regard to possibility of their incorporation into existing process simulation software packages.

We conclude that the most promising model of physical planarization at present time is the model of "surface diffusion"; also, it is already a module in the process simulation program SAMPLE, and therefore easily accessible. In this model free surface energy is considered as the driving force that forms the topography of planarization layer. Planarization layers are regarded as layers of liquids with different viscosities. When viscosity of a liquid is appropriately low, liquid can flow in such a manner as to minimize the surface energy. This flow is called surface diffusion. Material properties, environment and other parameters are implicitly defined in variable diffusion coefficient.

Lubrication model of planarization can very accurately predict form of a topography planarized with liquid methods, but is less useful for predicting the results of planarization with physical methods. The essence of this model is solving the Navier-Stokes equations. In spite of the accuracy of predictions for cases within model limitations, the model is not yet incorporated in commercially available process simulation software.

As an example of a model which is based on fitting parameters to experimental data, a model is described that regards planarizing layer as a low pass filter. The starting topography of an IC with many steps and trenches is regarded as a high frequency signal and on the planarized surface only low frequencies are allowed. When the values of parameters in this model are based on large numbers of experimental data, the model can be very accurate and used for predicting the forms of planarized surfaces. Even though the model is computationally very simple it is not yet integrated in a process simulation program as a module.

In spite of different approaches and many attempts to validate simulation results with experimental data, simulations can not yet accurately predict the form of planarized surface, therefore new work and investigations of planarization processes are still necessary.

1. Uvod

Programi za simulacijo procesnih korakov lahko pri razvoju in modifikaciji procesa proizvodnje integriranih vezij prihranijo veliko časa in stroškov. Vzporedno z razvojem procesnih korakov zato običajno razvijajo tudi matematične modele za njihovo simulacijo. Dva pristopa sta k izgradnji simulacijskih modelov:

Prvi pristop izhaja iz obstoječih rezultatov meritev. Pri takem modelu se rezultati meritev in napovedi modela navadno dobro ujemajo. Kadar pa se pojavi neskladje med rezultati meritev in napovedmi modela je potrebno popraviti parametre, ki nastopajo v modelu in navadno je nastajanje dobrega modela tega tipa iterativen postopek. Za dober model na osnovi rezultatov meritev potrebujemo statistično signifikantno število merilnih rezultatov, kar je lahko drago in zato opravičljivo le za izdelavo modelov, ki bodo koristili velikoserijski proizvodnji.

Drugi pristop izhaja iz podrobnega poznavanja fizikalnih osnov procesnega koraka. Pri izdelavi modela tega tipa

najprej poskusimo določiti vse veličine relevantne v nekem procesnem koraku in nato ugotoviti njihovo medsebojno delovanje. Za kontrolo tako nastalih modelov procesnih korakov nam služijo merilni rezultati. Pogosto je pri modelih, ki izhajajo iz fizikalnih osnov, problem v tem, da zaradi zapletenega dogajanja v njih nastopajo poenostavitve in je od poenostavitev odvisno kako dobro simulacije nekega procesnega koraka lahko opisuje realno dogajanje. Razlog za poenosta-vitve je seveda omejena zmogljivost računalnikov. Po drugi strani pa je res, da so današnji računalniki, kljub omejitvam, že povsem primerni za simulacije na osnovi fizikalnih modelov.

Obstoja več programov za simulacijo procesnih korakov proizvodnje integriranih elektronskih vezij (SAMPLE, SUPREM, SUPRA, DEPICT2, SPEEDIE) /1, 2/. Za nove modele je ugodno, če jih lahko vgradimo v obstoječe programe in zato modeli za nove procesne korake navadno nastanejo v obliki modulov. Seveda je pogoj za uspešno vgradnjo novega modula za simulacijo nekega procesnega koraka v obstoječi program, da je združljiv z njegovimi vhodnimi in izhodnimi.

Med izdelavo integriranega vezja na silicijevi rezini na njeno površino na različnih mestih nanašamo prevodne, izolacijske in druge plasti; zato dobiva površina rezine, ki je bila spočetka sicer ravna, vse bolj razgibano topologijo, ki otežuje izdelavo integriranega vezja. Postopek planarizacije pa zniža prehode med ravni-nami na površini tabletke (čipa). Največje višinske razlike na površini tabletke integriranega vezja nasta-nejo proti koncu njegove izdelave in za sledeče fotolitografske postopke ter postopke naprševanje je ugodno, pri majhnih kritičnih dimenzijah integriranih vezij (<1,2 μm) pa celo nujno, da je površina vezja uravnana.

2. Numerično modeliranje planarizacijskega postopka

Pri reševanju problematike planarizacije se je izoblikovalo več pristopov /3/. Različni pristopi se razlikujejo po nastanku in sestavi plasti za planarizacijo. Ena od možnih delitev je na fizične in fluidne metode. Pri fizičnih metodah planarizacije na površino silicijeve rezine najprej nanesemo dielektrično plast z ostrimi prehodi, ki jo nato z drugim fizičnimi procesi zgladimo (na primer nataljevanjem dopiranega silicijevega dioksida nanešenega iz plinske faze). Pri fluidnih metodah dielektrična plast nastane iz suspenzije ali raztopine reaktantov v ustreznem topilu, zato ima izhodiščna snov nizko viskoznost. Zaradi nizke viskoznosti lahko površinska napetost uravna površino dielektrične plasti. Površinski napetosti pomagamo še s centrifugalnim nanašanjem planarizacijskega materiala. Takšna planarizacija je, na primer, nanašanje tekočega stekla ali organskih planarizacijskih materialov.

Poznavanje fizikalnih dogajanj pri planarizaciji je že dovolj dobro, da ne predstavlja več bistvenih omejitev v primerjavi z zmogljivostmi računalnikov.

Kljub pomembnosti tankih plasti iz tekočega stekla za planarizacijo v proizvodnji integriranih vezij še vedno ni natančnega opisa prav vseh dogajanj pri nastajanju teh plasti, ker se pri tem srečujemo s prevelikim številom pojavov, ki bi jih morali upoštevati. Primer do pred kratkim zanemarjenega vpliva je vpliv topologije prehodov v okolici obravnavanega prehoda na izravnavanje. Sprememba položaja in velikosti elementov vezja v okoliški topografiji prehoda ter spremembe kemijske zgradbe plasti pod tanko plastjo iz tekočega stekla, lahko spremenijo debelino nanešenega polimera pri planarizaciji s tanko plastjo iz tekočega stekla.

2.1 Model difuzije površine

Model difuzije površine je uporaben za napovedovanje oblike planarizirane površine vezja po tečenju močno dopiranega stekla (boro-fosfo-silikatno steklo, BPSG), nanešenega iz plinske ali tekoče faze. Osnovni mehanizem pri uravnavanju površine, ki je prekrita z dopiranim steklom, je delovanje površinske napetosti pri povišani temperaturi. Kot vsaka tekočina, tudi nataljeno steklo teži k temu, da bi imelo čim manjšo površinsko energijo. Pri tem modelu podrobna kinetika spreminjanja oblike površine ni pomembna, privzeta pa je difuzija materiala iz področij z višjo površinsko energijo v področja z nižjo energijo. Na ta način se površinska energija celotne površine zniža /4/. Na tem mestu ne bomo obdelovali natančnega mehanizma tega procesa, ampak le pokazali, da se da s sprejetimi predpostavkami narediti model, ki dobro opiše končno obliko površine vezja po planarizaciji.

Prednost tega modela pred drugimi je tudi v tem, da se njegovi vhodni in izhodni podatki zelo lahko prilagodijo obliki, ki jo uporablja priljubljeni program za simulacijo procesnih korakov SAMPLE. V programu SAMPLE so mnogi modeli za druge procesne korake, zato lahko enostavno simuliramo celoten kompleksen postopek planarizacije, ki vključuje tudi fotolitografske, depozicijske in korake jedkanja.

2.1.1 Osnovne predpostavke modela

Prosta energija površine je proporcionalna velikosti površine, kar opisuje naslednja enačba:

$$F = \gamma A \qquad (1)$$

kjer je F prosta energija površine, γ površinska energija na enoto površine (površinsko napetost) in A površina. Lokalno ukrivljenost površine v izbrani točki (x, y) opišemo z dvema glavnima krivinskima radijema R_1 in R_2, ki ležita v ravninah glavnih normalnih presekov (sta negativna pri konkavnih in pozitivna pri konveksnih površinah) /5/. Osi x in y ležita v oskulacijski ravnini v izbrani točki (x, y) in os z paralelno z binormalo. Površina infinitezimalno majhnega dela ukrivljene površine je torej dxdy. Če površini v točki (x, y) dodamo majhen del snovi se površina premakne v normalni smeri, to je v smeri z, krivinska radija v tej točki pa se spremenita. Kemijski potencial μ je definiran kot:

$$\mu = \frac{dF}{dN} = \Omega\gamma(1/R_1 + 1/R_2) \qquad (2)$$

kjer je N število delcev in Ω molekularni volumen. V splošnem se krivinski radiji spreminjajo od točke do točke na površini tekočine, kar pomeni da so gradienti kemičnega potenciala na površini različni od nič in delujejo kot sile, ki povzročajo pretok materiala, kar opisuje enačba:

$$\bar{J} = \frac{\left(D\gamma\nu\Omega^2\right)}{kT}\bar{\nabla}_p\left(1/R_1(p) + 1/R_2(p)\right) \qquad (3)$$

kjer je $\bar{J}$ volumski pretok materiala (na enoto dolžine), ν površinska koncentracija molekul, D difuzijski koeficient površine, k Boltzmannova konstanta in T temperatura. Enačba (3) opisuje transport materiala po površini kot posledico sil, izvirajočih iz površinske energije. D in γ v enačbi nastopata le kot produkt in enačbo poenostavimo:

$$\bar{J} = \frac{D'}{kT}\bar{\nabla}_p\left(1/R_1(p) + 1/R_2(p)\right) \qquad (4)$$

kjer je $D' = D\gamma\nu\Omega^2$ in predstavlja efektivni difuzijski koeficient površine. V limitnem primeru ravne površine, ko gresta krivinska radija proti $\pm\infty$, je pretok materiala po površini očitno enak nič. Robne pogoje lahko izberemo poljubno, parameter(D'/kT)t pa je neodvisen, kjer je t celoten čas pretoka. Imenujejo ga "količino pretoka" in v njem so implicitno upoštevani vplivi temperature, sestave tanke plasti in drugi vplivi okolice.

Kot omenjeno, je model difuzije združljiv s programom SAMPLE. Posebej enostavno v sicer pogostem praktičnem primeru, ko je eden od obeh krivinskih radijev mnogo večji od drugega (cilindrična simetrija).

2.1.2 Modifikacija modela za planarizacijo s tanko plastjo tekočega stekla

Gornji model lahko do neke mere prilagodimo tudi za simulacijo planarizacijskega postopka s tanko plastjo iz tekočega stekla, če upoštevamo izhlapevanje topila med postopkom /11/. Opis izhlapevanja zahteva dva parametra. Tak model je omejen na simulacijo planarizacije gostih prehodov med ravninami vezja, kajti le pri taki topologiji lahko zanemarimo vplive rotacije silicijeve rezine. V simulacijskem modelu sta upoštevana dva procesa, ki imata nasprotne učinke na stopnjo planarizacije: ker je skrček v grobem propocionalen volumnu tekočega stekla, je skrček plasti iz tekočega stekla večji v nižjih delih površine. Nasproten vpliv pa ima težnja, da zapolni nižje dele površine. Za natančen izračun vpliva izhlapevanja topila iz tekočega stekla bi morali rešiti dvodimezionalno difuzijsko enačbo na neplanarni geometriji s premičnimi mejami. Problem je poenostavljen tako, da model predpostavlja s časom eksponencialno upadajočo hitrost krčenja volumna tekočega stekla. Poleg tega je zanemarjeno tudi lateralno krčenje plasti. Simulacija oblike površine planariziranega vezja s tanko plastjo iz tekočega stekla se začne s predpostavko, da je površina takoj po nanosu tekočega stekla ravna.

2.1.3 Modifikacije modela za opis ponovnega tečenja BPSG

Ponovno tečenje je postopek, pri katerem s povišano temperaturo zaoblimo ostro izjedkane prehode kontaktnih odprtin. Model za simulacija tega postopka upošteva posebne robne pogoje, ki so za ta proces značilni. V kontaktnih odprtinah se stikata substrat ter rob plasti stekla in kot omakanja med njima je parameter, ki določa dinamiko procesa. Simulacija poteka v dveh korakih: najprej z nespremenljivo točko stika in s spremenljivim kotom ter nato z nespremenljivim kotom in pomično stično točko. Taka simulacija se dobro ujema z merjenimi rezultati /6/. Še posebej spodbudno je dobro ujemanje dejanskih rezultatov in simulacije razmer pri slabo poravnani kontaktni maski. V takih razmerah so stranice kontaktne odprtine izrazito nesimetrične.

2.1.4 Ocena uporabnosti modela

Model difuzije površine, kljub potrebnim poenostavitvam, dovolj natančno opisuje dogajanje na površini, ki jo želimo planarizirati. Uporaben je pri študiju geometrije planarizirane površine s tanko plastjo BPSG kot tudi s tanko plastjo iz tekočega stekla. Posebna prednost modela pred drugimi je to, da upošteva podatkovno strukturo komercialnega programa za simulacijo procesnih korakov SAMPLE in je zato takoj praktično uporaben.

2.2 Reološki model

Simulacijski modeli planarizacije, ki slone na teoriji mazanja, običajno opisujejo le dogajanje v radialnem prerezu površine (torej dve dimenziji) in opisujejo razmere za nehlapljive tekočine, vendar se jih da dopolniti, da upoštevajo tudi topološke lastnosti povr-šine v tangencialni smeri. Zaradi velike viskoznosti do-piranega silicijevega dioksida, nanešenega iz plinske faze, model ni uporaben za simulacije tega načina pla-narizacije, pač pa je zelo uporaben za opis nanašanja mnogo manj viskoznega tekočega stekla. Posebno dobro opiše tanjšanje plasti tekočega stekla pri nana-šanju /7/. Na obliko površine nanešenega tekočega stekla vplivajo površinska napetost, centrifugalna sila in debelina plasti tekočega stekla. Značilno je, da pri teh modelih na rezultate simulacij vplivajo tudi različne smeri prehodov med ravninami v radialni smeri (iz niže ležeče ravnine na višjo ali obratno). Novi, v nadaljevanju opisani model, do nekoliko upošteva tudi hlapnost planarizacijskega materiala, uporaba starejših tovrstnih modelov pa je nekoliko vprašljiva, ker niso podrobno raziskali njihovih omejitev in veljavnosti.

2.2.1 Osnovne predpostavke modela

Model simulira stopnjo planarizacije (SP), ki je definirana kot:

$$SP = \left(1 - \frac{\Delta d}{v}\right)x100\% \qquad (5)$$

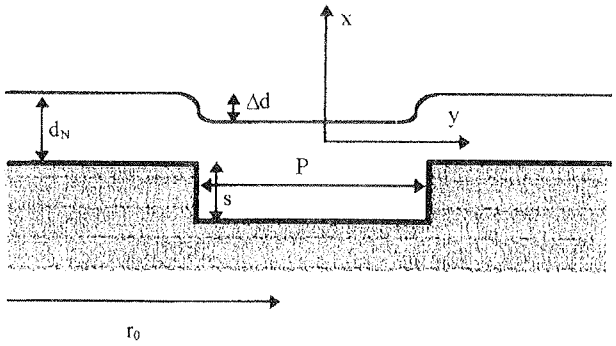
kjer je Δd največja deviacija od nominalne debeline plasti planarizacijskega materiala (n. pr. tekočega

stekla) in v višina prehoda med plastmi (glej sliko 1). Za kvantitativno oceno prevladujočega vpliva pri oblikovanju površine je v modelu definiran brezdimenzijski parameter ϖ^2, razmerje med centrifugalno silo (F_c) in površinsko napetostjo (F_γ), ki delujeta na del planarizacijskega materiala:

$$\varpi^2 = \frac{F_c}{F_\gamma} = \frac{\rho\omega^2 L^3 r_0}{\gamma d_N} \qquad (6)$$

kjer je ρ gostota tekočine, ω kotna hitrost, L širina prehoda, r_0 razdalja prehoda od osi vrtenja rezine in σ površinska napetost raztopine planarizacijskega materiala.

Z reološkim modelom simuliramo tudi značilno brazdo, ki se pojavi v plasti planarizacijskega materiala nekoliko za prehodom iz višje na nižjo ravnino vezja ter grbo, ki sledi obratnemu prehodu. Oba pojava so opazili pri raziskavah, kjer so plast tekočega stekla opazovali med nanašanjem /8/. Ujemanje rezultatov simulacije in meritev je dobro pri prehodih, ki so bili široki glede na njihovo pogostost.



Slika 1: Značilni prehod med ravninami, ki ga je potrebno planarizirati.

P je širina presledka, s višina prehoda med ravninama vezja, d_N nazivna debelina plasti planarizacijskega materiala, Δd maksimalna deviacija debeline plasti od nazivne debeline in r_0 radialna oddaljenost prehoda med ravninama od središča rezine (osi vrtenja).

Opomba: Radi bi opozorili, da je koordinatni sistem v tem primeru orientiran, glede na površino, drugače kot v prejšnjem.

2.2.2 Fizikalna izhodišča za model

Tok planarizacijskega materiala po površini rezine v reološkem modelu planarizacije opisujeta kontinuitetna enačba in momentna enačba (Navier-Stokesova enačba):

$$\nabla \cdot \mathbf{v} = 0 \qquad (7)$$

in

$$\eta \frac{D\mathbf{v}}{Dt} = -\nabla p + \eta \mathbf{g} + \nabla^2 \mathbf{v} \qquad (8)$$

kjer je **v** vektor hitrosti v tekočini, p je tlak v sistemu, **g** je vektor sile teže in η je viskoznost tekočine /9/.

Ker so opazovani prehodi med ravninama vezja običajno ozki v primerjavi z njihovo oddaljenostjo od osi vrtenja ($L << r_0$), lahko enačbi poenostavimo in ju rešujemo le v dveh dimenzijah. Poleg tega zaradi ozkega prehoda med ravninami vezja lahko zanemarimo spreminjanje centrifugalnega pospeška po širini prehoda - torej predpostavimo, da se centrifugalna sila po celi širini prehoda ne spreminja /10/. Dobimo sistem diferencialnih enačb:

$$\frac{\partial v_x}{\partial x} + \frac{\partial v_y}{\partial y} = 0 \qquad (9)$$

$$\rho\left(\frac{\partial v_y}{\partial t} + v_x \frac{\partial v_y}{\partial x} + v_y \frac{\partial v_y}{\partial y}\right) =$$

$$= -\frac{\partial p}{\partial y} + \eta\left(\frac{\partial^2 v_y}{\partial x^2} + \frac{\partial^2 v_y}{\partial y^2}\right) + \rho\omega^2 r_0 \qquad (10)$$

$$\rho\left(\frac{\partial v_x}{\partial t} + v_x \frac{\partial v_x}{\partial x} + v_y \frac{\partial v_x}{\partial y}\right) =$$

$$= -\frac{\partial p}{\partial y} + \eta\left(\frac{\partial^2 v_x}{\partial x^2} + \frac{\partial^2 v_x}{\partial y^2}\right) + \rho g \qquad (11)$$

Pred reševanjem enačbe transformiramo v brezdimenzijsko obliko. Hkrati z normiranjem ocenimo tudi vpliv posameznih členov enačb za tipične vrednosti, ki se pojavljajo pri simulaciji nanašanja tekočega stekla; nekateri členi v enačbah so namreč dovolj majhni, da jih v nadaljnjem obravnavanju lahko zanemarimo. Razdalje v smeri x so normirane z s, ki označuje višino prehoda med ravninama vezja. V starejših modelih so bile razdalje v normalni smeri na ravnino rezine normirane z nazivno debelino plasti tekočega stekla (d_N). Po razmisleku hitro vidimo, da vpliva na tok tekočega stekla višina prehoda med ravninama vezja in ne njegova nazivna debelina, zato je za normiranje bolj primerna višina prehoda med ravninama. Zaradi drugačnega normiranja je izraz za kvocient med centrifugalno in površinsko silo nekoliko drugačen kot v enačbi (6) - v novi obliki je to rotacijsko Bondovo:

$$B = \frac{\rho\omega^2 r_0 L^3}{\gamma s} \qquad (12)$$

Reynoldsovo število (Re), ki izraža relativni vpliv vztrajnostnih sil glede na viskozne, je:

$$Re = \frac{\rho^2\omega^2 r_0 d_N^2 s^2}{\eta^2 L} \qquad (13)$$

Če v izraz vstavimo tipične vrednosti (podane v tabeli 1) za planarizacijo prehodov med ravninama integriranih vezij s tekočim steklom, ugotovimo, da so vrednosti Reynoldsovega števila mnogo manjše od 1, kar pomeni, da je tok tekočega stekla po površini rezine silicija laminaren.

Tabela 1: Tipične vrednosti parametrov za reološki model planarizacije mikroelektronskih vezij

Spremenljivka	oznaka	tipična vrednost
višina prehoda med ravninama vezja	s	1-5 μm
širina prehoda med ravninama vezja	L	1-100 μm
gostota tekočega stekla	ρ	1 g/cm^3
kotna hitrost	ω	3000-8000 vrt./min
oddaljenost prehoda od osi vrtenja	r_0	2,5-10 cm
nazivna debelina plasti tekočega stekla	d_N	1-10 μm
viskoznost	η	0,1-10 kg m^{-1} s^{-1}
koeficient površinske napetosti	γ	0,02-0,04 kg s^{-2}

2.2.3 Ocena uporabnosti modela

V primerjavi s starejšimi modeli, pri katerih je za normalizacijo razdalj v normalni smeri glede na površino rezine služila nominalna debelina plasti planarizacijskega materiala, je nova normalizacija dala dobre rezultate v širšem področju pogojev nanašanja tekočega stekla. Model zelo natančno opisuje dogajanje pri nanašanju tekočega stekla, njegovo utrjevanje pa le približno. Huda pomanjkljivost sicer obetavnega pristopa je, da (po dostopnih podatkih) še ni doživel potrditve kot osnova simulacijskega modula kakega programa za modeliranje procesnih korakov. Druga pomanjkljivost predstavljenega modela je, da ni uporaben za simuliranje planarizacije s tanko plastjo dopiranega silicijevega dioksida, nanešenega iz plinske faze.

2.3 Model nizkega sita

Omenimo še tretji pristop k modeliranju planarizacijske plasti, ki planarizacijsko plast obravnava kot nizko sito za prehode. Tak pristop je še najbližji elektrotehniškemu pristopu analize vezij z metodo "črne škatle". Pri problemu poznamo vhodne podatke (topografijo vezja) in želene rezultate (planarizirano topografijo vezja). S planarizacijsko plastjo moramo priti od vhodnih podatkov do želenega rezultata. Lastnosti planarizacijske plasti so ekvivalentne prevajalni funkciji pri reševanju problemov v vezjih /11/.

2.3.1 Osnovni princip modela

Planarizacijske lastnosti tekočega stekla modeliramo z dvema parametroma. Prehodi med ravninama vezja imajo, glede na njihove različne gostote, tudi različne prostorske frekvence in zaporedje prehodov lahko obravnavamo kot periodičen signal. Planarizacijska plast je namenjena filtriranju visokih frekvenc tega signala. En parameter predstavlja planarizacijske last-nosti tekočega stekla pri tečenju, z drugim pa modeliramo gostoto prehodov /11/. Konkretne vrednosti parametrov dobimo po primerjavi merjenih rezultatov in rezultatov simulacij. S spreminjanjem vrednosti parametrov prilagajamo in izboljšujemo ujemanje napovedi modela z merilnimi rezultati.

2.3.2 Ocena uporabnosti modela

Pri tem modelu je bistveno prilagajanje parametrov modela na eksperimentalne podatke. Zaradi takega določanja parametrov je to empirični model, ki se lahko izkaže šele v razmerah, ko je na voljo veliko eksperimentalnih podatkov. V takem primeru je model primeren tudi za razvijanje novih postopkov. Model je uporabljen kot samostojen program, ki simulira postopek planarizacije in bi se ga verjetno dalo hitro vključiti v obstoječe programe, ki simulirajo tudi druge procesne korake. Po drugi strani pa model, ki temelji na prilagajanju parametrov, ni zanesljiv v vseh primerih. Če nek empirični model za procesni korak vključimo med modele za ostale procesne korake, med katerimi je še kakšen empiričen model, je izredno težko ugotoviti napovedi katerega modela se ne ujemajo z meritvami.

2.4 Prihodnost modelov procesa planarizacije

Primerjava vseh treh pristopov kaže, da so rezultati simulacij po vseh treh metodah uporabni, vendar ne brez zadržkov in omejitev. Trenutno ni modela, ki bi bil splošno uporaben za simuliranje vseh načinov planarizacije. Zaradi velikega zanimanja mikroelektronske industrije v zadnjem letu (1994) nastaja več modelov za kemo-mehansko poliranje. Modeli, ki temeljijo na fizikalnih osnovah kemo-mehanskega poliranja se bistveno razlikujejo od modelov za planarizacijo s tankimi plastmi tekočega stekla ali dopiranega silicijevega dioksida. Zaradi novega načina planarizacije, ki deluje na povsem drugih mehanizmih, se je področje za simulacije planarizacije razširilo in ostaja še naprej odprto.

Ta prispevek temelji na delu doktorske disertacije, ki jo je prvi avtor predložil Fakulteti za elektrotehniko in računalništvo v Ljubljani.

3. Literatura

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Prispelo (Arrived):10.07.95 *Sprejeto (Accepted): 29.08.95*

THERMALLY STIMULATED INTERACTIONS IN BILAYERS AND MULTILAYERS CONTAINING Ni AND Si DURING A TEMPERATURE RAMP

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Keywords: silicides, silicide layers, microelectronics applications, thin films, bilayers, multilayers, Ni layers, Si layers, layer interactions, thermally stimulated interactions, dependability of layers thickness ratio, bilayer structures, multilayer structures, constant rate heating, temperature ramps, electrical resistivity, electrical resistivity measurement, XRD, x-ray diffraction, Seeman-Bohlin x-ray diffraction, Bragg-Bretano x-ray diffraction, Rutherford backscattering, RBS, Rutheford Backscattering Spectra, Auger Electron Spectroscopy depth profiling, Ni-Si overall stoichiometry, interdiffusion phases, oxygen contamination

Abstract: Interactions between Ni and Si films in different types of bilayers and multilayers during constant heating rate of 3 °C/min in Ar or N as a function of starting Ni and Si thicknesses with overall stoichiometry ranging from $Ni_{0.78}Si_{0.22}$ to $Ni_{0.28}Si_{0.72}$ was systematically studied by in-situ electrical resistivity, x-ray diffraction, Rutherford backscattering and Auger depth profiling up to 500 °C. Two different phase sequences observed depend on initial Ni/Si thickness ratio. Diffusion in multilayers is detected above 150 °C. Additionally, bilayers contaminated with different oxygen contents during deposition were analyzed during heating. Several per cent of incorporated oxygen in either Ni or Si layer suppresses the interdiffusion strongly.

Toplotno vzpodbujene interakcije v dvoplastnih in večplastnih zgradbah, vsebujočih nikelj in silicij med enakomernim segrevanjem

Ključne besede: silicidi, plasti silicidne, uporaba v mikroelektroniki, plasti tanke, dvoplasti, večplasti, Ni plasti niklja, Si plasti silicija, vplivi med plastmi, interakcije toplotno vzpodbujene, odvisnost od razmerja debelih plasti, strukture dvoplastne, strukture večplastne, segrevanje enakomerno, klančine temperaturne, upornost električna, merjenje upornosti električne, XRD uklon Rentgen žarkov, Seeman-Bohlin XRD uklon Rentgen žarkov, Bragg-Brentano XRD uklon Rentgen žarkov, Rutherford sipanje povratno, RBS spekter Rutherford sipanja povratnega, AES Auger Spektroskopija elektronska - profiliranje globinsko, Ni-Si razmerje sestavin povprečno, faze difuzije medsebojne, kontaminacija s kisikom

Povzetek: S sprotnim merjenjem električne upornosti med segrevanjem s stalno hitrostjo 3°C/min do 500°C ter s kasnejšimi meritvami rentgenskega uklona, Rutherfordovega povratnega sipanja ter spektrov Augerjevih elektronov smo sistematično študirali mešanje plasti niklja in silicija v različnih dvoplastnih ter večplastnih zgradbah s povprečno sestavo med $Ni_{0.78}Si_{0.22}$ in $Ni_{0.28}Si_{0.72}$. Zaporedje nastajanja faz je odvisno od razmerja začetnih debelin obeh elementov. V večplasteh smo zaznali difuzijo že nad 150°C. Dodatno smo opazovali tudi dvoplasti z različno vsebnostjo kisika v posameznih plasteh. Nekaj odstotkov vgrajenega kisika v plasti močno omeji medsebojno difuzijo.

1. Introduction

Silicides have been a subject of research for many years. Their attractiveness has certainly been triggered by the characteristics of the metal/Si reaction, which have made the metal/Si diffusion couple a standard research subject for thin film reactions /1,2/. The sequence of the formation of phases from metal and silicon layers during heat treatment has only been established in a few silicide systems. Perhaps the most extensively studied of these is the Ni-Si system /3/. The potential microelectronics applications have widened the scope of research and have brought new characterization methods. Among other methods in-situ electrical resistivity measurement /4,5/ has been used to characterize interactions in Ni-Si system. However, these results have been obtained on two different structures only. In this paper we present a systematic analysis of reactions in different structures made of Ni and Si layers.

2. Experiment

Structures to be analyzed were deposited as 2.5 mm wide and 8 mm long strip onto polished (Ra = 25 nm) ceramic alumina substrates between two previously printed and annealed (at 850°C) thick film golden contacts which were bonded to the pads on a ceramic sample holder to enable the in-situ electrical resistivity measurement /6,7/. The sample was connected in series with a large resistor to the lock-in amplifier which measured the voltage drop on a film during heat treat-

Table 1: Description of the as deposited state of various types of films used in this study

sample type	Charge No.	No. of layers	d_A (nm)	d_B (nm)	A	B	overall stoichiometry	R_{RT} (Ohm)
A	1361	2	53	27	Ni	Si	$Ni_{0.78}Si_{0.22}$	14.8
B	1362	2	53	55	Ni	Si	$Ni_{0.64}Si_{0.36}$	14.2
C	1363	2	53	82	Ni	Si	$Ni_{0.54}Si_{0.46}$	12.6
D	1310	2	53	91	Ni	Si	$Ni_{0.52}Si_{0.48}$	14.4
E	1311	2	53	157	Ni	Si	$Ni_{0.38}Si_{0.62}$	15.2
F	1367	2	53	75	Ni	Si+O		14.3
G	1309	2	53	53	Ni	Si+O		17.2
H	1364	2	53	55	Ni	Si+O		15.1
I	1366	2	52	55	Ni+O	Si+O		68
J	1365	2	68	55	Ni+O	Si+O		560
K	1300	2	200	152	Ni	Si	$Ni_{0.71}Si_{0.29}$	4.1
L	1256	11	25	30	Ni	Si	$Ni_{0.56}Si_{0.44}$	4.9
M	1259	11	25	95	Ni	Si	$Ni_{0.28}Si_{0.72}$	5.1

ment. The resistivity of the film was typically four orders of magnitude lower than that of the resistor.

Silicon and nickel layers were sputtered in a RF mode at a power of 1000 W and in a DC mode at 1700 V / 0.6A, respectively, at the argon pressure of 0.2 Pa. During the deposition substrates were covered by masks to form strips of the measured film. In the as-deposited state transmission electron microscopy revealed that Si layers were amorphous and Ni layers were fine-grained polycrystalline with an average grain size of 20 nm.

As deposited samples were inserted into a tube furnace with argon or nitrogen gas flow at the atmospheric pressure. The temperature of the sample was monitored by a thermocouple levitating above it. The furnace was heated up at a constant rate of 3°C/min in all experiments and the resistivity was measured continuously in situ through the bonded contacts.

Measurements were done on various bilayers and multilayer samples with alternating Si and Ni layers of different thicknesses (Table 1). Some samples were contaminated with oxygen during deposition by inletting oxygen gas into the chamber.

Bilayers and multilayers of all groups were first heated at constant rate of 3°C/min while resistivity was continuously measured *in-situ*. After the determination of interesting temperatures, samples with the same structures deposited onto a silicon wafer with grown native oxide layer (Si monocrystal for easier X-ray spectral analysis and oxide layer to prevent from film-substrate interaction) were heated in the same way, but were taken out of the furnace at such temperature values to be later (*ex-situ*) analyzed by other techniques. On cooled samples X-ray diffraction (XRD) (Huber G600 diffractometer with Seemann-Bohlin (SB) geometry or Philips PW1710 diffractometer with Bragg-Brentano (BB) geometry), Rutherford backscattering spectro-metry (RBS) (Van de Graaff accelerator) and Auger electron spectroscopy (AES) sputter depth profiling (PHI 545A scanning Auger microprobe) were done to be compared with the results of the resistivity measurement. In x-ray diffraction of thin films classical Bragg-Brentano geometry (Read camera) /8/ is used for oriented samples with crystall planes parallel with the surface while Seemann-Bohlin geometry is best suited for randomly oriented polycrystalline samples.

3. Results and discussion

Results of the in-situ electrical resistivity measurement of bilayer types A, B, C, D, E and K during heating are presented in Figure 1.

It can be seen that in all those samples there is an influence of the temperature coefficient of a resistivity at low temperatures which is followed by an increase which is more pronounced for bilayers with thicker Si

layer. The behaviour at higher temperatures depends on Si content as well. In curves A and B and K the increase is temporarily interupted by a decrease, continues again and becomes saturated. In curves D and E with the highest Si/Ni thickness ratio the increase is followed by an even more abrupt drop which later saturates at lower values. The curve C represents an intermediate case.

Samples of groups A, B, C, D and E with the same Ni thickness of 53 nm exhibit almost the same resistivity behaviour at low temperatures in Figure 1. At 260°C their resistivity already deviates from a linear increase. Rutherford backscattering spectra (RBS) in Figure 2 reveals that this is due to the interaction between both layers as the right edge of Ni signal and the left edge of Si signal are changed at this temperature in comparison with the as-deposited state. During the exponential increase of the resistivity both Ni and Si layers are being consumed while new intermediate silicide layer is growing. The overall conductivity of the bilayer is mostly determined by parallel resistivities of Ni and silicide layers. The consumed nickel appears in the form of the silicide which exhibits larger specific electrical resistivity than the pure metal. Therefore the resistivity is increasing as the silicide layer is growing at the interface.

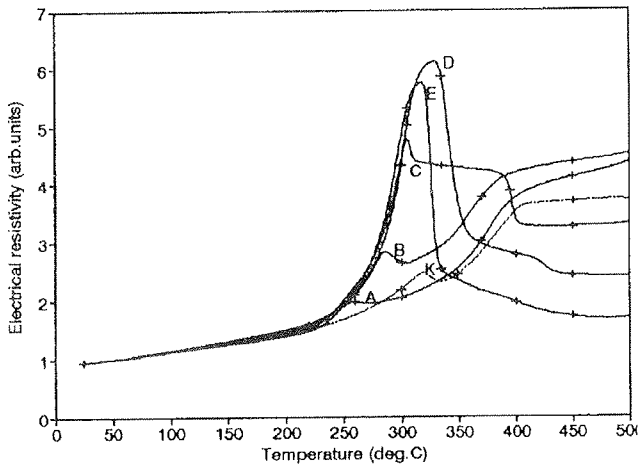

Figure 1: In-situ temperature dependence of electrical resistivity for bilayers with Ni and Si thicknesses of 53 nm/27 nm (A), 53 nm/55 nm (B), 53 nm/82 nm (C), 53 nm/91 nm (D), 53 nm/157 nm (E) and 200 nm/152 nm (K), respectively, heated up at 3°C/min in argon. Crosses mark temperatures to which XRD and RBS measurements correspond.

RBS of the sample A in Figure 2 shows that resistivity increase between 220 and 260°C can be attributed to the interdiffusion at the interface between both layers which consumes all Si layer below 260°C. This diffusion is then temporarily limited between 260 and 300°C where resistivity exhibits a peak, probably due to a crystallization of Ni_2Si like it will be later shown for sample B. Next Ni diffusion into the silicide is taking place which is becoming slower as the depth distribution of nickel is becoming more homogenous.

In the sample B thicker Si layer is consumed at higher temperature (below 300°C) than for the sample A as can be seen in Figure 2. The resistivity of the sample drops slightly and then rises again up to the saturated value. The drop corresponds to the crystallization of Ni_2Si as its peaks appear in the XRD spectrum at 300°C (Figure 3). According to RBS spectra crystallization of the newly-formed silicide can start only after the limitatation of the diffusion. The following resistivity rise is due to the diffusion of Ni into the silicide layer (and therefore Ni layer consumption). The ending silicide stoichiometry is defined by the starting content of both elements in a bilayer. XRD spectra indicate that between 370 and 450°C recrystallization is taking place yielding a mixture of Ni_2Si and $Ni_{31}Si_{12}$.

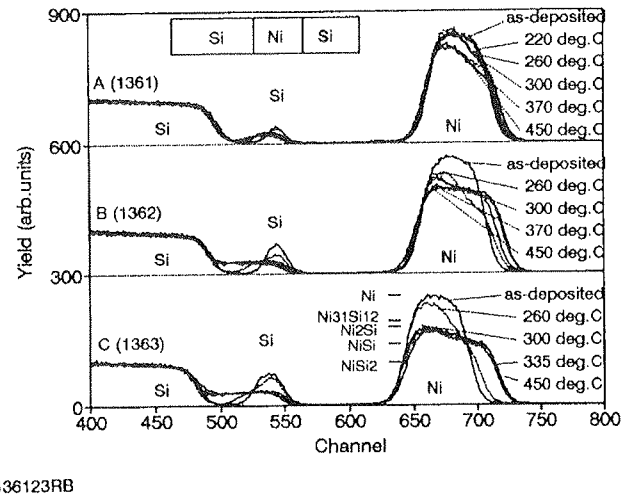

Figure 2: Ex-situ 1.45 MeV $^4He^+$ Rutherford backscattering spectra of samples A, B and C with Ni and Si thicknesses of 53 nm/27 nm, 53 nm/55 nm and 53 nm/82 nm, respectively, heated at 3°C/min. up to different temperatures in argon and then cooled rapidly. The signal of Ni layer appears at higher channels (ener-gies) than the signal of Si layer due to larger mass of Ni atoms in comparison with Si atoms although Ni layer is located below Si layer.

The sample C, exhibits strong initial increase. Here the difference between RBS spectra (Figure 2) obtained at room temperature, 260 and 300 °C is easy to notice. The intermixing in samples A, B and C is more rapid for thicker Si layers as Si atoms seem to diffuse more rapidly than do the Ni atoms. In X-ray diffraction spectrum of the sample C (Figure 4) at 300°C only broad and weak Ni peak is present which seems to get a neighbour of the growing Ni_2Si phase. Namely, at 335°C peaks of this new phase appears. Obviously resistivity detects

well the consumption of initial layers and the crystallization of Ni_2Si. Moreover, while RBS spectra remain almost constant above 335°C in Figure 2, the resistivity of the sample C in Figure 1 drops obviously around 395°C and this agrees well again with XRD spectra in Figure 4 where additional peak of the NiSi phase appears at 395°C which is more pronounced at 450°C.

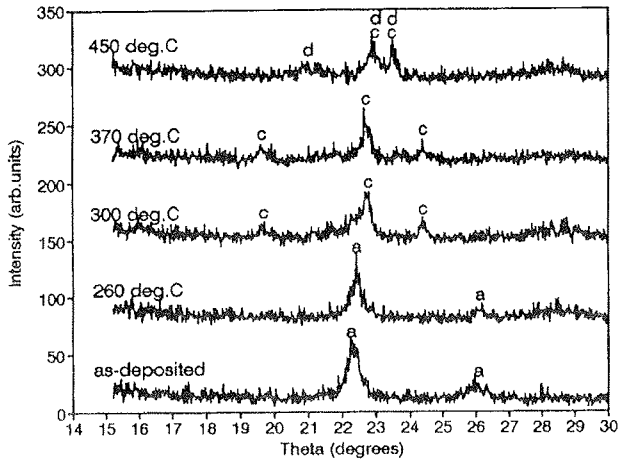

Figure 3: Ex-situ Seemann-Bohlin x-ray diffraction (XRD) spectra of the sample B (53 nm Ni/55 nm Si) after deposition and after heating at 3°C/min up to different temperatures and then cooled rapidly.

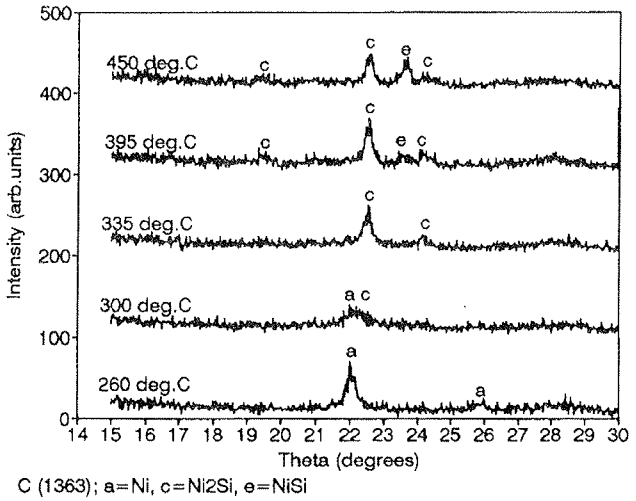

Figure 4: Ex-situ Seemann-Bohlin x-ray diffraction (XRD) spectra of the sample C (53 nm Ni/82 nm Si) after deposition and after heating at 3°C/min up to different temperatures and then cooled rapidly.

At this point it shall be explained that the sequence of the phases formed depends on the starting Ni/Si thickness ratio. The formation of nickel silicide between a film and a Si wafer exhibits a sequential growth of three phases: Ni_2Si, NiSi and $NiSi_2$ /9/. In a bilayer where Si layer is thinner than Ni layer Canali /10/ found different sequence: Ni_2Si, $Ni_{31}Si_{12}$ and Ni_3Si. Tu /11/ added this result to his results obtained on bilayers with thicker Si layer than Ni layer and suggested phase formation sequences for both cases: If Si layer is thinner than Ni layer Ni_2Si, $Ni_{31}Si_{12}$ and Ni_3Si will form sequentially. On the other hand if Si layer is thicker than Ni layer Ni_2Si, NiSi and $NiSi_2$ will appear with increasing temperature. It shall be noted here that references /10,11/ talk about Ni_5Si_2 as the existence of such phase was earlier reported by Saini /12/ and included with its characteristic peaks into reference x-ray diffraction pattern /13/. Later a correction of the stoichiometry to $Ni_{31}Si_{12}$ was included into this pattern /14/.

Samples D and E with high silicon content, like the sample C, exhibit strong initial resistivity increase. XRD spectra in Figures 5 and 6 show that the resistivity drop after the already explained increase (Figure 1) can again be correlated well with the crystallization of the NiSi phase as for the sample C. As can be seen in Figure 1 this process appears at lower temperatures for films with thicker initial Si films. It is interesting that peaks of both Ni_2Si and NiSi appear in the same temperature range between 305 and 335°C which differs from the sample C where peaks of only Ni_2Si appeared first and those of NiSi were added later. This may be caused by a Si diffusion which is rapid in comparison with sample A. However, RBS spectra of the sample E in Figure 7 reveal that after quite homogenous silicide layer with a stoichiometry close to NiSi is formed, the diffusion of remaining Si layer is limited. Evidently even temperature of 450°C is not high enough to enable the formation of homogenous layer with higher silicon content (e.g. $NiSi_2$).

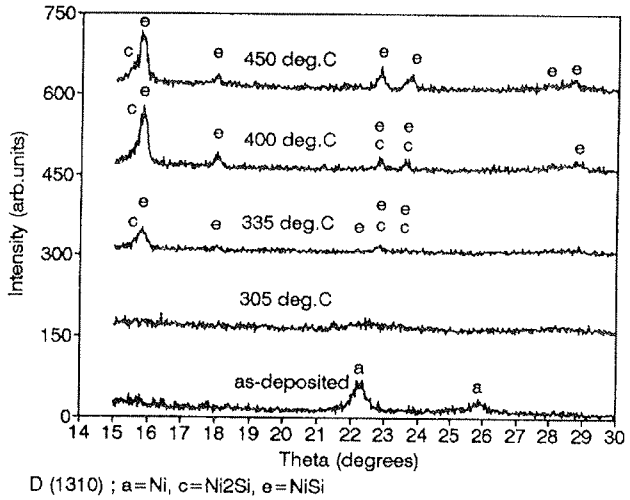

Figure 5: Ex-situ Seemann-Bohlin x-ray diffraction (XRD) spectra of the sample D (53 nm Ni/91 nm Si) after deposition and after heating at 3°C/min up to different temperatures and then cooled rapidly.

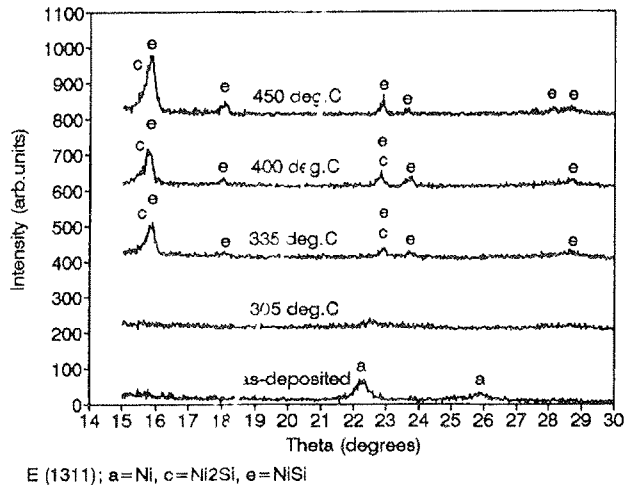

Figure 6: Ex-situ Seemann-Bohlin x-ray diffraction (XRD) spectra of the sample E (53 nm Ni/157 nm Si) after deposition and after heating at 3°C/min up to different temperatures and then cooled rapidly.

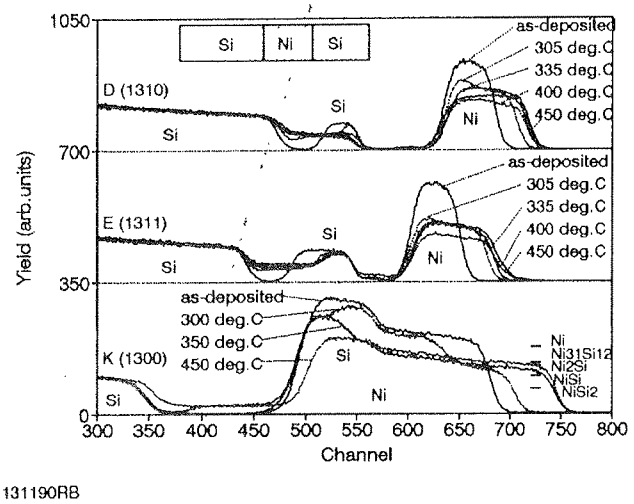

Figure 7: Ex-situ 1.45 MeV $^4He^+$ Rutherford backscattering spectra of samples D, E and K with Ni and Si thicknesses of 53nm/91nm, 53nm/157nm and 200nm/152nm, respectively, heated at 3°C/min. up to different temperatures in argon and then cooled rapidly.

Up to this point bilayers with the same thickness of Ni layer were presented. This was done to enable the comparison between different bilayers with various thicknesses of Si layer as initial resistivity is determined mostly by nickel. Now we shall examine the effect of thicker Ni layer in the sample K. Its resistivity dependence is similar to that of the sample B which possesses similar starting Ni/Si thickness ratio. The resistivity curve K in Figure 1 is shifted to higher temperatures as it can be expected that it takes more time for thicker layer of Ni to be consumed during temperature ramp. A comparison between XRD spectra in Figure 3 (sample B) and Figure 8 (sample K) shows that in both cases at temperatures below the resistivity peak traces of Ni are present only. Above the peak beside traces of remaining Ni other peaks are present as well. In the case of sample K beside Ni_2Si peaks, visible in spectra of sample B, signs of $Ni_{31}Si_{12}$ and NiSi are present, too. It is possible that last two phases are also present in thinner bilayer samples with similar thickness ratio, but their quantities may be below the detection limit for XRD which is about 20 nm /11,16/. Another possibility is that higher temperatures needed in thicker bilayers for one of the layers to be consumed have effect on a process of the crystallization of the silicide layer which is triggered by this consumption. A presence of Ni_2Si, $Ni_{31}Si_{12}$ and NiSi in the sample K heated up to 350°C was noticed in XRD spectrum obtained in Bragg-Brentano geometry as well.

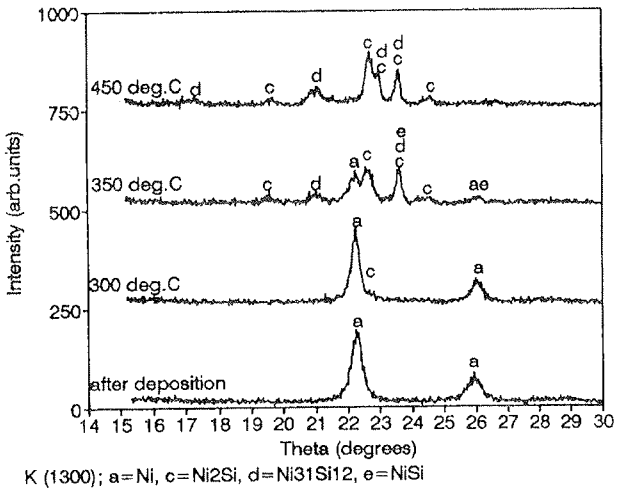

Figure 8: Ex-situ Seemann-Bohlin x-ray diffraction (XRD) spectra of the sample K (200 nm Ni/152 nm Si) after deposition and after heating at 3°C/min up to different tempera-tures and then cooled rapidly.

The sample K is thicker than other samples and signals from Ni and Si layers partially overlap in RBS spectra. At the same time larger thickness makes the observation of changes in depth profiles easier. At 300°C we can see that nickel atoms are detected at higher channels than after deposition - they are moving into the silicon layer, producing a step in a Ni signal which means that the growing silicide layer is rather homogenous. We analyzed RBS spectra by two different computer programs /17,18/ and found that the stoichiometry is between Ni_2Si and NiSi. At 350°C, after the resistivity peak, Ni atoms spread all the way to the surface of the film - all Si layer is consumed. Another evidence for this is smaller height of the right shoulder of Si signal. The second rise of the signal is due to remaining pure Ni layer near the substrate. The silicide layer exhibits stoichiometry close to Ni_3Si_2 which can be a mixture of Ni_2Si and NiSi as it was already observed in similar films /19/. If we heat the sample higher up to 450°C, Ni atoms

diffuse into the silicide and result in a homogenous film on a substrate. Its composition is defined by the starting overall composition of the bilayer. Nickel is not reacting with the substrate up to 450°C as can be seen from a non-moveable left edge of the Ni signal of other bilayer samples. The main reason for this comes from native oxide as oxides are known to limit interactions between films /20/.

To compare situation in samples A, B, C, D, E and K after heating at 3°C/min up to 450°C their x-ray diffraction spectra are presented in Figure 9. It can be clearly seen that situation depends on starting Ni/Si thickness ratio as well as on absolute values of thicknesses. For sample A nickel peak is the strongest and beside it small peaks of Ni_2Si and $Ni_{31}Si_{12}$ appear. If we increase the thickness of silicon, nickel peaks disappear and only peaks belonging to other two phases remain in sample B. Sample C possesses no traces of $Ni_{31}Si_{12}$. Instead, NiSi peak grows up beside peaks of Ni_2Si. If we increase Si content furter, peaks of NiSi become dominant. As Si layer is amorphous we do not detect it although there is some remaining Si layer in sample E. Situation in sample K is similar to the state of sample B except the number of phases detected is larger.

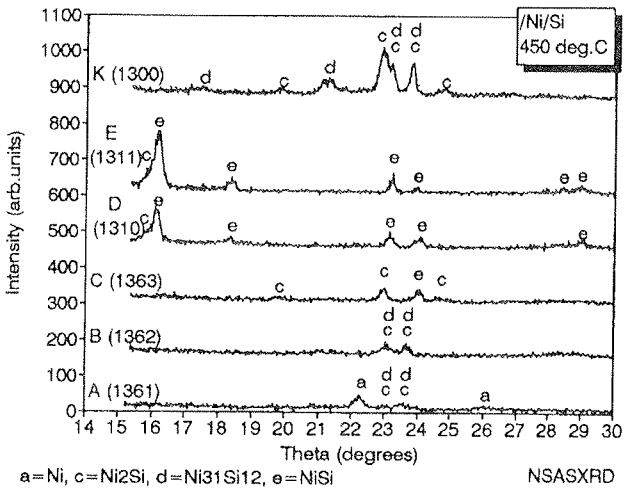

Figure 9: Ex-situ Seemann-Bohlin x-ray diffraction (XRD) spectra of bilayers with Ni and Si thicknesses of 53nm/27nm (A), 53 nm/55 nm (B), 53nm/82 nm (C), 53nm/ 91nm (D), 53nm/ 157nm (E) and 200nm/152nm (K), respectively, heated up to 450°C at 3°C/min in argon and then cooled rapidly.

As can be seen in Table 1 several samples were contaminated with oxygen during deposition to study its influence on interactions between nickel and silicon. Depth profiles of samples F, G, H, I and J are presented in Figure 10. As AES is not an absolute analytical method several standards would be needed to calibrate these measurements. Therefore, Auger peak-to-peak height is used for presentation which enables relative comparison of similar samples. We applied RBS method which is absolute, too. It is not best suited for light elements, but as an estimation it gives the stoichiometry of SiO_2 in oxidized Si layer of the sample F and $Ni_{0.8}O_{0.2}$ in oxidized Ni layer of the sample J.

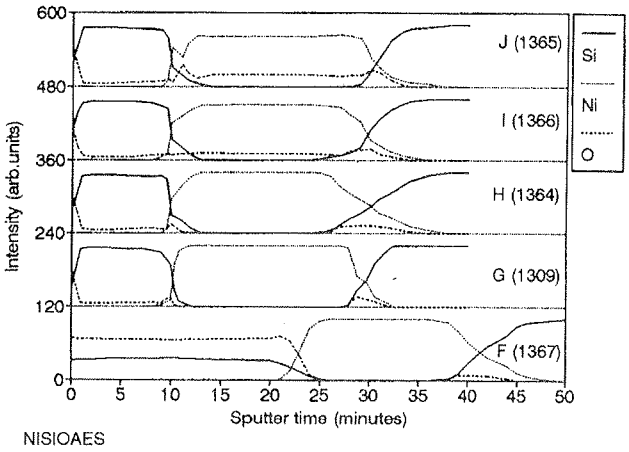

Figure 10: Auger electron spectroscopy (AES) depth profiles of as-deposited bilayer samples F, G, H, I and J, contaminated with oxygen during deposition.

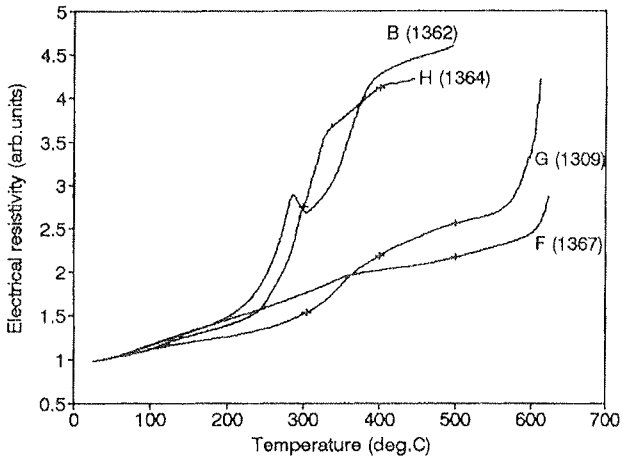

Figure 11: In-situ temperature dependence of electrical resistivity for bilayers without oxygen contamination (type B) and with oxygen included into Si layers (types F, G and H with decreasing oxygen content) heated up at 3°C/min in argon and then cooled rapidly. Crosses mark points to which RBS and XRD measurements correspond.

As can be expected /20/ oxygen limits interactions. In-situ dependence of resistivity for samples with contaminated Si layers is given in Figure 11. Resistivity dependence of sample B which was not intentionally contaminated is shown for reference. It can be seen

clearly that several per cent of incorporated oxygen can strongly limit interactions in sample G. In sample F, where SiO_2 was grown on Ni, we can see the Currie point of nickel at 260°C - resistivity dependence similar to one we get if nickel is deposited only. There is good correlation between resistivity measurements in Figure 11 and RBS spectra in Figure 12. The lesser the changes in resistivity the more constant RBS signal is. X-ray diffraction spectra of those samples in Figure 13 heated up to 400°C or more confirms observations of both techniques that the formation of new phases is strongly suppressed if oxygen is present.

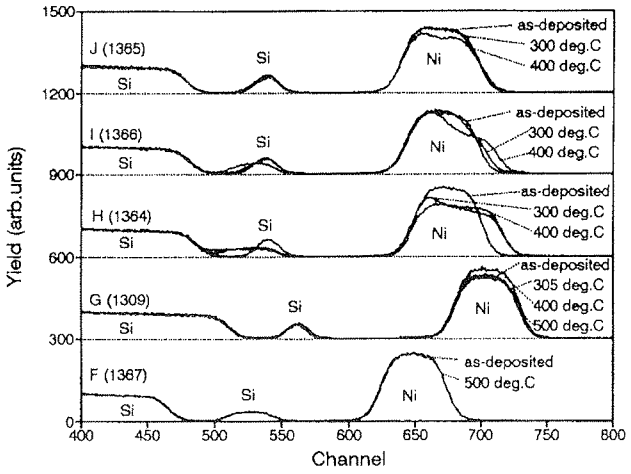

Figure 12: Ex-situ $^4He^+$ Rutherford backscattering spectra for bilayers without oxygen contamination (type B), with oxygen included into Si layers (types F, G and H with decreasing oxygen content) and with oxygen included into Ni layers (types I and J with increasing oxygen content) heated up to different temperatures at 3°C/min in argon and then cooled rapidly. The energy of the incoming ions was 1.45 MeV (F, H, I and J) and 1.5 MeV (G).

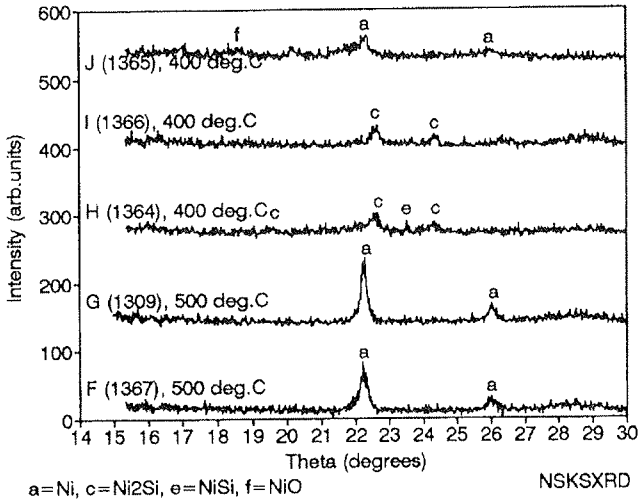

Figure 13: Ex-situ Seemann-Bohlin x-ray diffraction (XRD) spectra of bilayer samples F, G, H, I and J, contaminated with various amounts of oxygen during deposition, heated up to 400 or 500°C at 3°C/min in argon and then cooled rapidly.

If silicon layer is contaminated, mostly conducting nickel layer is unaffected. Resistivity measurements can be normalized with room temperature values and compared mutualy. On the other side if nickel layer is contaminated its resistivity can be increased by orders of magnitude. Therefore, in such samples absolute values of resistivity are to be compared as is presented in Figure 14. Their resistivity during heating alters and some changes can be seen in RBS spectra in figure 12 as well. Additionally, the state of samples I and J at 400°C is described by their XRD spectra in Figure 13.

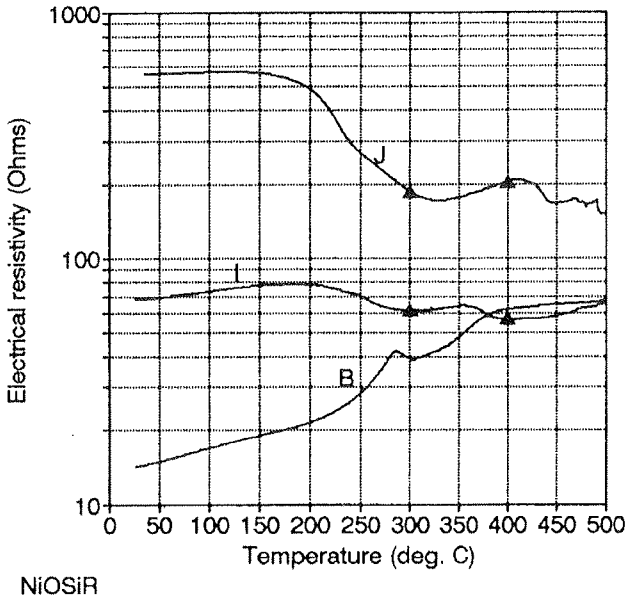

Figure 14: In-situ temperature dependence of electrical resistivity for bilayers without oxygen contamination (type B) and with oxygen included into Ni layers (types I and J with increasing oxygen content) heated up at 3°C/min in argon and then cooled rapidly. Triangles mark points to which RBS and XRD measurements correspond.

After the analysis of results on bilayers we shall focus on multilayer structures, containing 11 alternating layers of nickel and silicon. Multilayer samples from the group L have Si and Ni layer thicknesses of 30 and 25 nm, respectively. Group M possesses Si and Ni layer thicknesses of 95 and 25 nm, respectively. Taking into account the different volume density of atoms of the two elements, the Si/Ni ratio of the total number of atoms in a multilayer was 0.8 and 2.1 for group A and B, respectively. Obtained resistivity dependencies on temperature, along with results for bilayers C and E possessing similar overall stoichiometries, are shown in Figure 15.

Crosses again mark points to which x-ray diffraction spectra for the group L and M in Figure 16 and Figure 17, respectively, correspond.

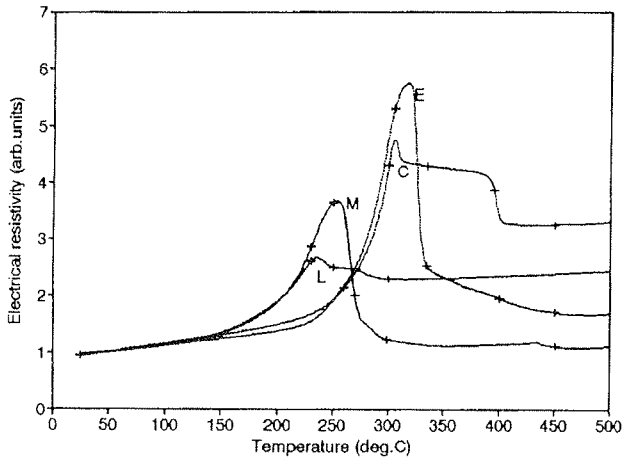

Figure 15: In-situ temperature dependence of electrical resistivity for bilayers with Ni and Si thicknesses of 53 nm/82 nm (C) and 53 nm/ 157 nm (E) and for multilayers (11 alternating layers) with Ni and Si individual layer thicknesses of 25 nm/30 nm (L) and 25 nm/95 nm (M), respectively, heated up at 3°C/min in argon. Crosses mark tempera-tures to which XRD and RBS measurements correspond.

As in bilayers temperatures of similar resistivity change were lower for the sample B than for the sample K, in multilayers composed of even thinner layers these temperatures are lower than for bilayers. The curves for bilayers and multilayers are, however, similar.This can be seen in figure 15. The expectance that similar resistivity behaviour describes processes like those in bilayers is confirmed by x-ray diffraction in Figure 16, where for the sample L the crystallization of Ni_2Si phase above resistivity peak was detected. After their appearance, at higher temperatures these peaks are shifting toward higher angles - the crystals are ordering and unit cells are becoming smaller. In sample M peaks of Ni_2Si are detected in the diffraction spectrum at the resistivity peak (Figure 17) and the following resistivity drop is connected with the appearance of crystalline NiSi beside still existing Ni_2Si. Finally, at 450°C NiSi phase is detected only by x-ray diffraction. In general for multilayer sample M reactions are similar to those in bilayer sample E. There are, however, differences in details. XRD spectra for bilayers in Bragg-Brentano geometry yield up to four times higher signals than in Seemann-Bohlin geometry while in multilayers the ratio of even 100 was noticed. This indicates that the crystallization in multilayers yields more oriented structures than in bilayers. Another difference is that in diffraction spectrum of multilayer M peaks of Ni_2Si are much more obvious than in bilayer E (and peaks of NiSi much less dominant) although the silicon content in the multilayer is higher than in the bilayer. RBS measurements in Figure 18 reveal that multilayer structure in sample L is ruined at 250°C yielding a homogenous depth profile. On the other hand, in multilayer M the alternating structure is affected but still visible even at 450°C. The reason for this may be similar as in bilayer E, where the intermixing is limited after a stoichiometry close to NiSi is obtained in a newly formed silicide layer.

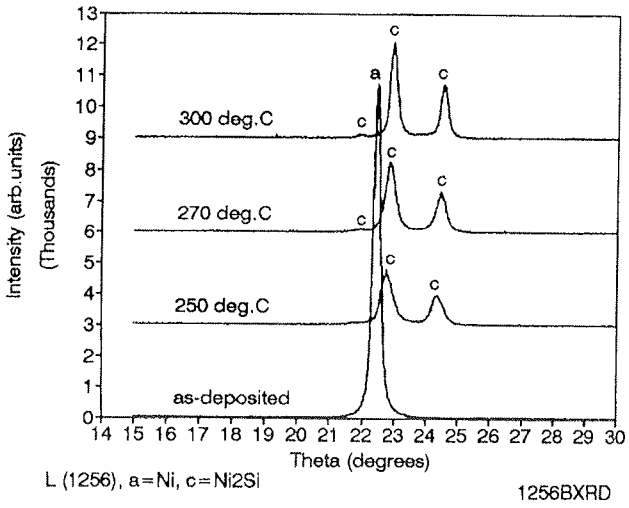

Figure 16: Ex-situ Bragg-Brentano x-ray diffraction (XRD) spectra of the sample L (11 alternating layers; 25 nm Ni, 30 nm Si) after deposition and after heating at 3°C/min up to different temperatures and then cooled rapidly.

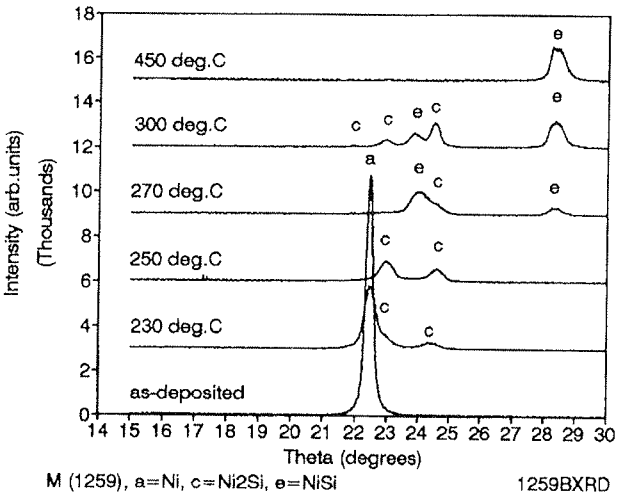

Figure 17: Ex-situ Bragg-Brentano x-ray diffraction (XRD) spectra of the sample M (11 alternating layers; 25 nm Ni, 95 nm Si) after deposition and after heating at 3°C/min up to different temperatures and then cooled rapidly.

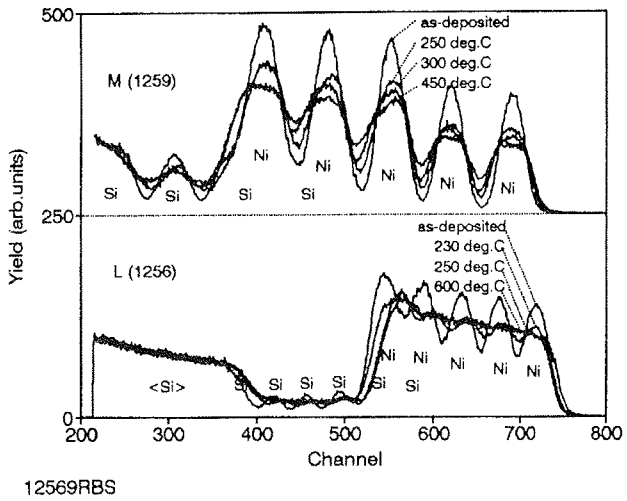

Figure 18: Ex-situ 1.5 MeV $^4He^+$ Rutherford backscattering spectra of multilayers (11 alternating layers) with Ni and Si individual layer thicknesses of 25 nm/30 nm (L) and 25nm/95nm (M), respectively, heated up at 3°C/min in argon.

4. Conclusions

We analyzed interaction between Ni and Si layers in bilayers and multilayers with various Ni/Si thicknnesses ratios on a basis of in-situ electrical resistivity measurements during dynamic heating of the sample. Results of resistivity curves prooved to be efficient starting points for straightforward use of other analytical methods as x-ray diffraction, Rutherford backscattering and Auger electron depth profiling and observations of all methods were well correlated. Temperatures at which phases occur after the intermixing of both elements depend on properties of measured structure.

In literature in the case of Ni on Si wafer Ni_2Si, NiSi and $NiSi_2$ were observed after an isothermal anneal at 280, 350 and 750 °C, respectively /11/. In bilayers with thinner Si layer Ni_2Si, $Ni_{31}Si_{12}$ and Ni_3Si were detected after similar heating at 280, 400 and 450 °C /10/. Several authors noticed Ni_2Si at 200 °C and $NiSi_2$ was found on amorphous silicon at 400°C /15/.

In our bilayers peaks of Ni_2Si were found in the sample B at 300°C, but according to RBS and resistivity measurements it is present already at 260°C. Additionaly it shall be noted that in multilayers with thinner layers resistivity exhibited changes about 50°C lower and similar temperature difference was found in XRD spectra as well. Presence of $Ni_{31}Si_{12}$ was noticed at 450°C in thinner bilayer B) and at 350°C in thicker bilayer (K). The formation temperature for NiSi in our bilayers depended on starting Ni/Si thickness ratio and varied between 335 and 395°C. In multilayers this temperature was again 50°C lower than the lowest temperature for bilayers. For temperatures up to 450°C $NiSi_2$ was firmly detected neither in bilayers nor in multilayers.

The incorporation of several atomic per cent of oxygen atoms into silicon or nickel layer suppresses the diffusion strongly. For lower oxygen contents Ni_2Si is present at 400°C, while for higher contents almost no changes are visible in x-ray diffraction and Rutherford backscattering spectra.

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Prispelo (Arrived): 03.10.95 *Sprejeto (Accepted): 17.10.95*

UDK621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 25(1995)3, Ljubljana

DEBELOPLASTNI KEMIJSKI SENZORJI

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Ključne besede: senzorji kemijski, senzorji polprevodniški, senzorji debeloplastni, senzorji iz materialov trdnih, senzorji elektrokemijski, elektroliti trdni, merjenje koncentracije plinov, merjenje koncentracije alkoholov, prevodnost ionska, merjenje koncentracije ionov v raztopinah, prevodnost električna, senzorji galvanski, senzorji amperometrični, SnO_2 senzorji, senzorji vlažnosti, senzorji vodika, SO_2 senzorji, CO_2 senzorji, Na+ion senzorji, senzorji ogljikovodikov

Povzetek: V prispevku je podan literaturni pregled nekaterih debeloplastnih kemijskih senzorjev. Opisani so principi delovanja, materiali in karakteristike kemijskih senzorjev.

Thick Film Chemical Sensors

Keywords: chemical sensors, semiconductor sensors, thick film sensors, solid state sensors, electrochemical sensors, solid electrolytes, gas concentration measurement, alcohol concentration measurement, ionic conductivity, ion concentration measurement in solutions, electric conductance, galvanic sensors, amperometric sensors, SnO_2 sensors, humidity sensors, hydrogen sensors, SO_2 sensors, CO_2 sensors, Na+ion sensors, hydrocarbon sensors

Abstract: This paper reviews the area of thick film solid state chemical sensors based on semiconducting and solid electrolyte materials. Research and development of chemical sensors are characterised by large gap between new ideas, materials and protopyes on one hand and limited number of practically reliased sensors which are manufactured in large quantity. Typical examples for commonly used chemical sensors are Lambda probe based on solid electrolyte to detect oxygen in the car exhaust and SnO_2 sensor based on conductance measurements to detect reducible gas in warning system.

Solid state chemical sensors are mainly divided in to two groups: semiconducting and electrochemical. First type of sensors are manufactured from following materials: SnO_2, ZnO, TiO_2, Nb_2O_5, $SrTiO_3$ etc. These metal oxide semiconductor based sensors can detect various gases by using conductivity changes due to absorption or desorbtion of gases. Electromotive force (EMF) from electrochemical galvanic type sensors is related to electrode reactions which involve gaseous species to be measured.

Chemical sensors may also be produced in thick film technology for producing hybrid circuits. Also, for some applications it provides a relatively inexpensive and convenient way to produce chemical sensors which can be integrated in to hybrid circuits. Starting materials for chemically sensitive layers are prepared from powders and organic vehicle. They are printed onto alumina substrate together with electrodes.

The principles, materials and performance of thick film SnO_2, humidity, hydrogen, carbon and sulfur dioxide, hydrocarbons and some other sensors are covered in this paper.

1. UVOD

Princip delovanja senzorjev je spreminjanje transportnih parametrov v senzorskem materialu, ko so ti izpostavljeni termičnim, radiacijskim, mehanskim, električnim, magnetnim ali kemjiskim spremembam. Kemijski senzorji postajajo vse pomembnejši pri kontroli kemijskih procesov, meritvah onesnaženja kot tudi v vsakodnevnem življenju. Kemijski senzorji merijo koncentracijo plinov v zmeseh, kot npr: O_2, CO_2, CO, H_2O, H_2, NH_3, NO, NO_2, H_2S, AsH_3, PH_3, alkoholov, aminov, ogljikovodikov itd. Uporabljajo se tudi za merjenje koncentracij ionov v raztopinah kot naprimer: H^+, Cu^+, Ag^+, NO_3^- itd.

Osnovno vprašanje, ki nastane ob odkritju novega materiala za kemijski senzor je, ali ta reagira tudi na spremembe drugih sestavin, ki so prisotne v mernem sistemu. Lep zgled za to je SnO_2 senzor. Reagira namreč na veliko večino reducirajočih plinov. Težava pa je, kako izdelati tak senzor in določiti pogoje njegovega delovanja, ki bo reagiral le na spremembe koncentracije določenega plina.

Kemijske senzorje, izdelane iz trdnih materialov (ang. solid state sensors) razdelimo v dve skupini: polprevodniške in elektrokemijske. Prvi so izdelani iz teh-le materialov: SnO_2, ZnO, TiO_2, Nb_2O_3, WO_3, $SrTiO_3$. Pod vplivom kemijskih sestavin se tem materialom spremeni električna prevodnost. Bistveni del elektrokemijskih senzorjev je ionsko prevoden trdni elektrolit. Elektrokemijske senzorje delimo še na galvanske in amperometrične. Pri galvanskem tipu je napetost oz. gonilna sila proporcionalna razliki koncentracije merjene komponente na obeh straneh elektrolita. V primeru amperometričnega senzorja pa na elektro-kemijsko celico priključimo električno napetost in merimo tok skozi trdni elektrolit. Mejni tok skozenj je proporcionalen koncentraciji merjene komponete.

Za izdelavo senzorjev se uporabljajo različne tehnologije. Razvoj je usmerjen v debeloplastne in tankoplastne tehnologije, kajti če je senzorski material tanek hitreje reagira na spremebe koncentaciji merne sestavine. Te tehnologije obenem omogočajo integracijo senzorja z merno elektroniko. Senzor prihodnosti bo integriran z elektroniko v taki meri, da ga bo mogoče priključiti

direktno na računalnik. Debeloplastna tehnologija izdelave kemijskih senzorjev je v primerjavi z tankoplastnimi tehnologijami preprostejša in cenejša. V debeloplastni tehnologiji je možno izdelovati tako majhne prototipne serije kot velike serije. Pri izdelavi kemijskih senzorjev je bistveno tudi to, da je možno zelo hitro izdelati pasto novega ali spremenjenega materiala jo natisniti in preiskusiti, kar pa ne velja za druge tehnologije.

Kemijske senzorje bi lahko ločili na dve veliki skupini:

- senzorje, ki se uporabljajo za določitev primarnih komponent neke zmesi, kot na primer vsebnost kisika, CO_2, vlage ipd. v zraku, kjer so koncentracije komponent kot tudi koncentracijsko območje, ki jih mora zaznati senzor, dokaj velike. Na primer senzor kisika v avtomobilu deluje v območju 21% in nekaj ppm.
- senzorje, ki merijo sledi prisotnih komponent (CO, ogljikovodiki, klor, fosfin, amonijak itd).

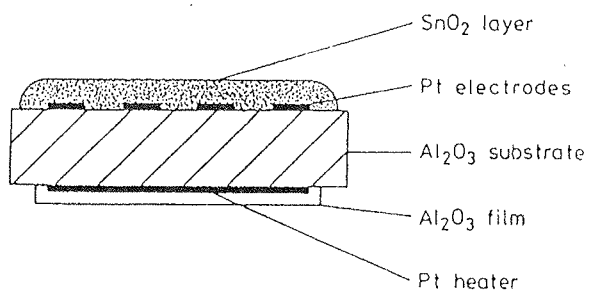
Namen prispevka je na kratko opisati nekatere kemijske senzorje, ki se jih lahko izdela v debeloplastni tehnologiji.

2. PRIMERI DEBELOPLASTNIH KEMIJSKIH SENZORJEV

2.1. SnO_2 senzor

SnO_2 senzor je v zadnjih parih desetletjih najpogosteje omenjen, raziskovan in uporabljen kemijski senzor. Detektira razne pline (ogljikovodiki, vodik, alkoholi, cigaretni dim, metan, dušikovi oksidi, arzin, fosfin itd). Kaj detektira, je odvisno od dodatkov in temperature delovanja /1/. Najpogostejša uporaba SnO_2 senzorjev je za plinske alarme v industriji in gospodinjstvih.

Za izdelavo se uporabljajo prav vse znane tehnologije med drugim tudi debeloplastna tehnologija. Pasta iz SnO_2 in dodatkov se natisne na korundni substrat in žge pri določenih pogojih /2/. Sintrane plasti so debele približno 20 μm. Za izdelavo finih prahov SnO_2 se zadnje čase precej uporabljajo plazemske metode /3/. Prah, pridobljen po teh metodah, ima nanometrske delce, ki se sintrajo v obliki paste že pri 500 °C. Na nasprotno stran senzorja oz korundne ploščice se natisne še grelnik, ki segreva senzor na določeno temperaturo. Prerez skozi SnO_2 debeloplastni senzor je na sliki 1. V primerjavi z SnO_2 senzorji, izdelanimi v tankoplastni tehnologiji, ima debeloplastni slabšo selektivnost ter večjo občutljivost na spremembe temperature in relativne vlažnosti, je pa zato cenejši /1/.



Slika 1: Debeloplastni SnO_2 senzor /8/

2.2 Senzor vlage

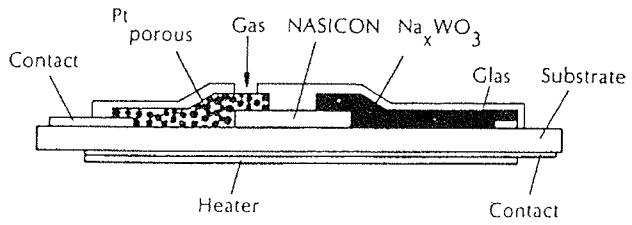
Tudi senzorji vlage spadajo med kemijske senzorje in se uporabljajo v klimatskih napravah, rastlinjakih, v procesih sušenja, raznih napravah itd. Na primer, vsak videorekorder je opremljen s senzorjem vlage, ki prepreči vklop naprave, ko je vlažnost blizu rosišča, saj bi kapljice vode lahko poškodovale magnetni trak in odjemno glavo.

Navadno senzorji vlage merijo relativno vlažnost, to je razmerje med delnim in nasičenim parnim tlakom vodne pare pri določeni temperaturi. Signal iz senzorja je proporcionalen relativni vlažnosti in ga podajamo v procentih R.H. (relative humidity - relativna vlažnost). Za izdelavo senzorjev vlage uporabljamo različne materiale, npr. polimerne materiale, Al_2O_3, LiCl, $MgCr_2O_4$, TiO_2 - V_2O_3, $(Ba,Sr)TiO_3$ itd. /4/. Skoraj večina do sedaj razvitih senzorjev vlage je izdelanih iz polimernih materialov. Manj znana je generacija keramičnih senzorjev vlage. Dobri naj bi imeli tele lastnosti: veliko občutljivost, reverzibilnost, hiter odzivni čas, dolgo življenjsko dobo, selektivnost ter kemijsko in termično stabilnost. Tem pogojem v večini primerov zadostijo keramični senzorji vlage. To so porozni keramični materiali, katerim se zaradi adsorpcije vodne pare na površini spreminja električna prevodnost ali dielektričnost. V večini primerov se za izdelavo senzorjev vlage uporablja debeloplastna tehnologija. Na interdigitalne elektrode se natisne senzorska plast in žge tako, da ostane po žganju porozna. Ker lahko pri večji relativni vlažnosti ali onesnaženi atmosferi pride do ireverzibilnih sprememb v porozni senzorski plasti, imajo keramični senzorji vdelan še grelnik, ki občasno segreje senzor na okoli 400 do 600°C. Na ta način se odstranijo hlapne nečistoče (olja, saje, težkohlapne organske spojine itd.).

Z raziskavami keramičnih debeloplastnih senzorjev se ukvarjamo tudi na Odseku za keramiko na Institutu "Jožef Stefan". Potekajo v več smeri: sinteza novih materialov, priprava poroznih keramičnih struktur po sol gel postopku, študij interakciji med substratom, senzorsko plastjo in elektrodnim materialom med procesom priprave ter procesi staranja keramičnih senzorjev vlage.

2.3 Senzor vodika

Podobno kot za kisik je tudi senzor vodika elektrokemijska celica s trdnim elektrolitom. Napetost galvanskega člena je odvisna od reakcij na elektrodah. Kot trdni elektrolit se uporabljata naslednja protonska prevodnika: NASICON ($Na_3Zr_2Si_2PO_{12}$) /5/ ali $BaCeO_3$ /6/. Vse komponete senzorja (trdni elektrolit, referenčna elektroda in kontakti) so narejeni v debeloplastni tehnologiji. Shematično je senzor vodika predstavljen na sliki 2. Temperatura delovanja takega senzorja je okoli 200°C, zato je na drugi strani podloge natisnjen grelnik. Senzor je uporaben za merjenje koncentracij vodika v območju od 100 ppm do 100%.

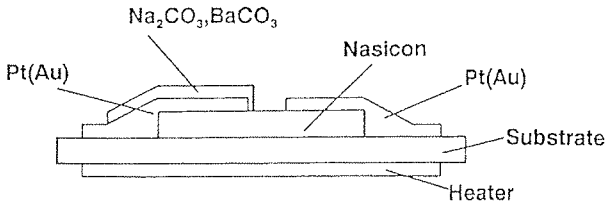


Slika 2: Debeloplastni senzor vodika. Merni plin prihaja skozi porozno platino /5/.

Senzor se uporablja v industriji za detekcijo vodika v raznih plinskih zmeseh.

2.4 Senzorji CO_2 in SO_2

Senzorja za CO_2 in SO_2 sta galvanskega tipa in imata kot trdni elektrolit NASICON oz. beta aluminijev oksid za CO_2 senzor /7/ . Merilni elektrodi sta Na_2CO_3 oz. Na_2SO_4. Ker sta oba trdna elektrolita ionska prevodnika Na^+, poteče na anodi razpad natrijevega karbonata ali sulfata. Na^+ migrira skozi trdni elektrolit in doseže katodo, kjer se vzpostavi ravnotežje. Podobno se dogaja v senzorju SO_2, samo da v ravnotežju sodeluje Na_2SO_4. Če je v mernem plinu prisotna voda, senzor ne deluje pravilno. Drugi problem pa je počasno izpare-vanje Na_2CO_3 oz. Na_2SO_4 z anodne strani na katodno stran pri temperaturi delovanja senzorja, to je od 400 do 600°C. Ta pojav povzroča senzorju lezenje. Shematsko je senzor prikazan na sliki 3. Senzor CO_2 se uporablja v skladiščih, rastlinjakih in fermentorjih, senzor SO_2 pa za kontrolo dimnih plinov iz kurišč in izpuhov.

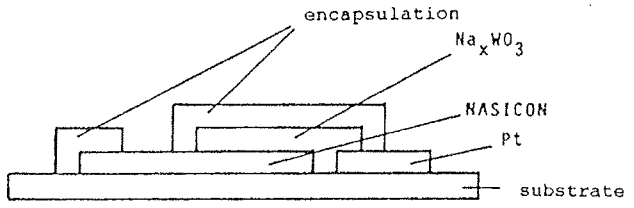


Slika 3: Debeloplastni senzor CO_2 /7/.

2.5. Senzor Na^+ ionov

Kot primer senzorja, ki deluje v raztopinah, bi omenil senzor Na^+. Ta senzor in še več podobnih senzorjev se uporablja v industriji, zdravstvu, kmetijstvu itd. za kontrolo vsebnosti ionov v raztopinah.

Že omenjeni trdni elektrolit NASICON /5/ je bil razvit za uporabo v Na/S baterijah kot dober prevodnik Na^+ ionov. Zato je uporaben tudi za izdelavo Na^+ senzorja /9/. NASICON je natisnjen na korundni substrat, nanj pa še referenčna elektroda iz $Na_{0.7}WO_3$. Ta je zaščitena še

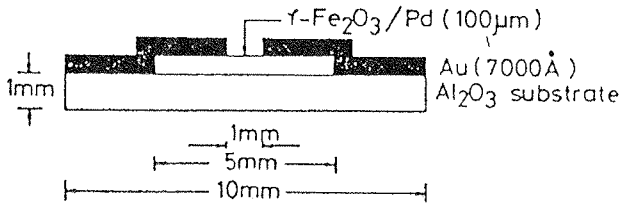


Slika 4: Debeloplastni senzor Na^+ ionov. Raztopina pride v stik z NASICON trdnim elektrolitom /9/.

s stekleno pasto. Shematsko je senzor prikazan na sliki 4. Senzor je uporaben za merjenje koncentracije Na^+ ionov v vodnih raztopinah pri 25°C v koncentracijskem območju od 1 do 10^{-2} mol/l.

2.6. Senzor ogljikovodikov

Za detekcijo ogljikovodikov se uporabljajo polprevodni kovinski oksidi, katerih prevodnost se spreminja med absorpcijo in desorpcijo ogljikovodikov. Uporabljajo se sledeči kovinski oksidi: ZnO, SnO_2 in Fe_2O_3 /10/. Ti senzorji so namenjeni detekciji ogljikovodikov, ki so prisotni v zemeljskem plinu in plinu v jeklenkah, ki se uporabljajo za ogrevanje in kuhanje v gospodinjstvih. Zadnje čase se vedno pogosteje za te namene uporablja Fe_2O_3, ki je občutljiv na propan in butan in nekaj manj na metan, vendar je ravno detekcija metana izredno pomembna v primeru uporabe zemeljskega plina. Zato dodajajo Fe_2O_3 dodatke, ki izboljšajo občutljivost na metan. Pomembno je, da senzor zazna že količine reda velikosti nekaj deset ppm. Senzor se v debeloplastni tehniki izdela v obliki upora, tipični Fe_2O_3 senzor ogljikovodikov je prikazan na sliki 5.



Slika 5: Debeloplastni senzor ogljikovodikov /11/. Plin prihaja v stik z Fe_2O_3 med dvema elektrodama.

2.7. Ostali senzorji

V tabeli 1 so navedeni nekateri polprevodni materiali, ki se uporabljajo za izdelavo kemijskih senzorjev za detekcijo nečistoč v plinih. Vsi materiali so polprevodnega tipa in se jim v prisotnosti nečistoč spremeni električna upornost.

Tabela 1: Primeri materialov, ki se raziskujejo ali uporabljajo za kemijske senzorje nečistoč v plinih /12/

Material	p ali n tip prevodnika	Temperatura delovanja (°C)	Nečistoča
ZnO	n	450	freoni
WO_3 (Pt)	n	250 do 400	NH_3, H_2S
TiO_2 (Ru)	n	560	trimetil amin
$BaTiO_3$	n	300	CO
$BaSnO_3$	n	300 do 500	H_2, CO, CH_4, SO_2
$SrFeO_3$	p	470	CH_4
Cr_2-y$TiyO_3$	p ali n	250-500	H_2S /13/

3. SKLEP

V prispevku so opisani nekateri kemijski senzorji, ki jih je možno izdelati v debeloplastni tehnologiji. Pomebni so predvsem zato, ker so preprosti in jih je lahko z odgovarjajočo elektroniko vklopiti v merilne in regulacijske sisteme. Tudi na IJS, v Odseku za keramiko, se ukvarjamo z raziskavami na področju senzorjev, in sicer TiO_2 in (Ba,Sr)TiO_3 senzorji vlage. Naše delo je osredotočeno na uporabo debeloplastne tehnologije izdelave ter na preiskavo reakcij, ki potekajo med pripravo in izdelavo posameznih senzorskih elementov.

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Prispelo (Arrived): 03.10.95 *Sprejeto (Accepted): 19.10.95*

REPLACEMENT OF CFC SOLVENTS BY NEW "NO CLEAN" FLUXES OR NEW SOLVENTS FOR ELECTRONIC CIRCUIT CLEANING AFTER SOLDERING

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Keywords: printed circuits, circuits manufacturing, surface cleaning, cleaning after soldering, electronic circuits, organic solvents, CFC, Chlorofluorocarbon solvents, "no clean" fluxes, CFC-113, trichlorotrifluoroethane, thick film technologies, ionic contamination, ionic conductivity, ionic conductivity measurement, insulation resistance, functional reliability, humid environment, Montreal protocol, no-residue fluxes, flux residue removal, rosin fluxes, water soluble fluxes, synthetically activated fluxes, no clean soldering, aqueous cleaning, water cleaning, semiaqueous cleaning, solvent testing, solder pastes

Abstract: Some "no clean" fluxes and solder pastes containing residueless fluxes were tested by ionic contamination measurements on circuits after soldering. The influence of ionic contamination on the reliability of circuit functioning was measured by insulation resistance measurements in humid conditions. The same measurements were used to evaluate some new organic solvents for possible substitution of trichlorotrifluoroethane (CFC) solvents in the cleaning of electronic circuits after soldering.

Zamenjava CFC topil z novimi fluksi "brez ostankov" ali pa z novimi topili za čiščenje elektronskih vezij po spajkanju

Ključne besede: vezja tiskana, proizvodnja vezij, čiščenje površin, čiščenje po spajkanju, vezja elektronska, topila organska, CFC topila klorofluoroogljikova, fluksi čistilni "nečisti", CFC-113 triklortrifluoretan, tehnologije debeloplastne, kontaminacija ionska, prevodnost ionska, zanesljivost delovanja, okolje vlažno, Montreal protokol, fluksi brez ostankov, odstranjevanje ostankov fluksov, kolofonija fluksi, fluksi vodotopni, fluksi sintetično aktivirani, spajkanje brez čiščenja, čiščenje vodno, čiščenje polvodno, preskušanje topil, paste spajkalne

Povzetek: Preizkusili smo nekatere flukse "brez ostankov" in pastozne spajke s fluksi "brez ostankov" s pomočjo meritve ionskih ostankov na vezjih po spajkanju. Vpliv ionskih nečistoč na zanesljivost vezij smo ugotovili s pomočjo meritve izolacijske upornosti v vlažni atmosferi. Enake meritve smo uporabili za ovrednotenje nekaterih novih topli kot možne zamenjave za triklortrifluoretan (CFC) v postopku čiščenja elektronskih vezij po spajkanju.

INTRODUCTION

According to theMontreal Protocol the use of CFC-113 (trichlorotrifluoroethane) and 1,1,1 trichloroethane is to be reduced and phased out completely by the year 2000 /1,2/. Possible alternatives for replacing CFC solvents used for electronic circuit cleaning after soldering include new fluxes which do not need to be cleaned, or the choice of solvents other than CFC. Dependent on the type of fluxes used for circuit cleaning (rosin flux, water soluble, synthetically activated fluxes) suitable cleaning must be applied for flux residue removal. New fluxes, the so called "no residue" fluxes with very low solid content ($\leq$5%), have been developed which do not require cleaning, or when necessary it is possible to clean with organic solvents other than CFC. When rosin based fluxes are used for ciruit soldering, new organic solvents other than trichlorotrifluoroethane must be chosen.

The attention of industry has been focused on four primary strategies for removing CFCs from use: HCFC as replacements for CFC, semiaqueous and aqueous cleaning and no-clean soldering. These are becoming available at increasingly attractive prices. When selecting a possible solution for circuit cleaning many aspects must be taken into consideration; material compatibility, energy consumption and also the selection of solvents, which are usually in the form of a mixture. Terpenes, water and other solvents are mixed with varying amounts of surfactants, detergents, saponifiers or other agents to maximize performance in specific applications.

In our work we have tested two solvents other than CFC for circuit cleaning after soldering, and which were selected on the basis of previous work on solvent testing /3,5,6/. Also five "no residue" fluxes were tested for circuit soldering without cleaning in comparision with

RMA flux, as well as two solder pastes containing "no residue" flux.

EXPERIMENTAL

Ionic residues after the soldering of circuits were determined by ionic conductivity measurements of the solvent containing dissolved contaminants, and by insulation resistance measurements on the test sample between closely spaced soldered conductors in humid conditions /3/.

The main characteristics of the fluxes and solder pastes tested are presented in Table I and Table II. The characteristic of RMA fluxes normally used for circuits soldering are also given in Table I for comparision. The characteristics of the new solvents A and B compared to Freon (CFC) are given in Table III.

Table I: Main characteristics of fluxes used for immersion or wave soldering

Flux	Solid content (wt%)	Flux activity	Halide content
A	<2	no residue	0
B	2	no residue	0
C	2	no residue	0
D	2.1	no residue	0
E	2	no residue	0
Alpha 611	37	RMA	0.1
Alpha GR8	40	RMA	0.1

Table II: Solder pastes characteristics

Solder paste	Alloy composition	Metal content (wt%)	Flux activity
A	62Sn36Pb2Ag	89	no residue
B	62Sn36Pb2Ag	90	no residue

Table III: Main characteristics of solvents

Solvent	Compo-sition	Mol. weight	Boiling point (°C)	ODP* value
A	CCl_2 F-CH_3	117	32	0.1
B	alcohol mixture	-	78	-
Freon	CCl_2 F-$CClF_2$	187	48	0.8

* Ozon depletion potential

Ionic contamination measurement

Samples for ionic contamination measurements were soldered by circuit immersion in a solder pot when using fluxes A,B,C,D and E for hybrid circuit soldering, or wave soldered with fluxes A and B for printed circuits. Fluxes were preheated before soldering to the specified temperature, and after soldering circuits were not cleaned.

The dimension of hybrid circuit ceramic substrate were 2.5 cm x 2.5 cm and of the printed circuit 9 cm x 6 cm. Two circuits were used for each ionic contamination measurement. Ionic contamination on the circuits after soldering was measured by the static conductivity method in which the ionic conductivity of a mixture of 50 vol% distilled water: 50 vol% isopropyl alchohol was measured before and after immersion of the circuit in the solution for 10 minutes, using an Iskra MA 5964 Conductometer /3/.

The dynamic conductivity method was also used for ionic contamination measurements using two instruments;an Iskra Conductometer and an Omegameter 600 SMD in which the mixture of distilled water: isopropyl alchohol was circuled in the system after calibration with NaCl. The ionic contamination value measured is expressed in μg NaCl/cm^2 according to Standard MIL-P-28809A. To determine the quantity of ionic contamination on a specimen under test, the conductivity of a fixed amount of test solution used to extract and dissolve the contaminants was measured. The system detects and records the concentration of contaminants in the test cell at the begining of the test to establish a base line. Subsequent calculation represents only the amount of contamination added to the extract solution during the test. A state of equilibrium is attained when all the contaminants have dissolved in the test extract solution. At the conclusion of the test the final contamination level in equivalent micrograms of NaCl/cm^2 are recorded. Before running another test, the solution is regenerated through a built - in deionising system to establish a clean solution and a new base line for the next test.

Insulation resistance measurement

The test circuits for insulation resistance measurements were prepared according to DIN-32513 and IPC-SF-818 as given in Fig.1 and Fig.2. On the DIN-32513 test sample the distances between lines are 1.3 mm and the line widths 0.7 mm, and on the IPC-SF-818 test sample the line spacing is 0.7 mm and the line width is 0.35 mm.

Ten test samples were soldered with the same fluxes on ceramic substrates and on printed circuits. The insulation resistance between closely spaced soldered conductors was measured before and after testing in a humid chamber under conditions of 93%RH, at 40°C with 50V DC applied. Ten samples were also soldered with a rosin flux for testing and the circuits cleaned with Freon and solvents A and B.

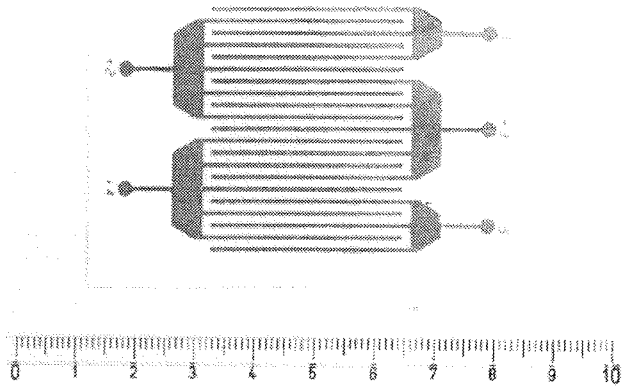

Fig.1: DIN-32513 test sample

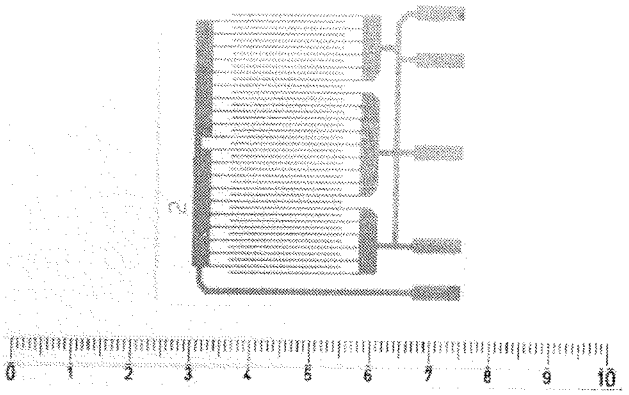

Fig.2: IPC-SF-818 test sample

RESULTS AND DISCUSSION

Ionic contamination measurement

The results of ionic contamination measurements are presented in Table IV for hybrid circuits printed on ceramic substrates and on printed circuits when the fluxes given in Table I were used for circuit soldering. The circuits were not cleaned after soldering. Visual inspection after soldering showed that the best appearance (clean, bright lines without solder balls) were obtained when fluxes A and E were used for soldering. For comparision the results when Alpha 611 was used for hybrid circuit soldering and Alpha GR8 for printed circuits soldering are also given.

The results of ionic contamination measurements when solder pastes were used for hybrid circuits or Alpha 611 for soldering in the solder pot and cleaned with Freon and the new solvents A and B are given in Table V. Ionic contamination was measured on hybrid circuits only, and by static and dynamic conductivity measurements using the instruments mentioned ealier. The solvent volume used to dissolve flux residues from a circuit surface of 1 cm^2 after soldering was 3 ml/cm^2 for static conductivity measurements.

The results obtained from dynamic conductivity measurements were expressed in $\mu g\ NaCl/cm^2$, because the instruments were calibrated with NaCl.

Table IV: Ionic conductivity measurement results

Flux	Ionic conductivity (μS/cm)		Ionic content ($\mu gNaCl/cm^2$)		
	Iskra Conductometer		Iskra Conductometer		Omega-meter
	Ceramic	Printed	Ceramic	Printed	Ceramic
A	0.35	0.5	0.6	-	0.5
B	0.3	-	0.8	0.6	0.5
C	0.4	0.6	0.5	-	0.7
D	0.2	-	0.7	-	1.4
E	0.8	-	2.1	-	5.9
A 611	0.4	-	0.8	-	-
A GR8	-	0.6	-	0.7	-

Table V: Ionic conductivity measurement results

Solder paste	Ionic conductivity (μs/cm)	Ionic content ($\mu gNaCl/cm^2$)	
	Iskra Conducto-meter	Iskra Conducto-meter	Omega-meter
A	0.1	1.2	-
B	0.2	0.8	-
Flux Alpha 611 cleaned with:			
Freon	0.2	1.3	1.1
A	0.1	0.8	0.6
B	0.05	0.6	0.3

The results given in Table IV show that fluxes D and E leave more ionic residues on the ciruits after soldering than fluxes A, B and C, and the results are comparable with results obtained for samples using Alpha 611 and Alpha GR8 rosin fluxes.

The highest of ionic redsidue after soldering was measured when flux E was used and is greater than the allowed limit of 1.3 μgNaCl/cm according to MIL-P-28809A. All other results are lower than the allowed limit of ionic content on circuits after soldering.

No great difference in ionic contamination left after soldering on ceramic substrates or printed circuits was observed. The measurements performed with the Iskra 5964 Conductometer were not so sensitive when the difference between the ionic contamination on the circuits were small.

The results given in Table V for solder pastes A and B containing "no residue" fluxes show comparable ionic residues on the circiuts after soldering. When hybrid circuits were soldered with Alpha 611 RMA flux and the circuits cleaned with Freon and solvents A and B, the results obtained with three instruments show that highest of ionic residue left on the circuits was measured when the circuits were cleaned with Freon and only a very small quantity of ionic residues when the circuits were cleaned with solvent B.

Insulation resistance measurements

The results of insulation resistance measurements after humidity testing under conditions of 93% RH, at 40°C, 50 V DC are given in Table VI when measured on DIN 32513 test sample and in Table VII on IPC-SF-818 test samples.

Table VI: Results of insulation resistance measurements on the DIN-32153 test sample after humidity testing

Flux	Insulation resistance after humidity testing (ohm)					
	168 hours		500 hours		1000 hours	
	Ceramics	Printed	Ceramics	Printed	Ceramics	Printed
A	10^{12}	10^{12}	10^{12}	5.10^{11}	5.10^{11}	10^{11}
B	8.10^{11}	8.10^{11}	5.1011	2.10^{11}	6.10^{11}	10^{11}
A 611	5.10^{11}	-	5.10^{11}	-	10^{11}	-
A GR8	-	10^{12}	-	10^{11}	-	$0.2.10^{11}$
Solder paste						
A	10^{12}	$0.8.10^{12}$	5.10^{11}	10^{11}	10^{11}	10^{11}
B		-	10^{11}	-	5.10^{11}	-

The insulation resistance was measured on DIN 32513 test samples on both substrates when residueless fluxes and solder paste containing residueless fluxes were used for soldering. The insulation resistance was measured only on hybrid circuits when Alpha 611 flux was used for circuit soldering and cleaned with the new solvents and Freon. The insulation resistance on the IPC-SF-818 test sample was measured on hybrid circuits only.

Table VII: Results of insulation resistance measurements on the IPC-SF-818 test sample after humidity testing (only on hybrid circuits)

Flux	Insulation resistance in humidity chamber; 93% RH,40°C (ohm)	
	Before test	168 hours
A	10^{11}	2.10^{8}
B	10^{12}	10^{10}
C	10^{11}	10^{10}
D	6.10^{10}	10^{7}
E	5.10^{10}	10^{7}
A 611	10^{12}	5.10^{11}
Soldered with Alpha 611 and cleaned		
Freon	8.10^{11}	8.10^{10}
A	8.10^{11}	5.10^{11}
B	10^{12}	10^{11}

The results of insulation resistance measurements given in Table VI after humidity testing in the humid chamber at 93% RH, 40°C with a voltage applied to the test circuits show that after 500 and 1000 hours no significant reduction of insulation resistance was observed on all samples. The minimum value of insulation resistance measured after 1000 hours on hybrid circuits and printed circuits was 10^{10} ohm which is higher than the allowed value of 10^{9} ohm according to Standard IPC-SF-818.

The results of insulation resistance measurements given in Table VII obtained on IPC-SF-818 test sample with very small distances (0.7 mm) between soldered lines (measured only on hybrid circuits) show a significant lowering of insulation resistance after 168 hours testing in the humid chamber. The lowest insulation resistance of 10^{7} ohm was measured when samples were soldered with fluxes D and E. The same test samples soldered with Alpha 611 and cleaned with solvents A and B and Freon showed an insulation resistance of 10^{11} ohm which is higher than allowed according to IPC-SF-818.

CONCLUSIONS

Five "no residue " fluxes and two solder pastes containing "no residue " fluxes and two organic solvents for circuit cleaning after soldering as substitutes for CFC

solvents were tested by ionic conductivity measurements of dissolved flux residues and insulation resistance measurements on test samples between closely spaced soldered conductors in humid conditions.

The results for ionic contamination left on the hybrid and printed circuits after soldering, measured with three instruments for measuring the conductivity of the solution in which the circuits were immersed, show that the "no residue" flux E contains a higher ionic content than the other fluxes. The most sensitive measurements were obtained using the Omegameter 600 SMD instrument.

When using the new solvents A and B for cleaning Alpha 611 flux after soldering, a very low ionic residue was measured on the circuit.

The insulation resistance measurements show a very low decrease of insulation resistance when measured on DIN 32513 test sample in all cases when compared with the results obtained on IPC-SF-818 test samples. The lowest insulation resistance of 10^7 ohm was found when measured on IPC-SF-818 test sample for hybrid circuits soldered with fluxes D and E as compared with 10^{11} ohm measured on samples soldered with Alpha 611 and cleaned with the new solvents A and B. This value was higher than the 10^{10} ohm measured on samples soldered with Alpha 611 and cleaned with Freon (CFC).

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Prispelo (Arrived): 13.10.95 *Sprejeto (Accepted): 20.10.95*

OPTIMIZACIJA PARAMETROV INJEKCIJSKEGA BRIZGANJA KERAMIKE

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Ključne besede: proizvodnja keramike, CIM brizganje keramike injekcijsko, brizganje vroče, pritiski visoki, oblikovanje keramike, izolatorji električni, proizvodnja množična, keramika steatitna, smole termoplastične, brizganje prahov, prahovi keramični, veziva termoplastična, odstranjevanje veziv, sintranje, poliranje

Povzetek: Pripravili smo različne termoplastične zmesi, izdelali poizkusno orodje za brizganje in odbrizgali poskusne serije vzorcev. Kritične stopnje v procesu injekcijskega brizganja so bile: mešanje keramičnega prahu in termoplastičnega veziva, izdelava poizkusnega orodja in brizganje vzorcev ter odstranjevanje veziva iz brizganih izdelkov. Sintranje in poliranje vzorcev sta bila standardna postopka. Izdelke smo na koncu izmerili in primerjali z referenčnim vzorcem. Analizirali in primerjali smo tudi mikrostrukture poliranih prerezov sintranih vzorcev. Ugotovili smo, da ima sestava z 20 ut. % PEG 20000 najugodnejše lastnosti za injekcijsko brizganje, pri sintranju se izdelek manj krči in zvija.

Parameters' Optimisation of the Injection Moulding of Ceramics

Keywords: ceramic manufacturing, CIM, Injection Moulding of Ceramics, hot moulding, high pressure, moulding of ceramics, electrical insulators, mass production, steatite ceramics, termoplastics resins, powder moulding, ceramic powders, thermoplastics binders, binder removal, sintering, polishing

Abstract: Powder injection moulding is a technology able to produce a new range of components from powders. Development was accelerated by increasing requirements of the electronic industry for intricate shapes. Thin and uniform walled parts are best suited for injection moulding, no matter how complicated in shape.

This paper reports about parameters' optimisation in the moulding process. The most critical steps were mixing of the powder and the binder, moldmaking and moulding and binder removal. Sintering and consolidation were common processing steps as for all ceramics. Several thermoplastic mixtures were prepared and different samples were injection moulded with experimental tool.

We used a commercial available Ba-steatite powder. To achieve a proper granulometric composition for the injection moulding we sintered and then re-milled the Ba-steatite powder. The binder was a water solved PEG 20000. The ceramic / binder compound was prepared with Z blade mixer at the room temperature. Composition was determined with injection moulding tests to achieve the best compromise between volume ratio of plasticiser / ceramic powder, injectability and sintered parts quality. Tests were carried out on a 150 g semi - automatic plunger injection moulding maschine Boy (FRG). First we tested the composition with the 22,5 wt.% PEG 20000 and 2,5wt.% camphor as a plasticiser (total volume part of binder was 44,4 vol.%). Thermal debinding of green ceramic parts was realised by free standing up to 290°C. After sintering at the 1330°C the ceramic parts were sectioned perpendicular and parallel to the flow direction of the mixture. After polishing the microstructure was analysed by optical microscope. We found out, that microstructure was dense and homogenous with fine pores of max. 30 μm. The average porosity was 4,3 %. In order to reduce distortion of moulded parts, we made the mixture with 18,0 wt.% PEG 20000 and 2,0 wt.% camphor plasticiser. Total volume part of the binder was 37,5 vol.%. The microscopic analyses showed fine microstructures with pores under 25 μm. Total porosity was 7,5 %. The distortion of sintered parts was reduced. Continuing reduction of binder amount on 18 wt.% (34,5 vol.%) didn't get dense microstructure.

Finalised samples were compared with the reference sample. It was found out, that the composition with 20 wt.% PEG 20000 has the most suitable properties for the injection moulding process, has a low shrinkage and distortion at the sintering.

UVOD

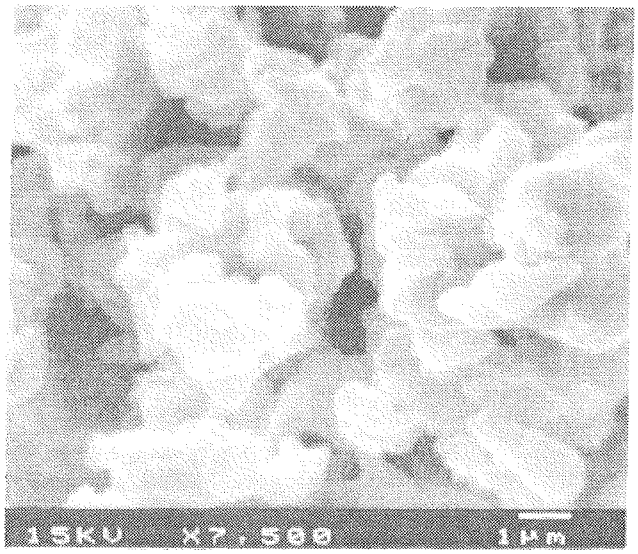
Injekcijsko brizganje keramike (CIM) je postopek, ki omogoča ekonomično oblikovanje najzahtevnejših oblik keramike kot so npr.: električni izolatorji kompleksnih oblik, vodila niti, itd. Postopek je primeren tako za izdelavo unikatov kot tudi za veliko serijsko proizvodnjo /1,2/.

Vroče brizganje keramike je cikličen proces, kjer se granulat iz keramičnega prahu in termoplastičnega veziva segreje do zmehčišča, nato pa s pritiskom vbrizga v kalup, kjer se ohladi in strdi, pri čemer nastane izdelek z določeno obliko. Postopek je zelo podoben brizganju plastičnih mas /3/.

Kritične točke postopka brizganja keramike so: priprava termoplastične mase, izdelava kovinskega modela in brizganje izdelka in nazadnje postopna odstranitev termoplastičnega veziva iz izdelka /4/. Sintranje in površinska obdelava kot zadnji stopnji v izdelavi keramike sta standardna postopka in sta odvisna od vrste keramike.

EKSPERIMENTALNO DELO

Uporabili smo komercialen Ba-steatitni keramični granulat /5/, ga sintrali pri 1320°C in suho zmleli do 2% ostanka na situ 63 μm. Porazdelitev velikosti delcev zmlete keramike smo pregledali s SEM mikroskopom (slika 1) in se tako prepričali, da keramični prah ne vsebuje koloidnih delcev, ki bi slabo vplivali na viskoz-



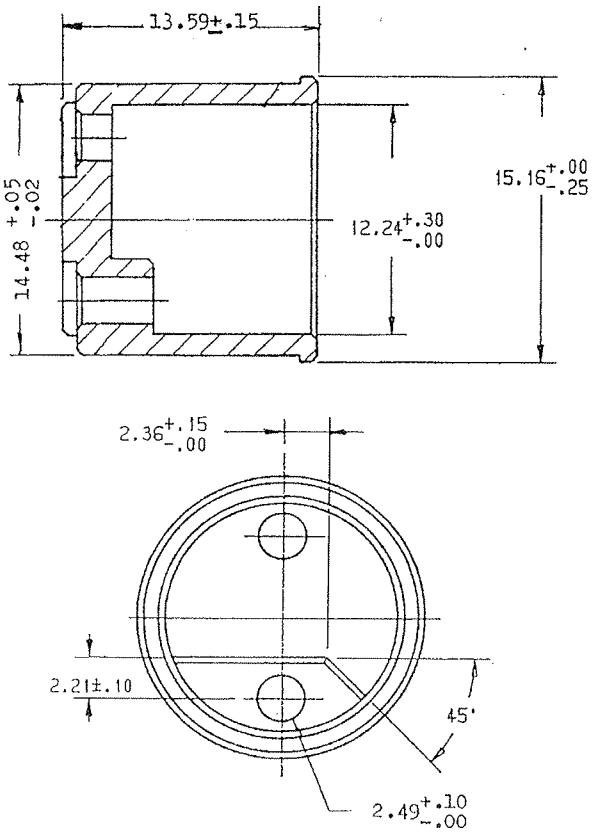
Slika 1: SEM posnetek suho mletega Ba-steatitnega granulata

nost in livnost termoplastične mase /6/. Termoplastične mase smo pripravili v laboratorijskem kolenastem gnetilcu volumna 1000 ml (Netzsch, ZRN). Keramični prah in 50% vodno raztopino PEG 20.000 (tabela 1) /7,8/ smo gnetli eno uro pri sobni temperaturi, posušili v sušilniku pri 110°C. Posušeno maso smo zdrobili v kolenastem gnetilcu in tako dobili granulat primeren za doziranje v stroj za injekcijsko brizganje. Vzorce smo brizgali na 150 g polautomatskem stroju za brizganje plastičnih mas Boy (ZRN). Vezivo smo iz oblikovancev odstranjevali v laboratorijskem sušilniku s postopnim dviganjem temperature (5°C/h) do 290°C. Izdelke z izgnanim vezivom smo sintrali v industrijski peči pri 1330°C, z zadrževanjem pri maksimalni temperaturi 2,5 ure. Temperatura v peči je v temperaturnem območju od 20 do 650°C naraščala s hitrostjo 80°C/uro, od 650 do 1330°C pa s hitrostjo 150°C/uro. Na obrusih sintranih vzorcev smo analizirali mikrostrukturo keramike. Poroznost smo izmerili z linearno mikroskopsko metodo tako, da smo izmerili delež por, ki so ležale na namišljenih črtah. Ta delež por odgovarja volumskemu odstotku por. Sintrane izdelke smo zbrusili s korundnim prahom št. 280 v porcelanskem bobnu in nazadnje izmerili, kako se geometrija izdelka ujema z načrtom izdelka.

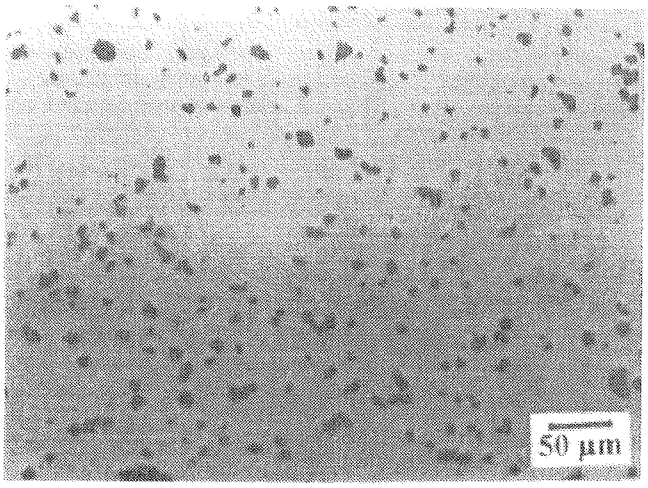
REZULTATI

Za preizkuse brizganja smo izbrali zahtevnejši izdelek, ki služi kot električni izolator pri povišani temperaturi (slika 2). Izdelek ima tanke (1,12 mm) in dolge (10,80 mm) stene, zato ga s klasičnimi tehnologijami oblikovanja ne moremo izdelati.

Preizkusili smo različne kombinacije termoplastičnih veziv, od katerih bomo opisali najzanimivejše poizkuse z vodotopnim vezivom PEG 20.000 prozvajalca Hoechst (ZRN), (tabela 1). Kot mehčalo smo dodali sintetično, tehnično čisto kafro (Hoechst, ZRN) in sicer 10 ut.% glede na dodatek PEG. V nadaljevanju opisujemo poizkuse s 25, 20 in 18 ut.% dodatka termoplastičnega veziva.



Slika 2: načrt keramičnega izdelka za vroče brizganje



Slika 3: mikrostruktura vroče brizganega izdelka s 25 ut. % PEG 20000 (opt. mikroskop)

Najprej smo odbrizgali termoplastično zmes s 25 ut.% veziva, ki je bilo sestavljeno iz 22,5 ut.% PEG in 2,5 ut.% kafre. Vezivo je volumsko predstavljalo 44,4 vol.%. Temperatura brizgalnega polža je bila 160°C, temperatura orodja 30°C, čas stiskanja 2 min in pritisk v orodju

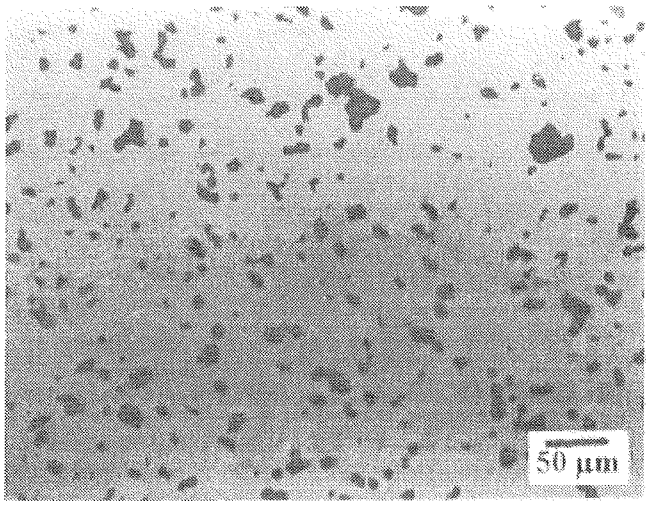
0,5 MPa. Izdelkom smo odstranili vezivo in jih sintrali. Homogenost mikrostrukture smo preiskali z optičnim mikroskopom (slika 3). Dosegli smo zelo gosto in enakomerno mikrostrukturo, z drobnimi porami pretežne velikosti 5 do 30 μm. Povprečna poroznost vzorca, merjena z mikroskopom, je bila 4,3%.

Da bi zmanjšali deformacije izdelka pri izganjanju veziva in sintranju, smo zmanjšali koncentracijo termoplastičnega veziva na 20 ut.% (18,0 ut.% PEG in 2,0 ut.% kafre) in odbrizgali vzorce. Volumski delež veziva je bil 37,5 vol.%. Vzorcem smo izgnali vezivo, jih odsintrali in analizirali mikrostrukturo (slika 4). Mikrostruktura vzorca je bila še vedno gosta, z mikroskopsko določeno povprečno poroznostjo 7,5%. Pretežna velikost por je 3 do 25 μm. Deformacija izdelka se je zmanjšala.

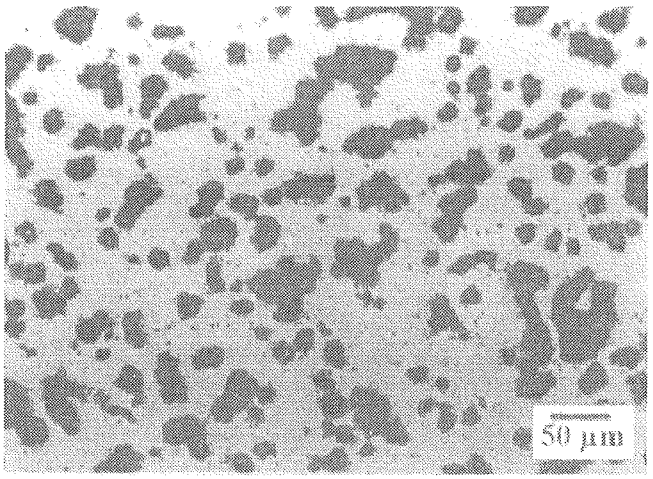
Pri nadalnjem zmanjšanju vsebnosti termoplastičnega veziva na 18 ut.% (16,2 ut.% PEG in 1,8 ut.% kafre), pri enakih pogojih brizganja, nismo več dosegli goste mikrostrukture (slika 5), pore so ostale povezane. Volumski delež veziva je v tem primeru znašal 34,5 vol.%.

Tabela 1: tehnični podatki za PEG 20000 /5/

opis	voščeni kosmiči krem barve
rel. molarna masa	okoli 20000
temperatura strdišča (°C) /DIN 51570/	okoli 60
hidroksilno število /DIN 53240/	<7
topnost v vodi pri 20 °C (ut. %)	nad 50
viskoznost 50 % razt pri 20°C (mPa.s)	2200-2800
piroliza	nad 250°C prične razpadati in do 400°C razpade brez ostanka



Slika 4: mikrostruktura vroče brizganega izdelka z 20 ut. % PEG 20000 (opt. mikroskop)



Slika 5: mikrostruktura vroče brizganega izdelka z 18 ut.% PEG 20000 (optični mikroskop)

ZAKLJUČKI

S kalcinacijo in mletjem smo pripravili steatitno keramično maso za vroče brizganje pod visokim pritiskom. S kalcinacijo steatitnega granulata in mletjem kalcinata smo pripravili primerno zrnatost keramičnega prahu za vroče brizganje. Termoplastrično maso smo pripravili s homogenizacijo keramičnega prahu in vodne raztopine PEG 20000. Za mehčanje smo dodali kafro. Za brizganje kompleksnega keramičnega izolatorja z dolgimi in tankimi stenami smo izdelali štiri gnezdno jekleno orodje z izmenljivimi videa vložki. Obliko dolivnih kanalov smo prilagodili visoki viskoznosti termoplastične keramične mase tako, da smo dobili brezhibno zalivanje kalupov. Na polavtomatskem stroju smo optimizirali parametre brizganja: vsebnost termoplastičnega veziva, temperaturo brizganja, temperaturo orodja, pritisk in čas brizganja. Mikrostrukturo odžganih keramičnih vzorcev smo spremljali na obruskih z optičnim mikroskopom. Optimizirali smo postopek izgona veziva iz brizganih izdelkov, na zraku, v temperaturnem območju od 20 do 290°C. Vzorcev pri izganjanju veziva nismo zasipali, ampak so prosto stali v pečici za odstranjevanje veziva. Izbrali smo najugodnejše parametre za celoten postopek izdelave brizgane keramike, pri čemer so bile kritične točke izbira vrste in količine veziva in način vmešavanja, izdelava orodja in izbira pogojev za brizganje ter postopek odstranjevanja veziva iz oblikovancev. Ostale operacije izdelave keramike so bile standardne.

ZAHVALA

Delo je bilo opravljeno s finančno podporo Ministrstva za znanost in tehnologijo Slovenije.

Optično mikroskopske analize je izdelala Marija Prelec, dipl. ing.

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Prispelo (Arrived): 03.10.1995 *Sprejeto (Accepted): 19.10.1995*

UPORABA ELEKTRONSKIH KOMPONENT

PRENAPETOSTNA ZAŠČITA V TELEFONIJI

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1. UVOD

Področje prenapetostnih zaščit v telefoniji z visokim porastom elektronskih vezij in podsestavov izpodriva relejno tehniko že nekaj desetletij. Z novimi številnimi funkcijami, ki jih omogočajo sodobne telekomunikacijske naprave, rastejo zahteve v kar največjo tehnično tehnološko integracijo. Cilji vsake nove generacije telefonskih central so čimveč funkcij na kar najmanjšem prostoru, križne komunikacije, kar najnižji strošek na telefonsko linijo, velike spominske zmogljivosti, fleksibilno prespajanje mreže s čim boljšo izrabo zmogljivosti telefonske mreže in nudenje dodatnih dražjih uslug.

Ker optične komunikacije še niso presegle rentabilnostnega praga pri najnovejši dolgoročni želji "z optičnim vlaknom do doma", preostaja klasični bakreni linijski telefoniji v nekem delu trase od centrale do naročnika kar dovolj prostora pa tudi zahtev za prenapetostno zaščito.

Sodobna telefonska centrala povezuje vse vrste modernejšega prenosa govora, slik in tekstov, ter računalniških podatkov, mobilno telefonijo, optične zveze, radio relejne in radijske zveze, sisteme klicanja oseb, satelitske zveze, itd. V desetletju se je tehnologija prevesila predvsem na množico občutljivih elektronskih elementov, pri katerih prednjačijo čipi s podmikronsko tehnologijo in množico softwarskih vrstic, ki jih upravljajo.

Tudi predstopnje na glavnih razdelilnikih telefonskih central so se fizično zmanjšale. Prej velike sobane z drdrajočimi centralami z releji in premikajočimi se mehanskimi deli in predsobanami s prepletajočimi se kabli ter velikimi telefonskimi letvicami, so zamenjali prostori z urejeno klimatizacijo, posebnimi vrstami tal in drugimi prej znanimi zaščitnimi pristopi za velike računalniške centre. V sodobni telefonski centrali je 100 krat in več računalniške zmogljivosti, kot je bilo pred leti v računalniških centrih velikih firm.

Temu ustrezna bi morala biti tudi prenapetostna zaščita in zaščita proti streli, ki jo opredeljujejo številna priporočila, standardi in predpisi.

Direktne in bližnje razelektritve

Direktni udari strele v zaščitnem razredu I izkazujejo naslednje najvišje parametre:

Zaščitni razred:	po IEC 1024-1 ..	visoki
Prvi delni udar strele:	v kA	200
.....	T_1 v µs	10
.....	T_2 v µs	350
naslednji:	I v kA	50
.....	T_1	0,25
.....	T_2, µs	100
dolgi tok:	I v A	400
.....	T v s	0,5

2. SISTEMSKA ZAŠČITA TELEFONSKIH CENTRAL

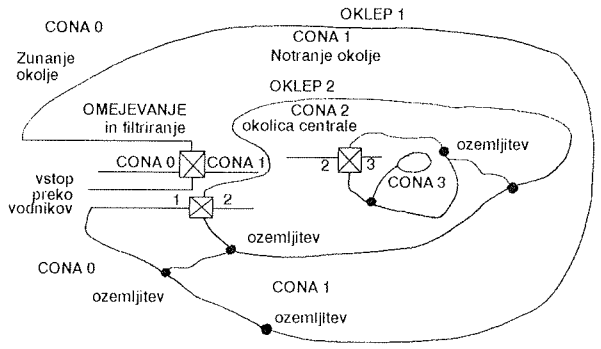
Sistemska zaščita vsebuje mere zunanje in notranje zaščite telefonskih central.

Popolna zaščita proti direktnemu udaru strele je možna le na energetski strani s postopnim zmanjševanjem naletnega vala toka strele preko niza sistemskih mer.

S sistemom zunanjih mer moramo strelo najprej ujeti, začenši s strelovodno napeljavo, jo odvesti postopoma proti zemlji ter prenapetosti spraviti na neškodljiv nivo. V enem prevodnem kanalu strele je več delnih udarov. Tudi naslednji delni udari strele so zelo nevarni, ker se jim povečujejo, zaradi že vzpostavljenega prevodnega kanala oblak-zemlja, hitrosti vzponov amplitude vsakega udara. S tem se povečajo elektromagnetni indukcijski vplivi škodljivih pojavov. Več kot polovico škod iz prenapetosti in strele povzročijo drugi izviri motenj, kot so energetske naprave, električna vleka (tramvaj, vlak, podzemna železnica) in industrijske motnje.

2.1 Zunanja zaščita proti streli in prenapetostim po IEC 1024

V standardih IEC 1024 prevladuje sistem zaščitnih con. V coni 0 izvirajo motnje. V coni 1 so naprave, ki lahko občasno tudi izpadejo ali pa so manj občutljive na prenapetosti. V coni 2 so najpomembnejše naprave , ki ne smejo zatajiti. Cono 3 pa predstavljajo kovinska



Slika 1: Oklapljanje in ozemljevanje con pri kompleksnih napravah. Mesto prenapetostnih elementov je prikazano s kvadratom z diagonalnim križcem.

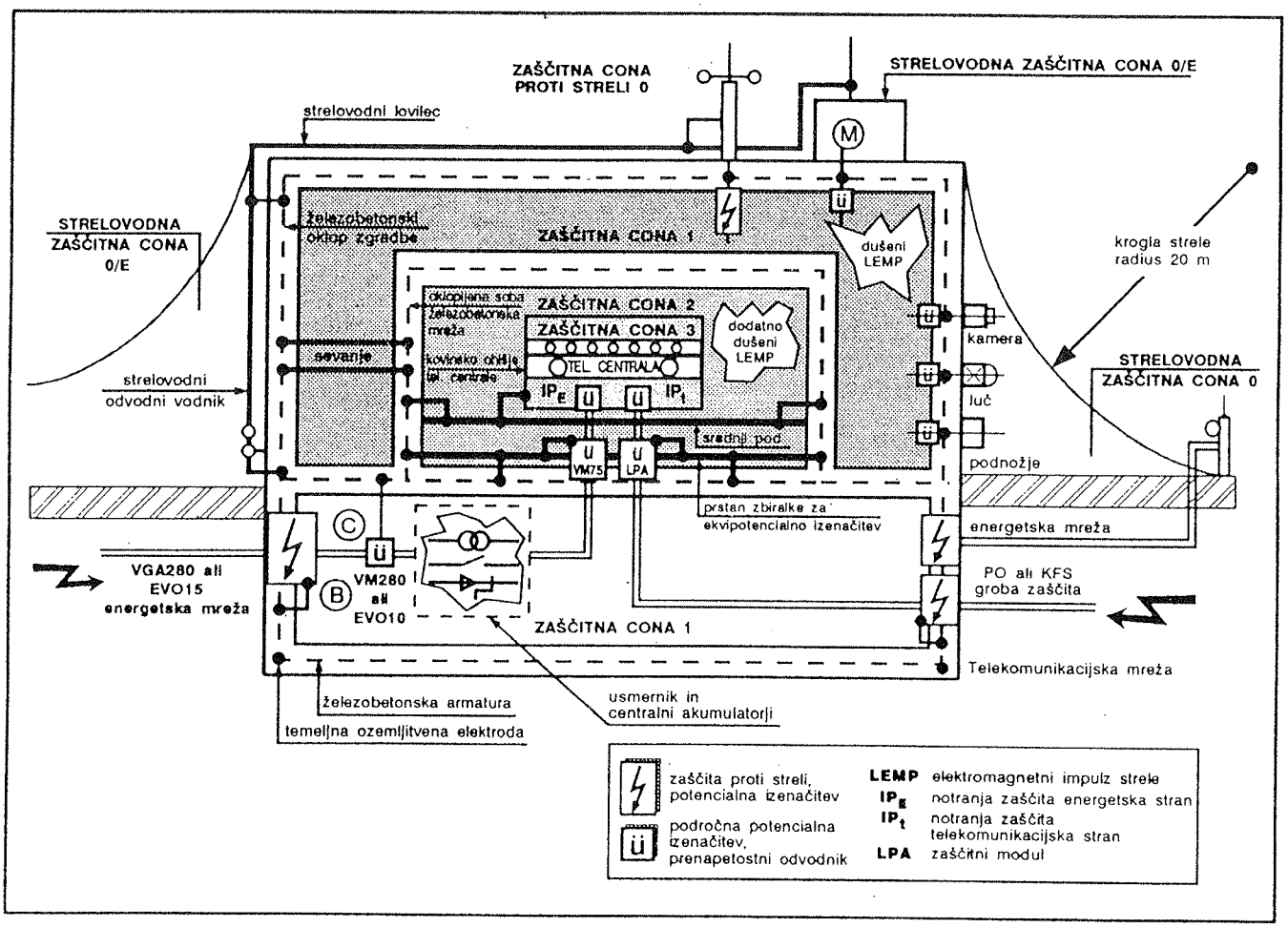
ohišja le teh (same telefonske centrale in koncentratorjev itd.)

Seveda je pri telefonskih centralah bistven še vnos možnih naključnih motenj preko telekomunikacijskih vodnikov. Tako so glavni delilniki telefonskih naprav pogosto v coni 1. Vsaka zaščitna cona mora imeti svoj oklop.

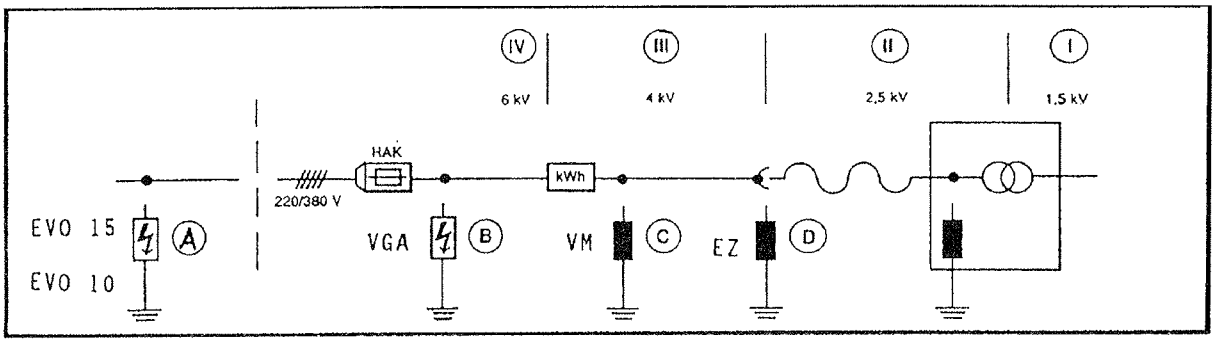
Prva cona ima oklop iz železne armature zgradbe, druga iz armature sobe, v kateri se nahaja centrala. V njej bi se moral praviloma nahajati glavni delilnik z zaščitnimi elementi in centrala ter tretja zaščitna cona kot že omenjeno ima kovinski oklop iz samega ohišja telefonske centrale.

Z leve je prikazana priključitev energetske mreže in zaščite na njej, z desne pa telekomunikacijska. Glavni delilnik in zaščita na njem so prikazani s simboli zaščite U in LPA. S pomočjo oklapljanja se zagotavlja telefonski elektroniki zaščiteni prostor pred elektomagnetnimi sevanji in odpravlja možnost, da se preko elektromagnetne indukcije pojavijo več tisoč voltov visoke prenapetosti.

Potrebno je še zamašiti luknje, ki jih za motilne impulze predstavljajo poteki vodnikov na prehodih v posamezno višjo zaščitno cono. To se odpravi v več stopnjah z zaščitnimi napravami različnih lastnosti.



Slika 2: Primer pravilnega ščitenja telefonske centrale z zunanjo in notranjo zaščito. S prelomljeno puščico so označene zaščitne naprave ali elementi za odvod strele. Znak U označuje prenapetostne zaščitene naprave in kompleksne elemente zaščite.



Stopenjska vgradnja zaščitnih naprav po razredih v skladu z DIN VDE 0675.
Legenda:
- EVO 15
- VGA 100 kA zaščita
- VM 15 kA zaščita

Slika 3. Stopenjsko odvajanje udara strele v energetskem napajalniku. Vgradi se med vsako fazo, ničenjem in ozemljilom.

2.2 Zunanja in notranja zaščita na energetski napajalni strani

Energetska zaščita mora odvesti po stopnjah naletni val strele in prenapetosti na neškodljiv nivo na napajalni strani.

V predstopnji pred stavbo je energetski odvodnik (na primer varistorski odvodnik EVO 15 V 275), ki ga namesti elekrodistribucija. V prvi stopnji v stavbi je običajno za števcem odvodnik strele v glavni razdelilni omarici, na primer Blitzduktor ali iskrišče Dehnguard, nato sledi v področni razdelilni omarici varistorski prenapetostni odvodnik VM 275.

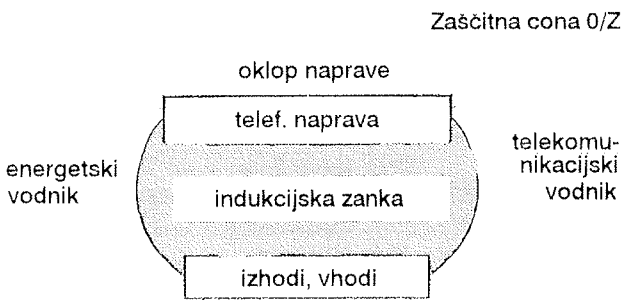
Sledi prenapetostni odvodnik VM 70 izza napajalnika na enosmernem napajanju iz centralne baterije in tik pred samo telefonsko centralo na prehodu iz zaščitne cone 1 v cono 2. Centrala sama ima lastno notranjo zaščito na energetski strani v zaščitni coni 3.

2.3. Ekvipotencialno izenačevanje

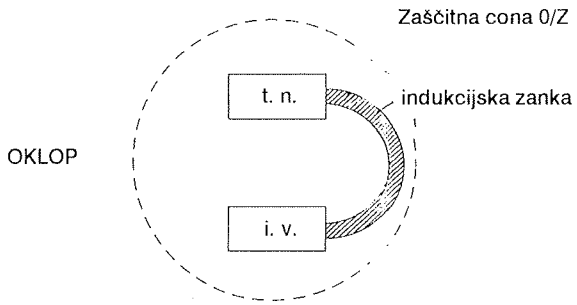
Vsak prehod preko ene zaščitne cone v drugo mora z izvedenimi ekvipotencialnimi izenačitvami ustvariti lokalno plavajočo mrežo. Prva funkcionalna plavajoča zemlja naj bo okrog centrale same za cono 3. Druga naj bo v armaturi prostora, kjer je centrala in druge potrebne naprave, to je okrog zaščitne cone 2; tretja v stenski železobetonski armaturi stavbe in okrog cone 1 in četrta na vkopanem ozemljilu celotne stavbe. Priporočljivo je čimvečje prepletanje vodnikov med ekvipotencialnimi ozemljili posameznih zaščitnih con. Lokalna ozemljila so večinoma izvedena v obliki ekvipotencialnih zbiralk.

2.4. Elektromagnetne zanke

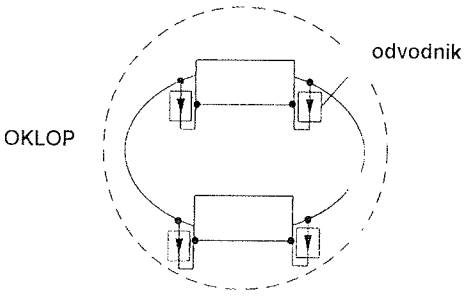
Najpogostejša napaka, ki kljub vgrajeni kompleksni zaščiti z LPA moduli vnese visoke prenapetosti tik pred vhodom v centralo na telefonskih linijah, so ustvarjene elektromagnetne zanke med energetskimi vodniki napajanja in tekekomunikacijskimi vodniki. Oboji morajo potekati paralelno blizu skupaj tako, da se inducirane napetosti še da obvladati.



Slika 4. Neprimerni poteki vodnikov, elektromagnetne zanke povzročajo visoko inducirano napetost.



Slika 5. Zmanjšana indukcijska zanka.



Slika 6. Alternativna rešitev, odvodniki tik pred telefonskimi napravami. Vgrajeni naj bodo v kovinskih ceveh ali mreži.

Dogaja se, da zaradi nepravilnega postavljanja vodnikov z zaščitnimi moduli LPA očiščeni telefonski vodniki preko elektromagnetne indukcije ponovno prejmejo visoke za centarlo škodljive prenapetosti. To se dogaja v okolju, v prostorih, kjer niso upoštevani standardi zunanje zaščite po zaščitnih conah po IEC 1024.

2.5. Stopenjska vgradnja zaščitnih naprav

Pri stopenjski postavitvi zaščitnih elementov in modulov je zelo pomembna skladnost razdalj med zaščitami. Že pri impulzu 3 kA 8/20 μsek in 1 μH/m induktivnosti vodnika se pojavi dodatna napetost 1 kV na 1 m. Zato je priporočljivo, da zaščitni moduli na glavnem delilniku in druge zaščite niso več kot 5 m oddaljene od ščitenih naprav.

3. ELEMENTI PRENAPETOSTNE ZAŠČITE V TELEFONIJI

Skoraj vse osnovne elemente prenapetostne zaščite se smiselno uporablja tudi v telefoniji.

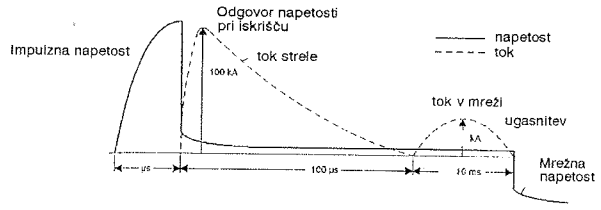
Idealnega zaščitnega elementa ni. Pogoji posameznega okolja in ščitene naprave zahtevajo poseben izbor elementov. Projektanti in lastniki telefoskih naprav bi želeli čim bolj enostavne in splošne rešitve. Le kombinacije elementov v prenapetostnih modulih odpravljajo slabosti posameznih neidealnih lastnosti določenega elementa.

Tehnični komite TC/SC IEC 37 je doslej izdal več standardov in predlogov standardov s področja elementov prenapetostne zaščite. Specifični elementi za tokovne in prenapetostne odvodnike motenj za zaščitne naprave so iskrišče, plinski odvodniki (GDT), kovinski oksidni varistorji (MOV), avalanche dvosmerne ali enosmerne diode in tiristorski supresorji za prenapetosti.

3.1. Iskrišča

Iskrišča se uporablja pri direktnem odvodu strele na energetski mreži.

Največ uporabe je bilo pri televizijskih stolpih, v katerih je običajno nameščena tudi oprema za mobilno telefonijo. Druga večja uporaba je v premakljivih radiorelejnih in mobilnih postajah.



Slika 7. Obnašanje iskrišča kot odvodnika strele

Po vzpostavitvi standarda IEC 1024 se uporabljajo iskrišča posebnih izvedb tudi v široki mreži energetske zaščite kot prvi odvodnik strele na stavbi. Odgovarja zaščitnemu razredu B.

Za posamezni preizkusni odvod strele je potrebno uporabiti v telefoniji na linijah 5% od preizkusnega toka strele. Zadnji znaša 100 KA oblike 10/350 μ sek.

3.2. Plinski odvodniki

Plinski odvodnik je najpogostejši element prenapetostne zaščite v telefoniji. Ko prenapetost prekorači nominalno vrednost in toleranco pri počasnem dvigovanju napetosti z vzponom 100 V na sekundo, se plinski odvodnik vžge. Pri tem notranji plin, ki je bil do tedaj visok dielektrik, preide v ionizirajoče stanje ter iz več M ohmske vrednosti postane povsem prevoden.

Plinske odvodnike se vgrajuje paralelne med vodnike linije in zemljo v telefonski mreži, v predstopnjah, na glavnem delilniku in v nekaterih elektronskih telefonskih napravah.

Plinski odvodniki so obravnavani v standardih CCITT K 12 in K 20 ter v ustreznem predlogu standarda IEC 1647.

Velika prednost plinskih odvodnikov je visok odvodni tok, slabost pa relativna počasnost odpiranja pri zelo hitrih impulzih strele, pa tudi pri nekaterih industrijskih motnjah.

Tako hitri motilni impulzi preskočijo običajno enega od dvo-elektrodnih plinskih odvodnikov v paru na telefonskih paricah in neposredno poškodujejo plošče tiskanega vezja ter pripadajočo elektroniko ščitene naprave.

Boljši so troelektrodni plinski odvodniki, še primernejši pa so kompleksni zaščitni moduli LPA (lightning protection assembly), ki vsebujejo plinske odvodnike v večstopenjski funkcionalni zloženki, skupaj s hitrejšimi elementi.

Ker tipični, v telekomunikacijah uporabljeni plinski odvodnik z nominalno napetostjo vžiga 230 V ne ugasne pri napetosti 220 V 50 Hz, je potrebno dodajati v zaščitne podsestave še tokovno zaščito.To velja v vseh

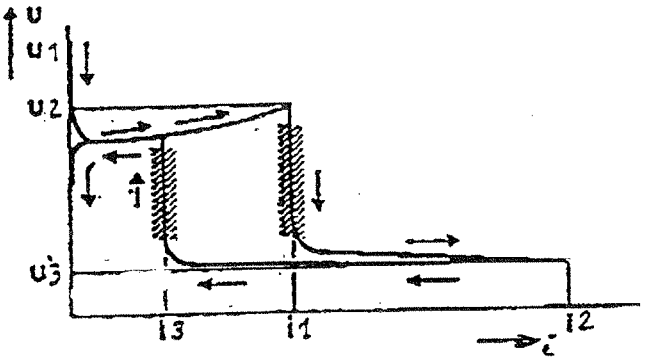
primerih, ko je možno, da pride energetska linija v stik s telefonsko. Primeri so redki, vendar povzročijo visoke škode, saj zgori kar cela centrala. Lahko se razvijajo škodljivi plini, ki povzročijo še dodatno škodo. Kratkostično tokovno zaščito se izvaja z raznimi talilnimi vložki, ki se tale med 90 do 145 stopinjami Celzija. Prespoje posamezni ogroženi vodnik preko elektrode plinskega odvodnika z zemljo. Visoki trajni tokovi proti zemlji pa še vedno ogrožajo vodnike in njihovo izolacijo. Zato so priporočljivi dodatni ukrepi s termičnimi odvajali, ki prekinejo zelo redki predolgo trajajoči škodljivi tokokrog energetske napetosti na telefonski liniji.

3.3 Varistorji

V telefoniji se uporabljajo kovinsko oksidni varistorji (MOV), tako za zaščito energetskega napajalnega dela največ v zaščitnem razredu C kot tudi na telekomunikacijski strani. Pogosto tvorijo varistorji notranjo zaščito linij telekomunikacijskih naprav. Kristalna struktura varistorja omogoča slično delovanje kot pri množici bidirekcionalnih diod. Slabost sicer hitrih varistorjev, ki s časom reakcije prekašajo plinske odvodnike za 5 do 10 krat, pa je staranje. V kolikor stojijo samostojno ali brez filtrskih vmesnih členov, jih številni škodljivi impulzi notranje načenjajo. Zato morajo biti vgrajeni varistorji v mreži 220 V napajanja vedno s termičnimi varnostnimi varovali, v telefonskih linijah pa v funkcionalnih zloženkah v kompleksnih zaščitnih modulih. Naloga integriranih termičnih varoval je, da odklopijo varistorski odvodnik od napajalne napetosti, če se varistor segreje nad dovoljeno temperaturo, kar se zgodi pri preboju varistorja.

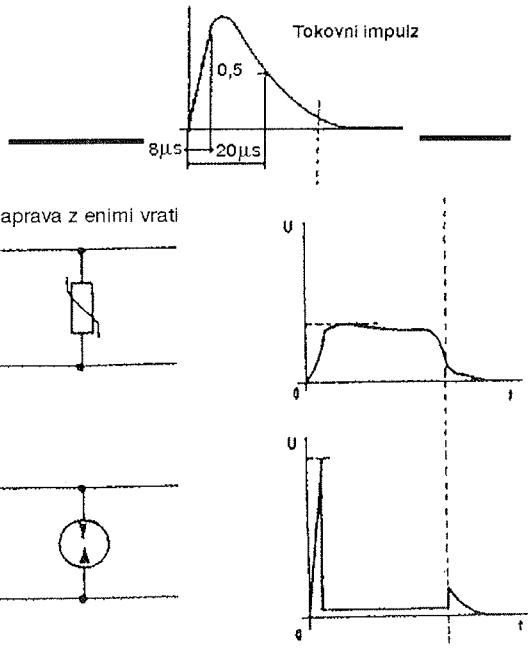
V telefonskih zaščitah nastopajo varistorji v funkcionalnih zloženkah.

Za zaščite v telefoniji so še posebno pomembne visokofrekvenčne karakteristike. Zato priredimo varistorje v proizvodnji z inačico zelo nizkega povratnega prepustnega toka, visoko ohmsko začetno upornostjo in hitrim odzivom na račun energetskih lastnosti. Zadnje zagotavlja plinski odvodnik v funkcionalni zaščitni zloženki kot je na primer zaščitni modul LPA.



U_1 Istosmerna napetost iskrenja
U2 napetost žarenja
U3 napetost loka
I1 prehodni tok žarenja v lok
I2 vrhnji tok žarenja v lok
I3 prehodni tok

Slika 8a: Napetostno tokovne lastnosti plinskih odvodnikov

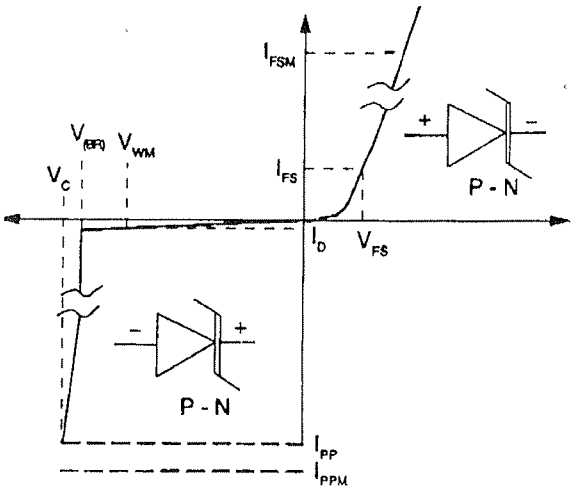


Slika 8b: Odgovor plinskega odvodnika in varistorja na tokovni impulz

3.4. Silicijeve plazovite (avalansche) diode (SAD)

Naloga teh diod je prav tako omejevanje prenapetosti in odvajanje škodljivih tokov s hitro spremembo prevodnosti. Pri Vbr (breakdown voltage) začne taka dioda hitro prevajati in pri Vc (clamping voltage) doseže Ipp vrhnji impulzni tok.

Na sliki 9 je prikazana karakteristika plazu pri enosmerni diodi. Več so v uporabi dvosmerne zaščitne diode. Te

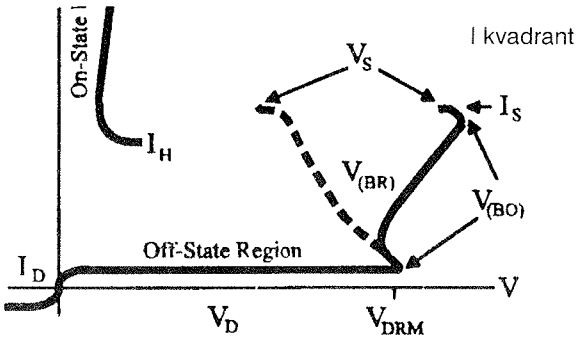


V_{wm} nominalna napetost
I_d max stand-by tok
Vbr prelomna napetost
I_{cc} vrhnji impulzni tok pri Vc

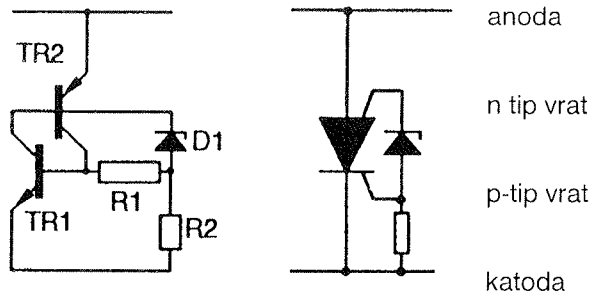
Slika 9: Karakteristika enosmerne zaščitne diode.

diode so lahko zelo hitre in odpirajo v pikosekundnih časih. Omejitve uporabe nastopajo zaradi nizkih tokovnih odvodnih sposobnosti. V zloženih variantah samih elementov je po več diod paralelno, da izboljšajo odvodne lastnosti. Še pogosteje se hitre prenapetostne diode uporabljajo v funkcionalnih zloženkah prenapetostnih modulov skupaj s plinskimi odvodniki in filtrskimi vmesnimi členi. Predlog mednarodnih opredpisov, ki jih bo verjetno prevzela tudi Slovenija, je standard IEC 1647-2.

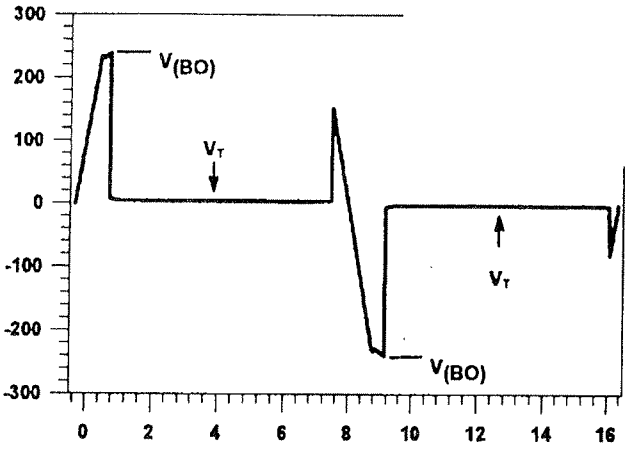
3.5. Tiristorski prenapetostni odvodniki (po IEC 1647-4)



Slika 10: Tokovno napetostne karakteristike tiristorskega prenapetostnega odvodnika



Slika.11: Nadomestno vezje in tiristorskih ekvivalent.



Slika.12: Odziv 230 V TTS na prenapetostni dvostranski impulz izmenične napetosti 600 V, kratek stik 1,2 A

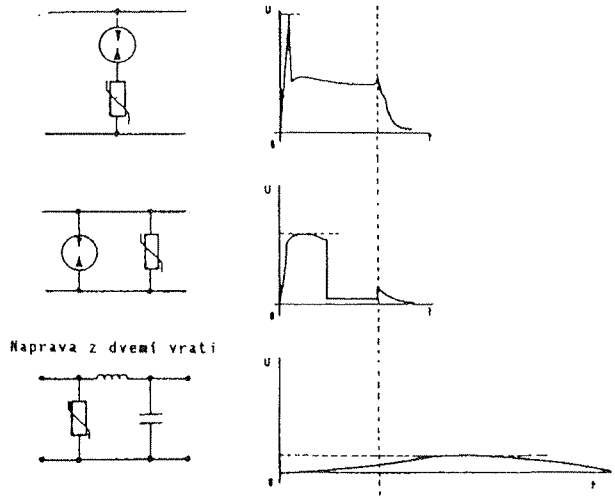
Tiristorski prenapetostni odvodniki imajo serijo n in p plasti v silicijevem čipu. Osnovna gradnja ima tri pn spoje kar zahteva štiri polprevodniške plasti (npnp).

Tranzistor TR1 je izdelan z $n^+ pn^-$ plastmi. TR2 je izdelan s pn-p plastmi. Preklopno funkcijo prikazuje plazovita dioda D1. Upor R2 skupaj s stranskim uporom p plasti R1 tvori shunt za spoj baza-emitor tranzistorja TR1.

4. PRENAPETOSTNE ZAŠČITE V FUNKCIONALNIH ZLOŽENKAH

4.1 Zaščite z dvemi vrati

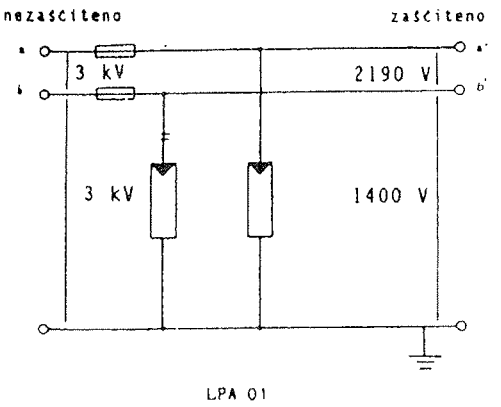
Potem, ko smo si pogledali elemente prenapetostne zaščite z enojnimi vrati, poglejmo še zaščitne kombinacije z dvemi vrati. Na vhodno stran je vsiljen prenapetostni impulz. Vsiljene in omejene napetosti na izhodni strani posameznih sestavov so podane na sliki 13.



Slika 13: Tipične nepopolne in izboljšane zaščite z dvemi vrati.

Na glavnem delilniku telefonske centrale obstoja več pristopov pri uporabi prenapetostne zaščite. Preprosta zaščita vsebuje le plinski odvodnik v liniji v smereh vodnika a proti zemlji in vodnika b proti zemlji. Taka vrsta zaščite je umestna le v visoko zaščitenih okoljih z vkopanimi in z zares kovinskimi cevmi oklopljenimi kabli. V vsakem drugem primeru gredo upravljalci telefonskih central v rizike z zastoji v prometu, v zahtevnejše vzdrževanje, z večjim skladiščem rezervnih delov in ekonomsko večjo škodo.

Preizkus, ki simulira sekundarne učinke toka strele z ustreznim impulznim generatorjem, daje rezultate, ki so prikazani na sliki 14. Na vhodnih sponkah vsiljujemo 3 kV napetost oblike 0,3 /50 μ sek.

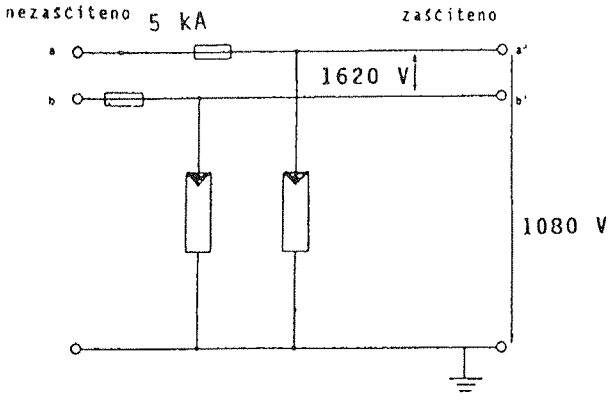


Slika 14: Prikaz reakcij enostavnega prenapetostnega modula na vsiljeno hitro napetost.

Tipično je, da prepočasni plinski odvodnik v LPA 01 dopusti preostalo napetost, ki je višja od nominalne (1kV) prebojne trdnosti centrale. Posebno očitni so ostanki prenapetosti celo preko 2.000 V med vodnikoma a in b na izhodih, ki sta označena na sliki z a" in b", kadar gre za dva dvopolna plinska odvodnika. Ta imata lahko različne statične napetosti reagiranja (230 V ±20%), ki v dinamičnih razmerah še bolj povečata preostalo napetostno razliko med vodnikoma na vhodu telefonske centrale. Tako povečanih napetosti centrala ne vzdrži ter pride do velikih poškodb. Popolnejši zaščitni modul LPA 08 s celotno kompleksno zaščito dopusti cca 410-560 V preostale napetosti, ki jo telefonska centrala s svojo notranjo zaščito zlahka vzdrži.

Značilno je, da pride do poškodb centrale, ki ima v zaščiti le plinske odvodnike, ko po cca letu in pol popusti notranja zaščita v centrali zaradi poslabšanja zaščitnih lastnosti vgrajenih elektronskih elementov zaščite.

Običajno se elektronske plošče v centralah ne popravlja ampak se menjajo v celoti. Zamenjave elektronskih plošč so v drugi vgradnji po garancijski dobi vsaj tri do štirikrat dražje, kot so take plošče v prvi vgradnji. Kot

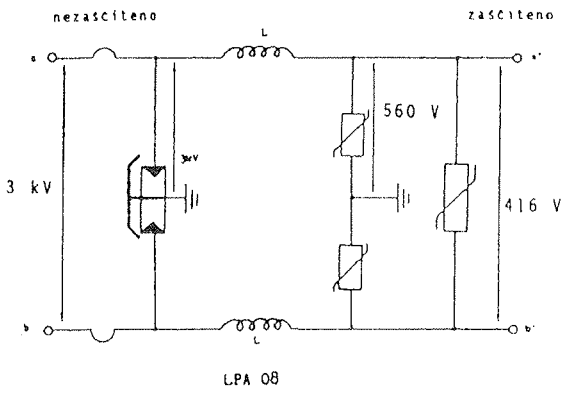


Slika 15: Visoke preostale napetosti pri enostavni zaščiti le z dvopolnimi plinskimi odvodniki na 5 kA impulz (8/20 μ sek)

rezervni deli ob prvem nakupu stanejo zaradi visoke integracije nekaj tisoč nemških mark, kasneje pa tudi pet do osem tisoč.

Kompleksna prenapetostna LPA 08 (lightning protection assembly) zaščita ima 13 stopenj zaščite z več notranjih plavajočih zemelj. Odziv je štirikrat hitrejši kot pri samih plinskih odvodnikih. Vmesni induktivnosti zadržita prvi škodljivi impulz z visoko induktivno upornostjo, ki je posledica hitrih sprememb električnih veličin na vgrajeni vmesni stopnji s tuljavo. Večstopenjsko delovanje nadomešča množico dragih ukrepov v zunanji in notranji zaščiti. Tako je navidezno višja cena kompleksne večstopenjske zaščite hitro poplačana, ker se število intervencij povsem zniža in je le malo izpadov dela centrale. Riziko izpada telefonske centrale je zmanjšan na minimum.

V primeru redko nastopajoče motnje stika telefonske linije z energetsko linijo 220 V deluje tokovno izmenična zaščita.



Slika 16. Ostale prenapetosti ob istem preizkusu kot na sliki 14 na kompleksnem zaščitnem modulu. Prenapetosti so padle na neškodljiv nivo.

Prva termična zaščita na plinskem odvodniku stali talilni vložek in stakne po nekaj sekundah plinski odvodnik kratko z zemljo. Tok, ki po predpisih CCITT K 20 zahteva 15 minut delovanja ob uporu 10 Ohm, bi pretvoril plinski odvodnik brez te zaščite v žareč kos keramike, ker deluje kot 9000 W peč, kar ima za posledico gorenje plastičnih delov na glavnem delilniku in možnost požara v centrali.

Druga termično tokovna zaščita s termoodvajali ščiti vodnike, da se ne smode, cede in da ne zagorijo. Medsebojna rezporeditev elektronskih elementov zaščite v kompleksnem prenapetostnem modulu ščiti vsak element v njem in zaščitni modul tako, da se nekaj 100-krat poveča življenjska doba najbolj šibkih elementov-členov v modulu.

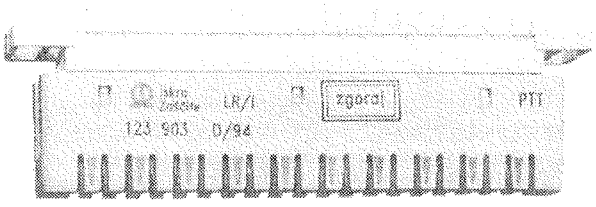
Da bi lahko dosegli zahtevo po visokih nominalnih odvodnih tokovih nad 10 kA 20 krat in stopenjsko zavarovanje elektronskih telefonskih naprav, smo v Iskri

Zaščite razvili novo družino prenapetostnih modulov v uporabo vseh navedenih elementov zaščit.

Istočasno smo razvili vse sestavne dele za glavni delilnik, ki je nosilec zaščite. Telefonske ranžirne in delilne letvice iz te družine so uporabne tudi v omaricah in razvodnih dozah.

Osnovne zahteve so bile brezplinsko tesnenje kontaktov vodnikov na letvici, sekanje vodnikov brez odstranjevanja izolacije in izvedba kontaktov brez lotanja ter zahteve po PTT predpisih. Dodatne nadstandardne zahteve so bile: izboljšana ozemljitvena upornost, visoka prenapetostna trdnost nad 4 kV za napetostni udarni impulz 1,2 / 50, vsaj 20 tokovnih udarov nominalnega 10 kA tokovnega voda (8/20), konkurenca garantira za zaščitne module 5 kA nominalne udare, namestitev ozemljitvene zbiralke v notranjosti letvice, da se izognemo snemanju vseh modulov pri ponovnih ranžiranjih, oblika zunanjega kontakta za priključene vodnike, ki omogoča vklapljanje stare in nove centrale brez prekinitve delovanja, izboljšane galvanske lastnosti kontaktnih površin, boljša protioksidacijska zaščita kontaktnih površin z dvojnim glavanskim postopkom, povišana stopnja samougasnosti plstičnih delov, višja obstojnost v agresivni atmosferi, hitrejša montaža z istočasnim rezanjem dveh vodnikov in zato posebej razvite montažne klešče, ostane rezanje enega vodnika, 8 linijska in 10 linijska oblika letvice.

Možna je le uporaba enostavnih, večstopenjskih enolinijskih zaščitnih modulov in zaščit za 10 linij hkrati. Za zaščitne module je Iskra Zaščite prejela v maju 1995 odločbo o podelitvi slovenskega patenta. Za letvico in izvedenke (ranžirna, ločilna, stikalna, ozemljitvena in označevalna) je patent v postopku.

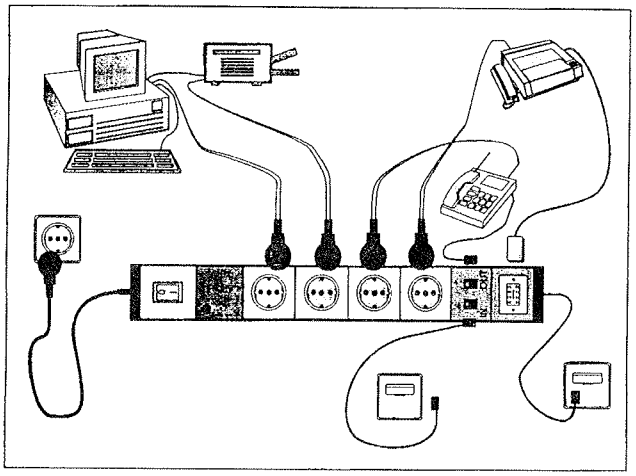


Slika 17: Slika nove telefonske letvice Iskre, ki skupaj z zaščitnimi kompleksnimi elementi vzdrži najmanj 10 kA impulze oblike 8/20 μ sek 10 krat.

S triletnimi razvojnimi prizadevanji na lastnih telefonskih letvicah in skoraj 10 letnimi na prenapetostnih zaščitah je omogočen kompleten asortiman ponudbe za telefonske centrale in mrežo s priključnimi in tranzitnimi omaricami ter terminale. Le finančno zahteven namensko opremljen laboratorij ter številne izkušnje in znanje omogočajo konkurenco na svetovnem nivoju kvalitete.

5. ZAŠČITA TELEFONSKIH TERMINALOV

Raznolikost telefonskih terminalov zahteva raznolikost terminalnih zaščit. Številne države zahtevajo, da motnje



Slika 18: Elementi prenapetostne zaščite v podaljšku za zaščito telefonskih terminalov v sodobni pisarni.

iz telefonske merže očisti organizacija, ki upravlja s telekomunikacijsko mrežo. Telekom drugje predpisuje zaščite, ki jih mora vgraditi porabnik. To opravijo z različnimi eno- ali večvratnimi elementi in moduli prenapetostne zaščite. Tretji zahtevajo visoko odporno notranjo zaščito pred strelo in drugimi motnjami.

Številne zahteve za zaščito terminalov izpolnjuje energetski podaljšek, v katerega so vgrajeni zaščitni moduli in plavajoča lokalna zemlja. Zaščiti lahko istočasno odvisno od števila in vrste vgrajenih zaščitnih modulov računalnik, monitor, telefon, brezžični telefon ali malo telefonsko centralo.

Ena izmed možnosti zaščit za sodobno pisarno je na sliki 18.

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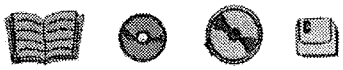

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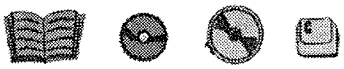

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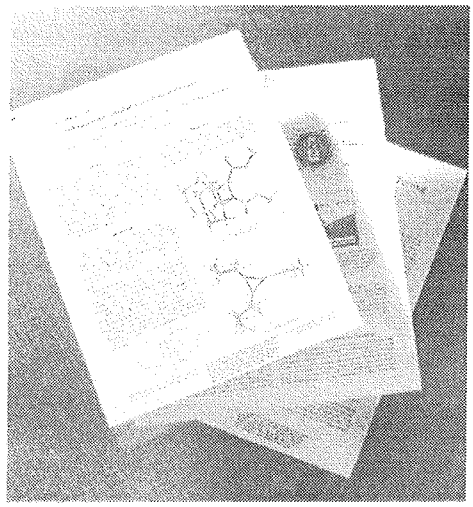

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VENDOR MANAGED SERVICES "A PARTNERSHIP FOR THE ENVIRONMENT"

Introduction

Hazardous Materials Management is a central issue for all semiconductor manufacturing operations. The hazards associated with the chemicals and gases used in the industry are significant, so the protection of employees, the surrounding community, and the environment must remain a primary focus. Accordingly, hazardous materials storage and handling practices are strictly regulated at the federal, state, country, and city levels. At SGS-THOMSON Microelectronics, Inc. in Phoenix, Arizona, an innovative approach to Hazardous Materials Management has been adopted. The concept is known as "Vendor Managed Services."

What is Vendor Managed Services?

Olin Electronic Materials' Chemical Management Services Group was selected to provide SGS-THOMSON with a comprehensive Hazardous Materials Management System. The mission statement governing Olin's commitment to SGS-THOMSON reads as follows:

"To assume total product accountability and ensure total product integrity for the chemicals utilized in our customer's fab."

Several basic functions have been identified and agreed upon as a part of the "Vendor Managed Services" contract. These functions represent Olin's responsibilities and can be divided into five major areas - chemical procurement, inventory management, equipment operation, waste disposal, and regulatory report preparation.

Olin is tasked with supplying all production chemicals at a guaranteed level of quality to the "point of use" in the fab. This includes alternate source selection, material delivery, unloading the materials from the truck, product quality inspection, and transferring the delivered items to appropriate chemical storage areas.

The chemical inventory is tracked and updated by Olin to minimize the quantities of chemicals stored on-site. All chemical containers are labeled with a bar code that is scanned in and out of the inventory system. When inventory levels fall below a predetermined minimum, the chemical is automatically reordered. This concept is known as "Just-In-Time" Materials Management and is preferred by our regulatory community.

Within their primary work area, Olin Technicians operate a variety of specialized equipment and respond to emergency situations, (e.g. chemical spills and leaks). For example, Chemical Delivery Modules CDM's) are used to pipe selected chemistries to the fab. Olin Technicians manage and maintain these bulk delivery systems. The monitoring of critical operating parameters of the plant's Wastewater Treatment System and Vent Scrubber Systems is another essential function performed jointly by Olin and SGS-THOMSON personnel. A "real time" assessment of the critical parameters is made possible by a computer software *system* called Datatrax. The Datatrax system uses transfer equations to convert data from analog and digital instruments located throughout the plant into numeric and graphic displays. In the Wastewater Treatment Plant, the pH of the neutralization tanks, total dissolved solids, tank volumes, gallons per minute of flow, and fluoride levels are tracked and recorded. Datatrax looks at pump flow, differential pressure, pH and total dissolved solids for the wet scrubber system. In addition to its monitoring and record-keeping capabilities, Datatrax is equipped with an automated alarm and paging function. Predetermined control limits for a chosen parameter are programmed into the computer. If at any time the control limits are breached, the computer pages appropriate SGS-THOMSON and Olin technicians to respond to the area where the problem was detected. Employing Vendor Managed Services to monitor these critical parameters affords SGS-THOMSON extended coverage essential to our operations.

All activities associated with waste disposal are under the direction of Olin's Chemical Management Services. An Environmental Services Engineer from Olin has been assigned to SGS-THOMSON to prepare waste profiles, arrange for the analysis of samples, select the appropriate Treatment, Storage, and Disposal Facilities (TSDF), schedule waste shipments, and prepare and maintain all necessary documentation. The Environmental Services Engineer is responsible for the preparation of waste-related regulatory reports and is available to assist SGS-THOMSON with the preparation of required programs addressing pollution prevention and waste minimization. Currently, the Engineer is developing a comprehensive waste management program to include the recycling/reuse of targeted waste streams, such as sulfuric acid, hydrofluoric acid, mixed solvents, empty glass and poly bottles, drums, as well as packaging materials. Olin Technicians inspect our waste storage area on a weekly basis to ensure that our drums are properly labeled, securely closed, and in good condition. And finally, personnel from Olin's Corporate Environmental Department provide additional knowledge and resources to SGS-THOMSON whenever a need is identified.

Why Choose Vendor Managed Services?

A variety of benefits have been attributed to hiring a vendor to provide chemical management services. They include environmental advances, safety enhancements, improvement of quality and financial savings.

Environmental Advances

- Increased recovery/recycling capabilities
- Application of "Best Available Technology" for Waste Disposal
- Improved auditing of Treatment, Storage & Disposal Facilities
- Comprehensive monitoring of Pollution Control Equipment

Safety Enhancements

- Decreased frequency of crisis shipments
- Reduced quantities of hazardous materials on-site
- Avoidance of accidents caused by inexperienced personnel
- Increased materials handling efficiency

Quality Improvement

- Controlled monitoring of supply streams
- Customer yield improvement
  - Line yield from fewer interruptions
  - Increased up time of the chemical distribution system
  - Reduced scrap loss
- Enhanced quality control and R & D efforts

Financial Savings

- Decreased internal labor resources and supervisory time dedicated to chemical management
- Reduced overhead and shortened cycle time
- Elimination of excess costs with the introduction of "Just-In-Time" inventory methods
- Increased efficiency in transportation and handling functions

Conclusion

SGS-THOMSON Phoenix believes that the benefits of "Vendor Managed Services" for Hazardous Materials Management are numerous. Olin Electronic Materials is a manufacturer of chemicals offering a wealth of experience, technical information, and resources. Forming a partnership with Olin's Chemical Management Services Group has provided SGS-THOMSON with the ability to focus on our primary objective - "to be the best 8 inch wafer manufacturing fab in the world".

Written by
Peg Goodrich
Environmental Engineering Specialist
SGS-THOMSON Microelectronics, Inc.
and Frances Lupoe
Environmental Services Engineer
Olin Electronics Materials Division
June 1995

PREDSTAVLJAMO PODJETJE Z NASLOVNICE

SEMCOTEC, Austria

Semcotec's Quad Channel Line Interface Circuit Kit QuadCLIC

The Semcotec development is unique worldwide and represents an integrated complete chip-set for four channel voice and signalling data generation and transmission based on a QuadCOMBO, QuadSLIC plus two other chip types: DualPower and RingDriver.

The heart of the chip-set is composed of:

- the 4-channel-Combo or QuadCOMBO on a single chip

and

- the 4-channel-SLIC or QuadSLIC on a single chip

combined with DualPower and Ring Driver chips to form the QuadCLIC.

The name CLIC is the acronym for Complete Line Interface Circuit. Based on the 4-channel-solution it is called the QuadCLIC.

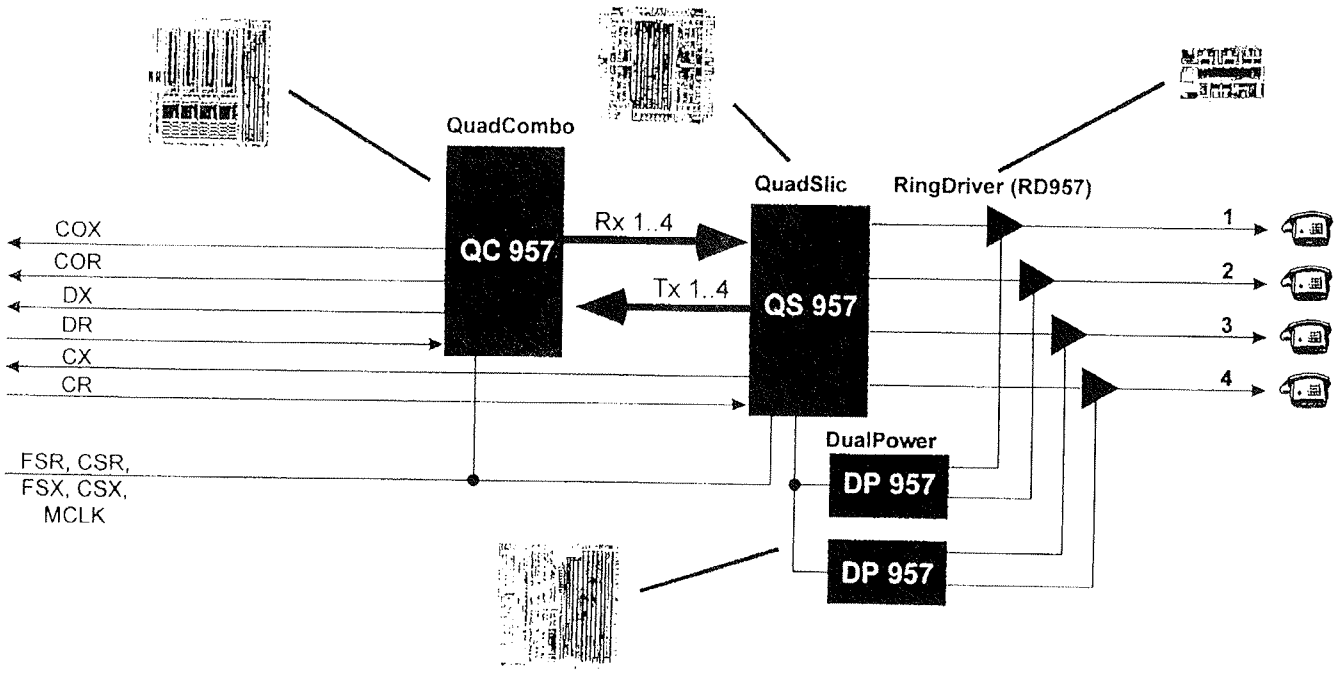
These chips are shown as core or heart of a wide variety of most advanced telecom applications, making these applications easier and by far more cost effective than using solutions based on standard products or chips from other manufacturers.

Remote Maintenance and Service Features

The QuadCLIC chip-set interfaces analog telephone subscriber or corresponding terminal equipment in applications like Pair Gain, PABX (Private Automatic Branch Exchanges), Rural Exchanges and Concentra-

Semcotec's Quad Channel Line Interface Circuit Kit - QuadCLIC

Core of all Applications



tor systems with increased technical performance and reductions in components count and manufacturing costs compared to other solutions.

The **QuadCLIC Kit QK 957** offers advanced control and maintenance features, providing capabilities to monitor the subscriber loop and the CLIC status itself.

The maintenance and service communication is handled completely digital via the serial control status links to the QK 957, either directly in analog line cards or through the ISDN interface D-channel protocol in pair gain systems.

The respective QK 957 serial protocol has an easy access to an external controller for remote line status supervision, analysis and data logging.

The serial control status link delivers continuously information about the subscriber loop and the CLIC operation, up-dated with 8 kHz.

The received digital codes with 8 bits per channel can be processed by the system control computer as LEGAL and ALARM types, depending on the line's operational modes like IDLE, RINGING, or TALK.

Multiple usage of existing cabling

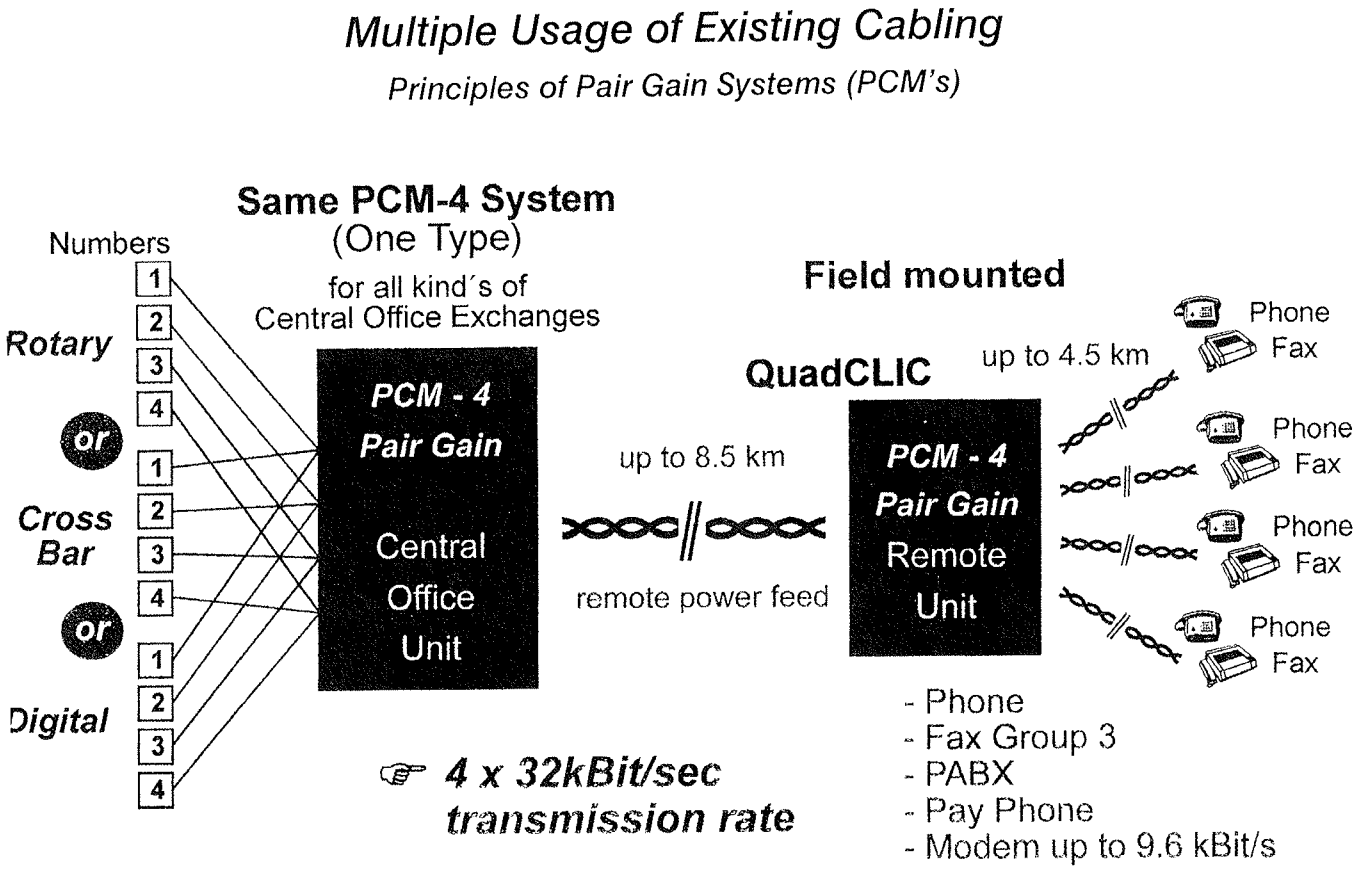
The following describes the principles of a state-of-the-art digital transmission system using just one standard telephone twisted pair copper wire for four fully independent voice and/or data transmissions without any correlating interference during simultaneous transmission between the Central Office and four subscribers.

This System - the first application for the QuadCLIC circuitry - is called ***PCM-4*** (from Pulse Code Modulation).

Principles

1. The system consists of the CENTRAL OFFICE UNIT, a printed circuit board (pcb) mounted together with other CO Units in a 19-inch-rack in the Central Office near to the mechanical or electronic exchanges and
2. the REMOTE UNIT installed in home or office-buildings, on poles, or other field mounting possibilities.
3. The CENTRAL OFFICE UNIT can operate with mechanical, half-electronic or fully digital exchanges.
4. To the CENTRAL OFFICE UNIT are connected the four call numbers from the CO exchange and the CO exchange battery supply.
5. The REMOTE UNIT is a small printed circuit board mounted in a steel, aluminum or plastic casing for outside installation.

The choice of casing material and the casing itself depends on the environmental conditions and the requirements of the domestic PTO's (Post Telegraph Organization).



The Remote Unit is connected by **A SINGLE** wire pair to the CO Unit and by four wire pairs to the four subscribers, phone sets, or faxes as shown.

The Remote Unit does **NOT NEED ANY INTERNAL BATTERY OR OUTSIDE POWER CONNECTION.**

The power to the Remote Unit is fed over the same wire pair used for the voice and data transmission from the CO Unit.

Operating Details

All transmissions are fully simultaneously bi-directional and fully digital in accordance to CCITT G.712 and Q.552 recommendations.

That means all chips used in the data and signal streams work fully bi-directional with data and signal streams in both directions at the same time. All chips are strictly designed in accordance to CCITT.

1. The CENTRAL OFFICE UNIT

1.1. takes the analog signal of the 4 call numbers from the exchange,

1.2. converts into digital data streams with 64kBit/sec per channel,

1.3. compresses each of these data streams to 32 kBit/sec using a standard ADPCM algorithm according to CCITT G.726,

1.4. and transmits these compressed data streams via the so-called ISDN (Integrated Services Data Network) U-Interface chip (terminus technicus) together with signaling information, like ringing, teletax or callfee impulses, polarity reversal and loop state (onhook/offhook condition) over just ONE standard telephone twisted pair copper wire to the REMOTE UNIT.

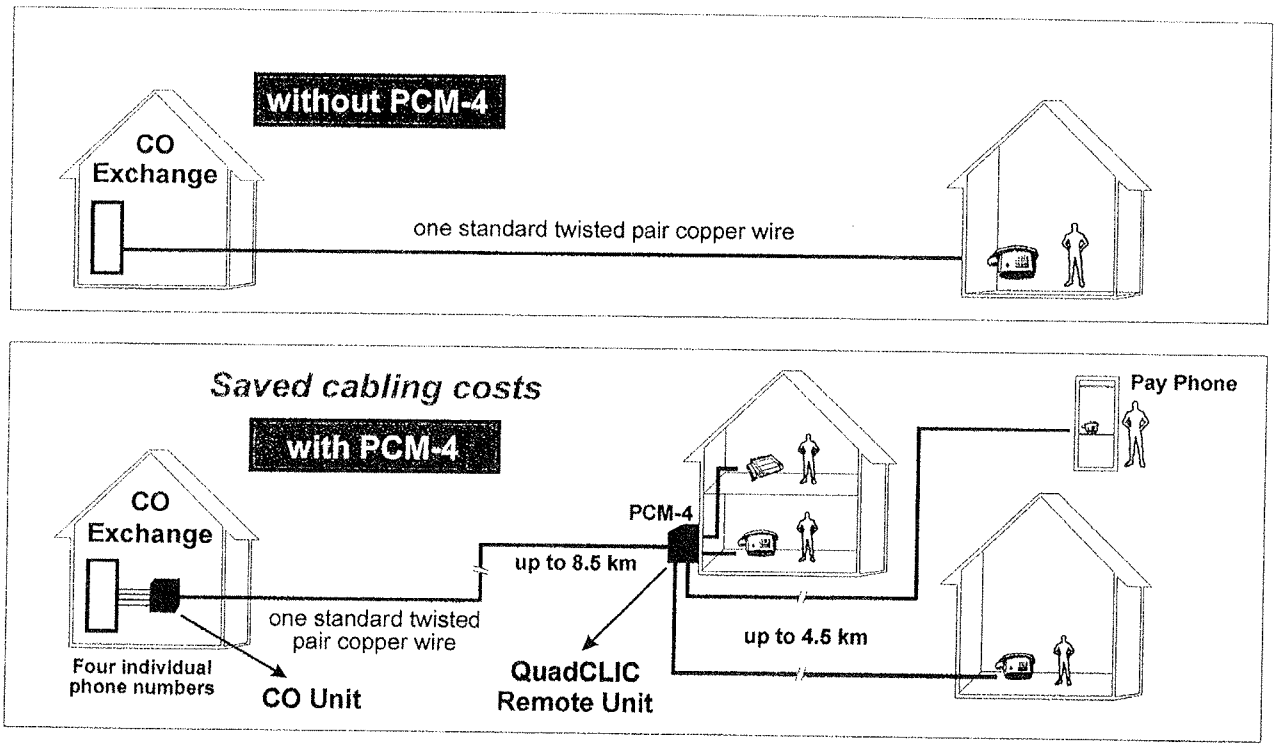
2. The REMOTE UNIT

2.1. receives the incoming signals from the CO Unit through the U-Interface chip,

2.2. de-compresses the channel-signals back to 64kBit/sec via the ADPCM,

2.3. converts the channel data from digital to analog signals via the QuadCOMBO,

Multiple Usage of Network Cabling



These figures show a comparison between a usual "one call number, one wire and one subscriber connection" and the expanded possibilities of four call numbers connected through the CENTRAL OFFICE UNIT and just ONE wire to the REMOTE UNIT - built with one QuadCLIC circuitry - and from there on to FOUR completely independent subscribers.

In this example are shown: Phone sets, fax, and a public telephone box or pay phone, the latter an important feature in some installations.

2.4. refines the analog channel signals assigned to the respective Central Office call numbers via the SLIC functions and connect the signal to the subscriber terminal equipment, for instance telephone sets or fax.

This functionality uses the same principles vice versa for the data streams from the subscriber to the Central Office.

Technical and Commercial Details

The distances shown - 8.5 km CO to Remote Unit and 4.5 km, Remote Unit to subscriber - are not only defined by the CCITT transmission standard used and implemented in the U-Interface chip, but also by the wire diameter and the physical conditions of the telephone wires in the connection.

The experience of Semcotec shows no difficulties with respect to the latter conditions :

PCM-4's have been installed under worst case conditions in cabling networks, having parts more than 50 years old.

Distances up to 10 km are possible with wire diameters of about 0.6 to 0.8 mm in good conditions.

In urban areas the average requested distance is around 2 to 3 km.
The cost saving is clearly given by the possible multiple usage of wires. Only one wire is needed for 4 call number connections in PCM-4.

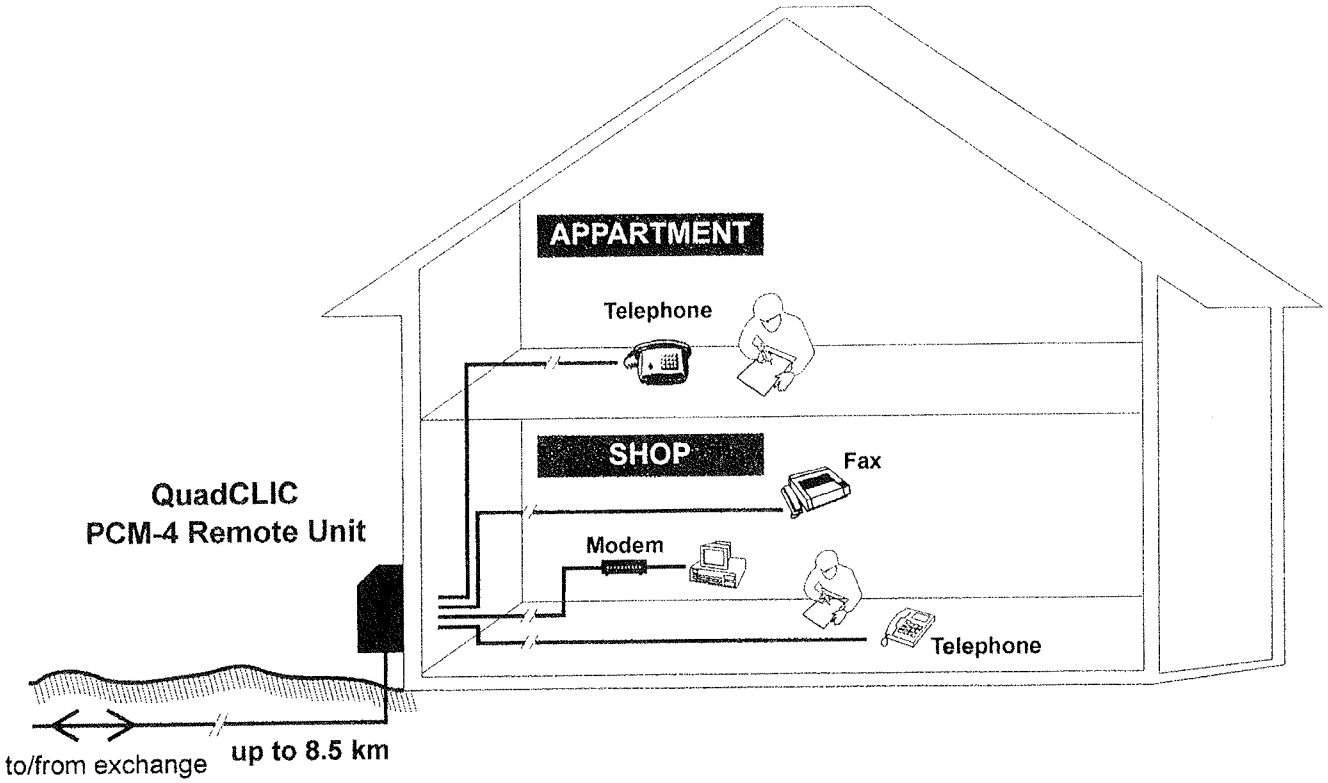
PCM-4 Remote Unit

Schematic

As described previously the QuadCLIC circuitry is the core of a wide variety of telecom applications, as part of the PCM-4, in the field of voice and data transmission. As previously shown, the PCM-4 exists of the CENTRAL OFFICE UNIT and the REMOTE UNIT.

This figure illustrates the Semcotec Integrated Remote Unit, designed with the QuadCLIC as the master circuitry. Shown are the principles with the incoming wire from the Central Office (right side) and the complete circuitry of the high integrated Semcotec PCM-4 Remote Unit from right to left:

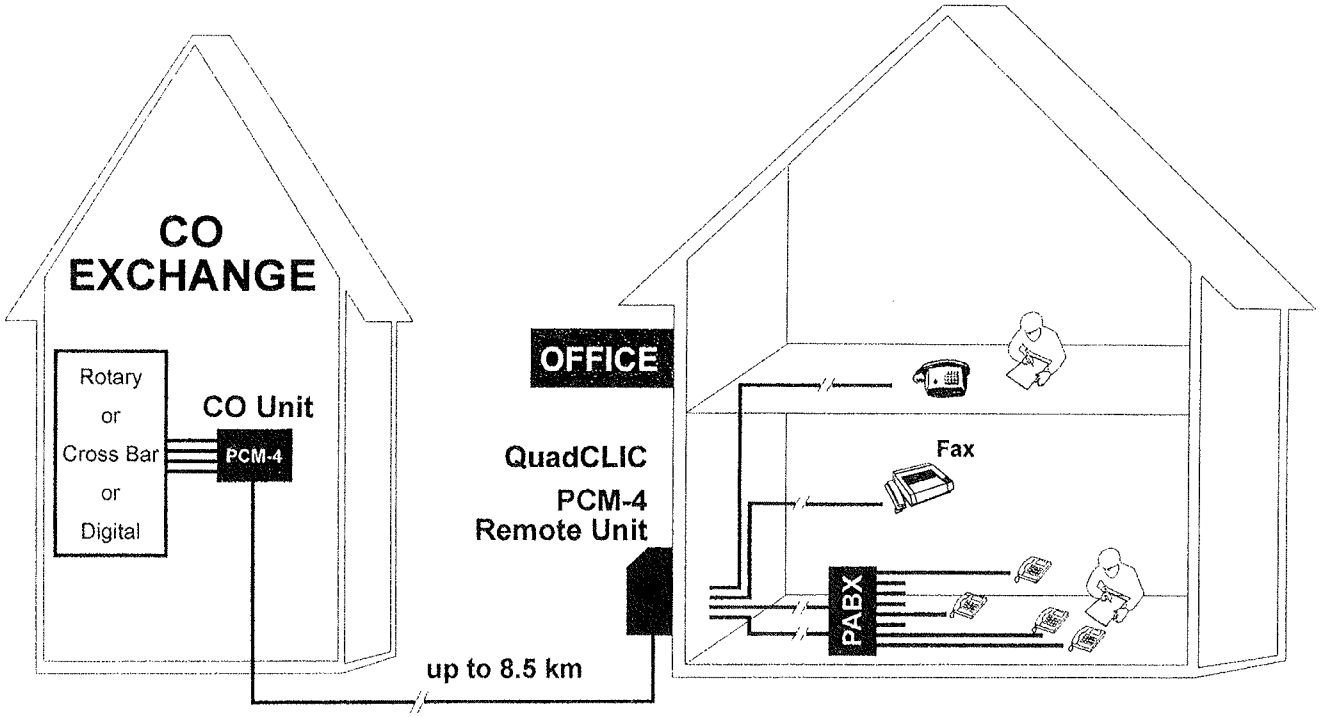
Typical PCM-4 Application



In this figure are again connected FOUR subscribers in one building demonstrating the usage of four call numbers for private, and business applications.

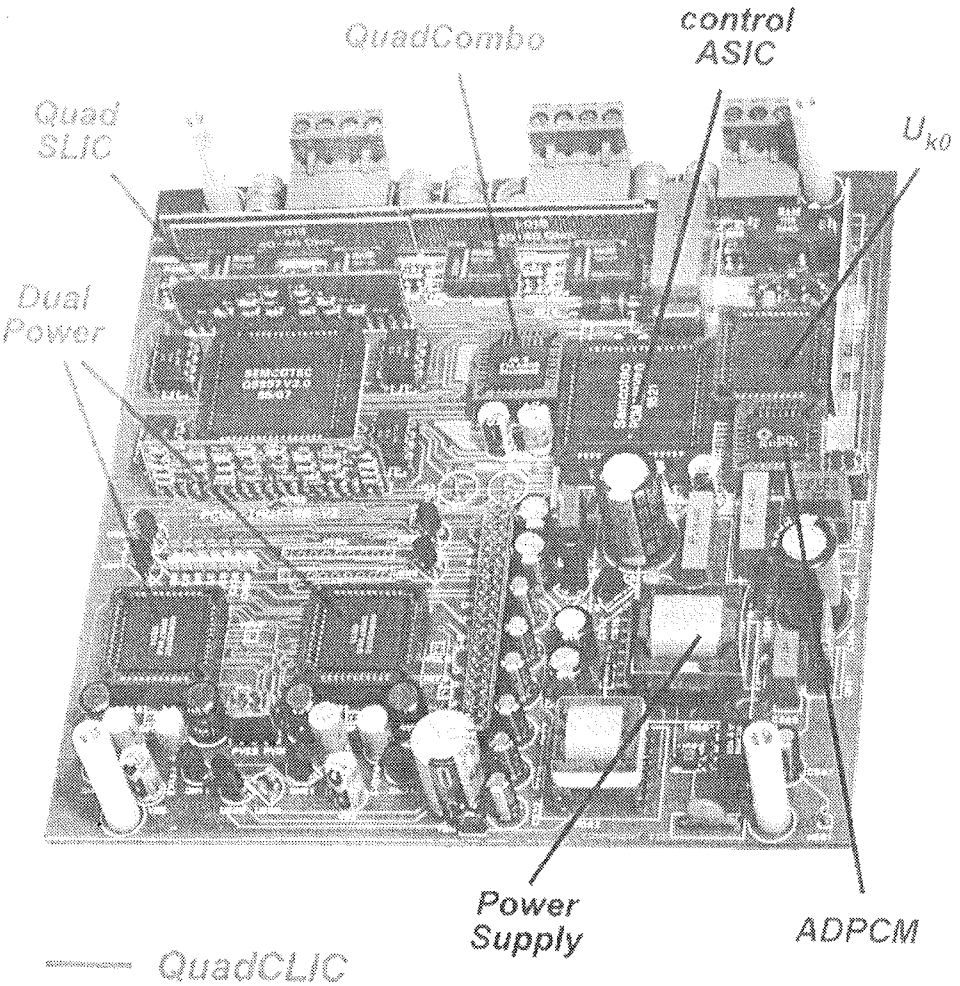
Added is a possible Modem transmission.

Rural Area with PABX Application



PCM-4 Integrated Remote Unit

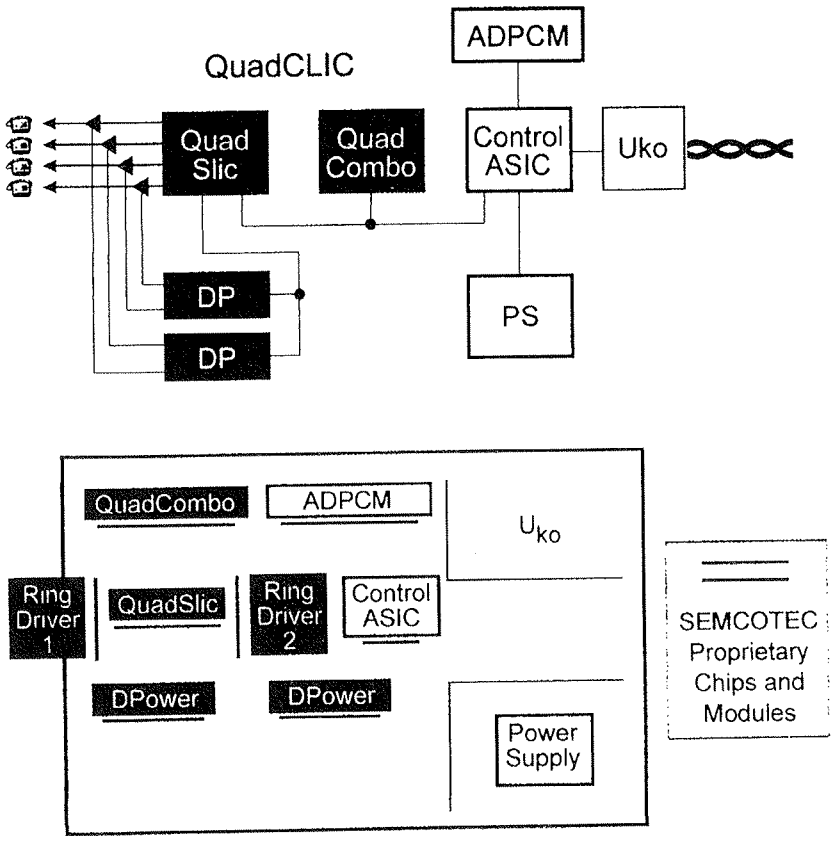
shows fully assembled printed circuit board chipside (two layers only)



PCM-4 Remote Unit

Schematic

SEMCOTEC Integrated Version



U_{ko} = U-Interface chip

This chip, in accordance to CCITT and ISDN standards is a modem circuit for full duplex 144kBit/sec transmission rate and echo cancellation.

ADPCM = Adaptive Digital Pulse Code Modulation chip

This device performs the function of compressing and de-compressing the data channels in accordance to CCITT from 64kBit/sec to 32kBit/sec and vice versa. The chip works fully bi-directional. The kBit-rate of 64kBit/sec is part of the so-called ISDN standards, where ISDN means Integrated Services Data Network.

Within this standard either 4 channels with compressed 32kBit/sec can be handled, which means PCM-4 or 2 channels uncompressed with 64kBit/sec are possible, the latter means **PCM-2.**

Semcotec offers its own 8-channel ADPCM chip in 1995.

Control ASIC (Application Specific Integrated Circuit)

This chip controls the main part of the data flowing in the Remote Unit.

The Chip is designed and supplied by Semcotec.

PS means Power Supply Module

This unit, which is designed as a DC/DC-converter takes the operating voltage via the telephone wire from the Central Office Unit - by Remote Power Feed. It generates - with a very high efficiency - all necessary voltages and currents for the operation of the Remote Unit circuitry as well as the connected four telephone sets, for complete simultaneous parallel ringing and talking.

The Power Supply Module is designed by Semcotec for this specific application.

QuadCLIC

The set consists of QuadCOMBO, QuadSLIC, Dual Power's and four Ring-Drivers as explained earlier.

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KONFERENCE, POSVETOVANJA, SEMINARJI, POROČILA

Poletna šola o tehnologiji materialov za feroelektrične mikrosenzorje, mikroaktuatorje in mikroelektronske komponente

Lausanne, Švica, 28. 8. - 1. 9.1995

V času od 28. avgusta do 1. septembra 1995 sva sodelovala na poletni šoli "Summer school on materials technology for ferroelectric microsensors, microactuators and microelectronic components" na Visoki politehnični šoli (Ecole polytechnique federale de Lausanne) v Lausanni, Švica.

Program poletne šole je bil razdeljen na dva dela, ki sta vsebovala tako predavanja kot tudi laboratorijske vaje.

Vprvem delu so predavatelji predstavili osnove feroelektričnosti, piezoelektričnosti in piroelektričnosti tako v keramiki kot v tankih plasteh, osnove meritev ter piezo- in piroelektrične elemente.

Dr. Enrico Colla je v predavanju o fenomenologiji fero-, piro- in piezoelekričnosti predstavil fazne prehode, ki so osnova navedenim pojavom, s stališča termodinamike. S pomočjo Landau-ove teorije je razložil, kdaj so izpolnjeni termodinamski pogoji, pri katerih lahko makroskopsko merljiv efekt razložimo z mikroskopskimi modifikacijami v materialu. Na podlagi rezultatov lahko napovemo, v katerih kristalnih razredih lahko pričakujemo simetrije, ki so pogoj za fero-, piezo- in piroelektrični odziv v materialu.

Dr. Dragan Damjanovič je v predavanju o piezoelektričnih elementih najprej predstavil sistem piezoelektričnih meritev, nato pa razložil razlike med meritvami monokristalov, keramike (vpliv orientacije domen) in tankih plasti (vpetost vzorca na podlago). Poleg tega je predstavil delovanje piezoelektričnih motorjev, hidrofonov in aktuatorjev.

Dr. Aleksander Tagantsev je v predavanju o tankih plasteh podal pregled fizikalnih pojavov, ki vplivajo na ferroelektričnost tankih plasti in razložil razlike v obnašanju keramike in keramičnih tankih plasti. Razložil je obnašanje feroelektrika v električnem polju, pojav dielektrične plasti ob elektrodi, polprevodniški značaj te plasti in vpliv defektov na premik domen.

Dr. Christian Wuthrich je imel predavanje o piroelektričnih elementih, v katerem je podal pregled optimiranja in modeliranja piroelektričnega senzorja ter priprave večplastnih struktur z metodo mokrega jedkanja in erozije.

Pri laboratorijskem delu so predavatelji pokazali meritve omenjenih količin pri keramiki in tankih plasteh. Med demonstracijami je bilo dovolj časa za razgovor o izvedbi meritev, o eksperimentalnih problemih (vpenjanje vzorca, kontakti) in virih napak.

V drugem delu poletne šole smo se seznanili z različnimi postopki priprave in s karakterizacijo ferroelektričnih keramičnih tankih plasti. Poleg tega so predavatelji predstavili tudi postopke izdelave mikroelektronskih komponent (senzorjev, aktuatorjev, motorjev, črpalk, ...).

Dr. Paul Muralt je v predavanju o pripravi tankih plasti podal pregled najpogosteje uporabljenih materialov in njihove lastnosti ter pregled metod za nanašanje keramičnih tankih plasti. Poudaril je pomen kompatibilnosti materialov pri integraciji na silicijeve rezine in nadaljnje procesiranje večplastnih struktur.

Dr. Marija Kosec je v predavanju o pripravi tankih plasti s poudarkom na sol-gel kemiji razložila potek reakcij v postopku sinteze in pregled sintez za pripravo P(L)ZT tankih plasti. Dr. Keith Brooks je v nadaljevanju poudaril, da na kvaliteto in orientiranost plasti ne vpliva le kemizem pri sintezi sola, pač pa tudi elektrodni material in termična obdelava.

Dr. Enrico Colla in dr. Andrei Kholkin sta razložila modele degradacije in pojav utrujenosti v ferroelektričnih tankih plasteh.

Dr. Georges Racine je predstavil prototipe mikromotorjev in postopke izdelave, Dr. Philippe Lerch pa uporabo računalniškega programa ANSYS za simulacijo delovanja piezoelektričnih elementov.

V praktičnem delu je vsak udeleženec pripravil keramično tanko plast po sol-gel postopku in izvedel električno karakterizacijo vzorca. Ogledali pa smo si tudi delo v laboratorijih za pripravo elektrod (sputtering) in obdelavo večplastnih struktur (micromachining).

Prof. Nava Setter je v sklepnem predavanju predstavila področja raziskav in usmeritve pri izdelavi računalniških pomnilniških elementov. Poudarila je trenutne pomanjkljivosti, predvsem zanesljivost, zaradi katerih je uporabnost keramičnih tankih plasti še omejena. Nadaljnje raziskave bodo predvidoma na področjih piroelektričnih aplikacij, računalniških spominov in piezoelektričnih elementov v mikro- sistemih.

dipl.ing. Uroš Delalut
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Osma mednarodna delavnica o steklih in keramiki iz gelov

Faro, Portugalska, 18. - 22. 9.1995

Osma mednarodna delavnica o steklih in keramiki iz gelov (8th International Workshop On Glasses And Ceramics From Gels) sodi v serijo konferenc o dosežkih in razvoju znanosti in tehnologije sol-gela. Predhodne konference so potekale v Padovi (1981), Montpellierju (1985), Kyotu (1987), Rio de Janeiru (1989), Sevilli (1991) in v Parizu (1993). Konferenca je potekala v mestu Faro na jugu Portugalske, organizirala pa jo je skupina profesorja Rui Almeida iz Oddelka za materiale Tehniškega instituta v Lisboni. Sodelovalo je približno 250 udeležencev iz 30 držav.

V enajstih sekcijah (kemija sol-gel procesov, struktura in lastnosti gelov, sintranje in kristalizacija gelov in tankih plasti, prevleke in membrane, hibridi in nanokompoziti, biomateriali, električno aktivni materiali, aerogeli in katalizatorji, aktivni optični elementi, nelinearna in integrirana optika, nove usmeritve in aplikacije) je bilo predstavljenih približno 300 prispevkov. V sekciji o strukturi in lastnostih gelov smo sodelovali z delom Študij alkoksidnih prekurzorjev keramike na osnovi $PbZrO_3$-$PbTiO_3$ avtorjev Barbare Malič, Iztoka Arčona, Marije Kosec in Alojza Kodreta.

Sol-gel sinteza se je uveljavila na področju priprave stekla, steklo-keramike, monolitov, steklenih in keramičnih vlaken, zaščitnih prevlek, kompozitov in tankih plasti. Bistvene prednosti sol-gel sinteze glede na klasične postopke so homogenost, čistost in nižje temperature priprave.

Po alkoksidnem sol-gel postopku lahko sintetiziramo tudi keramične prahove. Predvsem za elektronsko keramiko, ki je tipično večkomponentna, je doseganje večje homogenosti in nižjih temperatur priprave, ki so posledica manjše velikosti delcev, izredno pomembno. Zato se precej keramičnih laboratorijev ukvarja s sintezo submikronskih neaglomeriranih prahov za piezokeramiko, superprevodnike, ferite. Na področju feroelektričnih tankih plasti, pripravljenih po sol-gel postopku (PZT, PLZT), so raziskave usmerjene v potek kristalizacije in možne reakcije plasti z elektrodo (Pt) in podlago.

V sklepnem predavanju konference je prof. D. Uhlmann na podlagi ankete med 50 raziskovalci s sol-gel področja napovedal, da so "naj" materiali prihodnosti, sintetizirani po sol-gelu, optične prevleke na osnovi silicijevih alkoksidov, SiO_2 aerogeli kot izolacijski materiali in prahovi za elektronsko keramiko. Problem keramičnih prahov je po njegovem mnenju predvsem prenos v proizvodnjo.

Naslednja konferenca bo čez dve leti v Sheffieldu, Velika Britanija, v organizaciji profesorjev Angele Seddon in Petra Jamesa iz Univerze v Sheffieldu.

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VESTI

NEWS FROM AMS

Notification of improvement of the intermetal insulation of 1.2μ., 2μ, and 3 μ processes

As part of the AMS continuous improvement programme, the company has revised the intermetal oxide layer introducing an undoped oxide underlayer. The advantages are:

- Increased layer uniformity and step coverage
- Perfect sealing of metal-1 lines
- Enhanced stress buffer capability to metal-1
- Unchanged electrical process parameters

The new oxide step is deposited on the same equipment as before but improved by an undoped oxide layer. The total thickness of the intermetal oxide remains the same.

For further information please feel free to contact us.

New Laser Beam now operational at AMS

AMS announces that its new high performance ETEC Argon scanning laser beam pattern generator was put into operation this week. The laser beam generator, made in Oregon, USA, combines innovative hardware and software advances with high speed raster graphics and precision optics the result of which is a high performance system optimized to write both the high precision masks and reticles required by today's high performance and complex ASICs (Applications Specific Integrated Circuits).

The advantage for AMS is that this laser beam generator has the highest throughput currently available in the industry - with its 8 independent parallel writing split beams (200mW) it can complete a mask within approximately one quarter of the time required by the traditional E-beam generator used by AMS up to now.

Furthermore, because of its extremely high precision overlay accuracy of 100 nm and its ultra low defect density which is 100 times better than that of an E-beam generator this is a further step towards increased quality at AMS. Since this new equipment exposes geometries of down to 0.5 micron it will be utilized well into the turn of this century at AMS.

Note: A laser beam is used for writing geometries, the final layout pattern of an integrated circuit, onto a Chromium plated quartz glass referred to as mask. The mask in turn is used for exposing the silicon wafer and thus transferring this layout pattern onto the wafer. A set of up to 18 masks are required for the completion of an average wafer.

The Third Quarter 1995

Austria Mikro Systeme International AG (AMS) reports its third-quarter results (Results of AMS AG without consolidation of SAMES):

	1-9/1995 in Mill. ATS	1-9/1994 in Mill. ATS	Change in %
Order Entry	1,326	1,285	+3
Net Sales	1,349	752	+79
Backlog (Sept.30)	724	962	-25
Capital Expenditure	209	240	-13
Employees (Sept.30)	705	647	+9
Profit on Ordinary Activities	220	73	+201

While the profit on ordinary activities corresponded with the net income in the first three quarters as well as for the whole of 1994 AMS will be subjected to taxation in the course of the second half of 1995 - as discussed in the shareholder's report for the first half of 1995 - and this will reduce the OVFA results accordingly.

Mr. Horst Gebert, President and CEO: *"Customers have realized the new potential of AMS and now view the group as an equal partner to the large international semiconductor manufacturers because of the participation with Sames and the reduced delivery times as a result of this participation. The increase in new engineering projects of over 50 % in the third quarter secure the long term competitiveness of AMS and confirm the new situation."*

AMS is technology partner of the European Union for the new SHAPE Project (**Sub Half** Micron CMOS **P**rocess for **E**uropean Users) together with SGS-Thomson, Philips, Siemens, Alcatel-Mietec, GEC-Plessey and Matra-MHS for the development of the next generation of integrated circuits with process structures of <0,5 micron, which will determine the semiconductor technology after the turn of the century.

Mr. Johann Stritzelberger, CFO: *"Shorter delivery times for new projects and orders* - an *important sales argument in the ASIC business* - *are reflected in the order entry and backlog with an increase in sales* of 79 % *at the same time. The delivery restrictions of AMS will be systematically reduced because of the new possibilities of the* AMS *group."*

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CMP introducing low-cost microsystems prototyping

All market studies agree that the market of microsystems is expected to boom, driven by more and more applications on automotive, medical, process industries, and aerospace. One way to make this technology available to many designers, i.e. to move the technology from the specialized research laboratories to the commercial market is to offer low cost prototyping and small volume production by applying the same principles as those applied 15 years ago for integrated circuits: a multi-project wafer (MPW) approach, where the cost of a wafer is shared among multiple users.

CMP is introducing Micro Electro Mechanical Systems (MEMS) fabrication based on CMOS 1.0 m. DLM/SLP front side bulk micromachined by EDP at ESIEE. MEMS like cantilevers, membranes, microbridges, etc... may be processed together with the electronics. Design rules have been defined, available to designers upon signature of a Confidentiality and Licence Agreement (CLA). A CADENCE OPUS design kit is available to allow the generation of the layout including electronic and non-electronic parts. The kit includes an extended DRC and an extended parameter extractor (from layout to netlist) distinguishing electronic and non-electronic parts. A netlist is generated allowing an electrical simulation where bridges, cantilevers and membranes are considered as a resistance, and a behavioural simulation where these structures are represented by a model in the language HDLA/ELDO from ANACAD. Other CMOS processes, surface micromachining, GaAs processes, LIGA, Quartz micromachining will be introduced gradually.

The cost of the service is 1500 FF/mm^2, 15 samples being returned to the user, which is affordable even by small companies.

The design rules, the design kit including extended DRC and extended extractor, as well as a basic library are available.

B. COURTOIS, Director of CMP, said that *"introducing microsystems, CMP will contribute to the development of this market, as CMP contributed to the development of integrated circuits 15 years ago when CMP pioneered MPW service for microelectronics. There are 2 conditions to the development of that market: a low-cost access to prototyping, and CAD tools. CMP is greatly contributing to both issues, by extending fabrication and design facilities well known to present IC designers. To make use of infrastructures that were developed 20 years ago for microelectronics will allow economy of*

scale and thus push microsystems from research laboratories to a massive commercial market. CMP is proud to represent the European effort in this approach, since presently only USA have introduced it with ARPA and MOSIS efforts. CMP is pioneering the efforts here, as it was a pioneer in Europe 15 years ago".

J. PERRIN, Director of Group ESIEE, said: *"The industrial equipment of ESIEE includes 300 m^2 of 10.000 and 100 class clean rooms fully equipped for IC manufacturing and microsystem technology. That equipment includes furnaces, LPCVD, PECVD, contact optical aligners, double-side aligner, anodic bonding, silicon direct bonding, anisotropic wet chemical silicon etching, plasma RIE. ESIEE is thus very well prepared to work with CMP on the development of microsystems by offering a professional post-processing facility".*

Cost:

- 1 500 FF/mm^2, 5 mm^2 minimum charge.
- 15 samples returned including 5 samples packaged.

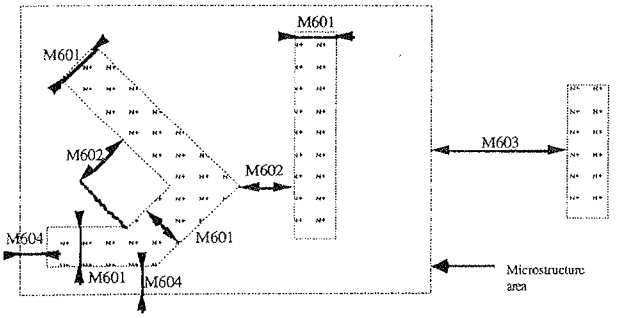
Documents and files available upon request:

- CMP Micromachines Program (October 1995).
- ES2 CMOS 1.0 m Front-side Bulk Micromachining Design Rules, upon signature of a CLA.
- Design kit including extended DRC and extended extractor, upon signature of a CLA.
- Cell library, being continuously expanded, upon signature of a CLA.

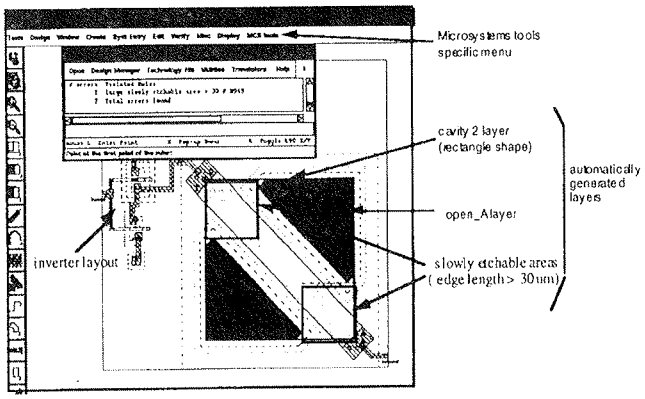
See samples overleaf.

Next runs:

- 7 December 1995
- 19 February 1996
- 9 April 1996
- 17 June 1996



Design rules example

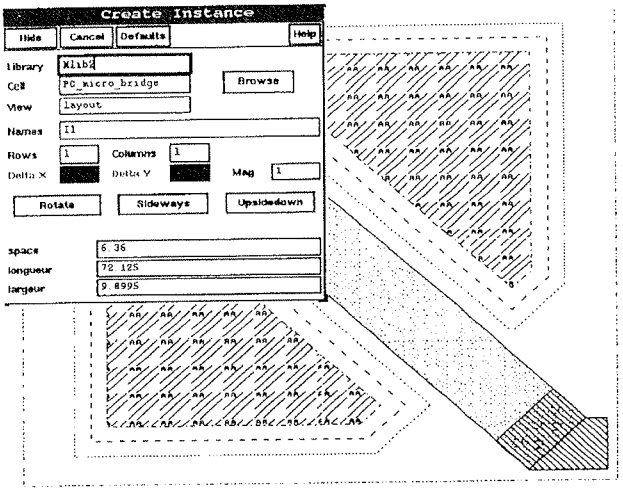


Design rules checking: prediction of a post-process etching problem

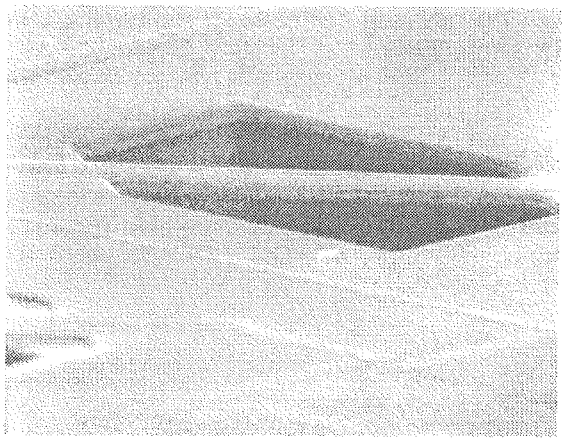
layer: 60.

name: N+IMPLANT.

Rule Number	Parameter	min. dimension
M601	width of N+ implant	1.5
M602	spacing between 2 areas of N+ implant	2
M603	spacing to microstructure area	5
M604	margin to microstructure area	1
M605	neither N+ implant pin nor N+ implant net is allowed inside microstructure area: N+ implant must not be used for interconnections inside microstructure area	



Instanciation of the micro-bridge parameterized cell



The micro-bridge obtained by front side bulk micromachining

CMP is a broker for a number of technologies (prototyping and low volume production). Since 1981, 140 Institutions from 30 countries have been served. More than 1600 projects have been prototyped through 130 runs, 15 semiconductor houses have been interfaced.

- ***Integrated circuits***

  1.2 μ,1.0 μ, 0.7 μ CMOS DLM from ES2
  1.2 μ, 0.8 μ CMOS DLP/DLM from AMS
  1.2 μ, 0.8 μ BiCMOS DLP/DLM from AMS
  0.5 μ CMOS TLM from SGS-Thomson/France Telecom (JESSI)
  0.6 μ GaAs from VITESSE
  0.2 μ GaAs HEMT from PHILIPS (up to 90 Ghz)

- ***Micromachining***

- ***CAD software:***

  CADENCE, COMPASS, VIEWLOGIC, TANNER, ...

- ***MCM and 3D packaging***

  MCM-L and MCM-LD from Montpellier Technologies/IBM
  MCM-C (HTCC) from Montpellier Technologies/IBM
  MCM-C (PCM, LTCC, Thick/thin film on alumina) from DASSAULT Electronique/SOREP
  3D-MCM (MCM-V) from Thomson-CSF DOI.

- ***Design kits:*** *available from most of the processes to*:

ALLIANCE	MDS
DOLPHIN	SYNOPSYS
MAGIC	COMPASS
MENTOR GRAPHICS	TANNER
CADENCE	VIEWLOGIC
EXEMPLAR	

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Electronics, February 1995

8-Bit MCU market screams for product

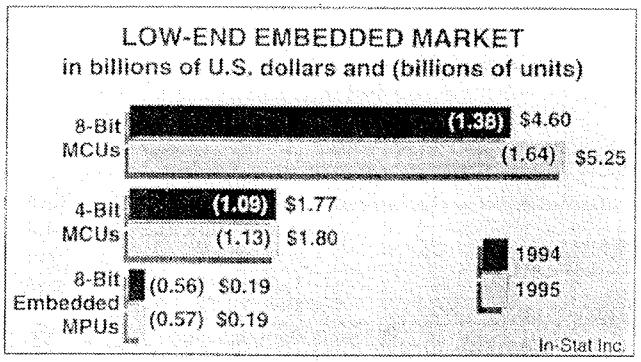
In some 8-bit microcontrollers lines, customers face backlogs up to 50 weeks for product shipments, declared Dataquest Inc. in San Jose. Jerry Banks, principle analyst at the market research firm, said Motorola Inc. of Austin, Texas, caused the renaissance with its 68HC05, priced under US$ 1.

At this low price, many applications using 4-bit microcontrollers switched to 8-bit units and, in the process, made the 68HC05 the leading chip in this market category. The 8-bit market is growing 15% a year and currently outsells 16-bit microprocessors 14 to 1.

The second highest shipping 8-bit microcontroller architecture is the 8051. It holds 28% of the 1993 market. Banks credits Philips Semiconductor of Sunnyvale, Calif., for keeping 8051 alive in the market. Intel Corp. of Santa Clara, Calif., who created the chip, now wants back in the market. Today (13 Feb.), it debuted a new version (see related story).

Banks said another reason for the popularity of 8-bit processors is they use fab capacity being abandoned by products migrating to the next level of process technology. It is not cost effective to build a new facility to make the parts.

For example, Intel's new 8051 version is a high-volume chip for 0.8-micron fab capacity being abandoned by the 486 and Pentium CPUs. Motorola's problem is not having excess fab capacity. It is buying existing IC fabs from other companies to build 8-bit processors.



Intel aims to take back 8051 market

After long ignoring the 8051 microcontroller market, Intel Corp. today reentered the market with its new 8xC251SB. Continued strong customer demand for the 8-bit chip that the Santa Clara company invented 15 years ago pulled it back into the market.

The pervasiveness of the architecture in telecom line cards, phones, modems, printers, copiers, CD ROM drives, and hard disk drives ensures Intel a ready market

for the new chip. Its great advantage is an enriched 16- and 32-bit instruction set at a price of US $6 to $7 in large quantity.

Yet another strong attraction for the product is its ability to run existing 8-bit binary programs unchanged with a five-times performance boost. The 8xC251SB's major competitor-the 80C51 XA 16-bit upgrade CPU debuted last year from Philips Semiconductor of Sunnyvale, Calif.-requires recompiling 8-bit code.

Intel claims rewriting 8bit code for its chip boosts performance 15 times.

Features of Intel's new chip include a three-stage pipeline and a register-based CPU architecture, in addition to an expanded instruction set. A larger 1 kbyte of on-chip RAM also boosts performance. Available now, the CPU comes with 16 kbytes of on-chip onetime-programmable memory or ROM. ROMless versions are also available.

KOLEDAR PRIREDITEV

DECEMBER

04.12.-06.12. 1995
5th INTERNATIONAL SEMINAR ON DOUBLE LAYER CAPACITORS AND SIMILAR ENERGY STORAGE SYSTEMS
Deerfield Beach, Florida, USA
Info.: + 00 1 407 338 8727

11.12.-15.12.1995
SEMICONDUCTOR TECHNOLOGY SEMINAR
Austin, Texas, USA
Info.: + 00 1 407 941 8272

06.12.-08.12.1995
SEMICON JAPAN 95
Mukuhari, JAPAN
Info.: +00 1 415 964 -5111 (USA)

10.12.-13.12.1995
INTERNATIONAL ELECTRON DEVICES CONFERENCE
Washington DC, USA
Info.: + 00 1 301 527 0900

JANUARY

16.01.-17.01.1996
OSHA LAB STANDARDS SEMINAR
Orlando, Florida, USA
Info.: + 00 1 412 457 6576

22.01.-25.01.1996
REALIBILITY AND MAINTAINABILITY SYMPOSIUM
Las Vegas, Nevada, USA
Info.: + 00 1 708 255 1561

FEBRUARY

04.02.-06.02.1996
EUROPIAN INDUSTRY STRATEGY SYMPOSIUM
Dresden, Germany
Info.: + 00 49 32 2736 2058

05.02.-06.02.1996
1st EUROPIAN WORKSHOP ON MICROELECTRONICS EDUCATION
Grenoble, France
Info.: + 00 33 76 57 46 82

06.02.-08.02.1996
DISPLAY WORKS '96
San Jose, CA, USA
INfo.: + 00 1 415 967 5375

12.02.-16.02.1996
EMERGING MICROELECTRONICS & INTERCONNECTION TECHNOLOGIES CONFERENCE
Info.: + 00 91 80 662 8091

26.02.-29.02.1996
FAILURE AND YIELD ANALYSIS SEMINAR
Tampa, Florida, USA
Info.: + 00 1 415 941 8272

MARCH

04.03.-07.03.1996
SEMICONDUCTOR PURE WATER AND CHEM CONFERENCE
Santa Clara, C, USA
Info.: + 00 1 408 734 2276

10.3.-15.03.1996
INTERNATIONAL SYMPOSIUM ON MICROLITOGRAPHY
Santa Clara, CA, USA
Info.: + 00 1 800 483 9043

11.03.-14.03.1996
EDAG-ETC-ASIC
Paris, France
Info.: + 00 33 76 57 47 47