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VSEBINA CONTENT

Društvo MIDEM v letu 1995

Leto 1995 je bilo za društvo MIDEM in marsikaterega našega člana dinamično in je minilo v znamenju prizadevanj uresničiti tiste cilje, ki smo si jih zastavili na začetku leta. Priznati moram, da je zaradi vse hujše finančne stiske iz leta v leto vse težje zadovoljiti pričakovanja naših članov glede strokovnega nivoja in kvalitete dela društva nasploh. Kakorkoli, zadovoljstvo ob narejenem še vedno prekrije grenak priokus ob kritikah nekaterih članov, da bi stvari lahko bile še boljše.

Pred Vami je končno zadnja številka letnika 1995, kar pomeni, da smo tudi letos uspeli izdati vse štiri številke revije "Informacije MIDEM". Še več. V številki 25(1995)2 sem Vas obvestil, da je revijo z letom 1995 začel zajemati v svoje podatkovne baze tudi ISI - Institute for Scientific Information. Upajmo, da bo v letu 1996 temu ustrezno revija dobila od nič različen SCI faktor.

Zadnja številka v letu 1995 je tradicionalno posvečena minuli Mednarodni konferenci o mikroelektroniki, elektronskih sestavnih delih in materialih, MIEL-SD'95. Poleg vseh vabljenih referatov objavljamo še tekste predstavitev laboratorijev in sponzorjev v okviru konference, kakor tudi poročilo o sami konferenci. Splošna ocena je, da je letošnja konferenca uspela, zato še bolj zagnano pripravljamo že naslednjo v Novi Gorici.

Obenem vse člane društva in bralce revije vabim k sodelovanju, kajti uspehi društva so sorazmerni količini in kvaliteti vloženega dela. Ravno tako Vas prosim, da s svojimi svežimi idejami in nasveti pomagate novim organom društva pri delu v naslednjem mandatnem obdobju.

MIDEM Society in 1995

The year 1995 has been for MIDEM Society, as well as for its members, a dynamic one, full of efforts to realise the goals planned at the beginning of the year. I must admit that due to tough financial situation it is harder and harder each year to satisfy the expectations of MIDEM members regarding the quality and professional level of the work done in general. However, the satisfaction which we feel after a successfully finished project still covers the bitterness after the criticism of some MIDEM members that certain things could have been done better.

Finally, You have in front of You the last issue of 1995 volume which means that we have succeeded in publishing all four issues of Journal "Informacije MIDEM" planned for 1995. And more : starting with 25(1995)1, ISI - Institute for Scientific Information - indexes the Journal for several of its products. We all hope that this also means that in 1996 the Journal's SCI impact factor will be grater than zero.

Last issue of the Journal in the 1995 is again traditionally devoted to the International Conference on Microelectronics, Electronic components and Materials, MIEL-SD'95. Besides invited papers we are bringing also texts of laboratory and sponsor presentations which were held in a special session, as well as full conference report. It is generally accepted that MIEL-SD'95 Conference was a success but we are already working with full power on preparation of the new one in Nova Gorica.

That is why I am inviting all MIDEM members and readers of our Journal to actively join to all MIDEM activities since Society successes are proportional to the quality and amount of work inputted. As well, I kindly ask You to help newly elected MIDEM bodies with their work during the next election period by giving them fresh ideas and advises.

Editor in Chief

Iztok Šorli

INTEGRATED SMART POWER CIRCUITS INTRODUCTION, DESIGN AND APPLICATION

W. Pribyl, A. Lechner
Siemens Entwicklungszentrum für Mikroelektronik Ges.m.b.H., Villach, Austria

INVITED PAPER
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Key words: microelectronics, IC, integrated circuits, smart power IC, automotive technology, EDP, electronic data processing, semiconductor technology, circuit design, telecommunications, future trends, consumer electronics, applications, SIPMOS technology, SPT, Smart Power Technology, power regulation, triggering actuators, environment conditions, cost reduction

Abstract: Integrated smart power circuits gain more and more importance, as many segments of microelectronics move towards system integration. The combination of many functions - analog, digital and power - on a single chip enable the design and production of even more miniaturised systems for different applications in the fields of automotive, telecommunication and electronic data processing. This paper gives an introduction to the available semiconductor technologies, shows some circuit design examples specific to the problems of smart power devices and focuses on available real products in different application areas. A discussion of future technical trends under the constraints of an extremely price-sensitive market concludes the paper.

Inteligentna močnostna integrirana vezja Uvod, načrtovanje in uporaba

Ključne besede: mikroelektronika, IC vezja integrirana, vezja integrirana močnostna inteligentna, tehnologija avtomobilska, EDP procesiranje, tehnologija polprevodnikov, snovanje vezij, telekomunikacije, trendi prihodnji, elektronika porabnikova, aplikacije, SIPMOS tehnologija, SPT tehnologija močnostna inteligentna, regulacija moči, proženje aktivatorjev, pogoji okolja, zmanjšanje stroškov

Povzetek: Pomembnost inteligentnih integriranih močnostnih vezij narašča iz dneva v dan, saj se posamezni segmenti mikroelektronike gibljejo v smeri vse večje sistemske integracije. Kombinacija velikega števila funkcij - analognih, digitalnih in močnostnih - na enem integriranem vezju, omogoča načrtovanje in izdelavo vse manjših sistemov za uporabo na različnih področjih elektronike, kot so npr. avtoelektronika, telekomunikacije ter elektronska obdelava podatkov. V prispevku uvodoma opišemo razpoložljive polprevodniške tehnologije in nato podamo prikaz nekaterih načrtovalskih prijemov, ki so specifični za načrtovanje močnostnih integriranih vezij. Kot primer opišemo tudi nekatera vezja, ki smo jih dejansko načrtali, izdelali in so trenutno v uporabi v zgoraj naštetih sistemih. Na koncu prikažemo in komentiramo nekatere tehnične trende, ki bodo v bodočnosti pod vplivom cenovno izredno občutljivega trga narekovali smernice razvoja inteligentnih močnostnih integriranih vezij.

1. INTRODUCTION

Integrated circuits show a significant growth potential, not only in the traditional segments as information- and signal processing (electronic data processing, telecommunications and consumer electronics) but also in the fields of power electronics and sensor systems. Modern smart power technologies on silicon enable innovative solutions, which substitute conventional elements as fuses, relays and switches. But furthermore they open up complete new opportunities by system integration. A more complex functionality of the single IC can be combined with higher reliability and less volume and weight. The most important area of application for smart power ICs seems to be the automotive industry. Higher safety standards, tighter environmental legislation and the demand for increasing comfort on board lead to a constantly increasing amount of microelectronic components built into modern cars. Anti-lock braking and airbag systems, an efficient motor management, anti-theft devices and electronic devices for all conveniences in the car will be standard equipment in the near future. Besides smart power devices the sensor elements play a key role in these applications. Active hall effect sensors for position and rotational speed can be produced as low cost devices with high reliability as integrated circuits.

The development of modern, system oriented smart power technologies as Smart-SIPMOS® and SPT (Smart Power Technology) have fostered today's widespread use of microelectronic components in these new fields of application. These technologies allow the monolithic implementation of power output stages together with complex analog and digital functions. Currently maximum supply voltages of 80 V, in special cases up to 170 V and switching currents of several amps can be handled.

2. SMART POWER TECHNOLOGIES

Depending on the different application areas, various smart power technologies provide the best possible solution considering technical and economical aspects. These technologies are characterised by the available active and passive elements - mainly in the power electronics part - the isolation technique applied, the direction of current flow and last but not least the breakdown voltage. A key feature of modern technologies is the integration of standard CMOS and bipolar transistors together with DMOS-devices, which allow low power control circuits for the output stages and guarantee a large safe operating area.

2.1 Smart SIPMOS® Technology

As an example of a CMOS based self isolated technology, the Smart SIPMOS® technology is shown in fig. 1. The power device, realised as a vertical n-channel DMOS-transistor, uses an epitaxial drift layer, grown on a highly doped substrate. The current flows in a vertical direction through the wafer and is collected at the backside via the die attach area to the package. This allows very high current densities and makes the technology the ideal choice for low on-resistance (Ron), high current high side switches (s.fig. 15). But there is a significant limitation: Due to the construction (common n+substrate) all switches on the same chip have to share the positive supply voltage in a common drain configuration. In addition CMOS devices for low and high voltage are available.

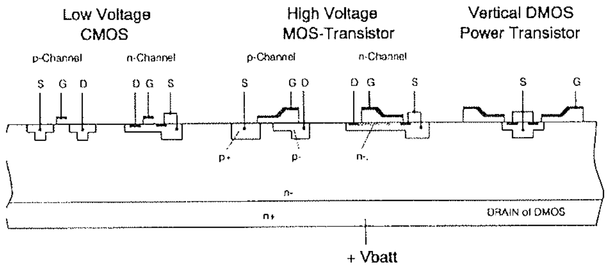

Fig. 1: Cross section of the Smart SIPMOS®-technology

2.2 Smart Power Technology SPT

Fig. 2 shows the cross section of a junction isolated smart power technology (SPT), which is based on BiCMOS enhanced by an optimised DMOS power device. The application of a junction isolation with a p-substrate and a n+epitaxial layer offer the combina-tion of high voltage DMOS, low voltage bipolar and CMOS for high and low voltages. As the current path in the power device is vertical, but is brought back to the surface via a buried layer and sinkers (updrain configuration) this approach allows the integration of several power devices on the same chip without any wiring constraints. In this advanced concept the benefits of CMOS for high integration of logic functions, of bipolar circuits for high precision analog functions (low noise, offset and drift) can be combined with power devices such leading to "systems on silicon".

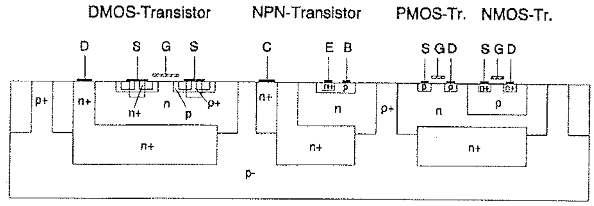

Fig. 2: Cross section of junction isolated SPT-technology

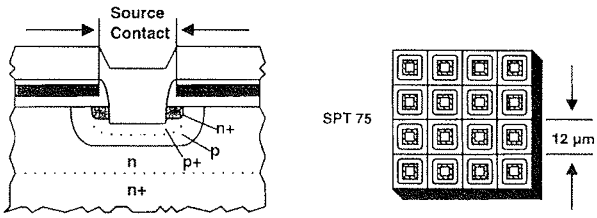

Fig. 3: Detail of DMOS-transistor (cross section and top view)

Today SPT75 as a leading technology using a selfaligned DMOS (Fig. 3) is available for production of smart power devices, mainly for automotive applications.

As a central load-dump protection will be a standard feature in new cars, a reduction of the maximum blocking voltage will be possible. Together with the general trend of reduced feature size in integrated circuits, current developments focus on further reduction of the Ron and a significant increase of packing density in digital and analog circuit areas, thus leading to substantial cost reduction for the customer.

3. FUNCTION BLOCKS FOR SMART POWER

Today's automotive electronic systems must provide highest reliability and robust operation. This includes withstanding voltage spikes, a very extended temperature range and immunity to electromagnetic interference, while not being a source of electromagnetic interference by themselves. Therefore self diagnostic monitoring on chip is important to report the system condition to the controlling microprocessor and to protect the circuit. This leads to different function blocks, which are required for smart power devices in automotive applications (Fig. 4).

An interface part connects the smart power switch to the controlling microprocessor - a good application for the CMOS components. The smart part is responsible for all the diagnostic and protective functions. It is the area of analog circuits using the bipolar or low voltage CMOS components. Last but not least the power switch itself is defined by the DMOS transistor.

INTERFACE	SMART PART	POWER OUTPUT
serial parallel bus status output for diagnostics	over temperature short circuit open load over voltage load dump protection under voltage current limiting di/dt - limiting	high side switch low side switch
CMOS Digital	Bipolar or MOS Analog	Power DMOS

Fig. 4: Functional blocks of smart power circuits

The following figures show some typical functional building blocks and some remarks on their respective functions:

Current Measurement Circuits

For the detection of overcurrent or open load conditions a current measurement circuitry is needed. A simple solution is the direct measurement via a shunt resistor (fig. 5) usually implemented as a part of the metal layer. The reference voltage Vref defines the current threshold, the output of the comparator can be used as diagnostic signal or be directly connected to the gate in a feedback loop to control the current.

The circuit shown in fig. 6 needs no comparator and no voltage reference. Assuming the same collector currents for Q1 and Q2, the current limit threshold is well defined by the ΔVBE of Q1 and Q2, which is known as

$$\Delta VBE = Vt \cdot \ln(AreaQ1 / AreaQ2)$$

Vt = kT/q depends on the absolute temperature, but this temperature coefficient is first order compensated if the resistor RS is made using the aluminium interconnect metal. Therefore this circuit leads to a good temperature compensated current limiting and is therefore often used.

A disadvantage using a shunt resistor is the voltage drop, because the resistor is connected in series to the load circuit. To avoid this voltage drop, the use of a

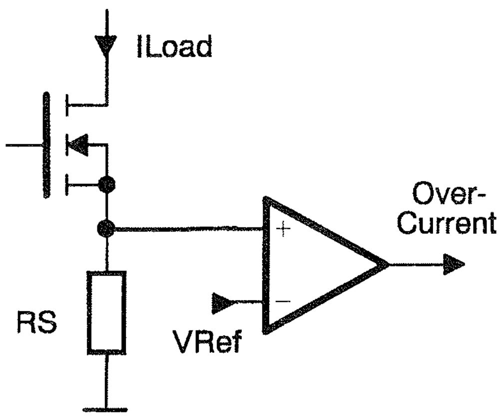

Fig. 5: Current measurement by using a shunt resistor

sensing transistor is known, as shown in fig. 7. For this sensing transistor M2 a few cells of the power transistor M1 are separated and used like a current mirror.

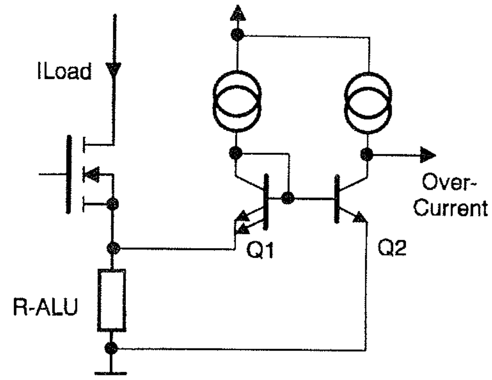

Fig. 6: Current measuring circuit which needs no reference voltage

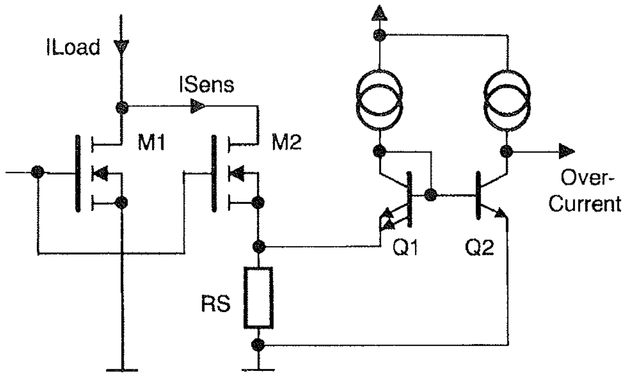

Fig. 7: Current measurement/overcurrent detection with a sensing transistor

Gate Drive Circuits

According to the required switching speed or frequency of the power switch a driver circuit to switch on and off the power DMOS has to be designed. To minimise the power dissipation during switching a fast transition always seems to be a good choice but it can cause significant problems within the circuit and in the surrounding circuitry due to radiated and conducted electromagnetic noise. An appropriate and simple countermeasure to control di/dt-transients is the use of current sources for driving the gate (fig. 8). In the design process a careful balance has to be found between speed and acceptable EMI (electromagnetic interference).

Besides the power loss in the DMOS during the on-state, which has to be dissipated via the package also the protection measures against overvoltage when switching inductive loads and the subsequent heating of the chip has to be taken care of. Fig. 8 shows optional protective circuitry consisting of diodes and zener diodes. This path being turned on during overvoltage conditions switches on the DMOS device and such leads to a reduction of the voltage across the power stage.

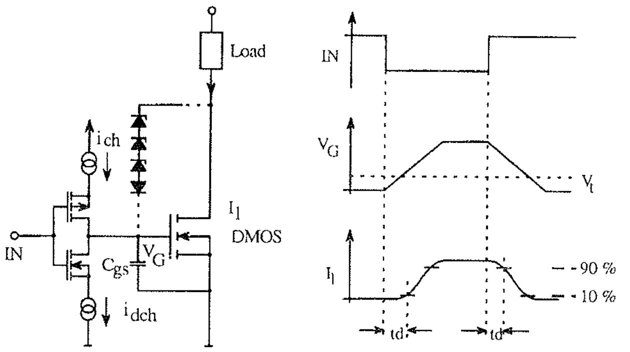

Fig. 8: DMOS-driving circuits with optional overvoltage protection for inductive loads

Temperature Sensors

In applications for smart power circuits as e.g. in the automotive industry the highest possible level of reliability is required for obvious reasons. To achieve this, it has to be guaranteed for all thinkable conditions of the circuit, that critical parameters are recognised in time and that appropriate countermeasures are taken immediately. In addition the circuit has to report status signals to the central unit and to protect itself and other external components in such a way, that no destruction may occur. Besides over-voltage and overcurrent the temperature of the die is a valuable indicator, as overheating can destroy the element. Temperature sensors are built into the circuit for these reasons at appropriate locations. Fig. 18 shows the microphoto-graph of a PROFET® switch, right in the centre of the DMOS-cell array a small circuit to monitor temperature on chip has been placed. The following fig. 9 shows the circuit of such a temperature sensor, which makes use of the well known temperature dependence (fig. 10) of the VBE of a bipolar transistor (Q1).

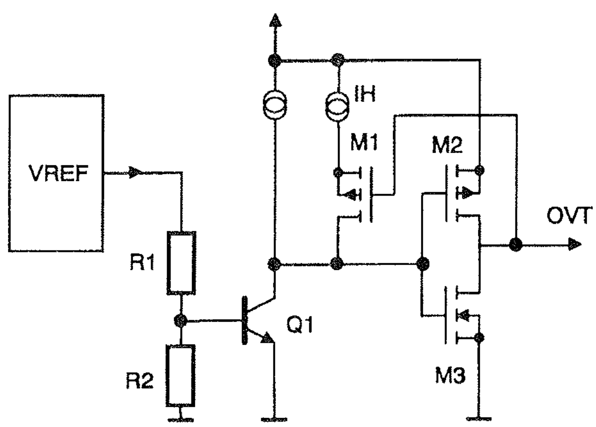

Fig. 9: Temperature sensor with hysteresis

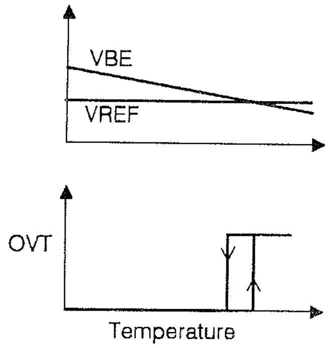

Fig. 10: Characteristic of sensor circuit

The circuit compares the VBE (Q1) with a temperature independent reference voltage, usually supplied by a bandgap reference circuit. The CMOS output stage M2/M3 is connected to the gate of M1 which switches an additional current IH on or off depending on the output level, this defines the hysteresis characteristic. This principle is used frequently, via the voltage divider R1/R2 it is possible to adjust a well defined switching temperature because the VBE voltage is not so sensitive to fabrication tolerances.

Charge Pump Circuit

In a high side switch the power transistor, which always is an n-channel device, is used in a source follower configuration. This requires a positive voltage higher than the supply voltage for the gate to achieve a low Rds-ON, see fig. 11.

Sometimes also low side switches should use a high gate drive voltage to improve the Rds-ON if they are working at low supply voltages (fig. 12). This high gate voltage is commonly generated by a charge pump circuit.

Fig. 13 shows a simple voltage doubler circuit, fig. 14 a practical realisation used in a Smart SIPMOS® high side switch. As bipolar diodes are not available in this process, lateral high voltage n-channel MOS-diodes are

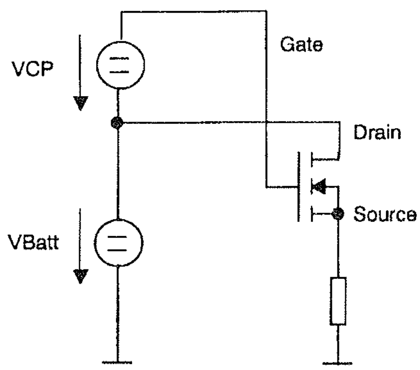

Fig. 11: High side switch requires a high voltage for the gate

used in this circuit. An oscillator is needed to activate the charge pumping operation. Frequency stability is in general not a question, so simple circuits like a ring oscillator or a simple R-C oscillator are used. The working frequency usually is in the range of a few 100 kHz to a few MHz.

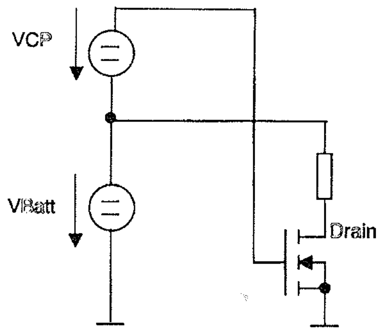

Fig. 12: High gate voltage improves the Rds-ON for a low side switch

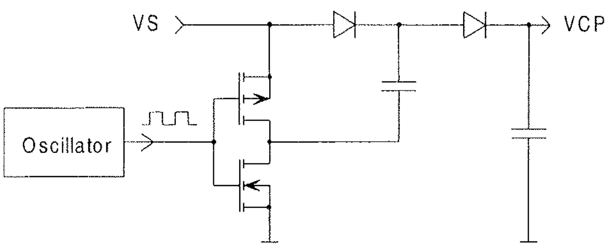

Fig. 13: Simple charge pump circuit (voltage doubler)

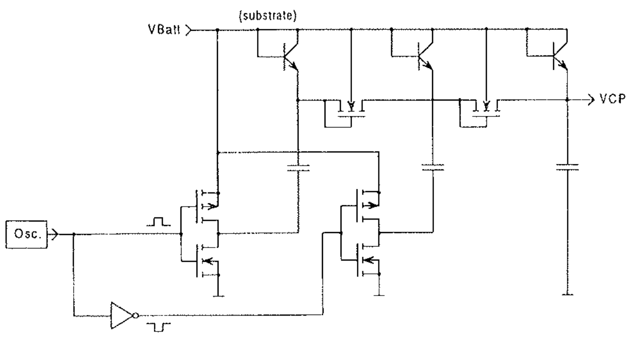

Fig. 14: Practical implementation of a dual stage charge pump circuit for a high side switch in a MOS-based self isolating technology

4. APPLICATION AREAS

As smart power technologies allow the integration of analog and digital functions together with power output stages, robust system ICs can be implemented, which are perfectly matched to the system requirements. They are the interface elements between the electronic system and the environment. They provide reliable and stable power supply for the system, drive signal lines and busses and they control actuators as lamps, motors and valves. In the latter cases the smart part plays a key role: current, voltage, temperature and load conditions are monitored continuously, the switches protect themselves in this way and signal eventual malfunction to the central controller. Switching transients are limited to reduce EMI from the power circuits. Only now these smart power ICs enabled the production of low cost systems with utmost reliability.

The most important application field for smart power is the automotive market. Electronic components can be found in three main areas there:

- Substitution of relays and switches
- Dedicated systems (e.g. motor management, airbag, anti-lock brakes)
- Bus systems (e.g. CAN-bus) for reduction/elimination of cable harness

For the substitution of conventional switches and relays primarily intelligent power switches produced in the Smart-SIPMOS®-technology are used in the configuration as Highside, Lowside or Bridge (fig. 15).

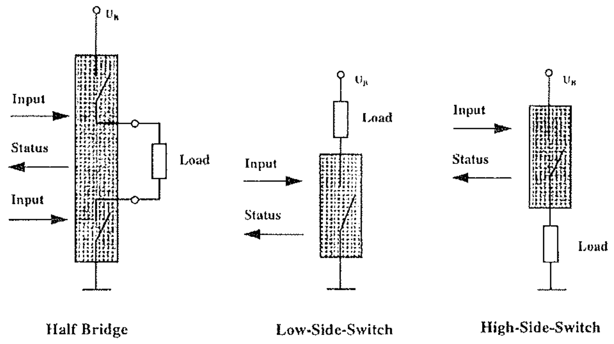

Fig. 15: Different types of smart power switches

The latest generation HITFET® (Lowside) and PROFET® (Highside) provide optimal solutions from the economic and technical point of view.

The HITFET® contains an integrated sensor system including a double overtemperature protection by an integrated and an add-on temperature sensor (fig. 16 and /1/). This feature enables the circuit to react individually to puls-type and continuous overload conditions, such a destruction of the device is not possible. The current limiting function leads to increased lifetime of the light bulbs and the limited di/dt reduced the emission of EMI.

The PROFET® BTSxxx-family provides similar functionality as the HITFET®, but is used in highside applications. In addition these circuits provide a status signal for the system, which indicates error conditions as e.g. overtemperature or broken lamps. Significant progress in reduction of package volume could be achieved in this device family in the last time, a very important achievement for the automotive customer. The innovations are: combination of several switches into one package (2, 4, 8 channels), change to SMD-packaging (P-DSO-20) and modern design concepts (silicon substitutes heatsink).

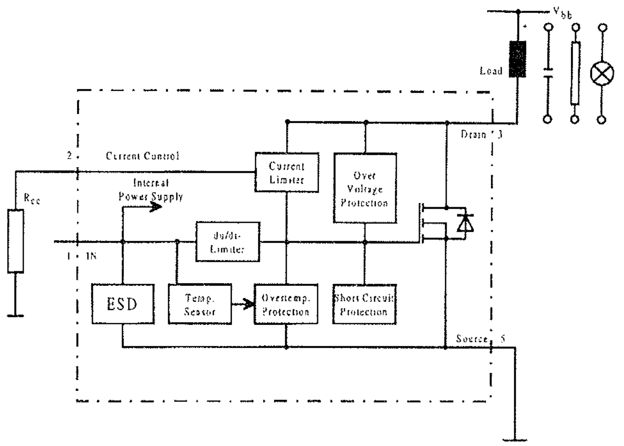

Fig. 16: Block diagram of a HITFET®

„Silicon substitutes heatsink" expresses the advantage for the system designer: spending some more silicon area for the output driver leads to lower Ron and to lower power loss inside the chip; intelligent protective functions turn the device off in critical conditions and such designs became possible, where additional heat sinks are not needed any more, which saves a lot of printed circuit board space and therefore cost for the customer /2/. Fig. 17 is a schematic representation of these innovations, fig. 18 shows a microphotograph of an advanced switch of the PROFET® family.

Integrated sensors also are of key importance for dedicated systems for automotive applications. Hall effect sensors, which can be designed in smart power processes very effectively, gain increasing significance for the picking up of movement, rotation and position. These components do not wear out, deliver an easy to process digital signal are very reliable and can be produced at moderate costs today.

For sensing position hall switches, as e.g. SILC® family is used. Fig. 19 shows as block diagram. In this design, the output switches depending on the absolute value of the magnetic field. The thresholds are generated internally and contain a hysteresis to avoid signal bouncing /4/.

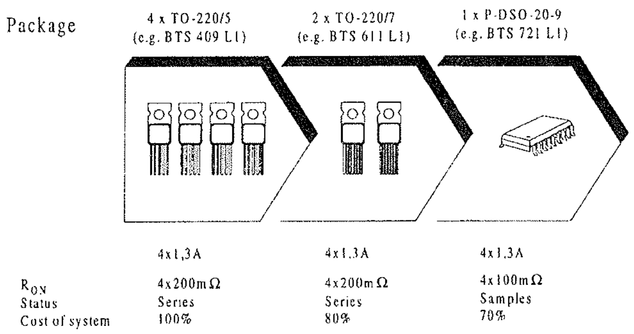

Fig. 17: Innovation with PROFET®-highside switches

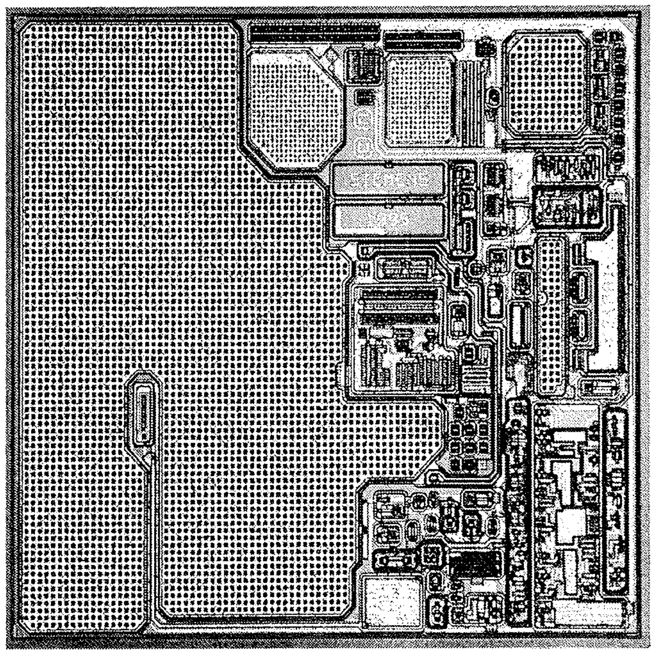

Fig. 18: Microphotograph of a PROFET® highside switch

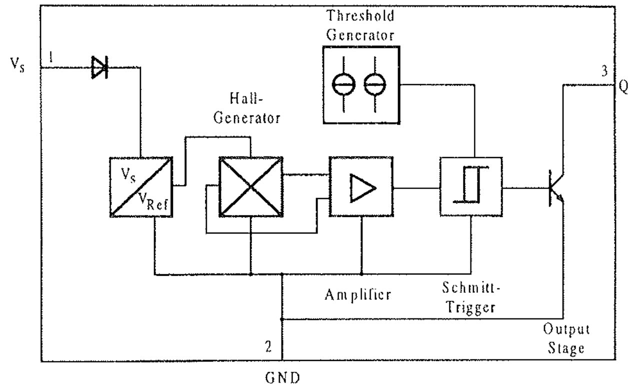

Fig. 19: Block diagram of a SILC®-hall device

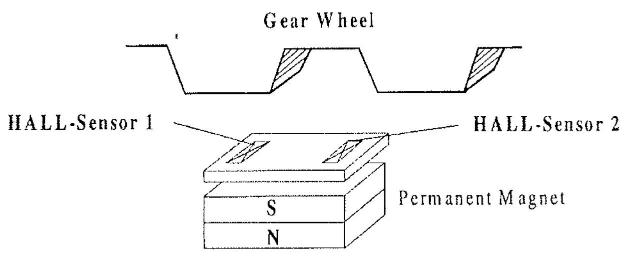

Fig. 20: Functional principle of differential hall IC

To record speed, especially the rotational speed of wheels, differential hall designs are well suited, they are often called gear wheel sensors. Two integrated hall elements are implemented on the chip at a distance of approximately 2.5 mm (fig. 20,21).

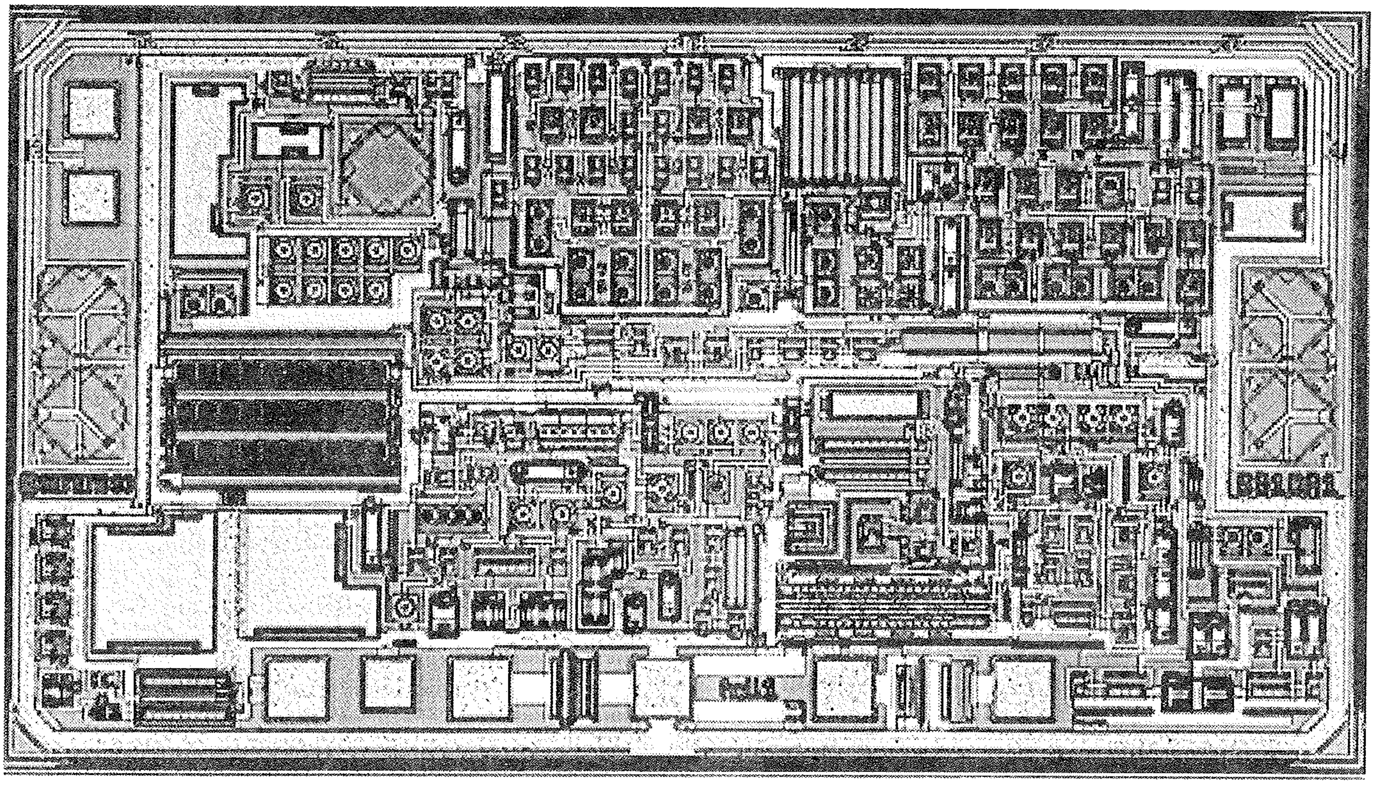

Fig. 21: Microphotograph of the TLE 4921-U3 differential hall sensor chip

Using this approach differences in magnetic field as low as a few mT (milli-Tesla) can be detected. The principle is not sensitive against vibrations on the wheel and generates a very reliable output signal. To give an example the TLE 4921-3U shall be mentioned. The device features very stable thresholds over an extended operating range -50 °C up to +200 °C and is hardened against disturbing pulses in the sense of DIN 40839 standard /5/. It is currently used e.g. in BMW cars of the 7-series /6/.

Many smart power functions, initially developed for automotive applications, are as used in industrial electronic applications (intelligent switches, driving circuits for stepper motors, etc.).

5. SYSTEM INTEGRATION

System integration means the combination of all necessary functions of a dedicated electronic unit as e.g. anti-lock braking system, airbag systems or motor management on as few chips of silicon as possible. In the field of industrial electronics or in peripheral devices for electronic data processing as printers or disk drives similar approaches are needed. System integration leads to a systematic miniaturisation of the systems but needs the combination of many different functions as power control, analog and digital functions up to controllers and memory on a single piece of silicon. In many cases a higher integration level leads to reduction in cost, but this has to be investigated in more detail looking on all the requirements as:

- Implementation of many different functions
- Voltage generation and stabilisation within the system
- Blocking voltage up to 80 V
- Low impedance driving stages at several pins

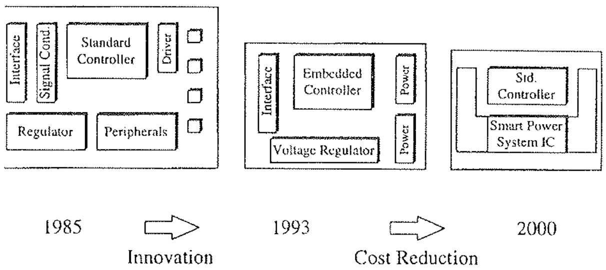

Fig. 22: History of system integration for automotive applications

	Smart Power Technologies	µC-Technologies
Blocking Voltage	30 V - 75 V	5 V --> 3 V
No. of masks	approx. 18	approx.. 15 (18 with NVM)
NVM (non volatile memory)	no	yes (E²PROM, flash)
Feature size	2 µm --> 1 µm	0,8 µm --> 0,5 µm
Analog circuits	yes (BICMOS)	no (only ADC)
DMOS (power)	yes	no

Fig. 23: Comparison of different technologies

- Several pins for signal I/O and some power pins for high current

Fig. 22 shows an overview of system solutions, how they where are and will be approached in the future. At the beginning several low level integration chips and discretes had to be combined into a system, the solutions with so called embedded controllers have been designed.

But nowadays due to the high costs of complete systems many applications use a cheap standard controller and one or a few smart power parts, which comprise all the rest of the system. The smart power system of today typically contains the following building blocks, the available technologies are matched to these tasks and differ significantly from advanced CMOS technologies as used for cost optimised controllers (fig. 23):

- Power supply/regulation for the whole system
- Power output drivers for actuators
- Analog circuits for supervision and diagnosis
- Interface circuits for analog/digital parts

Fig. 24 shows an example of a smart power system IC for automotive applications and its respective functional blocks. The IC is built in the SPT75 technology and contains approx. 5.000 devices.

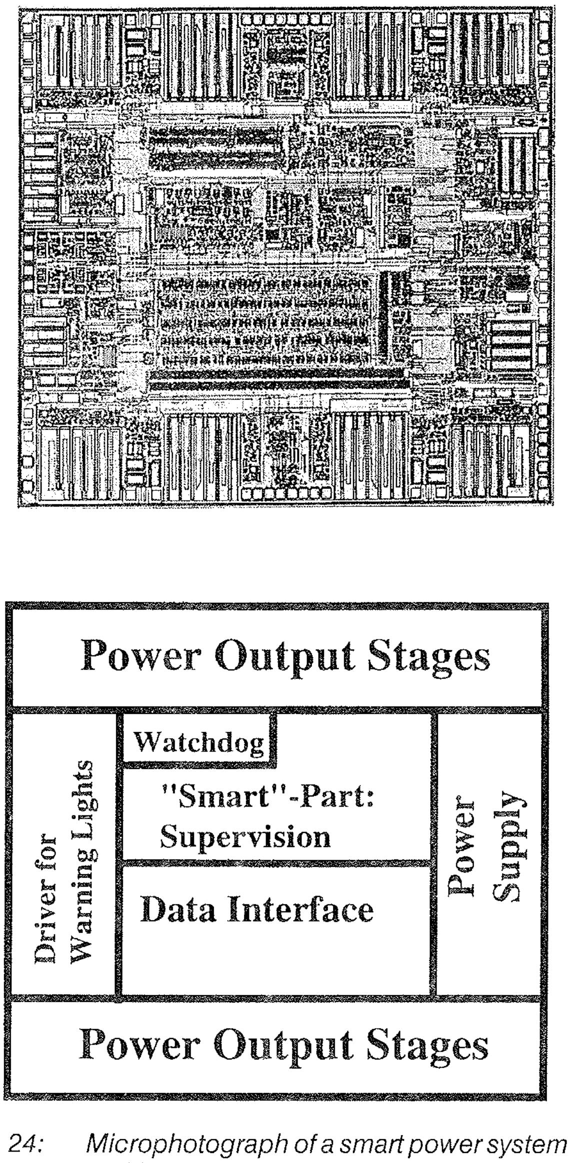

Fig. 24: Microphotograph of a smart power system IC and its respective building blocks

6. SUMMARY AND DISCUSSION

Smart power technologies are the key to further development of dedicated systems, as e.g. anti-lock braking, airbag or motor management in automotive applications, but also for systems structured in a similar way in the industrial, telecommunication and electronic data processing fields. The chips that are now available supply and regulate the power, trigger actuators and monitor and diagnose systems to recognise irrgeular or even dangerous conditions. Smart power ICs make it possible to develope systems with higher reliability, lower volume and weight, less power dissipation which are last but not least even cheaper than their predecessors.

The future evolution of smart power technologies has to be closely related to the system designers benefit. Reduced feature size, innovative circuit design and packaging concepts as space saving SMD-packages lead to ever more advanced and complex smart power circuits and to strongly increased demand for them. The rough environmental conditions, the safety relevant operation together with an extreme cost pressure will force partnerships between silicon supplier and user. In this way concurrent engineering and joint qualification procedures will enable the best possible solutions for both partners. A continuous cost reduction program will be necessary to foster the migration of microelectronics even in the middle and lower price ranges of automobiles.

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Dr. W. Prybil, dipl.ing.,
Dr. A. Lechner, dipl.ing.,
Siemens Entwicklungszentrum für Mikroelektronik Ges.m.b.H.
A-9500 Villach, Siemensstraße 2, Austria
Tel: +43-4242-305-340
FAX: +43-4242-305-223

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ASPECTS OF REALIZATION OF BURIED CAPACITORS IN THICK FILM MULTILAYER CIRCUITS

Walter Smetana
Institut für Werkstoffe der Elektrotechnik,
Technische Universität Wien, Wien, Austria

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Key words: electronic circuits, thick film multilayer circuits, buried capacitors, thick film capacitors, miniaturization of electronic circuits, three dimensional circuits, packing density, capacitor properties, high-K dielectrics, multilayer dielectrics, temperature dependence, firing process, refiring, hybrid circuits

Abstract: To improve the position of thick film hybrids against conventional printed circuits built up in fine line technology attention has to be spent to increase the packing density of hybrid circuits by means of further miniaturization of thick film components or by applying multilayer technique.

Besides conductors and insulating layers, passive components like resistors and capacitors can be produced in thick film technique. This paper discusses the properties of different high-K dielectrics applied for capacitors embedded in multilayer structures. The dielectric is usually exposed to multiple firing cycles during the production process. Interactions between the high-K dielectric, the multilayer dielectric, and the electrode have to be expected. Finally, all these effects govern the performance characteristics of the embedded capacitors.

Načini izvedbe pokopanih kondenzatorjev v debeloplastnih večnivojskih hibridnih vezjih

Ključne besede: vezja elektronska, vezja debeloplastna večplastna, kondenzatorji zakriti, kondenzatorji debeloplastni, miniaturizacija vezij elektronskih, vezja trodimenzionalna, gostota pakiranja, lastnosti kondenzatorjev, dielektriki z visokim K, dielektriki večplastni, odvisnost temperaturna, proces žganja, žganje ponovno, vezja hibridno

Povzetek: Standardnim tiskanim vezjem izdelanim z veliko gostoto povezav morajo debeloplastna hibridna vezja konkurirati tako, da stalno povečujemo gostoto elementov na enoto površine. To dosegamo bodisi z nadaljno miniaturizacijo komponent na vezju ali pa z uporabo večnivojskih povezav in pokopanih komponent.

Poleg prevodnih in izolacijskih plasti na hibridnem vezju znamo izdelati tudi debeloplastne pasivne komponente kot so upori in kondenzatorji. V prispevku opisujemo lastnosti različnih dielektrikov, ki jih uporabljamo za izvedbo pokopanih kondenzatorjev v večnivojskih strukturah. Dielektrik je ponavadi izpostavljen večkratnim temperaturnim obdelavam med tehnološkim procesom. Vsled tega lahko pričakujemo interakcije med dielektrikom za kondenzatorje, izolacijskim dielektrikom za večnivojske povezave in elektrodo. V končni fazi določajo vsi ti procesi končne električne lastnosti pokopanih kondenzatorjev.

1. INTRODUCTION

To improve the position of thick film hybrids against conventional printed circuits built up in fine line technology attention has to be spent to increase the packing density of hybrid circuits by means of further miniaturization of thick film components or by applying multilayer technique. Beside conductors and insulating layers, passive components like resistors and capacitors can be produced in thick film technique. Capacitors on the other hand are usually attached as SMDs to the circuit. Thick film capacitors are commonly realized in a plate configuration. Modified ferroelectric materials with low sintering temperature have to be selected as high-K dielectrics for thick film applications. Dielectrics on the base of $BaTiO_3$ or relaxor ceramics are already available appropriate for thick film processing /1,2/. The ferroelectric ceramic material exhibits a high porosity which induces a high sensitivity to humidity. For protection purpose thick film capacitors have to be sealed by a two layered glass or a polymer coating. But the electrical performance of this high-K dielectric is also affected by chemical reactions between the fluxes and the binder system of the applied conductor paste and the ferroelectric phase. These reactions are often reflected by a low K-phase which lowers the effective capacitance. Beyond that a thick film capacitor in a plate configuration covers a larger substrate area than a conventional chip capacitor of the same capacitance value. Especially the last factor is the reason for the only restricted practical application of thick film capacitors.

As an approach to a further miniaturization of thick film circuits it must be considered to integrate thick film components in the inner layer of multilayers. In this manner the area on the surface of the circuit usually provided for passive components will be reduced. Actually a three dimensional circuit module will be built up. Several papers deal with the integration of resistors inside a multilayer structure. Usually already small deviations from the nominal resistance value are already critical for the circuit performance. The process dependent resistance drift of buried resistors cannot be adjusted by a trimming process as easily as usual. On other side for many applications capacitors of very tight tolerances are not required. With regard to increase the packing density of circuits it seems practicable to bury capacitors inside a multilayer structure. Besides, no additional passivation of the high-K dielectric is necessary. In turn, electrical properties of the high K-dielectric are sensitive to the processing conditions, especially to the firing in the presence of conductors and multilayer dielectrics. According to technical reports it is well documented that the permittivity increases as the silver content of the electrode material increases /1/. This must be related to the lower binder content of Ag-conductors in comparison to conventional PdAg-conductors. To prevent silver migration the application of a buffer dielectric is recommmended often.

This paper discusses the properties of different high-K dielectrics applied for capacitors embedded in multilayer structures. The dielectric is usually exposed to multiple firing cycles during the production process. Interactions between the high-K dielectric, the multilayer dielectric, and the electrode have to be expected. Finally, all these effects govern the performance characteristics of the embedded capacitors.

2. EXPERIMENTAL

2.1 Test structure

Constituents which are not part of the high-K dielectric may diffuse into the embedded capacitor in two ways: One is peripherally from around the electrode, the other through or from the electrode. The sum of these effects affects the properties of the capacitors. The performance of the buried capacitors has to be evaluated with regard to two aspects: The actual capacitance value and the temperature dependent performance of capacitors.

High-K capacitors are usually found in applications where operation is nearer room temperature, a Q as low can be tolerated and the exact capacitance value is not critical. Bypass and many coupling applications, for instance, often need only a minimum capacitance value for proper operation. For some of these applications even Z5U can be used over the full -55°C and 125°C temperature range, as long as their application requires only the minimum capacitance obtained at the temperature extremes. The dielectric constant at these temperature extremes is often still more than that of the more stable but intermediate-K materials.

The topic of this study deals with the specification of parameters affecting the change of performance characterics of high-K thick film dielectrics. Interdigitated capacitor samples overprinted with the selected dielectric have been prepared to eveluate their dielectric behavior /3/. The finger test structure is quite better suited than the conventional plate configuration to specify the contribution of different material interaction effects by means of capacitance measurements. The total capacitance of the interdigital pattern results from stray fields inside the alumina substrate and the applied dielectric. If the dielectric is applied in an appropriate thickness the stray field of the finger capacitor develops inside the layer (Figure 1a) otherwise a certain fraction of the stray field protrudes the surface of the deposited dielectric which reflects a lower total capacitance (Figure 1b).

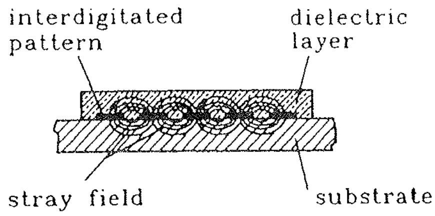

Figure 1a

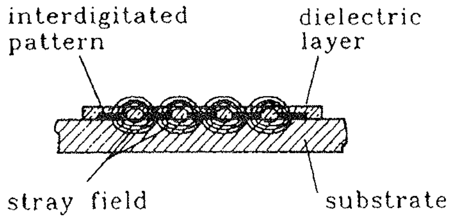

Figure 1b

Fig. 1a-b: Distribution of stray fields

Standard thick film techniques were employed to prepare capacitor test samples on 96% alumina substrates. Table 1 lists the materials used in this study.

Multilayer system:	Conductor (metal type)	High-K dielectric (K at 1kHz)	Multilayer Dielectric	Buffer
DuPont	QS 170 (AgPt)	5540 (6000)	QM42	5520
ESL	D9516 (AgPt)	4210 (10000)	4913	-

The capacitor structure consists of the interdigital conductor pattern, followed by two, up to four layers of dielectric. Conductors were printed with a 325 mesh screen coated with a 20μm thick emulsion. Dielectrics were applied with a 200 mesh screen with an emulsion thickness of 30μm. After printing each paste was dried for 10 minutes at 150°C before firing. The firing was conducted in a belt furnace with cycle duration of 60 minutes and 10 minutes at peak temperature of 850 °C. All layers were separately fired. The target fired thickness of the high-K dielectric was 70 to 80 μm. The thickness of the multilayer dielectric was 40 or 80μm respectively.

Due to the geometrical proportions of the gap width between the electrodes (150 μm) and the thickness of the dielectric (80 μm) the total capacitance becomes sensitive to any additionally applied layer with differing permittivity (Figure 1b). To evaluate the influence of multilayer compositions on the performance of the high-K dielectric, batches of different samples with varying sequences of layer deposition have been prepared (Figure 2):

Arrangement A: electrode pattern overprinted by high-K dielectric (thickness: 70-80μm).

Arrangement B: structure identical with arrangement A, but overprinted - if necessary - with a buffer-layer (thickness: 20μm) and multilayer dielectric (thickness: 40μm or 80μm).Arrangement C: structure identical with arrangement A, but overprinted with a conductor layer.

Arrangement D: structure identical with arrangement C, but covered with multilayer dielectric (thickness: 80μm).

The printed areas of all applied layers are identical.

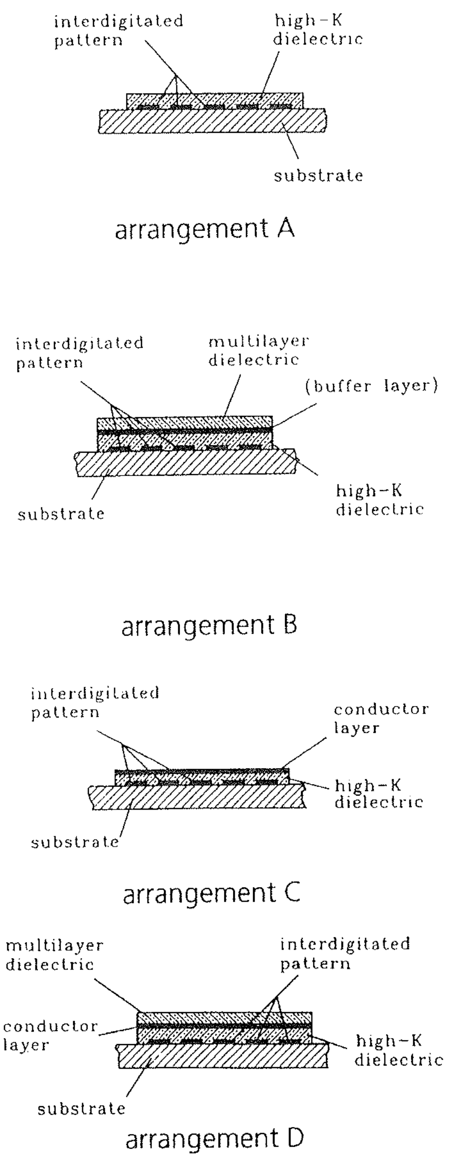

Fig. 2: Arrangement in layers

2.1.1. Results

Capacitance and dissipation factor were measured with a HP4192A impedance analyser. Measurements were carried out using an automated equipment over the temperature range -55°C -125°C realized by a thermostream (Froilabo).

The performance of dielectrics is characterized by a change on capacitance. In order to specify the interaction effects and to compare the performance of different high-K dielectrics a normalized graphical representation for the capacitance shift at a frequency of 1kHz has been selected. Figure 3 shows the temperature characteristics for the high-K dielectrics under investigation (arrangement A, Figure 2).

The maximum of the capacitance curve (Curie-temperature) shifts from 5°C to 35°C and the curve becomes broader as the high-K dielectric of the Du Pont system

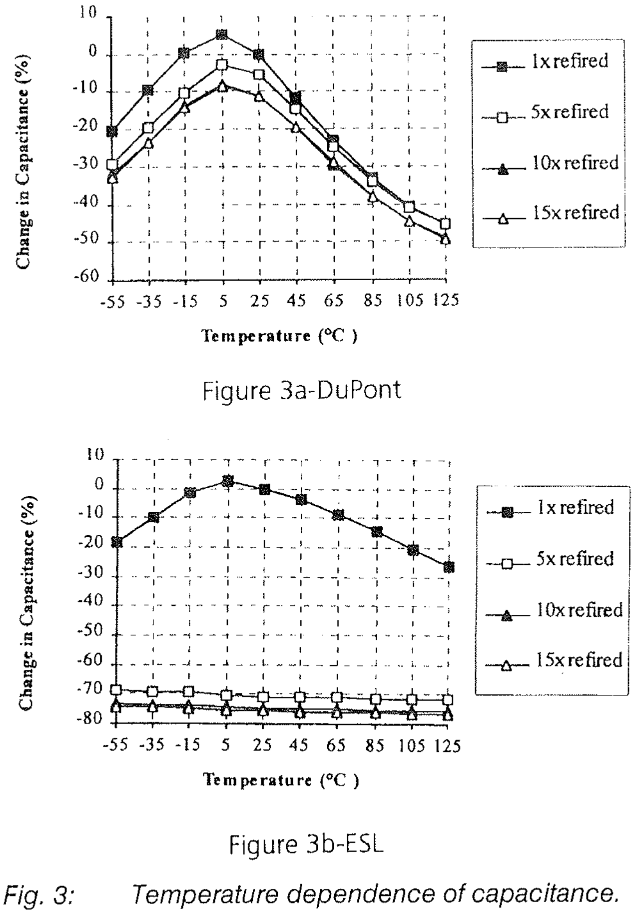

Fig. 3: Temperature dependence of capacitance.

is overprinted by the buffer layer as well as by the multilayer dielectric (thickness: 40 μm) according to arrangement B (Figure 2 and Figure 4). Due to the dilution of the ferroelectric phase the capacitance drops slightly (within 10%) if an additional layer of multilayer dielectric (total thickness of multilayer dielectric: 80μm) is applied.

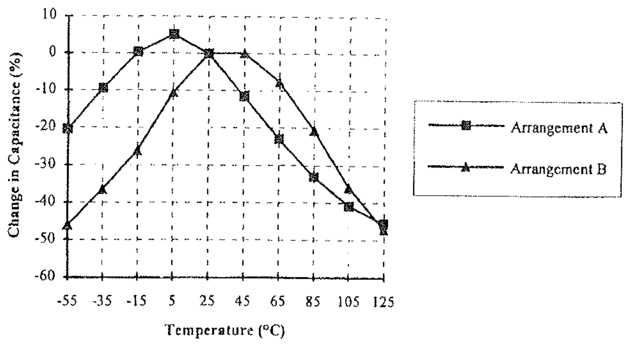

Fig. 4: Influence of buffer and multilayer dielectric on the temperature characteristic of a high-K dielectric.

According to the processing conditions of thick film multilayers test samples with a different arrangement of layers (Figure 2) have been exposed to multiple firing cycles in order to evaluate the sensitivity of the high K-dielectric to refiring. Figure 5 depicts the changes in capacitance versus additional firings.

The ESL high-K dielectric exhibits fairly large shifts especially upon the first five refiring cycles (arrangement A). The considered refire shifts in capacitance are negative. The capacitance response of arrangement D to extra firing must be related to two opposite effects: The refiring process contributes to an increase of capacitance (arrangement C), as well as to a drop of capacitance on behalf of the sensitivity of the high-K dielectric to refiring (arrangement A). The net effect is the sum of these. The sum can be positive or negative depending on their effectiveness. Migration of electrode material during firing might be a plausible reason for the increase on capacitance of the Du-Pont-composition and the ESL paste system because a further densification of the dielectric could not be detected. Measuring the dielectric thickness before and after refiring cycles showed no change.

The temperature characteristic of arrangement B for the Du Pont system shows evidently an interaction between

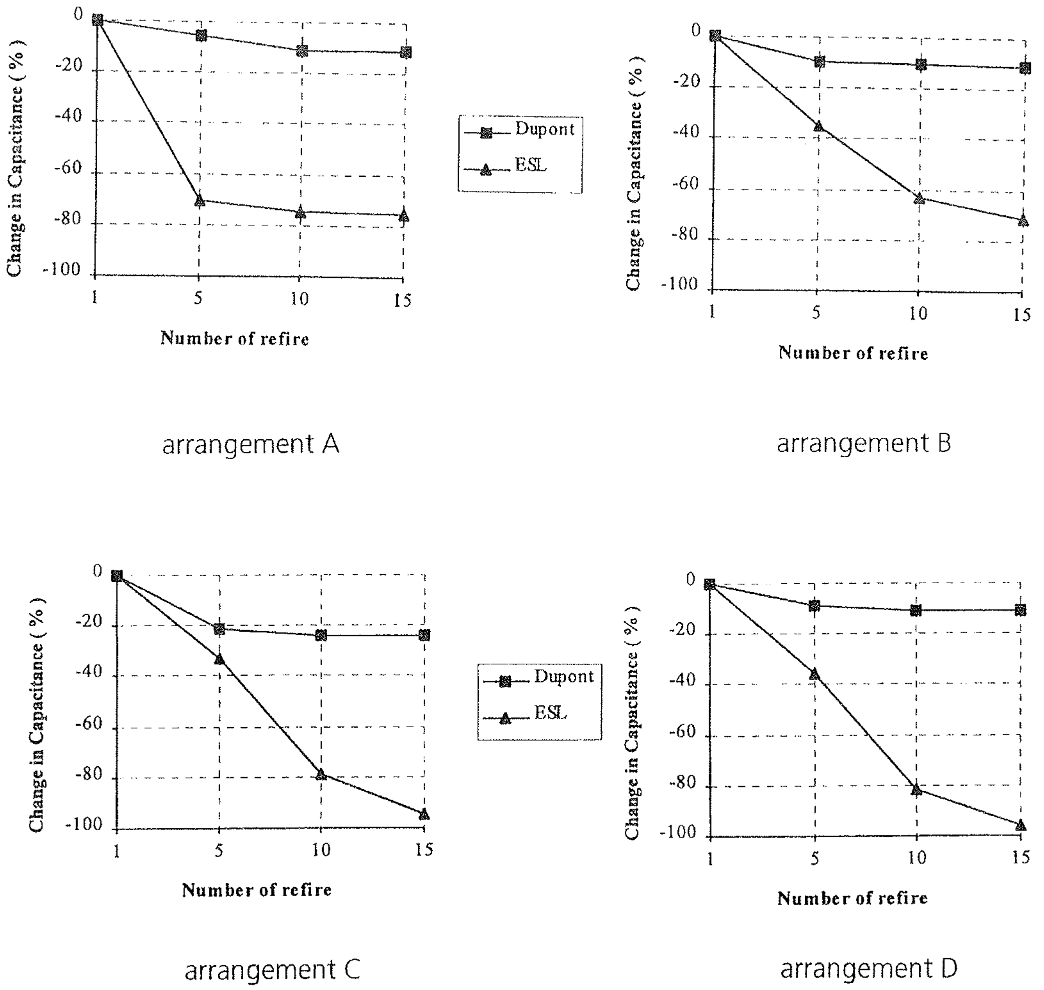

Fig. 5: Change in capacitance in dependence of refiring cycles.

the dielectric layers (Figure 6) due to extra firings which results in a further shift of the Curie temperature.

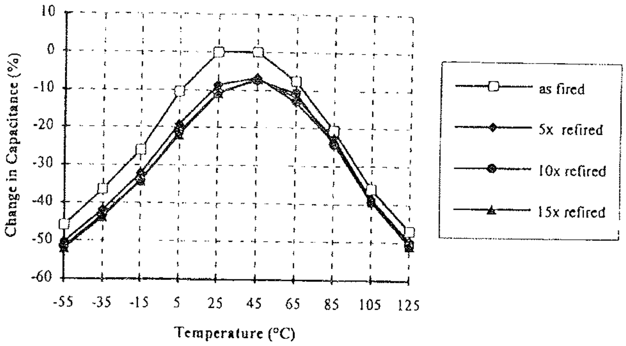

Fig. 6. Shift of temperature characteristic due to extra firing.

2.2. BURIED CAPACITORS

In a next step of the study the viability of realizing buried capacitors will be demonstrated by application of the Du-Pont-system and the ESL-paste- system. To get familiar with the size dependent aspects of capacitance shift, capacitor arrays built up on two substrates by a bottom plate of 22mm x 36mm and square parallel top plates capacitor structures of 2mm x 2mm, 3mm x 3mm, 4 x 4 mm, 5 mm x 5 mm, 6 mm x 6 mm, 8 mm x 8 mm, 10mm x 10mm and 12 mm x 12 mm have been produced. Two types of samples have been prepared: Samples of type A have been placed on the substrate followed by firing a buffer layer (only for the Du-Pont-system) and a multilayer dielectric on top (Figure 7). The capacitor arrays of type B were placed on the multilayer dielectric or on the buffer layer, respectively (Figure 8). No additional layer on the top of the capacitors has been applied. The multilayer as well as the high K-dielectric were printed in two layers using a 200 mesh screen. The thickness of the high-K dielectric is 48 μm for the Du-Pont-system and 55 μm for the ESL-system. To simulate the processing conditions of multilayer circuits, the samples were exposed up to ten additional firing cycles. Figure 9 and Figure 10 depict changes in capacitance versus temperature with varying number of firings for samples of type A with and without buffer layer. Samples built up with a buffer layer show a pronounced shift of Curie-temperature with additional firings. Besides that, lower capacitance values will be realized. They exhibit also a low stability to refire process. For samples of type B the peak of capacitance at Curie-temperature is flattened drastically with an increasing number of firing cycles (Figure 11). The typical temperature dependence characteristic for ferroelectrics is lost as an additional buffer layer is applied. The capacitance values as well as the refire stability of these samples are low.

The ESL-high K dielectric shows a characteristic relaxor behavior (Figure 12). Capacitors of type A, built up with this paste yield high capacitance values with an excellent refiring stability (Figure 13). In the contrary the refiring stability of the capacitors of type B is only poor (Figure 14).

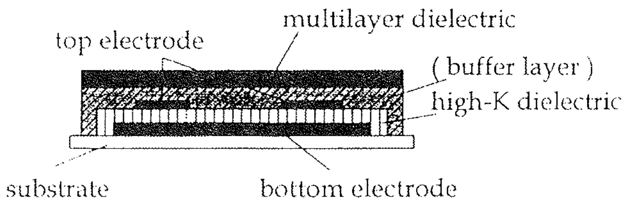

Fig. 7: Sample type A

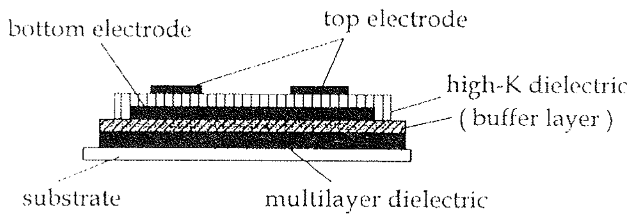

Fig. 8: Sample type B

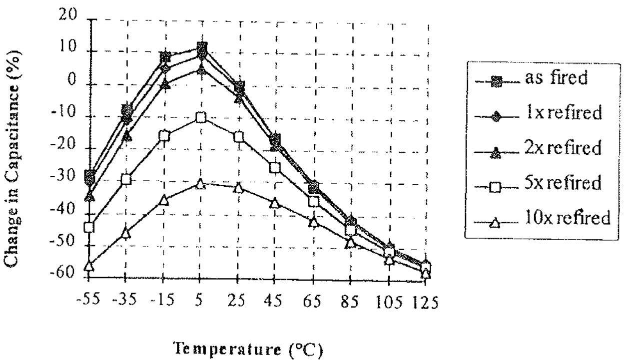

Fig. 9: Capacitance change due to additional firings: sample type A without buffer

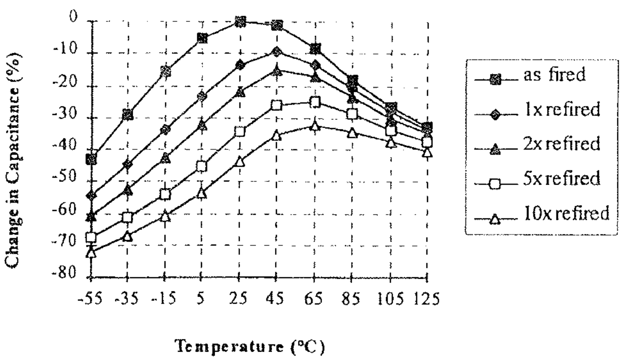

Fig. 10: Capacitance change due to additional firings: sample type A with buffer

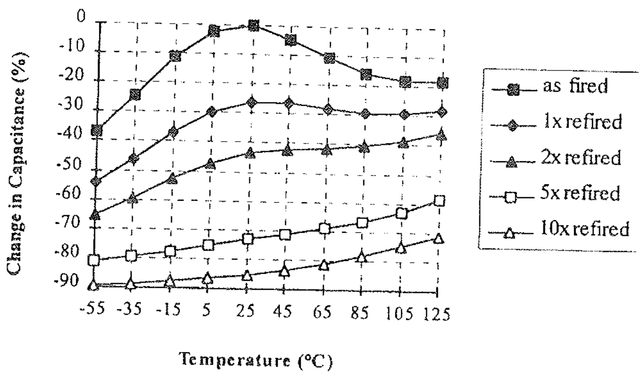

Fig. 11. *Capacitance change due to additional firings: sample type B*

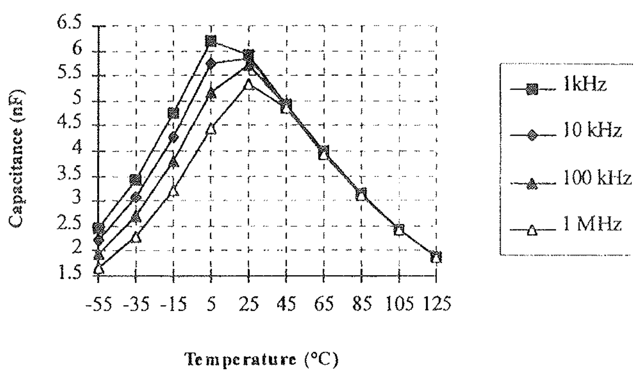

Fig. 12: *Temperature dependence of capacitance (relaxor behavior)*

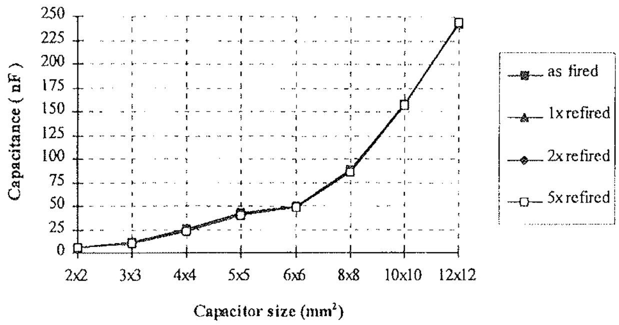

Fig. 13: *Capacitance change due to additional firings for samples type A*

The capacitance shift of capacitors of type A, independent of the employed paste system, becomes greater as the capacitor size is reduced (Figure 15). This must be related to a peripheral diffusion because the silver electrodes form a nearly impenetrable barrier for diffusion. Therefore the diffusion becomes more effective as the area to circumference ratio of the electrodes becomes smaller. In contrary the capacitance shift of capacitors of type B is increasing with capacitor size for devices of small dimensions or nearly constant for capacitors of larger geometrical proportions (Figure16).

There is evidently a strong interaction from the multilayer dielectric through the bottom electrode. This effect is increased by applying the buffer layer for the Du-Pont system.

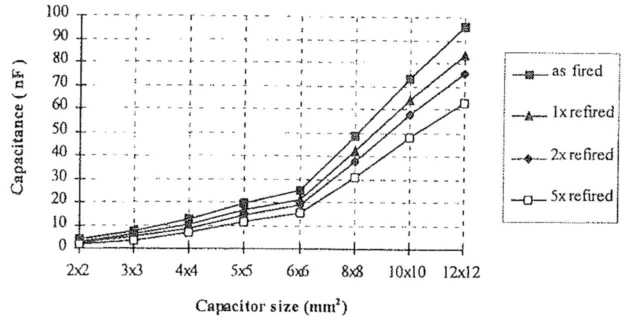

Fig. 14: *Capacitance change due to additional firings for samples type B*

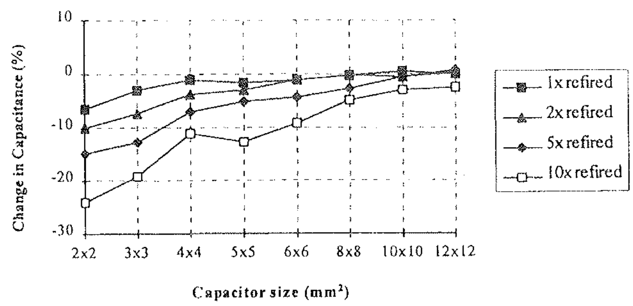

Fig. 15: *Capacitance shift due to additional firings: type A (ESL)*

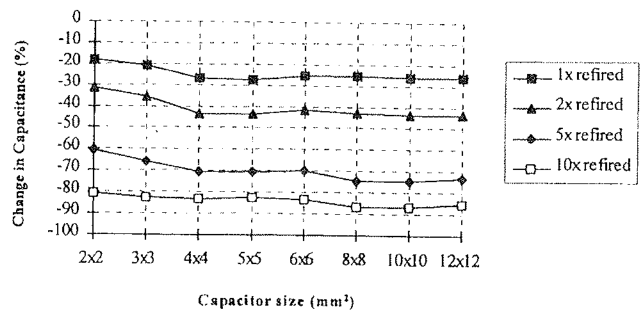

Fig. 16: *Capacitance shift due to additional firings: type B (DuPont)*

3. Summary

The fabrication of thick film capacitors integrated in multilayer structures is very critical due to the sensitivity of high-K dielectrics to multiple firings and to diffusions. Based on our study it is possible to realize buried capacitors in tight tolerances. The buried capacitors have to be placed immediately on the substrate. This arrangement minimizes the influence of repeated firing cycles on the stability of performance of integrated capacitors. The integration of capacitors in multilayer structures is a viable method to increase the packaging density of thick film hybrids.

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Dr. Walter Smetana, dipl.ing.
Institut für Werkstoffe der Elektrotechnik,
Technische Universität Wien, Gußhausstraße 27,1040
Wien, Austria
tel.: +43 1 588 01
fax: + 43 1 504 1587

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THE NEW SYNCHROTRON LIGHT SOURCES - POWERFUL TOOLS FOR RESEARCH AND PRODUCTION

Mark Pleško
Jožef Stefan Institute, Ljubljana, Slovenia

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Key words: synchrotron radiation, synchrotron light sources, VLSI circuits, circuit production, VLSI devices, micro mechanic devices, device production, properties of synchrotron light, experimental methods, XAS, X-ray Absorption Spectroscopy, XANES, X-ray Absorption Near Edge Structure, EXAFS, Extented X-ray Absorption Fine Structure, XSW, X-ray standing waves, XRF X-Ray Fluorescence spectroscopy, EPS, electron photoemission spectroscopy, HREELS, High Resolution Electron Energy Loss Spectroscopy, measuring methods, ESCA, Electron Spectroscopy for Chemical Analysis, XRD, X-Ray Diffraction, WAYS, Wide Angle X-ray scattering, SAXS, Small Angle X-ray Scattering, LEED, Low Energy Electron Diffraction, LIGA, lithography, electroplating, moulding process

Abstract: In the last two years, new high-brilliance synchrotron light sources have been commissioned and taken into operation. Compact synchrotron sources dedicated to the production of VLSI and micro mechanic devices are being built, too. This article gives a basic list of the properties of synchrotron radiation, provides a brief overview of the main experimental methods and shows how synchrotron radiation can be used for production of micro devices. The new synchrotron light source ELETTRA, which has been built at Trieste, and the planned Slovenian beam line BOSS are presented in more detail.

Novi izvori sinhrotronske svetlobe. Močno orodje za raziskave in proizvodnjo

Ključne besede: sevanje sinhrotronsko, viri svetlobni sinhrotronski, VLSI vezja, proizvodnja vezij, VLSI naprave, naprave mikromehanske, proizvodnja naprav, lastnosti svetlobe sinhrotronske, metode eksperimentalne, XAS spektroskopija absorpcijska z Rentgen 'arki, XANES absorpcija struktur blizu roba z Rentgen žarki, EXAFS absorpcija Rentgen žarkov struktur finih razširjena, XSW valovi stojni Rentgen žarkov, XRF spektroskopija fluorescenčna z Rentgen žarki, EPS spektroskopija elektronska fotoemisijska, HREELS spektroskopija ločljivosti visoke z izgubo energije elektronov, metode merilne, ESCA spektroskopija elektronska za analizo kemično, XRD uklon Rentgen žarkov, WAXS stresanje Rentgen žarkov širokokotno, SAXS stresanje Rentgen žarkov ozkokotno, LEED difrakcija elektronov energije nizke, LIGA proces litografije, galvanizacije, odtisa tipografskega

Povzetek: Večje število novih izvorov sinhrotronske svetlobe z veliko svetilnostjo je bilo postavljeno in spuščeno v pogon v zadnjih dveh letih. Ravno tako so tudi mnogi kompaktni sinhrotronski izvori namenjeni proizvodnji VLSI vezij in mikromehanskih struktur še v fazi izdelave, oz. priprave. V prispevku najprej opišemo osnovne lastnosti sinhrotronske svetlobe, podamo pregled glavnih eksperimentalnih metod, kjer uporabljamo sinhrotronsko svetlobo in komentiramo, kako lahko sinhrotronsko svetlobo uporabimo za izdelavo mikro komponent. Na koncu bolj podrobno predstavimo predvideno slovensko žarkovno linijo BOSS pri novem izvoru sinhrotronske svetlobe ELETTRA, ki je zgrajen blizu Trsta.

1. Introduction

Synchrotron radiation became available in a routine manner to the scientific community in the early 1980s. Since that time the use of techniques employing synchrotron radiation has proliferated, so that its unique properties are now having a major impact on many areas of natural and technical sciences such as chemistry, material science, physics, biology, biochemistry, pharmacology, ecology, medicine, etc. /1-4/. Not only have new opportunities with existing methodologies been opened up but also several new techniques have become available. It is interesting to note that synchrotron radiation was first generated in the bending magnets of accelerators built for high energy particle physics research and that it took ten years before it was considered a potentially useful research tool instead of a mere technical nuisance for accelerator builders /5/.

Particle physics accelerators were soon inadequate to meet the demand for synchrotron radiation which was increasing within the scientific community. Dedicated storage rings and associated instrumentation with enhanced performance characteristics were then constructed in Europe, Asia and the USA (second generation sources).

During this period it became apparent that the brilliance of a source could be tremendously increased by introducing magnetic insertion devices in the storage ring (undulators and wigglers). The results were such that third generation sources, based essentially on insertion devices, were proposed in various places.

Third generation synchrotron radiation sources are characterised in general by an increased emphasis on the quality of the photon beam, expressed in terms of its spectral brightness, i.e. the number of photons emitted per second in a unit of the solid angle, source surface, and frequency bandwidth. High spectral brightness requires therefore a high photon beam intensity, a narrow spectral distribution and ease of focusing onto a small spot.

From the accelerator designer point of view, this implies a low emittance of the electron beam. This condition requires a strong focusing electron optics /6/. A strong focusing optics has the disadvantage of requiring strong chromaticity correction sextupoles and increased sensitivity to quadrupole misalignment and movement, which lead to short beam lifetimes and movements of the photon source. The challenge of the new generation of light sources is that the same optics characteristics that produce a high-brightness photon beam also make it difficult to obtain stable and reproducible operating conditions.

2. The Properties of Synchrotron Light

The main advantages of synchrotron radiation over conventional sources (X-ray tubes and UV lamps) can be summarised as:

- analytic computability of the source properties
- broad and continuous spectrum without peaks and dips
- high flux
- small divergence
- high brilliance
- pulsed operation for time-resolved studies
- highly polarised
- very stable and reproducible source
- UHV clean source for surface analysis - no gases, no plasma

2.1 Radiation of a single charged particle

Synchrotron radiation, which is electromagnetic radiation emitted during the transverse acceleration of charged high energy particles /7-10/ (electrons and positrons), got its name because it has been first seen at a synchrotron /11/. When the high energy particles pass into the magnetic field of the bending magnet they deviate and emit light tangentially to the curve /12/. The radiation emitted has the shape of a fan with an opening angle of the order $1/\gamma$ where γ is the relativistic Lorentz factor:

$$\gamma = \left(1 - v^2 / c^2\right)^{-1/2}$$

which is proportional to the electron energy $E = mc^2\gamma$

The total power emitted scales with the fourth power of γ and is inversely proportional to the second power of the electron's radius of curvature ρ:

$$P = \frac{e^2 c\,\gamma^4}{6\pi\varepsilon_0\,\rho^2}$$

with e being the electron charge. The power is continuously distributed over the frequency spectrum such that the so-called critical frequency

$$\omega_c = \frac{3c\,\gamma^3}{2\,\rho}$$

divides the total power spectrum into two equal parts. For a synchrotron light source with E = 2 GeV ($\gamma \approx 4000$), ρ = 5.5 m, the critical frequency and the corresponding critical wavelength $\lambda_c = 2\pi c/\omega_c$, respectively, belong to the X-ray domain: λ_c = 0.38 nm.

For the soft X-ray and ultraviolet range, an energy of 2 GeV is sufficient and such third generation sources are built on a national scale (BESSY II - Germany, ELETTRA - Italy, ALS - USA, Pohang - Korea, SRRC - Taiwan). To achieve wavelengths of several hundredths of a nanometer higher energy is required. Three hard X-ray facilities are under construction or in operation: SPring8 (Japan - 8 GeV), APS (Argonne/USA - 7 GeV), ESRF (Grenoble/France - 6 GeV). In the case of the ESRF, European co-operation was needed for the construction of such a facility in view of its complexity, cost and experimental potential.

2.2 Insertion devices

In the new light sources the most important elements are the magnetic systems, called insertion devices/13/, inserted in the straight sections of the storage ring. There are two types of insertion devices: wigglers and undulators. Each comprises a succession of small magnets of alternating polarity (figure 1) producing a vertical component of the magnetic field as $B_x(s) = B_0 \cos(2\pi s/\lambda_u)$ with s being the longitudinal co-ordinate and λ_u the period of the magnetic structure.

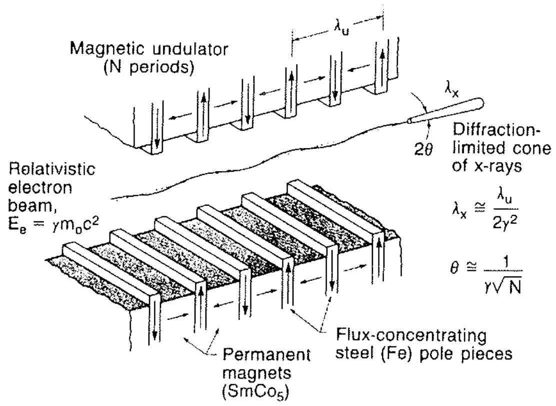

Fig. 1: Schematic of a periodic magnet structure (an undulator). The amplitude of the electron trajectory and the light cone size are not to scale.

The resulting magnetic fields force the electrons to oscillate around a linear trajectory. The light cones emitted at each bend superimpose and in the case of the wigglers their intensity increases proportionally to the number of bends while the spectrum is still continuous.

In the undulators the deviations are weaker, thus the light cones from the different bends overlap and at wavelengths given by /14/

$$\lambda_x \approx \frac{\lambda_u}{2\gamma^2}\left(1+K^2/2\right)$$

the interference effects produce a spectrum with a brilliance increased by the square of the number of bends. This radiation has peaks at odd multiples of λ_x and has a spectral width of $\lambda_x/\Delta\lambda_x \approx 1/N$, N being the number of undulator periods (figure 2). The dimensionless variable $K = 0.934\ B_0$ [T] λ_u[cm] is a measure for the type of insertion device ($K >> 1$ for wigglers and $K \leq 1$ for undulators). The magnets on the undulator are mounted on two jaws that can be opened or closed as required in order to change the on-axis magnetic field B_0 and in turn the value of K. Thus the wavelength maxima λ_x of the radiation emitted by the undulator can be shifted over part of the spectrum. The spectral brilliance of a typical rotating anode X-ray source is only around 10^7 photons/s/mm^2/mrad^2/(0.1% bandwidth), while the best synchrotron sources reach 10^{19} and more.

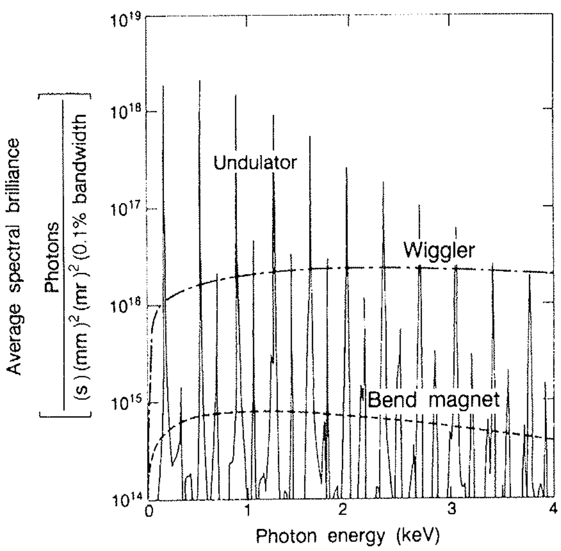

Fig.2: Harmonic content of undulator radiation arising from interference of radiation from different undulator periods (full line) compared to the spectrum of wiggler (dash-dotted) and bending magnet (dashed) radiation for the ALS /15/.

3. EXPERIMENTAL METHODS

Only a brief overview of the main experimental methods with synchrotron light is presented here. The reader is encouraged to read the exhaustive overviews in references /1-4/.

3.1 X-ray Absorption Spectroscopy

X-ray Absorption Spectroscopy (XAS) is ideally suited to probe the immediate environment of specific atoms. An X-ray absorption spectrum is usually divided, for convenience of interpretation, into three regions: the pre-edge and edge; the X-ray absorption near edge structure (XANES); the extended X-ray absorption fine structure (EXAFS).

The excitation of a core electron into the continuum may be convoluted with transitions from the core level to outer bound states resulting in features in the absorption spectrum that precede the absorption edge. The position and intensity of such features are dependent upon the electronic structure and the local symmetry at the primary absorber as the atomic transition is forbidden by the $\Delta l = \pm 1$ selection rule. Valuable structural insights may be obtained from the nature of such effects. The chemical shift in the absorption edge is a measure of the net charge on the primary absorber and, therefore, can serve as an indicator of the element's oxidation state.

The spectral features of XANES and EXAFS arise as a consequence of local electron diffraction. The principal distinction between XANES and EXAFS is that the former invariably involves multiple scattering of the photoelectron within the cluster of atom surrounding the primary absorber, whereas the latter usually does not. The XANES is therefore difficult to interpret, making it an empirical, although very sensitive, fingerprint of the immediate environment about the primary absorber. Direct comparisons of measured spectra can prove extremely useful.

First discovered in the 1930s /16/, the interpretation of EXAFS has progressed from the plain wave, single scattering approximation, to a full spherical wave treatment /17/ which allows the inclusion of multiple scattering pathways. Analytical procedures in k-space involve simulations of EXAFS profiles and refinement of structural and other parameters to produce the optimum agreement between the theoretical and measured data as described in /18/.

The structural parameters available from EXAFS analysis are the distance, the occupation number and Debye-Waller parameter for the nearest and possibly next-to-nearest shell of atoms around the primary absorber (up to an atomic distance of 0.3 - 0.5 nm). Careful modelling of the measured data can also reveal the atomic number Z of the neighbouring atoms.

The simple correlation between EXAFS and the local atomic environment, which has been first pointed out in /19/, is extremely important. Unlike X-ray diffraction, which collects information simultaneously on a large number of atoms in the system and is therefore extremely non-local in nature, the EXAFS is not limited to systems with long-range order. The technique is therefore unique for the study of the chemical structure of amorphous solids, liquids, solutions and gases. Also, since the EXAFS spectrum is measured on a known absorption edge, due to an atom of known chemical type, the technique is chemically specific, giving the co-ordination of a known type of atom.

If, instead of measuring the absorption directly, the secondary process of X-ray fluorescence is monitored /20/, a considerable improvement in the spectral quality of low concentration atoms is achieved, pushing the sensitivity of the EXAFS technique to the levels necessary for the detection of diluted impurities /21/. The same method is also applied for thick samples, where the transmitted X-ray intensity is too low for a precise determination of the absorption coefficient.

Surface EXAFS (SEXAFS) is the surface-sensitive version of the EXAFS technique which implies the use of a surface-sensitive detection method. One of the possibilities is to measure the yield of secondary electrons /22/, because they have a mean free path in the sample between 0.5 and 5 nm, depending on their energy. By tuning the position in energy of the detecting window, one can, in principle, obtain layer-by-layer information on the local atomic structure. This method can be made atomic-species selective on the cost of losing depth tunability by tuning onto the energy of the Auger electrons produced by the core-hole recombination as pioneered in /23/.

3.2 X-ray Standing Wave

X-ray standing waves occur parallel to the surface of a crystal when the incoming and the Bragg reflected waves interfere. At normal incidence of the primary beam, the reflection curve has a wide range, therefore the effect takes place also in less perfect crystals. This opens the possibility to perform XSW on a wide range of materials.

When the photon energy is scanned through the region of a Bragg reflection, the standing wave outside the surface will move. This is equivalent to rotating the sample, as in measurement of the crystal rocking curve.

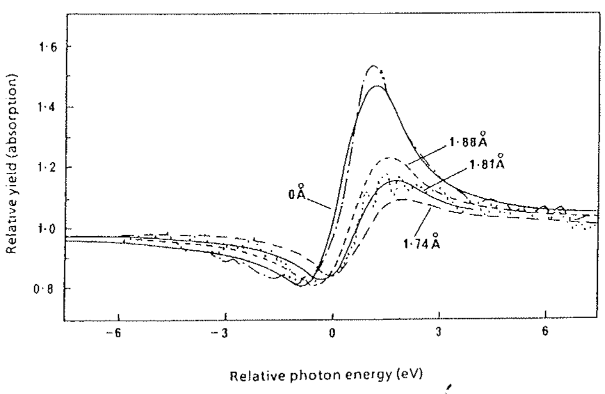

Figure 3: Experimental copper (-.-.-) and chlorine (...) Auger electron yields as a function of photon energy around the normal incidence [111] Bragg reflection. The theoretical curves are calculated for different plane spacing, showing that copper coincides with the surface and that the chlorine layer is 1.81 Å above the surface.

As the node passes through the position of adsorbed atoms, the characteristic Auger electron or fluorescence signal from these atoms will go through a minimum, while an antinode will produce a maximum. Thus the vertical distance of the adsorbate layer can be determined to a precision of a few pm, even at very low adsorbate concentrations, down to a few percent surface coverage. An example is shown in figure 3 for a regular overlayer of chlorine atoms on a Cu[111] surface /24/. This technique actually measures the spacing of the overlayer atoms from a continuation of the perfect bulk lattice rather than from the real surface layer, which may be relaxed or reconstructed in some way. By measuring XSW on two or more lattice planes, the exact position of the adsorbed atoms with respect to the substrate atoms can be determined through simple triangulation.

To have diffraction at normal incidence with low index Miller planes, a range in energy between 2 and 6 keV is necessary. The experiments are quite simple involving only a scan in energy of the incoming radiation instead of a scan in angle. However, the required monochromator resolving power is about 5000. Since SEXAFS and XSW can use the same beam line and the same experimental apparatus, this is a natural combination of methods for determining surface adsorbate geometries.

3.3 X-ray Fluorescence Spectroscopy

Fluorescence X-rays occur when an electron of a higher atomic shell decays into the previously emptied core level and releases its energy.

The characteristic energy of the fluorescence X-rays, different for each chemical element, makes X-ray fluorescence spectroscopy (XRF) a very suitable method for the detection of elements in very low concentrations. Several methods exist that allow to determine concentrations of major, minor and trace elements from the fluorescence yield, either by using reference standards or based on fundamental parameters /25/.

The following characteristics of synchrotron radiation besides the obvious high incident X-ray flux available are exploited for XRF trace element analysis in order to achieve the lowest possible detection limit:

- the tunability of the excitation energy offers the possibility of obtaining the highest sensitivity throughout the whole range of elements of interest by tuning the excitation energy just above the binding energy of the electrons in a particular shell of the element of interest;
- the linear polarisation of the synchrotron beam enables a low background to be achieved, in particular if the fluorescence X-rays are detected at 90° to the incident radiation where no Compton scattering occurs.

Compared with ion-bombardment, the radiation damage induced in the specimen under investigation is considerably less. Especially for biological applications this is a major advantage. Moreover, one can perform

XRF measurements in air or under a protective atmosphere instead of the vacuum necessary for ions.

Because of the high flux available, a wavelength dispersive detector with a higher resolution and thus a better signal/noise ration can be used instead of the more common solid state energy dispersive detector. The lowest detection limit depends very much on the element and the underlying matrix, however, detection limits as low as a few parts /26/ to a few tens of parts /27/ per billion have been reported.

If the photon beam impinges on the sample at angles below the critical one, total reflection occurs. The penetration depth is very small resulting in a good surface sensitivity and in a complete suppression of the scattering background in the fluorescence spectrum. The total reflection XRF method was successfully explored using X-ray tubes /28/, nevertheless up to now the full potential of this method has not been exploited at synchrotron radiation sources yet.

3.4 Electron Photoemission Spectroscopy

Since electrons have a mean free path of only a few atomic diameters in the energy range of 50 - 1500 eV, a number of particle-based techniques are surface sensitive such a low energy electron diffraction (LEED), Auger electron spectroscopy (AES), high resolution electron energy loss spectroscopy (HREELS) and others.

For photoelectron spectroscopy with a synchrotron light source, major advantages arise from the tunability, polarisation and brightness of the source. Tunability allows to optimise surface sensitivity by maximising cross-section and by gearing the kinetic energy of the emitted electron to the minimum escape depth. The polarised nature of the source allows the symmetry of electron states in the surface to be determined.

Here, only one striking example is shown in which the tunability of the source may be exploited to yield interesting information. For instance, figure 4 shows the photoemission yield from amorphous metallic glasses of $Cu_{30}Zr_{70}$ and $Cu_{40}Zr_{60}$ measured at two different photon energies /29/. The valence bands comprise a mixture of states derived from Cu 3d and Zr 4d orbitals. The former exhibit a fairly smooth variation in cross-section as the energy is varied but the 4d states, with a node in their wave function, change in intensity by about two orders of magnitude in the range chosen, allowing easy separation of the contributions to the valence band, with the Zr states found to be near the Fermi level (E=0) and thus dominating the conductivity.

Another powerful method is the measurement of core level shifts. The binding energies of core level electron states are sensitive to the valence level environment of the atom. The corresponding chemical shifts of the core level energies of adatoms, typically by several electron volts, are used to monitor the presence of different valence states on surfaces. This is the basis of the familiar use of ESCA (electron spectroscopy for chemical analysis) which has been pioneered by K. Siegbahn /30/. More recently, using high resolution instrumentation, core level shifts of substrate atoms has been measured, and favourable circumstances, it has proved possible to use this technique to distinguish surface substrate atoms from bulk atoms and even from atoms on intermediate layers (figure 5) /31/. The shifts here

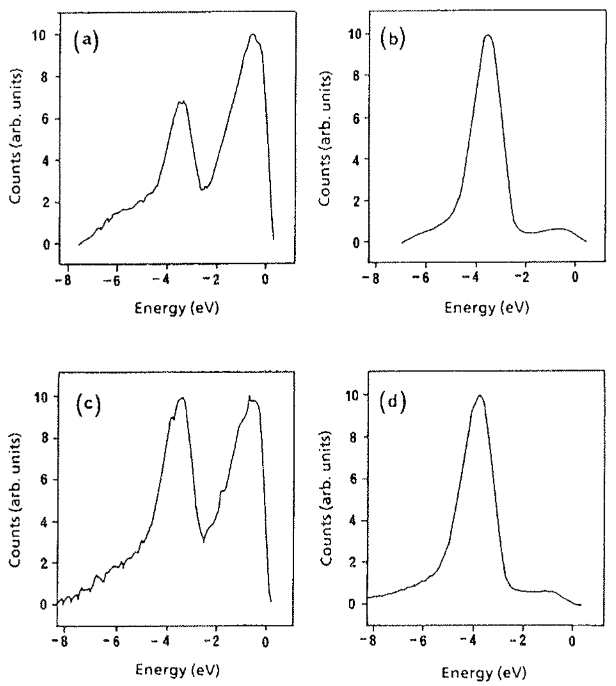

Fig. 4: Photoemission spectra of (a), (b) $Cu_{30}Zr_{70}$ and (c), (d) $Cu_{40}Zr_{60}$ at photon energies of (a), (c) 40 eV and (b), (d) 120 eV.

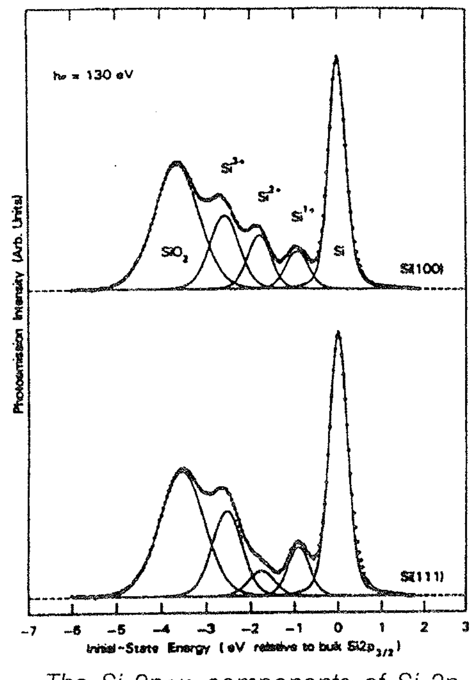

Fig. 5: The Si $2p_{3/2}$ components of Si 2p spectra from thin oxide films of approximately 0.5 nm thickness thermally grown on Si(100) and Si(111) surfaces. Note the reduced intensity of Si^{2+} for Si(111), assumed to be due to structural differences in the interface.

arise from the difference in co-ordination of surface atoms and bulk atoms. This narrows the valence band, which is shifted in energy in order to maintain charge neutrality at the surface. A similar shift is observed by all the core levels. Further shifts are also induced by charge transfer to or from chemisorbed atoms, and surface core level shifts thus provide a useful tool for the characterisation of adsorption sites.

Even more powerful experiments include the measurement of the photoelectron angular distribution. Those methods include angle-resolved photoemission, photoelectron diffraction, Auger electron diffraction and photoelectron holography /32/, which can actually give the position and orientation of single adatoms on surfaces.

3.5 X-ray Diffraction

For decades, elastic X-ray scattering techniques have been the leading probe of the geometric micro structure of molecules and solids. They can be divided into two broad areas. Experiments in the first area (wide angle X-ray scattering - WAXS) investigate systems with long-range order such as single crystals. The second area (small angle X-ray scattering - SAXS) investigates disordered systems, such as liquid solutions and alloys, and partially ordered systems like fibrous biological specimens, liquid crystals, polymers, and others.

Wide angle scattering from crystalline material, i.e. diffraction, is most simply described in terms of the Laue equations, the solutions to which are given by $\Delta\mathbf{K} = \mathbf{G}$; where $\mathbf{G}$ is a vector of the reciprocal lattice and $\Delta\mathbf{K}$ is the scattering vector, i.e. the difference between the wave vectors of the incident and scattered radiation. Each diffracted beam corresponds, in reciprocal space, to the scattering vector touching a reciprocal lattice point. From the positions of the scattering peaks, therefore, one can in principle determine the crystal lattice.

The intensities of the peaks on the other hand are related - besides a dependence on the Debye-Waller factor - to the square of the structure factor containing the information on the electron density inside the unit cell. However, since the intensity is a scalar quantity, the phase of the complex structure factor is indeterminate - the basis of the well-known 'phase problem' in crystallography. Classically this has been approached using the technique of multiple isomorphous replacement (MIR) /33/.

The tunability of synchrotron radiation can be exploited for an alternative solution, based on the technique of multiple wavelength anomalous diffraction (MAD) /34/. The phenomenon arises from resonance effects due to the fact that core level electrons scatter differently from free electrons. As the elemental absorption edge is approached, the atomic scattering factor of that element becomes complex and varies rapidly unlike in the case of Thompson scattering. The net intensity of each Bragg reflection is then energy or wavelength dependent and this variation may be used to solve the problem in a manner analogous to, but without the inherent problems of, the MIR method.

X-ray scattering is so powerful in the determination of crystal structures, because the wavelength of the radiation is comparable to inter atomic distances. Measurements of larger structures in principle needs radiation of longer wavelength. However, the electromagnetic spectrum between 1 and 100 nm is unsuitable for scattering techniques because of strong absorption. Structures of these dimensions can therefore only be studied using X-rays scattered at small angles. SAXS provides information on the overall shape and size of the scattering objects, its density, orientation, packing with other objects, etc. Since X-ray scattering arises from electron density fluctuations in the specimen, a scattering object can be any inhomogeneity - a molecule in solution, a small crystal, a part of a large molecule, a solid or a liquid particle, and so on.

The interpretation of SAXS measurements depends on models for individual types of specimen. The most common parameters are obtained from the plot of scattered intensity I versus magnitude of the scattering vector q. From Guiner's Law /35/, valid in the low angle region, the radius of gyration of the scatterer is obtained. The limit of large q is described by Porod's Law /36/ revealing the mean square electron density fluctuation, which is determined by the periodicity of the system. In case of aggregated systems, the region in between is directly related to the fractal dimension of the system.

The ability to perform anomalous dispersion studies is important also for SAXS measurements. It is especially valuable for disordered materials, because in that case anomalous dispersion directly allows to distinguish con-

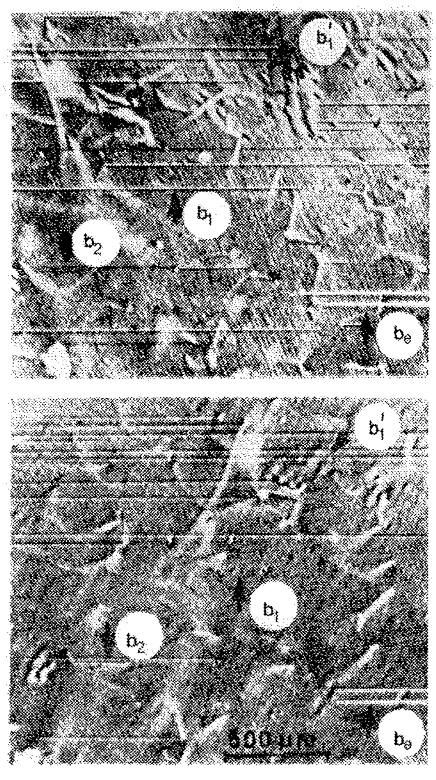

Fig. 6: Epitaxial dislocations in $Ga_{1-x}Al_xAs_{1-y}P_y$ / GaAs heterojunctions (after /37/). Indicated are the Burger vectors.

tributions from different types of atoms to the scattering intensity, without having to refer to models.

X-ray topography is a subfield of X-ray diffraction which produces two-dimensional maps of crystal distortions /37/. The intensity of a Bragg reflection changes when the crystal is distorted. By monitoring the intensity of a Bragg reflection in different points of the crystal, one can create a two-dimensional map of its distortions (see figure 6). This topographic method is very powerful in the study of imperfect crystals and overlayers with technological interest. X-ray topography has a spatial resolution of several micrometers which is much worse than that of dark field transmission electron microscopy. However, due to the low absorption of X-rays, fairly massive single crystals may be imaged and X-ray imaging techniques are characterised by a unique strain sensitivity, down to 10^{-8}.

4. PRODUCTION WITH SYNCHROTRON LIGHT

Although synchrotron light has been mainly used as a source of photons for analytical purposes, the radiation can be also used to induce chemical reactions and thus produce structures just like in normal photo chemistry. Due to the short wavelength of the radiation, it is particularly suited for micro fabrication. Two most prominent applications are the production of integrated circuits on the micro- and nanoscale with X-ray lithography and the production of micro- and nanomechanic devices by means of the Liga method.

4.1 Lithography

Since the early 1980s it has been predicted that the limit in the spatial resolution of conventional fabrication has been reached and that the next generation of integrated circuits will have to be produced with synchrotron sources. X-ray lithography with synchrotron radiation has proved to be a valuable technique in the laboratory and can sustain comparison with deep-UV lithography and electron beam lithography regarding resolution, wafer throughput and process latitude. However, the conventional techniques have been improved constantly and there are only a few dedicated X-ray lithography light sources at major companies in Japan (NTT, Mitsubishi and Sumimoto) /38-39/ and one system at IBM's plant in Fishkill /40/, which was constructed by Oxford Instruments /41/. The transfer of synchrotron radiation lithography technologies to an industrial production environment just involves considerable problems that have yet to be overcome in order to be acceptable by the industry. If we are to believe current estimates /42/, then it will become a major technique in the year 2001 when UV techniques will reach their final limit.

The main limitation of the micro lithography process based on ultraviolet radiation exposure is caused by diffraction. The intrinsic diffraction limit in reproducing narrow features of the mask is approximately equal to the wavelength of the radiation. A typical photon source for UV lithography is the intense mercury line at 365 nm, although weaker sources exist at smaller wavelengths of 230 - 300 nm. The spatial resolution can be improved by using suitable demagnifying lenses. However, these lenses have a short depth of focus, i.e., they require very flat silicon wafers. Another serious problem are dust particles, which are strong scatterers of UV radiation in the above range.

These factors make it desirable to use radiation of shorter wavelengths. Besides removing the diffraction problem, shorter wavelength photons have the additional advantage of being less sensitive to dust than UV radiation. X-ray lithography can be in principle implemented with conventional sources, e.g. stationary anode sources and laser-induced plasma sources.

A synchrotron radiation source offers clear advantages /43/. The first one is the intensity of the synchrotron radiation source. This shortens the exposure time of each wafer and decreases the production costs. A second advantage is the small source size, which reduces the penumbra effect (figure 7a). The penumbra effect can be reduced also by placing the source far from the mask. This is easily achievable due to the third advantage of synchrotron radiation, namely the small divergence. The same considerations apply to another problem, illustrated in figure 7b. This is the geometrical distortion due to the different angle of incidence of a divergent X-ray beam in different areas of the mask. The technical term for this problem is "run-out". Once again, the small angular divergence of synchrotron radiation is extremely helpful in removing this problem.

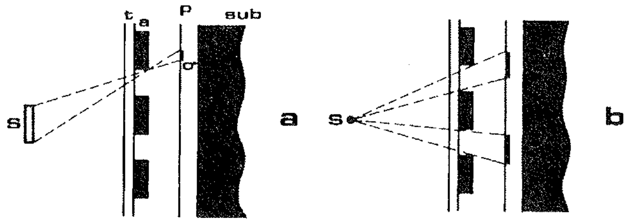

Fig. 7: Two problems affecting X-ray lithography with conventional sources: a) the finite size of the source causes penumbra effects, with an edge blurring corresponding to the area s and b) the divergence of the source causes distortions of the transferred pattern.
s - source, t - transmitting substrate,
a - absorbing pattern, p - photoresist,
sub - substrate.

Currently the most developed technique in terms of R&D is the so-called X-ray proximity lithography (XRL), where a mask with a patterned absorber is placed in close proximity (<50 μm) to a resist-coated substrate. New chemically amplified resists of high sensitivity (30-100 mJ/cm^2) and high resolution (0.1 μm) are commercially available /44/. X-ray steppers are also manufactured with an overlay performance in 3σ of 70-90 nm /45/ and have been used for device fabrication. High performance SRAMs in a 0.25 μm CMOS technology have been fabricated by IBM /46/. The NTT (Japan) program is also aimed at 0.25 μm CMOS /47/ and it is expected that the XRL technology can be pushed down to 0.1 μm or even 50 nm. Currently, the mask technology remains the key point to insure the complete success of XRL. It has been considerably improved in the last decade, but further improvements are still necessary.

An X-ray mask consists of a transparent flat membrane supporting opaque absorber structures. Membranes are formed by the deposition or growth on a silicon wafer. Their thickness must not exceed 3 μm in order to get enough X-ray transmission. Many materials have been studied in the last decade, as they have to meet a number of relevant properties: low roughness, flatness, robustness, high fracture strength, stiffness, stability under irradiation, large thermal conductivity, low thermal expansion coefficient, and visible optical transparency. Today, B doped Si /48/ are the most widely used in the US, while SiN_x is the current standard in Japan /49/. The best materials for future membranes seem to be SiC and diamond, but there is still some development to be done. The absorber is a high atomic weight material. Currently, Gold, Tungsten and Tantalum are the most used ones. The mask patterning is realised by a focused electron beam system with electron energies from 50 to 100 keV.

X-ray lithography does not require a high-resolution monochromator to filter the radiation emitted by the synchrotron radiation source. A wide band of wavelengths is typically used, since this increase s the total power reaching the wafer and decreases the exposure time. However, the exposing wavelength must be compatible with a relative good absorption in a resist film (i.e. 10-50% in a thickness of 1 μm), minimised diffraction effects and easy mask technology. This last requirement implies a reasonable transmission through the mask membrane (50-90%) and reasonable attenuation in an absorber for a film thickness no more than 4 times the minimum feature size. This fixes the optimum spectral range for XRL between 0.8 and 1.5 nm.

4.2 Liga

Three-dimensional microscale structures can be fabricated with the Liga process, which uses deep etch X-ray lithography, electroforming and plastic moulding. Development of the Liga process began at the Karlsruhe Nuclear Research Centre (KfK) in the late 1970s as an inexpensive method of producing very small slotted nozzles of any lateral shape for uranium isotope separation /50/. Liga is a German abbreviation of the three major process steps: lithography (Lithographie), electroplating (Galvanoformung) and moulding (Abformung).

A schematic diagram of the steps involved in fabrication of basic Liga microscale structures is shown in figure 8. In the first step the absorber pattern of an X-ray mask is transferred into a resist layer several hundred micrometers in thickness by X-ray shadow projection. Synchrotron radiation is used because of its very high collimation and short wavelength. The range used extends from 0.2 to 10 nm. The X-ray masks consist of a thin membrane (e.g. 3 μm titanium or 30 μm beryllium) together with absorbers consisting of gold layers that

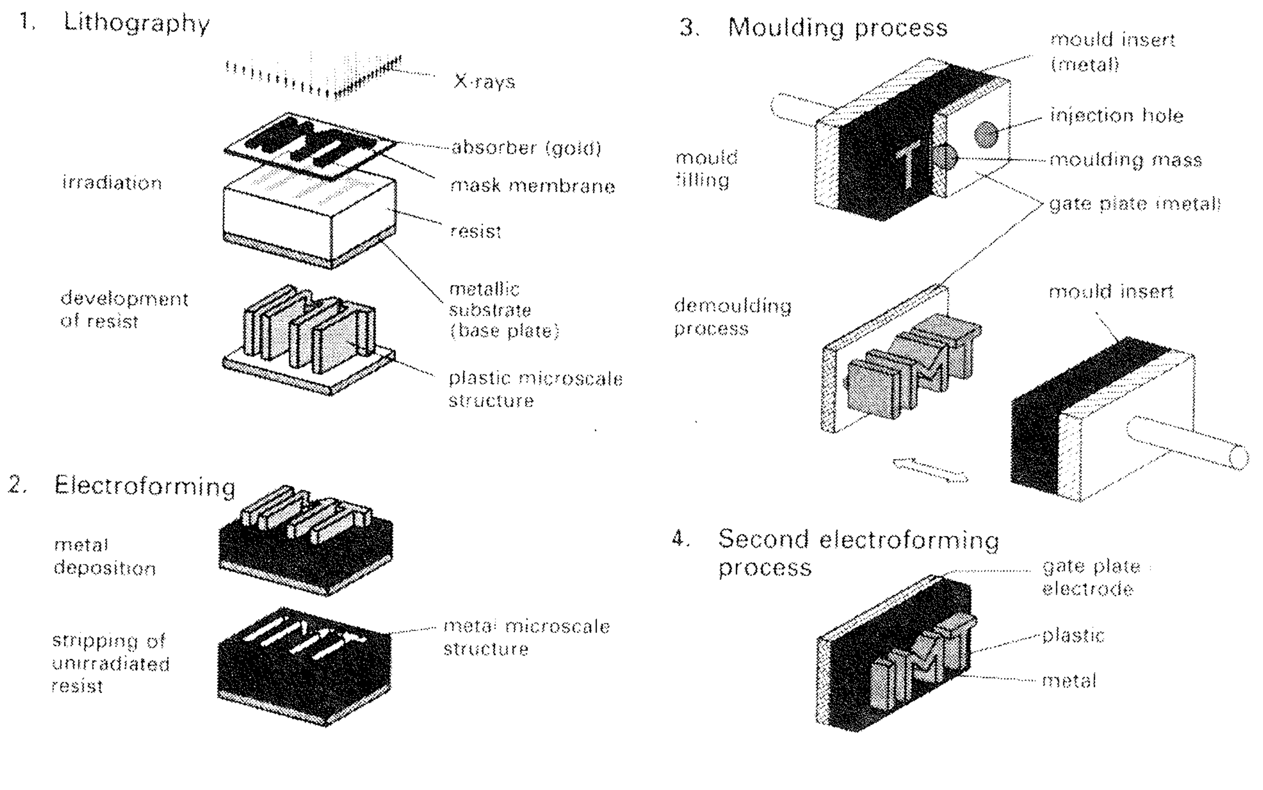

Fig. 8: The principal process steps for fabrication of microscale structures by the Liga technology.

are thicker than 10 μm in order to achieve the required mask contrast. Within the irradiated sections of the resist layer the polymer chains are destroyed, reducing the molecular weight. In most cases polymethylmethacrylate (PMMA) is used as the X-ray resist. During the subsequent development step, the exposed resist is selectively dissolved while the unirradiated parts remain unchanged. The unexposed regions of the resist, covered during irradiation by the absorbers of the mask, form the primary microscale structure.

Electrodeposition on a microscale can then be employed to build up a complementary pattern in a metal such as copper, nickel or gold, by filling the empty spaces of the electrically non-conducting resist. The metal pattern produced in this way can then be used to manufacture, with a high degree of detail and at relatively low cost, almost any number of plastic copies by means of moulding processes such as reaction injection moulding, thermoplastic injection moulding and hot embossing of thermoplastics.

The latter is particularly suitable for moulding microscale structures on processed silicon wafers, e.g. on microelectronic circuits /51/.The wafer, already carrying the protection and metallised layers, is laminated with the moulding compound. In the next step the wafer and the plastic material are heated and an evacuated mould insert is pressed into the moulding compound. Once the compound has cooled the mould insert is removed. A wide variety of plastic materials can be patterned by these moulding techniques, including PMMA, polycarbonate, polyamide, polyethersulfone, polyoxymethylene, polyvinylidene fluoride and epoxy resin.

The plastic structures can again be filled with metal in a second electroforming process. Therefore, metallic microscale structures can also be fabricated in a cost effective way. As an example, in figure 9a a micro mesh honeycomb structure made of nickel is shown, which was built up on a processed silicon wafer by the embossing and electroforming technique.

In order to obtain partly or totally movable microscale structures together with fixed structures on a single substrate, a integrated fabrication technology, based on a sacrificial layer technique, has been developed /52/. The substrate is first coated by physical vapour deposition with a thin (<1 μm) metallic layer, which is patterned by photolithography and wet etching. This layer serves both as a plating base and as an electrically conducting level for the finished structures. In the second step a sacrificial layer, about 5 μm in thickness, is deposited on the substrate and also patterned by the same methods. Titanium is used as sacrificial material because it adheres well to the resist and to the electrodeposited layer and can be etched with hydrofluoric acid which does not attack the materials (chromium, silver, nickel, copper) usually used in the Liga process.

The standard Liga process is then used: polymerisation of the thick X-ray resist directly on to the substrate, exposure to synchrotron radiation through a precisely adjusted mask, development of the resist and electrodeposition. Some parts of the metallic microscale structures will be built up on the first metal layer, while other parts lie on top of the sacrificial layer. After stripping the resist, the sacrificial layer is etched selectively against all other materials, exposing some parts of the micro structure.

With the techniques described above, the Liga process may be used to fabricate microscale structures of any lateral shape and with the following characteristics:

- structural heights up to and greater than 1 mm
- edge details less than 0.25 μm in dimensions
- lateral dimensions of the order of a few micrometers
- sub micrometer accuracy over the total height of the structure.

New process steps /53/ permit even a variation of the geometry in the third dimension in order to produce stepped structures and structures with inclined sidewalls. One of the most novel features of the Liga process is the wide variety of materials that may be used, including plastics, metals, alloys and ceramics.

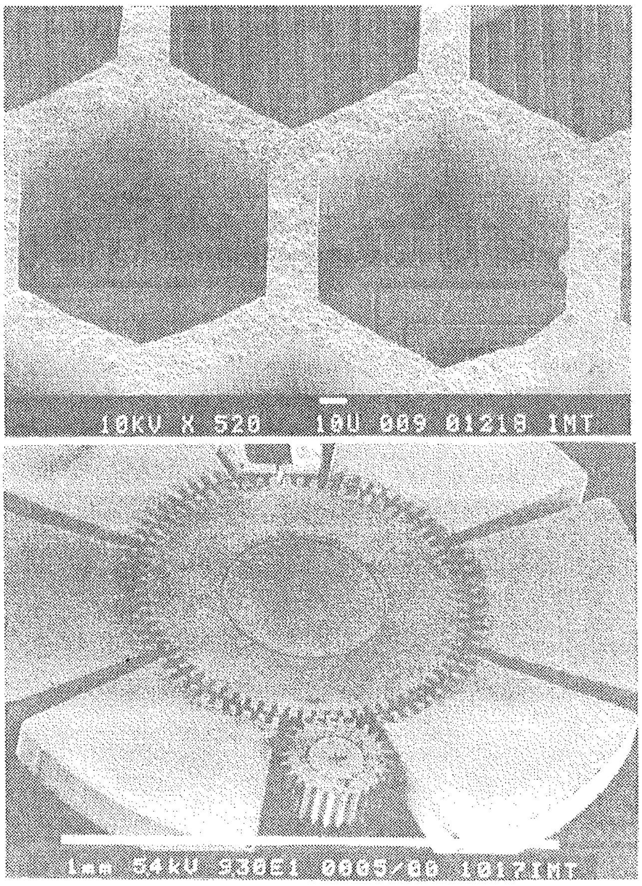

Fig. 9: Two examples of microfabricatrion with Liga: a) Nickel honeycomb structure fabricated on processed silicon wafer by the hot embossing technique and the electroforming process: width of walls 8 µm, height 100 µm; b) Electrostatic nickel micromotor with toothed rotor (dia. 700 µm) and stators, gear wheel (dia. 250 µm) for torque transmission and fixing groove for optical fibre to allow speed measurement: gaps between rotor and axle and rotor and stators 4 µm, height 120 µm.

A list of movable micro structures produced include physical sensors and actuators, such as acceleration sensors, turbines, linear electromotors, circular electromotors (figure 9b) and pumps. /54/. Numerous further microscale structures are under development, for example: micro coils, ultrasonic sensors, electrostatic linear actuators, springs and micro optical components /55/ which are used for optical communication technology and fibre optical sensing. In future, the combination of Liga process technology with other micro fabrication techniques such as anisotropic etching of silicon or reactive ion etching will greatly expand the number of applications by taking advantage of the special benefits provided by these individual technologies. Particularly promising are medical applications for minimal invasive therapy where lies the greatest interest for micro structures .

5. THE SYNCHROTRON LIGHT SOURCE ELETTRA

The Trieste synchrotron light source ELETTRA /56/ is the world's brightest light source in the UV and soft X-ray region. As such it further extends the possibilities of research with respect to existing light sources. The storage ring operates at an energy of 2 GeV with an electron current of 200 mA, to be increased to 400 mA in a later phase. The total circumference of the machine with 24 bending magnets is 260 m. Eleven straight sections can be equipped with 4.5 m long insertion devices, each feeding two beamlines. A wiggler can serve two beamlines simultaneously, while the light cone from an undulator is too small to be split in two. Therefore, a switching mirror distributes the light between the two attached beamlines. In addition, 13 bending magnets may be used as light sources for experiments with 2 beamlines per magnet. Over 25 beamlines have been proposed up to now, out of which 8 are already in operation or in the phase of commissioning (table 1). The first official operation run with experiments that have been selected from proposals through an international scientific review committee has started recently (August 30-th).

6. THE BEAM LINE BOSS

Triggered by the proximity of this excellent source, researchers in Slovenia have established the collaboration BOSS (Beam line Of Slovenian Scientists) which seeks ways to perform research at ELETTRA and to construct the beam line BOSS.

Since the beam line BOSS is a national project, it has to allow as many experiments as possible to researchers from Slovenia, as long as they can be reasonably well performed on BOSS, even though some fields may be covered by other beamlines. Hence BOSS is a multipurpose beam line, employing the following experimental methods: XAS (X-ray absorption spectroscopy, i.e. XANES - X-ray absorption near edge structure and EXAFS - extended X-ray absorption structure), XRF (X-ray fluorescence) and XPS (X-ray photoelectron spectroscopy), with the possible extension to WAXS (wide angle X-ray scattering), SAXS (small angle X-ray scattering) and XSW (X-ray standing wave).

*Table 1: The main characteristics of the beamlines currently or shortly in operation. The last two (marked with an asterix *) employ special focusing optics such that the photon beam size is only 50 nm. The photon spectral flux in this spot is of the order of 10^9 photons/s/0.1%b.w. . The other beamlines have beam sizes around 0.1 - 1 mm and have fluxes in the range from 10^{12} - 10^{14} photons/s/0.1%b.w. .*

Name	Eph [keV]	resolution	experiments
SuperESCA	0.1 - 2	10000	high resolution and/or high flux ESCA; photoelectron diffraction; studies of dynamic surface phenomena
VUV Photoemission	0.02 - 1.2	10000	semiconductor surfaces; interface formation; high-T superconductors; electronic structure of metals and their surfaces
ALOISA	0.25 - 8	5000	surface X-ray diffraction; photoelectron diffraction; coincidence experiments
Diffraction	5- 25	>1000	determination of macromolecular biological structures; studies of temporal variations of structures
SAXS	5.4, 8, 16	1000	material physics; polymer science; biomembranes
GasPhase Photoemission	0.02 - 1.2	12000	gas phase reactions of chemicals; chemistry of combustion; electronic structure of gas atoms and molecules
Spectromicroscopy*	0.02 - 0.8	3000	high lateral resolution photoemission, used for highly inhomogeneous solids, micro crystals, biological structures; study of localised bad-bending phenomena caused by imperfections in semiconductors
ESCA microscopy*	0.1 - 2	3000	high lateral core level photoemission for the same topics as above

A recent survey among research groups in Slovenia has shown that there is interest practically in all experimental methods that can be offered by ELETTRA. Fortunately, more than 70% of the requests can be fulfilled by a single beam line operating in the X-ray region between 2 and 12 keV. About two thirds of those want to utilise absorption spectroscopy, in particular EXAFS or one of its flavours (SEXAFS, fluorescence EXAFS).

The EXAFS spectroscopy is a particularly interesting method for the industry, too. An analysis of recent industrial use of the SRS at Daresbury /57/ shows that 47% percent of the use is allocated to experiments with EXAFS making it the most widely used method for industrial synchrotron radiation research.

The beam line BOSS has been therefore designed primarily for absorption spectroscopy, exploiting the high spectral flux and small source point of the ELETTRA bending magnet as compared to other X-ray sources. The spectral region covers either the K-edge or the L-edge of almost all elements between and including phosphorous (Z=15) and platinum (Z=78), giving sufficient tunability for a wide range of absorption experiments. The limits actually come from the absorption in the C and Be filters below 2 keV and from the poor reflectivity of the gold coated mirror above 12 keV /58/.

The expected characteristics of the beam line are a good photon energy resolution (3000 to 6000) in the range between 2 keV (0.62 nm) and 12 keV (0.1 nm), high spectral flux from a bending magnet source (about 10^{12} monochromatised photons/second over the whole spectral region), small focal spot size on the sample (below 1 mm^2) and a vertical divergence below 0.4 mrad /58/. These characteristics are probably sufficient also for XSW experiments, therefore XSW is considered as a potential method even though no proposals were submitted from Slovenian researchers yet.

The other two methods that have been requested by Slovenian research groups and are well suited to the characteristics of BOSS are fluorescence and photoelectron spectroscopy. None of them is covered by other beamlines at ELETTRA in the complete range between 2 and 12 keV. The main purpose of electron detection at BOSS is to allow total electron and Auger yield measurements for SEXAFS. However, the equipment can be set up in order to allow electron spectroscopy, too. The photon energy range of BOSS does not fall into the classical XPS region, although some useful spectra may be obtained at the lowest energy range from 2 - 3 keV.

Yet the higher photon energies could be efficiently exploited for some specific topics like:

- thick films, in particular buried interfaces, where the larger thickness forbids the penetration of low energy electrons to the surface
- the study of the change of the ratio between the main and satellite peaks between low and high energy photons, which is due to the difference between the adiabatic and sudden transitions.

Furthermore, the photoelectron spectra at these higher photon energies are relatively unexplored and it is always possible that new interesting phenomena could be observed. Therefore a thorough investigation of photoelectron spectra with BOSS might prove useful.

Photoelectron spectra obtained from BOSS are of interest also for atomic physics to study correlated processes in events with multiple photoelectron emission. Some proposed experiments include:

- Auger spectroscopy of satellite and hyper satellite lines;
- threshold spectroscopy for double K shell ionisation;
- Auger spectroscopy;
- determination of fluorescence yields and Coster-Kronig transition rates.

X-ray scattering already sees two dedicated beamlines at ELETTRA, the diffraction and the SAXS beam line (see table 1 above). However, the characteristics of BOSS allow also a range of scattering experiments and this can be exploited in order to allow Slovenian users immediate usage without having to wait for beam time at the dedicated lines. In addition, due to the fixed wavelengths of the SAXS beam line, BOSS is a possible candidate for anomalous SAXS experiments.

The main experimental chamber will be equipped to allow several types of measurements of the absorption coefficient, via the detection of the transmitted flux as well as the secondary processes like fluorescence, photoelectrons and Auger electrons. The chamber will allow the addition of particular sample chambers which will allow the study of crystalline, amorphous, liquid and gaseous samples under different temperatures, pressures and other physical and chemical conditions. Measurements of trace elements with XRF will be possible with the same chamber.

Other experiments will need a dedicated experimental chamber, such as surface science experiments, or dedicated detectors, such as atomic physics experiments, which is beyond the scope of the proposed project. However, the Slovenian beam line will deliver the proper type and quality of radiation. The chambers and specialised detectors will be constructed or are already under construction by individual users, like an energy and a wavelength dispersive X-ray spectrometer, an electron energy spectrometer, a four crystal monochromator, etc. Attachment ports for several kind of experimental chambers and detectors are foreseen.

For surface mapping, the addition of a glass capillary microprobe is envisaged, giving spatial resolution to all of the aforementioned methods of about 10 - 30 μm /59/ or even down to 1 μm /60/. For some cases the use of a PEEM (photoelectron emission microscope) camera is considered, giving a resolution of 0.5 μm and better /61/. A four crystal monochromator to be added after the mirror will provide a resolving power of 10000 whenever needed.

The scientific case, where 35 proposals from Slovenian research groups have been presented /62/, has been recently approved by the Programme Advisory Committee of Sincrotrone Trieste. It is planned that once funds for the project become available, the beam line should be constructed in two years time.

7. CONCLUSIONS

Synchrotron radiation has proven to be a potentially powerful tool both for basic and applied research. The great success of the new third generation light sources has already triggered plans for other machines and even ideas for fourth generation machines. Maybe the only reason why many laboratory-based scientist have not used synchrotron radiation in their research yet, is the fact that synchrotron radiation is available only at large, centralised facilities.

However, the complexity and cost of modern experimental science is forcing experimenters to look for equipment that may not be available at the home laboratory. Some scientists may not like this trend, but it is a reality with which we must cope. Fortunately, due to the increasing supply of synchrotron radiation from all those sources and the construction of new national and regional sources (like Elettra) we can expect rapid expansion of research made with synchrotron light and - what is important for small groups - the continuation of free access both in financial and in scientific terms.

Whether synchrotron radiation will become the standard of industry based production of microelectronics and micro mechanics and whether all large IC producers will have their own compact synchrotron sources in their production plants still remains an open question. Technical problems notwithstanding, the feasibility of synchrotron radiation lithography has been clearly demonstrated in a number of prototypical production tests. It is definitely a challenging and highly expanding field.

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Dr. Mark Pleško, dipl.ing.
Institut "Jožef Stefan"
Jamova 39, POB 100, 61111 Ljubljana,
Tel.: +386 61 1773 900
Fax: +386 61 1261 029
E-mail: Mark.Plesko @ijs.si

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SPACE CHARGES IN MATERIAL SCIENCE

Gerhard Herzog
Institut für Chemische Technologie Anorganischer Stoffe
Technische Universität Graz, Austria

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Key words: material science, space charges, electric charges, interfacial phenomena, liquid materials, contact regions, semiconductor materials, electroceramic materials, electrolytic materials, practical applications, photoactive materials, semiconductor interfaces, dry solar cells, electrolytical solar cells, solutions, Debye-Hueckel theory, dielectric media, MOS transistors, varistor effect, PTC effect, Positive Temperature Coefficient effect, passive layers, photo catalysis

Abstract: Whenever two different liquid and/or solid materials are brought into contact with each other, interfacial phenomena occur. Space charges, built up in the contact region or interface are the key to their understanding. In some electrical components or devices at all, space charges are intentionally used, but in many other cases they are undesired and must be eliminated. In an introductory review principles and applications of space charges in and at electrolytical (I), semiconducting (II) and electroceramic (III) materials are described. A special application of space charges are photo or solar devices (IV), which will finally be discussed.

The reason for including electrolytical systems is a historical one too, because the treatment of space charges by Debye and Hückel, aiming at chemical and electrical properties, was carried out a long time ago before solid contacts became interesting. However, the goal of their treatment is so general, that we can easily transfer and extend the basic ideas to nowadays modern materials and devices.

Prostorski naboji v znanosti o materialih

Ključne besede: znanost o materialih, naboji prostorski, naboji električni, pojavi vmesniški, materiali tekoči, področja stična, materiali polprevodniški, materiali elektrokeramični, materiali elektrolitični, aplikacije praktične, materiali fotoaktivni, področja stična polprevodnikov, celice sončne suhe, celice sončne elektrolitične, razstopine, Debye-Hueckel teorija, mediji dielektrični, MOS transistorji, efekt varistorski, PTC efekt koeficienta temperaturnega pozitivnega, plasti pasivne, kataliza foto

Povzetek: Kadarkoli stopita dve različni tekoči ali trdni snovi v kontakt, pride do površinskih pojavov. Prostorski naboji, ki se tvorijo v območju kontakta ali na površini, so ključ za razumevanje teh pojavov. V nekaterih elektronskih komponentah površinske naboje namenoma uporabljamo, drugje pa so nezaželjeni in se jih želimo znebiti. V prispevku na pregleden način podajamo osnove in opisujemo uporabo prostorskih nabojev v in na elektrolitičnih (I), polprevodniških (II) in elektrokeramičnih (III) materialih. Posebno področje uporabe prostorskih nabojev so foto, oz. sončne komponente (IV), o katerih bomo govorili na koncu.

Razlog, zakaj smo v ta prispevek vključili tudi elektrolitične sisteme, je deloma zgodovinski, saj sta prostorske naboje obravnavala že Debye in Hückel. Njiju so predvsem zanimale njihove kemične in električne lastnosti, čeprav je bilo njuno delo opravljeno preden so meje in stična področja med snovmi v trdnem stanju sploh postale aktualne. Kljub vsemu je njuna obravnava tako splošne narave, da jo lahko mirno prenesemo in razširimo na področje današnjih modernih materialov in komponent.

I. SPACE CHARGES WITHIN SOLUTIONS

Debye-Hückel theory

Any ensemble of localised or mobile electronic or ionic charge carriers in a dielectric medium builds up a charge distribution or space charge. Look at the simplest and most familiar case, i.e. ions in an electrolytical solution. Cations and anions are mobile because of thermal agitation in the dielectric material of water. They arrange themselves by the action of electrostatic forces until the minimum of free system energy is reached.

Ions in a solution don't order in a lattice structure, because their thermal energy is too high. As well they are hydrated with water dipoles, which break long range ordering. Looking, however, at nearest ion-ion distances, we observe a certain kind of order. Each hydrated cation is surrounded by an ion shell, which itself is on the average negatively charged. So we can speak of an ion cloud around the cation, which makes it heavy and sluggish, when it is forced to move in an electrical field. This cloud is also the reason why ions move with about the same velocity or mobility and show relaxation effects like dipoles.

The structure of the cloud is governed by electrostatic interactions between the hydrated ions and their thermal agitation. The cloud structure is necessarily centrosymmetric. All we have to do for a quantitative treatment is to solve the Poisson-Boltzmann equation, which is merely a combination of the electrostatic Poisson equation and a statistical Boltzmann expression for the charge density ρ (pair function):

$$\Delta\varphi \sim \rho$$

$$\sim \sum_i q_i c_i e^{-q_i\varphi/kT} \qquad (1)$$

A power series expansion and some abbreviations lead to the following simplified differential equation for the electrical potential φ in the neighbourhood of the central cation:

$$\Delta\varphi = \beta\varphi \qquad (2)$$

The parameter β contains the ionic charges q_i, the concentrations c_i, the temperature T and the dielectric constant of water ε. Solving equ. (2) to a first approximation one obtains for the electrostatic potential

$$\varphi(r) \sim \frac{1}{r} e^{-\sqrt{\beta}\, r} \qquad (3)$$

and for the charge density profile:

$$\rho(r) \sim -\frac{\beta}{r} e^{-\sqrt{\beta}\, r} \qquad (4)$$

As shown in fig.1 both the potential $\varphi(r)$ and the space charge density $\rho(r)$ behave exponentially /1/. The so-called Debye-radius $1/\sqrt{\beta}$ is a measure for their mean spatial extension. In other words, the central ion is screened by the ionic cloud to a more or less extent, depending mainly on the ionic carrier concentration or ionic strength. The higher the concentration the stronger is the screening and the thinner is the space charge around the central ion. The energy difference between the isolated and the screened central ion corresponds to the difference of the chemical potential of the cation and is therefore related to the activity coefficient. This concept is only valid for low-concentrated solutions.

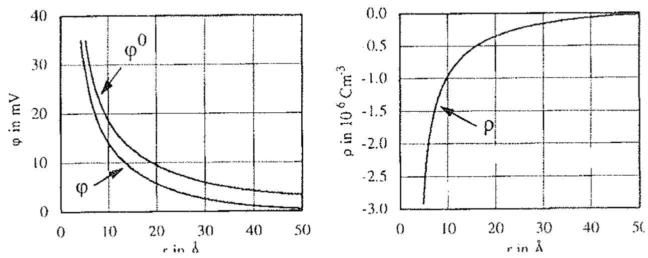

Fig.1: Potential and density profiles

Electrolytical space charge at a metal electrode

When a metal electrode is dipped into a solution and is external charged, it creates also an electrolytical space charge with a similar exponential behaviour of charge and potential profiles. Here traditionally the ionic arrangement is called diffuse double layer. Once again, with great ion concentrations the diffuse layer is relatively thin and what remains is a kind of surface instead of space charge. It is most probably mixed with adsorbed and oriented water dipoles.

Only when the metal is polarisable the contact can be biased externally, otherwise an electrochemical reac-

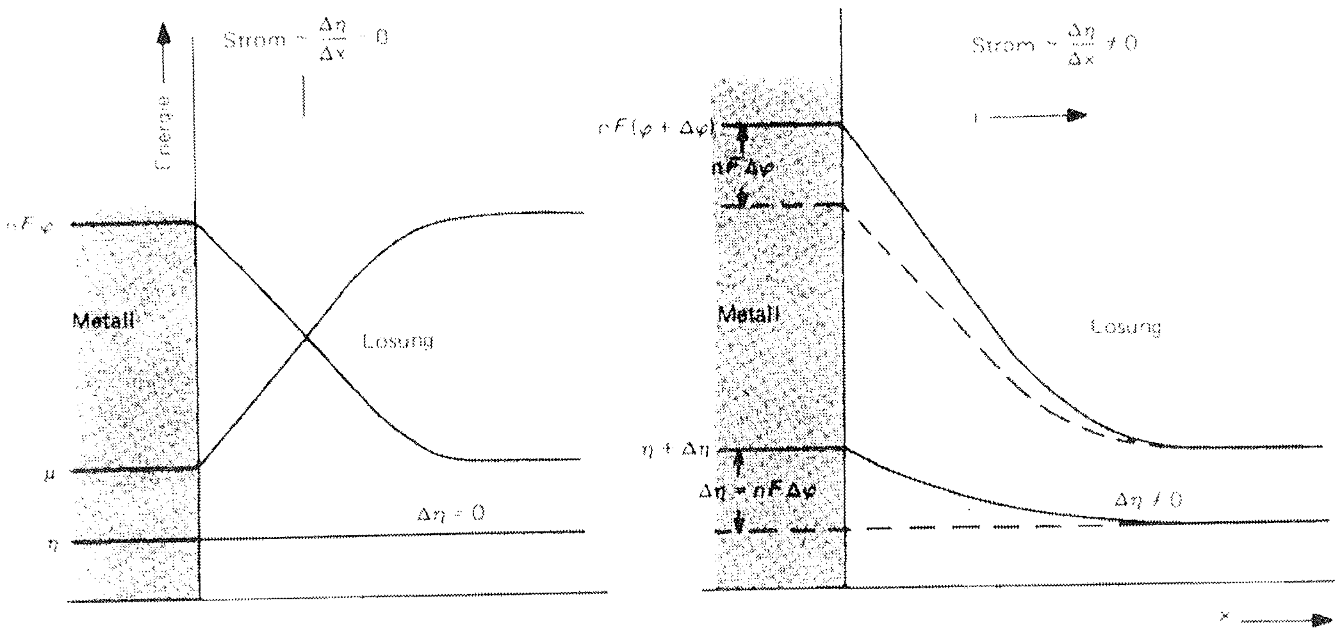

Fig. 2: Electrochemical equilibrium and non-equilibrium

tion proceeds. Equilibrium and non-equilibrium, described by the difference of the electrochemical potential η of exchangeable particles in both phases, is schematically shown in fig.2. In the situation $\Delta\eta \neq 0$, a faradaic current due to some reaction will flow /1/.

Measurement of electrolytical space charges

Spatial dependences of charges and potentials at interfaces cannot be measured directly. By electrical means we can only observe overall or statistically averaged

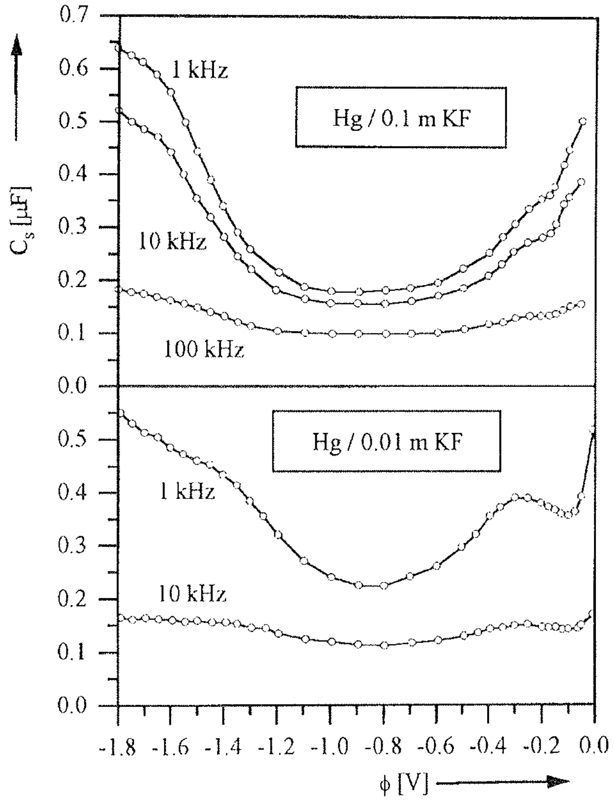

Fig. 3: The potential (vs. Hg/HgO) dependence of double-layer capacitance at 30 °C

properties as the integral or differential capacitance. As space charges at interfaces act like ensembles of dipoles the most convenient experimental method is impedance spectroscopy in the frequency or time domain. Both domains are interconnected via Fourier transformation. Physically most profitable results are obtained by capacitance/voltage dependences and relaxation time analysis. In the years 1975 to 1980 we especially studied contacts with metallic micro-electrodes. The experimental curves in fig. 3 show, that the differential capacitance vs. voltage behaves parabolic with superimposed humps /2/. When the parabola are ascribed to faradaic capacitances, the humps remain to be explained.

Explanation by an adsorption model

From our experimental studies a simple thermodynamical adsorption model for ions at metal contacts was claimed /3/. The basic assumption is an electrochemical equilibrium between dissolved ions A, free adsorption states B and adsorbed ions AB with a Langmuir-like concentration dependence. By differentiation of the adsorbed charge with respect to the electrical potential drop between the surface and the bulk phase an expression for the differential capacitance is obtained. Although in this model only one kind of ions is involved and adsorbed water dipoles as well as a diffuse layer were neglected, it gives a good approach of the observed capacitance/potential behaviour and predicts humps on both sides of zero potential quite easily (fig. 4).

$$\Delta\eta = \Delta\mu + e\Delta\varphi = 0 \tag{5}$$

$$\Delta\eta = -kT\,\ln K + kT\,\ln\frac{c_{AB}}{\left({}^{0}c_{AB} - c_{AB}\right)c_B} + e\Delta\varphi = 0 \tag{6}$$

$$c_{AB} = {}^{0}c_A\,\frac{1}{1 + \dfrac{1}{Kc_B}\,e^{e\Delta\varphi/kT}} \tag{7}$$

$$C = \frac{\partial e c_{AB}}{\partial \Delta\varphi} = \frac{e^2}{kT}\,{}^{0}c_A\,\frac{Kc_B e^{e\Delta\varphi/kT}}{\left(Kc_B + e^{e\Delta\varphi/kT}\right)^2} \tag{8}$$

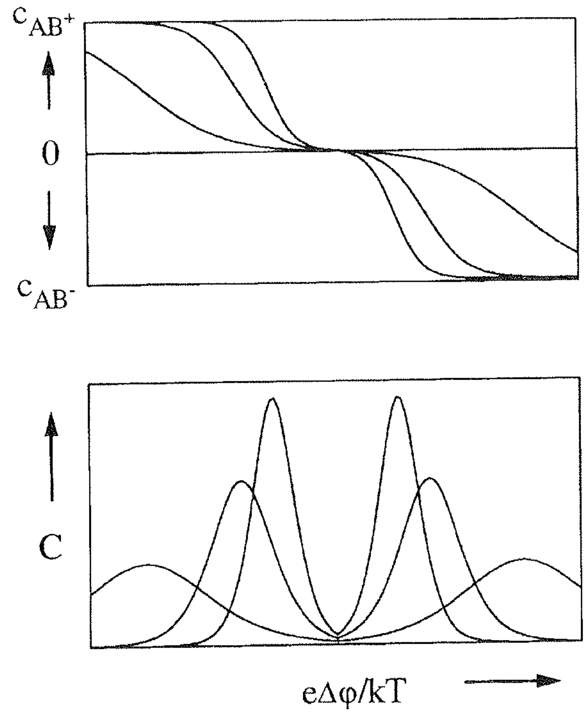

Fig. 4: Adsorbed ion density and differential capacity

Simulation of electrolytical space charges

Since the ab initio treatment of metal-electrolyte contacts is quite impossible, we tried to get more insight by a grand canonical Monte-Carlo simulation using the most simple potential functions for ion-ion and ion-metal interactions. The solution was simulated by hard sphere ions in a homogenous water dielectric, because ten years ago the application of soft potentials, allthough now available was too CPU time consuming.

According to the above mentioned adsorption model the chemical potential difference of the surface and the bulk phase of the solution must be calculated. The surface phase is enriched with ionic excess charges because of its contact with an externally charged wall. Since this can only be done in a grand canonical simulation, our Monte-Carlo program with Metropolis sampling was adapted to a grand canonical (μ,V,T) ensemble with variable ion number N. The simulation procedure consisted of the following steps /4/.

1. Movement of a random ion as in canonical simulation with an analogous exponential probability.
2. Stochastical decision if an ion is added or subtracted and continuation with step 3 or 4.
3. Ion addition at a random position in the system and acceptance probability with new ion number N. Continuation with step 1.
4. Ion subtraction using a randomly selected particle with a proper acceptance probability. Continuation with step 1.

In the following the transition probabilities p_{ij} are given. ΔU is the potential energy change of the whole particle configuration. The free parameter B contains the chemical excess potential μ' and the equilibrated particle number N' /5/:

$$p_{ij} = 1 \qquad for \quad \frac{\Delta U}{kT} \leq 0 \qquad (9)$$

$$p_{ij} = e^{-\Delta U/kT} \qquad for \quad \frac{\Delta U}{kT} > 0$$

$$p_{ij} = 1 \qquad for \quad \frac{1}{N} e^{B-\Delta U/kT} \geq 1 \qquad (10)$$

$$p_{ij} = \frac{1}{N} e^{B-\Delta U/kT} \qquad for \quad \frac{1}{N} e^{B-\Delta U/kT} < 1$$

$$p_{ij} = 1 \qquad for \quad Ne^{-B-\Delta U/kT} \geq 1 \qquad (11)$$

$$p_{ij} = Ne^{-B-\Delta U/kT} \qquad for \quad Ne^{-B-\Delta U/kT} < 1$$

$$B = \frac{\mu'}{kT} + \ln N' \qquad (12)$$

After a simulation run with a given parameter B the excess potential or activity coefficient γ is found:

$$\gamma = e^{B-\ln N'} \qquad (13)$$

The simulation procedure was proved by calculating the concentration dependence of the activity coefficient in comparison with the first and second Debye-Hückel approximations. For the simulation of metal-electrolyte contacts the metal-ion interaction was modeled by the effective potential

$$V = \frac{PeZe}{4\pi\varepsilon_0 x} \qquad (14)$$

The external potential, equivalent to the potential drop $\Delta\varphi$ between the metal and the solution, is established during simulation by the ionic density profiles and is varied implicitely via the parameter P.

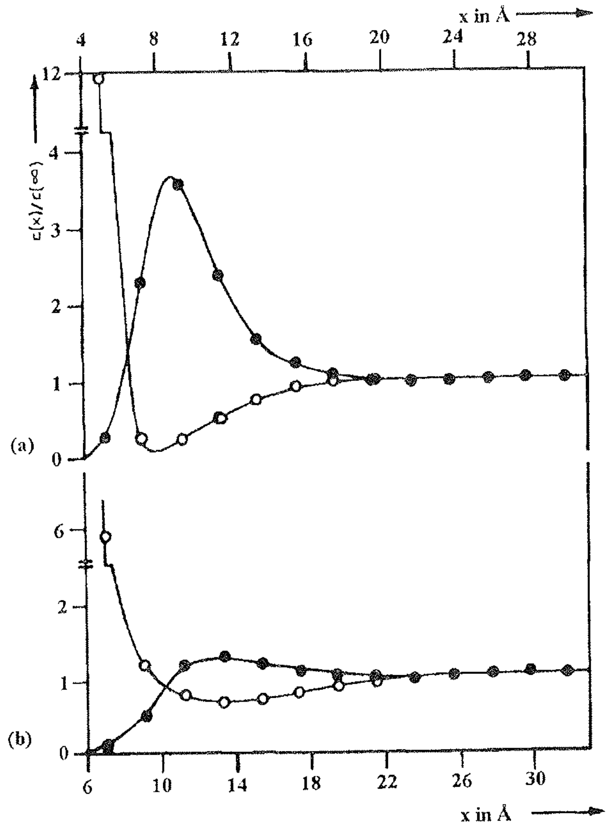

Fig. 5: Simulated density profiles of anions (o) and cations (•) with metal charge Pe at x = 0 and metal boundaries at x = 4 (a) and x = 6 Å (b)

Results of simulation

Two typical examples of profiles are shown in fig. 5. Both anions and cations are accumulated in the surface phase of about 20 Å extension. From the difference of the total ion numbers N' the excess charge q is obtained. Comparing the system with a plate condenser, one is able to calculate by means of the Poisson equation the electrical potential drop at the metal-electrolyte contact:

$$\Delta\varphi = -\frac{q\bar{x}}{\varepsilon_0\varepsilon F} = -\frac{q}{\varepsilon_0\varepsilon}\int_{x=0}^{\infty}(c_+ - c_-)x\,dx \qquad (15)$$

The main goal, however, of this simulation work was to obtain charging curves from which by differentiation the differential capacitance is obtainable (fig. 6). At small potential drops the hard sphere system behaves like an ideal plate condenser. With increasing charge there is an increase of the differential capacitance as expected, but unfortunately because of missing CPU time we could not wait until a hump came out.

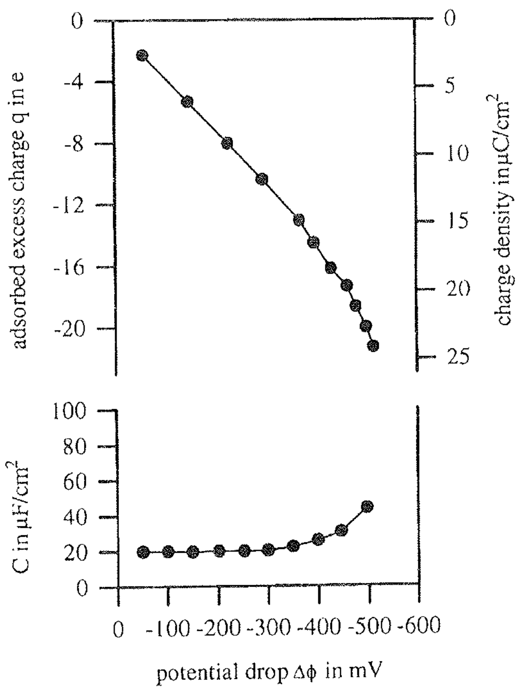

Fig. 6: Simulated charge density and capacity curves

Experiences from the study of electrolytical space charges

Before switching over to a discussion of some real and practically more important solid-solid contacts, let us summarise what we can learn just from electrolytical space charges.

- Space charges or double layers occur between two chemically different and eventually externally charged phases, when mobile ions or electron/holes are present.
- The charge and potential profiles are connected through the Poisson equation. They extend exponentially into the bulk phase, and look like double layers when the mobility of the charge carriers is high.
- Equilibrium is given by the balanced electrochemical potential within two phases being in contact, beyond equilibrium reactions with charge transfer will occur.
- In general, charge and potential profiles cannot be measured directly, only potential drops and capacitances with the help of plate condenser model. Charging and/or capacitance depend non-linearly on external bias.
- To interpret charging or capacitance curves potential models preferring either surface or diffuse profiles, have to be introduced but remain ambiguous.
- Computer simulations can support the interpretation of statistical properties as the capacitance, but they depend on proper atomic potentials.
- Generalisation to solid-solid interfaces is only a gradual step, bearing in mind that the mobility of charged species can be very different.

II. SPACE CHARGES IN AND AT SEMICONDUCTORS

As already mentioned, it is very instructive to discuss space charge phenomena with respect to their practical importance. So, some applications of semiconductor-electrolyte interfaces concern corrosion and photo processes, which can be desired or undesired.

When we dip a metal like Fe, Zn, Al, Si or Ti into a corrosive solution, the growing oxide layer behaves like a semiconductor because of unoxidised metal atoms. On the other hand the same will happen with Si in an O-containing atmosphere at high temperatures (see SiO_2 formation in MOS technology). Advanced formation of an intact layer lowers the rate of corrosion, which is very useful, although corrosion itself is not. The semiconducting properties of the oxide layer control the progress of the corrosion via transport of mass and charge. Of course any external bias can enlarge or prevent this process by the formation of space charges at both sides of the interface, one within the semiconductor and one within the electrolyte. In the following we don't take care of the latter and confine ourselves to the first.

Space charges in semiconductors

When a semiconductor is externally charged a space charge in the surface region is built up. From the solution of Poisson equation with FD statistics for mobile electrons or holes and neutrality condition, three different cases can be distinguished (fig. 7): Accumulation, depletion and inversion of majority carriers. For small surface charges the solution for potential and density profiles is once more an exponential function of extension, the Debye-length now given by

$$L = \sqrt{\frac{\varepsilon\varepsilon_0 kT}{e^2(n+p)}} \qquad (16)$$

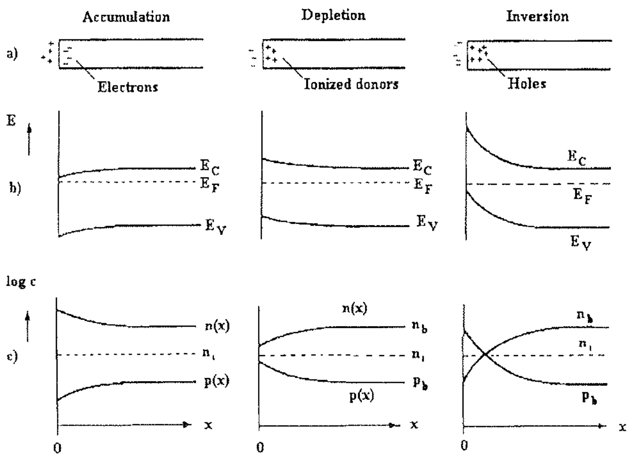

Fig. 7: Charge distribution (a), electron energy (b) and carrier concentration (c) of space charge layers in n-semiconductors, taken from /6/

Following Schottky the depletion case can be treated with a separate approximation, if all donors are ionised and the charge density is merely given by the constant donor density N. From twofold integration the potential proftle (0<x<d) and the band bending φ_s at the surface (x = 0) is obtained

$$\varphi_s = \frac{eN}{2\varepsilon_0\varepsilon} d^2 \qquad (17)$$

As the total space charge within the region d is q=edN:

$$\varphi_s = \frac{q^2}{2\varepsilon_0\varepsilon Ne} \qquad (18)$$

and 1/C = dφ /dq, we obtain a very useful expression for determining donor densities from capacitance measurements:

$$\left(\frac{1}{C}\right)^2 = \frac{2}{2\varepsilon\varepsilon_0 Ne}\varphi_s \qquad (19)$$

There are a lot of applications of equ. (19), two of them are shown in fig. 8 and 9. They concern ZnO-crystal- and corroded Zn-electrolyte contacts to confirm semiconduction of the as-grown oxide layers /7/. We will return to the depletion case in the discussion of electroceramic components.

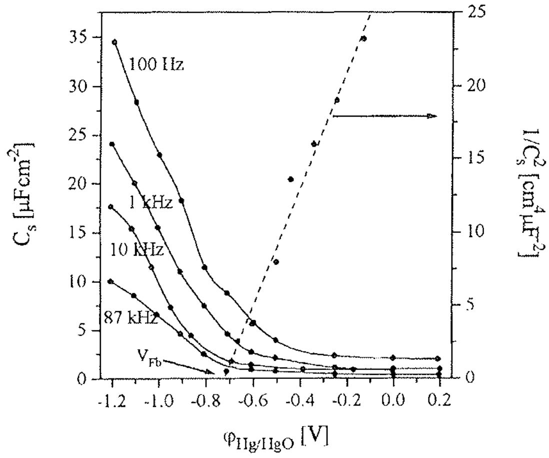

Fig. 8: Potential dependence of double layer capacitance C_S of ZnO - 0.1 M borax at various frequences

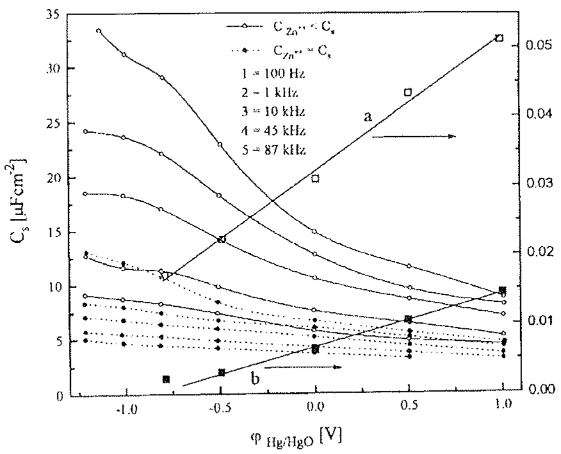

Fig. 9: Schottky plots of corroding Zn - 0.1 M borax without (a) and with (b) correction due to the electrolytical capacitance

The MOS transistor

Todays best-known and most important application of space charge theory is the MOS transistor, which operates under inversion condition. The transistor principally consists of a MOS capacitor, to which a gate voltage is applied, and of drain-source electrodes attached to the channel region to pick up the drain current (fig.10).

As can be seen from drain current/voltage curves for operation a certain minimum gate voltage the so-called threshold voltage is necessary. Inversion is established, when the band bending φ_S is twice the difference of the Fermi and donor or acceptor energy ϕ. In this case the minority carrier density at the surface becomes as large as the majority carrier density in the bulk. The corresponding energy situation is outlined in fig. 11.

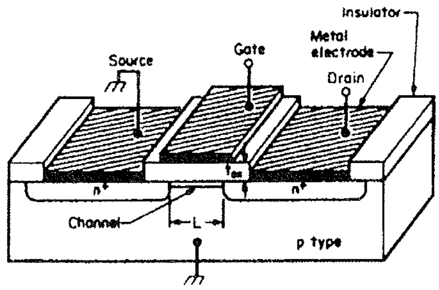

Fig. 10: n-channel MOS transistor, taken from /8/

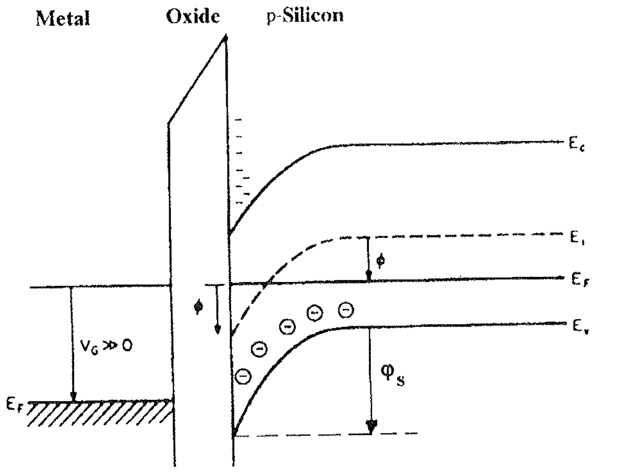

Fig. 11: Band bending in the case of inversion

Dielectric and charge balance considerations lead to the central expression for the treshold voltage of n-channels:

$$V_T = V_{Fb} + \frac{1}{C_0}\sqrt{2e\varepsilon_s\varepsilon_0 N(2\phi + V_G)} + 2\phi \qquad (19)$$

In the ideal case the flat band voltage $V_{Fb}=0$, otherwise V_{Fb} is determined by the difference of the work functions V_{MS} and the space charges located near the Si-SiO2-boundary.

$$V_{Fb} = V_{MS} + \sum \frac{space\ charges}{C_0} \qquad (20)$$

ε_S is the dielectric constant of Si, N the acceptor density, C_0 is the oxide capacity and ϕ is the above defined energy difference. In the theory so far we have assumed an uniform substrate doping. But in a real MOS-device, the doping profile is far from uniformity. Impurity ions will be redistributed during thermal processes and ion implanted profiles are intentionally applied /9/ for a better design of devices (fig. 12).

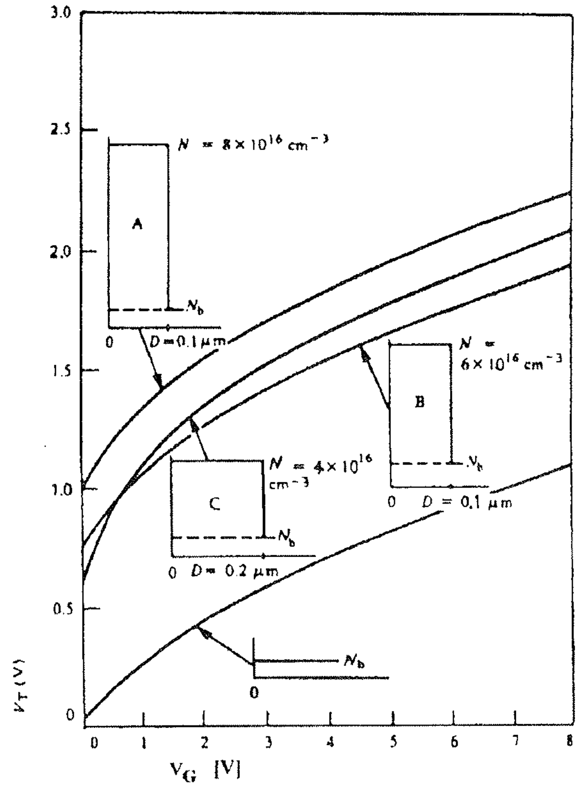

Fig. 12: Calculated treshold voltage for some cases of implantation, taken from /9/

MOS capacitance/voltage plots

As with metal-electrolyte contacts most instructive knowledge about space charges within MOS-structures are obtained from CV measurements (fig. 13). It is easily realized what is measured with such a setup. With negative gate bias p-type silicon is in accumulation and the capacitance (C) is simply that of a parallel plate condenser with SiO_2 as the dielectric (C_0). At a gate voltage V_G that is more positive than the flatband voltage (V_{FB}) depletion is established and creates a space charge capacitance in series. When the gate voltage exceeds the threshold voltage inversion is formed and then the total capacitance depends on the measuring frequency. If in the high frequency case the inversion layer cannot follow the AC field the total capacitance will be minimum (C_{min}) and stay constant with increasing gate voltage. Deep depletion is only observed with fast enough potential scan.

A simple analysis for the CV curves in the depletion and inversion region yields

$$\frac{C}{C_0} = \left(\sqrt{1 + \frac{V_G}{V_0}}\right)^{-1} \qquad \left(V_0 = \frac{eN\varepsilon_s\varepsilon_0}{2C_0^2}\right) \tag{21}$$

$$\frac{C_{min}}{C_0} = \left(\sqrt{1 + \frac{V_T}{V_0}}\right)^{-1} \tag{22}$$

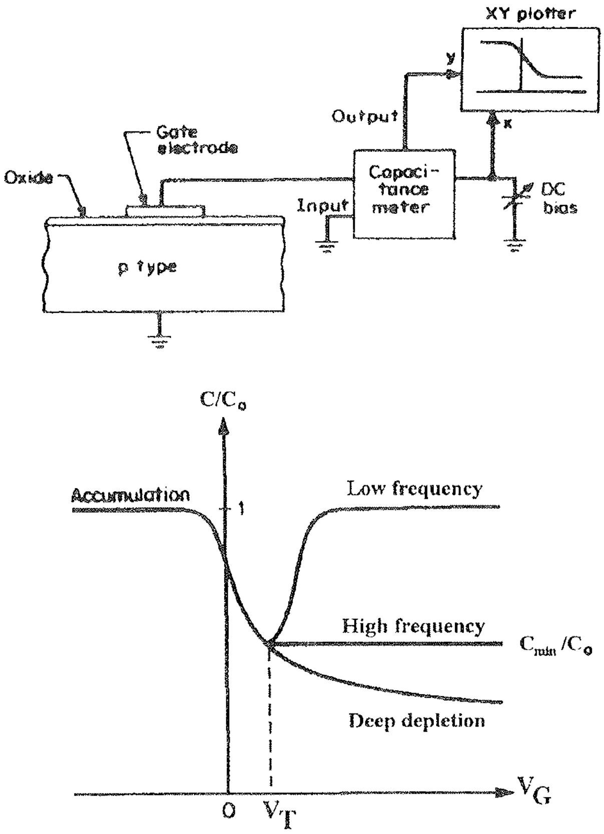

Fig. 13: CV setup and frequency dependent CV plots, taken from /8/

each of them causing characteristical shifts or other kinds of deviation.

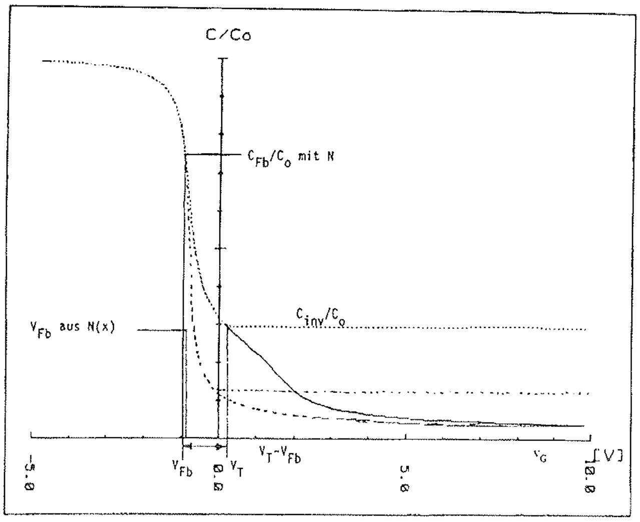

Fig. 14a: CV plots of implanted (upper curve) and native (lower curve) p-material

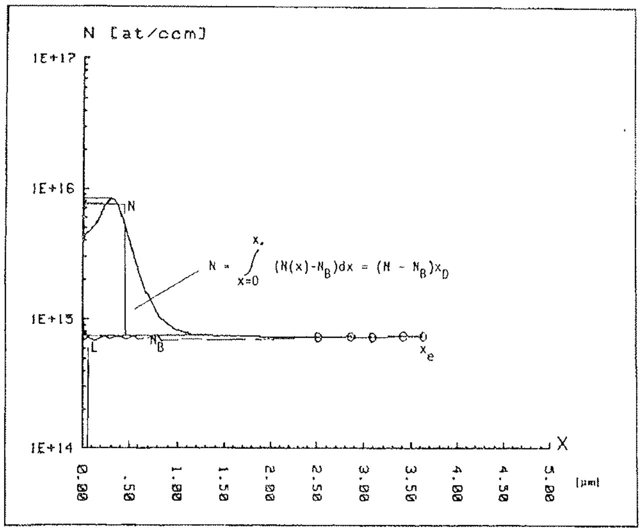

Fig. 14b: Evaluation of implanted profiles

From CV plots implanted regions can be evaluated (fig. 14) /10,11/ and undesired space charges can be identified /12/. They must be minimised during the processing of devices. However, the structural mismatch between Si and SiO_2 is an intrinsic property /13/. In general one has four types of charges with the thermally grown oxide interface /14/,

1) fixed oxide charges,
2) mobile ionic charges,
3) interface states and
4) oxide trapped charges,

III. SPACE CHARGES IN AND AT ELECTROCERAMIC MATERIALS

The key effects in electroceramic components as ZnO varistors and PTC's made of doped $BaTiO_3$ are most probably a crucial consequence of space charges at grain boundaries, and not of internal blocking layers or external electrode contacts. In a stochiometric composition both materials are insulators with band gaps of about 3 eV. By a proper doping of single crystals with aliovalent impurities both materials become n-semiconducting, ZnO showing band and $BaTiO_3$ polaronic conduction. However, in a ceramic material up to a certain breakdown voltage ZnO and above the Curie temperature $BaTiO_3$ are insulators.

Double Schottky layers

What is desired in electroceramics? Good varistors should have a steep current increase at the breakdown voltage (especially for low-voltage protection) and PTC's should have a steep resistance increase at a certain temperature. Although both characteristics look very different, their underlying basic electrical phenomenon is quite the same. At grain boundaries inside the same ceramic material acceptor surface charges are assumed to be generated during processing, which themselves create space charges at each side of the boundary /15,16/. So a double Schottky depletion layer with an energy barrier is formed (fig.15).

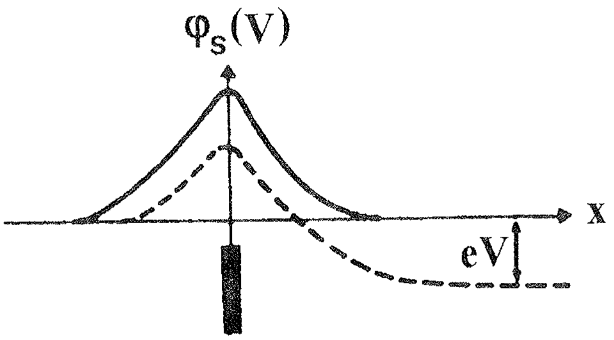

Fig.15: Energy barrier without and with external bias

According to equ. (18) the barrier height is proportional to the square of the surface trap density N_T at the boundary and inverse to the donor density N:

$$\varphi_s = \frac{N_T^2 e}{2\varepsilon_0 \varepsilon N} \tag{23}$$

As conduction electrons have to overcome the barrier (activation energy), the resisivity ρ increases exponentially with temperature:

$$\rho \sim e^{e\varphi_s/kT} \tag{24}$$

By application of an external voltage V the barrier $E \equiv e\varphi_s(0)$ is reduced and the resistivity ρ changes accordingly.

$$\varphi_s(V) = \varphi_s(0)\left(1 - \frac{V}{4\varphi_s}\right) \tag{25}$$

The varistor effect

Usually current/voltage curves of varistors (fig.16) are fitted by

$$I \sim V^{\alpha} \qquad \left(\alpha = \frac{V}{I}\frac{dI}{dV}\right) \tag{26}$$

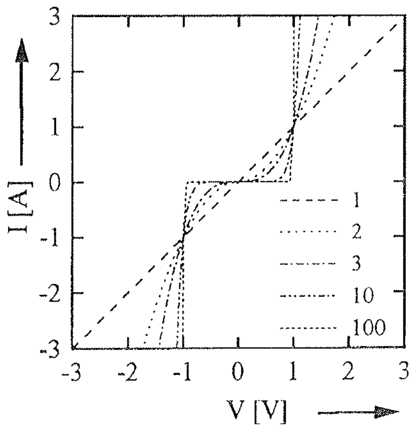

Fig.16: Schematic current/voltage curves, taken from /16/

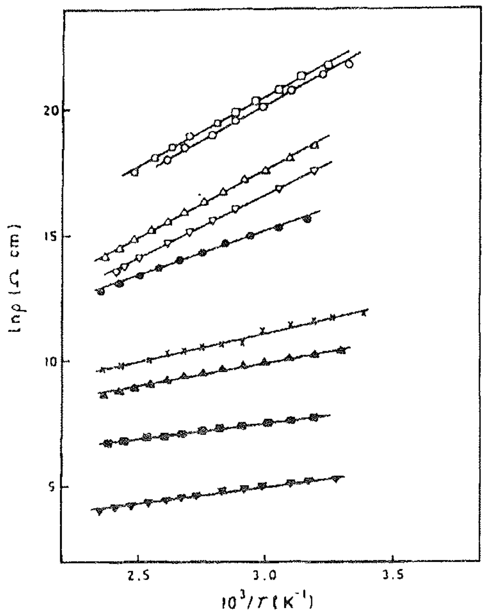

Fig. 17: DC resistivities of a differently quenched ZnO varistor

An example for a double Schottky layer evaluation is taken from /17/. In fig.17 and 18 DC resitivities vs. temperature and CV plots are reproduced. According to equ. (24) from the slope of resitivity at low voltages the barrier height is found to be of the order of 0.5 eV, but depends strongly on the quenching temperature. Reciprocal CV plots according to equ.(19) give straight lines, from which donor and acceptor densities can be obtained.

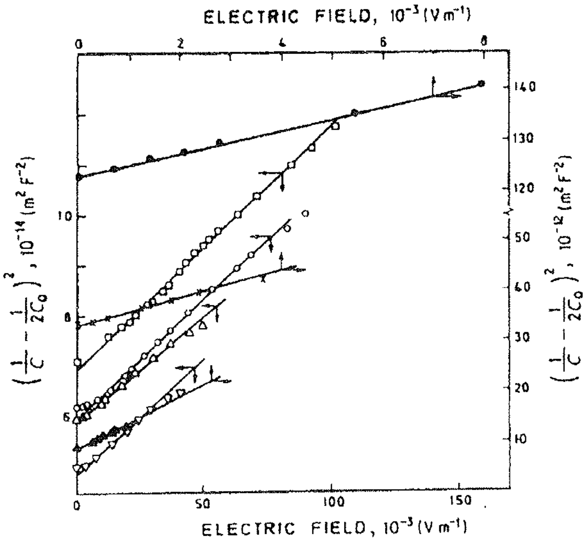

Fig. 18: *Schottky plot of a differently quenched ZnO varistor (C capacitance; C_0 zero field capacitance)*

Results of the evaluation are plotted in fig.19. At processing temperatures higher than about 800 °C defect equilibrium and barrier formation seem to be established.

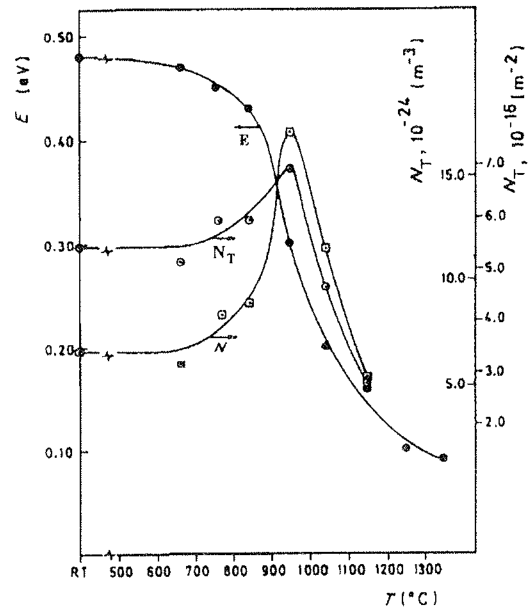

Fig.19: *Dependence of activation energy E, donor density N and trap density N_T on quenching temperature*

The dielectrical breakdown of ZnO varistors begins beyond 3.2 V per grain boundary, which is equal to the band gap energy. For the steep current increase a lot of different tunnelling models have been proposed (fig. 20) /18/. For the explanation of the extremely non-linear current the minority carriers in combination with ionic lattice defects seem to play an essential role. A lot of work on chemical tailoring of varistors, beginning with Matsuoka /19/ has been done especially by Kolar et al. /20/.

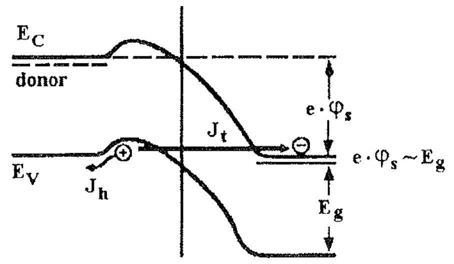

Fig. 20: *Zener band to band tunneling, taken from /16/*

The PTC effect

The PTC characteristics, i.e. DC-resistivity of about 10Ωcm below and about 6-8 orders, of magnitude higher above the Curie temperature, is easily understood from equ.(23-25). Below the Curie temperature the dielectric constant of $BaTiO_3$ is by a factor of about 100 greater and the barrier height lower than above. Thus the PTC characteristics is not only a space charge effect, but coupled to the ferroelectric property of the base material $BaTiO_3$. Without donor doping $BaTiO_3$ would behave as a capacitor, which is also widely used in electroceramics. As with all electroceramic components, PTC processing is made at high temperature, so

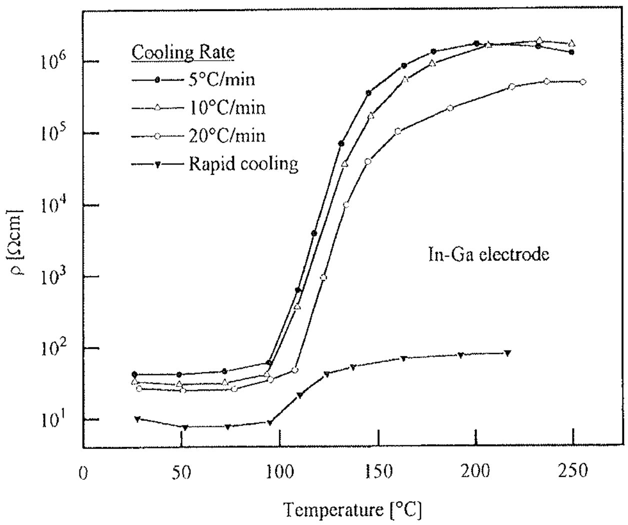

Fig. 21: *PTC effect for different cooling rates /21/*

that sintering temperature, soaking time, cooling rate etc. influence dramatically the formation of the barrier layers at the grain boundaries (fig. 21).

From impedance measurements the following simple equivalent circuit consisting of an ohmic bulk resistance, a grain boundary and an electrode interface impedance is proposed (fig. 22).

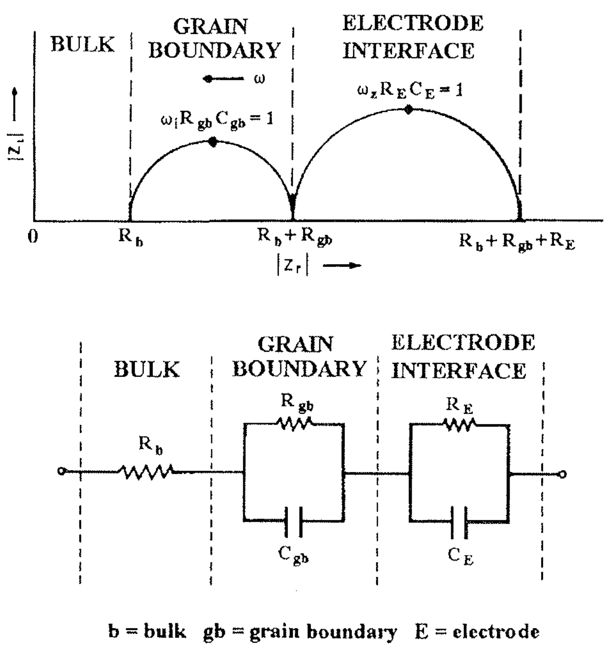

Fig. 22: Generalised impedance diagram and equivalent circuit /21/

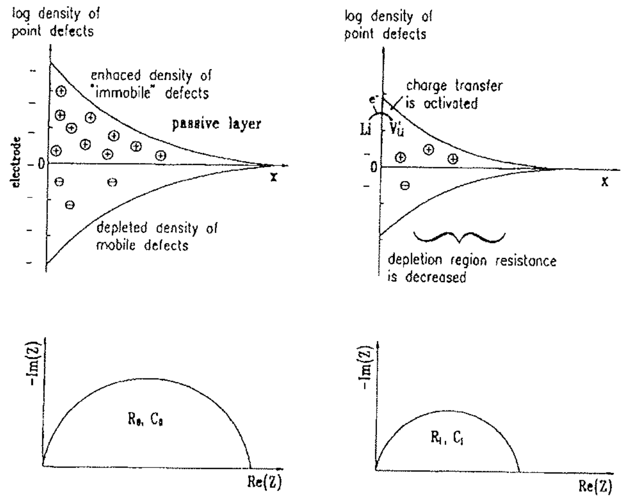

Fig. 23: Space charge model for Li-passive layer without and with bias, taken from /22/

Passive Layers

Ionic space charges within passivating layers may play an important role for the mass transport e.g. in Li-batteries. Nowadays great effort is made to develop layered batteries. The key to more progress in this technology seems to be the nature of the passive layer between metallic Li and the electrolyte, which roughly can be compared with a polycrystalline ceramic layer.

$Li\text{-}SOCl_2$ ($AlCl_3$) contacts have been extensively studied by Pejovnik and coworkers /22/. The as-grown LiCl layer behaves like a good Li^+ conductor, at least because of Al^{+++} doping during passivation and growth. A space charge at the metal contact is assumed to be built up by depleted mobile Li^+ and enhanced immobile Cl^- vacancies, being responsible for the high ohmic resistance. When anodically biased, the depletion and the enhancement are lowered and the resistance decreases (fig. 23). As the accomodation of the space charge region needs some time, battery charging is delayed.

IV. SPACE CHARGES AT PHOTOACTIVE MATERIALS

Aspects of usefulness of space charges are to be considered, when a semiconductor interface is irradiated with light of band gap wavelength. The light will excite electrons from the valence to the conduction band, thus creating electron-hole pairs. After dissociation and some time of diffusion the charge carriers will combine radiationless. However, if this creation of holes happens within a region of high stationary electrical field, the pairs will be separated to give an electron and a hole current, in other words to give a photo current /23/. This photo current can be used in a positive practical sense in photo devices, but is awful when it leads to progressive corrosion or destruction of the semiconducting material /24/.

The sources of high electric fields are once again space charges, created at semiconductor interfaces. External biasing increases or lowers the space charge and thus the field. In the following the photo effect of some solar devices is qualitatively explained.

Dry Solar Cells

As shown in fig. 24 at a metal-n semiconductor-metal structure in the dark there is a certain band bending and electric field on both sides of the semiconductor. If one metal side is made transparent and illuminated with light of band gap, positive holes will flow to the negative charged metal and electrons to the opposite side. Thus a discharge of the illuminated space charge is obtained. At constant illumination a steady state will be reached, when in the decreasing field the production of electron-hole pairs is balanced by their recombination. In this non equilibrium steady state a difference of the metal Fermi levels arises, which is equivalent to a photo emf. If the external circuit contains a consumer, a photo current is observed. The same principle holds for Si pn-contacts, today being the most interesting commercial solar device.

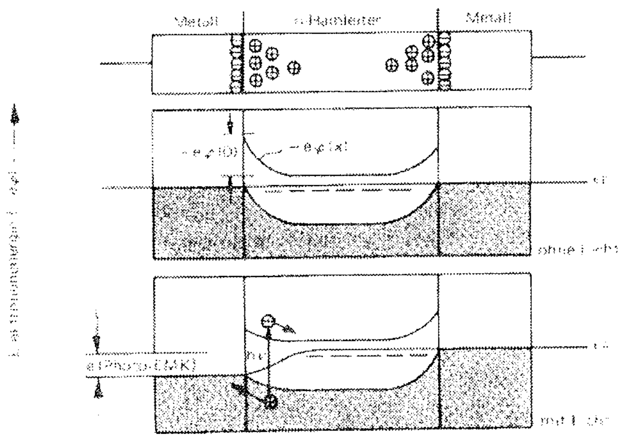

Fig. 24: Photo effect at a metal-semiconductor contact /1/

Electrolytical Solar Cells

Quite similar electron-hole pairs are generated in an electrolytical solar cell, which can be in combination with a counter electrode to give a solar battery. The basic component is a transparent semiconductor-electrolyte contact, whose diffuse space charge is able to separate photo electrons from holes (fig. 25).

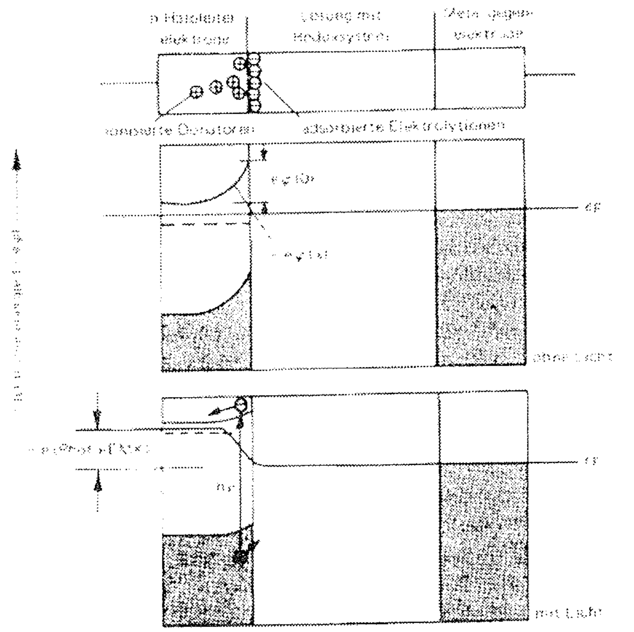

Fig. 25: Photo effect at a semiconductor-electrolyte contact /1/

However, instead of an external bias to create a space charge, the latter is here performed by an internal redox system. Under open circuit conditions the according Nernst potential is established and if this one is positive enough, a Schottky depletion layer will be formed. On illumination discharge and a photo emf will occur. If there are enough hole acceptors present in the electrolyte, and if there are corresponding reactions at the counter electrode possible, the device can act as a battery.

In the past one tried to construct regenerative and energy storing batteries, but two serious disadvantages prevented from a commercial application. Reasonable semiconductor electrodes were made of oxides or sulfides and these materials are 1. to a certain extent soluble in the electrolyte and 2. oxidable by the holes itself. Thus lattice anions are oxidised and the material decomposes.

Photo catalysis

Photo hole and electron production with subsequent reactions can be utilized in some chemical devices and for instance considered for waste water treatment. The degradation of organic material in waste water can be enhanced effectfully by suspending and illuminating TiO_2 powder within the band gap. A flux of oxidising holes and reducing electrons at the oxide surface will be the result of the illumination, so that one can speak of a catalytical photo effect.

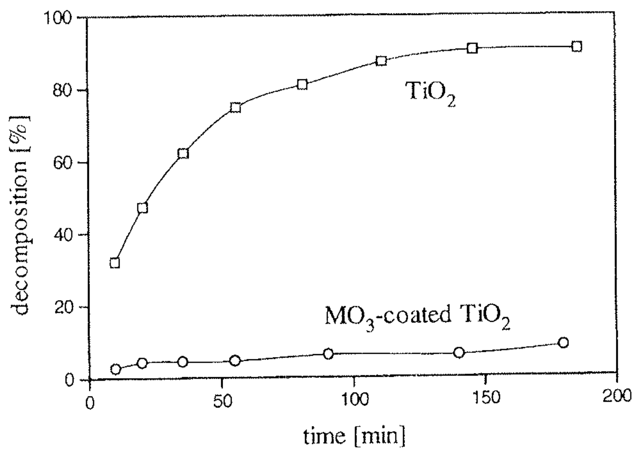

Fig. 26: Photo catalytical decomposition of dichlorpyridine into CO_2 in illuminated suspensions of MO_3- coated (o) and uncoated (□) TiO_2 powders /25/

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Dr. Gerhard Herzog, dipl.ing.,
Institut für Chemische Technologie
Anorganischer Stoffe
Technische Universität Graz,
A-8010 Graz, Stremayrgasse 16
Tel.: +43 316 873 82 85
Fax: + 43 316 83 76 19

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THE PIN/TCO/NIP SOLAR MODULE

W. Kusian[1], J. Furlan[2], G. Conte[3]
[1]Siemens AG, Corporate Research and Development, München, Germany
[2]University of Ljubljana, Faculty of Elect. and Comp. Eng., Ljubljana, Slovenia
[3]ENEA, CRIF, Portici, Italy

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Key words: solar modules, solar cells, a-Si, amorphous silicon, pin, positive-intrinsic-negative structures, nip, negative-intrinsic-positive structures, semiconductors, TCO, Transparent Conductive Oxide, TCO layers, very highly efficient solar cells, thin-film solar cells, polycrystalline silicon, a-Si:H, Hydrogenated amorphous Silicon, SWE, Staebler-Wronski-Effect, pin/TCO/nip parallel connected structures, laser patterning, i-layers, intrinsic layers

Abstract: Solar cells made from amorphous silicon normally have the structure pin and degrade under prolonged illumination. This paper proposes a new cell type with the structure pin/TCO/nip. Using a suitable module design, an integrated solar module can be produced with laser patterning. The incorporation of buffer layers at the n/i and i/p junctions in nip cells improves their performance, making it as good as that of pin devices under illumination through n. In initial pin/TCO/nip cells, the total efficiency is higher than in the front pin cell alone.

Sončni modul s strukturo pin/TCO/nip

Ključne besede: moduli solarni, celice sončne, a-Si silicij amorfni, pin strukture pozitivno-notranje-negativno, polprevodniki, nip strukture negativno notranje-pozitivno, TCO oksid transparentni prevodni, TCO plasti, celice sončne z izkoristkom zelo visokim, celice sončne tankoplastne, silicij polikristalinični, a-Si:H silicij amorfni hidrogeniziran, SWE Staebler-Wronski efekt, pin/TCO/nip strukture paralelne, risanje vzorcev lasersko, i-plasti notranje

Povzetek: Sončne celice, izdelane iz amorfnega silicija, imajo ponavadi strukturo pin in degradirajo, če so izpostavljene daljši osvetlitvi. V prispevku opisujemo novo sončno celico s strukturo pin/TCO/nip. Ob uporabi ustrezno načrtanega osnovnega modula lahko izdelamo integriran sončni modul s pomočjo laserske litografije. Dodane plasti na n/i in i/p spojih nip celic izboljšajo njihove lastnosti, ki postanejo primerljive s pin celicami, ko jih osvetlimo skozi n plast. V pin/TCO/nip celicah je celoten izkoristek višji kot pa pri sami pin celici.

1 Introduction

The research work in the field of photovoltaics for terrestrial applications comprises two basic directions: One is the development of very highly efficient solar cells made from crystalline silicon /1/ and the other is the development of thin-film solar cells. The latter direction has the advantage of reduced material consumption, which is very cost effective. Thin-film solar cells can be made from various materials, e.g. CdTe /2/, CIS /3/, polycrystalline silicon /4/, and hydrogenated amorphous silicon (a-Si:H) /5/.

The conventional a-Si:H solar cell has the structure pin. For small areas, the maximum achieved efficiency with this cell type is 13 % /6/. For larger areas, the initial efficiency of solar modules is already greater than 10 % /7/. The main application for amorphous silicon solar cells is in consumer products such as watches, pocket calculators and small battery chargers. However, the use of a-Si:H solar modules in power applications is impeded mainly by the light-induced degradation of performance during operation (Staebler-Wronski-Effect, SWE) /8/.

Several investigations have shown that the SWE is not a direct interaction between the material and the light but an indirect one. The photogenerated carriers can recombine or can be trapped in defect states within the material, and this leads to the production of metastable states. Although the microscopic origin of the effect is still not clear, it has been shown that a reduction of recombination or trapping probability will improve the stability of the cell. One way to do this is to increase the electric field across the i-layer in the pin structure. For this, thin i-layers are required /9/, but then the absorption path for light is also reduced and leads to smaller photocurrents.

Sufficient light absorption together with a strong electric field can be obtained in multi-junction solar cells /10/. These structures consist of thin single pin junctions stacked upon each other. The summation of such junctions leads to a sufficient total cell thickness. Double-junction solar cells, in which the individual junctions are made from the same material, are called double-stacked cells. The junction facing the incoming light is called the top cell while the remaining one is the bottom cell.

Conventionally, double-stacked solar cells have the structure pin/pin and are electrically in series. Although these devices behave more stably than single-junction cells /10/, their main disadvantage is that the photocurrent generated in both junctions has to be equal. This represents a very stringent condition with respect to the two i-layer thicknesses. Stability requirements dictate an upper limit for the i-layer thickness of the bottom cell of approximately 350 nm, and this consequently demands very thin i-layers of less than 80 nm for the top cell. This stringent requirement is even more problematic for large area solar module fabrication because of the thickness fluctuation and the use of textured substrates. An additional restriction is that the photocurrent matching condition can only be optimized for one spectral distribution of the sunlight irradiance. Changes in the solar spectrum during the day or the year always lead to a reduction in the conversion efficiency of the total stacked device.

One can avoid these problems along with the current matching requirement by connectiong the two junctions within the double-stacked configuration electrically in parallel /11/. Then, the generated photocurrents simply add up and only the photovoltages generated at the maximum power point have to be equal in both diodes. In this paper, we wish to demonstrate how a double-stacked solar module with parallel connections can be implemented and to describe the andvantages as well as the problems with this type of module.

2 Cell design and fabrication

2.1 The pin/TCO/nip design

The stacked cell with prallel connections can be implemented by depositing the layer sequence TCO/pin/TCO/nip/TCO. Fig. 1 shows the basic device structure in detail. On a glass substrate coated with a transparent conductive oxide (TCO), first the pin diode is deposited with conventional deposition parameters. For the front TCO layer, for example, fluorine-doped SnO_2 or boron-doped ZnO can be used. After the a-Si:H pin deposition, a second TCO layer follows in order to contact the n-layer. For this TCO layer, doped ZnO is a suitable material because of its low process temperature (170°C) at which no damage of the underlying a-Si:H layers occurs. The deposition of the nip diode is made with the same conditions as for the pin diode, but with the reversed deposition sequence. The third TCO layer, the back electrode, completes the device. This solar cell structure represents a three-terminal device. The parallel connection of the two subcells is made by externally connecting the front and back TCO electrodes. The implementation of the parallel connection can be made in an integrated solar module. Fig. 2 shows a cross-sectional view of such an integrated solar module. The five different patterning steps have to be performed immediately after the deposition of the layer. The front TCO is patterned into stripes by laser scribing, the lift-off technique, or mechanical patterning. For the patterning of the a-Si:H pin layer, laser scribing is best. This second cut must be offset slightly from the first one. The second TCO layer is patterned slightly beside the second cut. The patterning cuts of the a-Si:H nip diode have to lie above the cuts of the pin diode and the front TCO layer, respectively, (i.e. cut 4 is above cut 2 and cut 5 is above cut 1). With this arrangement of the patterning cuts of the two diodes (subcells) and the three TCO layers, two connecting modes are implemented. The parallel connection is implemented by connecting the two p-layers of one solar cell stripe. The series connection is made by connecting the n-layer (middle TCO-electrode) of one solar cell stripe with the p-contact (front and back TCO-electrode) of the neighboring solar cell stripe. For clarification, a circuit diagram is also shown at the top of Fig. 2.

The modelling of the light characteristics of a parallel connected stacked solar cell was performed with a simulation program using numerical methods to solve the Poisson equation and the continuity equations for electrons and holes /12/. Fig. 3 shows simulated current-voltage characteristics and AM1.5 sunlight of the total stacked device together with the characteristics of the two subcells. The thicknesses of the two i-layers were 200 nm and 400 nm for the top and bottom cell, respectively. As can be clearly seen, the filtered light

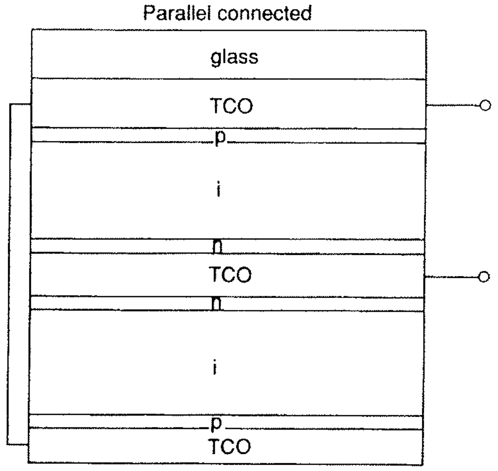

Fig. 1: Basic device structure of the parallel-connected stacked pin/TCO/nip solar cell.

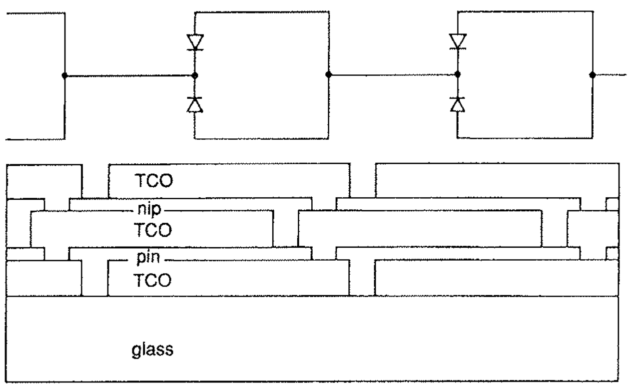

Fig. 2: Cross-sectional view of the integrated solar module, consisting of parallel-connected stacked solar cells together with the related circuit diagram.

from the top cell only generates a small short-circuit current in the bottom cell. However, there is nearly no difference in the photovoltage of two subcells at the maximum power point. Therefore, the output power of the individual subcells adds up with almost no electrical loss to the output power of the total device.

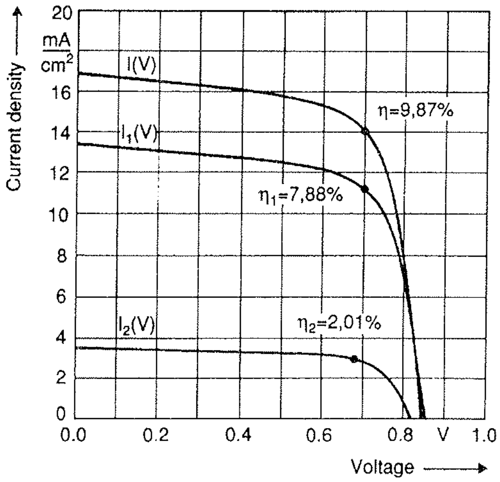

Fig. 3: Computed current-voltage characteristics under AM1.5 light of the individual pin and nip cells in a stacked solar cell and of the composite pin/TCO/nip parallel connected structure

2.2 Amorphous Silicon Technology

For the fabrication of a-Si:H films for solar cells, even on an industrial scale, the plasma enhanced chemical vapour deposition technique (PECVD) is always used /13/. Fig. 4 shows schematically a deposition apparatus. Two electrodes are located within a distance of approximately 40 mm in a vacuum chamber. Both electrodes can be heated. The bottom electrode is grounded and serves as a substrate holder. The top electrode is connected to the rf power supply and normally operates at a frequency of 13.56 MHz. The pumping system controls the pressure during the deposition process in a range from 0.1 mbar to 0.5 mbar. The gas mixing system regulates the amount and composition of the process gases used. For the deposition of intrinsic a-Si:H films, only silane gas (SiH_4) is necessary. The rf transmitter burns a glow discharge between the two electrodes. The gas molecules form a plasma, are decomposed, and are partially deposited onto the substrate. By adding doping gases such as diborane (B_2H_6) or phosphine (PH_3), one can also deposit p- or n-doped layers, respectively. Furthermore, the optical band gap can be enhanced by adding methane gas (CH_4), and reduced by adding germane gas (GeH_4). Etching gases such as CF_4 or SF_6 are able to clean the deposition chamber /14/. This is important for large systems that have to be cleaned regularly.

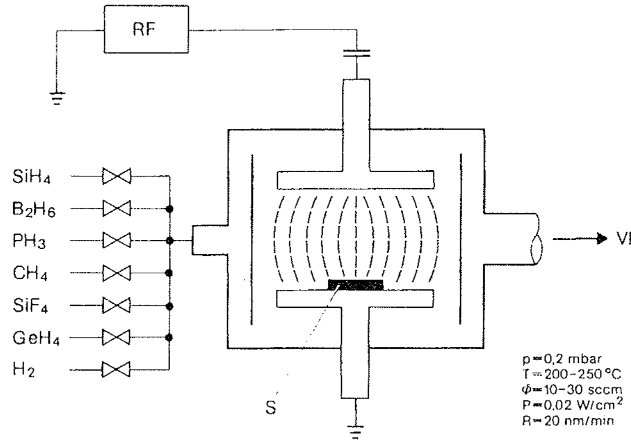

Fig. 4: Schematic view of an a-Si:H deposition system.

The pin solar cells produced in our research laboratory at Siemens AG were deposited in a two-chamber in-line system. It consists of a load-lock chamber and two process chambers. Chamber one is used for depositing the doped p- and n-layers, and chamber two is used for fabricating intrinsic material only. The chambers are separated by valves through which the substrate holder can be moved. This apparatus is able to deposit substrates having a size of up to 40x40 cm^2. We used this machine to develop 10x10cm^2 solar modules having the structure pin or nip. The deposition conditions are described elsewhere /15/.

2.3 Patterning

The scribing of the cut lines in the different layers was made by laser patterning. We used two types of laser. One IR laser (1042 nm) for patterning the front TCO1 layer and a frequency-doubled Nd:YLF laser (523 nm) for all other patterning steps. The setup for the laser scribing is shown in Fig. 5. The two lasers are positioned at pos1 and pos2. With two surface mirrors and one lens (f=100mm) the laser beam was focused and directed onto the sample, which was mounted on a moving table. The laser light always entered the sample through the glass substrate. For the P#1 the IR light was absorbed

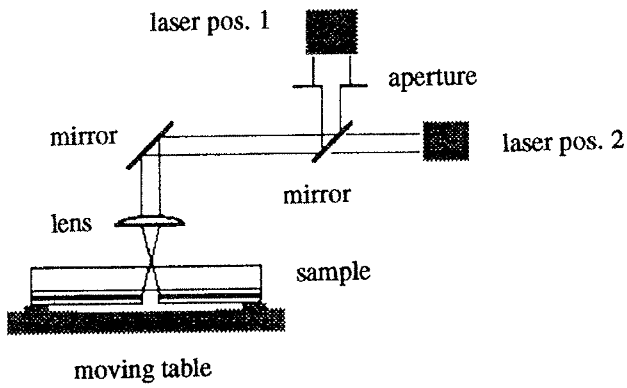

Fig.5: Schematic view of the setup for the laser patterning

in the TCO1 layer and removed the material. In all other patterning steps, the light is absorbed in the first a-Si:H layers (pin diode). The absorption leads to a considerable warming of the a-Si:H material and induces thermal expansion. As a consequence the material peels off. The effect is so pronounced that all layers deposited onto the first a-Si:H layers will be removed as well. Thus, the patterning steps P#4 to P#5 can be performed with the same technique. The details of the laser scribing are given in table 1.

Table 1: Parameter of the laser scribing

Parameter		P#1	P#4 to P#5
laser		Laser Appl. Model 9560 QT	ADLAS 321
wavelength	[nm]	1042	523
power	[mW]	800	8
pulse width	[ns]	80	15
frequency	[kHz]	4	1
focal diameter	[μm]	50	50
scribing velocity	[m/min]	6	2.9

The laser scribing through the substrate required a slightly different arrangement of the patterning lines. Fig. 6 shows a schematic cross-sectional view of the patterning, again together with the circuit diagram. The distance between the P#2 and P#3 line was increased and the P#4 and P#5 lines are located between them.

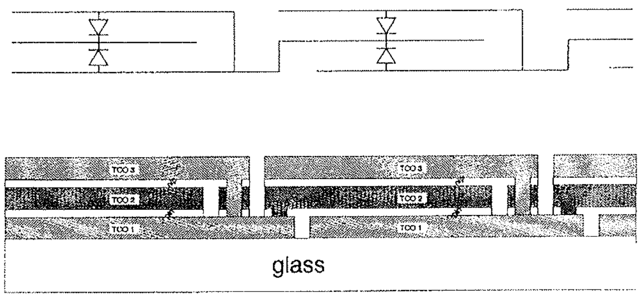

Fig. 6: Cross-sectional view of the patterning lines together with the circuit diagram

In order to control the laser scribing, REM pictures of the cross-sectional view were made. Fig. 7 shows the P#1 cut. One can clearly see that the patterning works very well. The front TCO1 is completely removed and the subsequently deposited layers show excellent covering of the P#1 line. The most critical patterning step is the P#3 line. This cut has to separate the center TCO2 layer. Furthermore, the following a-Si:H layers have to cover this cut such that no connection is made to the back TCO3 layer. Fig. 8 demonstrates that the demands are completely fullfilled. The center TCO2 layer is removed and the nip structures cover the scribed area completely.

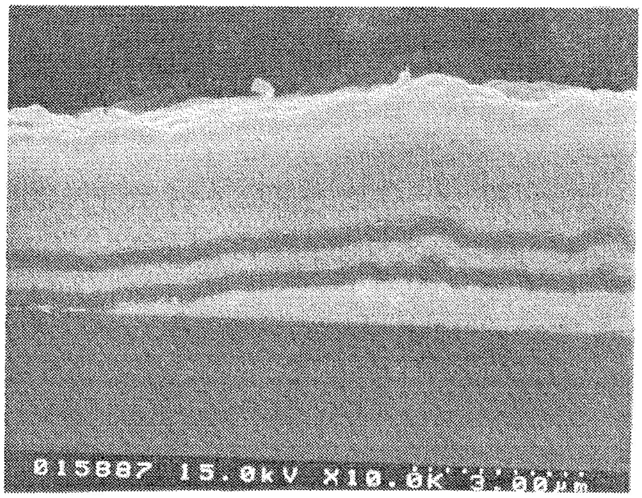

Fig. 7: REM picture of a cross-section of the P#1 line

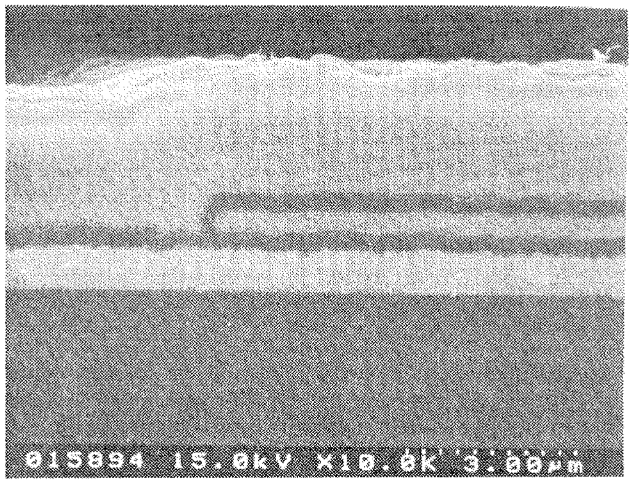

Fig. 8: REM picture of a cross-section of the P#3 line.

3 Results of cells and modules

3.1 PIN and NIP cells

The nip structure on glass/TCO substrates incoporates two difficulties: one is the inversed deposition sequence and the second is the illumination through the n-layer. In order to distinguish these two effects, we deposited pin as well as nip diodes with p-SiC layer having transparent electrodes on both sides. The cells were then investigated by dark and light characteristics and their spectral response for illumination through both sides.

Looking first to the pin device, we summarize the results in table 2. As one can clearly see, the n-side illumination reduces all parameters of the light characteristics. In fig.

9 the short-circuit spectral response of the pin cell is shown for both illumination directions. It demonstrates that the reduced short-circuit current for the n-side illumination is caused by a poorer blue response. The possible reasons for this are that the n-layer is too thick, that the surface recombination velocity at the n/i junction is very strong, and that the lifetime of holes is not sufficient to pass the i-layer completely. The fill factor and especially the open-circuit voltage are also lower for the n-side illumination mode. The low U_{OC} value indicates a strong surface recombination velocity at the n/i and also i/p junction.

Table 2: Measured results for a pin solar cell illuminated through the p- and n-side

Parameter		p-illum.	n-illum.
η	[%]	8.44	5.96
U_{OC}	[mV]	840	811
I_{SC}	[mA/cm^2]	14.17	11.71
FF	[%]	70.9	62.8
n		1.59	1.59
I_0	[A/cm^2]	$1.21*10^{-11}$	$1.21*10^{-11}$
Q(400nm)	[%]	62.8	36.6
Q(600nm)	[%]	87.3	81.4

Table 3: Measured results for a nip solar cell illuminated through the p- and n-side

Parameter		p-illum.	n-illum.
η	[%]	5.65	3.91
U_{OC}	[mV]	785	746
I_{SC}	[mA/cm^2]	11.72	9.31
FF	[%]	63.6	56.3
n		1.48	1.48
I_0	[A/cm^2]	$6.46*10^{-12}$	$6.46*10^{-12}$
Q(400nm)	[%]	51.1	19.5
Q(600nm)	[%]	76.7	72.0

The same qualitative results are obtained with the nip diode. Table 3 summarizes the parameters. As before, p-side illumination leads to higher efficiencies than n-side illumination. But the absolute values are lower compared to the pin device. In particular, the open-circuit voltage is very poor for both illumination modes. The same holds true for the spectral response, as can be seen by comparing fig. 10 with fig. 9. The deposition in the two chamber reactor makes it possible to achieve identical i-layer properties in both types of diodes. We thus concluded that the differences in the pin and nip diodes are primarily related to different properties of the p/i and i/n junctions.

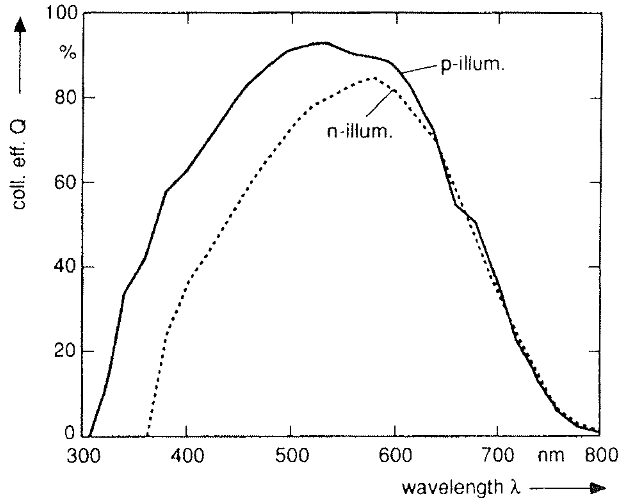

Fig. 9: External collection efficiency Q versus wavelength λ of a pin solar cell for illumina-tion through the p- and n-side

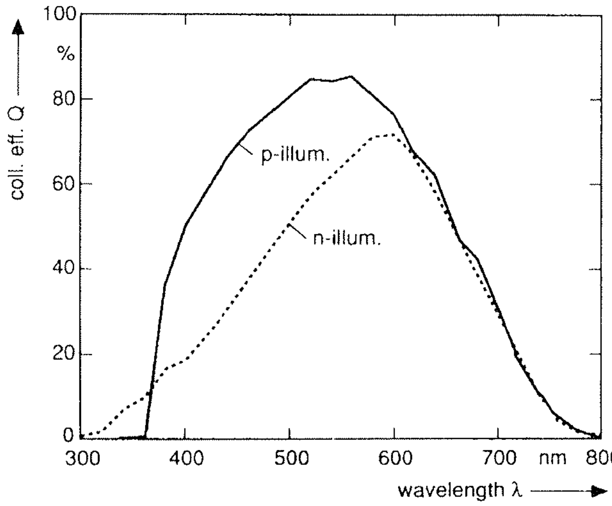

Fig. 10: External collection efficiency Q versus wavelength λ of a nip solar cell for illumination through the p- and n-side

3.2 Improvement of the nip solar cell

Several changes were made in order to overcome the above-mentioned problems. First of all, the n-layer thickness was reduced. This increased the external collection efficiency for blue light (λ = 400 nm) to values up to 58 % and the short-circuit current to up to 11.5 mA/cm^2. The AM1 efficiency was then more than 5 % being close to the efficiency value of the pin device illuminated through the n-side.

Table 4: Results of nip diodes having differently doped i-layers.

B_2H_6/SiH_4	[ppm]	0	1.25	2	2.5	3.25
η	[%]	2.50	5.37	4.99	5.51	5.13
U_{OC}	[mV]	735	843	869	854	930
I_{SC}	[mA/cm^2]	6.28	10.26	10.34	10.76	10.41
FF	[%]	54.1	62.1	55.6	59.9	53.0
n		1.38	1.67	1.82	1.86	1.84
I_0	[A/cm^2]	$2.14*10^{-12}$	$6.90*10^{-12}$	$1.54*10^{-11}$	$3.02*10^{-11}$	$1.67*10^{-11}$
Q(400nm)	[%]	9.3	33.8	41.1	37.7	41.8
Q(600nm)	[%]	49.5	62.4	59.7	68.6	61.1

In a second step, we tried to improve the hole properties by slightly doping the *intrinsic* layer. The doping concentration was varied between 0 and 3.25 ppm B_2H_6/SiH_4. The results are presented in table 4. With increasing doping, the open-circuit voltage increases from 735 mV (without doping) to 930 mV (3.25 ppm). However, too much doping causes the fill factor to decrease.

Finally, the incorporation of buffer layers at the n/i and i/p junctions was also tested. Different buffer layers were used at the two junctions. Between the n- and i-layers, a boron doped buffer layer was incorporated, whereas on the other side an intrinsic a-SiC layer was used. The results are summarized in table 5. One can clearly see that the buffer layer at the n/i junction slihgtly improves the open-circuit voltage up to a value of 791 mV. But the major effect is an improvement of the fill factor (up to 63%). The carbonized buffer layer at the i/p junction has the greatest influence on the open-circuit voltage. The incorporation of this layer increases U_{OC} to 844 mV, which is equivalent to the U_{OC} values of pin solar cells. The efficiency of this cell is comparable to the efficiency of pin cells under n-side illumination.

Table 5: Results of nip diodes with buffer layers.

buffer		no buffer	at n/i	at n/i and i/p
η	[%]	2.50	5.34	5.96
U_{OC}	[mV]	735	791	844
I_{SC}	[mA/cm^2]	6.28	10.72	11.23
FF	[%]	54.1	63.0	62.9
n		1.38	1.36	1.60
I_0	[A/cm^2]	$2.14*10^{-12}$	$2.53*10^{-11}$	$6.0*10^{-12}$
Q(400)	[%]	9.3	45.5	40.1
Q(600)	[%]	49.5	63.0	63.2

3.3 The pin/TCO/nip cell

The first pin/TCO/nip cells were produced using the standard deposition parameters for the pin and the improved process for nip cells. For this, we start with a relatively thick pin diode having a thickness of approximately 420 nm in order to overcome shunting problems. The thickness of the nip diode was about 500 nm. The TCO2 thickness was chosen to be as low as possible so that covering of the P#3 cut with the nip structure is effective. As a result, the thin TCO2 layer formed a relatively high series resistance and the inhomogeneity hindered the function of a complete module. In order to investigate individual pin/TCO/nip cells of a module, we made an additional patterning line as shown in fig. 11. This P#6 cut makes it possible to measure the pin, the nip and the pin/nip cells separately, because load 1 contacts the middle TCO layer. Thus, connecting the loads 1 and 3 measures the pin cell, loads 1 and 2 the nip cell, and loads 2 and 3 measures the complete pin/nip device.

Table 6: Results of the pin/TCO/nip cell and the individual pin and nip cells

cell	η	U_{OC}	I_{SC}	FF	U_{mpp}
	[%]	[mV]	[mA/cm^2]	[%]	[mV]
pin	7.00	870	11.91	67.6	667
nip	0.83	698	2.41	49.3	470
pin/nip	7.24	832	14.31	61.5	616

The results of the light characteristics are presented in table 6 and fig. 12 shows the characteristics. One can see that the overall efficiency is better than the efficiency of the pin cell itself. However, the nip cell contributes little to the total efficiency because the thickness of the pin cell was too great. In order to improve the nip cell's component and the stability of the total device, the thickness of the pin front cell must be reduced.

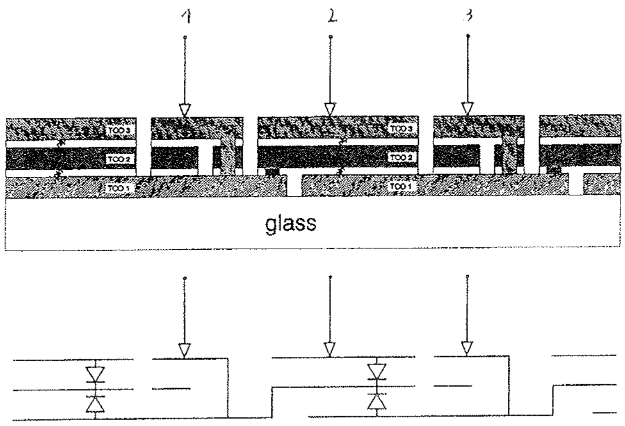

Fig. 11: Schematic view of the patterning lines for measuring the pin, nip, and pin/nip cells separately.

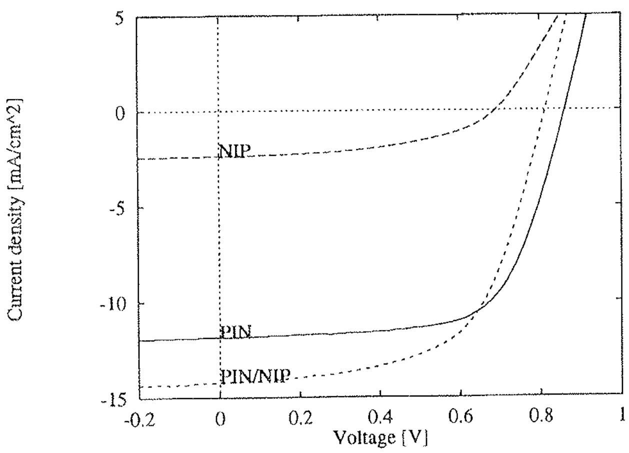

Fig. 12: Light characteristics of a pin, nip and pin/nip cell.

4 Conclusion

The parallel-connected stacked solar cell represents a design for a-Si:H solar cells which meets the demands for strong electric fields within the i-layer and sufficient light absorbtion without the disadvantage of the current matching requirement. It has been shown that the design could work. The patterning can be done with laser scribing and nip cells can be made as efficiently as pin devices illuminated through the n-layer. However, it seems that the structure could not be deposited on textured substrates, because of shunting problems with thin pin modules. The use of smooth substrates can overcome this problem. In any case, the parallel connection is a powerful alternative to the conventional series connected stack cells.

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Dr. W. Kusian,dipl. phys.
Siemens AG ZTE TEP 23
Otto Hahn Ring 6
D-81739 München, Germany
Tel.: +49 89 636 44 682
Fax: +49 89 636 49 164
Dr. J. Furlan, dipl.ing.
University of Ljubljana,
Faculty of Elect. and Comp. Eng.,
61000 Ljubljana, Tržaška 25, Slovenia
Dr. G. Conte, dipl.ing.
ENEA, CRIF,
I-80055 Portici, Italia

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THERMAL AND ELECTRICAL OPERATION AND MALFUNCTION OF ELECTRONICS DETECTED AND IMAGED BY MEANS OF LOW COST LIQUID CRYSTAL SENSING

Nihal Sinnadurai
TWI, Cambridge, England

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Key words: microelectronic components, malfunction detection, electronic circuits, electrical operation, thermal imaging, thermal loses, thermal properties, thermal images, nematic LC, nematic liquid crystals, malfunction location, measuring techniques, fine resolution, high sensitivity, resolution <1μm, polarized light, hot spots, precise temperature measurement, faulty operation tracing, hot spot location, thermal profiling, ULSI, Ultra Large Scale Integration, hybrid circuits, circuits boards

Abstract: Complex microelectronics devices of today have fine geometries, giving rise to the challenge of requiring equally fine resolution and high sensitivity measurement techniques in order to characterise their operation and to locate and help diagnose malfunction. A dual technique ideally suited to such measurement combines the high sensitivity field response and the precise isotropic transition temperature of nematic liquid crystals as invented by the author more than two decades ago. Nematic liquid crystals respond to changes in electric fields by causing brightness contrasts with a line definition of 1 micron, when viewed with polarised light. When heated, nematogens also undergo a transition from optical birefringence to isotropy at a temperature reproducible to 0.2°C also with a spatial resolution of 1 micron. A number of original analyses are illustrated, such as the failure site of a relay driver integrated circuit diagnosed by locating the consistent occurrence of a hot spot on just one branch of the dual emitter output transistor. The failure of multiple emitter power transistors was traced to the faulty operation of one of the branches of the transistor. Precise temperature measurement and characterisation of thin-film nichrome resistors and location of hot spots due to laser trimming of thick-film resistors is readily accomplished. Thus, the high-resolution capability of the liquid crystal technique for functional observation and thermal profiling has benefited the full raft of microelectronics components ranging from ULSI through to hybrid circuits and circuit boards.

Uporaba cenenih tekočih kristalov za opazovanje in odkrivanje napak delovanja elektronskih komponent in vezij

Ključne besede: deli sestavni mikroelektronski, detekcija delovanja slabega, vezja elektronska, delovanje električno, upodabljanje termično, izgube termične, lastnosti termične, slike termične, LC kristali tekoči nematični, lociranje delovanja slabega, tehnike merilne, ločljivost fina, občutljivost velika, ločljivost < 1μm, svetloba polarizirana, mesta vroča, merjenje temperature precizno, sledenje delovanja napačnega, lociranje mest vročih, profiliranje termično, ULSI integracija ultra visoke stopnje, vezja hibridna, vezja tiskana

Povzetek: Današnje kompleksne mikroelektronske komponente odlikujejo izredno majhne geometrijske strukture, ki na drugi strani zahtevajo enako fine merilne tehnike z visoko ločljivostjo in občutljivostjo, s katerimi vrednotimo delovanje teh komponent, oz. odkrivamo in diagnosticiramo njihove odpovedi. Tehnika, ki jo je izumil sam avtor pred dvema desetletjema, in je idealna za izvajanje opisanih meritev, združuje visoko občutljivost odziva in natančno temperaturo izotropnega prehoda nematičnih tekočih kristalov. Nematični tekoči kristali reagirajo na spremembo v jakosti električnega polja s spremembo v svetlobnem kontrastu s prostorsko ločljivostjo 1 μm, če jih opazujemo s polarizirano svetlobo. Ravno tako nematogeni, če jih grejemo, spremenijo stanje iz optične dvolomnosti v izotropno pri temperaturi, ki je ponovljiva do 0.2°C in prostorski ločljivosti do 1μm. V prispevku podajamo vrsto originalnih analiz s to metodo, kot npr. odpoved integriranega krmilnika relejev, kjer smo kot vzrok odpovedi odkrili vroče mesto le na enem kraku izhodnega tranzistorja z dvojnim emiterjem. Nadalje smo podobno ugotovili, da leži vzrok odpovedi močnostnega tranzistorja z večimi emiterji v odpovedi le ene njegove veje. Sledijo opisi natančnih meritev temperature in karakterizacija tankoplastnih NiCr uporov ter odkritja vročih mest zaradi laserskega doravnavanja debeloplastnih uporov. Tehnika uporabe tekočih kristalov je izredno občutljiva, cenena in primerna za opazovanje delovanja in odkrivanje napak raznovrstnih elektronskih komponent od VLSI preko hibridnih do tiskanih vezij.

1. INTRODUCTION

The electrical operation and temperature distributions in microelectronics components are clear indicators of their performance and reliability. However, such detail within a microcircuit is rarely uniform, instead being distributed according to the microscopic dimensions of the fields subtended at the surface and the power dissipation and heat conduction paths. Therefore techniques have been sought to observe electrical operation and to measure temperatures and thermal profiles on a microscopic scale.

Amongst the more popular techniques for observing microcircuit operation is the use of the scanning electron microscope (SEM) with the electron beam as the electrical probe. This provides very versatile capability and also enables prototype testing of integrated circuits (ICs) /1/. However, it does require major investment in such equipment and does require the component to be operated in vacuum and also subjects the component to high energy electrons which can alter the local behaviour of the circuit. Therefore a complementary technique which could be used in conjunction with existing laboratory microscopes and did not involve evacuation or high energy bombardment was desirable.

One of the early innovations for high resolution temperature measurement was the infrared micro-radiometer, which measures the radiation emitted from microscopic areas /2/. In principle the technique has a spatial resolution down to 8 μm and a temperature sensitivity of 0.5°C. In practice the technique rarely performs to its limits and suffers the drawback of needing considerable calibration and computation to translate the measured radiation into temperature.

In order to meet both objectives, Liquid crystals were examined following reports of the use of nematogens for electrically controlled imaging and cholesterogens to measure surface temperatures. Cholesterogens /3,4/ were soon abandoned because the technique was found to have a poor spatial resolution (>20 μm) and required the application of a non-reflecting coating which impaired the microscopic temperature profiles. Instead, an alternative property of nematic liquid crystals (nematogens) was uncovered and has been successfully exploited into a technique /5/ for the measurement of surface temperatures with a spatial resolution of better than 1 μm and sensitivity of better than 0.2°C. The TEMPCOL© (TEMPerature COntrast by Liquid-crystals) technique is briefly described in this paper which is devoted more to illustrating its application to a range of microelectronics components. During this work, it was also discovered that the identical experimental set-up was effective also in revealing the electrical operation at the surface of the microcircuit, which has therefore been developed into the VOCOL© (VOltage COntrast by Liquid-crystals) technique /6,7/, also with a spatial resolution of 1 μm.

2. THE TECHNIQUES

In its liquid state, a nematogen is birefringent at temperatures up to a well defined critical temperature *(Ti)* called its "Isotropic Point," above which it is isotropic. Thus, plane-polarised light is doubly refracted when transmitted through a nematogen below *Ti*, but is unaltered by a nematogen above *Ti*. In the application of the techniques to microcircuits, a metallurgical microscope is employed in the experimental arrangement shown in Figure 1. A planar component coated with a thin layer (~5 μm) of liquid crystal is illuminated with vertically-incident plane-polarised light and viewed through a "crossed" analyser. In the VOCOL© technique dynamic electrical operation of the circuit is then observable as locally varying microscopic regions of brightness. The

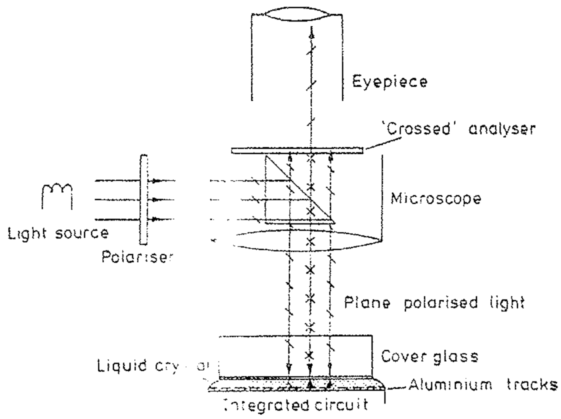

Fig. 1 : Schematic of experimental arrangement for temperature and voltage contrast

sequence of photomicrographs Figs 2a to 2d illustrate the increasing brightness associated with the positive electrodes. Such contrasts are also observable on real complex ICs, again the brightness being associated with the positive electrode according to the analysis in Reference 7. However, because the observations are of dynamic changes, photomicrographs are not convincing representations of the observed phenomena, and instead the observations have to be made in real time on a video monitor /6/.The technique has been copied and successfully exploited by many other researchers, (e.g. /8/).

In the TEMPCOL© technique, for temperature measurement and profiling, regions of the component at temperatures below Ti remain visible because one of the components of the doubly-refracted light is transmitted through the analyser; while regions above Ti appear dark because light is absorbed by the analyser. The boundaries between dark and light regions are then isotherms precisely at Ti, which has been found to be reproducible to within 0.2°C, whilst the spatial resolution has been determined to be better than 1 μm /9/. The high resolution capability is illustrated by the precise boundaries of the 5 μm diameter hot spot example (Figure 3), produced by dissipation in a thin-film nichrome resistor. In order to measure temperatures below Ti, for a particular dissipation, the component ambient temperature (Ta) is increased until light is extinguished in the area of interest. Then Ti - Ta is the temperature rise for that dissipation. The distribution of temperatures between Ti and Ta is obtained by raising Ta by small increments to produce a succession of isotherm boundaries corresponding to each Ti - Ta. The temperature distribution in the resistor from the earlier example was obtained in this way (Figure 4). Figure 4 also illustrates the manner in which the areas bounded by the isotherms widen as Ta is increased by 1°C and 2°C, and the corresponding effects are illustrated in Figures 5 and 6. Temperatures above the isotropic point of a particular nematogen may be measured either by cooling the ambient or by using nematogens with a higher Ti. Nematogens have been identified with isotropic points in the range 25°C to 300°C.

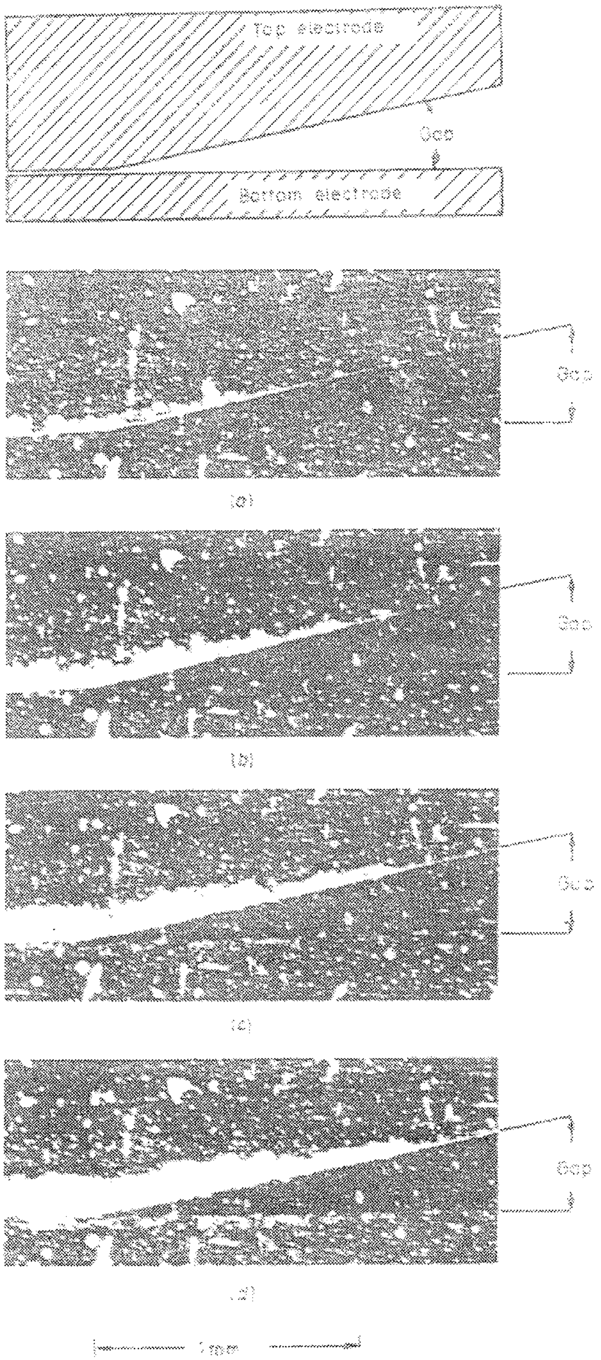

Fig. 2: Brightness Contrasts in a Test Pattern for Positive Potentials Applied to the Top Electrode: (a) 7V, (b) 8V, (c) 9V, (d) 10V

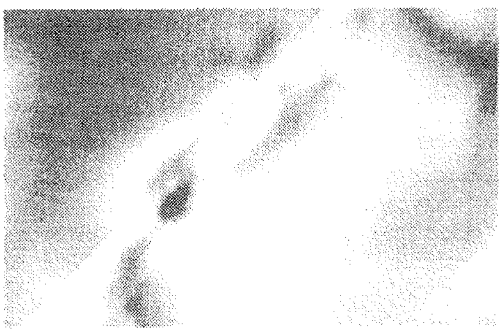

Fig. 3. Hot Spot on Nichrome Resistor (10µm wide)

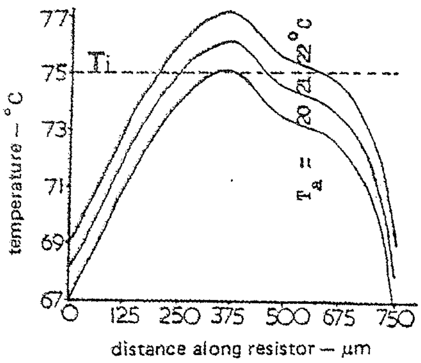

Fig. 4: Temperature Distribution Along Resistor of Figure 3 for Successively Increased Ambient Temperatures

Fig. 5: Isothermal Boundaries of Figure 3 Extended by Raising Ambient by 1°C

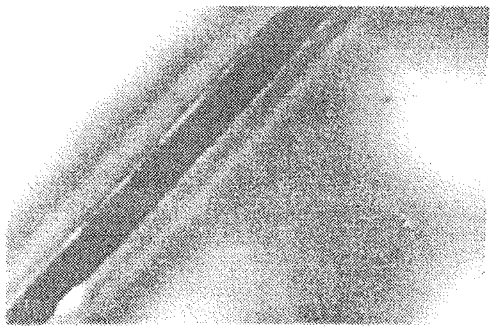

Fig. 6: Isothermal Boundaries of Figure 3 Extended by Raising Ambient by 2°C

3. APPLICATIONS

3.1. Monolithic Semiconductor Components

The technique is especially suited to monolithic microcircuits and transistors, where the high resolution is exploited. The following examples have been chosen to illustrate the obvious benefits of the immediate visual information obtained.

The first example shows the operation of an interdigitated transistor, clearly revealing, in Figure 7, the satisfactorily symmetrical distribution of temperature about the centre of one segment. The outer elements just reaching Ti are clearly distinguishable. Figure 8 shows that one entire segment of the transistor was malfunctioning requiring excessive dissipation in the other three segments to get the fourth up to operating temperatures.

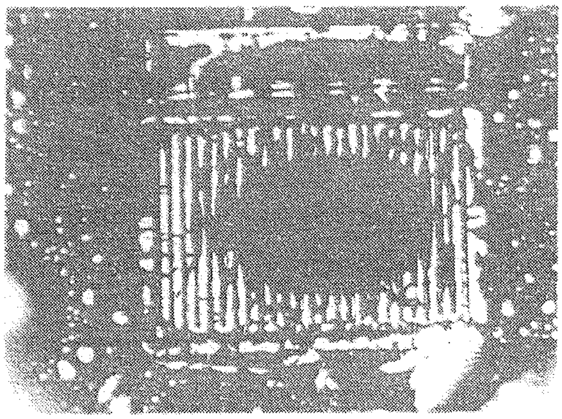

Fig. 7: Temperature of One Branch of an Interdigitated Power Transistor

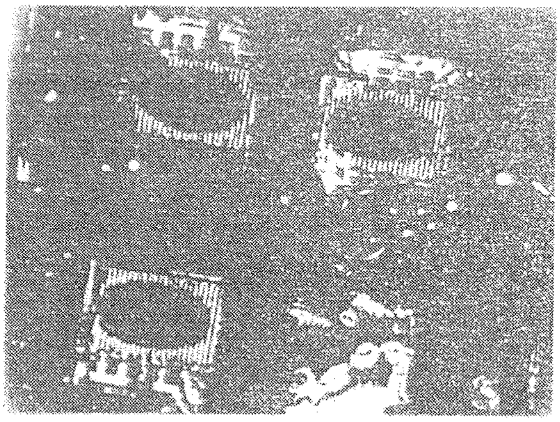

Fig. 8: Malfunction Revealed in One Segment of the Power Transistor

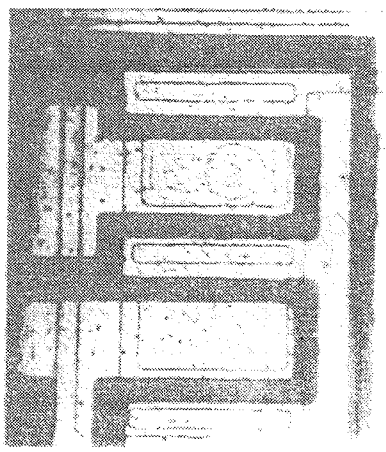

Fig. 9: Photomicrograph of Output Transistor of Relay-Driver IC

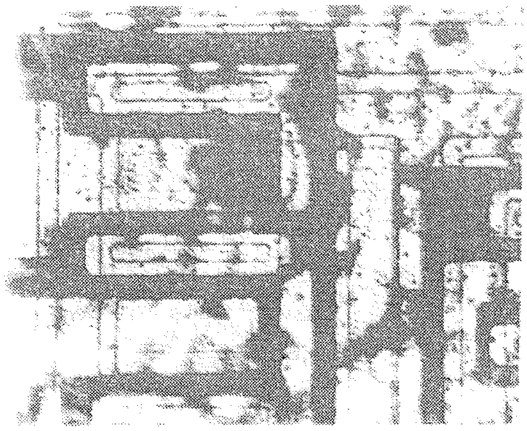

Fig. 10: Hot Spot at One of the Dual Elements of the Output Transistor of Figure 9.

A second example is of the diagnosis of faulty relay driver transistors (Figure 9) of a type that frequently failed under transient surge conditions. Figure 10 shows the hotter operation of one of the two elements of the emitter due to persistent unbalanced operation which was found to contribute to eventual failure by thermal runaway.

3.2. Thick-Film Resistors

In support of current reliability studies of other microelectronics components, attention has also been given to thick-film resistors whose large planar areas are ideally suited to examination by the technique. The examples presented here are for resistors in arrays in various dual-in-line packages, which were used as test vehicles in the studies. In order to relate thermal ageing during stress tests to the temperatures generated within the resistors, it was necessary to refer to a common parameter such as thermal resistance (R_θ) (defined as the temperature rise per unit power dissipated). Because the measurements showed that the temperature distributions were distinctly non-uniform, and ageing is fastest in the hottest parts, thermal resistances were calculated for the hottest spots on the resistors.

Single resistors gave the most straightforward results because the hot spots occurred at the known sites of maximum dissipation. Illustrated in Figure 11 is a typical observation, that hot spots always originate at the ends of laser "plunge" cuts, the hotter spots occurring at the longer cuts. The values of hot spot thermal resistance for resistors of similar geometry were found to be confined to a small range regardless of their electrical resistivity. Typical thermal resistances were 100°C/W to 125°C/W for 2 mm x 2.2 mm resistors and 55°C/W to 65°C/W for 2 mm x 4.5 mm resistors in the range 50 ohm to 50 k.ohm. Generally, resistors located in the middle of substrates had a lower thermal resistance because of the substantial heat sink surrounding them; but significant variations of R_θ also arose because of differences in the extents of laser cuts in nominally similar resistors.

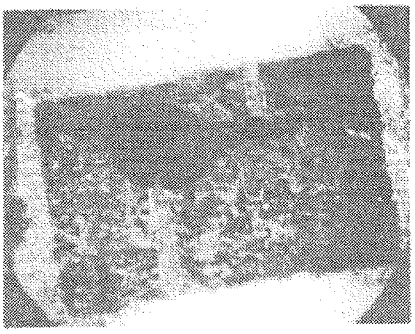

Fig. 11: Close-up of Hot Spots at the Ends of Laser Cuts of Thick Film Resistor

The technique has also been used to aid the diagnosis of faults in resistors. Low value resistors, which dramatically increased in value after exposure to voltage surges, were found to have developed hot spots at locations remote from constrictions due to trimming (Figure 12), implying that new constrictions had developed in the structures. The occurrence of cracks in the resistors, terminating at the location of the hot spots was confirmed by laboriously probing the resistors to produce equipotential contours. The contours in Figure 13 correspond to the resistor in Figure 12 (the crack looks like a laser cut).

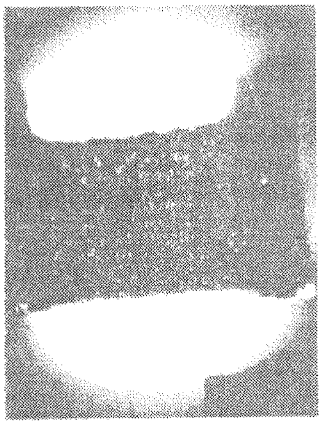

Fig. 12: Hot Spot in a Damaged Resistor

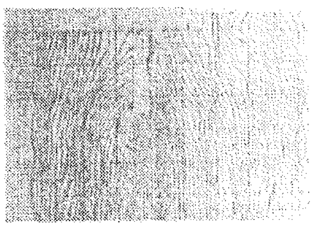

Fig. 13: Equipotential Distribution Over the Damaged Resistor

4. DISCUSSION AND CONCLUSIONS

The foregoing illustrations show that the liquid crystal technique is simple yet provides high spatial resolution, giving it distinct advantages over even the more advanced of the alternative methods of temperature measurement of microcircuits and providing a complementary alternative to the use of the SEM for observing circuit electrical function and malfunction. In principle, the method may be applied to any planar horizontal surface and has a ceiling of about 300°C. The ready application of the technique to both active and passive microelectronics components, and the obvious benefits of simultaneous visual examination of entire components have been illustrated by the examples presented.

Fine geometry ICs and also thick-film resistors have been shown to be eminently suitable components for examination by the technique, in support of characterisation, design verification versus simulation /10/ (a future paper) and reliability evaluation.

The observations of thick film resistors are consistent with heat conduction between the resistors and substrates. This was particularly notable when significantly non-uniform dissipation within a resistor array still produced a fairly uniform temperature distribution. It was only in single resistors that local dissipation played a significant part - the variation in thermal resistance due to different extents of trimming giving warning that families of resistors could age at different rates because of trimming cut variations within the design rules of some manufacturers.

The applications of the technique extend beyond the supportive role to reliability evaluation. For instance, it is clear that measurements of thermal resistance and temperature distributions can be used to estimate resistance changes associated with the temperature coefficient of resistance, and in calculating any derating adjustments that are necessary. Thus, the high-resolution capability of the liquid crystal techniques for functional observation and thermal profiling has benefited the full raft of microelectronics components ranging from ULSI through to hybrid circuits and circuit boards.

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We are pleased to acknowledge the support of Temptronic Corporation in providing their ThermoSocket which has been used for precise device temperature control during this work.

We are pleased to note that Temptronic has adopted the TEMPCOL© liquid crystal technique in their product range

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Prof. Dr. Nihal Sinnadurai
Principal Consultant in Electronics Technology, Reliability and Business Analysis
TWI, Abington Hall, Abington, CB1 6AL, England
Tel.: +44 1223 891162
Fax: +44 1223 892588

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HIPOT-HYBRID, d.o.o.

COMPANY PROFILE

HIPOT HYBRID, Production of hybrid circuits and sensors, d.o.o., Šentjernej (formerly a part of the Iskra Company) has 20 years experience in the production of custom thick film hybrids and 8 years experience in the production of sensors for medical applications.

The company is based in Šentjernej where the manufacturing plant together with the headquarters and technical service division is located, and employs some 120 workers on a floor area of 950 m^2. The company has a turnover of some 5.5 million USD (8 million DEM) in 1994 and approximately 7.5% of total income is invested in R&D. HIPOT HYBRID is an export oriented company since more than 70% of its production volume is sold on world markets. The major part of the export production line is devoted to sensors for invasive blood measurements (about 1 million pcs in year 1994).

Constant monitoring of international and domestic customer requirements and demands, as well as the introduction of state-of-the-art knowledge and technology into the manufacturing process make it possible for the company to be present effectively on domestic and world markets.

In the field of research and development, as well as in system upgrading the company works in close relationship with scientific institutions and technical associations both in Slovenia and worldwide. Such institutions include:

- Jožef Stefan Institute - Ljubljana,
- Iskra IEZE RR Institute - Ljubljana,
- Faculty of Electrical and Computer Engineering - University of Ljubljana,
- Faculty of Electrical Engineering, Computer Science and Information Technology - University of Maribor,
- Ecomedis - Altenberge,
- etc.

HIPOT HYBRID has implemented and now maintains a quality control system which fulfills the requirements of ISO 9001 (Reg. No 14 589-01). The quality audit was performed in 1993 by DQS - the German Association for the Certification of Quality Systems.

HIPOT HYBRID is one of daughter companies of HIPOT. Other companies, which are also located in Šentjernej, produce LCD, polymer board panels and potentiometers. A tooling workshop is also included. The wide range of available technologies and of know-how at the same site gives the possibility to create complete solutions to meeting customer needs.

MILESTONES IN HIPOT-HYBRID

- 1969 - education
- 1973 - first products (passive thick film circuits, cermet potentiometers)
- 1975 - hybrid thick film circuits for telecommunication
- 1977 - SMD
- 1980 - multilayer hybrids, chip and wire hybrids, hermetic incapsulation
- 1982 - hybrid circuits for mobile radio equipment
- 1986 - pressure sensors
- 1993 - ISO 9001 (DQS)

PRODUCTION PROGRAMME

HIPOT-HYBRID has the following production programme:

- thick film resistor networks
- SMT thick film hybrid circuits
- chip and wire thick film hybrid circuits
- pressure sensors and transducers

RESEARCH AND DEVELOPMENT

The R&D Department of company in close relationship with scientific institutions and technical associations work on following R&D activities:

- studying new trends in thick film technology
- incorporating new technologies and materials
- electronic design
- thick film hybrid circuit design
- sensors (pressure, humidity, temperature, load cell)
- transfer to production
- quality control of thick film hybrid circuit production
- educating and training specialists for hybrid circuit production

- publications (ISHM, Eurosensor, MIEL-SD, Hybrid Circuits, Microelectronics Journal, Elektrotehniški vestnik, ...)
- every year one or two R&D projects are supported by the Ministry of Science and Technology of the Republic of Slovenia

THICK FILM HYBRID CIRCUITS

A production facility with a controlled environment, and modern equipment for CAD, printing and firing, laser trimming, automatic wire bonding, pick and place, packaging and computer controlled testing enables the following technological processes to be carried out:

- Double sided multilayer construction
- Fine line conductors
- Through hole connections
- Mixed assembly of soldering and chip-and wire techniques
- Double sided surface mounted component attachment
- Active trimming
- Hermetic and nonhermetic encapsulation techniques

The products range from precision networks with absolute and relative tolerances down to ±0.1%, to complex hybrids and sensor assemblies functionally trimmed to meet the most exacting specifications. The majority of product are for applications in telecommunications, medical electronics, industrial control, computers, military electronics, and consumer fields.

HIPOT HYBRID mostly develops the technical design of hybrid circuits and takes responsibility for the details involved in testing and producing them. Delivery time is from 1 to 6 months, depending on the project. For successful start the customer is requested to provide the following information:

- dimensions (LxWxT)
- electronic circuit (if possible) or desired function
- component specifications (if available), or approved source
- electrical performance
- environmental requirements
- package type
- pin assignments
- other.

SENSORS AND TRANSDUCERS

Industrial pressure sensors and transducers

- Pressure range: from 0-5 mBar to 1-15 Bar
- Pressure measurement type: absolute, differential, gauge
- Fully temperature compensated
- Accuracy: up to 0.5% FS
- Output: voltage, current, switch, digital
- Standard or custom designed thermoplastic housing

Customized pressure sensors and products

- Medical applications
- Air flow control
- Analogue, digital and micro controller sensor modules

Force and weight sensors

- Strain gauge on ceramic substrate
- Force range: 1 N - 1000 N
- Low cost

PTC and NTC thick film resistors

- TCR: up to $+3500\times10^{-6}$/K, -10000×10^{-6}/K
- Desire resistivity value
- Integrated in hybrid circuits

Proximity switch

- Custom design
- Miniaturized thick film technology

SOME SIGNIFICANT EQUIPMENT

- Design: 2 HP CAD
- Substrate cutting: 2 CO_2 lasers (up to 4"x4")
- Printing: .5 DEK, 5 Aurel, 1 Presco
- Firing: 4 furnaces
- Trimming: 2 CLS33, 1 CLS37
- Assembly:
  - 2 SMD pick and place (2x2000/h)
  - 3 terminal insertion
  - 3 reflow and 1 infrared furnaces for soldering
  - 1 K&S automatic thermosonic gold ball bonder
  - 3 semiautomatic bonders
  - 1 ultrasonic aluminium wedge bonder
  - 1 Al bonde (300 mm)
- Testing: automatic test equipment (HP)
- The infrastructure of research partner enables a basic research of materials

TECHNICAL SPECIFICATIONS OF THICK FILM HYBRIDS

Substrates:

96 - 99.5% Al_2O_3 ceramic
Maximum size 102 x 102 mm^2
Thickness 0.4 - 2 mm

Conductors:

Pd/Ag, Au, Ag

Resistors:

Value range	1 Ω to 300 Ω
Tolerance	absolute down to 0.1%, matching down to 0.1%
TCR	standard $100x10^{-6}$/K, available $50x10^{-6}$/K
TCR tracking	down to $10x10^{-6}$/K

Add-on components:

Resistors	chip and MELF styles
Capacitors	ceramic, tantalum chips
Inductors	chip inductors and other miniature coils
Semiconductors	die and/or SMD (SO, LCC, ...)

Packaging:

Styles	SIL, DIL, on customer request
Protection	overglaze, printed organic, conformal coat hermetically sealed metal
Terminals	2.54 mm or 1.27 mm pitch

THE ADVANTAGES OF THICK FILM HYBRID CIRCUITS

- **Reduced size and weight**

Thick film circuits can be up to 5 times smaller than traditional PCB, whilst contributing to improved circuit performance.

- **Performance**

Combining complementary technologies such as analogue and digital circuits can give a performance often unattainable in a monolithic solution.Standardization of commonly used circuits.

- **Temperature tracking**

Because the resistors are on a common ceramic substrate their temperature coefficient and ageing characteristics track. This significantly improves analogue performance over many other technologies.

- **Heat dissipation**

The high thermal conductivity of the ceramic substrate ensures good heat dissipation.

- **Reliability**

A number of components are laid down directly onto the substrate. The reduction of the number of soldered connections undoubtedly improves circuit reliability considerably. Resistors and conductive paths are laid down simultaneously by repetitive processes, which results in uniform behaviour with respect to both time and temperature.

- **Functional trimming**

Trimming the circuit under dynamic conditions enables each hybrid to function as a complete finished component without the need for external adjustment.

- **Testing**

All circuits are fully tested to the customer's own specification.

- **Cost**

A direct comparison between the cost of a thick film module and an equivalent PCB circuit may, or may not, favour the thick film approach. For a correct economic evaluation, the reduction in the number of components to be specified, bought, quality controlled and stacked must also be considered.

- **Economic for large and small quantities**

A short design period, rapid prototyping, and acceptable development and production costs can be offered with hybrid technology with quantities as low as a few hundred pieces.

COMPANY ADDRESS

HIPOT HYBRID d.o.o.
Production of hybrid circuits and sensors,
Šentjernej, Trubarjeva 7,
68310 Šentjernej,
Slovenia

Tel.: +386 68 81220
Fax.: +386 68 81370

Director of the Company: Jože Colarič
Head of the Commercial Department: Jože Luzar
Head of the R&D Department: Darko Pavlin
Head of the Technological Department: Lojze Simončič
Head of the Production: Silvo Vinšek
Sensors Product Manager: Stojan Šoba

JOŽEF STEFAN INSTITUTE
Thin film and surfaces department

A) The department for thin films and surfaces at the Jožef Stefan Institute in Ljubljana is doing research mainly in the following four areas:

1. **Ion and plasma interactions with solid surfaces,** including the study of interactions during ion etching and thermal annealing

2. Synthesis of new **wear, oxidation and corrosion resistant coatings**

3. A study of **interface interaction** in bi- and multilayer structure during thermal annealing and preparation of standards in the form of multilayer structure for depth profile analysis

4. Development and application of **new technologies in the field of metallurgical coatings**

B) A part of our department is also **Hard Coatings Centre** (Dom'ale), established in 1985 to develop new metallurgical coatings for industrial applications and to serve industrial needs. In the last ten years, more than 500 000 pieces of tools and machine parts for machine, electrical, wood and other industries were protected by TiN and CrN hard, corrosion and oxidation resistant coatings.

C) In the last fifteen years we investigated and developed various types of thin films, coatings and multilayer structures, which can be divided into two groups:

a) Hard protective coatings

- binary nitrides and carbides of the transition metals: TiN, ZrN, CrN, WC
- ternary nitride: TiZrN, CrTiN
- TiN/CrN, ZrN/CrN
- other protective coatings: NiCrTi
- standard reference materials in form of multilayer coatings (Ti-N/Ti/TiN, Zr-N/Zr/ZrN, Cr-N/Cr/CrN)

b) Thin films for electronics and microelectronics

- indium tin oxide transparent conductive films (ITO)
- NiCr, NiCrAl and Ta_2N thin film resistors
- metalization structure for VLSI circuit: <Si>-$TiSi_2$/TiN/Al
- transition metal silicides and aluminides (Ti-Si, Zr-Si, Co-Si, Ni-Si, Cr-Si, Ni-Al, Fe-Al....)
- standard reference materials in the form of multilayer structures: Ni/Cr, Ni/Cr/Cr_2O_3, NiO/Cr_2O_3, Cr-O/Cr/Cr_2O_3, Ni-O/Ni/NiO, Ti-O/Ti/TiO_2, Zr-O/Zr/ZrO_2)
- YBaCuO high temperature superconducting films and superconducting multilayer systems: YBaCuO/NiO, YBaCuO/ZrO_2
- $LiTaO_3$ ferroelectric thin films

D) For preparation we use various PVD techniques:

(a) DC and RF sputter deposition
- plasma beam sputtering apparatus SPUTRON (Balzers),
- 2 cylindrical magnetrons

(b) Ion plating technique
- BAI 730 (Balzers)
- BAI 730M (Balzers)

(c) Flash evaporation
- BAK 600 (Balzers)

E) For complete characterization (composition, structure, microstructure, ...) of thin films and surfaces, we use the following experimental techniques:

(a) continuous in situ electrical resistivity measurements
(b) X-ray diffraction (XRD)
(c) Rutherford backscattering spectrometry (RBS)
(d) Auger electron spectroscopy (AES)
(e) differential scanning calorimetry (DSC)
(f) cross-sectional transmission electron microscopy (XTEM)
(g) X-ray photoelectron spectroscopy (XPS)
(h) Raman spectroscopy
(i) Scanning electron microscopy (SEM) and energy disspersive spectrometry (EDS)
(j) Atomic force microscopy (AFM)
(k) Glow discharge optical spectrometry (GDOS)

1. BASIC RESEARCH

A brief overview of our investigations in the area of a basic research:

- In the area of ***interactions of ions and plasma with solid surface***s the main activities are:
  (a) A study of mechanisms of **reactive sputtering**
  (b) **Sputtering rate measurements, the observation of surface damage, topographical changes and ion erosion effects** during high ion dose bombardment of materials, used for the first wall in fusion reactors.
  (c) A study of **plasma treatment** of substrate surfaces, **plasma cleaning** of metals, alloys and hard metals at temperatures bellow 250°C. For this investigation we are using Balzers PPM421 plasma process monitor to measure the mass and energy distribution of plasma species during three processes: (a) substrate heating by electrons from low voltage plasma arc, (b) substrate cleaning by argon ion etching, and (c) deposition of hard coatings, using ion plating process.

- Research on ***wear, corrosion and oxidation resistant coatings*** includes:
  (a) determination of **basic physical properties** of hard coatings (microhardness, adhesion, frictional coeficient, lattice parameters, electrical and optical properties),
  (b) a study of **corrosion and passivation behaviour** of anodically and thermally oxidized hard coatings (by electrochemical methods - potentiodynamic and potentiostatic polarization - in combination with surface analytical techniques to identify the corrosion products),
  (c) a systematic investigation of **oxidation mechanisms** of various binary and ternary transition metal nitrides in form of the single layer and multilayer, (we measure the activation energy for oxidation, the main migrating elements)
  (d) a development of the **coating to protect tools** which operate at high working temperatures (600-700°C) and tool steels with low tempering temperature (deep drawing-cold forming and Al-alloy die casting tools).

- a study of ***interface interactions*** during annealing of various bilayers and multilayers; using different experimental techniques we investigate:
  (a) **the phase formation sequence**,

(b) **the kinetics of phase formation,**

(c) **the main migrating elements** of the reactions.

Various Me/Si and Me/Me bi- and multilayer structures were investigated in last years: Ni/Si, Al/Si, Cr/Si, Co/Si, W/Si, Mo/Si, Nb/Si, Ni/Cr, Ni/Cr/Cr_2O_3, NiO/Cr_2O_3, Fe/Al, Ni/Al.

- In cooperation with the research groups of Institute for Electronics and Vacuum Technique (Ljubljana) and Max-Planck Institut für Metallforschung (Stuttgart, Germany) **the influence of diffusion, segregation, reaction at the interface and sputter parameters on depth resolution** of Auger, XPS and secondary ion mass depth profile techniques were studied. Three years ago interlaboratory comparison (round robin, experiment) of depth profiling results for Ni/Cr multilayer using AES, XPS and SIMS was organized between four laboratories.

- In cooperation with research groups of Kernforschungszentrum Karlsruhe (Germany) and Institute for Electronics and Vacuum Technique (Ljubljana) **the interfacial diffusion effects and the changes in elemental composition of YBaCuO/NiO and YBaCuO/ZrO_2 bilayer and multilayer** and their metallic (Cu,Ag and Au) overlayered componets were investigated during thermal annealing. These systems were investigated with a view to their possible technological use in microelectronic devices, detectors, etc.

2. APPLIED RESEARCH

The most important results of our applied reseach are:

- Tools and machine parts have been coated for more than 300 manufacturers in Slovenia and abroad. Systematic analyses of performance tests in industry have been performed. Using tools, protected with our TiN (JOSTiN® technology) and CrN coatings in the Slovenian machine, electrical and wood industry, production experts improved productivity and the quality of products.
- The first standard reference material - SRM (NBS N°2135) for surface analysis in form of Ni-Cr multilayer has been developed and manufactured for NIST, Washington.
- Standard reference material for depth profile analysis in the form of Cr/Ni/Cr_2O_3/Cr/Ni multilayer structure was also made on the request of Bodenseewerk Perkin-Elmer GmbH (Munich).
- Development and characterization of SRM for hard coatings by AES, XTEM and RBS techniques.

3. GROUP MEMBERS

Members of the research group of our department are:

1. Prof. dr. Boris Navinšek, Head of the Thin Film and Surfaces Department and Center of Hard Coatings
2. Dr. Peter Panjan, researcher
3. Mag. Andrej Cvelbar, postgraduate
4. Dr. Ingrid Milošev, researcher
5. Joško Fišer, technician
6. Damjan Matelič, technician
7. Tomaž Sirnik, technician
8. Andrej Mohar, technician

We closely cooperate:

(a) with several other research groups at the J. Stefan Institute,

(b) Institute for Electronics and Vacuum Technique,

(c) Faculty of Mechanical Engineering and Institute of Metals and Technologies, Ljubljana.

Whitin several international projects, such as COST 515, bilateral projects with research institutions in Germany and Liechtenstein, we cooperate with:

(a) Balzers Wear Protection - Research and Development Division, Liechtenstein

(b) Max-Planck Institut für Metallforchungs, Stutgart,

(c) Kernforschungszentrum Karlsruhe,

(d) Universität Düsseldorf - Physicalische Chemie und Electrochemie,

(e) Institute for Materials Research - University Hallam - England,

(f) Institute for Materials Research - Limburgs University - Belgium and

(g) Institute of Physics - University West Bohemia - Czech Republic.

4. EQUIPMENT

Our department has the following apparatus for PVD thin film and coatings preparation and characterization:

1. Plasma beam sputtering equipment, SPUTRON DC/RF, Balzers AG., Liechtenstein
2. Thermoionic arc ion plating system BAI 730, Balzers AG., Liechtenstein
3. Thermoionic arc ion plating system BAI 730M, Balzers AG., Liechtenstein
4. Flash evaporation system BAK 600, Balzers AG., Liechtenstein
5. Low energy accelator (10-20 keV) (home made) with magnatic separator (Danfysic)
6. 2 cylindrical magnetrons (home made)
7. Adhesion tester (Automatic scratch tester, CSMS Revetest) Neuchatel, Switzerland
8. Hardness Testing Machine, Mitutoyo, MVK-H2, Micro Vickers H/P, Japan
9. Plasma process Monitor PPM 421, Balzers AG., Liechtenstein
10. Langmuir Probe
11. Quadropole mass analyser, QMS 60, Balzers AG., Liechtenstein

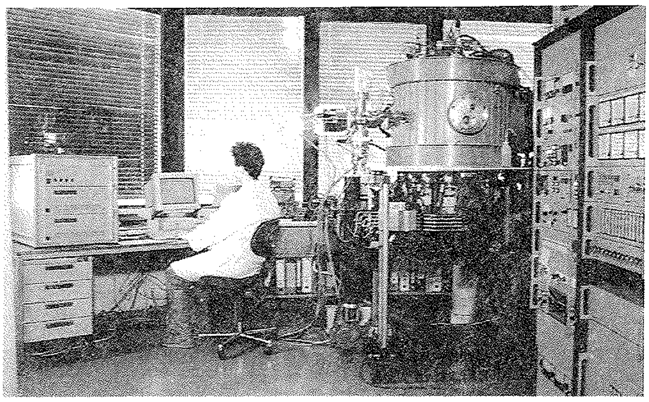


Fig. 1: Hard Coating Centre, Domžale; on the left side there is the new Balzers Plasma Monitor PPM 421 to be used for plasma diagnostics.

12. Ion milling system with two TELETWIN ion source (Institute of Physics, University, Budapest, Hungary)
13. Equipment for metalurgical specimen grinding and polishing (Struers, Denmark)
14. 2 x Ultrasonic cleaning systems (20 kW, Balzers AG., Liechtenstein, 2 kW, Ultraschall technik Martin Walter, Germany)

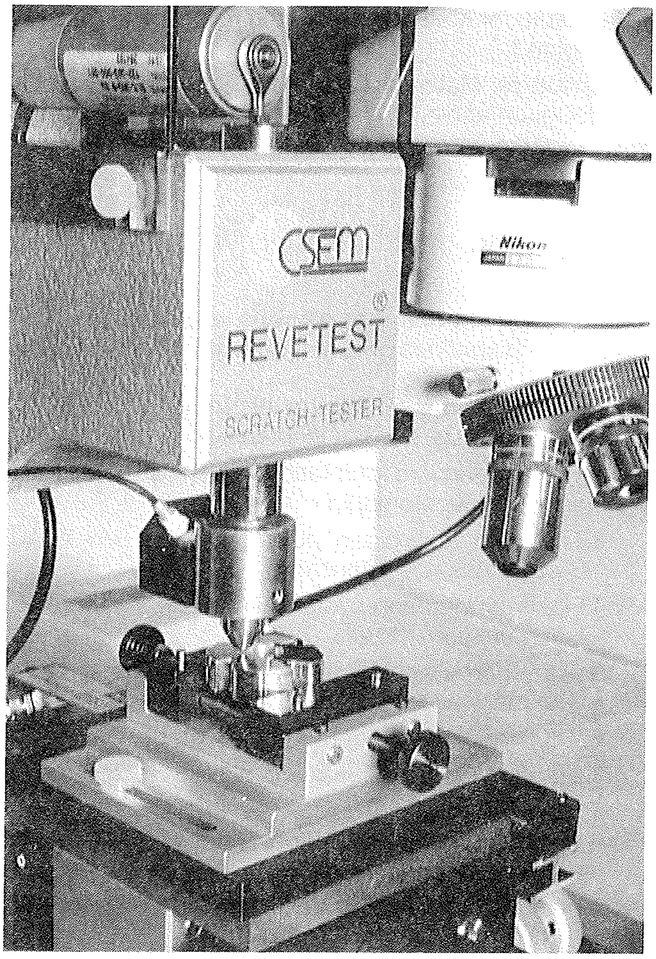


Fig. 2: Adhesion tester - Automatic scratch tester, CSEM, Revetest, Neuchatel, Schwitzerland

15. 4 x optical stereomicroscopes
16. 2 x quartz crystal microbalance (Inficon, Sloan)
17. Low energy broad ion beam source - Kaufman ion source (200-500 eV) (home made)
18. Tolansky interferometer for measurement of thin film thicknesses
19. Instrument for measurement of coating thicknesses, Kalotest tester (home made)
20. Electronic hardness tester, EMT 1101
21. Sheet resistivity prober: four point measurement
22. 4 x Keithly multimeters (1x160B, 3x196DMM)
23. Lock-in amplifier (model 5209, Princton Applied Research)
24. Temperature Controller 818P (Eurotherm)
25. 2 x Data aquisition systems (analog, digital, GPIB, RS232) (Burr-Brown)
26. 2 x PC 386
27. 3 x PC 486

Dr. Peter Panjan
Jožef Stefan Institute
Jamova 39
61111 Ljubljana
Slovenia

ISKRA FERITI

Podjetje Iskra Feriti ima več kot 40-letno tradicijo kot proizvajalec feritnih materialov in navitih komponent. V zadnjem času prodamo preko 80% svojih izdelkov na zahodnoevropskih trgih. Naši kupci so proizvajalci računalniških monitorjev, televizijskih sprejemnikov, telefonskih central, avtomatike in ostalih izdelkov industrijske elektronike.

Svoj program delimo v tri skupine:

MEHKOMAGNETNI FERITI

Mehkomagnetne feritne materiale proizvajamo v širokem spektru, od nizko izgubnih, visokopermeabilnih in močnostnih feritov. Iz teh materialov proizvajamo standardne in posebne oblike feritnih izdelkov. Izdelujemo feritne palčke, cevke, E in U jedra, toroide, RM in FL jedra ter tuljavnike za profesionalno, industrijsko in širokopotrošno elektroniko.

TRDOMAGNETNI FERITI

Iz trdomagnetnih feritnih materialov proizvajamo usmerjene in neusmerjene oksidne magnete raznih oblik in dimenzij. Magnete uporabljajo v beli tehniki, široki potrošnji in avtomobilski industriji.

NAVITE KOMPONENTE

Navite komponente so induktivni elementi, sestavljeni na osnovi feritnega jedra. Izdelujemo jih po naročilih in zahtevah kupcev. Delimo jih v več zvrsti:

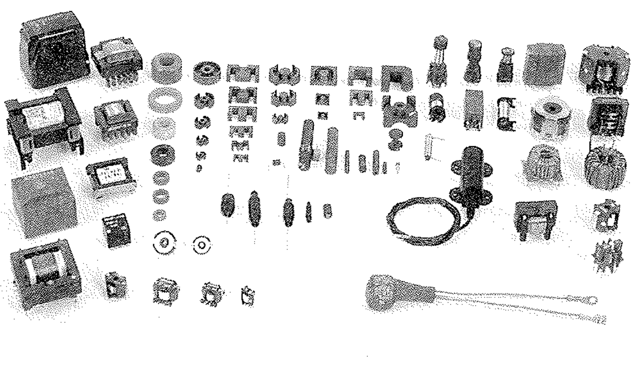
- dušilke na paličastih in toroidnih feritnih jedrih za aplikacije električnih filtrov v električnih in elektronskih napravah, kot zaščita proti sevanju in za odpravo električnih motenj.
- korektorje linearnosti geometrije slike v računalniških monitorjih in televizijskih sprejemnikih.
- transformatorje za stikalne napajalnike in pretvornike, ki delujejo na frekvencah nad 20 kHz. Izdelujemo jih za različne principe delovanja, z galvansko ločitvijo ali brez nje.
- transformatorje za prilagoditev impedanc in ločevanje tokokrogov v telekomunikacijskih napravah.

Kot novosti na področju mehkomagnetnih feritnih materialov in navitih komponent imamo v programu:

- spekter močnostnih feritnih materialov. Med njimi bi opozorili na naš novi material 35G, ki je primeren za delovne temperature do 100 °C in frekvence do 500 kHz.
- navite komponente za površinsko montažo (SMD). Izdelujemo različne tipe in velikosti SMD komponent: EE 12, 6; EF 15; EP 13; RM4; RM5 in RM6.
- korektorje linearnosti z nastavljivo delovno točko za računalniške monitorje. Uporabni so v frekvenčnem področju od 31,5 kHz do 85 kHz. Odlikujejo se po točnosti prednastavitev elektromagnetnih parametrov. Za proizvodnjo teh korektorjev smo razvili računalniško vodeni magnetilni sistem, za katerega imamo patent.

V primerjavi s klasičnimi komponentami, lahko SMD komponente doprinesejo k večji gostoti elementov na tiskanem vezju, možnosti vgradnje na obeh straneh tiskanega vezja, povečajo hitrost montaže elementov in kvaliteto spajkalnih mest ter znižajo stroške izdelave tiskanega vezja.

Na razvojnem področu sodelujemo z Institutom "Jožef Stefan" in Fakulteto za elektrotehniko v Ljubljani. Uspešno sodelovanje je bilo v letošnjem letu zaokroženo s podelitvijo dveh patentov. Patent štev. 9300259 smo prejeli za "Kemijske sestave, tehnološki in proizvodni postopek priprave močnostnih Mn-Zn feritov, uporabnih v frekvenčnem področju od l6 kHz do 1 MHz". Patent štev. 9300284 pa za "Tehnološki postopek kalibracije s trajnim magnetom predmagnetiziranih dušilk".



Izdelki podjetja ISKRA FERITI

ISKRA FERITI
Podjetje za proizvodnjo feritov in navitih komponent, d.o.o.
Stegne 29, 61000 Ljubljana
tel. (061) 159 12 31, faks (061) 159 10 17

Iskra IEZE Holding d.o.o.

Skupina podjetij združenih v Iskra IEZE Holding d.o.o. proizvaja standardne in specifične elektronske in elektromehanske ter zaščitne in senzorske elemente in eletronske podsklope za uporabo v vseh področjih elektroindustrije.

S sledenjem novih zahtev in pristopov v svetu in z izmenjavo znanja in izkušenj na področju programske tržne strategije, priprave in vodenja RR in inovacijskih projektov, uvajanja in vzdrževanja sistemov kakovosti v podjetjih ter osvajanja kulture in pristopa TQM, člani skupine podjetij Iskre IEZE Holdinga laže pridobimo in ohranimo konkurenčne prednosti in lahko nudimo svojim kupcem izdelke v skladu z njihovimi potrebami.

- Razvojno smo se organizirali v okviru Iskra Razvojno raziskovalnega inštituta IEZE.
- Svoje izkušnje posredujemo tudi zunanjim interesentom.
- Dejavnost bomo nadaljevali tudi po pripojitvi Iskra IEZE Holdinga d.o.o. k Iskri Holding d.d.

Iskra IEZE Holding d.o.o.

The group of the enterprises working in the frame of Iskra IEZE Holding d.o.o. produces standard and application specific electronic and electro-mechanic, EMC and overvoltage protective components, sensors and subassemblies for application in all fields of electronics.

Following the new demands and solutions in the world and by interchange of knowledge and experiences in the field of programme and market strategies, preparation and management of R&D and innovation projects, implementation and maintenance of the quality management system in the enterprises and implementation of TQM culture and approach the members of Iskra IEZE Holding are more effective in achieving and preserving the competitive advantages and can therefore supply to our customers the products in accordance with their needs.

- We have our R&D organised within Iskra R&D Institute IEZE.
- We are ready to cooperate and sell our experiences also to the third parties.
- We shall proceed our activities also after merging of Iskra IEZE Holding d.o.o. with Iskra Holding d.d.

Igor Pompe
Iskra IEZE Holding d.o.o.
61000 Ljubljana, Stegne 27

MIEL-SD'95 KONFERENCA - POROČILO
MIEL-SD'95 CONFERENCE - REPORT

23. Mednarodna konferenca o mikroelektroniki, MIEL'95
31. Simpozij o elektronskih sestavnih delih in materialih, SD'95

27.9.95 - 29.9.95, Terme Čatež, Slovenija

Triindvajseta mednarodna konferenca o mikroelektroniki, MIEL'95 nadaljuje tradicijo mednarodnih konferenc, ki jih vsako leto prireja MIDEM - Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale. Že četrtič zapored je ta konferenca potekala skupaj s tokrat enaintridesetim Simpozijem o elektronskih sestavnih delih in materialih, SD'95.

Oba dogodka nudita priložnost mnogim strokovnjakom širom Evrope, da predstavijo svoje delo in najnovejše rezultate, kakor tudi da izmenjajo izkušnje s svojimi kolegi. Rdeča nit konference je ostala možnost druženja, povezovanja in graditve prijateljstva med strokovnjaki s tega področja.

Obe konferenci sta znani tudi zaradi udeležbe priznanih povabljenih referentov.

Letos smo imeli priliko poslušati W.Pribyla, Razvojni center za mikroelektroniko, Beljak, čigar referat "Inteligentna močnostna integrirana vezja - uvod, načrtovanje in uporaba" je obravnaval izredno zanimivo razvijajoče se področje mikroelektronike - načrtovanje analognih, digitalnih in močnostnih funkcij na istem integriranem vezju. Naslednji povabljeni referent, W. Smetana, Tehnična Univerza, Dunaj, v referatu "Načini izvedbe pokopanih kondenzatorjev v debeloplastnih večnivojskih hibridnih vezjih" je obravnaval integracijo pokopanih kondenzatorjev kot način povečanja gostote debeloplastnih hibridnih vezij. M. Pleško, IJS, Ljubljana, je v referatu "Novi izvori sinhrotronske svetlobe - močno orodje za raziskave in proizvodnjo" opisal lastnosti in uporabo sinhrotronske svetlobe v mikroelektroniki in mikromehaniki. G. Herzog, Tehnična Univerza, Graz, je v referatu "Prostroski naboji v znanosti o materialih" pregledno opisal osnove in lastnosti prostorskih nabojev na in v elektrolitičnih, polprevodniških in elektrokeramičnih materialih. W. Kusian, Centralni razvojni laboratorij, Siemens, München, je v referatu "Sončni modul s strukturo pin/TCO/nip" opisal novi tip sončne celice iz amorfnega silicija, katere učinkovitost je večja od konvencionalne strukture pin celice. Zadnji povabljeni referent, N. Sinnadurai, TWI, Anglija, je v referatu "Uporaba cenenih tekočih kristalov za opazovanje in odkrivanje napak delovanja elektronskih komponent in vezij" opisal zanimivo tehniko opazovanja in odkrivanja napak pri delovanju elektronskih komponent.

Zaradi nenadne bolezni se, žal, konference ni mogel udeležiti dr. W. Smetana, eden od vabljenih referentov, vendar je njegov prispevek objavljen v zborniku.

Zbornik referatov, ki smo ga izdali, obsega 400 strani in je razdeljen v več delov, podobno kot je potekala konferenca in sicer MIEL sekcije: Integrirana vezja, Tehnologija, Modeliranje in fizika polprevodnikov, Fotovoltaika in SD sekcije: Tankoplastna tehnologija, Debeloplastna tehnologija, Keramika, kovine in kompozitni materiali.

Letos je bila posebna sekcija posvečena predstavitvi podjetij, raziskovalnih laboratorijev za mikroelektroniko in elektronske materiale ter konferenčnih sponzorjev. Namen predstavitve je bil seznaniti širši krog poslušalcev z delom in možnostmi, ki jih nudijo različne raziskovalne skupine in firme. Same predstavitve niso tiskane v zborniku, vendar jih objavljamo v tej številki revije "Informacije MIDEM".

Obenem se vsem sponzorjem konference zahvaljujemo za zaupanje in finančno podporo.

Konferenca je potekala od 27. do 29. septembra 1995 v Termah Čatež. Poleg naravnih danosti Term in primernih prostroskih zmogljivosti, ki jih nudijo organizatorjem konferenc, sta vodstvo in osebje hotelskega kompleksa s svojo prizadevnostjo pripomogla k uspehu konference in se jim za to prisrčno zahvaljujemo.

Še nekaj suhoparnih podatkov:

- na konferenci je bilo predstavljenih 51 referatov
- celotno število udeležencev konference je bilo 73 in sicer po državah:
  Slovenija: 58
  Italija: 5
  Nemčija: 3
  Švica: 2
  Češka: 2
  Avstrija: 2 in
  Anglija 1

Za konferenčne pogoje, sam potek konference ter strokovni nivo konference lahko trdimo, da je bil visok, število udeležencev in referatov zadovoljivo, pa tudi 16%-na udeležba strokovnjakov iz industrije ni bila zanemarljivo majhna.

Upam, da se zadovoljstvo udeležencev vidi tudi na objavljeni "gasilski" fotografiji, posneti pred konferenčno dvorano.

Predsednik Programskega odbora MIEL-SD'95
Mag. Iztok Šorli, dipl.ing.

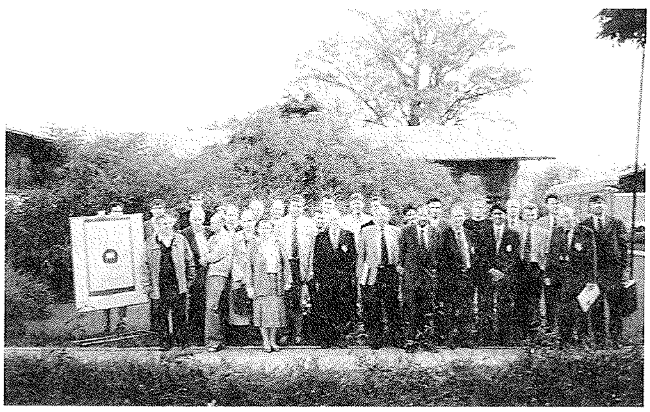
23rd International Conference on Microelectronics MIEL'95 31st Symposium on Devices and Materials SD'95

27.9.95 - 29.9.95, Terme Čatež, Slovenia

The 23rd Conference on Microelectronics MIEL'95 continued the tradition of the annual international conferences organized by MIDEM, Society for Microelectronics, Electronic Components and Materials, Ljubljana, Slovenia. For the fourth time, the Conference was organized jointly with the 31st Symposium on Devices and Materials, SD'95, another annual meeting of the same Society. Traditionally, these conferences have provided an opportunity for experts from all over the Europe to meet and discuss new developments in the fields covered by the Conference. The goal of connection, collaboration and building of the friendship among the scientists and their companies remained the keystone of the organizer.

As well, the Conference has always attracted distinguished guest speakers.

This time we had the opportunity to meet Dr. W. Pribyl, from Siemens Microelectronics R&D Center in Villach whose paper "Integrated Smart Power Circuits - Introduction, Design and Applications" covered important segment of modern microelectronics - integration of analog, digital and smart power on a single chip. Next guest speaker, Dr. W Smetana, from Technical University of Vienna, in the paper "Aspects of Realization of Buried Capacitors in Thick Film Multilayer Circuits" dealt with the integration of capacitors in multilayer circuits as a way to increase the packaging density of thick film hybrids. Dr. M. Pleško, Jožef Stefan Institute, Ljubljana, in the paper "The New Synchrotron Light Sources - Powerful Tools for Research and Production" overviewed the properties of synchrotron radiation and its application in VLSI and micromechanical devices. Dr. G. Herzog from Technical University of Graz, in the paper "Space Charges in Material Science" overviewed principles and applications of space charges in and at electrolytical, semiconducting and electroceramic materials. Dr. W. Kusian and co-authors in "The pin/TCO/nip Solar Module" presented a new amorphous silicon cell type which total efficiency was higher than that of the standard front pin cell alone. Last invited paper by Dr. N. Sinnadurai, TWI, Cambridge: "Thermal and Electrical Operation and Malfunction of Electronics Detected and Imaged by Means of low Cost Liquid Crystal Sensing" described a liquid crystal technique for functional observation and thermal profiling of microelectronic components ranging from ULSI through to hybrid circuits and circuit boards. Unfortunatelly, due to sudden illness, Dr. W. Smetana was unable to attend and present his paper at the Conference. However, his contribution is published in the Proceedings.



The Conference Proceedings, 400 pages in volume, which was published along with the Conference is divided into several parts according to the Conference sessions such as MIEL sessions: Integrated Circuits, Technology, Device Physics and Modeling, Photovoltaic Devices, and SD sessions: Thin Films, Thick Films and Ceramics, Metals and Composites.

This year, a special session devoted to presentation of microelectronics and material research laboratories, enterprises and Conference sponsors was held. The aim of the presentation was getting acquainted with the work and possibilities of different research groups, companies and their projects. These presentations are not published in the Proceedings but appear in this issue of the Journal "Informacije MIDEM".

As well, we would like to thank all our sponsors for their financial contribution.

The Conference was held at Terme Čatež, Slovenia, a picturesque tourist resort, September 27th - 29th 1995. Besides the natural Terme capabilities, as well as its good conference capabilities, also its managerial and technical staff support brought this Conference to a successful end for which we are very thankful.

Let me add some statistical data:

- on the Conference 51 papers were presented
- there were totally 73 participants from the following countries:
  Slovenia: 58
  Italy: 5
  Germany: 3
  Switzerland: 2
  Czech Republik: 2
  Austria: 2 and
  UK: 1

Conference conditions were very good, scientific level of the presented articles was high, we were satisfied with total number of participants and papers presented out of which 16% came from industry.

I hope this satisfaction is reflected also in the published group photo taken in front of the Conference hall.

Program Committee Chairman, MIEL-SD'95
Iztok Šorli, M.S.E.E.

UDELEŽENCI KONFERENCE MIEL - SD'95
MIEL - SD'95 CONFERENCE PARTICIPANTS

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2	AMON SLAVKO	FACULTY OF ELECTRICAL AND COMPUTER ENGINEERING	TRŽAŠKA 25	SVI LJUBLJANA
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7	DE VENUTO DANIELA	DIPARTIMENTO DI ELETROTECNICA E D'ELETRONICA POLITECNICO BARI	VIA ORABONA 4	I BARI
8	DEGEN ANDREJ	FACULTY OF CHEMISTRY AND CHEM. TECH.	AŠKERČEVA 5, P.O. B.537	SVI LJUBLJANA
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13	GIACOMOZZI FLAVIO	IRST INS. PER LA RICERCA SCI. E TECNOLOGICA	LOC PANTE	I TRENTO, POVO
14	GRAMEGNA ENZIO	DU PONT ELECTRONIC DEPARTMENT, MICROCIRCUIT MATERIALS	CHEMIN DU PAVILLON,2	CH GENEVA
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16	HERZOG GERHARD	Institut für Chemische Technologie Anorganicher Stoffe, TU	STREMAYRGASSE 16	A GRAZ
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24	KUSIAN WILHELM	Siemens AG, Corporate Research and Development	OTTO HAHN RING 6	D MÜNCHEN
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46	PRIBYL WOLFGANG	SIEMENS Entwicklungszentrum für Mikroelektronik Ges.m.b.H.	SIEMENSSTRAßE 2, pp173	A VILLACH
47	RESNIK DRAGO	FACULTY OF ELECTRICAL AND COMPUTER ENGINEERING	TRŽAŠKA 25	SVI LJUBLJANA
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MIEL-SD 96
First Announcement and Call for Papers

JOINT

24th INTERNATIONAL CONFERENCE
ON MICROELECTRONICS, MIEL'96
AND
32nd SYMPOSIUM ON DEVICES
AND MATERIALS, SD'96

September 25.- 27.1996, NOVA GORICA, SLOVENIA

ORGANIZER

MIDEM - Society for Microelectronics, Electronic Components and Materials
Dunajska 10, 61000 Ljubljana, SLOVENIA

CONFERENCE SPONSORS

Ministry of Science and Technology of the Republic of Slovenia
Iskra Avtoelektrika, Nova Gorica, Slovenia
Iskra IEZE Holding d.o.o., Ljubljana, Slovenia
Iskra Zaščite d.o.o., Ljubljana, Slovenia
RLS d.o.o., Ljubljana, Slovenia
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Stane Pejovnik, National Institute for Chemistry, Ljubljana, Slovenia

Wolfgang Pribyl, SIEMENS EZM, Villach, Austria

Nava Setter, Ecole Polytechnique Federal de Lausanne, Lausanne, Switzerland

Giovanni Soncini, IRST, Trento, Italy

Iztok Šorli, MIKROIKS d.o.o., Ljubljana, Slovenia

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GENERAL INFORMATION

MIEL-SD'96 is an International Joint Conference organized by MIDEM, uniting two meetings with long traditions: the 24th International Conference on Microelectronics and the 32nd Symposium on Devices and Materials.

Both conferences are very well known in the electronic community. Hundreds of distinguished scientists from all over the world took part in the MIEL-SD conferences in the past. The goal of establishing contacts, collaboration and friendship among scientists and their companies remains the keystone of the organizer.

The conference will be held in the **HIT HOTEL CASINO PERLA, NOVA GORICA, SLOVENIA, September 25.-27. 1996.**

ORIGINAL PAPERS IN THE FOLLOWING AREAS ARE SOLICITED:

- Novel monolithic and hybrid circuit processing techniques
- New device and circuit designs
- Process and device modeling
- Semiconductor physics
- Sensors and detectors
- Optoelectronics
- Photovoltaic devices
- New electronic materials and applications
- Electronic materials science and technology
- Materials characterization techniques
- Reliability and failure analysis
- Education

Presentation of companies, laboratories and conference sponsors working in the field of microelectronics, electronic devices and materials will be held after the afternoon sessions.

INVITED PAPERS:

The following speakers will present introductory review papers before sessions:

1. **M.Bui Ai, Universite Paul Sabatier - CNRS, Toulouse, France**
   "Zinc Oxide Based Varistors and Parallel Circuit Protection. The State of the Art"

Abstract: In this conference the Author gives the historical of the research and the technology of Zinc Oxide based varistors since 1960 to this day with the following points:

- Discovery of the varistor effect in 1960 by Russians
- Industrial development by Japanese
- Current manufacture technique
- Current performances: Threshold voltage, Residual voltage, Energy absorption capacity, Aging
- Main applications: High voltage, Distribution voltage and Domestic protection module
- Main manufacturers in the world

The author describes the main orientations of research and development:

  - Increase of the threshold voltage (from 200V/mm to 400V/mm)
  - Increase of the energy absorption capacity (from 200J/cm^3 to 600J/cm^3)
  - Mixed powder method for making varistors

2. **C. Claeys, IMEC, Leuven, Belgium**
   "Technological Challenges for Future Silicon Technologies"

Abstract: An overview will first be given of the present status and the future requirement in association with the increasing functionality added to the core technologies, such as e.g. mixed signal, low voltage, low voltage non volatile memories and smart technologies. This will put stringent requirements on the optimization of different process modules. Future trends related modules such as optical lithography, isolation, salicides and interconnects will be addressed. To some extent restrictions imposed by device physics and reliability aspects have to be taken into account. Finally, the potential of Silicon-on-Insulator technologies and/or low temperature device operation are pointed out.

3. G. Dražič, Jožef Stefan Institute, Ljubljana, Slovenia
"Analytical Electron Microscopy of Advanced Ceramic Materials"

Abstract: The development of advanced electronic materials is strongly connected to the simultaneous development and use of different methods for microstructural characterization. In many cases the knowledge of a chemical composition and a structure of submicron (or even nanometer) phases (precipitates, intergranular layers, corrosion products, interface layers) is important for better understanding of chemical and physical processes taking place during the fabrication and use of ceramic materials.

Analytical electron microscopy (transmission electron microscope combined with energy dispersive X-ray spectroscopy) was found to be a very useful technique for the investigations of advanced ceramic materials due to a relatively small analyzed volume and simultaneous examination of structure, structural relationships between phases (using electron diffraction techniques) and chemical composition. In the lecture principles of transmission electron microscopy and quantitative elemental analysis using energy dispersive X-ray spectroscopy will be described and examples of the use of the analytical electron microscopy in the development of advanced ceramic materials will be displayed.

4. Vilho Lantto, University of Oulu, Oulu, Finland
"Gas Sensors as an Example of Research with Thick Film Transducers"

Abstract: The research on solid state transducers started in the University of Oulu in the middle of the 1970s, soon after the beginning of the research on thick film hybrids in the Microelectronics Laboratory. Different thick film printing techniques have been the main techniques in our research on solid state transducers. Screen printing is the common technology for the fabrication of both hybrid circuits and thick film sensors, which has served also as a good possibility of the integration of our thick film sensors with the necessary signal processing electronics in the form of a hybrid module. A novel double paste screen printing method was also developed in our laboratory for the fabrication of multilayer transducer structures. Gravure offset printing is another thick film printing technique which offers the possibility of printing fine lines down to a width of about 50 μm. Therefore, it offers a possibility for more dense structures, especially in thick film sensor arrays. An useful feature of the technique is that it offers a possibility to 3-dimensional printing, which allows a printing of complicated structures.

Semiconductor gas sensors are taken here as an example of our study on thick film transducers. Our research on semiconductor gas sensors has continued since 1983 and during 1987-1991 we were a research partner in an EUREKA project that aimed to develop semiconductor gas sensors for some practical applications. We have also studied the possibility of using semiconductor gas sensors for monitoring of pollutant gases in combustion emissions and in city air. Semiconductor gas sensors use the chemical sensitivity of the semiconductor surfaces for gas sensing applications. Semiconducting oxides are usually employed in these devices as gas sensitive resistors for monitoring changes in oxygen partial pressure (lambda sensors) and small concentrations of impurity gases in different ambient atmospheres. In a semiconductor gas sensor, the chemical receptor signal on the semiconductor surface is transduced through the microstructure of a sintered ceramic into a resistance change of the ceramic. Therefore, different thick film techniques serve as a useful and economic way to produce these devices.

5. A. Lechner, SIEMENS EZM, Villach, Austria
"Innovative Smart Power Semiconductors for Automotive and Industrial Applications"

Abstract: The paper gives an overview of the manifold benefits of smart power semiconductors. Today, these devices are the key for further fuel reduction of the cars, for energy saving in industry and household, as well as for increased safety and comfort of future automobiles. The presentation links technology features, circuit implementations and device characteristics in order to show the interdependence of all required aspects for practical electronics system solutions.

6. B. Margesin, G. Soncini, M.Zen, IRST, Trento, Italy
"Chemical Sensors Based on ISFET Transducers"

Abstract: An up-to-date overview of the status and trends of Chemical Sensors based on Silicon Integrated Ion Sensitive Field Effect Transistors (ISFET) will be presented, with emphasis on multisensing arrays with signal pre-elaboration circuitry integrated on the same sensor chip. This requires the development of a dedicated ISFET-CMOS compatible fabrication technology, since the ISFET ion-sensing layer, usually LPCVD silicon nitride on thermal oxide, imposes high temperature processing steps that cannot be accommodated into a conventional CMOS poly-Si gate processing sequence. The ISFET-CMOS technology approach proposed and currently carried on in IRST will be described, and examples of device characteristics, both ISFET and CMOS, currently being fabricated, will be presented and discussed. Problems related to device reliability and packaging, as well as to different possible approaches aimed at integrating reference electrodes on the sensor chip will be addressed.

Examples of applications mainly devoted to environmental monitoring, currently being developed at IRST, will be presented.

7. Paul Muralt, Ecole Polytechnique Federal de Lausanne, Lausanne, Switzerland
"PZT Thin Films for Micro Sensors and Actuators"

Abstract: The paper will review deposition, integration, device fabrication and applications of PZT films. Emphasis is given to piezoelectric thin films on membranes (e.g. for micromotors) and pyroelectric thin films for infrared detectors.

Due to its outstanding properties, i.e. high piezoelectric coefficients and its high ferroelectric polarization, the perovskite structured compound $PbZr_xTi_{1-x}O_3$ (PZT) is one of the most studied materials for ferroelectric thin

films. At high Ti concentrations a suitable pyroelectric material with a fairly high pyroelectric coefficient and a rather low dielectric constant is obtained. Compositions near the morphotropic phase boundary ($x \approx 0.5$) are chosen for high piezoelectric coefficients.

Low voltage ultrasonic micromotors are an attractive field of applications for piezoelectric thin films. The first well working PZT thin film micro motor has recently been demonstrated, applying a hybrid type motor with an elastic fin rotor on a silicon diaphragm. The motor could be operated with less than 1.0 V_{rms}. A detailed characterization of diaphragms with PZT thin films will be presented.

Pyroelectric infrared detection could be an another fruitful application for ferroelectric thin films. For not too low frequencies, the sensitivity of micro machined thin film devices is potentially as high as the one of single crystal devices. This is achieved by an extremely good thermal isolation of the element by micromachining techniques. In addition, the estimated production costs are low and interesting for sensor arrays. Pyroelectric thin films are in direct competition with thermopile structures. Whereas the latter hardly achieve higher sensitivities than 100 V/W, a value of 700 V/W was achieved in our laboratory with a thin film pyroelectric array element on a micromachined membrane.

8. **H. Schmid, B. Kegel, W. Petasch, G. Liebel, Technics Plasma GmbH, Kirchheim bei München, Germany**
   "Low Pressure Plasma Processing in Microelectronics"

Abstract: Low pressure plasmas are widely used to modify surface properties of different materials. This technique is indispensable for manufacturing of very large scale integrated circuits used by the microelectronics and electronics industry.

We will present a newly invented dry cleaning process of wafer boats coated by LPCVD - Si and Si_3N_4 through plasma etching, which has a dramatic decrease of boat consumption. Another plasma process in IC fabrication is photoresist ashing. Results of a microwave batch system will be depicted. Information about both etching equipment will be given.

On the other side ICs are mounted on PCBs and bonded to gold pads. These pads can be efficiently cleaned through a Low Pressure Plasma increasing the pull strength of bond wires.

Classic PCB technology using conventional drilled holes is limited in dimensions. The Dycostrater® Technology which is using a Low Pressure Plasma Drilling Process is pushing the dimensions of PCB structures beyond these limits.

SUBMISSION OF PAPERS

PREPARATION OF SUMMARIES

A summary not longer than 60 lines is required. It must clearly state what new results have been obtained and what techniques used.

SUMMARY DEADLINE

Deadline for receiving the summaries is **April 15th, 1996.**

NOTIFICATION OF ACCEPTANCE

Deadline for the notification of the paper acceptance is **May 15th, 1996.**

DEADLINE FOR RECEIPT OF PAPERS

Deadline for the camera ready manuscript of the paper is **September 1st 1996.**

PREPARATION OF PAPERS

Papers should be prepared on a maximum of **6 pages in A4 format**, camera ready for reproduction in the Proceedings. Invited papers are not limited to 6 pages. Further detailed information will be given in the notification of acceptance.

CONFERENCE PROCEEDINGS

Invited papers and accepted papers will be published in the Conference Proceedings distributed at the Conference registration.

LANGUAGE

The official Conference language is English.

IMPORTANT DATES

Summary deadline: **April 15th**
Notification of acceptance: **May 15th**
Advance Programme: **August 15th**
Paper deadline: **September 1st**
Final conference programme:
on registration, **September 25th**

REGISTRATION

- The registration fees are as follows:
  MIDEM members who are also employees of MIDEM or Conference sponsors: **150 US$**
- MIDEM Society members: **210 US$**
- Employees of MIDEM or Conference sponsors: **240 US$**
- FULL registration fee: **300 US$**

The fee includes Conference Proceedings and free access to all Conference events. A welcome cocktail party will be held on September 25th and the Conference dinner on September 26th.

Undergraduate students have free access to all Conference sessions on submitting their study papers. For other Conference events they will be additionally charged.

ACCOMMODATION

We strongly recommend accommodation in the Hotel Casino Perla,Nova Gorica, where the Conference will take place.

Nova Gorica is about 100 km west of Ljubljana on the Slovene-Italian border. The best way to reach the Conference site is to fly to Ljubljana or Trieste airport and then to continue by car.

Please make Your hotel reservation directly to:

HIT HOTEL CASINO PERLA (for MIEL-SD'96)
Mr. Fabjan Vičič or Mrs.Majda Vodopivec
Kidričeva 7, 5000 Nova Gorica, Slovenia
tel.+386 (0)65 28 890
fax.+386 (0)65 28 885

Programme and Organizing Committee:

MIDEM Dunajska 10
1000 Ljubljana, SLOVENIA

tel.+386-61-312 898,
fax.+386-61-319170
Mrs. Meta Limpel

Preliminary Registration Form
MIEL-SD'96 Conference
Nova Gorica, September 25. - 27. 1996

Family name　Given Name　Title

Company　Address

City　City code　State

Telephone　FAX　E-mail

Date　Signature

IMPORTANT :
Further Conference information will be distributed only to persons returning this registration form !

Please circle as appropriate :

I intend to contribute a paper	YES	NO
I intend to take part in the conference	YES	NO
I intend to present the work of our laboratory	YES	NO
I intend to present our company	YES	NO
I would like to make a commercial presentation	YES	NO
I am interested in sponsoring the conference - send me more information	YES	NO

COMMENTS :

Please fill in the preliminary registration form and send it by April 15th to the address :

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UPORABA MIKROELEKTRONSKIH KOMPONENT
APPLICATION OF MICRO COMPONENTS

This time we publish two contributions from AMS, Austria Mikro Systeme International, Graz, Austria

First Universal Single-Chip Telephone!

Intelligent chip easily adaptable to any PTT environment: Simply Plug and Play
High quality speech circuit / repertory dialler / melody generator / ringer
Can be used in all telephones world wide
Virtually no external components
Optimum ultra-high integration
Easy use and high comfort
One chip = one telephone

AMS announces the immediate availability of **the first universal single chip telephone in the world,** a continuation of the widely accepted and successful AMS single chip concept introduced in 1993.

The main feature of this chip is that with the realization of a "plug and play" concept - the first of its kind in the industry - it can be easily implemented by any telephone manufacturer worldwide. The telephone manufacturer does not need to bother with programming the chip according to the highly complex local PTT requirements - the intelligent AMS single chip is built into the telephone and is immediately operational and ready for individual utilization!

This new universal chip includes an enhanced speech transmission circuit with repertory dialler, melody generator and ringer **all on a single chip:** the AS2533, an integrated circuit that performs all the functions required of a medium range high performance electronic telephone: The advantage of this new ASIC is that it minimizes design efforts and the external component count by up to 80% of the average telephone set!

The AS2533 is now available in 28 pin DIP or SOIC packages. For further information and a detailed data sheet please contact your local AMS Sales Office or AMS Corporate Communications, Schloss Premstatten, A-8141 Unterpremstatten.

Note to the Editor:

The AS2533 is designed to be in compliance with ETSI standards for connection to the analogue PSTN (Public Switched Telephone Network). Since the RFI sensitivity has been minimized by the consequent use of CMOS technology no expensive coils are needed.

The AS2533 allows an easy adaptation to a wide variety of different international PTT requirements without changing the PCB of the telephone. This is provided by built-in pre-programmed pin options.

The device incorporates LD/MF repertory dialling functions, melody generation, ring frequency discrimination and an advanced speech circuit. Additionally to the basic functions, the speech circuit includes soft clipping. The AS2533 also incorporates a volume control for the earpiece.

Furthermore, a pacifier tone and LED indication for higher user comfort during programming is made available. Also, when the line is busy, the repeat dialling key when pressed will automatically regularly redial the call until the line is free.

During on-hook the repertory number store is maintained with less than 0.1 mA - the device has an operating range from 13 mA to 100 mA but can operate down to as low as 5 mA with a somewhat reduced performance. An on-chip power-on reset assures correct start-up. Furthermore, no battery is required. The device features a 31 digit last number redial and a 14 number repertory store.

Universal Single Chip Telephone IC with 14 Number Repertoary Dialler - AS2533

Key Features

- Line/speech circuit, LD/MF repertory dialler and tone ringer on one 28 pin CMOS chip
- Operating range from 13 to 100 mA (down to 5 mA with reduced performance)
- Soft clipping to avoid harsh distortion
- Volume control of receive signal
- Line loss compensation selectable by pin option
- Low noise (max. - 72 dBmp)
- Real or complex impedance
- NET 4 compatible
- LD/MF switchable dialling
- Pacifier tone during programming
- 31 digit last number redial
- 14 memories, 4 direct/10 indirect
- Repeat dialling by busy lines or engaged
- Sliding cursor protocol with comparison
- Pause key for access pause or wait function
- 3 flash keys,100 ms, 280 ms and 600 ms
- On chip MF filter (CEPT CS 203 compatible)
- Ring frequency discrimination
- 3-tone melody generator

General Description

The AS2533 is a CMOS integrated circuit that contains all the functions needed to form a high performance electronic telephone.

The device incorporates LD/M F repertory dialling, melody generation, ring frequency discrimination and a high quality line/speech circuit.

A RAM is on chip for a 31 digit last number redial and 14 memories each containing up to 21 digits/data. The sliding cursor procedure makes the LNR function easy to use under various PABX systems. Also centrex keys are provided.

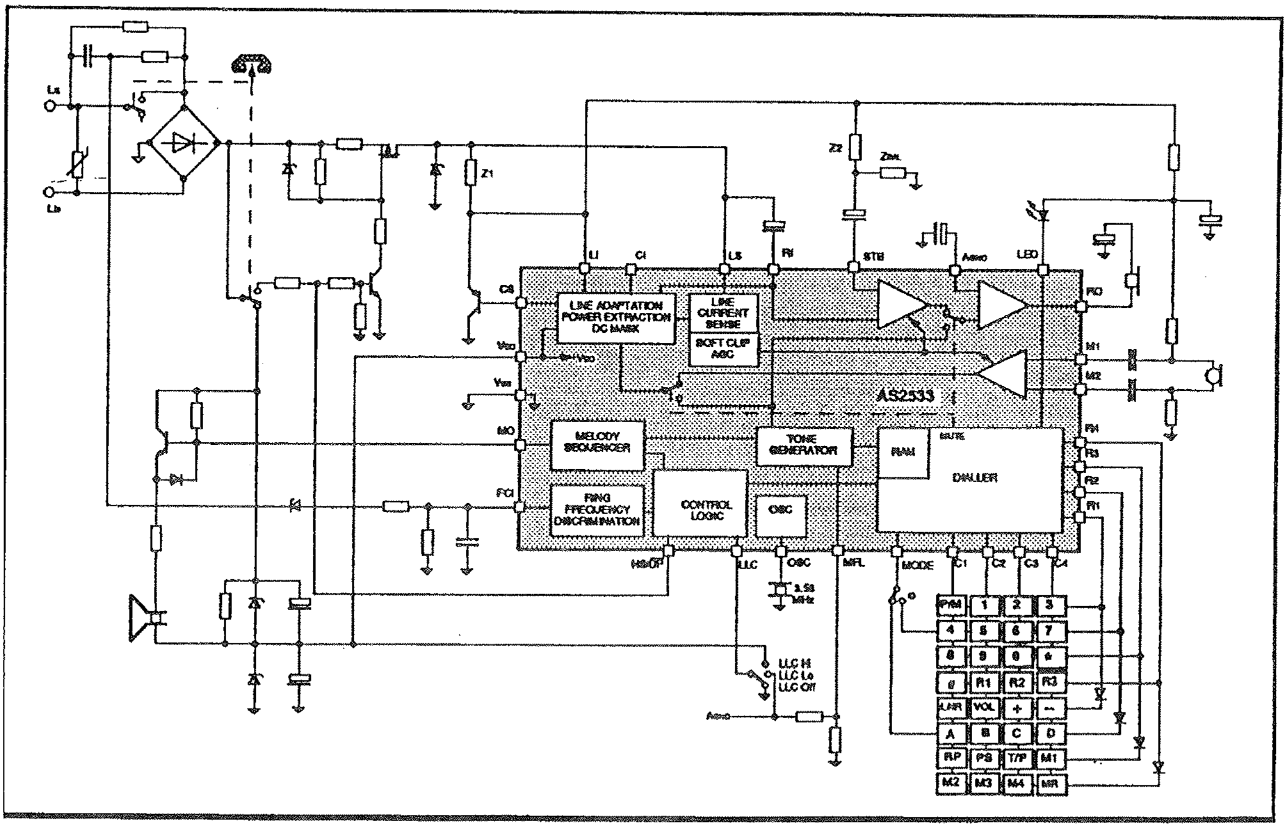
The AS2533 incorporates a volume control for the earpiece. The volume can be controlled by the VOL key (+6 dB) or by the -/+ keys (+6 dB/-4 dB in 5 steps).

The versatility of the circuit is provided by pin options and a few external components. This allows easy adaptation to different PTT requirements.

Package

Available in 28 pin SOIC or DIP.

Block Diagrame



Mixed Signal ASIC's with Embedded Microprocessor

The integration of an embedded microprocessor, or microcore into an ASIC is becoming much more common. Increasingly the use of microcores is extending beyond those few applications where the volumes are enormous. The practical difficulties of programming the core and debugging it within such an ASIC have been addressed. What is more, effective mixed signal ASIC technology means that embedding a micro into an otherwise analogoue device is a little harder than carrrying out any other mixed signal ASIC development, subject to the need to programme the microcore.

CMOS processes are particularly suitable for mixed signal ASICs with embedded microprocessor. These processes have themselves benefited from the drive to develop more highly integrated single chip micro-controllers. In particular most major manufacturers like to offer analogue functions such as A/D and D/A, to help interface the micro to the world. The technology has been developed further to allow the addition of analogue components resistor and capacitors. Transistor performance has also been characterising in detail, to allow analogue modules to be designed and built successfully. The experience gained in developments of this kind has been invaluable in enabling the design and implementation of more sophisticated mixed signal / embedded designs.

Two approaches

Two different starting point can be adopted when loocking at mixed signal ASIC design. The first (and most silicon efficient) is the design and integration of a processor core including memory structured to perform the specific task required. Such a function block is often referred to as DSP engines. It is becoming common practice for such a block to be included within an ASIC.

The alternative is to integrate a microprocessor core that is logically or functionally equivalent to an established standard microprocessor. This approach gives the ASIC designer the ability to re-use his system knowledge and software which may have been developed over a period of many years.

The second approach is by far the most popular. As example, consider the integration of a 8 bit microcore which is functionally compatible with the industrial standard microcontroller family 68HC05. That is, the core is 100% machine code compatible and offers an extended instruction set and enlarged address space. Such a core is available from AMS in a Standard Cell format (AMS 2205). This "microcore" contains datapath, microcode ROM and sequencer. This part of the embedded microcomputer would be optimised to the specific requirements using a microcore synthesis tool. The resulting netlist is then automatically layout.

A standard or a customised interrupt controller, the stack area (which may be modified) and scan paths for testing and debugging are then added to the core. If the microcore is to be used in a system emulator a break point register may be also be added.

In parallel, of course, the rest of the ASIC is developed, which will contain peripheral blocks such as ROM, RAM, I/O and any other functions required.

Simulation

At simulation, core operation is modelled using an HDL (hardware description language) model of the microcore. This can be placed within a hierachial design and simulated concurrently with the peripheral blocks. These peripheral blocks are considered normal ASIC blocks. ROM and RAM will normally be automatically compiled. HDL simulation models are also preferred for these blocks. Peripheral block registers should be decoded in accordance with the memory map.

The CMOS process on which the ASIC integration is targeted will be a tradeoff between achieving the desired performance for the microcontroller, and optimising the peripheral circuitry. In other words, the speed, size and complexity of both the analogue and digital circuitry needs to be considered as is normal for mixed signal ASICs. The microcore is considered as a block of digital logic (synthesised gates) which will be merged with the rest of the ASIC at the netlist stage prior or during the IC layout stage. Its speed and silicon area can be optimised using the microcore synthesiser for the selected process.

The remaining peripheral circuitry and any additional functions will need to be simulated and finally designed within an IC design software suite which contains a model of the microcore. This is usually done by the silicon vendor, and requires a "golden simulator" for timing check and design "sign-off".

Developing the microcore software

One difficulty in the development of a Mixed signal ASIC with embedded microcore, is the emulation of the microcore for software debugging. In practice, this can only be done if the core is separate from the other circuitry, since an embedded microcore is not normally accessible via the ASIC external pin connections. Emulation of the microcore within the ASIC would only be possible by an emulating of the entire ASIC, not economically feasible for each ASIC design.

Development cost and process considerations mean that the design and lyout of a second EEPROM/EPROM based ASIC to produce a programmable version of the embedded microcore is not a practical solution.

It is up to the ASIC vendor to provide adequate emulation support for their microcore implementations. AMS provides a PC based solution for system emulation and Software debugging of the AMS2205 including software (including ScanDebugger) and a 2205 Emulation board. The board contains a fully bonded out version of the generic microcore, RAM, ROM, PC-interfaces, emulation probes, signal recorder and PGA's (Programmable Gate Arrays).

From front end design of the digital peripheral cells, the circuit designer can generate suitable format netlists, which can be programmed into the PGAs, to give system emulation. As a result the peripheral digital circuit design can using the tool above and any additional simulator at very low startup costs, subsequently to be transferred to standard cell (or full custom) silicon design. If needed a breadboard can be appended to the emulation system, explained above, to test functionality and to develop the detail of the Analogue part of the specification. It follows that system design and software development can begin at any stage within the project cycle.

Using a DSP engine

The dedicated Microcore (or DSP engine) is designed from the gate level upwards or from HDL models downward in common with all digital functions. It is sometimes easier to implement algorithms in software than it is to generate hardwied blocks which performing the same function. This is particularly true where large quantities stored in RAM (or registers) during the calculation. These functional blocks are most useful when a small number of operating instructions can perform a very repetitive task (Reduced Instruction Set). This approach is not ideal for general purpose control application of a Microcomputer. Generally such a design path requires a higher degree of design expertise and time than using a compiled microcore, but has the advantage of yielding more efficient use of silicon and thus lower unit costs.

Conclusion

It is fair to say that imbedding a microcore into an analogue ASIC in no harder than developing any other mixed signal design. The only special element is the code development - and here it pays to ensure that the selected vendor has had an acceptable solution before making a commitment.

As always, the key to success in mixed signal ASIC development is a close dialogue between vendor and the designer.

Austria Mikro Systeme International AG
Schloss Premstatten
A-8181 Unterpremstatten, Austria
Tel.: +43 3136 500
Fax: +43 3136 52 501

PRIKAZI DOGODKOV,DEJAVNOSTI ČLANOV MIDEM IN DRUGIH INSTITUCIJ REPRESENT OF EVENTS, ACTIVITIES OF MIDEM MEMBERS AND OTHER INSTITUTIONS

Prof. dr. Miha Drofenik, inž. Andrej Žnidaršič in mag. Marjeta Limpel - dobitniki nagrade RS za znanstvenoraziskovalno delo

*Skupina je dobila nagrado za izum kemične sestave in tehnološkega postopka za izdelavo novih močnostnih Mn-Zn feritov. Brez teh materialov, je med drugim rečeno v utemeljitvi podelitve, si ne moremo zamišljati sodobne profesionalne elektronike, komunikacijske tehnike in zabavne elektronike. V skupini so trije člani. **Dr. Miha Drofenik** je raziskovalni svetnik na inštitutu Jožef Stefan, kjer vodi skupino za magnetno keramiko, hkrati pa je tudi redni profesor na fakulteti za kemijo in kemijsko tehnologijo v Mariboru, kjer predava tehnologijo keramike. Diplomirani inženir kemije **Andrej Žnidaršič** je kot vodja razvoja zaposlen v tovarni Iskra Feriti. **Mag. Marjeta Limpel** je 30 let vodila razvoj v Feritih; skupaj z inž. Žnidaršičem sta delala približno štiri leta, po njeni upokojitvi pa je delo na področju feritov prevzel on.*

Inž. Andrej Žnidaršič, mag. Marjeta Limpel in prof. dr. Miha Drofenik.

• *V Ljubljani je tovarna, ki dela ferite že nekaj desetletij in tudi vi ste dobili nagrado za neko vrsto feritov. V čem je razlika med vašimi in tistimi, ki jih delajo v Iskrini tovarni?*

Drofenik: Feritna keramika je znana že več desetletij. Proizvajati so jo začeli takoj po drugi svetovni vojni in glavni iznajditelji so bili Japonci in tudi Nizozemci. Izboljševanje teh materialov je napredovalo vzporedno z razvojem elektronike, ki se je v zadnjih desetletjih močno razvila. Danes med drugim prevladuje tudi tako imenovana močnostna elektronika - uporabljamo jo za prenašanje moči - ta pa potrebuje drugačne materiale. To je sicer še vedno ferit, vendar z drugačnimi lastnostmi. Pri tem gre pač za boj s časom in z lastnostmi ferita, ki se že desetletja razvija. Današnji feriti imajo še vedno spinalno strukturo, vendar so njihove lastnosti bistveno drugačne. Spineli so spojine, ki imajo podobno zgradbo kot mineral spinel, le z drugačno kemično sestavo; deloma so nekateri ioni zamenjani, tako da imajo bistveno drugačne lastnosti. Uporabljajo se v elektroniki, v tem primeru v močnostni elektroniki. Za prenašanje moči, za napajanje sistemov itd.

• *Kaj je močnostna elektronika?*

Žnidaršič: Prek ferita z visoko frekvenco prenašamo določeno moč, ki je potrebna za delovanje različnih elektronskih naprav. Vsi ti feriti se vgrajujejo v izredno širok spekter elektronskih komponent. Če vzamemo področje široke porabe, so to naprave kot televizorji in sploh celotna računalniška industrija, vsa mikroelektronika, vse telekomunikacije. Bistvo našega izuma je v tem, da smo z vgradnjo nekaterih ionov bistveno spremenili osnovne lastnosti obstoječih feritnih materialov in je zdaj nova generacija dejansko sposobna prenašati moč pri frekvencah od 16 kHz pa do enega megaherca, torej na izredno visokih frekvenčnih področjih. To pomeni, da je možnosti aplikacije dejansko nešteto.

• *Poleg močnostne elektronike na širokem področju elektronske industrije najbrž obstaja še neka druga, ki ni močnostna. Katera je to?*

Žnidaršič: Ja, obstaja. Doslej smo govorili o materialih, namenjenih prenosu določenih moči, njihova funkcija je napajanje, vendar poznamo še druge feritne materiale, ki jih uporabljamo kot različne dušilke, filtre, poleg njih pa še različne induktorje, ki so za induciranje določene napetosti in so potem funkcionalno povezani v določenem elektronskem sklopu. Vsak elektronski sklop potrebuje izvor napajanja. To je funkcija močnostnih feritov, kot rečeno pa se vgrajujejo še drugi feritni materiali, ki imajo druge funkcije, denimo odpravo motenj itd.

• *Vaš ferit, piše v utemeljitvi, se lahko uporablja tudi v hi fi napravah. Ali to pomeni, da bomo odslej imeli boljše ojačevalnike, laserske gramofone itd.?*

Žnidaršič: Pri tem gre zlasti za miniaturizacijo feritnega jedra. Če se nam posreči zmanjšati visokofrekvenčne izgube feritnega jedra, lahko prenos moči izvedemo pri višjih frekvencah, pri katerih pa je možno uporabiti ferite z manjšo prostornino. Torej gre za isto funkcijo, kot jo ima na primer ferit s prerezom petih kvadratnih centimetrov, z novim materialom - če govorimo o hi fi napravah - pa dobimo enako napajanje pri prerezu velikosti enega kvadratnega centimetra. Miniaturizacija je danes praktično glavno gibalo elektronske industrije.

Drofenik: Če pri prenosu moči zvišamo frekvenco, se prenesena moč tudi poveča, ker se poveča število impulzov v časovni enoti. Tak ferit mora biti izjemno kvaliteten, da so izgube v njem manjše. Z različnimi dodatki ga moramo preoblikovati, kar zahteva veliko temeljnega znanja, in s tem zmanjšati prostornino, seveda pa moramo obratovalno frekvenco povečati. Tako pridemo na primer s 300 kHz na en megaherc, prostornina pa se hkrati zmanjša recimo za desetkrat. Če bi nam uspelo napajati s frekvenco enega megaherca, bi bil ferit majhen kot naprstnik. Prenosno elektronsko napravo, ki jo danes težko nosite na rami, boste potem morda nosili kar v žepu. Dejansko gre za novo generacijo feritov, ki jih trenutno še ni na trgu. Ta se perspektivno odpira v letih 1997-98, tako da smo s tem razvojem nekje v svetovnem vrhu.

• *Precej je bilo že tudi prodaje, kar 20 milijonov kosov v letu 1994.*

Žnidaršič: Ja, prodajamo že feritne materiale do 500 kHz, predvsem na zahodnoevropske trge, to so Nemčija, Švica in skandinavske države. Toda postopoma prihajajo v poštev omenjeni novi materiali, tiste z uporabno frekvenco od 16 do 500 kHz pa že normalno prodajamo.

• *To torej kupujejo tovarne, ki pač delajo različne elektronske naprave.*

Žnidaršič: Tako je.

• *Ali je to nekaj podobnega, kot če bi kupil vijake, proizvajalec pa sploh ne bi vedel, za kakšen namen jih bom potreboval?*

Žnidaršič: Ni čisto tako. Res je sicer, da se ti elementi vgrajujejo v določene elektronske sklope, vendar je material, iz katerega so elementi narejeni, nadvse specifičen. Ko si enkrat pridobimo kupca in postanemo njegovi dobavitelji, ta zelo težko zamenja proizvajalca, saj je njegova odvisnost izredno velika. Zato je tudi boj za prodor na trg na tem razvojnem sektorju izredno hud.

• *Kupec torej natanko specificira: rabim tak in tak ferit in vi potem delate zanj natančno take.*

Žnidaršič: Tudi tako je, ja.

• *To je ferit Mn-Zn, dodatka sta torej mangan in cink.*

Žnidaršič: Osnova so železov mangan in cinkovi oksidi, ki tvorijo spojino s spinelno zgradbo. Toda majhni dodatki, ki so najstrožje varovana tajnost, določene mere tudi količine in tako naprej, pa odločilno vplivajo na končne magnetne lastnosti.

• *To je tisto, zaradi česar jih drugi ne morejo delati, mar ne?*

Žnidaršič: Točno tako. Če sledimo razvojnim trendom, ugotovimo, da se pojavljajo različne kombinacije teh dodatkov. Razvili smo pač svoj sistem, ki uspešno funkcionira.

• *Majhni dodatki so najbrž majhne količine različnih elementov...*

Drofenik: Upornost takega ferita je mogoče spremeniti na več načinov in po enem od njih se spremeni upornost mej med zrni. To je pač keramika, ki ima zrna.

• *Samo podvprašanje: to se torej vedno dela s sintranjem, mar ne?*

Drofenik: Ja, to je postopek, po katerem se izdeluje keramika - zgoščevanje surovih oblikovancev iz prahu pri višji temperaturi.

Žnidaršič: Najprej sta pomembni osnovna kemična sestava in priprava prahu, oblikovanje je znano, sledi pa sintranje v zaščitni atmosferi, ki vpliva tako na zgoščevanje materiala kot tudi na končne elektromagnetne lastnosti. To, skupaj s pravilno kombinacijo in količino osnovnih mikrododatkov, je tajnost vsake feritne tovarne in do tega podatka ne pride nihče.

Drofenik: Še o dodatkih. Te je teba izbrati, ione je treba izbrati s pravim polmerom in nabojem, da se ne puste raztopiti v kristalni mreži, ker jih ta kot tujek zavrže in se koncentrirajo na meji med zrni, kjer tvorijo neprevodno plast, ki poveča električno upornost ferita. Mehanizem izboljšanja električne upornosti in drugih lastnosti ferita smo tudi objavili v ustreznih mednarodnih strokovnih revijah.

• *Torej pri tem ni šlo zgolj za tehniko, za tehnično področje, ampak nekoliko tudi za temeljne raziskave.*

Žnidaršič: Pretok informacij na področju novih feritnih materialov je strogo zaupna zadeva. Mi pokrivamo celotno področje, od ideje do prodaje.

• *Kar je natanko tisto, o čemer v Sloveniji že ves čas govorimo, namreč da moramo razvijati ves proces, od temeljne raziskave do trženja izdelka.*

Žnidaršič: Povezava med industrijo in pa inštitutom je tu res dobra. S profesorjem Drofenikom delava skupaj že deset let in rekel bi, da sva uspešno razvila in potem tudi vpeljala na trg že kar nekaj novih materialov. In ferit je tipičen material, keramika, ki zahteva zelo veliko dela in znanja. To niso enostavni materiali, saj je tudi njihova industrijska proizvodnja zahtevna stvar. Po osamosvojitvi smo bili v Sloveniji prvi, ki smo v obliki »know howa« izvozili tehnologijo, in sicer na Tajvan, šlo pa je za tehnologijo ene skupine teh materialov. In to uspešno. Vsaj iz zadnjih informacij sledi, da v tovarni delajo s polno paro in da si že želijo povečati proizvode zmogljivosti. Ker vse razvijamo sami, ni nobenih licenčnih omejitev in lahko z znanjem dejansko razpolagamo.

• *Kako pa je z objavami?*

Žnidaršič: Z referati sva med drugim nastopila na šesti svetovni konferenci v Tokiu, bila pa sva praktično na vseh keramičnih konferencah, ki so po Evropi, to je predvsem v Španiji in Nemčiji. Imava že več kot 25 objav s področja močnostnih feritov, tako v tujih strokovnih revijah kot v zbornikih znanstvenih konferenc.

• *Nekateri govorijo, da smo Slovenci za temeljne raziskave premajhni in da se moramo držati predvsem aplikativnih. To radi poudarjajo tudi v resornem ministrstvu, vendar je vprašanje, ali je tako ločevanje sploh smiselno.*

Drofenik: Osnova vsega so temeljne raziskave, tehnične aplikativne in praktično delo so pa njihova nadgradnja. Kdor ne pozna osnovnih pojmov in temeljnih raziskav, tudi drugega ne more delati. Če naj nekoliko karikiram, je to tako, kot pri tistemu, ki se v šoli noče učiti fizike, matematike in kemije, češ, saj tega ne bom nikoli potreboval. Šel bi v tovarno in se tam priučil. Toda tisti, v katerem so vse te stvari, lažje tehniško razmišlja. Saj ne vemo, kaj imamo v podzavesti, ampak naš način razmišljanja je potem dejansko drugačen. Jasno pa je, da se je tega zoprno učiti, saj je zoprno sploh hoditi v šolo. Taki potem govorijo, češ, kaj nam bodo citatni indeksi, nam tega ni treba. To je kvalifikacija, ki jo potem uporabljajo tudi drugje. Toda večina zanimivih in zelo uspešnih aplikacij se je porajala v temeljnih raziskavah in so bile objavljene v uglednih znanstvenih revijah. Ljudje nočejo polagati računov in se izogibajo vsakemu sistemu, ki lahko njihovo delo natančno meri.

Temeljna raziskava, tehnična raziskava... Kaj je sploh aplikativna, tehnično uporabna raziskava? V bistvu ni nič drugega kot temeljna raziskava, ki ima nekje možnost za aplikacijo.

Žnidaršič: Kako sploh razviješ ferit? Smernice dobiš iz aplikacije. Oni povedo, kakšen ferit bi radi, potem pa se vrneš in lahko rečeš aplikacijski ali temeljni razvoj. Razviti moram tak material in navsezadnje je vseeno, kako to imenujem - razviti ga moram in potem spraviti na trg.

• *Kaj je čista temeljna raziskava, je pravzaprav zelo težko reči, razen morda v fiziki osnovnih delcev. Pa še tam prej ali slej pride do take ali drugačne praktično uporabnost.*

Drofenik: Govorili smo o definiranju. To se natančno vidi, čeprav človek svojega znanstvenoraziskovalnega dela le ne more v celoti meriti z vatlom ponudbe in povpraševanja. Kot imate recimo neki material in potem trg pove, ali se zanj zanima ali ne, ima raziskovalec ali razvojnik svoje delo - revije mu ga objavijo ali pa ne, ljudje se zanj zanimajo ali pa ne. Te stvari so torej merljive, toda ljudje ne marajo objektivnih ocen.

• *Kako pa je kaj z uporabo računalnikov? Ali vam Internet pri zbiranju informacij kaj koristi?*

Žnidaršič: Kot rečeno, je teh informacij izredno malo. Kar se pojavlja, je že zastarelo, kljub temu pa jih uporabljamo. V teh prispevkih včasih kljub temu najdeš rdečo nit ali kakšno zrno, ki ga potem po svojih izkušnjah nadgrajuješ.

Drofenik: Največ uporabnih informacij dobiš od kolegov, ki delajo na podobnih področjih, in imajo projekte s tovarnami v Združenih državah. Vprašamo jih, kaj zanje delajo, pa nam to vsaj v poglavitnih obrisih povedo, rezultati pa bodo objavljeni šele čez leto ali dve, čez tri ali morda celo čez štiri leta.

Žnidaršič: Glavni vir so konference in osebni stiki z ljudmi, ki jih poznava in ki delajo na določenih področjih. Tam morebiti dobiš določene stvari, vsaj kar se tiče razvojnih trendov, vsaj to, kam se razviti svet obrača, kam gre. V tujino seveda ne hodiva le pasivno ampak tudi aktivno, z referati. Sicer pa bi direktor težko dovolil hoditi tja samo tako, poslušat tuje referate, ampak je treba imeti s seboj kaj svojega.

Tomaž Švagelj
"DELO", sreda, 3.1.1996
rubrika "ZNANOST"

Dr. Radomir Kužel - IN MEMORIAM

Professor Radomir Kužel Ph.D., D.Sc., died on September 8, 1995. He is mourned by family, friends, and his colleagues in the Czech Republic and other countries. His very productive life was interrupted by an insidious disease in its prime, in the middle of his creative work.

Radomir Kužel was born in Prague, Czechoslovakia, on May 18,1931. Since graduating at the Faculty of Mathematics and Physics of the Charles University, Prague, in 1954, he has been working at the same faculty.

He worked at first as an assistant, later as an Assistant Professor and an Associate Professor at the Department of Solid State Physics for fifteen years. All the time he was interested in semiconductor physics. His research work spanned a wide range of problems including transport and surface phenomena, photoconductivity, photochemical reactions, surface phenomena and various semiconductor structures. Solid state transport properties were his favourite domain. He read introductory lectures on semiconductor physics, and special lectures on transport phenomena, physics of surfaces and measurement methods.

He spent two years (1968-1970) at the University of Alberta, Canada, where he developed his studies on polycrystalline cuprous oxide established in Prague. In cooperation with Professor F. L. Weichman he produced a series of experimental and theoretical publications on electrical, galvanomagnetic and surface phenomena in cuprous oxide single crystals.

Returning to Prague he extended his interest on II-IV semiconducting compounds newly introduced in the Department of Semiconductors. Since 1976 he has been the head of the Department of Semiconductor Physics at the Faculty of Mathematics and Physics of the Charles University, Prague. Finally, in 1989 he became Full Professor of Solid State Physics.

Since the beginning of 70s he developed broad cooperation with industry from which arose a new research dealing with heterogeneous systems and thick films based on various matrices and conductive components for hybrid microelectronics. Together with the team of his co-workers, he proposed and developed a new technology of preparation of resistive pastes for screen printing, and a technology of ceramic (enamel, glass) coated copper or steel substrate. Both have been protected by patents. The development of alumina substrates cladded with copper by means of enamels belongs also to his achievements. Last five years his attention was attracted to polymeric composites filled with carbon black or precious metals and oxides. He discovered new types of temperature sensors and voltage dependent systems.

Professor Kužel contributed to many international conferences on solid state physics, semiconductor physics and microelectronics. During last decades, he also devoted many efforts organizing some of them. He took part in arranging microelectronics conferences of ISHM-Europe as a member of Technical programme committee. He was one of the first foreign members of MIDEM bodies. For many years he participated in preparation of international MIDEM conferences.

Last years Professor Kužel spent a lot of time with his students. He was an author or co-author of several text books. Even if he transferred the focus of his activity in the last twenty years onto thick films and composites, the research on modern semiconductor physics in other groups of his department was subject of his intensive support. He had a great merit in providing up-to-date experimental instrumentation for research such as solar cells, or semiconductor defects characterization.

Professor Kužel contributed greatly to the development of his field of science and research at least in our country. His personal qualities and his outstanding example as a teacher, organizer and researcher will be greatly missed by his students, colleagues and friends.

Ivo Krivka

PREDSTAVLJAMO PODJETJE Z NASLOVNICE

terme čatež

OAZA TOPLIH VODA 365 DNI V LETU

Nazadnje se je "zgodil" Termopolis - pika na I čateške ponudbe. V programu po "receptu" za vsakogar nekaj bodo nastopali znani glasbeniki in pevci, organizirali bodo disko večere, plesne večere ob večno zelenih melodijah, modne revije, gledališke predstave, srečanja, delovala bo igralnica z okoli 30 igralnimi avtomati...

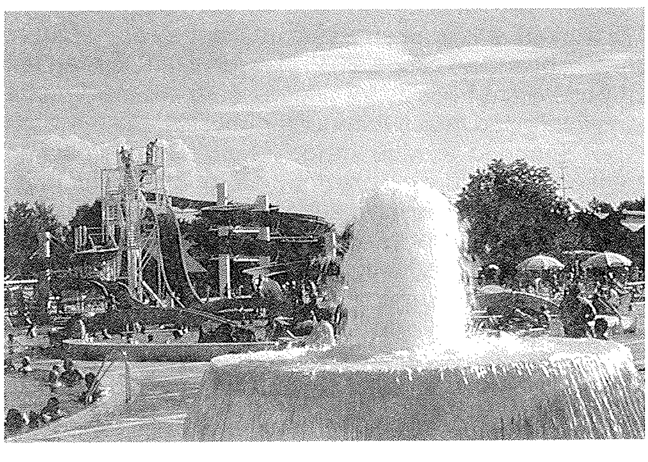
Pred Termopolisom "je bil" hotel Toplice. V središču čateškega zdravilišča, med zimsko in poletno termalno riviero, je na temeljih nekdanjega zrasel hotel za najzahtevnejše goste, ki predstavlja dejanski začetek stacionarne zdraviliške dejavnosti v Čateških toplicah...

Še pred hotelom Toplice in Termopolisom se je "odprl" bazen z valovi. V dveh mesecih in pol so obiskovalci dobili bazen površine 1250 kvadratnih metrov, v katerem posebna naprava ustvarja valove, visoke prek enega metra. Istočasno je bilo čateško zdravilišče "obogateno" še z restavracijo ob olimpijskem bazenu...

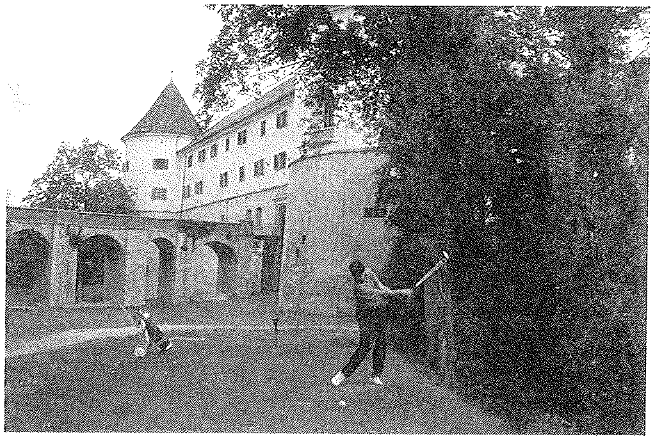
ZABAVA NA IN OB VODI:

Toda najprej je bil Čatež. Z naravnim bogastvom - vrelci, ki so jih odkrili že konec 18. stoletja in ki so zaradi svojih izrednih zdravilnih lastnosti kmalu postali znani po vsej Evropi. In z vsem, kar je zraslo do letošnjega, investicijsko plodnega leta: devet odprtih bazenov s tobogani in skupno površino več kot 9000 kvadratnih metrov; vodni slap, vodna goba, hitra reka, valovi, whirlpooli, umetno jezero... Različno veliki bazeni imajo tudi različne temperature vode, tam med 27 in 35 stopinj Celzija.

Še posebej pa je v tem času treba izpostaviti zimsko Termalno riviero s 1200 kvadratnimi metri vodnih površin. Zunanji bazeni namreč ostajajo brez obiskovalcev, v zaprte pa boste brez strahu pred prehladi spustili tudi svoje otroke. Njim seveda v Čatežu niti trenutek ne bo dolgčas, kajti "zaščitna znamka" čateških term niso le ogromne količine vode, temveč tudi prostori za igro, šport in rekreacijo. Skupaj z njimi boste lahko igrali tenis, odbojko, nogomet, kolesarili ali pa se razgibavali v fitness studiu. Lahko boste obiskali savne ali solarij, ali pa se morda podali do bližnjega gradu

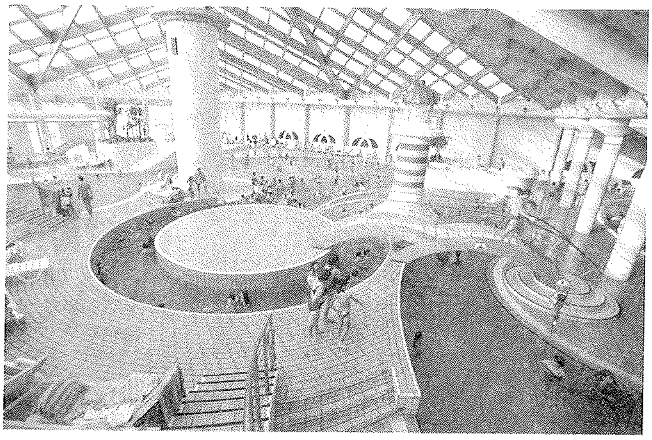


Mokrice, kjer Vas bodo pričakali jahalni konji in igrišče za golf z 18 luknjami. Če niti ne jahate niti ne igrate golfa, potem boste na Mokricah morda raziskali grajsko okolje s 16 hektarov velikim angleškim parkom in se sprehodili skozi nasade hrušk viljamovk (in na koncu tudi popili kozarček viljamovke, seveda).



OB VSAKEM ČASU ZA VSAKOGAR NEKAJ:

V Čatež lahko skočite za pol ali za cel dan, lahko ostanete tam za konec tedna ali pa pri njih preživite daljši dopust. Programi so narejeni za vse in za vsakogar - narejeni tako, da, je izključena samo ena stvar: ni se mogoče dolgočasiti. Kajti ob termalni vodi, restavracijah (ne pozabite na slaščičarno Urška in njen sladoled), trgovinicah, otroških igriščih itd. v zdravilišču niso pozabili na to, da so zdravilišče. Tako poskrbijo tudi za to, da si utrdite zdravje, morda shujšate, pozabite na to, da so v človeškem telesu živci; popravijo Vam zobe ali pa Vas "stanjšajo". Če želite, Vas odpeljejo ali pa Vam pokažejo pot do bližnjih izletniških točk, kjer Vas bo pričakala neokrnjena narava ter domača hrana in pijača.



Zakaj ni razlogov, da bi se ne odpravili v Čatež? Najprej zato, ker je čateška ponudba jesensko-zimska, in pomladansko poletna; ker je namenjena mladim in malo manj mladim, zdravim in tistim, ki jim zdravje kdaj pa kdaj ponagaja, tistim, ki si želijo aktivnega dopusta in vsem, ki želijo le nekaj dni počivati, in ker je čateška ponudba takšna, da zadovolji tudi tiste, ki se želijo predvsem zabavati.

Drugič pa ni razlogov za razmišljanje zato, ker boste samo v Čatežu lahko 365 dni v letu plavali in imeli skoraj tisoč možnosti za rekreacijo.

TERME ČATEŽ in GOLF HOTEL GRAD MOKRICE potencialni kraj organiziranih poslovnih in strokovnih srečanj:

Dodatna, zelo zanimiva ponudba Term Čatež z Golf hotelom **Grad Mokrice**, je možnost organizacije seminarjev in poslovnih srečanj.

V ta namen je na voljo več delovnih prostorov:

- v hotelu Terme
  (dve dvorani - vsaka za cca 35 udeležencev);
- v hotelu Zdraviliški dom
  (dvorana za cca 100 udeležencev).
- v Golf hotelu Grad Mokrice:
  - Viteška dvorana za max 40 oseb
  - Apartman za max 20 oseb
  - Dvorana štirje letni časi za max 100 oseb.

Udeležencem poslovnih srečanj lahko ponudimo namestitev v stilno opremljenih sobah in apartmajih v srednjeveškem gradu.

Udeležencem dvo ali večdnevnih srečanj na Mokricah bodo na Golf igiršču - vadbišču nudili brezplačno informativno uro golfa.

Informacije in rezervacije:
Terme Čatež d. d., Topliška c. 35,
68250 Brežice,
tel.: 0608 35 000,
telefax: 0608 62 721

KONFERENCE, POSVETOVANJA, SEMINARJI, POROČILA
CONFERENCES, COLLOQUYUMS, SEMINARS, REPORTS

Fourth Grove Fuel Cell Symposium

19. do 22. september, 1995, London

Udeležil sem se četrtega Grove-ovega simpozija o gorivnih celicah, ki je bil od 19. do 22. septembra na Commonwealth Institutu v Londonu. Simpozij, ki poteka vsako drugo leto, se imenuje po Sir William Grove-u, ki je prvo gorivno celico konstruiral in o njej poročal leta 1839, pred več kot 150 leti.

Gorivna celica je element, ki pretvarja kemijsko energijo goriva naravnost v električno energijo, namesto s pretvorbo preko toplotne energije v mehansko delo in naprej v električno energijo. Zato lahko doseže boljši izkoristek kot toplotnimi stroji, kjer je idealen oz. najvišji možen izkoristek omejen z razliko temperatur med toplotnim ponorom in temperaturo delovanja naprave. S tem je povezana tudi do 50% nižja emisija CO_2 na proizvedeno kWh kot pri, na primer, termoelektrarnah. Temperature delovanja vseh, tudi visokotemperaturnih celic, so prenizke, da bi nastajali dušikovi oksidi. Zato so gorivne celice ekološko sprejemljiv način proizvodnje električne energije.

Gorivna celica je sestavljena iz dveh elektrod, anode in katode, med katerima je elektrolit. Oksidant prihaja na katodo, reducent (gorivo) pa na anodo. Elektrolit, skozi katerega tečejo ioni, preprečuje mešanje goriva in oksidanta. Karakteristike pomembnejših tipov gorivnih celic, ki bodo omenjane v poročilu, so podane v tabeli I. Po sestavi elektrolita jih delimo na:

- alkalne gorivne celice (**AFC** - alkaline fuel cell)
- gorivne celice s trdnim protonskim prevodnikom v obliki polimerne membrane (**SPFC** - solid proton conductor fuel cell ali **PEMFC** - proton exchange membrane fuel cell)
- gorivne celice s fosforno kislino (**PAFC** - phosphoric acid fuel cell)
- gorivne celice s staljenimi karbonati (**MCFC** - molten carbonate fuel cell)
- gorivne celice s trdnim oksidnim elektrolitom (**SOFC** - solid oxide fuel cell).

Najbližje komercializacijo so danes PAFC - gorivne celice s foforno kislino, ki že obratujejo na nekaterih krajih v Združenih državah Amerike in na Japonskem. Na Japonskem že deluje elektrarna na naravni plin s kapaciteto 11 MW in izkoristkom okrog 40%. Gorivne celice s staljenimi karbonati (MCFC) so predvidene za večje, predvsem stacionarne aplikacije, na primer elektrarne, gorivne celice s polimerno membrano (SPFC) pa za manjše enote, recimo za pogon vozil. Po nekaterih optimističnih napovedih na konferenci ta dva tipa loči samo še nekaj let od komercializacije. Na Japonskem in v Združenih državah Amerike postavljajo pilotne elektrarne (MCFC) s kapaciteto do 2 MW, v Kanadi pa so predstavili avtobus z gorivnimi celicami s polimerno membrano. Gorivne celice s trdnim keramičnim elektrolitom imajo teoretično najboljše karakteristike, med ostalim najvišje izkoristke in možnost uporabe širokega spektra plinskih ali vplinjenih goriv, vendar so zaradi zahtevne konstrukcije, pogojene s keramičnimi materiali in visoko temperaturo delovanja, zaenkrat še najbolj daleč od komercializacije. Na Japonskem deluje postaja na osnovi SOFC s kapaciteto okrog 100 kW.

Gorivne celice z alkalnim elektrolitom (AFC) se ne razvijajo več za komercialne namene, ker so preveč občutljive na CO_2, ki je lahko prisoten tako v gorivu kot v zraku. Zato se mora uporabljati zelo čist vodik za gorivo in zelo čist zrak ali kisik za oksidant, kar (preveč) podraži uporabo. Seveda pa se uporabljajo v aplikacijah, kjer cena ni tako zelo pomembna, na primer na podmornicah ali vesoljskih plovilih. Kot zanimivost naj omenim, da je cena gorivnih celic za vesoljska plovila okrog miljon dolarjev za kWh.

Tabela I Karakteristike pomembnejših tipov gorivnih celic

	Nizkotemperaturne celice			Visokotemperaturne celice	
	AFC	SPFC	PAFC	MCFC	SOFC
Elektrolit	voda + KOH	polimer	H_3PO_4	$(K,Li)CO_3$	ZrO_2
Anoda	porozen Ni	grafit + Pt	grafit + Pt	porozen Ni	Ni + ZrO_2
Katoda	porozen Ni	grafit + Pt	grafit + Pt	NiO + Li_2O	(La,Sr) MnO_3
Temperatura	100°C	100°C	200°C	650°C	1000°C
Gorivo	čist H_2	čist H_2	H_2 (brez CO)	H_2 + CO + naravni plin	H_2 + CO + naravni plin

Na simpoziju je bilo registriranih preko 250 udeležencev iz 21 držav. "Govorjeni" referati so imeli okrog pol ure časa za predstavitev in nato četrt ure za diskusijo, na koncu vsake sekcije pa je bilo na voljo še okrog pol ure za bolj splošno diskusijo. Glavne teme so bile gorivne celice v transportu in energetiki, predvsem s stališča ekonomike in okolju prijazne energije. Bolj tehnični prispevki so bili predstavljeni kot posterji, teh je bilo 72.

V poročilu bom na kratko opisal vsebino nekaterih zanimivejših prispevkov, na razpolago pa je zbornik razširjenih povzetkov. Recenzirani prispevki bodo izšli v reviji Journal of Power Sources, obljubili so, da čez dobrega pol leta.

Najprej bom omenil moje vtise o razlogih za vlaganja v razvoj gorivnih celic v Evropi, na Japonskem in v Združenih državah Amerike. Vsi tipi gorivnih celic zaenkrat proizvajajo električno energijo, ki je dražja, pri, na primer SOFC, nekajkrat dražja kot elektrika iz "običajnih" elektrarn. Tudi vozila na gorivne celice, zaenkrat so izdelali samo nekaj prototipov, predvsem avtobusov, so precej dražja. V Združenih državah Amerike je najbolj pomembno "gonilo" skrb za okolje, kar najbolj pride do izraza v Kaliforniji. V prenaseljeni Evropi je razlog decentralizacija proizvodnje električne energije, ker zmanjkuje lokacij, kjer bi lahko (brez pretiranih protestov prebivalcev) postavljali velike centralne, termične ali nuklearne, elektrarne. Na Japonskem, kjer uvažajo preko 95% goriv, pa je poglaviten razlog dober izkoristek pretvorbe kemične v električno energijo, ne glede na začetno ceno same elektrarne. Zato načrtujejo velike centrale z močjo do 200 MW. Moram pa še enkrat poudariti, da so omenjeni razlogi samo moj vtis in da tega v predstavitvah ni noben eksplicitno povedal.

Na začetku simpozija so podelili priznanje za življenjsko delo (Sir William Grove Memorial Medal) B. Podolny-ju (Int. Fuel Cell Corp.). Podolny je bil v Združenih državah Amerike "gonilna sila" pri razvoju gorivnih celic za proizvajanje električne energije v vesoljskih plovilih in podmornicah. Sodeloval je pri razvoju gorivnih celic s fosforno kislino, ki jih je pripeljal do roba komercialne uspešnosti. V zahvalnem govoru je Podolny izrazil rahlo zagrenjenost, ker gorivne celice kljub dolgemu razvoju še niso komercialno uspešne. To je pripisal premajhnim vlaganjem in primerjal s situacijo na področju nuklearne energije po drugi svetovni vojni, ko so velika vlaganja razmeroma v kratkem času pripeljala do jedrskih elektrarn.

W. P. Tegan je v uvodnem referatu, s katerim se je začel simozij (Fuel cell commercialization - the key issues), povedal, da so najbliže komercializaciji PAFC gorivne celice, za ostale tipe pa pričakujejo, da bodo postali konkurenčni ostalim virom električne energije v kakih desetih letih. Govoril je o začaranem krogu, ki so ga omenili tudi mnogi drugi referenti; dokler se gorivne celice, ne glede na tip, ne bodo serijsko izdelovale, bodo predrage. Dokler bodo predrage, pa jih možni uporabniki ne bodo kupovali, zato ne more priti do serijske proizvodnje. P. B. Bos (Commercializing fuel cells-managing risks) je to imenoval "Catch-22" situacija. Možna strategija je nekaj, kar bi lahko imenovali metodo palice in korenčka. Zaostreni pogoji za varovanje okolja bodo prisilili uporabnike, predvsem v transportu, k uporabi čistejših vozil, predvsem v Kaliforniji, kjer pripravljajo zakon o Zero Emission Vehicle (ZEV). To - palica oz. prisila - bo pripeljalo do večjih serij gorivnih celic, sledilo bo znižanje cene na sprejemljivo raven, izdelovalec celic pa bo imel dobiček (korenček); to pričakujejo čez kakih 10 let.

M. Nurdin je v svojem prispevku (An assessment of strategic approaches to the commercialisation of fuel cells) povedal, da Japonska daleč vodi pri vlaganju v razvoj gorivnih celic. Razvoj je financiran 100%, postavljanje demonstracijskih postaj pa 50%. Japonski cilji so 200 MW moči po letu 2000 (tehnologija PAFC) in 2200 MW po letu 2010, od tega predvidoma 10% PAFC in 90% MCFC. Zdužene države Amerike vodijo pri raziskavah in razvoju, vendar imajo instaliranih samo okrog 4,5 MW. Firma International Fuel Cells, katere predsednik je bil do upokojitve leta 1992 Bill Podolny, letošnji dobitnik Grove-ove nagrade, je razvila in prodaja 200 kW postaje PC25 (tehnologija PAFC). Trenutno je instaliranih 56 teh postaj. Njihova cena je v zadnjih dveh letih padla na polovico in sedaj stanejo 3000 $ za kW, upajo pa, da bo do leta 1998 cena samo še 1500 $ za kW. Pri tej ceni bodo konkurenčne ostalim virom in subvencije ne bodo več potrebne.

P. Patil (The new generation of vehicles-market opportunity for fuel cells) in ostali, ki so govorili o možnostih transporta z gorivnimi celicami, so predvsem poudarjali dobre izkoristke in zelo nizke emisije okolju škodljivih snovi. Za osebne avtomobile se zaenkrat kažeta najbolj prespektivni gorivna celica s protonsko membrano (nizka temperatura delovanja) in SOFC (visoki izkoristki in možnost uporabe različnih goriv), vendar nobena od teh tehnologij še ni zrela. Osnovni problem pri komercializaciji osebnih vozil na gorivne celice bi se lahko, seveda zelo poenostavljeno, predstavil takole: "navaden" avto rabi, da se pelje, gorivo in motor; avto na gorivne celice rabi prav tako gorivo in motor, poleg tega pa še za nekaj tisoč dolarjev (danes kar nekaj deset tisoč dolarjev) vredne gorivne celice. Zato bo težko ceno avtomobilov znižati na konkurenčno raven. Ocenjujejo, da bo leta 2030 okrog 8% osebnih avtomobilov na gorivne celice. Pri osebnih avtomobilih je dodaten problem tudi distribucija goriva; gorivo, na primer metanol, mora biti dostopno na mreži črpalk tako kot sedaj bencin, da bi bili uporabniki pripravljeni zamenjati "navadne" avtomobile za take z gorivnimi celicami. Drugačna je situacija pri avtobusih in tovornjakih, kjer nekateri obetajo komercializacijo prej kot v desetih letih. Danes že vozijo demonstracijski avtobusi (Ballard Power Systems Inc., Kanada) z gorivnimi celicami s polimernim elektrolitom (moč 205 kW), ki kot gorivo uporabljajo vodik. Pričakujejo, da bo do leta 1998 tak avtobus sicer stal še vedno dvakrat več kot dizel, vendar bo zaradi boljšega izkoristka cenejši pri uporabi.

V nadaljevanju poročila bom opisal predvsem prispevke, ki se ukvarjajo z "našim" področjem, to so gorivne celice s trdnim oksidnim elektrolitom (SOFC) in materiali zanje. Kot smo že omenili, visokotemperaturne gorivne celice s trdnim oksidnim elektrolitom delujejo pri temperaturah do 1000°C. Trdni oksidni elektrolit je v večini primerov ZrO_2 keramika, ki je dober ionski prevodnik. Na strani katode kisik sprejme elektrone in kot ion potuje skozi gosto ZrO_2 keramiko. Kisikovi ioni elektrone oddajo na strani anode in reagirajo z gorivom, ki je lahko vodik, mešanica vodika in ogljikovega monoksida ali pa ogljikovodiki. Visoka temperatura delovanja namreč omogoča "notranji reforming", to je reakcijo med vodno paro in ogljikovodiki, tako da dobimo vodik in CO v sami celici. Nekateri avtorji obetajo celo izkoristke (kombinirana proizvodnja električne in toplot-ne energije) do 80 %.

B. Barp (Natural gas fuel cells for residental applications) je predstavil švicarsko firmo Sulzer Innotec, ki razvija majhne SOFC postaje za "domačo" uporabo. Kot gorivo bodo uporabljale naravni plin, do temperature delovanja pa jih bo ogrel vgrajen plinski gorilnik. Prototipi z močjo 1 kW so že testirani v laboratoriju, leta 1997 bodo začeli s proizvodnjo in pričakujejo, da bodo do leta 2002 že komercialni, kar pomeni ceno 1000 do 1500 $ za kW. Dimenzija posameznih modulov bo 1,6x0,8 m^2, moč modula pa 7-15 kW. Firma SOFCo (Salt Lake City, Združene države Amerike) razvija10 kW SOFC mobilno postajo za vojaške namene. Dva prispevka angleških avtorjev sta predstavila razvoj SOFC s cevastimi elementi, pri čemer so cevi oziroma cevke zelo tanke s premerom 3 mm, kar omogoča zelo hitro segrevanje oziroma ohlajanje celice. Za elektrode uporabljajo "tradicionalne" materiale, to je manganit za katodo in kovinski nikel v YSZ matrici za anodo. M. Mogensen (Riso Natl. Lab., Roskilde, Danska) je poročal o karakterizaciji SOFC katod, ki so narejene iz zmesi perovskitov in YSZ. Perovskiti so dobri elektronski prevodniki, YSZ pa kot ionski prevodnik zmanjša polarizacijske izgube in se dobro veže na YSZ trdni elektrolit. Cassidy (Napier University, Edinburgh, Anglija) je poročal o razvoju strukture SOFC, kjer ni več nosilec razmeroma debel elektrolit (200-250 μm), ampak se, zaradi zmanjšanja ohmskih upornosti, nanese tanka plast elektrolita (10-20 μm) na debelo nosilno anodo iz zmesi nikla in YSZ.

A. Akinaga in koavtorji pa so poročali o razvoju cevastih SOFC elementov, kjer je nosilec razmeroma debela cev poroznega latodnega materiala na osnovi $LaMnO_3$, nanjo pa je s pomakanjem v suspenzijo nanešen in sintran tanek film YSZ. Tu omenimo, da tudi pri firmi Siemens skušajo zamenjati nosilno cev iz poroznega cirkon oksida s cevjo iz katodnega materiala. A. Swan in sodelavci so študirali vpliv različnih atmosfer na strani SOFC anode (vodik, metan, vodik in vodna para) na karakteristike in mikrostrukturo Ni/YSZ anodne plasti. T. Yamamoto in sodelavci so preiskovali možne reakcije med anodnim materialom na osnovi Ni/YSZ in različnimi kromiti, ki se uporabljajo za izdelavo vmesnika. Reakcije na stikih posameznih komponent SOFC lahko vodijo pri visokih temperaturah obratovanja do novih faz, ki poslabšajo izkoristek celice.

K. Wippermann in sodelavci (Forschungszentrum, Jülich, Nemčija) so dobili Cookson-ovo nagrado za najboljši poster na področju raziskav materialov. Naslov je bil "Catalysis of the electrochemical processes on SOFC cathodes", v prispevku pa so poročali o modifikacijah tako katodnega materiala kot YSZ elektrolita za zmanjšanje polarizacijskih izgub. Te izgube so sorazmerne z aktivacijsko energijo reakcije prehoda O_2 v O^{2-} pri prehodu kisika iz zraka v kristalno rešetko YSZ. Ugotovili so, da dopiranje perovskitov na osnovi manganitov s plemenitimi kovinami ali kobaltovim oksidom ali dopiranje YSZ z železovim oksidom zmanjša polarizacijske izgube. W. Winkler (Fachhochshule, Hamburg, Nemčija) je poročal o testiranju kovinskih materialov - visokotemperaturnih zlitin - za vmesnik, ki povezuje posamezne gorivne celice in ki ima pri njihovem designu tudi vlogo izmenjevalca toplote. Problemi, na katere so naleteli, so bili predvsem neujemanje temperaturnih razteznostnih koeficientov in slabo tesnenje.

Več avtorjev je predstavilo uporabo meritve kompleksnih impedanc kot metodo karakterizacije SOFC materialov ali komponent. Tu je bil zanimiv poster z naslovom "Characterisation and fault diagnosis in a SOFC by the method of electrochemical impedance spectroscopy" (F. Gobal, Sharif University, Iran), kjer so poročali o testiranju gorivne celice z elektrolitom na osnovi $BaCe_{0,9}La_{0,1}O_3$ (namesto YSZ) in anodo na osnovi $La_{0,4}Ce_{0,6}O_x$ (namesto Ni/YSZ). J. Palma in sodelavci (Instituto de Ceramica y Vidrio, Madrid, Španija) so preiskovali redukcijo kisika na stiku med $(La,Sr)MnO_3$ katodo in trdnim YSZ elektrolitom.

Kot poster je bil na simpoziju predstavljen tudi naš prispevek z naslovom "Some characteristics of $LaFeO_3$ based cathode materials for SOFC" (D. Kuščer, M. Hrovat, J. Holc, S. Bernik, D. Kolar). Poročali smo o vplivu dodatka kalcijevega ali aluminijevega oksida na električne in mikrostrukturne karakteristike $LaFeO_3$, ki je zanimiv kot alternativna katoda. Ima sicer višjo električno upornost kot $LaMnO_3$, vendar podatki iz literature nakazujejo, da ima nižje polarizacijske izgube.

Marko Hrovat
Institut "Jožef Stefan"
Jamova 39
61000 Ljubljana

PRODUCTRONICA 95

Productronica, to pot že enajsta po vrsti, je v času od 7. do 10. novembra 1995 v Münchnu praznovala svojo dvajsetletnico, kot največji mednarodni sejem za proizvodnjo v elektroniki. Nekaj številčnih podatkov o letošnjem sejmu: razstavna površina 140.000 m^2, 1583 razstavljalcev in 165 dodatno zastopanih firm iz 35 držav. Iz Slovenije je bil prijavljen samo DONIT, Medvode, vendar na sejmu ni razstavljal. Okoli 60.000 obiskovalcev je bilo iz 75 držav.

Strokovno je bil sejem razdeljen v pet sektorjev:

Sektor A, proizvodnja elementov mikroelektronike (18% razstavljalcev), prikazane vse tehnologije polprevodniške tehnike;

Sektor B, proizvodnja nosilcev vezij (20% razstavljalcev) s težiščem na proizvodnji tiskanih vezij in površinski montaži; močan poudarek je bil na ekološko prijaznih postopkih;

Sektor C, proizvodnja podsklopov in sistemov (2% razstavljalcev), kjer so bile na tem najmočnejšem razstavnem področju Productronike prikazane vse tehnike gradnje in spajanja elektronskih naprav s poudarkom na avtomatizaciji;

Sektor D, merilne in preizkusne naprave (21% razstavljalcev), ki sledijo zahtevam po visokih kakovostnih standardih v proizvodnji elektronike; tudi tu narašča ponudba avtomatiziranih merilnih sistemov v skladu s splošno tendenco avtomatizacije v proizvodnji;

Sektor E, sredstva za proizvodnjo in storitve (12% razstavljalcev), porazdeljen po skoraj vseh halah in je nudil pregled nad polizdelki, kovinskimi in nekovinskimi materiali, pa tudi proizvodno informacijskimi sistemi.

Sejem so spremljale tudi druge strokovne dejavnosti, simpoziji in mednarodni FORUM o ekonomskih kriterijih in pomenu izbora najprimernejše makro lokacije za proizvodnjo elektronskih naprav in elementov: tu so imeli referate in so predstavili svoje strategije vodilni predstavniki Siemensa, Matsushite, McKinseya, Hewlett-Packarda,LTX Corporation in Temic-a.

V program sejma so spadali tudi trije vrhunski simpoziji oziroma konference, organizirani v tesnem sodelovanju z industrijo, in sicer:

- tridnevna konferenca Inovativna proizvodnja elektronskih sistemov, s temami MID - Molded Interconnect Devices, Tehnologije spajanja v proizvodnji elektronike in In-line zagotavljanje kakovosti;
- enodnevni simpozij Tehnologije mikrosistemov o njihovem sedanjem stanju, perspektivi, proizvodnji tehnologiji in napravah za proizvodnjo;
- enodnevna konferenca o napravah in materialih za proizvodnjo polprevodnikov iz 300 mm rezin ter "single wafer" procesiranje.

Zborniki za vse tri konference so na razpolago v uredništvu revije Informacije MIDEM.

Letošnja Productronica je utripala v znamenju booma na področju elektronike, ki ga po recesiji v času zadnje Productronice ni skoraj nihče pričakoval. Razvoj pri elektronskih izdelkih se kaže v parametrih: manjši, hitrejši, učinkovitejši, cenovno ustreznejši, krajši time-to-market. Osrednje tehnološko težišče je napredujoča integracija in prilagajanje elektronskih sklopov vedno hitrejšim čipom. Sklaldno z napredkom in rastjo same elektronske industrije pa se je seveda povečala tehnološka ponudba in izdelava opreme za proizvodnjo, kar kažejo podatki iz nekaterih najvažnejših segmentov.

Pri napravah za izdelavo tiskanih vezij so novi postopki kot n.pr. Fine pitch tehnika, BGAs (Ball Grid Arrays), Chip on Board in multičip moduli spremenili plošče tiskanega vezja. Zaradi zmanjšanih dimenzij lukenj je prišlo do uporabe laserskega vrtanja ali jedkanje mikrovrtin s plazmo. Stare kemične bakrove kopeli se opuščajo in nadomeščajo z Directplate postopkom, ki omogoča neposredno povezavo s sledečim fotopostopkom in galvansko ojačanje plasti. Zelo interesantna nova tehnika je Dycostrate postopek, ki dela s poliimidnimi nosilci in ne zahteva več mehanskega vrtanja; omogoča strukture do 50 μm in luknje do 80 μm, ki jih "štancajo" z reaktivnim ionskim jedkanjem.

Izredna zasedenost proizvajalcev integriranih vezij z naročili in rast tržišča (cca 70% v dveh letih 1994/95) je na eni strani povzročila skoraj prezaposlenost industrije polprevodniške opreme, na drugi pa so prišli do polnega izraza trije zgodovinski trendi v proizvodnji integriranih vezij: manjše dimenzije, večje rezine in povečana uporaba single wafer procesiranja. Evropski program "Joint European Submicron Silicon - JESSI" se je pri tem pokazal kot popoln uspeh, vendar bo za prihajajoče rezine 300 mm potrebna spet nova oprema.

Uporaba opreme za proizvodnjo polprevodnikov se ni razširila samo na področje prikazalnikov in na solarno tehniko, temveč tudi na še eno izredno zanimivo področje - mikrosistemsko tehniko. Tu pride do izraza integracija in kombinacija mikromehanike, mikroelektronike, mikrofluidike in mikrooptike z uporabo novih tehnologij. Mikrosistemska tehnika je dejansko novi val visoke tehnologije in kaže preko fizike nanotehnologije, supramolekularne kemije in kvantne elektronike nova pota do bodoče superminiaturizacije. Mikrosistemi združujejo senzorske in aktuatorske funkcije kot tudi analogna in digitalna integrirana vezja. Imajo mnoge prednosti in možnosti pred konvencionalnimi sistemskimi rešitvami, ker so manjših dimenzij, cenejši in zanesljivejši, obenem pa omogočajo nove funkcije in rešitve. Najbolj znan mikrosistem je danes Airbag senzor v avtomobilih ki s svojim hitrim prodorom na trg napoveduje tudi prodor uveljavljanja te nove tehnologije. Posebno napredne rešitve glede kompleksnosti, miniaturizacije in optimalne izpolnitve zahtev nudi ravno silicijeva tehnologija, vendar bo potrebno še mnogo tehnoloških naporov, mnogo raziskav in razvoja za osvojitev specifičnih mikroproizvodnih tehnik.

Kot kaže gornji kratki opis tehnoloških tendenc v posameznih segmentih elektronike, nudi Productronica poleg Electronice v Münchnu izredno dobre možnosti strokovnjakom za oceno najnovejšega stanja in tende razvoja tehnike v svetu. Zato ni čudno, da je bilo videti na sejmu kar precejšnje število obiskovalcev iz Slovenije, vendar večinoma v individualni organizaciji. Morda bi v društvu MIDEM veljalo razmisliti o zopetnem organiziranju skupinskega potovanja v sejemski München, kot smo ga že izvajali pred leti.

Milan Slokan

VESTI - NEWS

First Announcement

International Conference on

New Opportunities for Research at Third Generation Light Sources

Lipica, SLOVENIA, May 25-29, 1996

Financially supported by
the Slovenian Ministry of Science and Technology

Under the auspices of EPS, Jupak, UNESCO, IAEA and CEI

The Conference

The conference is aimed at people, who are interested in research with synchrotron radiation at third generation sources, like the ESRF and ELETTRA. Therefore, the focus is on methods which are newly opened up or enhanced by the advent of high brilliance sources. Invited experts from a broad range of research fields will present the newest aspects from their particular field.

One of the goals of the conference is also to promote synchrotron radiation research in the central European countries and to help in establishing links between the research groups from these countries with experienced researchers at synchrotron radiation centres.

The participants of the conference will present their work with contributed papers. A poster session with the contributions will last over the entire conference so as to give ample time for discussions among the participants. A committee of experts will nominate awards for the best posters. The contributions will be published in a special issue of the Journal of Synchrotron Radiation subject to the usual refereeing procedure.

An industrial exhibition will be taking place during the conference. Companies are invited to inquire for detailed conditions.

Topics

Status of light sources and beamlines
Beamline design and instrumentation
X-ray absorption spectroscopy
Macromolecular and other high-res. diffraction
Small-angle scattering
Photoelectron spectroscopy
X-ray fluorescence spectroscopy
Real-time experiments
Microscopy and microbeam applications
Industrial applications of SR
Designs for new generation light sources

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D. Metelko and N. Novak Tušar, National Institute of Chemistry

Mailing address

Lipica Conference
c/o
Jožef Stefan Institute
Jamova 39
P.O.B. 100
61111 Ljubljana
Slovenia

Tel. + 386 61 177 34 53
Fax + 386 61 219 385

Electronic mail

Lipica@ijs.si

World Wide Web

http://www2.ijs.si/~denis/Lipica/

News from European Semiconductor, January 1996

Intel P6 is launched as Pentium Pro

Intel has developed a new processor that out-performs Digital's Alpha.

Intel has launched its latest processor, the Pentium Pro, previously called the P6. The new product is aimed at the workstation and server markets. With a SpecInt92 figure of 366 in its 200 MHz form, it out-performs Digital's Alpha chip.

This high effectiveness comes from Dynamic Execution microarchitecture. The Pentium Pro anticipates forthcoming instructions which greatly improves its CPU usage and scheduling.

The 5.5 million transistor 32 bit chip is built using the techniques pioneered for the Pentium. Fast versions (180 and 200 MHz) will be built on 0.35 micron geometry in the USA. Slower (150 and 166 MHz) versions will be built at Leixlip in Ireland with 0.6 micron technology.

Although there are many similarities between the Pentium Pro and the Pentium, the company has no plans to provide an upgrade path between the two. Apparently the architecture differences would make it barely worthwhile.

Intel intends to keep the Pentium as its home-PC product until at least 1997, when prices for the Pentium Pro are expected to fall significantly. A radical new processor product from Intel is not expected until at least the end of that year.

The Pentium Pro targets an area where Intel has not been strong, and may allow it to further dominate the processor market. Already many companies have announced high-end products incorporating the new chip. Significantly, these include Digital.

Intel has recorded a revenue of $4.17 billion for the third quarter ended 30th September 1995, a 46% increase compared to the same period 1994. For the first nine months of this year, revenue of $11.62 billion was up 40% from $8.29 billion for the same period last year.

MEDEA proposed to succeed JESSI

Horst Nasko, newly appointed JESSI chairman, indicated at Productronica that a proposal has been put forward to the European Commission and governments for a programme to follow JESSI after its termination at the end of 1996. The new research consortium would be called MEDEA - Microelectronics Development for European Applications.

It is anticipated that, much like JESSI, the European Commission as well as national governments will fund MEDEA. However, the new consortium intends to fund fewer, but bigger, projects if the overall funds remain the same. Government decisions are not expected until the middle of next year.

Erik Kamerbeek, Chairman of JESSI's Equipment and Materials Subprogram, announced that the direction which European E&M research has to focus on in 1996 is 300 mm wafer technology. He believes that an avid participation is essential for European companies. Unless equipment suppliers follow other countries immediately in their development work, they will not be able to get involved in new wafer fabs and offer 300 mm wafer compatible equipment when needed.

JESSI's Equipment and Materials side aims to carry out studies to assess the feasibility of 300 mm equipment projects. It will also try to involve the European industry in Sematech's 300 mm equipment evaluation initiative.

At Productronica, Horst Nasko took the opportunity to announce the winner of the JESSI Award 1995. It was given to the "Silicon Wafers for Submicron Technology" project. GRESSI, IBM, Philips, SGS-Thomson, Siemens, Temic Telefunken and Wacker Siltronic jointly cooperated in the project.

IBM plans to invest $1 billion in France

IBM has announced a $1 billion investment in its existing chipmaking facility in Essonnes, France. The investment will be made over the next three years to produce 64 Mb DRAMs, using 0.35 micron process technology. About 1000 jobs will be created over this period, increasing the number of employees to 3,000 by 1998.

In the first stage of the investment - late 1995, early 1996 - the necessary production area will be made available. To make space, IBM's existing bipolar line will be closed down. This closure also indicates IBM's intention to convert completely to CMOS technology.

Towards the end of 96, early 97, 16 Mb facilities will be installed, which will then be upgraded to 64 Mb approximately a year later, depending on when this capability is required in the industry There are currently no plans increase the 35,000 m^2 of cleanroom capacity.

A further $400 million investment in the company's Burlington facility (Vermont, USA) will add 0.35 and advanced 0.25 micron technology for manufacturing microprocessors, embedded controllers and other logic chips, including leading-edge multimedia devices. This investment will begin in 1996.

IMEC wins EC project

IMEC has been named as the first equipment assessment site for optical lithography, under the EC's Semiconductor Equipment Assessment (SEA) initiative, which was announced last year.

The research institute is leading a team of industrial users that will evaluate a Deep-LTV stepper from ASML (PAS 5500/300), aimed at future 0.25 micron CMOS processes. Some exploratory work on 0.18 micron CMOS will also be undertaken.

Industrial members of the team include Philips, Siemens; GPS, AT&T, National Semiconductor, Texas Instruments, AMD, TSMC (Taiwan) and Goldstar (Korea). Team members - ASML equipment users and non-users - are geographically distributed throughout the world in order to obtain the most efficient dissemination of the assessment results.

The total budget for this project is in excess of 6 million ECUs ($8 million), funded by the EC and the programme partners.

Siemens opening in Dresden

On 10th November, sixteen months after construction work began, chip production commenced at Siemens Microelectronics Center in Dresden. So far, about $800 million has been invested, with a further investment of $1.9 billion to be made by the year 2004.

Currently, the number of employees amounts to 950. By autumn 1996, however, the workforce will total 1,450.

As a first step, memory chips of the 16 Mb generation are being produced. Production technologies range from 0.5 to 0.3 micron pattern width. A second ultra-clean cleanroom of the same size will come into service early next year. Mass production is expected to start in summer 1996. Later on, Siemens also plans to produce logic chips.

Intel fab in Israel

Intel has announced a flash memory wafer fab in Kiryat Gat, Israel. The facility, Fab 18, will cover approximately 93,000 m^2 of floor space, with 7,400 m^2 of Class 1 cleanroom. It will manufacture high integration Smart Voltage flash memory products and future high density flash memory products.

The plant is scheduled for completion in 1998 and is projected to cost $1.6 billion.

Four-way alliance

Motorola researchers are expected to join IBM, Siemens and Toshiba development teams at IBM's Advanced Semiconductor Research and Development Center in East Fishkill, New York.

Siemens and Motorola have also signed a memorandum of understanding to build a joint facility in the US to produce DRAMs. A location has not been finalised yet.

300 mm collaboration

Applied Materials has signed an agreement with SGS-Thomson (ST) to immediately begin cooperative work in Crolles (France) and Agrate (Italy) on a variety of 300 mm wafer manufacturing technologies that will be used by SGS-Thomson. No specified timetable for equipment purchases has been agreed, but the agreement involves a plan for the development of many specific processes.

Existing development work by ST with process equipment suppliers, mostly carried out within the JESSI programme, includes 200 and 300 mm wafer sizes. The new agreement will complement this work, since Applied Materials' range of process technologies and its commitment to rapid 300 mm development will help ST to move very quickly through the evaluation and early manufacturing steps for 300 mm wafers.

SGS-Thomson is also known to be working with Varian on the ion implantation of 300 mm wafers.

Virtual digital signal processor for video

Pilkington Microelectronics (DSP) Ltd is busy developing a high performance digital signal processor technology targeted at video applications. Their proposed device is a reconfigurable and scalable multiprocessor called the Virtual DSP. It is likely to be fabricated in a 0.5 μm triple-layer metal CMOS process.

The Virtual DSP combines thirty-two 8-bit reconfigurable DSP cores, an MCU, a DMA engine, cache sequencer, and memory into a single device (figure 1). Each core contains a multiplier, ALU, registers, memory and the other logic necessary to implement common DSP functions. Cores can be cascaded to form much larger structures in 8-bit slices creating 8, 16, 24, 32, 40, 48, 56 and 64bit multipliers, adders, or other functions.

The smaller devices are aimed at cost-sensitive applications, such as set-top boxes where only decompression is required; a 32-bit core Virtual DSP is capable of performing real-time MPEG1 video compression and decompression on a die of 13 mm on a side.

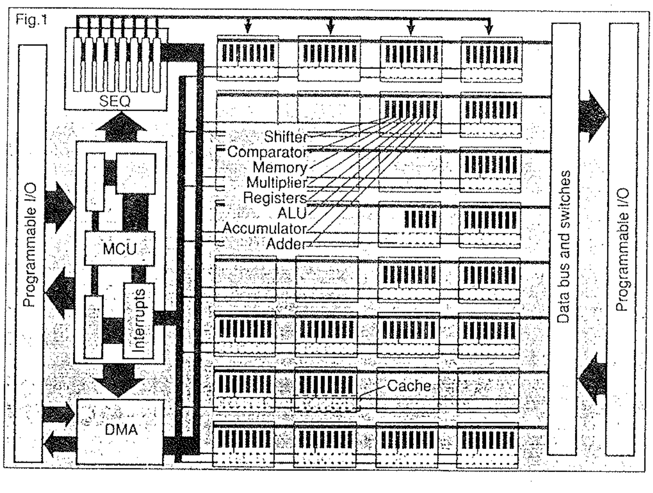

Fig. 1: Internal architecture of the PMe(DSP)L's proposed Virtual DSP

Cache and microcontroller

The caches configure the underlying architecture of each core, allowing any core to be configured to directly implement a complex function, rather than the conventional approach of implementing complex functions as a series of simple instructions. This approach enables a significant performance advantage over a conventional DSP. Functions can be performed in single or multiple cores. A 32 core array can perform an 8 x 8 discrete cosine transform in 320ns.

Each cache can hold four configurations. A programmable sequencer is utilised to select which cache is active at a particular instant. Switching to a new cache configuration takes 5ns. Configurations are loaded into each cache by the DMA engine. When a configuration has been utilised the DMA engine updates non-active cache locations with new configuration data.

The microcontroller directs the flow of configuration data through the DMA engine and supervises cache selection via the sequencer. In addition, each core has an associated timer and interrupt logic that links directly to the microcontroller. The microcontroller program responds to interrupts to issue new instructions to the sequencer or DMA engine. A higher speed control link is also provided enabling any core to directly control the selection of active cache addresses.

Virtualising

The hardware can be "virtualised" to dynamically implement new functions, such as a discrete cosine transform (DCT) or Huffman coder by continuously switching active caches and updating caches with new configuration data.

Video compression techniques are continually evolving. The Virtual DSP's reconfigurable architecture enables designers to implement new standards without the need for custom silicon.

The device can read algorithms and architecture descriptions from video storage media - particularly important for the games market where decompression has to be achieved along with the generation of complex graphics.

Design tools

The Virtual DSP device family will be supported by a suite of software tools being developed in parallel with the device. This interactive development environment (IDE) will provide a variety of design entry methods: from behavioural C or VHDL, to Verilog, and schematic entry (EDIF), through to assembler.

The software tools will take the algorithm description, perform scheduling (ie, the automatic dynamic allocation of resources) and do the necessary placement and routing to implement the design on the chosen target. The compiled set of configuration files can then be down-loaded onto the device.

The entire system can be simulated within the IDE with full access to internal states for single-stepping or debug, or on third party tools.

DIGITAL ICs - FOCUS ON PLDs/FPGAs

Flash-Based CPLDs Run Fast, Need Just 5 V

Based on a 5-V reprogrammable flash-storage technology, the XC9500 series of complex programmable logic devices provides designers with from 800 to 12,800 usable gates. The high-performance family delivers pin-to-pin delays of just 5 ns, allowing it to compete with the highest-speed grades of other CPLD families. Also referred to as the FastFlash series, the CPLDs developed by Xilinx operate from a single 5-V supply, yet offer the ability to interface with 3.3-V signals. The chips also allow in-system reprogrammability as well as over 10,000 reconfiguration cycles-a level several orders of magnitude higher than most other flash-based CPLDs.

Fabricated with a 0.6-μm dual-metal CMOS process, the programmable chips were developed in conjunction with Seiko-Epson Ltd., Fujimi, Japan. The non-volatile storage cell employed in the FastFlash circuits consists of a dual-transistor structure that uses high-speed logic transistors, with one optimized for reading and the other optimized for writes. Both the select and the control transistors can be driven separately, permitting better control and higher performance.

In addition, the cell includes built-in erase Vt control, thanks to the second transistor, which helps improve device endurance. Although not as small as the single-transistor flash cell used by others, the cell is only about one third the size of the full four-transistor EEPROM cell.

The small area allows many routing switches to be fabricated in the critical regions of the chips and also reduces parasitic capacitances, which, in turn, improves chip performance. Furthermore, with more routing switches available, pin signals can be locked, even if the internal logic has to be modified. With most other CPLDs, logic changes often force the pinout to change due to limited internal routing options.

The abundant routing resources allow the configuration software to provide 100% interconnection of all pins and function blocks.

One unique functional capability is the availability of user-programmable ground pins-this ability allow the user to strategically position groundpins on the chip to lower ground inductance and reduce ground noise.

All the chips in the XC9500 family have a similar architecture-an array of function blocks that surround the FastConnect wiring matrix, which also connects the blocks to the configurable I/O cells. Each chip also has an enhanced JTAG controller that can be used for determining device type, chip programming and diagnostics. Active power is approximately 0.01-mA/MHz/-macrocell in typical applications.

In each function block is a 36-input AND array, which feeds a product-term allocator, which, in turn, feeds 18 macrocells. The macrocells can feed their outputs either to the I/O cells, or back to the interconnect matrix. A flexible product-term allocation architecture in the macrocells allows any macrocell to increase its logic capacity without affecting adjacent macrocells, permitting logic capabilities to "stretch" to handle requirements that don't neatly fit into one cell.

Initially there will be nine members in the family, with the first part to be sampled, the XC95108, packing 108 macrocells (about 2400 usable gates) and offering 7.5-ns pin-to-pin delays. The chip, which is now being sampled, will offer up to 108 user I/O's and come in either an 84-lead PLCC or 100- or 160-lead PQFPs. Following next quarter will be smaller versions-the 800-gate XC9536 and the 4800-gate XC95216, which will have delays of 5- and 10-ns, respectively The rest of the family will be released throughout 1996.

The XC9500 series is supported by the company's XACTstep version 6.0 for EPLDs. Enhancements to the tools include automatic device selection, a design manager and flow engine to simplify design capture and subsequent configuration, and a timing driven multichip partitioning module that keeps critical paths on the same chip. Also available is a static timing analyzer and an on-line help capability with "expert" assistance.

The software upgrade is free to users on maintenance contracts; for new users the full package sells for $995.

Samples of the XC95108 are immediately available and sell for $49.50 each in 100-unit lots (for the 100-lead PQFP version). For the latest information, access the company's Web site at http://www.xilinx.com.

Xilinx Inc., 2100 Logic Dr.,
San Jose, CA 95124;
Nick Kucharewski, (408) 559-7778.

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izvirni znanstveni članki, predhodna sporočila, pregledni članki, razprave z znanstvenih in strokovnih posvetovanj in strokovni članki.

Članki bodo recenzirani.

Časopis objavlja tudi novice iz stroke, vesti iz delovnih organizacij, inštitutov in fakultet, obvestila o akcijah društva MIDEM in njegovih članov ter druge relevantne prispevke.

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