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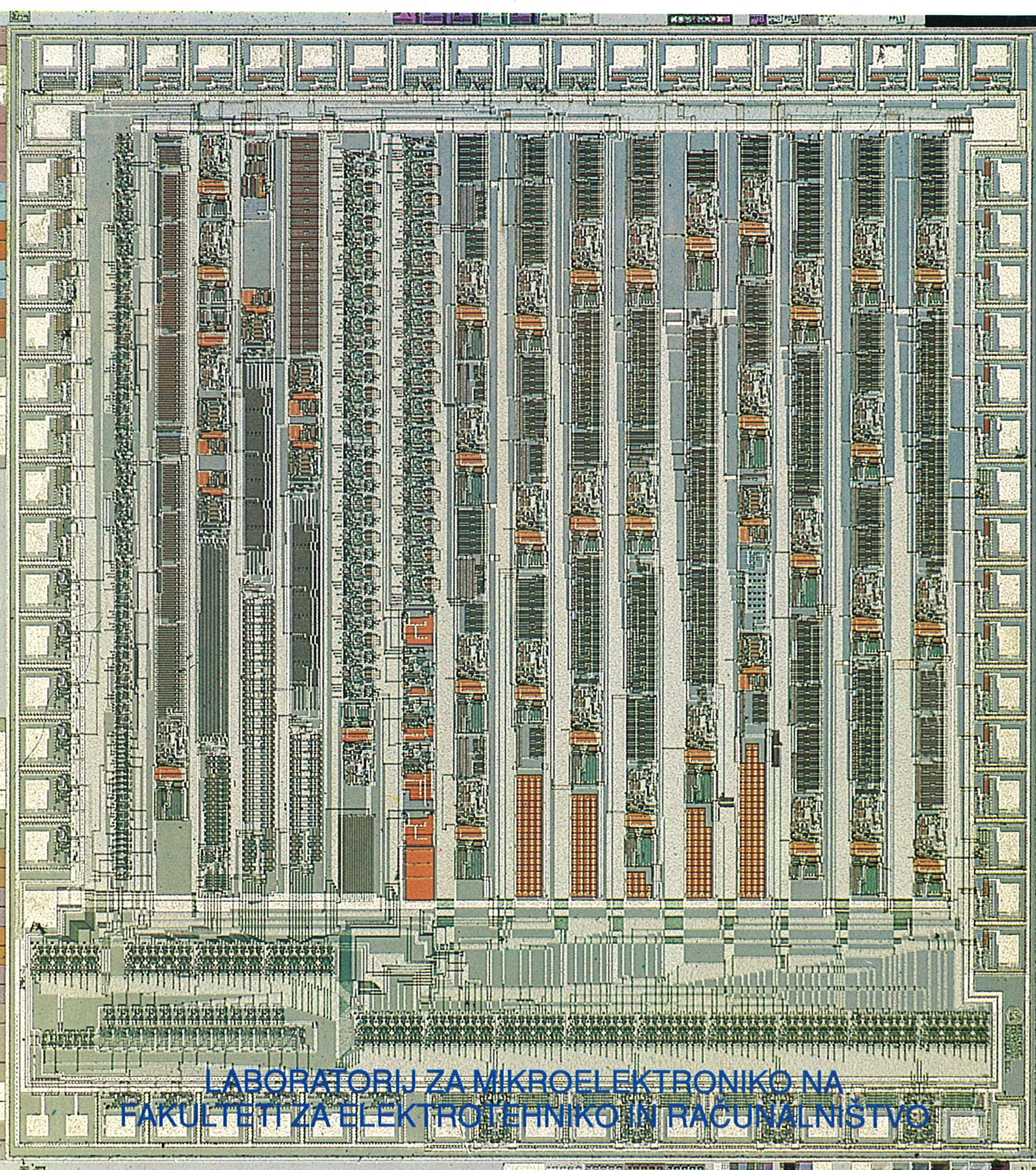

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VSEBINA CONTENT

RESTRICTIVE CRITERIA OR REDUCTION OF STATE MEANS FOR DEVELOPMENT

On the 7th of May, 1993 a final resolution regarding financing of science research projects, put up for competition in July of the last year, was adopted by the Slovene Ministry of Science and Technology after its thorough review, selection and coordination.

In the field of electronic components and technology 10 projects will be financed, 7 of which are granted their financing during all three years, one of them for two years and two for one year. These latter will have to demonstrate certain results during the first year in order to be able to benefit of the integral financing.

Such a resolution was proposed to the Ministry to be signed on the basis of principle criteria checked by Coordination Councils that have also prepared the project motion. Nevertheless, it was opposed by the field coordinator who proposed equal treatment of all projects.

In what way have the projects been selected and evaluated?

All projects have been professionally evaluated by a Slovene and a foreign expert selected from the list of the reference experts proposed by the sponsor of the project. Afterwards they have been classified into 3 groups, each having a factor to correct required means, with respect to the review result, evaluation feasibility of the project and significance of the research group. Once the amount of the research work within the field intended means was known and after the verification of the proposed research group vacancy a motion for projects financing has been elaborated. It was coordinated at the Field Coordinator meeting within the Technics Council II and was integrally adopted.

Subsequently international references of the projects protagonists and specially so called "citation index" have been verified at Coordination Councils, the result of which is the motion proposed to the Ministry.

What is the amount of the means referred to?

Within the field of electronic components and technology 98.649.000 SIT will be contributed by the Ministry.

This amount is propotional to the amount that this field was granted in previuos periods and higher in relative share with respect to means intended for industrial research projects. There is a strategy tendency of the Ministry to finance groups that have proved to be excellent so far.

Does it mean that quality criteria have become more stringent or is it simply an excuse for increasingly diminishing of means that are intended to research activity by Slovenia every year?

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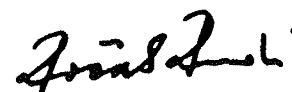

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BiCMOS CIRCUIT DESIGN USING THE LATERAL PNP. A MODEL AND SOME CIRCUIT APPLICATIONS.

Sean A. Smedley

KEYWORDS: CMOS devices, bipolar devices, single chip, circuit design, device fabrication, complementar properties, PNP bipolar transistors, BiCMOS circuits, lateral PNP, circuit models, SPICE computer program

ABSTRACT: This paper presents a SPICE model for the lateral PNP bipolar transistor that can be formed in a standard CMOS process with the p+ source diffusion and the n-well. This lateral PNP has an uncommitted collector, unlike the vertical PNP whose collector is always tied to the most negative supply voltage. The circuit designer is thus free to mix CMOS and Bipolar devices and to exploit their complimentary properties. Some examples of BiCMOS design are presented.

Načrtovanje BiCMOS vezij z uporabo lateralnih pnp bipolarnih transistorjev. Model in nekaj primerov uporabe

KLJUČNE BESEDE: CMOS naprave, naprave bipolarne, rezine enojne, projektiranje vezij, izdelava naprav, lastnosti komplementarne, PNP transistorji bipolarni, BiCMOS vezja, PNP lateralni, modeli vezij, SPICE program računalniški

POVZETEK: V prispevku je opisan SPICE model za lateralni PNP bipolarni transistor, ki ga lahko izdelamo v standardnem CMOS procesu, kjer sta za emiter in kolektor uporabljeni P + difuziji, n otok pa je baza. Tak lateralni PNP tranzistor ima izoliran kolektor, med tem ko je kolektor vertikalnega PNP tranzistorja vedno vezan na najbolj negativen potencial v vezju.
Načrtovalec tako lahko pri načrtovanju vezij uporabi CMOS in bipolarne komponente ter izkoristi njihove komplementarne lastnosti.
V prispevku je prikazanih nekaj primerov načrtovanja gradnikov integriranih vezij v BiCMOS tehnologiji.

Introduction.

Fig 1 shows the process cross section of a lateral pnp transistor fabricated on a standard CMOS n-well process. The transistor base width is determined by the polysilicon in exactly the same way as the MOS channel length. The majority of carriers injected into the n-well base are collected by the active collector, Ca, which completely surrounds the emitter. A minority escape into the substrate where they are collected by the substrate collector, Cs. This structure behaves like a lateral pnp and a vertical pnp in parallel, the emitters and bases being common, the collectors separate. This transistor

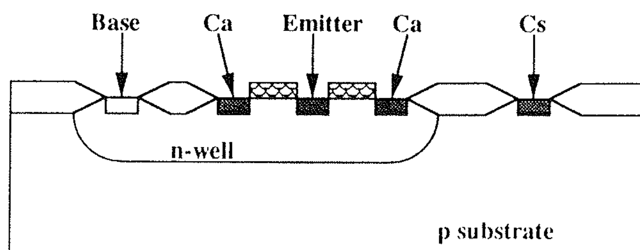

Fig. 1: Process Cross Section.

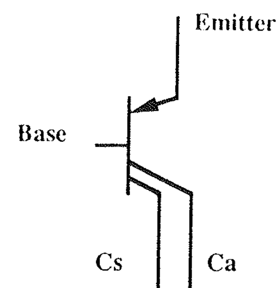

Fig. 2: Lateral PNP Symbol.

has been reported by several authors /1/, /2/. Fig 2 shows the double collector symbol for this device.

The Lateral PNP Model

Fig 3 shows the mask layout for the pnp used in the described circuits. We wish to maximise the lateral transistor action from the emitter periphery to the collector and minimise the vertical action from the bottom of the emitter down into the substrate. Therefore the emitter geometry should have the longest periphery to the smallest area. A minimum sized emitter fulfills this condition, 6 μ x 6 μ in our case. Assuming the current gains

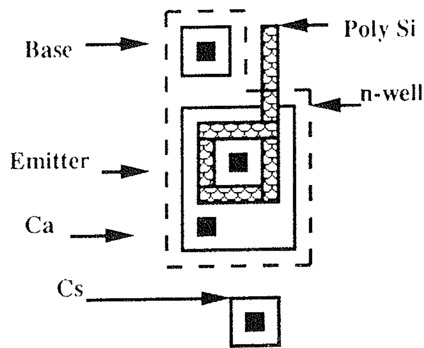

Fig. 3: Mask Layout.

are large enough to allow us to ignore base current, the emitter current, Ie, divides between the two collectors, Ca and Cs, as:

$$I_{ca} = \alpha \cdot I_e \text{ and } I_{cs} = (1 - \alpha) \cdot I_e$$

The current gains are defined as:

$$\beta_L = \left(\frac{Ica}{Ib}\right) \text{and } \beta_V = \left(\frac{Ics}{Ib}\right)$$

Fig 4 shows a typical plot of β_L against Ica. At very low currents β_L is reduced by "weak injection effects". The

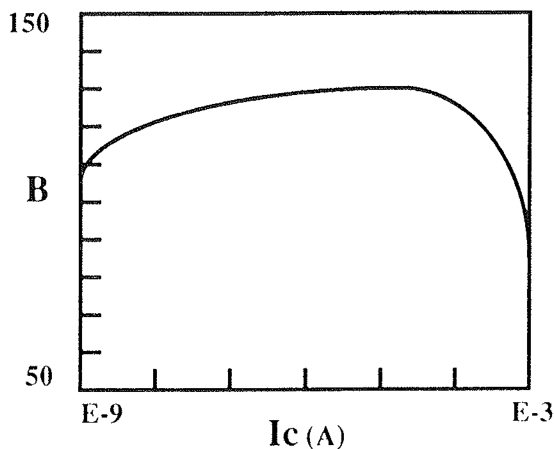

Fig. 4: B versus Ica.

principle one being that a proportion of the minority carriers injected into the base recombine at the sites of surface defects. At higher current levels "strong injection" dominates and the surface recombination is negligible. The useful current range for this device is 10^{-8} to 10^{-4} A.

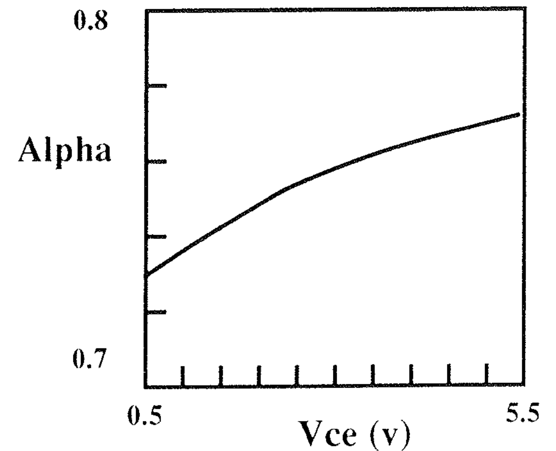

Fig. 5: Alpha versus Vce.

The division of the collector current into two parts, Ca and Cs, is very significant from a circuit design point of view. Unless the application requires both collectors to be connected to V-, the Ics current is effectively lost. So it is very important to characterise α. Fig 5 shows a typical plot of α against Vce. For this particular n-well process α varies from about 0.72 to 0.78. The model uses an average value of 0.75.

The Early voltages for the two transistors are quite different. This effect comes from the modulation of the depletion width of the base collector junction by the collector voltage. In the case of the lateral transistor this effect is severe and corresponds exactly with MOS channel length modulation. Early voltages of 10 to 15V are typical. The vertical transistor base collector junction is the n-well to substrate junction. These two lightly

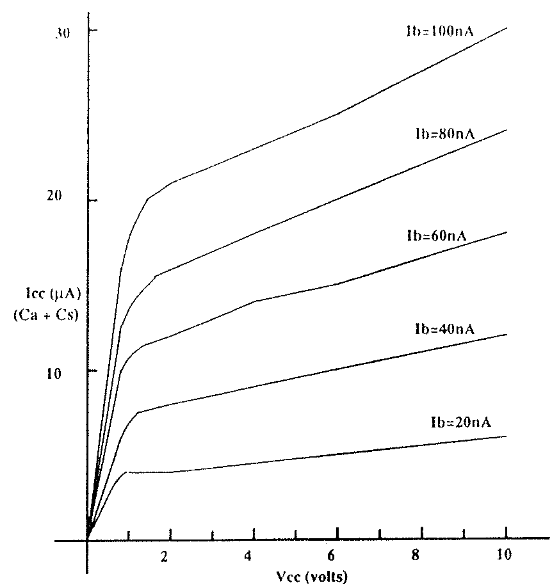

Fig. 6: Composite transistor Characteristics

doped regions have very little depletion region width variation so the vertical transistor Early voltage is very high, 100 to 300 V being typical. Fig. 6 shows typical transistor characteristics for the composite device.

The SPICE Model.

The vertical and lateral components of the transistor are formed into a SPICE code subcircuit as below:

```
.MODEL LATPNP PNP BF = 150 VAF=15 IS=2.5E-16
IKF=1 M ISE=5E- 19 NE=1.05 NF=1
.MODEL VERPNP PNP BF=9999 VAF=300 IS=9E-17
IKF=1M NF=1
.SUBCKT LPNP 100 101 102 103
**order is Ca Cs B E**
Q1 100 102 103 LATPNP
Q2 101 102 103 LATPNP
.ENDS
```

Example (1): A Band Gap voltage reference circuit.

Fig 7 shows a typical BiCMOS bandgap reference circuit fabricated in n-well CMOS technology. The bipolar pnp transistors are lateral devices as described above. The

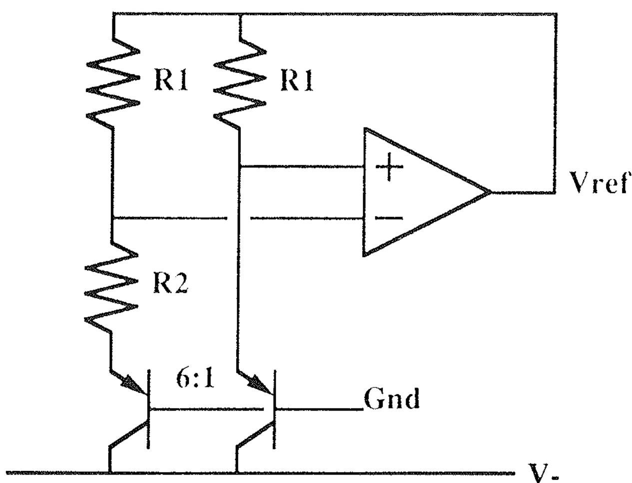

Fig. 7: The Bandgap Circuit.

CMOS Op-Amp can be quite standard. This particular circuit has the advantage that since both collectors of the composite bipolar transistor are connected to V- the current ratio between Ca and Cs is irrelevant. Precision matching of emitter areas is done with multiple copies of the same unit transistor. Precision resistor ratios are achieved by using a single unit and connecting as many as are necessary with metal. The op-amp output is the band-gap reference voltage and can be shown to be:

$$V_{BG} = V_{be} + V_t \frac{R_1}{R_2} \ln N,\ V_t = \frac{kT}{q}$$

N = ratio of emitter areas, 6 in this case

In the proces used here the n-well sheet resistivity is 2.1K/sq. and the designer chose R1/R2 = 13. so R2 was made a 10 sq unit resistor of 21K. R1 (=273K)was made from 13 individual 21K resistors connected in series. Note that unit resistors may be connected in any series/parallel combination and so practically any ratio can be accurately designed. SPICE simulations for this circuit are shown in the table below.

Temp.(deg. C)	0	25	50	75	100
Vref (V)	1.172	1.173	1.175	1.176	1.176
+ 15% resistors	1.168	1.170	1.171	1.171	1.172
- 15% resistors	1.176	1.178	1.179	1.180	1.181

Making R2 = 12.75 x R1 = 268 K leads to slightly better results but such fine tuning should be done on the actual silicon. Remember, you cannot get 1 % results from a 5 % model !

Example (2): A Differential Op-Amp Input Stage.

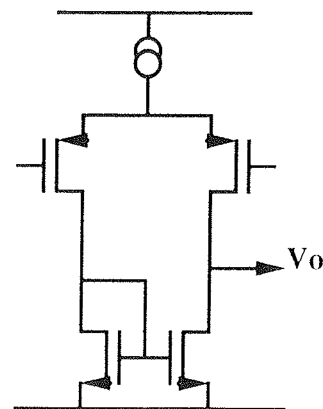

Fig. 8a: PMOS i/p devices.

Fig 8a show a standard single stage CMOS op-amp. Circuits such as this form the basic building blocks of most sampled data analog MOS circuits, frequently combined with switched capacitor techniques.

The transconductance of the MOS input transistor is given by:

$$g_m = \sqrt{2K \frac{W}{L} \cdot I_D}$$

We can replace the PMOS input transistors with PNP bipolar ones as in Fig 8b. The transconductance of the bipolar pnp transistor is now given by:

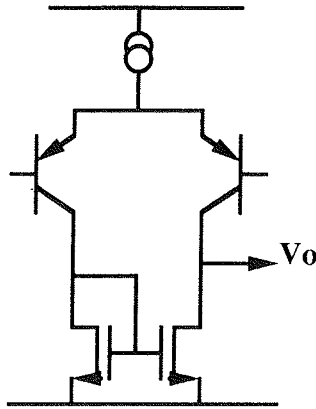

Fig. 8b: PNP Biplolar i/p devices

$$g_m = \frac{I_C}{V_t}$$

Assuming typical MOS parameters such as W/L = 10, K = 40µA/V2, we can tabulate the MOS and Bipolar gm for various bias currents.

Ic = Id	1 µa	10 µA	100 µA
MOS gm (x 10E-3)	0,028	0.09	0.28
Bipolar gm (x10E-3)	0.04	0.4	4.0

At bias currents above 1 µA the pnp bipolar input stage clearly has more gain. The table below gives some SPICE simulations for a load of 0.5pF.

Ic = Id	1 µa	10 µA	100 µA
MOS Gain (db)	45	35	25
MOS Band Width (MHz)	2.5	7	20
Bipolar Gain (db)	52	50	49
Bipolar Band Width (MHz)	4	30	200

If the supply of input base current can be tolerated then the circuit with bipolar inputs has a superior performance in every case, but particularly at higher bias currents. Such an op-amp will be used in high frequency continous time filters. The all MOS input stage is likely to remain the choice for switched capacitor speech filters.

The composite lateral pnp has a low Early voltage (reduced output impedence) so the NMOS current mirror load has been kept for both circuits.

Conclusions

Standard CMOS processing can give very useable bipolar transistors. A SPICE model for the lateral/vertical pnp bipolar transistor has been presented to enable BiCMOS circuits to be simulated and two practical design examples have been described:

(1) A Band Gap reference with 14mV variation over 0-100 deg. C and process extremes.

(2) A high performance 200 MHz op-amp with pnp input devices.

References.

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/2/ P. Masquelier, "Controlled Power on Reset Circuit". Third EURO-CHIP Workshop on VLSI Design Training, Grenoble, France. Analog class design competition.

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NOISE BEHAVIOR OF SC CIRCUITS

Slavko Starašinič, Janez Trontelj

KEYWORDS: *SC* circuits, *MOS* switches, noise properties, analysis, noise distribution, noise sources, spectral density, noise density, thermal noise, sampled noise, *SC* integrator

ABSTRACT: Noise behavior of *SC* circuits is analyzed in 'z' domain using simplified noise models for *MOS* switches and operational amplifiers. General mathematical description of *SC* circuit is upgraded by noise properties. Technique for analyzing of noise contributions of each individual noise source and also of spectral noise density of complete *SC* circuit is presented.

Šumne lastnosti vezij SC

KLJUČNE BESEDE: *SC vezja*, stikala *MOS*, lastnosti šumne, analiza, porazdelitev šuma, izvori šuma, gostota spektralna, gostota šuma, šumi termični, šum vzorčeni, *SC* integrator

POVZETEK: Z enostavnimi modeli stikal *MOS* in operacijskih ojačevalnikov so bile analizirane šumne lastnosti vezij *SC* v prostoru stanj. Splošnemu opisu vezij *SC* z diferenčnimi enačbami so bile dodane še šumne lastnosti. V članku je prikazana analiza porazdelitve šuma glede na posamezne šumne izvore kakor tudi spektralna gostota šuma celotnega vezja.

1. Introduction

Noise properties of analog building blocks is important parameter for design of analog systems on the silicon. By decreasing of noise floor of analog circuits the dynamic range is increased and from this view it is very important to reduce the noise of each building block. Noise of *SC* circuits is analyzed in this paper. For this purpose simplified noise models are prepared and are used in topological description of *SC* circuit. Noise voltage of each noise source is transferred to the output of *SC* circuit by its own transfer function. The 'z' domain analysis describes the sampled and held noise, which dominates in the signal frequency range ($f < \frac{f_s}{2}$). Complete behavior of *SC* circuits is described by topological matrix equations.

2. Basic Noise Models

Basic building blocks of *SC* circuits are switches, capacitors and operational amplifiers and main noise sources are operational amplifiers and switches. There are two basic mechanisms of noise generation:

- wide band noise
- sampled noise

Signals in *SC* circuits are sampled and stored in capacitors. In many cases this is the reason for smaller wide band noise compared to the sampled noise /2/. Sampled noise is divided into two groups:

- thermal noise of *MOS* switches
- noise of operational amplifiers.

Thermal noise of *MOS* switches and noise of operational amplifiers (thermal and 1/f noise) is sampled to individual capacitors and transferred to the output of *SC* circuit by its own transfer function. In many applications 1/f noise is eliminated by processing of direct and delayed signal at the same time /3/.

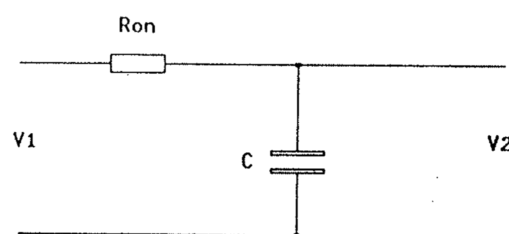

Fig. 1: Closed switch and corresponding capacitor

This allows simplified noise modeling of basic noise sources. Thermal noise of closed switch is sampled and stored in appropriate capacitor, and *RMS* voltage of such simple *RC* circuit shown in fig. 1 is /1/:

$$\overline{v_2^2(t)} = \frac{KT}{C} \qquad (1)$$

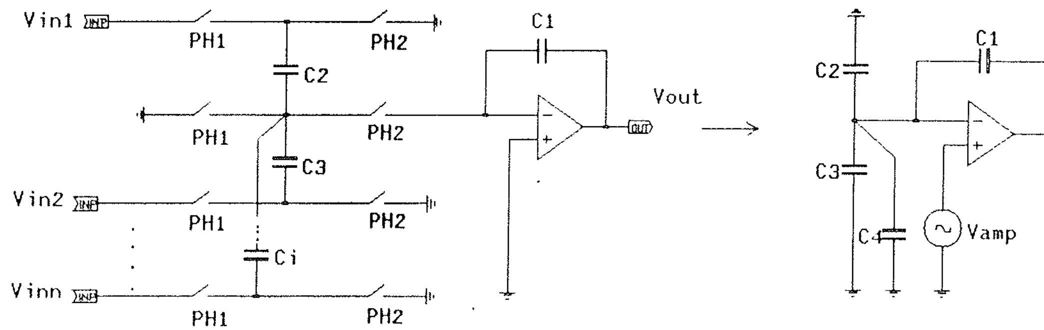

Fig. 2: *n - input integrating stage and corresponding schematic at phase* φ_2 .

where K is Boltzmann constant, T absolute temperature and C capacitance. For noise modeling of *SC* integrator the equivalent noise resistance R_{eq} of operational amplifier is used.

$$R_{eq} = \frac{\overline{v^2(t)}}{4KT\Delta f} = \frac{S_{amp}(f)}{4KT} \tag{2}$$

where $S_{amp}(f)$ is spectral noise density of operational amplifier. This simplified model can be generalized for *n - input* integrating stage in clock phase φ_2 as shown in fig. 2.

Total thermal noise of the operational amplifier in integrating stage is given by:

$$v^2_{int}(f) = \frac{KT}{C_1 + C_2 + \ldots + C_i} = \frac{KT}{\Sigma C_i} \tag{3}$$

where $v^2_{int}(f)$ is *RMS* noise voltage of integrating stage.

Top frequency for noise of integrating stage is defined by integrating capacitor and equivalent noise resistance of operational amplifier:

$$f_t = \frac{1}{2\pi C_1 R_{eq}} \tag{4}$$

Capacitors in *SC* circuits have defined ratio to the integrating capacitor so equation 3 can be transformed to:

$$v^2_{int}(f) = \frac{KT}{C_1\left(1 + \frac{C_2}{C_1} + \frac{C_3}{C_1} + \ldots + \frac{C_i}{C_1}\right)} = \frac{2\pi f_t KTR_{eq}}{1 + \gamma_1 + \gamma_2 + \ldots + \gamma_i} \tag{5}$$

where $\gamma_i = \frac{C_i}{C_1}$.

3. Topological description

By using simplified noise modeling mentioned above, noise analysis of complex *SC* circuits can be performed. Differentional equations transformed into the *'z'* domain describe signal transfer into the *SC* circuits. *n - stage* circuit can be described by the following matrix equation:

$$||A(z)|| \cdot ||V_n|| = ||N|| \cdot \lambda_{inp}(z) \cdot V_{vh} \tag{6}$$

Upper equation is valid for sampled signals and for equal duration of both phases of clock signal. Symbols in equation 6 are as follow:

$\|\|A(z)\|\|$	... matrix of circuit coefficients,
$\|\|V_n\|\|$	... vector of the voltages on the output of each integrator,
$\|\|N\|\|$	... vector of the input terminals,
$\lambda_{inp}(z)$	... input coefficient,
V_{inp}	... input voltage.

Number of the input terminals is defined by vector $||N||$. *This noise analysis is limited on one input and on one output terminal so vector* $||N||$ has the following form:

$$||N|| = \left|\left|\begin{matrix}1\\0\\0\\ \cdot \\0\end{matrix}\right|\right| \tag{7}$$

Noise analysis of *SC* circuits is performed by grounded input *(V_{inp} = 0)* and by adding matrix describing noise sources /4/. Equation 6 is therefore modified:

$$||A(z)|| \cdot ||V_n|| = ||B(z)|| \cdot ||V_{amp.n}|| + ||C(z)|| \cdot ||V_{sw.n}|| \tag{8}$$

where

$\|\|B(z)\|\|$	... matrix of circuits coefficients describing noise transfer from each operational amplifier,
$\|\|V_{amp.n}\|\|$	... vector of the noise voltages of the operational amplifiers,
$\|\|C(z)\|\|$	... matrix of circuits coefficients describing noise caused by switches and sampled on capacitors and

$||V_{sw.n}||$ ... vector of the noise voltages sampled on the groups of capacitors.

Noise behavior of *n - stage SC* circuit is described by equation 8. Two dominant noise sources are in each integrating stage - the first is operational amplifier noise and second are the switches causing the sampled noise voltage on the same capacitors. Decomposition of the upper matrix equation gives the group of *2n* linear equations for *n - stage* circuit. The noise voltage on the output of circuit is calculated for each uncorrelated noise source by solving of this group of equations. The transfer function from each noise source to the output is defined by this procedure. We have assumed a superposition theorem so only one noise source is active at a time and other are forced to zero. This is the reason for *2n* matrix equations. Vector of noise voltages of operational amplifiers have for *n - stage* circuit the following form:

$$\left\|V_{amp.n}\right\|_{(1)} = \left\|\begin{matrix} V_{amp.1} \\ 0 \\ 0 \\ . \\ 0 \end{matrix}\right\| \quad \left\|V_{amp.n}\right\|_{(2)} = \left\|\begin{matrix} 0 \\ V_{amp.2} \\ 0 \\ . \\ 0 \end{matrix}\right\|$$

$$\left\|V_{amp.n}\right\|_{(n)} = \left\|\begin{matrix} 0 \\ 0 \\ 0 \\ . \\ V_{amp.n} \end{matrix}\right\| . \qquad (9)$$

Noise transfer from each operational amplifier is defined in matrix $||B(z)||$. Order of this matrix is $n \times n$ and all nondiagonal coefficients are zero.

$$||B(z)|| = \left\|\begin{matrix} b_1 & 0 & 0 & . & 0 \\ 0 & b_2 & 0 & . & 0 \\ . & . & . & . & . \\ 0 & 0 & 0 & . & b_n \end{matrix}\right\| \qquad (10)$$

Coefficients $b_1, b_2 \ldots b_n$ describe noise transfer from corresponded operational amplifier to the output of the circuit. All operational amplifiers except the last amplifier are active by noise transfer to the output of *SC* circuit in one phase. Only the last amplifier transfer the noise to the output of *SC* circuit in both phases of clock. This is the reason for special treatment of coefficient b_n:

$$b_n \cdot V_{amp.n} = \left\|b_{n.1} \; b_{n.2}\right\| \cdot \left\|\begin{matrix} V_{amp.n1} \\ V_{amp.n2} \end{matrix}\right\| . \qquad (11)$$

Vectors of noise voltages on individual groups of capacitors have the following form:

$$\left\|V_{sw.n}\right\|_{(1)} = \left\|\begin{matrix} V_{sw1} \\ V_{sw2} \\ 0 \\ 0 \\ . \\ 0 \\ 0 \end{matrix}\right\| \quad \left\|V_{sw.n}\right\|_{(2)} = \left\|\begin{matrix} 0 \\ 0 \\ V_{sw1} \\ V_{sw2} \\ . \\ 0 \\ 0 \end{matrix}\right\|$$

$$\left\|V_{sw.n}\right\|_{(n)} = \left\|\begin{matrix} 0 \\ 0 \\ 0 \\ 0 \\ . \\ V_{sw1} \\ V_{sw2} \end{matrix}\right\| . \qquad (12)$$

Individual group of capacitors consists of all capacitors at each integrating stage. It is important to take into account the transfer function from each capacitor group to the output of *SC* circuit in both phases. Vectors of noise voltages caused by switches and matrix $||C(z)||$ are defined for φ_1 and φ_2. Matrix $||C(z)||$ have the following form:

$$||C(z)|| = \left\|\begin{matrix} c_{1.1} & c_{1.2} & 0 & 0 & . & 0 & 0 \\ 0 & 0 & c_{2.1} & c_{2.2} & . & 0 & 0 \\ . & . & . & . & . & . & . \\ 0 & 0 & 0 & 0 & . & c_{n.1} & c_{n.2} \end{matrix}\right\| . \qquad (13)$$

4. Results

All coefficients needed for calculation of individual spectral noise density are given by solving of *2n* systems of matrix equations. These coefficients are the voltages on the output of the circuits caused by individual noise sources. Simplified description of such solutions is presented by the following equations:

$$\begin{aligned} V_{n.amp.1} &= V_{amp.1} \cdot F_{amp.1} \qquad (14) \\ V_{n.amp.2} &= V_{amp.2} \cdot F_{amp.2} \\ &\vdots \\ V_{n.amp.n} &= V_{amp.n} \cdot F_{amp.n} \\ V_{n.sw.1} &= V_{sw.1} \cdot F_{sw.1} \\ V_{n.sw.2} &= V_{sw.2} \cdot F_{sw.2} \\ &\vdots \\ V_{n.sw.n} &= V_{sw.n} \cdot F_{sw.n} \end{aligned}$$

where the voltages of individual noise sources *($V_{amp.1}$, ... $V_{sw.n}$)* are multiplied by their own transfer function ($F_{amp.1}$, ... $F_{sw.2}$). Individual spectral noise density are calculated from equation 14. For this purpose spectral noise densities of noise sources are used and transfer function is multiplied by its own complex conjugated value. Spectral noise density of complete *SC* circuit is defined:

$$S_n = \sum_{amp.n=1}^{amp.n=n} S_{n.amp.n} + \sum_{sw.n=1}^{sw.n=n} S_{n.sw.n} \qquad (15)$$

Noise properties of individual noise sources transferred to the output are very important for improved design of *SC* filters. For optimal design the contribution of each noise source should be in the same range. The noise contribution of the switches can be decreased by larger capacitor unit, noise contribution of the operational

amplifiers can be smaller if operational amplifiers have both lower thermal noise and lower unity gain bandwidth.

5. Design example

Matrix equation for noise analysis of *SC* circuits was used for noise analysis of low pass Ladder filter from fig. 3.

Three matrix equation describing noise properties of operational amplifiers and additional three for noise of switches was defined for this circuit:

$$\left\|\begin{matrix} a_1 & a_2 & 0 \\ a_4 & a_5 & a_6 \\ 0 & a_8 & a_9 \end{matrix}\right\| \cdot \left\|\begin{matrix} V_1 \\ V_2 \\ V_3 \end{matrix}\right\| = \left\|\begin{matrix} b_1 & 0 & 0 \\ 0 & b_2 & 0 \\ 0 & 0 & b_3 \end{matrix}\right\| \cdot \left\| V_{amp.n} \right\| +$$

$$+ \left\|\begin{matrix} c_{1.1} & c_{1.2} & 0 & 0 & 0 & 0 \\ 0 & 0 & c_{2.1} & c_{2.2} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{3.1} & c_{3.2} \end{matrix}\right\| \cdot \left\| V_{sw.n} \right\| \qquad (16)$$

where the coefficients have the following expressions:

$$a_1 = z \cdot (1 + \lambda_2) - 1 \quad \lambda_1 = \frac{C_2}{C_1} \quad \lambda_2 = \frac{C_4}{C_1} \qquad (17)$$

$$a_2 = \lambda_3 \quad \lambda_3 = \frac{C_3}{C_1} \quad \lambda_4 = \frac{C_6}{C_5}$$

$$a_4 = -\lambda_4 \cdot z \quad \lambda_5 = \frac{C_7}{C_5} \quad \lambda_6 = \frac{C_9}{C_8}$$

$$a_5 = z - 1 \qquad \lambda_7 = \frac{C_{10}}{C_8}$$

$$a_6 = -\lambda_5 \cdot z$$

$$a_8 = \lambda_6$$

$$a_9 = z \cdot \left(1 + \lambda_7\right) - 1$$

$$b_1 = -\left[z \cdot \left(1 + \lambda_1 + \lambda_2 + \lambda_3\right) - 1\right]$$

$$b_2 = -\left[z \cdot \left(1 + \lambda_4 + \lambda_5\right) - 1\right]$$

$$b_3 = b_{31} + b_{32} \qquad b_{31} = -(z-1) \quad b_{32} = -\left(\lambda_6 + \lambda_7\right) \cdot z$$

$$c_{1.1} = z \cdot \left(\lambda_1 + \lambda_2 + \lambda_3\right) \qquad c_{1.2} = \left(\lambda_1 + \lambda_2 + \lambda_3\right)$$

$$c_{2.1} = -z \cdot \left(\lambda_4 + \lambda_5\right) \qquad c_{2.2} = \left(\lambda_4 + \lambda_5\right)$$

$$c_{3.1} = -z \cdot \left(\lambda_6 + \lambda_7\right) \qquad c_{3.2} = \left(\lambda_6 + \lambda_7\right).$$

RMS noise voltage on the outputs of the operational amplifiers are calculated for first two amplifiers for only one clock phase and for last amplifier for both clock phases:

$$b_3 \cdot V_{amp.3} = b_{31} \cdot V_{amp.31} + b_{32} \cdot V_{amp.32} \qquad (18)$$

$$V^2_{amp.31} = \frac{2\pi f_t\, KT\, R_{eq}}{1 + \lambda_1 + \lambda_2 + \lambda_3} \quad V^2_{amp.2} = 2\pi f_t\, KT\, R_{eq} \qquad (19)$$

$$V^2_{amp.31} = \frac{2\pi f_t\, KT\, R_{eq}}{1 + \lambda_6 + \lambda_7} \quad V^2_{amp.32} = 2\pi f_t\, KT\, R_{eq.} \qquad (20)$$

From matrix equation 16 six results are obtained, which represent noise contribution of each amplifier and of each group of switches. The following parameters were used for this analysis:

clock frequency of *SC* circuit ... f_t=1024 kHz

top frequency of operational amplifier ... f_T=5 MHz

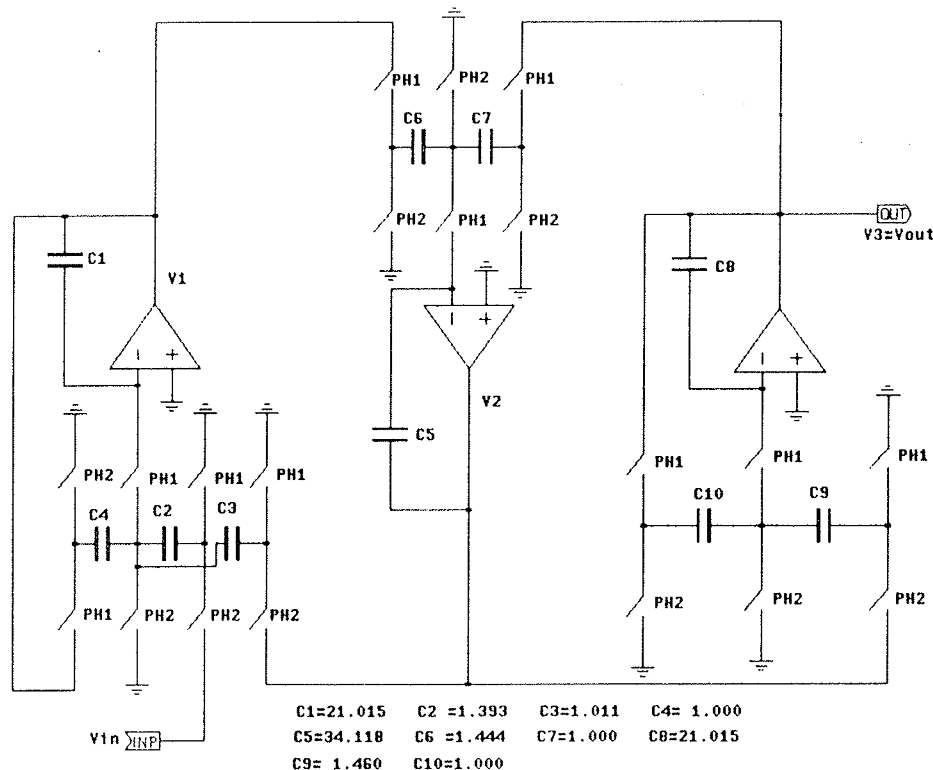

Fig. 3: Low pass Ladder filter (n=3).

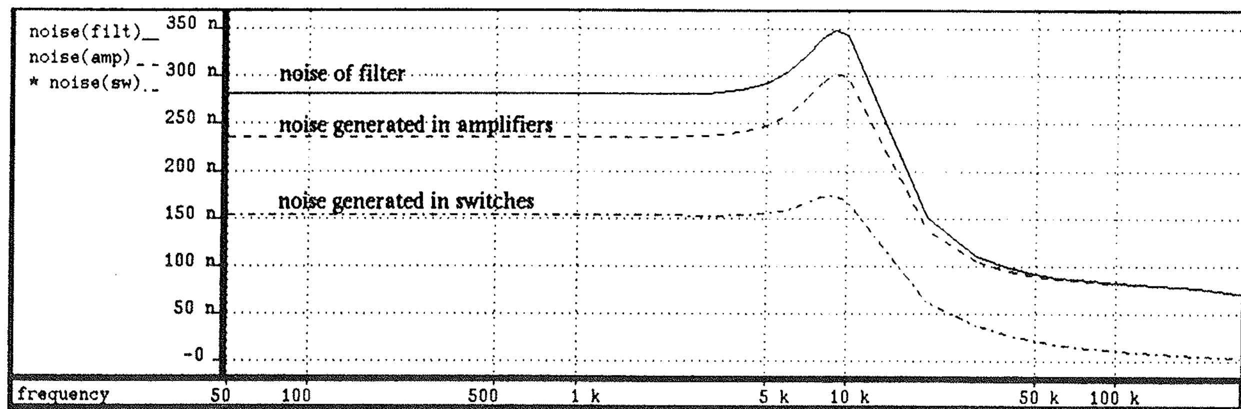

Fig. 4: *Noise properties of low pass filter.*

thermal noise of operational amplifier ... $u_n = 60 \frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$

unity capacitor ... $c_u = 0.5$ pF.

Fig. 4 presents spectral noise density of low pass filter. This filter was realised in high performance integrated telephone set with codec. The measurement in the system prooved good matching to calculated values.

6. Conclusion

The method for noise analysis of *SC* circuits is presented. For this purpose the topological description of main noise sources is added to the general matrix equation. Noise analysis is performed in 'z' domain. Resulted noise voltages are after this procedure transformed to *time* domain. Spectral noise density are calculated for each noise source contribution and for final result the spectral noise density of each individual noise source is summarized.

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THE ISKRA SOLID STATE ENERGY METERS
A single chip measuring module based on the integrated Hall effect sensor

Pavel Jamnik

KEYWORDS: electrical energy measurement, electrical energy meters, solid state energy meters, electrical meters, integrated HALL sensors, single chip, measuring modules

ABSTRACT: In this article we would like to present the latest achievement of the ISKRA factory in the field of the Solid State meter, class 2, for household as well as for industrial applications.

ISKRIN elektronski števec energije
Enočipni merilni modul na osnovi Hallovega efekta

KLJUČNE BESEDE: merjenje energije električne, števci energije električne, števci energije polprevodniški, števci elektronski, HALL senzorji integrirani, rezine enojne, moduli merilni

POVZETEK: Članek podaja zadnje dosežke tovarne ISKRA ŠTEVCI na področju elektronskih števcev energije, razred 2, tako za širokopotrošno, kot industrijsko uporabo.

Introduction

The very fast development of electronic technology and especially its most vital branch microelectronics lead to the discovery of many new principles of energy measurements in order to be competitive with the present dominant classic Ferraris energy meter. The first Solid State energy meters, developed in the early seventies, were high precision measurement instruments (accuracy class from 0.5 to 0.05). Since then, it has been necessary to spend 10 to 15 years on research in order to develop a reliable, cheap and accurate simple meter, class 2.

Integrated Hall Effect Sensor

The physical principle of the Hall effect was discovered in the nineteenth century (1879) but its wide application became reality only with the introduction of the microelectronics technology. The Hall effect principle is a very attractive solution for energy measurement because it senses and multiplies current and voltage at the same time. When we put piece of a semiconductor in a magnetic field caused by load current (IL) and force the current trough te semiconductor caused by load voltage (UL), we can sense the Hall voltage (UH) on the edges of the semiconductor which is proportional to the power of the load (UH*K=PL=UL*IL). The other very important advantages of the Hall effect sensor are the frequency and the phase indenpendence as well as the small dimensions ($s = 0.05\ mm^2$) and the wide dynamic range of sensing.

The Hall sensor can be produced by various semiconductor technologies (i.e. ITL, MOS, etc.) as well as different substrates (i.e. Si, GaAs) but none of these technologies or substrates are ideal. The raw sensor has many disadvantages, i. e. non-linearity, temperature dependency, offset voltage, long-term non-stability, sensitivity to mechanical stress, low output voltage, voltage dependency, etc.

This means that it is imposibble to use the original Hall sensor for professional measuring techniques without significant improvements.

The ISKRA factory developed the concept of the integrated sensor which can be produced in a standard industrial process. After years of research and development efforts, ISKRA managed to make Hall sensor which can be integrated with analoque and digital electronics on the same substrate, with satisfactory results and regardless the limitations of standard technology.

One-Chip-Meter - Integrated Solution of Measurement and functional Electronics

The measurement electronic of the Hall sensor, the analog/digital conversion of the very low sensor signals and the circutry for compensation of all undesirable effects are combined in the same chip. The temperature compensation assures a voltage reference with the programmed temperature coeficient in contrast with the sensor. Because of the common substrate there is no delay in compensation response.

The block of digital electronics controls the analoque functions and provides all the output signals which are important for various types of meter functions(i. e. direction indication of energy flow, starting current limiter, polyphase summator, stepped motor driver, active and reactive power selection, etc.).

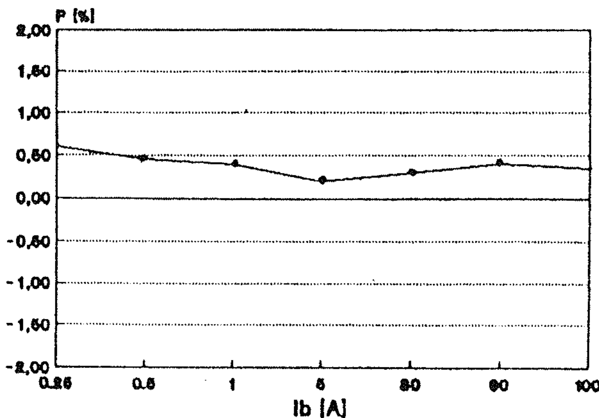
During the chip design phase full attention was focused on the lay-out in order to prevent mutual influences between analoque, digital and Hall sensor electronics.

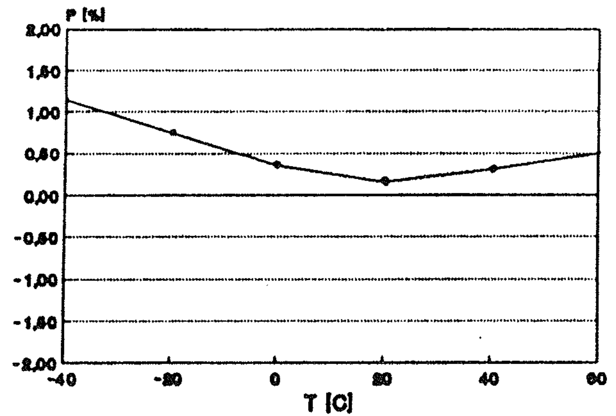
In order to meet high quality demands (long life, reliable and stable operation) a chip in a professional hermetic ceramic capsule has been used. ISKRA developed a special encapsulation line which can successfully satisfy specific parameters and allows high quality control over the most sensitive part of the meter.

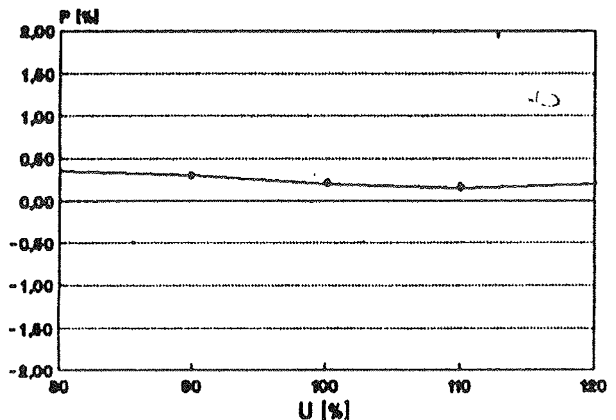
ISKRA Universal One-Chip Measuring Module

A very high degree of integration minimizes the necessity of out-chip components. The measuring module consists of current leads (terminals), main voltage connections, calibration elements, the magnetic system and the printed circuit board with chip.

The measuring module is designed as an universal element for all types of Solid State meters. **Figure 1** shows some basic measuring characteristics of this module.







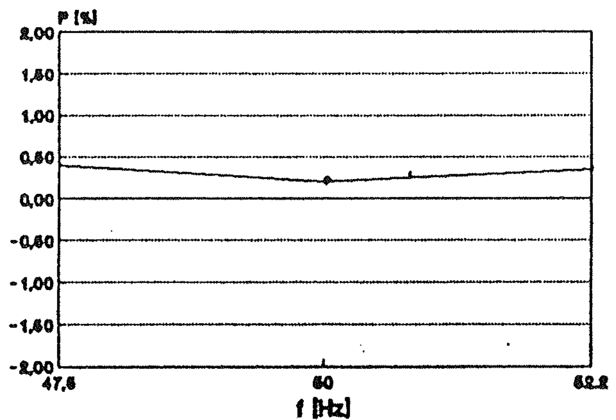


Fig. 1: Measuring characteristics of the measuring module

Family of Electronic Meters of Energy

With this unique universal measuring module ISKRA is able to make all types of energy meters concerning various main voltages, load currents, directions of energy flow, active and reactive energies, single and polyphase measurements. With the support of the micropro-

cessor it is possible to enrich the basic functions with a wide range of tariffs, maximum demand registrations, real time clock, load control functions, communication port and data protection.

Figures 2 and 3 show two typical representatives of the ISKRA Solid State meters. The first is a single-phase one-tariff kWh meter, the second is a three-phase kWh meter with a universal programmable multi-tariff unit with complete maximum demand possibilities, real time clock and communication port. The new technology, essentially microelectronics offers great challenge for classic measuring methods. With better and better results the Solid State energy meters have allready begun to replace classic Ferraris meters, espacially in the field of multifunctional measurements and communications. In the future the measuring unit will remain an important component in the system for energy control and management systems.

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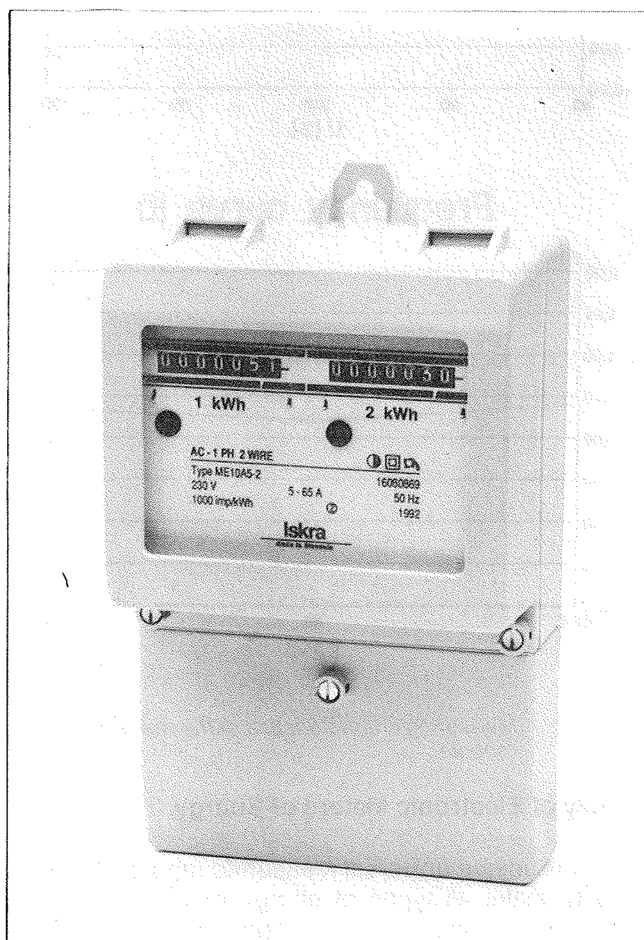

Fig. 2: Single phase one tariff KWh meter

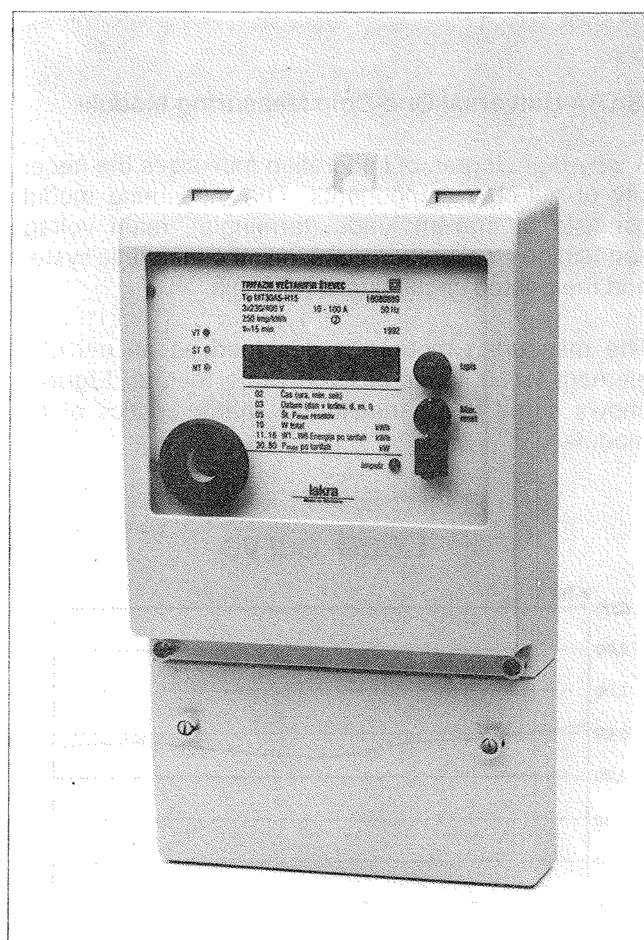

Fig. 3: Three phase kWh meter

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SPIN-ON-GLASS PLANARIZATION OF DEVICE TOPOGRAPHY

Radko Osredkar

KEYWORDS: microelectronics, integrated circuits, water fabrication, topography planization, SOG spin-on-glasses, siloxan, centrifugal deposition

ABSTRACT: In this paper materials, methods, and processing of the spin-on- glasses (SOG) for planarization of wafer topography in integrated circuit fabrication are reviewed.

Postopki planarizacije s centrifugalnim nanašanjem siloksanskih stekel

KLJUČNE BESEDE: mikroelektronika, vezja integrirana, proizvodnja mikroploščic, planarizacija topografije, SOG spin-na-steklu, stekla siloksanska, nanašanje centrifugalno

POVZETEK: V preglednem članku so opisani materiali, metode in tehnološki postopki za centrifugalno nanašanje planarizacijskih plasti siloksanskih stekel v mikroelektronskih proizvodnih procesih.

1. Introduction

Device planarization, the reduction of distances between topography extremes in the direction normal to the wafer plane and the reduction of the side-wall slopes in order to facilitate subsequent processing steps, came into the technology forefront as lateral geometries began to shrink. Planarization is most critical during the final processing steps in IC fabrication, where metalization and dielectric layers are used. In double metal IC fabrication processes planarization is used primarily to enhance the step coverage of the top metal layer. Also, it is much easier to image fine line geometries on nearly planar surfaces and to etch lithographic patterns into a film if the resist does not cover severe topography /1,2/.

Flow of the dielectric film will smooth device topography if the temperature of the dielectric is raised to the point where the surface tension of the film becomes the dominant force acting on the film /2,3,4/. The temperature at which the flow occurs depends on the dopants included in the film (e.g. phosphorus and boron) and the details of the process, and lies between 500 deg C and 1000 deg C. This temperature range is acceptable for use of this planarization technique over conductors such as polysilicon and silicides, but too high for use over aluminum.

A common method of planarization is the etch-back process, where a thick dielectric layer (eg. 3 μm) is deposited over the first metal level, rounding its shoulders and filling the trenches between metal lines. The dielectric is then etched back to approximately 1 μm. Even though there are no temperature constraints associated with this process, planarization of topography over closely spaced lines may form a void at the bottom of the trench, causing severe problems during subsequent processing and with the reliability of the device. Variations of the technique (eg. using TEOS or APCVD instead of PECVD oxide) seem to overcome some of the problems mentioned above.

The sacrificial layer etch-back technique involves the deposition of a relatively thick layer with good planarizing properties (eg. photoresist, polyimide, spin-on-glass) over the dielectric. This layer is first smoothed and then etched untill none of it remains on the wafer. If the etch rates of the sacrificial film and the underlying dielectric are the same, or in plasma etching, if the ratio of the etch rates for both films is selected to take account of the microloading effects, the smoothed top surface of the sacrificial layer will be transfered to the dielectric. This technique, though relatively simple in principle, is very demanding regarding maintaining the proper etch rates, with all the complications associated with plasma etching of polimer films. In planarizing trenches with high aspect ratios (trenches deep relative to their widths) there may remain some of the sacrificial material in them, which can not be allowed with polymer sacrificial film and may be undesirable with spin-on-glass.

There are now available several materials that find application as planarization layers either by replacing dielectric films or being used over a thin dielectric film.

Such materials are polyimide and non-etch-back spin-on-glass, and their use is based on the planarization effect of a spun-on film of low viscosity.

In this paper planarization techniques utilising a spin-on-glass sacrificial layer are reviewed and described in some detail.

2. Spin-on-glass material

Spin-on-glass planarization techniques combine the planarization effect on spun-on films with the oxide-like material characteristics on SOG, resulting in simple and straightforward processing /5/. As a dielectric layer in multilevel interconnection structures, SOG films offer the following advantageous properties:

- high thermal/oxidative stability,
- etch characteristics similar to those of CVD oxides,
- good adhesion to silicon, oxides, aluminium, etc,
- can be doped,
- low trace metal contamination levels.

Thus, SOG materials are compatible with materials and processes of the IC fabrication technology, and SOG processes are easily integrated into existing process flows.

Spin-on glass liquids consist of Si-O chain polymers dissolved in commmon organic solvents, such as alcohols, ketones, and esters. The polymers are prepared through the same basic chemistry as that employed in sol-gel technology. Commercially available SOG materials are of four major types, listed in Table 1.

Polymer	Film Composition
Silicate	(SiO_2)
Phosphosilicate	$(SiP_xO_y)n$
Siloxane	$(R_xSiO_y)_n$
Phosphosiloxane	$(R_xSiP_yO_z)_n$

Table 1. Types of SOG materials

The nature of the siloxane or silicate polymer is determined by the reaction conditions, such as molar ratio of H_2O to polymer, pH, concentration of the solution, etc. Unlike sol-gel technology in which the goal is to form dense gels quickly, the reaction conditions in SOG synthesis are chosen such, that the polymers are stable toward molecular weight increase for periods of several months. Since gelation time is a strong function of concentration, the equivalent silica (SiO_2) content of most commercial SOG products is typically 10 percent or less. Therefore the SOG film thickness is usually limited to a few hundred nanometers.

The properties of ther SOG materials can be modified by incorporating a substituted alkoxysilane with methyl or phenyl radical, or a dopant such as phosphorus or boron, during the hydrolysis reaction.

The material characteristics of SOG films are fundamentally similar to those of sol-gel glasses. However, there are two important distinctions:

1. The first one stems from the fact that a SOG film is always formed on a substrate toward which it exhibits good adhesion. When such a film is dried and cured, shrinkage can occur only in the direction perpendicular to the substrate plane, since the film is constrained to remain adhered to the surface. This results in buildup of tensile stress paralel to the surface. Consequently, SOG films have a propensity for cracking, and the spin-on process has to take account of it. This tendency for cracking is somewhat reduced by organic groups introduced into the SOG polymer.

A study /6/ shows, that the tensile stresses in SOG films are below 10^9 dyne/cm^2. Due to the film shrinkage, the tensile stress after a 450° C bake is higher than the stress in a film baked at 200°C. Higher annealing temperatures are required to rearrange the bond angles to relieve the stress. After 920°C annealing, the thermal stress overcomes the tensile stress, resulting in a compressive film, after cooling it to room temperature. Oxygen annealing gives a lower stress than nitrogen annealing, but the reduction is very limited.

2. In IC fabrication the maximum temperature at which a SOG film can be cured is often limited to 450°C because of the presence of aluminum interconnects. After such low temperature cures the SOG film is far from being completely densified and contains significant amounts of silanols, ≡Si-OH, and adsorbed water. If the SOG film can be densified at high temperature, typically at 800°C to 900°C, a silanol- and water-free film is obtained, as demonstrated by IR spectroscopy /5/. The elimination of the silanols and water from SOG films after the high temperature cure is accompanied by a drop in the wet etch (HF) rate of the film to that of thermal SiO_2, implying complete densification. However, complete loss of water and silanol after a high-temperature cure does not guarantee complete densification, and the actual extent varies - particularely among siloxane-type SOG films.

Thickness measurements and other observations indicate that the SOG, as deposited and dried, is somewhat porous and one of the effects of subsequent processing is to reduce the porosity. Experiments suggest /7/ that the porosity is not completely removed by high temperature (900°C) processing. Cured SOG films placed in high vacuum and heated to approximately 500°C will desorb H_2O, a process which takes about 250 sec. After desorption the films can be refilled by placing them close to an open beaker of water for 12 hours. This suggests that the desorption is due to water coming out of pores in the SOG, rather than from reaction by-products. The source of the H_2O that is desorbed is simply ordinary ambient air.

The dielectric properties of a cured SOG film are, to a great extent, determined by its silanol and water content (8). For instance, the dielectric constants of silicate films after curing at 425°C and 900°C are found to be about 9 and 4, respectively. The high dielectric constant indicates the presence of a significant amount of polarisable meterial in these SOG films. This polarisable species is H_2O that is adsorbed into the microporous structure of the SOG film. Due to reversible adsorbtion/desorbtion of H_2O variations in the dielectric constant value occur. The dielectric properties of the films densified at 800°C become quite comparable to those of thermal SiO_2. It is interesting to note thet the dielectric constant of the densified SOG film, i.e. 4.2, is somewhat lower than that of a densified CVD SiO_2 film /9/.

The resistivity of the SOG film, which has a low value that can be compared to that of thermal SiO_2, is attributed to ionic, specifically proton conductivity.

Physical properties of the two examples of the SOG materials, Allied Chemicals Accuglass series 204, and 211 are listed in Table 2.

product	Accuglass 204	Accuglass 211
product type	phenylsiloxane	metilsiloxane
silanol/water content[1]	high	negligible
dielectric constant[2]	9 - 10	< 5
thermal stability	excellent	good
film shrinkage[3], %	10 - 12	8 - 10
resistance to cracking	medium	high
thickness uniformity, %	< 2	
film density, g/cc	2,1 ± 0.1	
resistivity, Ωcm	10^{12} (400° cure)	
breakdown field, V/cm	10^6	
refractive index	1,43 ± 0.01	
pinhole density, 1/cm^2	< 1	
particulate density, 1/cm^2	< 1	

1. after 350° cure
2. after 400° cure
3. between 150°C/60 s bake and 425°C/60 min cure

Table 2. Physical properties of SOG material

3. Planarization

Processing techniques for SOG planarization are basically similar to what is being used in IC processing; while the deposition and curing of SOG are analogous to photoresist processing, the etching of SOG films closely resembles the methods employed for etching CVD oxyde film. However, the most common types of problems encountered in the use of SOG films, particulate contamination, cracking of dielectric layer, poor adhesion, are associated with the deposition and curing of the SOG films, and special spin-on techniques and equipment are used to eliminate them. Spin-on coaters designed specifically for SOG are available commercially.

SOG planarizaton layers have been successfully used in multilayer interconnection processing. Etch-back processes in which most of the SOG layer coated over a CVD dielectric layer is etched away, leaving only a small amount of the SOG meterial in the crevices between metal lines, are firmly established. Conversely, non-etch-back SOG planarization techniques have become more common only recently.

The limited film thickness of the available SOG materials, though not sufficient to allow their use as a stand-alone intermetal dielectric layer, is adequate for planarizing or smoothing a wide range of substrate topographies. The effect of a thin, 3,000 A SOG film on the step (space) profiles at two different structure densities is shown in conceptual illustration, Figure 1.

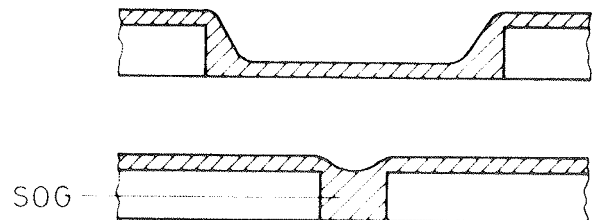

Fig. 1: Conceptual illustration of smoothing and planarization by a thin, 3000 A SOG film deposited over sparse (top) and dense (bottom) structure.

Detailed descriptions of the planarization properties of the spun-on thin films, as important as they are for the integrated circuit processing, are simply not available because of the complexity of the phenomena encountered. One of the most difficult aspects is the effect that the surrounding topography has on planarization. Change in the position, size of topological features, and chemical nature of the underlying films can change the polymer film thickness on adjacent features. To calculate SOG planarization properties from first principles is a difficult rheological problem that has not yet been solved. However, a semi-empirical approach to simulate the spun-on film planarization properties is available /10/ in which the spun-on film is considered to be a low-pass filter for the topography. There is also an extensive literature in which planarizing properties of the SOG films are treated exprimentally /5, 6, 11/. Based on this a qualitative picture of the SOG planarization process, as described below, can be established.

Very little planarization, defined as percent reduction in step height, is obtained over isolated lines or lines separated by 3 to 4 μm wide spaces. However, the 90

degree angle of steps is reduced to about 45 to 60 degrees. This smoothing of the vertical-walled features is quite suitable for conformal deposition of subsequent layers with a high degree of step coverage. At smaller geometries, where the aspect ratio of the space between lines approaches unity, a high degree of planarization is produced by similarly thin SOG films. At such geometries, a mere smoothing effect would not be acceptable. In either case the SOG thickness above the lines is too small to provide interlevel insulation (Figure 2).

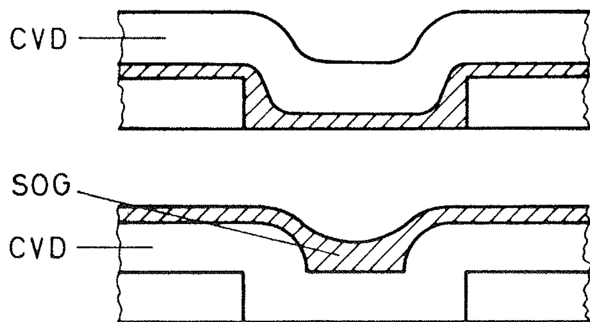

Fig. 2: Two-layer CVD / SOG dielectric structure.

Thus, the SOG planarization processes in use today employ SOG films primarily as a planarizing agent, with the bulk of the dielectric insulation functions provided by the CVD oxide layers. In some schemes, SOG films are used as a sacrificial planarization layer. Four of the more common schemes for planarization with SOG are /11, 12, 13, 14, 15, 16, 17/:

i) CVD / SOG two-layer dielectric
ii) CVD / SOG / CVD sandwich dielectric
iii) Partial etch-back of SOG in a sandwich structure
iv) Total etch-back of SOG

The two layer CVD / SOG dielectric structure shown schematically in Figure 2 is the simplest process of the four. Since the SOG layer is in direct contact with the interconnects in these structures, the SOG must exhibit very good dielectric characteristics. At polysilicon level, this can be ensured by carrying out a high temperature (800° to 900°C) cure of the SOG film, but the structure can not be used as an intermetal dielectric because of the problems associated with the possible chemical reaction between the metal layer and the H_2O emanating from the SOG layer. The order in which the SOG and CVD layers are deposited is a function of the geometry, and the nature of the underlying dielectric layer. In MOS IC fabrication the use of a phosphorus containing SOG material is common for Na^+ gettering purposes.

The use of a CVD / SOG / CVD sandwich structure, illustrated in Figure 3, relaxes the requirements on the dielectric properties of the SOG layer. Moreover, the bottom CVD layer serves to buffer the SOG from the effect of the relatively large thermal expansion of aluminum lines during thermal processing, and, vice versa, protects the aluminum lines from the the oxidizing effects of the SOG. Under certain conditions, as will be discussed later, the presence of the SOG within the via holes etched through the composite dielectric is a potential cause of high via contact resistance. In the partial etch-back sandwich process, shown in Figure 4, the problem is avoided by etching back the SOG layer to a point where it clears the top of the interconnect lines.

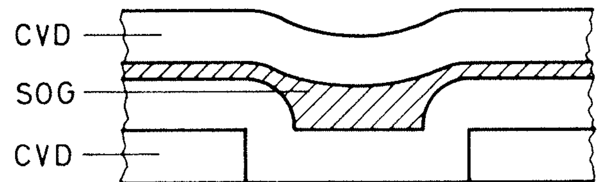

Fig. 3: CVD / SOG / CVD sandwich structure.

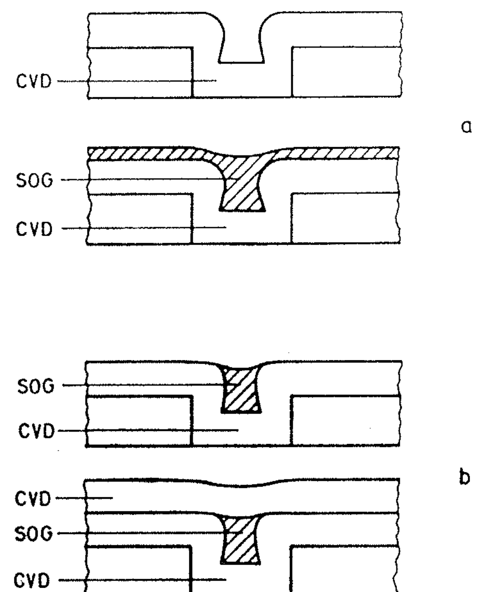

Fig. 4: SOG partial etch-back process; before plasma etching (a), after plasma etching and second CVD oxide deposition (b).

The process is particularly useful at very small geometries, where it is difficult to fill the narrow spaces with SOG material without cracking, or void formation. In such cases a SOG material with low shrinkage characteristics is necessary. The partial etch-back approach allows the use of such a material regardless of its effect on the via contact resistance.

The SOG etch-back process is a sacrificial layer etch-back technique. The use of a SOG as the sacrificial planarization layer offers several advantages compared to, e.g. a resist layer, particularly in the etching step. The etch rates of CVD oxide and SOG are easily matched through simple adjustments of the plasma chemistry. The process control is greatly improved as the plasma loading effects are minimized and the etch chamber is free from organic residues and deposits. The thinner SOG planarization layer does not accumulate excessively in low-lying areas of the chip, thus minimizing via depth variations in the planarized dielectric layer.

The selection of an optimal SOG material and planarization scheme in a given application is dictated by a number of factors including: device geometry, nature of the underlying interconnect, post planarization thermal processes, sensitivity of the device to mobile ion contamination, conformality of the CVD process, and thermal budget available for the SOG cure.

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HYDROGEN PLASMA

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KEY WORDS: hydrogen plasma, plasma generation, plasma characterization, single probes, catalytic probes, low pressure, ionized plasma, weak ionization, plasma tehnologies, plasma types

ABSTRACT: Low pressure weakly ionized hydrogen plasma is introduced. Different modes of plasma generation are presented and some advantages and disadvantages are emphasized. Characterization of plasma by Langmuir probes is briefly described and a recently developed catalytic probe for the measurement of atomic hydrogen density is described more detaily.

Vodikova plazma

KLJUČNE BESEDE: plazma vodikova, generiranje plazme, karakterizacija plazme, sonde enojne, sonde katalitične, pritisk nizek, plazma ionizirana, ionizacija šibka, tehnologije plazme, tipi plazme

POVZETEK: Prikazujemo nizkotlačno šibko ionizirano vodikovo plazmo. Opišemo različne načine generiranja plazme in poudarimo nekatere njihove prednosti in pomanjkljivosti. Na kratko opišemo karakterizacijo plazme z Langmuirjevimi sondami in podrobneje razložimo delovanje katalitičnih sond, s katerimi izmerimo gostoto atomarnega vodika.

1 Introduction

1.1 Some plasma technologies

The term *plasma* has become so frequently used that the old good question *Why should we use plasma?* has been replaced by the question *Is there any way to avoid using plasma?*. Really, plasma technologies have become so commonly used that the solutions of many problems arising in the processing of materials are often found by using some of plasma involved techniques. It was stated that if there was any field of science and technology that has been developing fast in the past decade, it would be the field of surface science and thin film processing. This could have been said also for the field of plasma technologies. Here is a short list of some most commonly used plasma technologies:

- Chemical and physical plasma cleaning
- Plasma etching, plasma ashing
- Sputtering and ion plating
- Plasma enhanced chemical and physical vapor deposition
- Plasma melting and smelting
- Plasma light sources.

1.2 Types of plasma

The term *plasma* was first introduced by I. Langmuir in 1926 /1/ when he studied the positive column of the glow discharge. Later, the term was used for the description of a certain state of gas. Since the original definition of Langmuir, many authors have tried to define the term more or less successfully. The most simple definition of plasma is that it is a partially ionized gas. Since all the gases are actually at least weakly ionized a requirement is stated at once, i. e. the density of charged particles should be rather high, or more physically, the Debye length should be much smaller than the typical dimension of the gas being studied. The Debye length is defined as

$$\lambda_D = \sqrt{\frac{\varepsilon_0 k T_e}{N e_0^2}} \qquad (1)$$

In equation (1), N is the density of charged particles, T_e the electron temperature and ε_0, e_0 and k are the influence constant, electron charge and Boltzmann constant, respectively. It is clear that a very rarefied gas can be described as plasma readily. On the other hand, dense gases can only be treated as plasma if the density of charged particles is very high. An overview of plasmas according to the density of charged particles and the average electron energy is given in Fig. 1.

Different types of plasmas have been divided into two major groups, i. e. thermal and non - thermal plasmas. Clearly, the main difference between the two groups is that thermal plasmas are in thermal equilibrium and non - thermal plasmas are not. More precisely, in thermal plasmas the temperatures of neutral gas, positive ions and electrons are fairly equal and the degree of dissociation is solely a function of the temperature. In non - thermal plasmas the electron temperature is usually more than 10000 K, while the gas temperature is 300 K or so. The positive ion temperature (i. e. the average

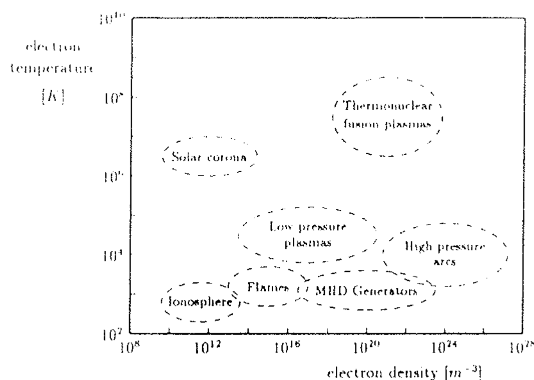

Fig. 1 *Classification of plasmas*

process	onset energy [eV]	max. cross section [$\cdot 10^{-16}$ cm^2]
$H_2 + e \rightarrow H_2^+ + 2e$	15.4	1.1
$H_2 + e \rightarrow H^+ + H + 2e$	18.0	0.005
$H_2 + e \rightarrow H^+ + H^+ + 3e$	46	0.005
$H_2^+ + e \rightarrow H^+ + H + e$	12.4	3-16
$H_2 + e \rightarrow H + H + e$	8.5	0.6
$H_2^+ + e \rightarrow H + H$	0	100
$H + e \rightarrow H^+ + 2e$	13.5	0.65
$H + e \rightarrow H^{\cdot}(2P) + e$	10.2	0.7
$H^{\cdot} + e \rightarrow H^+ + 2e$	3.3	15
$H_2 + e \rightarrow H_2^{\cdot} + e$	10.3	0.2

Table 1: *Some reactions in hydrogen plasma*

random velocity) is often close to the neutral gas temperature. Non - thermal plasmas are frequently used in advanced technologies.

1.3 Low pressure plasmas

Nonthermal plasmas are generated in vacuum systems. The neutral pressure may vary from 10^{-5} *mbar* to 10^1 *mbar*, according to special requirements. The density of charged particles vary from 10^{13} m^{-3} to 10^{20} m^{-3}. The electron temperature is between 104 *K* ($\approx$ 1 eV) and 10^6 K ($\approx$ 100 *eV*). The temperature of positive ions is rarely higher than a few thousand Kelvin. The neutral gas temperature is generally close to the room temperature. The fact that the positive ion temperature is only about 1000 *K* does not mean the ions impacting surfaces are fairly thermal. They may be accelerated in a high potential fall near the surfaces, reaching the (drift) velocity of several 100000 *m/s* (kinetic energy of several *keV*). High energy ions are used in many plasma technologies, such as sputtering, etching, ion plating, etc.

2. Low pressure hydrogen plasma

In the previous section we have stated some characteristics of low pressure non - thermal plasmas. Now we shall pay our attention to hydrogen plasma. Reactions that take place at inelastic collisions between fast electrons and heavy particles (neutral and ionized molecules and atoms) are summarized in table 1.

An important fact is that the onset energy for dissociation is much smaller than the onset energy for the ionization of a hydrogen molecule. Taking into account that the high energy tail of the electron distribution function is exponential (assuming the Maxwell distribution function), one can expect that the density of atoms in hydrogen plasma exceeds the density of charged particles for several orders of magnitude. This is true for most low pressure hydrogen plasmas. The only exception is plasma in tokamaks, where the ECR (Electron Cyclotrone Resonance) generation leads to very high ionization rates.

2.1 Plasma generation

Low pressure hydrogen plasma may be generated in many ways. Here is a list of some.

- Glow discharge. A glass tube with two metal electrodes is filled with gas at the appropriate pressure. A rather high voltage (of the order of several 1000 *V*) is applied between the electrodes. This method of plasma generation is nowadays rarely used since there are quite a few disadvantages, such as intensive sputtering of the cathode, low density of charged particles, low degree of dissociation, poor stability of the discharge, positive ion oscillations (known as striations), and the requirement of the high potential needed for the ignition of the discharge.
- Hot cathode discharge is nice for experimental study of hydrogen plasma, but of little practical importance. The cathode is a hot filament made of thoriated tungsten. The potential between the cathode and the anode is usually less than 100 *V*. The main disadvantage is the requirement of low pressure conditions. The typical pressure is of the order of 10^{-3} *mbar* or less. At higher pressure the ignition and the sustaining of the discharge is difficult.
- RF discharges are most commonly used in plasma technologies and industrial applications. Plasma is generated in a wide range of neutral pressures between 10^{-5} *mbar* and 10^2 *mbar*. At low pressure the ignition of the discharge is limited by the diffusion and the recombination of charged particles on the walls of the discharge vessel. Thus, large vessels are required for the sustaining of the discharge. The high pressure limit is determined by the output power of the RF generator. By the use of powerful generators this type of plasma generation has been extended to

the high pressure regime. The development of the high pressure, inductively coupled plasma torches has been reported /2/. The frequency of the RF generator is usually 13.56 *MHz* or a close harmonious. Plasma is coupled either capacitively or inductively. In the case of capacitively coupled discharge, the RF potential is applied between planar electrodes, while inductively coupled discharges are generated by using a coil. Capacitively coupled plasmas are generated in cases high drift velocity of ions at the electrode is needed, while inductively coupled plasmas are applied in the cases plasma is only a source of chemically active (thermal) particles. The RF discharges are applied in several modes including the popular magnetron discharges.

- MW discharges. A nice way of avoiding the high pressure troubles of RF discharges is the use of microwave discharges. Plasma is generated in a resonant cavity. The wavelength of microwaves is of the order of a **cm**, and that is the typical dimension of the resonant cavity. The MW plasmas are used, for instance, in the production of diamond films.
- Other discharges. They include the ECR (Electron Cyclotrone Resonance) and laser discharges. Their application is limited by the high cost of the equipment.
- Combination of discharges. In all the cases of plasma generation mentioned above plasma parameters depend on the power of the source and cannot be varied independently. However, in practical application it is often required that one of plasma parameters is changed while the others remain constant. In these cases it is advisable to combine two or more different means of plasma generation. The RF discharges are, for instance, often combined with the glow discharge. The RF field causes a rather high ionization rate of gas, while the energy of positive ions impacting the cathode is rather well controlled by the DC potential of the glow discharge. The combination of the hot filament and the glow discharge is efficient in some applications as well /3/.

3. Plasma characterization

3.1 Plasma parameters

Starting at the definition that plasma is a mixture of three types of ideal gases, i. e. the neutral gas, the positive ion gas and the electron gas, the state of plasma is well described, if the densities and the temperatures of the three gases are known. Usually, the density of neutral gas is much higher than the density of charged particles, so it can be easily determined by a vacuummeter. The temperature of neutral gas is also easily determined by a thermometer. The temperature of positive ions is often close to the neutral gas temperature, and since its density is equal to the electron gas density, one often describes the state of plasma by knowing only two plasma parameters, i. e. the density and the temperature of electrons. These parameters may be determined by the use of different electrical probes.

3.2 Single electrical probes

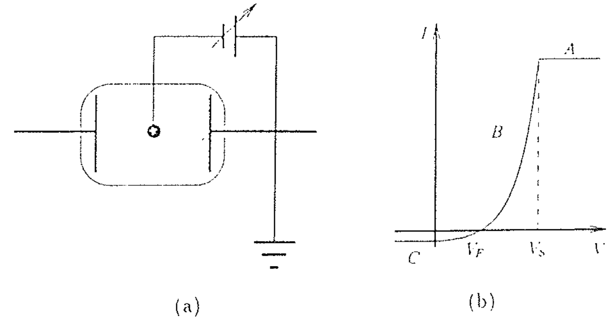

Fig. 2: Electrical circuit of a single probe (a) and its characteristic (b)

A single electrical probe is a small metal electrode immersed into plasma and connected to a variable voltage source, as shown in Fig. 2(a). The density and the temperature of electrons can be calculated from the probe characteristics, which is shown in Fig. 2(b).

When the probe is at the plasma potential, the net current on the probe is the sum of the electron random current and the positive ion random current. Since the positive ion current is much lower than the electron current it can be neglected. Speaking in terms of equations

$$I(V = V_S) = \frac{1}{4} N \, \overline{c_e} \, e_0 \, A_p \qquad (2)$$

Here, N is the electron density in plasma, $\overline{c_e}$ the mean random velocity in plasma and A_p the probe area. In the case electron distribution function is maxwellian, the current on the probe at the plasma potential is

$$I(V = V_S) = N e_0 A_p \sqrt{\frac{k T_e}{2 \pi m_e}} \qquad (3)$$

where T_e is the electron temperature and m_e its mass. The equation (3) gives the relation between the density and temperature of electrons. If we want to evaluate each of them, one must be determined separately. This may be done as follows. In section B on the characteristics (see fig. 2(b)) the electron current rises steeply with increasing potential. If the electron distribution function is maxwellian, this part of characteristics is exponential and we obtain

$$I(V_F < V < V_S) = I_0 \exp\left(\frac{e_0 (V_s - V)}{k T_e}\right) \qquad (4)$$

A plot of $\ln(I)$ *vs* V is linear with the slope of $-e_0/kT_e$, so we can calculate the electron temperature. Once T_e is

known the density of electrons is calculated using the equation (3).

3.3 Catalytic probes

Single electrical probes are commonly used tools which give information on the plasma density and the electron temperature. However, they cannot determine other plasma parameters, the most important being the density of atomic hydrogen. This could have been determined only by the use of expensive detecting machines. Recently, however, we have developed a somehow changed probe, which gives straightforward data on the density of atomic hydrogen.

In order to make measurements of atomic hydrogen density, an electrical probe must be made as follows. The disc should be made of a metal with a high recombination coefficient for the reaction $H + H \rightarrow H_2$. Instead of the leading wire, a pair of thermocouple wires should be connected to the disc.

When a probe is immersed into the hydrogen plasma, the temperature of the disc rises substantially over the ambient temperature because of the energy dissipated on its surface due to the recombination of hydrogen atoms. At the recombination process, an amount of energy equal to the dissociation energy of a hydrogen molecule is released. The density of random flow of hydrogen atoms on the disc surface is

$$j = n \sqrt{\frac{kT}{2 \pi m}} \tag{5}$$

where n is the density of atomic hydrogen in the vicinity of the probe, T is the temperature of the surrounding gas and m is the mass of a hydrogen atom. The energy dissipated on the disc in a unit time is

$$P = n \sqrt{\frac{kT}{8 \pi m}} \gamma W_D A_p \tag{6}$$

Here, γ is the recombination coefficient /4/, W_D the dissociation energy of a hydrogen molecule and A_p the total area of the disc, i. e. $A_p = 2 \pi r^2$.

Since the temperature of the surrounding gas is lower than the temperature of the probe, it is cooled through the processes of radiation and thermal conduction of the surrounding gas:

$$P_1 = (1 - a) \sigma \left(T_p^4 - T^4\right) A_p, \tag{7}$$

$$P_2 = \frac{3pk \alpha \left(T_p - T\right) A_p}{\sqrt{4 \pi k T m}} \tag{8}$$

Here, a is the reflection coefficient, α the accommodation coefficient, T_p the temperature of the probe and p the total pressure. Cooling of the disc through the thermocouple wires has been neglected since the wires are very thin. In the thermal equilibrium the heating of the disc is equal to the cooling so we can write $P = P_1 + P_2$ or

$$n = \frac{(1 - a) \sigma \left(T_p^4 - T^4\right) A_p}{\sqrt{\frac{kT}{8 \pi m}} \gamma W_D A_p} + \frac{3 p k \alpha \left(T_p - T\right) A_p}{\sqrt{4 \pi k T m} \sqrt{\frac{kT}{8 \pi m}} \gamma W_D A_p} \tag{9}$$

The density of atomic hydrogen in the vicinity of the probe can be calculated using the equation (9). However, the equation (9) includes not precisely determined constants, such as the reflection and accommodation coefficient, so it is better to determine the cooling experimentally. When the plasma is extinguished for a few seconds, the temperature of the disc decreases with time. The first derivation of the $T_p = T_p(t)$ curve is a measure of the disc cooling:

$$P_1 + P_2 = M c_p \frac{dT}{dt}. \tag{10}$$

Here, M is the mass of the disc and c_p its specific thermal capacity. The thermal equilibrium equation is simplified:

$$n = \frac{M c_p \frac{dT}{dt}}{\sqrt{\frac{kT}{8 \pi m}} \gamma W_D A_p}. \tag{11}$$

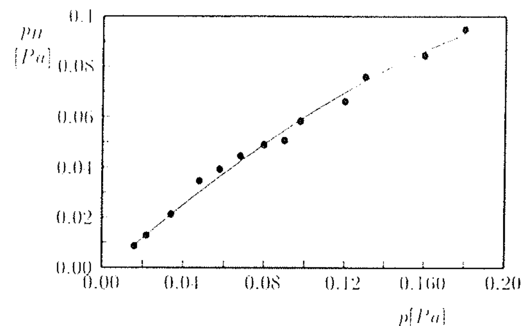

Fig. 3: *Partial pressure of atomic hydrogen vs total pressure.*

The density of atomic hydrogen is thus determined as follows: When a probe is immersed into the hydrogen plasma, the temperature rises until it reaches the constant value at the thermal equilibrium. This takes between one and several hundreds of seconds, depending on the density of atomic hydrogen and the mass of the disc. When the thermal equilibrium is reached, the plasma is extinguished for a few seconds and the measurement of the $T_p = T_p(t)$ curve is performed. The density of atomic hydrogen is then calculated using the equation (11).

The probes have been used to determine the density of hydrogen atoms in the reaction tube of a high vacuum system which we use for studies on the reduction of metal oxide thin layers at low temperature /5/. The

reaction tube was connected to an atomic hydrogen source, which is low pressure inductively coupled RF hydrogen plasma. The probe was a nickel disc with the radius of 1*mm* connected to thermocouple wires chromel - alumel with the radius of 0.012 *mm*. The density of atomic hydrogen was measured at different total pressures between 0.02 *Pa* and 0.2 *Pa*. The result is shown in Fig. 1. It is evident that the degree of dissociation of hydrogen remains constant in this pressure range having the value of about 60%.

4. Application of hydrogen plasma

Besides the use of hydrogen plasma for studies in controlled fusion, its most important application is in discharge cleaning of oxidized metal surfaces. Atomic hydrogen, which is produced in plasma, readily reacts with impurities chemically bonded in surfaces. By these reactions impurities such as oxides, chlorides, sulphides can be completely removed from the surface layer of samples treated by plasma. A very nice example of the efficiency of hydrogen plasma treatment is the discharge cleaning of old silver coins. Fig. 4 represents the composition of the surface layer of a coin before (a) and after (b) the treatment.

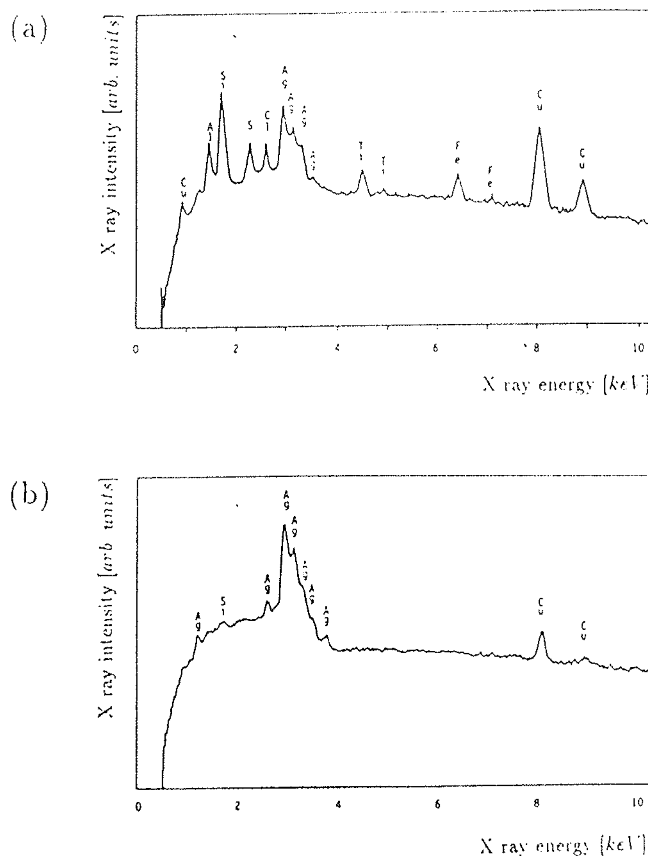

Fig. 4: Composition of the surface layer of a silver coin before (a) and after (b) hydrogen plasma treatment.

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HIGH TEMPERATURE METALLIZATION, ALUMINA GRAINS AND INTERGRANULAR VOLUME MODELLING

I.Belič, L.I.Belič

KEY WORDS: metal-ceramic seals, seal adhesion strength, hight temperture metalization, MoMn metalization, alumina microstructure, Al_2O_3 grain erosion, intergranular volume, ceramic grains, methematical models, grains models, computer models, 3D models

ABSTRACT: It is well known that the alumina microstructure highly influences the quality of the metal - ceramic high vacuum seals. The difference between metallization of fine and coarse grained alumina manifests in different seal adhesion strengths /1/. In the present paper the study of high temperature MoMn metallization of the debased 96% Al_2O_3 is presented. A strong adhesion of metallizing layer on alumina is possible only if enough glass phase is present in bonding layer. In the fine grained alumina sample we could not detect sufficient glass phase in the bonding region between alumina and metallizing layer and the adhesion is expectantly low. The loss of a glass phase in the fine grained alumina can be explained by the comparatively greater intergranular volume that is to be filled with glass phase. During the intergranular glass phase diffusion from metallizing layer in alumina, glass erodes the Al_2O_3 thus producing the new - bigger intergranular volume. The glass phase migration in alumina was observed by tracing the manganese diffusion. In order to simulate the behavior of the intergranular volume in alumina as the function of the average alumina grain size the 3D mathematical model was proposed and evaluated by computer. In the presented model the physical alumina grains are replaced with the modelled grains. The erosion process is modelled and the intergranular volume is calculated for the different erosion depths and different alumina microstructures.

Visokotemperaturna metalizacija, model za izračun zrn keramike in intergranularnega volumna med zrni keramike

KLJUČNE BESEDE: spoji keramika-kovina, trdnost spojev, metalizacija visokotemperaturna, MoMn metalizacija, mikrostruktura keramike korundne, erozija zrn Al_2O_3, prostor med zrni, zrna keramike, modeli matematični, modeli zrn, modeli računalniški, modeli 3D trodimenzionalni

POVZETEK: Iz literature je dobro znan pojav, da mikrostruktura keramike vpliva na lastnosti spoja med keramiko in kovino. Razlika pri metalizaciji grobo in drobno zrnate keramike je v natezni trdnosti spoja /1/. Vakuumsko tesen in trden spoj narejen s 96% Al_2O_3 keramiko nastane le v primeru, kadar je količina steklaste faze v vezni plati med keramiko in metalizacijsko plastjo dovolj velika. Primankljaj taline v vezni plasti drobnozrnate keramike povzroči slabšo trdnost spoja. Ta pojav pojasnjujemo z večjim intergranularnim volumnom med zrni Al_2O_3, ki ga zapolni talina iz vezne plasti. Intergranularni volumen nastane z raztapljanjem zrn Al_2O_3 med difuzijo modificirane taline v keramiko. V delu je predstavljen matematični model za izračun intergranularnega volumna ob upoštevanju različne zrnavosti keramike ter erozije zrn z modificirano talino. Novost predstavljenega modela so tudi zrna, ki so narejena v tridimenzionalnem prostoru.

INTRODUCTION

The metallization process of high alumina ceramics has been the object of many studies. Generally the seals are phenomenologically well understood. The most common metal - ceramic combination are molibden - alumina seals. A typical fabrication process consists of coating a part of alumina surface with MoMn paste. The coated ceramics is fired at a temperature between 1200°C to 1500°C in a moist hydrogen containing atmosphere. During the firing of metallizing paste the intergranular - glass phase from the debased alumina begins to migrate into the porous metallizing layer. The glass phase composition determines the temperature at which seals could be produced /2/. For the glass migration mechanism Twentyman /3/ proposed the twin capillary model in which the direction of the glass phase penetration is a function of capillary pressure between grains in alumina and in metallizing layer.

After firing the sintered coating is plated with thin layer of solderable metal, such as nickel and in the last step join the nickel plated MoMn surface with the metal part by brazing.

Systematic studies of ceramic - metal interfaces have started in the early 1960. The results of this studies were published and cover the topics of thermodynamic reactions, wetting phenomena and the work of adhesion. Chemical reactions between metal and ceramics are considered to be the set of equilibrium thermodynamics reactions. They include redox and dissolution reactions with and without the assistance of a moisture reducing gas. The wetting and contact angle are very significant properties in the metal ceramic seals forming. The glass wets the partially sintered molybdenum and enables adherence between ceramics and MoMn coating. The wettability by solder is also very important in brazing process when nickel plated metallizing layer has to be joined to a solderable metal part.

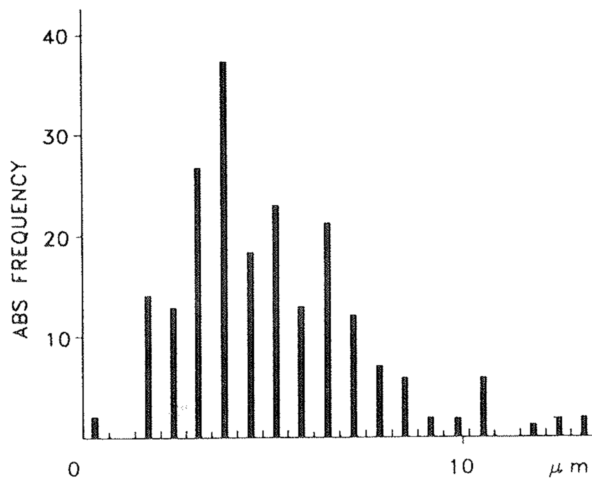
The understanding of physical interaction between metallizing layer and ceramic is not sufficient. The kinetics of metal - ceramic reactions are scarsely documented /4/.

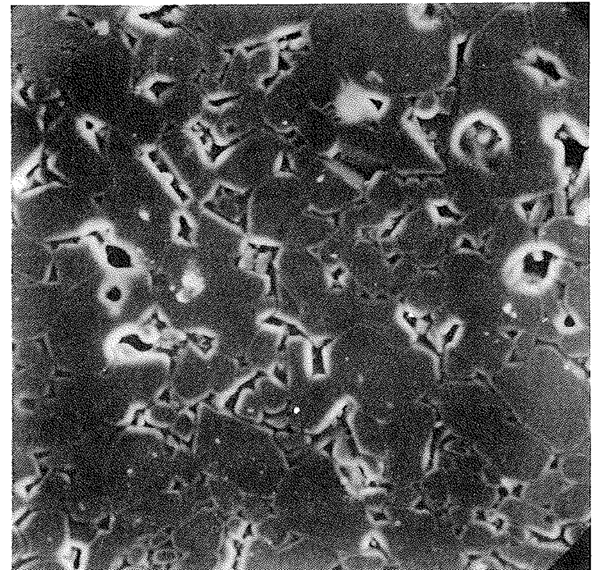
Seal strenght and vacuum tightness are very significant parameters from the commercial point of view.

Floyd /5/ found out that the seal strength depends on the glass phase type present in alumina. The same author also found out that the seal strength increases with metallizing temperature. Floyd and many others reported the empirical relationships between the seal strength and alumina grain size. The present paper proposes the possible answer to these phenomena.

EXPERIMENTAL

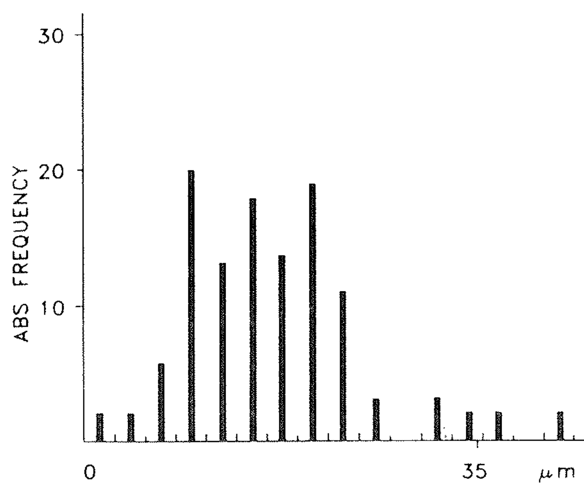
The fine (median diameter 4 µm) (Fig.1) and coarse (median diameter 16 µm) (Fig.2) type of debased alumina have been used. The alumina grain size arangement was determined on polished and thermally etched sam-

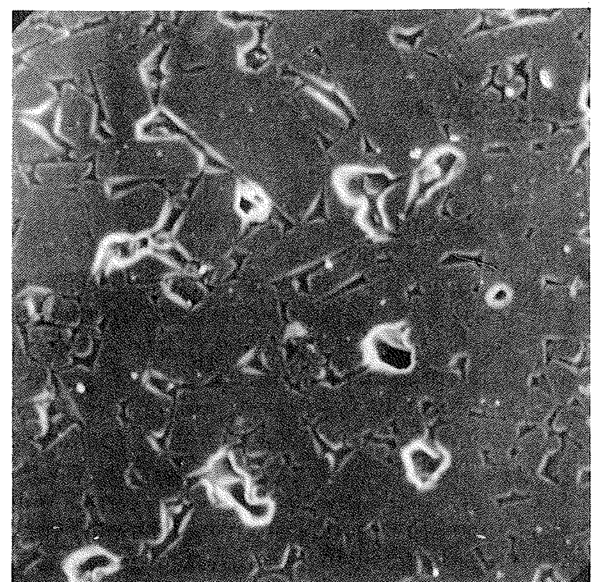




10µm

Fig. 1: *Microstructure of thermally etched fine grained alumina a.) Corespondent grain size distribution function.*





20µm

Fig. 2: *Microstructure of thermally etched coarse grained alumina a.) Corespondent grain size distribution function.*

ples. The MOP CONTRON M-15 device with equivalent spherical diameter method was used for alumina grains size distribution determination (Fig 1a., 2a.). The metallizing paint was produced from 80 wt.% molybdenum powder, 16 wt.% manganese, and 4 wt.% FeSi. The metallizing firings were carried out in 75 %N_2 + 25% H_2 atmosphere at various temperatures. Firing temperatures were in the range from 1250°C to 1450°C, furnace humidity was at a dewpoint at +25°C. The metallized samples were then coated with a thin layer of a nickel oxide paint. The reduction of nickel oxide occured in dry hydrogen at 950°C. The test pieces were brazed with silver-copper eutectic alloy. The brazing process was performed in dry hydrogen.

Depth distribution of manganese in boundary region and in alumina was detected with a WDX microanalyzer by shifting the specimen under stationary electron beam.

RESULTS AND DISCUSSION

Manganese is an additive to high temperature metallizing paste. During firing in wet reduction atmosphere the Mn oxidizes to MnO (ΔG = -137.000 kcal/mol) /6/ and reacts with the glass phase from alumina. The new - modifed glass has the lower melting temperature /4/ and is less viscous. This glass enables the bound formation between alumina and metallizing layer. It fills the porous metal layer and migrates in the debased alumina. The modified glass migration in alumina passes intergranulary. The alumina microstructure determines physical and chemical properties of the seal /7/. The bonding layer in strong and vacuum tight seals consists of a dense metal/glass layer. The effect of alumina microstructure manifests in different adhesion strengths, which are higher at coarse grained alumina, while at the fine grained samples adhesion is low. The reason for the low adhesion strength at fine grained alumina is, that almost the whole glass migrates from the bonding region into alumina, leaving no adhesive substance to keep the Mo cermet layer and alumina together.

The depth diffusion of modified glass was observed by tracing the manganese diffusion. The diffusion process is highly temperature dependent and starts at cca. 1250°C. At 1450°C (30 min) the diffusion depth of modified glass reaches approximately 900 μm.

For fine and coarse grained alumina types at the same coating thickness and at the same metallizing temperature the Mn diffusion depths were approximately the same. Glass diffusion depth is therefore considered to be indipendent on alumina grain size.

During modified glass diffusion into alumina this glass erodes alumina and produces larger intergranular volume (Fig.3). Newly emerged intregranular volume must be filled by the glass phase from ceramic - metallization interface to form strog seals. If there is not enough glass

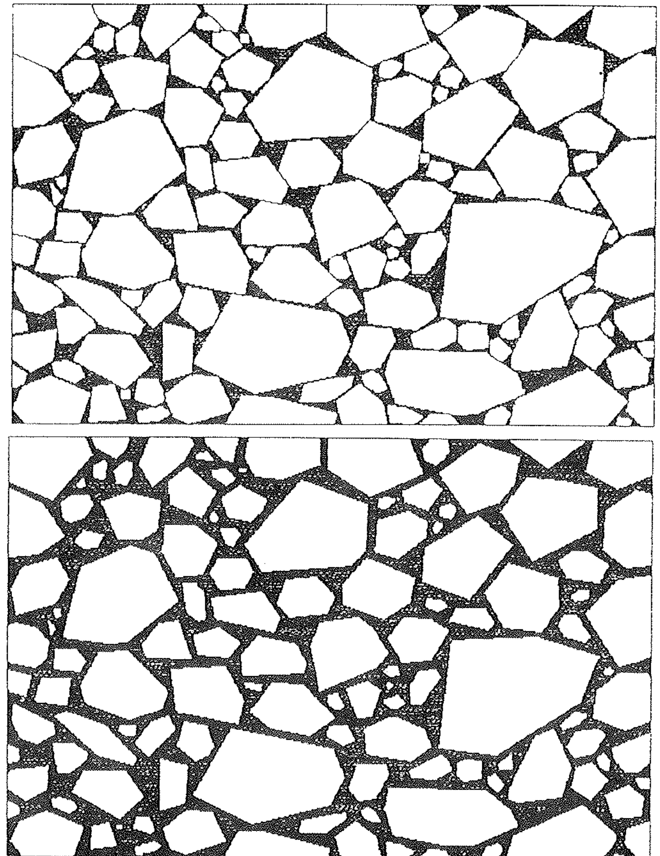


Fig. 3: Computer simulation of alumina microstructure a.) before erosion b.) after erosion.

phase to fill the intergranular volume the seal strength decreases /7/.

The three dimensional computer model explains the behavior of the intergranular volume in alumina as the function of alumina grains size distribution. The model also simulates the effects of alumina grains erosion during the sintering process.

The modelling process undergoes several steps as:

- model alumina grains generation
- tossing generated grains in the unit volume according to the grains size distribution function (distribution function was previously measured on real alumina)
- intergranular volume calculation
- grains erosion

By repeating the last two steps the functional dependence of intergranular volume versus erosion depth (firing time) is calculated.

THE ALUMINA GRAIN MODELLING AND GRAINS VOLUME CALCULATION

The grain is the elementary alumina construction block. The modelled grain shape must be as close as possible to the real alumina grain shape. It must be mathematically easy representable and the grain volume calcula-

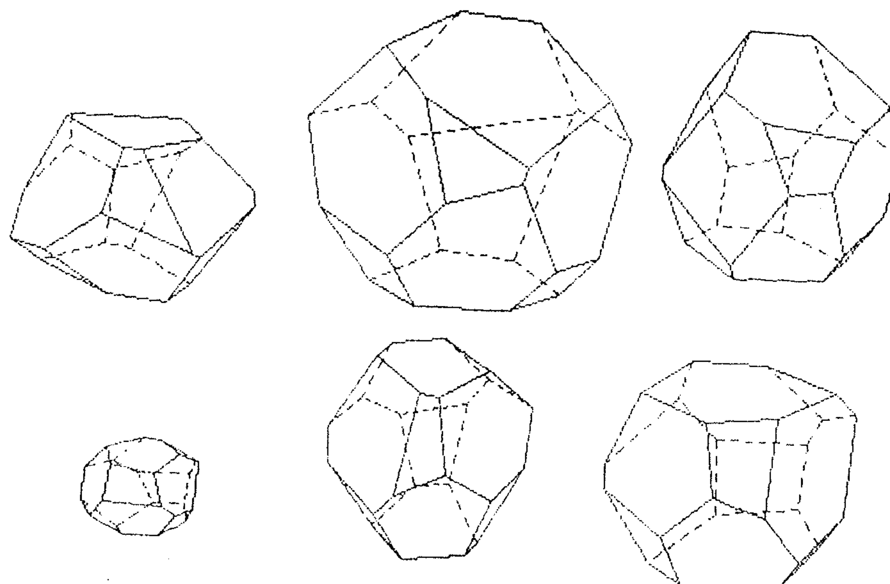


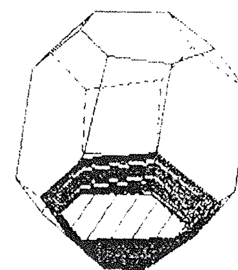
Fig. 4: Randomly generated 3D alumina grains.

tion algorithm must be efficient. The shape that fulfills these conditions is the tetrakaidecaedra /8/. The early studies in alumina moddeling showed us that inproper alumina grain shape selection leads to wrong results /9/. For example the spheras offer very easy and efficient calculations, but the inergranular volume versus grains volume ratio is too high comparable with real alumina. The sphera shape is too far away from real alumina grain shapes.

In order to create the set of different grains the basic shape (tetrakaidecahedra) is modified in process using pseudo random generator. The tetrachaidecahedra is mathematically defined by 14 border planes. For all border planes the planes orthogonal vectors and the vectors starting points coordinates are known.

The deformation is obtained by tilting the planes that define the form for some spatial angle. Of course the spatial angle must be chosen randomly in order to get different "grain" shapes. Border planes tilted for some angle intersect in different edges as they would be in the case of the regular form are thus creating the form of different shape and volume. Fig.4 presents two examples of random generated 3D grains.

Grain volume can be very effectively calculated by the slicing algorithm, where the grain is cut in the number of parallel cuts (Fig.5). For each cut the volume is calculated and the slices volumes sum over the whole grain is the grain volume.



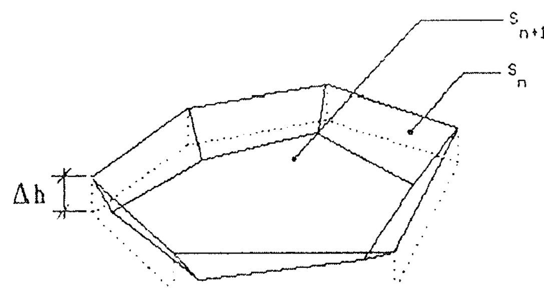


Fig. 5: The volume calculation uses the slicing

THE GRAINS SIZE DISTRIBUTION FUNCTION

The alumina consists of grains where the size distribution can be very accurately measured on the real alumina samples (Fig. 1a, 2a). The grains generation process generates grains of different sizes acording to the experimental distribution function. The intergranular volume is always calculated in the constant (unit) volume. In our case the constant volume is one - 1 mm^3.

For the intergranular volume calculation process it is neccessary to know the exact number of alumina grains in the unit volume.

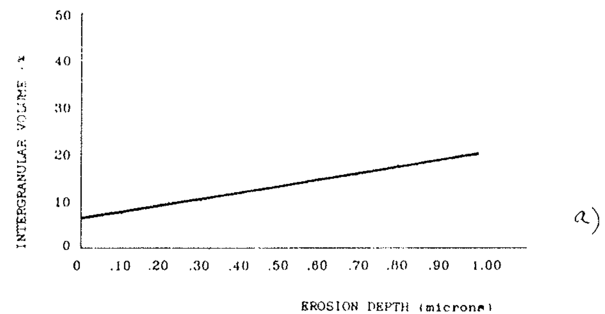
In present model the average grain size was used for calculation of the number of grains in constant volume. This assumption turned out to be good enough for our work.

When the number of the grains in the unit volume is known, grains are generated according to the given distribution function, the volume is calculated for each grain and at the end the total grains volume is subtracted from the unit volume.

THE GRAINS EROSION PROCESS

During intergranular glass phase diffusion the modified glass (containing MnO) erodes the Al_2O_3 grains /10/. The next step in simulation is the grains erosion process. This means that each and every grain is eroded for the same thickness.

Every single grain is eroded for the same depth (0.01 micron) in one computation step. For each step the computer calculates the intergranular volume in the unit volume. Fig. 6a and 6b show the diagrams of percentage of intargranular volume as the function of erosion depth. The given samples represent the erosion process at coarse and fine grained alumina. Those two examples are the proof of the theoretical asumption that the intergranular volume in fine grained alumina increases fast with the erosion depth. This intergranular volume increase is one of the reasons for the glass phase difficiency and therefore for the low seal adhesion strength. In fig. 6a and 6b it is necessary to point out the fact that the starting intergranular volume in the unit volume represents almost the same percentage of the total unit volume at both alumina types. The difference in the grains size distribution functions is not so drastic to have any significant influence on the starting intergranular volume. Even if the starting intergranular volumes are almost the same at both alumina types the erosion process simulation shows obvious difference at both alumina.



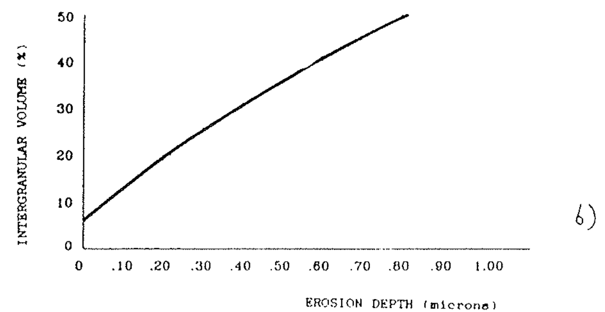


Fig. 6: Functional dependence of intergranular volumes versus erosion depth for a.) coarse grained alumina, b.) fine grained alumina.

EXPECTATIONS

The model turned out to be very succesfully designed and the results obtained with this model represent the proof of our theoretical speculation for the cause of a low adhesion strength at fine grained alumina.

The 3D computer simulation was developped in order to make the practically usefull tool in the designing the ceramic metal bonding techniques. The model with simulation should predict the amount of the glass phase needed for the particular alumina type. The simulation must be thoroughly tested with practical experiments.

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LOGIC NEURAL NETWORKS FOR A CHARACTER RECOGNITION PROBLEM

J. Ficzko, A. Dobnikar

KEYWORDS: logic neural network, pyramidal architecture, optimal architecture, a-algorithm, GHA Generalizeg Hebbian Algorithm, pattern recognition, character recognition, Alexander pyramida, system comparison, comparison of results

ABSTRACT: The paper presents a comparison between the recognition performance of logic neural networks for different pyramidal architectures and different basic elements of pyramids. The capabilities of Aleksander's pyramids /1/ do not reach those of the architecture based on the Generalized Hebbian Algorithm. The later depends on statistical features of patterns .

Logične nevronske mreže za problem razpoznavanja znakov

KLJUČNE BESEDE: mreže nevronske logične, arhitektura piramidna, arhitektura optimalna, a-algoritem, GHA Hebbian algoritem posplošeni, razpoznavanje vzorcev, razpoznavanje znakov, Alexander piramida, primerjava sistemov, primerjava rezultatov

POVZETEK: V članku je podana primerjava rezultatov razpoznavanja znakov z različnimi logičnimi nevronskimi mrežami za različne piramidne arhitekture in različne gradnike piramid. Osnovne Aleksandrove /1/ piramide po svojih zmožnostih ne dosegajo optimalne piramidne arhitekture, ki je določena na osnovi posplošenega Hebbovega algoritma. Ta arhitektura se prilagaja statističnim značilnostim vzorcev, zato so rezultati razpoznavanja po tej poti bistveno boljši.

1. Introduction

In pattern recognition problems the dimensionality of input data is often of order 100 or more. When using neural networks, we face with the problem of having large number of inputs per neuron in the first layer. This practicaly disable the hardware realization of neural network. Therefore we want to find the architecture with a limited connectivity between the input and the first layer of the neural network. We were looking for such architecture in two ways. First we tried to use the pyramidal architecture introduced by Aleksander /1/. It is composed of logic nodes (PLN or G-RAM) with reduced connectivity towards input layer that can be easily realized by RAM elements and some additional logic. Secondly we were looking for the architecture that depends on input data. As the Generalized Hebbian Learning Algorithm performs feature extraction by limiting the weight vectors of the 1st layer neurons toward the eigen vectors of the receiptive input field of the pattern we used this type of a layer as the second alternative.

The paper is organized in three parts. In the first part the data set for a character recognition problem is introduced.

In the second part the comparative results (number of necessary learning cycles, recognition rate) of Aleksander's pyramids - for a different architectures, different basic elements and consequently different learning algorithms are presented.

The pyramidal architecture based on GHA is introduced in the third part together with the testing results for a character recognition problem.

Conclusion finally gives a comment and a suggestion for further work.

2. The data set for a character recognition problem

The data set for a character recognition problem is composed of characters obtained from the scanner. Characters are taken from OCR font (digits from 0 to 9 and delimiters "S" and "h"). The data consists of 15 samples for each class, so the total is 180 characters. For learning purposes 10 samples of each class were used, so 5 samples of each class were available for testing. This data set was used with pyramidal architecture based on GHA.

Observing the recognition rate of Aleksander's pyramids, the ideal representatives for each class were chosen as training set. The testing samples were obtained by adding some amount of noise to the training set. The testing set T1 consists of samples that are in 1 bit different from learning samples, T2 consists of samples that are in 2 bits different from learning samples and T3

of samples that are in 3 bits different from learning samples. Such a learning set was used because of inability, in sense of capacity, of Aleksander's pyramids to learn the same data set as the pyramidal architecture based on GHA.

In both cases, the samples are 64-dimensional and represent a character on 8 x 8 pixel grid. The GHA pyramidal architecture is used also for 1024-dimension cases that represent a character on a 32 x 32 pixel grid.

3. Pyramidal architectures of logic neurons

Concerning the number of inputs to the first layer of Aleksander's pyramids (n), the number of inputs to one element (N), the depth of the pyramid (D) and relation $n = N^D$, where n = 64, with varying N=2,4,8,16,32,64 (different element at different layers) there are 32 different pyramidal architectures. Out of 32 possibilities we decided for 7 architectures that were used for testing:

- P(64;2,2,2,2,2,2)
- P(64;2,2,4,4)
- P(64;4,4,2,2)
- P(64;8,4,2)
- P(64;2,4,8)
- P(64;4,4,4)
- P(64;8,8)

The number c on the k-th place following ";" means the pyramid with c- input elements in the k-th layer. The selection of 7 pyramids includes all pyramids that have equal elements in all layers, as well as pyramids with different number of layers, where we set the elements with the greatest number of inputs in the first or the last layer.

We used the A learning algorithm (introduced by Aleksander /2/) with PLN elements with 3 possible contents in the first case and the A algorithm with additional spreading phase /3/ with G-RAM elements with 3 possible contents in the second case, where different numbers of spreading cycles were performed.

The comparison between different architectures and different learning algorithms was carried out on the basis of learning speed (number of learning cycles that are necessary to respond to the learning set without an error) and capability of generalizing to the testing set (the recognition error on the testing set).

The speed of learning of the particular architecture did not depend on learning algorithms.

Figures 1., 2., and 3. show the speed of learning where the pyramid P(64;8,8) is the fastest and P(64;2,2,2,2,2,2) the slowest. We find out that the speed of learning directly depends on the total number of memory locations in the pyramid. The greater the number, the faster the speed of learning. The lowest pyramid P(64;8,8) has 2304 memory locations whereas the highest - P(64;2,2,2,2,2,2) 252 only.

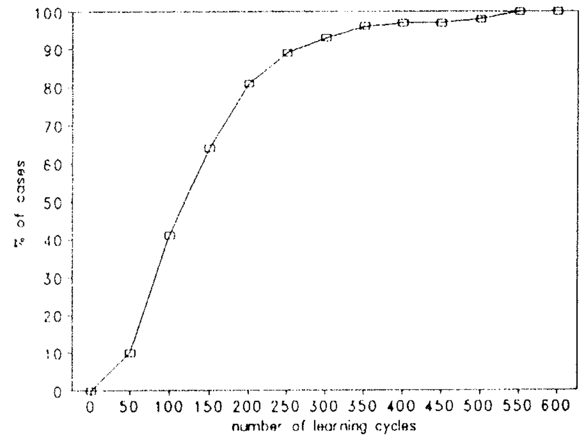

Fig. 1: The speed of learning of P(64;2,2,2,2,2,2)

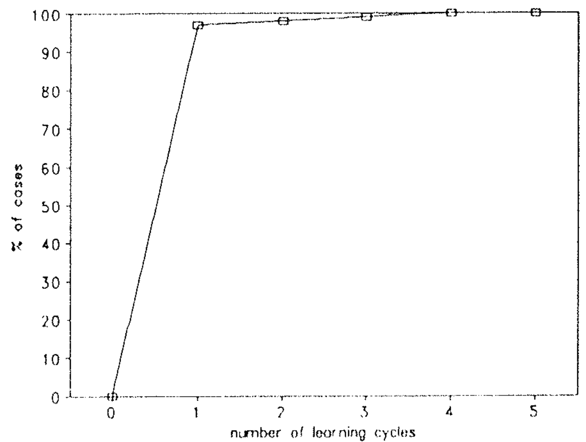

Fig. 2: The speed of learning of P(64;8,8)

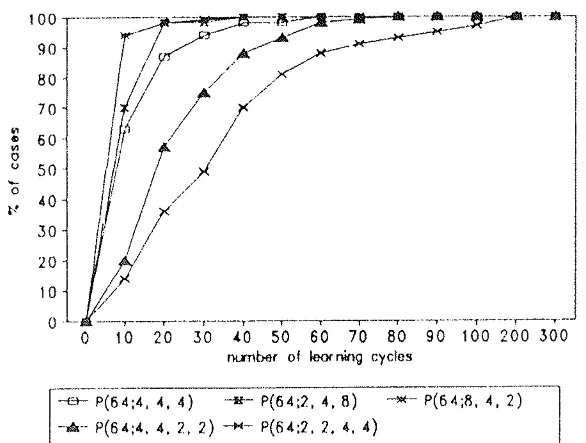

Fig. 3: The speed of learning of P(64;4,4,4), P(64;2,4,8), P(64;8,4,2), P(64;4,4,2,2) P(64;2,2,4,4)

Considering a capability of generalization, it is important to mention when does the recognition error occur. When the input signals address a location with undefined content, the output will be for 50% of time wrong. Therefore, after learning, the number of memory locations that have undefined contents should be as small as possible. The spreading phase carried out after the learning phase reduces the number of memory locations with undefined content. The classification error is therefore in the case of A algorithm with a spreading phase usually smaller than without a spreading phase.

The results shown in Figure 4. for T1 indicate that the highest pyramid P(64;2,2,2,2,2,2) generalizes to the testing set with the smallest error, then follow P(64;2,2,4,4), P(64;4,4,2,2), P(64;4,4,4), P(64;2,4,8), P(64;8,4,2) and the lowest pyramid P(64;8,8) which gives the worst testing results. If the spreading phase is performed, the order of pyramids does not change, but the classification error of the worst pyramid, as well as of the others, is almost equal to the classification error of the best pyramid (see Figure 5.).

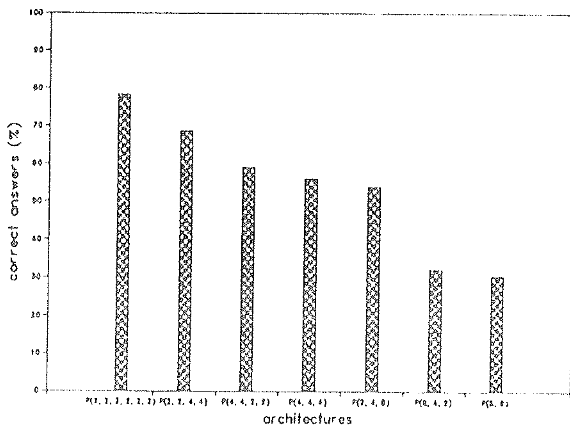

Fig. 4: *Correctly recognized characters from testing set T1 with different architectures implemented with 4 pyramids (spreading phase excluded)*

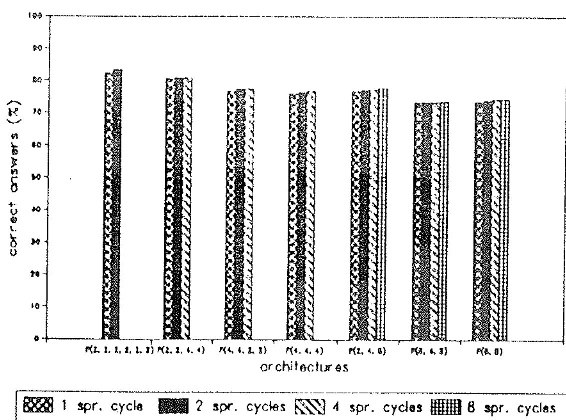

Fig. 5: *Correctly recognized characters from testing set T1 with different architectures implemented with 4 pyramids (speading phase included)*

Although the classification error is reduced by the spreading phase, the results for Aleksander's pyramids with G-RAMs as well as PLN elements are not acceptable. For a real application of a character recognition problem the achieved classification results are not sufficient.

4. The pyramidal architecture based on GHA for a character recognition problem

The problem of pattern recognition could be divided into two phases:

- feature extraction (or feature selection) and
- classification

One of the best known statistical technic for feature extraction is Karhunen-Loeve Transform /4/, which is the numerical intensive problem. The Karhunen-Loeve Transform could be performed iteratively /5/ with Generalized Hebbian Algorithm that is given by equation:

$$w_{ij}(t+1) = w_{ij}(t) + \gamma(t)\left(y_i(t)\, x_j(t) - y_i(t) \sum_{k \le i} w_{kj}(t)\, y_k(t)\right),$$

where learning rate Y(t) corresponds the conditions:

$$\lim_{t \to \infty} \gamma(t) = 0 \text{ and}$$

$$\sum_{t=0}^{\infty} \gamma(t) = \infty.$$

In the case of a single layer network, an optimally trained layer allows linear reconstruction of the inputs to that layer with a minimal squared error.

A neural network that we used for a character recognition problem based upon a GHA is a single layer locally connected neural network with a linear activation function. The whole input field is divided into smaller input fields (we choose N = 4 bits for each field) and the GHA is then performed on every input field independent of other fields. At the beginning two nodes are mapped onto each input field, but considering the output variances (when they fall bellow a certain threshold) some nodes could be removed.

The results of the GHA are used in logic neurons in that way, that information about the connection strength is stored into RAM locations. To do this, an output of every N-bits binary vector (although it may not be a member of the training set) should be computed from weights and stored into appropriate RAM locations. In this way, the response to the input vector, produced by neural network of conventional neurons, is written to the location that is addressed by the same input vector in logic neural

network. Because of a small input size of basic elements (N=4) this operation does not take a lot of time - computing and storing of outputs for only 16-input combination (of 4 bits each) is necessary.

The decision about class-membership of testing examples is based on two decision rules. The first, proposed by /6/, makes use of reference vectors for each class, while the second /7/ classifies a testing example into the class whose class subspace it has the longest projection in terms of the Euclidian vector norm. Both decision rules lead to the similar results, so only results for first decision rule are presented in this paper.

Figure 6. shows a recognition rate (98.8%) of characters on 8 x 8 pixel grid with 2 nodes mapping to the same input field. Removing nodes with small output variances, without reducing the recognition rate could be done only on one (of 16) input field.

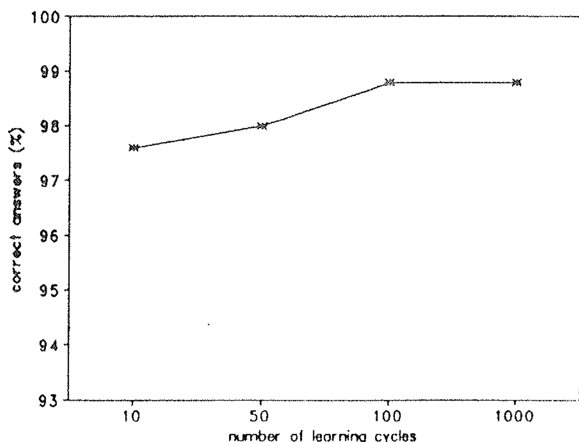

Fig. 6: *The recognition rate of characters on a 8 x 8 pixel grid, with 2 nodes per field*

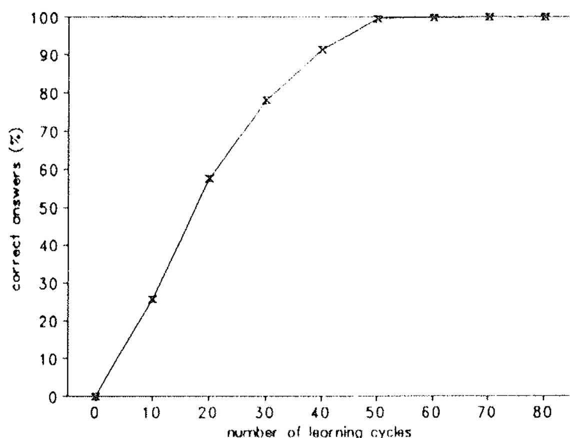

Fig. 7: *The recognition rate of characters on a 32 x 32 pixel grid, with 2 nodes per field*

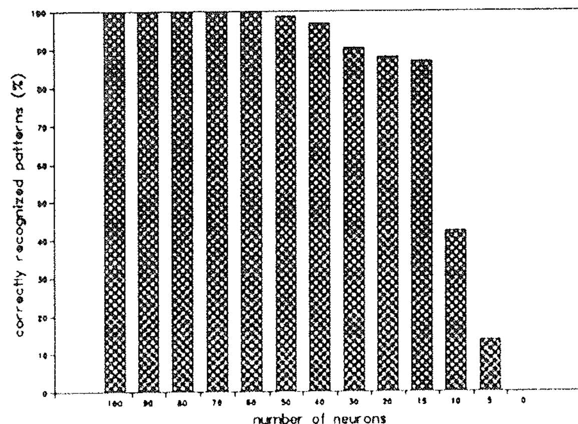

Fig. 8: *The recognition rate of characters on a 32 x 32 pixel grid for different number of nodes in the layer*

The recognition rate (100%) of characters on 32 x 32 pixel grid with 2 nodes mapping to the same input field is presented in Figure 7. Removing nodes with small output variances is very important for this size of a problem. Some input fields do not provide useful information to distinguish between classes, so they can be removed. Figure 8. shows how the recognition rate depends on the number of nodes covering the whole input field.

5. Conclusion

Neural networks for character recognition problems were studied in the paper. We were looking for the architectures that could be easily implemented in hardware. Two suggestions were outlined in the paper. The first one deals with the so called Aleksander' s pyramids and the second one with the layer based on GHA procedure. We showed that only the second approach succesfully follows the requirements regarding character recognition problem. Its hardware implementation is also obtained easily.

The work presented in the paper opens some new problems also. The one we shall try to deal with first is the problem of classification based on eigen vectors that result in the GHA of learning procedure. For the purpose of this paper we used the standard classification method based on minimal Euclidian distance from reference vectors.

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Prispelo: 21.05.93 ***Sprejeto: 15.06.93***

UPORABA POLPREVODNIŠKIH IN MIKROELEKTRONSKIH KOMPONENT

IDENTIFIKACIJSKA KARTICA

UVOD

Brezkontaktna zaznava, identifikacija in elektronsko odpiranje vrat že nekaj časa niso več znanstvena fantastika ampak sedanjost,ne samo v svetu, temveč tudi pri nas. V Iskri smo šli po poti razvoja sistemov nadzora in identifikacije in skupaj s Fakulteto za elektrotehniko in zunanjimi sodelavci razvili sistem SEZAM, ki bazira na brezkontaktni identifikacijski kartici.

Visoka zanesljivost je ključna značilnost nadzornega sistema SEZAM z RF/ID zaznavo kartic. Moderen način zapiranja ohišja kartice omogoča zanesljivo delovanje v času programiranja in ob čitanju kartic, hkrati pa zagotavlja odpornost proti vlagi, neposredni izpostavitvi vodi, prahu ali kemikalijam. Delovanje RF/ID sistema je neobčutljivo na elektro-magnetne udare.Odporen je na udarce in vibracije in odgovarja predpisanim tovrstnim standardom.

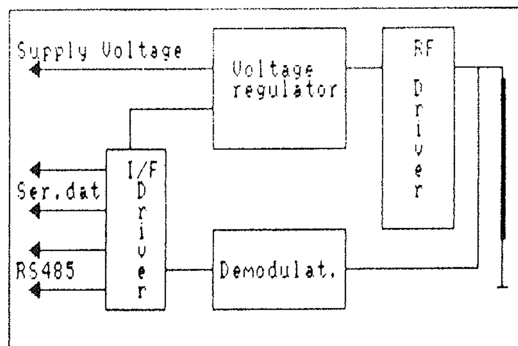
KARTICA

Podatkovni in energijski prenos v induktivnem sklopu z amplitudno modulacijo je zanesljiva in preizkušena metoda in se je v sistemu izkazala kot enkratna kombinacija.Kartica črpa energijo iz visoko frekvenčnega polja, ki ga generira čitalnik. Pri dovolj močnem induktivnem sklopu,ki omogoča čipu kartice zadostno energijo, le-ta prebere vsebino zapisa v PROMu.Vsebino zapisa serijsko posreduje v amplitudnem načinu modulacije,t.j. z dušenjem induktivnega sklopa.Signal vsebuje ponavljajoč vlak impulzov s 64 bitno informacijo in pavzo 16 bitov.Signal je sinhroniziran s 50kHz uro.Takšen način delovanja omogoča zaznavo in zapis vsebine kartice v nadzorni sistem, ki to uporabi kot zapis prisotnosti,komando za odpiranje vrat ali dvig zapore.

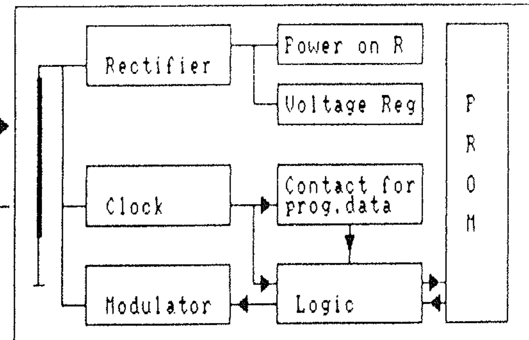
V čipu ID kartice je vgrajeno stikalno polje tranzistorjev s prežignimi elementi,kontrolna logika,napajalno vezje z napetostnim regulatorjem,modulacijsko vezje in visoko frekvenčna primopredajna stopnja ter urni generator.Čip s C elementi je nanešen na keramični hibrid in je z anteno zasnova kartice. Oblikovno je kartica v standardni velikosti, možne so tudi druge oblike, npr.obesek za ključe.

Tehnični podatki za kartico:

- Nosilna frekvenca za prenos podatkov je 13.56 MHz.
- Urni generator za sinhroni prenos podatkov ima 50 kHz.
- Podatki vsebujejo 64 bitno informacijo in 16 bitno pavzo.
- Ponovljivost informacije je na 10 ms.
- Pravilna zaznava je v območju od 0 do 10 cm.
- Induktivno napajanje.
- Deluje v temperaturnem območju od -25 do +70 st C.
- Zaščita proti vodi po IP 67.
- Velikost standardne kartice je 85 x 55 x 3 mm.



Blok diagram citalnika



Blok diagram ID kartice

ČITALNIK

Oddaja energije in sprejem serijske kode sta glavni nalogi analognega dela čitalnika.Čitalnik generira visoko frekvenčno polje in ga oddaja prek antene v prostor.Pri vzpostavitvi induktivnega sklopa s kartico, sprejema čitalnik modulirani signal od kartice. Signal demodulira in ga v obliki serijske kode posreduje procesorju. V primeru, da deluje samostojno, signal primerno oblikuje ter ga prek serijske komunikacije posreduje oddaljenemu procesorskemu delu čitalnika. Za serijski prenos podatkov se uporablja RS485. Čitalnik kartice kot sestavni del RF/ID sistema vsebuje visokofrekvenčno primopredajno stopnjo,demodulator,komunikacijski pretvornik ter napajalno vezje z napetostnim regulatorjem.

Tehnični podatki:

- Generator frekvence za prenos podatkov generira 13.56 MHz.
- Sevalna energija na anteni je 0.1 V/m.
- Čas čitanja je 10 ms.
- Napajalna napetost vezja je 5 V.
- Poraba vezja je 40 mA.
- Komunikacija poteka prek komunikacijskega kanala RS485.
- Velikost analognega čitalnika je 110 x 55 x 15 mm.
- Deluje v temperaturnem območju od -25 do +70 st C.
- Zaščita proti prahu po IP 45.

SEZAM
Sistem za registracijo delovnega časa in kontrolo dostopa

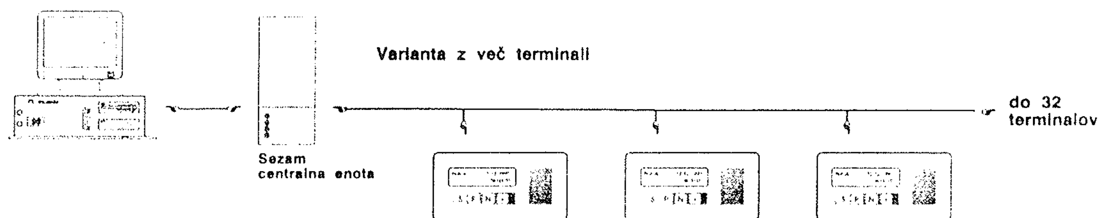
Značilnosti sistema:

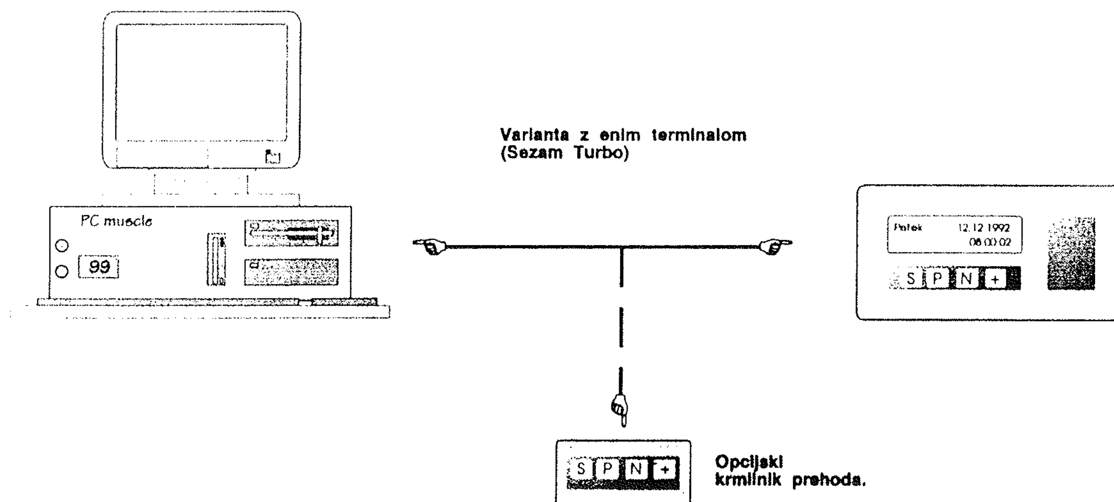
- Registracija delovnega časa
- Kontrola dostopa
- Obdelava podatkov

Namenjen je spremljanju delovnega časa in nadzoru pristopa v določene prostore. Deluje popolnoma samostojno. S sistemom komuniciramo prek PC-AT kompatibilnim računalnikom. SEZAM temelji na brezkontaktni kartici, ki omogoča hitrost in zanesljivost beleženja ter robustnost sistema.To je samostojni sistem z računalniško zasnovo ter ustrezno strojno in programsko opremo.

Le-ta omogoča:

- Pretok podatkov med posameznimi enotami sistema
- Vpis med 1 do 7000 indifikacijskih kartic





- Vnos podatkov časovnih omejitev za 16 različnih tipov dni
- 8 delovnih koledarjev
- Prehode v vseh oblikah, ki jih koristijo delovne organizacije, podjetja, ustanove...
- Posebne izhode in prehode
- Vnašanje, spreminjanje in spremljanje podatkov uporabnikov kartice
- Priprava podatkov za obračun osebnih dohodkov
- Izpis podatkov v najrazličnejših oblikah
- Varovanje podatkov v primeru raznih izpadov napajanja ali napak
- Hitri dostop do vseh podatkov, tudi do podatkov starejšega datuma
- Razširitev uporabnikov kartic na tri organizacijske nivoje
- Možnost vnosa sporočil za posamezne uporabnike kartice
- Avtomatsko računanje ur glede na vnose statistik
- Kreiranje podatkovnih baz
- Testiranje sistema
- Testiranje sistema prek modema na željo kupca

Sistem SEZAM sestavljajo:

- Centralna enota
- Programski paket
- Registracijski terminal s čitalnikom
- Varnostni terminal s čitalnikom
- Krmilnik prehodov
- Dodatni čitalnik
- Krmilje zapornice
- Identifikacijska kartica

Sistem je priključen na omrežno napetost 220 V / 50 Hz.Ima dodatno baterijsko napajanje in omogoča delovanje tudi ob izpadu omrežne napetosti.Terminali imajo vgrajen čitalnik, omogočajo še priključitev dodatnega čitalnika (krmiljenje vrat z obeh strani z enim terminalom) in krmilnika prehoda. Možno je izpisovanje podatkov na zaslon s tekočimi kristali in odaja zvočnega signala ob registraciji.Na terminale je možno priključiti senzorje, krmilijo pa lahko ključavnice in alarmne naprave.

Zgoraj navedene enote in programski paket zaokrožajo sistem. Tako SEZAM z vsemi enotami omogoča zanesljivo delovanje, enostavno spremljanje podatkov in zanesljiv nadzor nad dostopom nadzorovanih prostorov.

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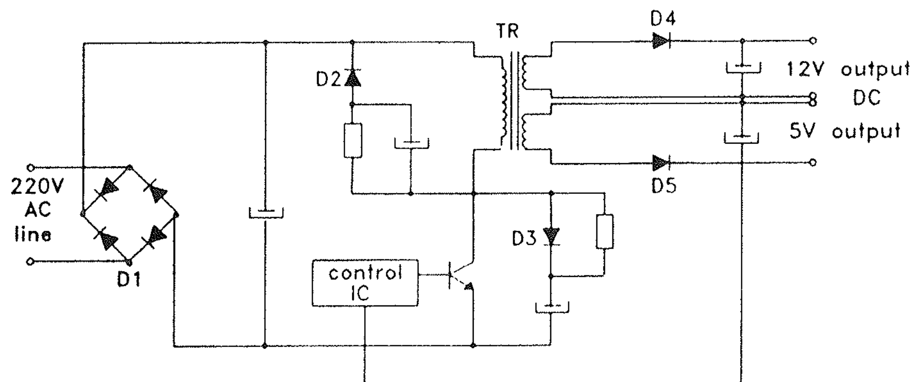
Fast and ultrafast diodes from ISKRA SEMICON

Fast recovery diodes are used wherever high frequency rectification (higher than AC line frequency) is needed.

The biggest use of this diodes is in switchmode power supplies. The switching power supply continue to increase in popularity and is one of the fastest growing markets in the world of power conversion.

They work by choping the rectified AC line at a high frequency 20 - 200 kHz. The input recifier (D1) is generally a standard recovery bridge. In the output section, where high frequency rectifiers are needed (D4,D5), most designers use schottky diodes for the low voltage (5V output) and a fast or ultrafast for higher voltages (12 to 15 V output). High voltage fast recovery or ultrafast



D1 - BRIDGE RECTIFIER: STANDARD RECOVERY
D2 - CLAMP DIODE: FAST OR ULTRAFAST RECOVERY
D3 - SNUBBER DIODE: FAST OR ULTRA FAST RECOVERY
D4 - OUTPUT RECTIFIER: FAST OR ULTRAFAST RECOVERY
D5 - OUTPUT RECTIFIER: SCHOTKY

recovery diodes are recommended for clamp diode and snubber diode (D2,D3).

They are used to limit voltage spikes, if necessary protection may be obtained by transient suppressor diodes.

All personal computers, monitors, TV sets, printers, solar energy regulators, UPS's and modern equipment have switchmode power supply inside. The ratio between diodes which are used in is:

- 25% standard recovery
- 75% fast and ultrafast recovery

The ultrafast is competing all: with the schottky where higher breakdown is needed, with the fast recovery and standard recovery where performance is more important than cost.

Parameter	Schottky	Ultrafast	Fast recovery	Stan. recovery
Uf Forward voltage	0.5-0.6 V	1-1.7 V	1-1.4 V	0.9-1.1 V
trr Reverse recovery time	< 10 ns	25-100 ns	150-500 ns	> 1ms
Ur Reverse blocking voltage	20-60 V	50-1000 V	50-1000 V	50- 1000 V
Cost ratio	3:1	2.5:1	2:1	1:1

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3A 5A DO-27
6A 12A DO-4
20A 35A DO-5
Voltage 50 V up to 1600 V

Fast diodes

1A 1.5A DO-41 t_{rr} = 100 ns - 500 ns
2A 2.5A 3A DO-27 t_{rr} = 100 ns - 500 ns
6A DO-4 t_{rr} = 200 ns - 500 ns
Voltage 50 V up to 1000 V

Ultra fast diodes

1A DO-41 t_{rr} < 75 ns
Voltage 50 V up to 1000 V
3A DO-27 t_{rr} = 75 ns
Voltage 50 V up to 1000 V

Si-rectifier round bridges

0.8A 1A 1.5A
Voltage 50 V up to 1000 V
Fast version t_{rr} < 500 ns

Si rectifier in line bridges

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3.7A 4A 5A
6A 8A
Voltage 50 V up to 1000 V
Fast version t_{rr} < 500 ns

Power bridges

10A 25A 35A
Voltage 50 V up to 1000 V

Low voltage suppressor diodes (bidirectional)

DO-41; DO-27
Voltage 1 V up to 5 V

Stabistor diodes (unidirectional)

DO-41

Transient suppressor diodes

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Voltage 5.5 V up to 97 V
600 W 1500 W DO-27
Voltage 5.5 V up to 97 V

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PRIKAZI DOGODKOV, DEJAVNOSTI ČLANOV MIDEM IN DRUGIH INSTITUCIJ

OSNOVNA PRAVILA MEDNARODNEGA SISTEMA OCENJENE KAKOVOSTI ELEKTRONSKIH ELEMENTOV (IECQ)

1. Naziv

"OSNOVNA PRAVILA MEDNARODNEGA SISTEMA OCENJENE KAKOVOSTI ELEKTRONSKIH ELEMENTOV (IECQ)"
v nadaljnem besedilu : "Sistem"
Skrajšan naslov je : "IECQ"

2. Predmet

Upoštevajoč predmet Mednarodne elektrotehnične komisije, kot je navedeno v poglavju 2 Statuta, je podrobnejši predmet Sistema, ki deluje v skladu s Statutom in pod okriljem IEC, olajšati mednarodni promet elektronskih elementov ocenjene kakovosti v skladu s principi recipročnosti.

Namen je doseči definiranje in izvajanje postopkov WE ocenjene kakovosti v tem smislu, da bi bili elementi, ki se spustijo v promet skladno z zahtevami ustreznih specifikacij, sprejemljivi za vse udeležence.

V tem sistemu je ustrezen standard ali specifikacija ena tistih, ki so v skladu s tč. 12. Ta sistem omogoča postopke za oceno kakovosti elementov, ni pa nujno, da daje zagotovila o skladnosti z varnostnimi zahtevami naprave, v katero se ti elementi vgrajujejo.

3. Področje uporabe

Ta sistem se uporablja za vse elektronske elemente, za katere se zahteva ocenjena kakovost.

4. Vodilni dokumenti

Dokumenti, ki določajo pravila Sistema in ki vodijo delo organizacije, so naslednji:

4.1 a) Statut IECQ,

b) Pravila postopkov IEC in generalne direktive za delo IEC, v kolikor ni drugače specificirano v pravilih postopkov Sistema.

Opomba:CMC (Certification Management Committee - Komite za vodenje certificiranja) ugotavlja, da so pravila postopkov IEC tista, ki določajo tehničnim komitejem IEC, zadolženim za specifikacije,vse njihovo delo po pravilih postopkov IEC ter generalne direktive dela IEC.

4.2 Osnovna pravila definirajo glavne principe Sistema in jih potrjuje Svet IEC

4.3 Pravila postopkov, ki določajo glavno delo postopkov Sistema na obeh nivojih, mednarodnih in nacionalnih. Pravila določa in dopolnjuje CMC v skladu z glasovalnim postopkom, opisanim v tč. 14.2, v soglasju z ICC (Inspectorate Co-ordination Committee - Komite za koordinacijo inšpektoratov) v zadevah, ki se tičejo slednjih. Ti ne smejo biti v nasprotju z dokumenti, navedenimi v tč. 4.1a) in 4.2.

O dopolnilih pravil postopkov Sistema je treba poročati svetu IEC.

4.4 Dokumente postopkov, ki jih pripravlja ICC in ki zagotavljajo enotno uporabo pravil Sistema in enakovrednost nacionalnih postopkov, je potrebno potrditi v skladu s postopkom glasovanja po tč. 14.2 ter tako postanejo del pravil postopka.

5. Način vključitve v Sistem

Predmet Sistema se doseže z naslednjim :

5.1 Ustanovitev primernih mednarodnih in nacionalnih teles za upravljanje in koordinacijo Sistema.

5.2 Pospeševanje priprave in uporabe IEC standardov, ki vsebujejo zahteve, potrebne za delovanje Sistema.

5.3 Priprava in izvajanje pravil postopkov Sistema obsega naslednje :

a) odgovornosti, politiko in organizacijo CMC,

b) odgovornosti, politiko in organizacijo ICC,

c) odgovornosti NAI (National Authorizet Institutions -Nacionalna pooblaščena institucija) in NMI (National Management Institution - Nacionalna vodilna institucija),

d) potrditev NSI (National Supervising Inspectorates -Nacionalni nadzorni inšpektorat),

e) potrditev neodvisnih preskusnih laboratorijev,

f) potrditev proizvajalcev, vključno z njihovimi preskusnimi laboratoriji,

g) potrditev neodvisnih distributerjev, kar zadeva njihovo sposobnost dobavljanja elementov ocenjene kakovosti v skladu s Sistemom,

h) detajliranje postopkov za ocenjevanje kakovosti in dobave elementov ter za podelitev atesta o ustreznosti, kot n.pr. oznaka certifikata, za elemente, ki so bili proizvedeni in dobavljeni v skladu s Sistemom.

6. Nacionalna organizacija

6.1 Nacionalna organizacija, ustanovljena za koordinacijo aktivnosti za ocenjevanje kakovosti elektronskih elementov v državi udeleženki sistema mora biti Nacionalni komite IEC ali telo, ki ga prizna Nacionalni komite IEC. V principu mora izpolnjevati naslednje funkcije :

6.1.1 Za vse države udeleženke

a) NAI, ki jo pooblasti ustrezna nacionalna organizacija (vlada, trgovinska združenja, organizacije za standardizacijo, i.t.n.), deluje kot vodstvo za izvajanje sistema na nacionalnem nivoju; NAI mora biti odgovorna za nacionalno zastopstvo svoje države v Sistemu.

b) Nacionalna organizacija za standardizacijo, ki pripravlja in izdaja nacionalne standarde in druge dokumente, ki niso povezani s Sistemom.

6.1.2 ter dodatno za države, ki izdajajo potrdila

a) NSI, ki je odgovoren za nadzorstvo vseh postopkov za ocenjevanje kakovosti, potrebnih za Sistem in za glavni nadzor v svoji državi v pogledu uporabe atestiranja o ustreznosti. NSI lahko tudi prevzame pod pogoji, določenimi v pravilih postopka, podobno odgovornost za izvajanje Sistema pri elementih, ki so bili delno ali v celoti proizvedeni v državah, ki nimajo NSI.

b) enega ali več priznanih servisov za kalibracijo, ki so lahko v drugih državah udeleženkah, katerim morajo NSI in preskusni laboratoriji poročati o periodičnih verifikacijah merilnih standardov v primerjavi z referenčnimi standardi, ki imajo znano razmerje glede na nacionalne ali mednarodne standarde.

6.2 V državah, kjer ni Nacionalnega komiteja IEC ali kjer ne želi Nacionalni komite prevzeti funkcije NAI niti priznati drugega telesa kot NAI, se bo po pravilih postopno definiral nadaljni postopek.

6.3 Zgoraj opisane funkcije se morajo izvršiti v skladu z nacionalnimi pravili, ki se izvajajo po pravilih Sistema ter se lahko opravljajo z že obstoječimi telesi ali pa s telesi, posebej vzpostavljenimi za Sistem. Nacionalna pravila različnih držav morajo biti primerljiva ter morajo zagotavljati enotno uporabo pravil Sistema.

7. Mednarodna organizacija

7.1 Največjo odgovornost za delovanje Sistema nosi CMC, ki je komite IEC in deluje s pooblastili sveta IEC.

7.2 Sestava CMC je naslednja:

a) delegacija vsake države udeleženke, sestavljena iz največ dveh delegatov, ki jih imenuje NAI,

b) predsednik,

c) podpredsednik,

d) blagajnik,

e) predstavnik, ki ga imenuje ICC,

f) generalni sekretar IEC,

g) sekretar.

7.3 CMC lahko ustanovi delovne skupine z jasno opredeljenimi pristojnostmi za poročanje o stvareh, ki se tičejo upravljanja Sistema.

7.4 CMC mora ustanoviti ICC z jasno definirano sestavo in pristojnostmi.

ICC mora biti odgovoren za nadzor nad poenoteno uporabo pravil postopka, ki zadevajo ocenjevanje kakovosti. Odnos med CMC in ICC določajo pravila postopka.

8. Uradniki in administracija

8.1 Na predlog CMC imenuje Svet IEC predsednika za dobo treh let z možnostjo ponovnega imenovanja za nadaljno obdobje treh let. Za časa svojega uradovanja predsednik ne deluje kot nacionalni delegat.

8.2 Na predlog CMC imenuje Svet IEC podpredsednika za dobo treh let z možnostjo ponovnega imenovanja za nadaljno obdobje treh let. V istem času je predsednik lahko nacionalni delegat na odboru, razen takrat, ko odboru predseduje.

8.3 Na predlog CMC imenuje Svet IEC blagajnika za dobo treh let z možnostjo ponovnega imenovanja za nadaljno obdobje treh let. Blagajnik je v istem času lahko nacionalni delegat na odboru.

8.4 Sedež sekretariata je na glavnem uradu IEC- in tvori del vodstva glavnega urada IEC. Kandidate za službo

sekretarja se predlaga po sklepu generalnega sekretarja IEC in predsednika CMC. Po potrditvi CMC imenuje sekretarja generalni sekretar IEC.

8.5 Predsednik, podpredsednik ali blagajnik opravljajo svoje dolžnosti, dokler Svet IEC ne imenuje naslednika.

9. Poročilo Svetu IEC

CMC podaja letno poročilo Svetu IEC v roku treh mesecev po preteku koledarskega leta.

10. Zahteve za udeležbo

10.1 Vsak nacionalni komite IEC, ki bi želel sodelovati v Sistemu, mora izpolniti naslednje zahteve:

10.1.1 Ustanoviti ali priznati mora NAI in nacionalno organizacijo za standardizacijo.

10.1.2 Strinjati se mora z izvrševanjem pravil Sistema ter objaviti potrebne nacionalne dokumente.

10.1.3 Brez diskriminacije se mora strinjati s priznanjem proizvajalcev, vključno z njihovimi preskusnimi laboratoriji, neodvisnih distributerjev in neodvisnih preskusnih laboratorijev, potrdil o kvalifikaciji elementov ter veljavnostjo periodičnih preskusov elementov, ki so jih dali v promet drugi udeleženci v skladu s Sistemom.

10.1.4 Sprejeti mora finančne obveznosti po tč. 16.

10.2 Vsak nacionalni komite, ki je izpolnil zahteve tč.10.1.1 in zadostil zahtevam tč.10.1.2, 10.1.3 in 10.1.4, bo na zahtevo CMC postal država udeleženka v Sistemu.

10.3 Države udeleženke so zastopane v CMC, kot je opisano v tč. 7.2a).

10.4 Vsaka država udeleženka, ki bi želela uporabljati postopke certificiranja, mora zadostiti naslednjim zahtevam :

10.4.1 Imeti mora NSI v skladu s tč. 6.1.2a), ki mora biti potrjen po pravilih Sistema. To odgovornost lahko prenese tudi na priznan NSI kake druge države udeleženke.

10.4.2 Imeti mora ustanovljen ali priznan servis za kalibracijo po tč. 6.1.2b).

10.5 Druge države, skupine proizvajalcev ali individualni proizvajalci, ki jih ne zastopa nacionalni komite IEC, ali če njihov nacionalni komite IEC ne želi sodelovati, morajo zadostiti zahtevam, objavljenim v pravilih postopka, ki jih upravlja Sistem za proizvajalce, distributerje in neodvisne preskusne laboratorije v državah nečlanicah.

10.6 Za posebne okoliščine, ki jih ta pravila ne vsebujejo, je pristojen CMC.

11. Zakonske odredbe

11.1 Mednarodni nivo

11.1.1 CMC se ne ukvarja s trgovino, je neprofitna organizacija in ne sodeluje pri nobenih ekonomskih poslih za svojo korist. Nima nobene marketinške funkcije ali funkcije, ki bi regulirala cene. S svojo dejavnostjo si prizadeva za dosego ciljev po tč. 2.

Odločitve CMC so prostovoljne na osnovi predpisanih volilnih postopkov.

11.1.2 Sedež Sistema je isti kot sedež IEC.

Zakoni države, kjer je sedež komisije, se uporabljajo v vseh tistih primerih, ki jih ta osnovna pravila posebej ne predvidevajo.

11.2 Nacionalni nivo

Za nacionalne organizacije se uporabljajo zakoni države članice.

Ničesar, kar je v teh osnovnih pravilih ali v pravilih postopka, ne sme kršiti zakonov države, v kateri Sistem deluje, niti povzročiti nečesa, kar bi bilo protizakonito.

NAI vsake države udeleženke ali NMI je prepuščena odobritev nacionalnih pravil za izvajanje Sistema, da bi se zagotovila potrebna zakonita zaščita proti kršitvi kateregakoli zakona.

11.3 Zakonska zaščita

Nobene od zakonskih odgovornosti, ki so v smislu nacionalne in mednarodne zakonodaje obveza proizvajalca ali distributerja certificiranega proizvoda, se s podelitvijo certifikata o ustreznosti ne prenaša na CMC ali IEC.

11.4 Izključitev obveznosti

Nacionalne organizacije, ki delujejo v imenu CMC, delajo to na lastno odgovornost in podvzamejo vse korake za izključitev vseh obveznosti CMC ali IEC.

11.5 Oprostitev

V primeru, ko je CMC ali IEC legalno odgovoren po mednarodnem ali nacionalnem zakonu za katerokoli akcijo nacionalne organizacije, ki deluje namesto CMC, potem nacionalna organizacija razbremeni popolnoma CMC in IEC takih obveznosti.

12. Standardi in specifikacije

12.1 Sistem bazira na IEC standardih, ki vključujejo tudi ukrepe za oceno kakovosti. Kadar je potrebno, naj bi bili ti standardi vsebovani v nacionalnih standardih za elektronske elemente države udeleženke , ki naj bi bili certificirani znotraj Sistema. V tem primeru jih države udeleženke lahko prepišejo, če je to potrebno, v skladu s pravili lastnega nacionalnega Sistema, vendar brez spreminjanja tehnične vsebine.

12.2 V primeru, ko ni ustreznih IEC standardov, se lahko začasno uporabljajo drugi dokumenti, ki jih NAI pošlje CMC. Če ti dokumenti niso v skladu z zahtevami Sistema, potem certificiranje odpade. Če so začasni dokumenti drugačni kot podrobne specifikacije, ali pa je vsebina širša kot v podrobnih specifikacijah, tedaj se zaprosi CMC, da jih potrdi, še preden se začno uporabljati v Sistemu. V pravilih postopka je potrebno določiti termin za akcijo.

Pri ustreznih tehniških komitejih IEC je treba zahtevati, da čimprej pripravijo IEC standard, ki bo pokrival področje začasnih dokumentov v skladu z normalnimi pravili in postopki.

Začasne specifikacije se lahko uporabljajo največ tri leta za potrditev kvalifikacije, vsekakor pa se jih vzame iz uporabe takrat, ko izide ustrezen standard IEC.

V primeru, da v treh letih še ne izide ustrezen IEC standard, lahko CMC glede na vzroke zamude podaljša uporabo začasnih standardov. Vodstvo ustreznega telesa IEC mora opozoriti tehnične komiteje, da stopijo v akcijo.

12.3 Dokumenti pod tč. 12.1 in 12.2 morajo vsebovati navodila za izdelavo detajlnih specifikacij, n.pr. okvirne podrobne specifikacije in če je praktično izvedljivo, detajlne specifikacije.

Če ni ustreznih detajlnih specifikacij, pripravijo potrebne detajlne specifikacije za to zadolžene skupine v skladu s pravili Sistema.

13.Ocenjevanje kakovosti

13.1 Zagotovilo, da elementi ustrezajo zahtevam odgovarjajočih specifikacij, je dano z atestom o ustreznosti pod nadzorstvom NSI v skladu s pravili Sistema.

Kadar se uporabljajo začasne specifikacije (glej tč. 12.2), mora biti to jasno označeno na certifikatu in če je možno, tudi na oznakah.

13.2 Pravila postopka Sistema predpisujejo zahteve za:

a) potrditev NSI,

b) potrditev neodvisnih preskusnih laboratorijev,

c) potrditev proizvajalcev, vključno z njihovimi laboratoriji,

d) potrditev neodvisnih distributerjev,

e) odgovornosti glavnega kontrolorja,

f) standarde ali specifikacije, ki se uporabljajo v Sistemu.

g) postopke za ocenjevanje kakovosti in odpošiljanja elementov ter dovoljenja za atestiranje elementov, ki so bili izdelani, preverjeni, odposlani in distribuirani v skladu s temi pravili,

h) poročanje o rezultatih preskusa.

13.3 NSI, potrjeni v Sistemu, morajo ustrezno ukrepati, da se vzdržuje zahtevana skladnost uporabe postopkov ocenjevanja kakovosti. Detajli teh ukrepov so v Pravilih postopka.

13.4 Pritožbe glede kakovosti elementov, ki nastanejo med proizvajalcem in uporabnikom (ali kupcem in prodajalcem) znotraj države, se rešujejo po ustreznih postopkih te države. CMC mora potrditi postopek za reševanje pritožb ter je sam odgovoren za reševanje tozadevnih prizivov, če je v to vključena več kot ena država.

14. Glasovanje

14.1 Odločitev sprejeta z glasovanjem NAI v skladu s tč. 14.2 ali 14.3 mora biti izvedena znotraj Sistema. Vsaka NAI ima samo en glas. Preostanek CMC nima glasov.

14.2 Odločitve, ki vplivajo na osnovna pravila ali pravila postopkov, morajo biti v skladu s "šestmesečnim glasovanjem" in "dvomesečnim glasovanjem", ki so definirani v Sistemu takole:

14.2.1 Šestmesečno glasovanje
Pri šestmesečnem glasovanju pošlje sekretar predloge cirkularno vsem NAI. NAI zaprosi za odgovor v roku šestih mesecev od datuma, ko so bili poslani, naj glasujejo, ali se strinjajo ali ne s poslanimi predlogi. Predlog je sprejet, dokler ne da ena petina ali več NAI negativen glas - razen v primeru, če je glas na dokumentu v skladu s tč. 4.4, tedaj odloči o glasovanju predsednik CMC po posvetovanju s predsednikom inšpektorata koordinacijskega komiteja.

Poročilo o glasovanju se razpošlje, vsebuje pa odločitev predsednika v akcijah, ki jih je treba storiti.

14.2.2 Dvomesečno glasovanje
Dvomesečno glasovanje se uporablja samo zato, da se zagotovi potrditev dodatkov, sprejetih po šestmesečnem glasovanju, če predsednik CMC meni, da je upo-

raba takega postopka primerna za naraščanje števila NAI, ki bi lahko sprejele predlog kot izboljšanega.

Dvomesečno glasovanje deluje enako kot šestmesečno, razen da je treba odgovoriti v dveh mesecih.

14.3 Ostale odločitve, vključno z zadevinimi dokumenti tehničnih komitejev IEC, s predlogi za delegate, ustanavljanjem delovnih skupin ter finančnimi zadevami, se normalno sprejemajo med zasedanjem CMC. Vsekakor pa se po odločitvi predsednika ali na zahtevo kake delegacije odločitve lahko sprejemajo s korespondenčnim glasovanjem.

Odločitve o stvareh, ki so na glasovanju med zasedanjem, so pozitivne, če zanje glasuje večina delegacij. Podpredsednik nima glasu glede na svoj položaj, vendar pa, če je on edini član delegacije, lahko glasuje namesto članov, kljub temu da je predsedujoči zasedanja.

Odločitve, za katere se glasuje korespondenčno, se sprejmejo kot pozitivne, če zanje glasuje večina NAI, kadar ni drugače predvideno v pravilih postopka. Korespondenčno glasovanje je zaključeno, ko glasujejo vsi NAI ali v treh mesecih - kar je pač krajše.

Kadar so glasovi enakomerno razdeljeni odloča o ukrepih predsednik. Odločitve CMC se posredujejo NAI.

15. Izstop iz Sistema

15.1 Države udeleženke, ki žele izstopiti iz Sistema, sporočijo to pismeno sekretariatu CMC, ki o tem obvesti vse ostale NAI. Zaznambo o tem izstopu je treba dati najmanj eno koledarsko leto pred dejanskim izstopom.

15.2 Udeležba se lahko umakne ali odpove po odločitvi sveta IEC na osnovi priporočila CMC, če se država udeleženka ne more držati glavnih dokumentov Sistema. Preden pride do teh akcij, ima država udeleženka pravico zvedeti (pred svetom IEC) za razloge, razen v primeru odpovedi udeležbe zaradi neplačevanja pristojbin. Pristojbin se ne vrača v primeru odstopa ali odpovedi udeležbe.

15.3 Položaj glede prenehanja udeležbe NMI ali proizvajalcev, distributerjev in neodvisnih preskusnih laboratorijev v državah, ki niso udeleženke, je enak kot pri državah udeleženkah, kot je opisano v tč. 15.1 in 15.2.

16. Finance

16.1 Sistem je neprofiten in se sam financira.

16.2 Za finančno administracijo je odgovoren CMC.

16.3 Finančno leto Sistema je koledarsko leto.

16.4 Prihodki Sistema izhajajo iz letnih pristojbin držav udeleženk sekretariatu ter iz drugih virov, ki jih odobri CMC. Letne pristojbine določa CMC.

16.5 Predlog letnega budžeta CMC, vključno s predlaganimi prostojbinami, pripravi sekretar v povezavi z blagajnikom. Predlog budžeta dobijo vse države udeleženke, na koncu pa se o njem dogovorijo na CMC. Ta postopek mora biti zaključen vsako leto 1. decembra, lahko pa se izvede tudi korespondenčno.

Po tem sklepu se budžet posreduje svetu IEC, ki potrjuje finančno politiko in glavne postavke budžeta ter zneske prispevkov CMC za vodstvo IEC.

16.6 Države udeleženke morajo plačati letne prispevke sekretariatu pred koncem junija tekočega leta.

16.7 Vsako leto do najkasneje 15. marca pošlje sekretariat državam udeleženkam račun Sistema za preteklo leto, ki ga potrdi profesionalni kontrolor in podpiše blagajnik CMC.

16.8 Za države udeleženke, ki za dano leto niso plačale pristojbin 31. decembra tega leta, se njihova udeležba ustavi s 1. januarjem naslednjega leta. Med to prekinitvijo nima pravice pošiljati delegacij na CMC ali sprejemati dokumentov ali publikacij CMC niti glasovati. Prekinjena je tudi pravica uporabe postopkov certificiranja.

17. Spremembe osnovnih pravil

Ta osnovna pravila se spremenijo po naslednjih postopkih:

17.1 Za nameravane spremembe osnovnih pravil je treba pismeno obvestiti sekretarja CMC, ki pošlje kopije NAI držav udeleženk najkasneje tri mesece pred zasedanjem CMC, na katerem naj bi razpravljali o spremembah.

Dodatno pošlje sekretar kopije predlaganih sprememb v luči aspektov ocenjevanja kakovosti inšpektoratu koordinacijskega komiteja v proučitev in razpravo.

17.2 Ko te predlagane spremembe v skladu tč. 14.2 CMC potrdi, se jih pošlje svetu IEC v potrditev.

18. Razpustitev Sistema

Razpustitev Sistema lahko predlaga CMC na zasedanju, sklicanem posebej za ta namen. Če je predlog sprejet v skladu s tč. 14, se ga posreduje svetu IEC v potrditev. V primeru razpustitve bo svet IEC uredil ukinitve preostale lastnine in kapitala po ureditvi vseh obveznosti.

Tone Tekavec
SIQ, Tržaška 2, Ljubljana

ZNANSTVENO RAZISKOVALNI PROJEKTI S POLJA ELEKTRONSKE KOMPONENTE IN TEHNOLOGIJE V SLOVENIJI ZA LETO 1993

Karakterizacija tankoplastnih struktur z metodami za analizo površin.
Odgovorni nosilec dr. Anton Zalar, izvajalec IEVT sredstva 10.750.000 SIT.

Mikrostruktura, duktilnost in magnetne lastnosti železa s 15-24 % Co in 20-28 % Cr.
Odgovorni nosilec dr. Franc Vodopivec, izvajalec IMT, sredstva 8.025.000 SIT

Optoakustični pojav.
Odgovorni nosilec dr. Janez Možina, izvajalec Fakulteta za strojništvo, sredstva 4.700.000 SIT.

Metodologija za avtomatizirano načrtovanje kompleksnih mikrovezij.
Odgovorni nosilec dr. Janez Trontelj, izvajalec Fakulteta za elektrotehniko in računalništvo, sredstva 28.210.000 SIT.

Tankoplastne tehnologije v mikroelektroniki
Odgovorni nosilec dr. Boris Navinšek, izvajalec IJS, sredstva 6.720.000 SIT.

Elektronska keramika: materiali in tehnologije.
Odgovorni nosilec dr. Marija Kosec, izvajalec IJS, sredstva 13.300.000 SIT.

Mikroelektronika: debeloplastna tehnologija in materiali.
Odgovorni nosilec dr. Janez Holc, izvajalec IJS, sredstva 11.840.000 SIT.

Vakuumska optoelektronika
Odgovorni nosilec dr. Alojz Paulin, izvajalec IEVT, sredstva 3.494.000 SIT.

Polprevodniške strukture, analiza notranjih efektov in modeliranje.
Odgovorni nosilec dr. Slavko Amon, izvajalec Fakulteta za elektrotehniko in računalništvo, sredstva 8.060.000 SIT.

Avtomatsko načrtovanje VLSI vezij, programabilne matrike vrat.
Odgovorni nosilec dr. Baldomir Zajc, izvajalec Fakulteta za elektrotehniko in računalništvo, sredstva 3.550.000 SIT.

Rekapitulirano lahko ugotovimo, da so dodeljena sredstva namenjena znanstveno raziskovalnim področjem:

mikroelektronika:	43.600.000 SIT
materiali:	24.050.000 SIT
karakterizacija:	10.750.000 SIT
optoelektronika:	8.194.000 SIT
elektronske komponente:	8.060.000 SIT,

po izvajalcih pa:

FER	39.829.000 SIT
IJS	31.860.000 SIT
IEVT	14.244.000 SIT
IMT	8.025.000 SIT
FS	4.700.000 SIT

Dr. Rudi Ročak

La Lettre du Toulouse

Danes po delu sem pohitel še do pekarne, da si nabavim bagutte-o za k večerji. Francozi ne marajo starega kruha, zato lahko čez cel dan dobite slastno sveže pečenega. Sicer pa te dolge štruce čez en dan resnično okamenijo in so uporabne le še za družinske prepire. Malo me je zaneslo, pravzaprav sem hotel povedat, da sem potem skočil na kavico, da se malo oddahnem po napornem dnevu in pogledam, kaj pravi dnevno časopisje. Kava je najcenejša stvar, ki jo lahko dobite v restavracijah in barih. Tudi v najboljših ni dražja od 6 frankov. Čim pa hočete čez še smetano, to ni več kava ampak kava s smetano in vas zato "košta" 2x več. Toliko kot sok ali navadna mineralna voda (z minerali ali brez) ali pa malo pivce - demi, kot mu tu pravijo. No, pravzaprav sem hotel povedat, kako v časopisu preberem, da je danes MOTOROLA SEMICONDUCTORS v Parizu javno naznanila, da bo investirala 250 miljionov frankov v izgradnjo dodatnih ultramodernih prostorov klase 10 v Toulousu, kjer sicer že 26 let teče proizvodnja polprevodnikov - 1900 zaposlenih že sedaj pridela na leto 2,6 miljarde frankov. Ta center bo namenjen produkciji Smart-MOS vezij za avtomobilsko industrijo, telekomunikacije in gospodinjske aparate - povsod se da stlačit še malo pameti. K razvoju novih elementov dosti prispeva tudi raziskovalni institut LAAS, s katerim imajo posebno pogodbo o sodelovanju. Zopet malo prehitevam, mogoče najbolje, da začnem od začetka.

Toulouse (Tolosa) je izgubljeno mesto moderne tehnologije in znanosti na jugozahodnem delu Francije. Pre-

daleč od morja, da bi bilo mediteransko ali atlantsko in predaleč od Pirinejev, da bi bilo "alpsko". Je torej mešanica vsega tega. Tu kraljuje AEROSPATIALE s svojim Airbusom, MATRA MARCONI SPACE s svojimi sateliti, ter cela množica raziskovalnih inštitutov, ki pripomore, da vse skupaj dobro leti skupaj z raketo ARIANE, ki jo tudi tu načrtujejo. In pa univerze. Toulouse, ki je velikosti Ljubljane (in obratno), ima kakšnih 5 univerz z okoli 40-50000 študenti. Pravo univerzitetno mesto, kar se mu tudi pozna; posebno ko posije sonce v mestu završi, vse poseda po neštetih barčkih, sreba kavo in opazuje brhke francozinje, ki letijo naokoli v mini krilcih.

Jaz sem jo konec februarja primahal z denarjem Evropske skupnosti, da bi osem mesecev (dva sem izgubil čakajoč na francosko vizo) preživel v že omenjenem laboratoriju LAAS (Laboratoire d'Automatique et d'Analyse des Systemes). LAAS spada v sistem največje in najbolj prestižne francoske raziskovalne inštitucije CNRS (Centre National de la Recherche Scientifique), sicer pa je povezan s Toulouskimi univerzami (Univerzo Paul Sabatier, l'Institut National des Sciences Appliquées de Toulouse). V njem dela 400 ljudi, od tega 300 raziskovalcev, profesorjev, doktorantov, post-doc ov itd.. Ta gmota na leto pridela okoli 550 publikacij, 45 doktorjev in 110 kontraktov. To je relativno mlad laboratorij (vsi smo mi mladi), letos je dopolnil 25 let.

LAAS je sestavljen iz treh delov (Avtomatika, Robotika in Mikroelektronika), ki nimajo kaj dosti več skupnega kot isti vhod, parkirišče, knjižnico in jedilnico. Mikroelektronika se zopet deli na štiri podsisteme: v skupini "Structures III-V" se ukvarjajo z raziskavami polprevodnikov III in V skupine, ki pridejo posebno v poštev na področju telekomunikacij, kjer so francozi kar "močni". Raziskujejo uporabo epitaksije za optične aplikacije ($GeAs/CaF_2$, GaAs/Safir, $CaSrF_2/GaAs$ ...), izdelavo diodnega laserja (GaAs), izdelavo heterospojnih elementov - TBH (GaAlAs/GaAs).

Naslednja skupina se ukvarja z mikrostrukturami in sistemi na podlagi silicija (Microstructures silicium et microstructures integrees), kamor spadajo vse vrste senzorjev, tanki filmi ... - široko področje.

Tretja skupina se ukvarja z visokofrekvenčnimi elementi(Composants et Circuits Micro Ondes), torej z raziskovanjem HEMT in HBT struktur.

In nenazadnje, čeprav nazadnje, skupina, ki se ukvarja z močnostnimi elementi (Composants et Integration de Puissance), kjer poskušam dvigovati raziskovalni nivo tudi jaz. Ta skupina ima pravzaprav zopet tri podskupine, ki pa med sabo sodelujejo oz. se dopolnjujejo. Skupina za fiziko polprevodnikov in novih močnostnih elementov, kjer najdete tudi mojo malenkost, se ukvarja predvsem z raziskovanjem močnostnih MOS transistorjev (lateralnih, vertikalnih), IGBT in MTCjev, ki so uporabni za integracijo v Smart Power ali HVIC vezja. Druga skupina se ukvarja s simulacijo močnostnih elementov na nivoju vezij (SPICE) za RF ojačanja, ter elektrotermično simulacijo. Tretja skupina pa se zabava z integracijo močnostnih elementov, torej predvsem s problemi izolacije med elementi. Vsi skupaj pa imajo na razpolago še ekipo (TEAM), ki dela v čistih prostorih (400 m^2) in 500 m^2 za teste in karakterizacijo. Večino elementov torej izdelajo in preizkušajo v lastnih prostorih.

Sam sem prišel nadaljevati delo, ki ga opravljam na Fakulteti za Elektroniko in Računalništvo v Laboratoriju za Elektronske Elemente v okviru doktorskega študija. Pod vodstvom prof.dr. Slavka Amona se ukvarjam z modeliranjem zaključitvenih tehnik močnostnih (visokonapetostnih) elementov, kar je tudi neposredno povezano z raziskovalnimi interesi skupine v LAASu.

Prve tri mesece sem preučeval Resurf tehniko (poleg urejanja eksistenčnih zadev), ki je predvsem primerna za realizacijo visokonapetostnih LDMOS tranzistorjev (lahko pa tudi JFET ali bipolarnih tr.). Raziskoval sem možnosti analitične razlage Resurf efekta, ki je sicer po svoji naravi tipično 2D efekt. Mislim, da mi je uspelo najti kar dober analitičen model, ki omogoča analizo vpliva različnih parametrov na prebojno napetost Resurf strukture. Zadnje čase pa se bolj posvečam tehniki zaključitve, ki močno spominja na zelo znane in razširjene varovalne obroče (guard rings), le da so ti sedaj med seboj povezani. Pravzaprav gre za difundirano spiralo, ki se ovija okoli glavnega spoja in je na koncu sklenjena z reverzno napetostjo. Spirala deluje kot uporovna plast tako, da so napetost okoli glavnega spoja dobro definirane. To je bila tudi glavna pomanjkljivost "floating" obročev, katerih prebojne lastnosti so zelo občutljive od površinskega naboja in medsebojnih razdalj. Tehnika s pomočjo spirale obeta bistveno manjšo občutljivost na različne parametre s tem pa tudi bistveno večjo uporabnost. Je pa tu kar enačb, ki se jih da vrteti naokoli. Dela mi skratka ne manjka, poleg tega bo pa potrebno na koncu vse rezultate še strniti v poročilo. To bo še naporno delo v času, ko se temperature dvigajo proti neznosnim razmeram. In ko bo morje zadišalo na svojih 200 km. Takrat bo začelo delovati domotožje.

Prav lepe pozdrave,
A BIENTOT, Dejan Križaj
A Toulouse, 18 Juin 1993

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KONFERENCE, POSVETOVANJA, SEMINARJI, POROČILA

SEMICON EUROPA 93
Palexpo .Ženeva, Švica . 30., 31. Marec in 1. April

V dneh od 30.3. do 1.4.1993 je v Ženevi, Švica potekala mednarodna konferenca in razstava "SEMICON Europa 93". Obseg razstave se je v zadnjih letih povečal do te meje, da razstavni center ZUSPA v Zürichu ni več ustrezal zahtevam po modernem razstavnem centru, zato se je letos po 18-tih letih razstava SEMICON Europa preselila v Ženevo, v razstavni prostor PALEXPO, ki je lociran neposredno ob železniški postaji in letališču in je dosegljiv iz centra mesta Ženeve v pičlih desetih minutah. To moderno razstavišče z ogromno razstavno površino omogoča potek razstave in konference pod eno streho. Razstavljalo je prek 700 razstavljalcev, pretežno iz ZDA in Evrope, ki so pokrili 1300 razstavnih mest. V povezavi z razstavo so potekali še trije kvalitetni industrijski izobraževalni programi.

Razstavo SEMICON organizira mednarodno združenje "Semiconductor Equipment and Materials International" (SEMI), ki združuje 1450 članic in ima sedeže v ZDA, Evropi, Koreji in na Japonskem. To združenje povezuje industrijo z 20 miljardami dolarjev kapitala. Njihovi programi vzpostavljajo uspešno okolje za naročnike in potrošnike s področja polprevodniške opreme in materialov, opreme in materialov za prikazovalnike z ravnimi zasloni in celotnega servisiranja obeh področij. Organizacija SEMI med številnimi nalogami skrbi za mednarodne industrijske standarde, organizira mednarodno konferenco (SEMICON), vodi tržno statistiko (SEMS), izdaja tehnične in marketinške informacije za področje polprevodništva in prikazovalnikov z ravnimi zasloni (SEMICOMM), skrbi za tehnično izobraževanje, organizira simpozije za industrijsko strategijo (ISS).

Mednarodni industrijski standardi, ki predstavljajo najbolj izčrpen izpis specifikacij standardov za polprevodniške naprave in materiale, združujejo potrebe in zahteve prodajalcev, uporabnikov in konzultantov. Vse izboljšane specifikacije se objavijo v devetih zvezkih, ki pokrivajo kemikalije, avtomatizacijo naprav, materialov, zapiranja, mikropreslikav, izsledljivosti, naprav in navodil za varnost. Tržna statistika (SEMS) zagotavlja uporabno poročilo o tržnih trendih in je brezplačen za vse, ki so včlanjeni v SEMI. SEMI letni SEMICON, ki združuje razstavo in konferenco, je najboljša mednarodna razstava za uvajanje novih proizvodov in tehnoloških dosežkov in je izključno namenjen proizvodom in ponudbi uslug s področja proizvodnje polprevodnikov in prikazovalnikov z ravnimi zasloni. Strateško je lociran na Japonskem, Koreji, Singapuru, Švici, Kitajski in ZDA.

SEMICOMM je načrtovan za distribucijo tehničnih in marketinških informacij za opremo, materiale in industrij, ki izdelujejo elemente s področja polprevodništva in prikazovalnikov z ravnimi zasloni.

Tehnični izobraževalni programi povezujejo svetovno priznane industrijske strokovnjake, akademske raziskovalce in poslovne eksperte, ki razpravljajo o najnovejših dosežkih in novostih s tega področja. Letos so potekali trije industrijski izobraževalni programi v času razstave:

- ☐ Izboljšave v tehnologiji prikazovalnikov z ravnimi zasloni
- ☐ Razumevanje in uporabna cena lastništva.
- ☐ Tehnična konferenca - Napredki v proizvodnji polprevodnikov

Konferenca je bila brezplačna za vse obiskovalce, ki so se predhodno registrirali. Izdan je bil tudi zbornik, ki ga je bilo mogoče kupiti na samem mestu registracije (80 SFR). Konferenca je bila razdeljena na štiri področja:

1) področje materialov in kemikalij

> Poudarek na vplivu defektov v substratnih materialih, lastnostih epitaksijskih plasti in kvaliteti kemikalij ter njihov vpliv na lastnosti elementov in združljivost z submikronsko tehnologijo izdelave integriranih vezij.

2) področje čiščenja površin

> Predstavitev možnosti za doseganje ekstremno čistih površin, kar je osnovna zahteva za izdelavo visoko kvalitetnih polprevodniških rezin in elementov. Podani so bili industrijski trendi, ki prispevajo k napredku v znanosti in tehnologiji čiščenja površin.

3) področje preslikovanj

> podan je bil pregled najnovejših tehnik pri suhem jedkanju in v litografiji, kjer je bil predstavljen razvoj na področju "i-line" litografije, globoke UV litografije, izdelave mask, novih naprav in procesnih konceptov.

4) področje optimizacije proizvodnje

> Predstavitev inovativnih dosežkov s področja avtomatskega rokovanja, transporta, shranjevanja,

novih kontrol kot tudi označevalnih in simulacijskih tehnik.

Prvi dan obiska sem se udeležil drugega dela tehnične konference na temo površinska čiščenja. Poslušal sem zanimivo predavanje o suhem čiščenju rezin. Avtor prispevka je zaključil, da bo prihodnost čiščenja v kombinaciji med suhim in mokrim čiščenjem. Glavna prednost suhega čiščenja predstavlja možnost uporabe čiščenja v tako imenovanih "In-situ cleaning in cluster tools " napravah.

Na področju mokrega čiščenja je bil poudarek po spremembi standardnega čiščenja (SC), kvalitetnejše sušenje rezin v parah izopropil alkohola (IPA vapor drying), kontamincija rezin s čistilnimi kemikalijami, vpliv kalcija na prebojno trdnost MOS oksida, dodatek tako imenovanega "surfactanta" za izboljšanje omočljivosti površine pri jedkanju v majhne oksidne odprtine, vpliv uporabe kemikalij različnih proizvajalcev na kvaliteto elementov, itd.

Drugi dan obiska sem namenil ogledu razstavnih mest. V veliko pomoč pri ogledu razstave mi je bil brezplačen programski vodič, ki sem ga prejel ob vhodu. Razdelitev razstavnih mest v šest specifičnih področij proizvodov (kemikalije, plini, materiali; čisti prostori, prikazovalniki z ravnimi zasloni; testiranje, montaža, transport; avtomatizacija elektronskega načrtovanaja in procesiranje rezin, procesne naprave) je omogočila večjo preglednost razstavnih mest in lažje iskanje proizvodov različnih proizvajalcev.

Od razstavljalcev, s katerimi že več let sodelujemo, sem iz prve roke dobil najnovejše informacije o njihovih proizvodih in trendih. Razpravljali smo o morebitnih problemih pri uporabi njihovih proizvodov. Osebno me je najbolj zanimalo področje procesnih naprav in opreme čistih prostorov in področje kemikalij, plinov in materialov. Kar se tiče procesne opreme sem se predvsem zanimal za laboratorijsko opremo, ki naj bi bila več namenska in ne avtomatizirana.

Veliko zanimanja je požela statična kontrola čistih prostorov z zračnimi ionizatorji. Zračni ionizatorji predstavljajo najbolj učinkovito metodo za odstranitev statičnega naboja v neprevodnih materialih. Zračni ionizatorji generirajo veliko količino pozitivnih in negativnih ionov v zraku in s tem povečujejo prevodnost zraka. Zmanjšanje statične elektrike zmanjša površinsko kontaminacijo, število elektrostatičnih razelektritev in probleme 'latch-up'-a v MOS integriranih vezjih.

'SEMICON Europa 93' je ponovno dokazala, da je najkvalitetneša razstava s področja polprevodništva in prikazovalnikov z ravnimi zasloni v Evropi. Nudi najbolj sveže informacije s tega področja in jo zato priporočam vsem strokovnjakom.

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PREDSTAVLJAMO PODJETJE Z NASLOVNICE

LABORATORIJ ZA MIKROELEKTRONIKO NA FAKULTETI ZA ELEKTROTEHNIKO IN RAČUNALNIŠTVO

Laboratoriji za mikroelektroniko s štiridesetimi visoko usposobljenimi raziskovalci usmerja svoje aktivnosti v raziskave, razvoj in poučevanje na področju monolitnih integriranih vezij. Pri tem so posebej poudarjene aktivnosti na področju submikronskih procesnih tehnologij BICMOS, na zasnovi kompleksnih elektronskih sistemov in na razvoju načrtovalskih metodologij za načrtovanje kombiniranih analogno digitalnih integriranih vezij. Med uspešno zaključene projekte v zadnjem času sodijo vezja za telefonski aparat nove generacije, vezja za avtomobilsko elektroniko, vezja s "pametnimi senzorji", knjižnica analognih celic, programska oprema za avtomatsko sintezo in analizo ter generacijo geometrije operacijskih ojačevalnikov in različnih filtrov in nekateri procesni koraki za submikronsko tehnologijo BICMOS.

Iz izkaznice Laboratorija lahko razberemo, da v njem deluje 13 doktorjev znanosti in 11 magistrov različnih profilov, od fizikov, kemikov, metalurgov do elektrotehnikov. V zadnjih nekaj letih so objavili prek dvesto prispevkov v domači in tuji periodiki. Nekateri med njimi so vzbudili širšo mednarodno pozornost. Na novo zgrajeni laboratorij ima prek 400 m^2 čistih prostorov razreda 10.

Oprema navzlic gradnji zaradi omejenih financ še vedno predstavlja dokaj moderno rešitev, saj ima npr. laboratorij v bogatem stanfordskem Centru za integrirane sisteme v Kaliforniji povečini enake naprave.

Laboratorij je aktiven tudi na pedagoškem področju, saj v njem potekajo vaje, diplomska in magistrska dela iz

rednega fakultetnega programa. Stalno v njem gostuje tudi po več raziskovalcev iz drugih inštitucij in industrije.

Potencialni vpliv laboratorija na slovensko okolje vidimo predvsem v naslednjem:

- Vzdrževanje pilotskega pogona v mikronski in submikronski tehnologiji BICMOS omogoča hitro in učinkovito verifikacijo sistemske zasnove vezja ASIC.
- Omogoča Ministrstvu za znanost in tehnologijo spodbujanje prestrukturiranja slovenske elektronske industrije po utečenem evropskem vzorcu, kjer vlade participirajo pri vsaki uspešni realizaciji elektronskega sistema z vezjem po lastni zasnovi pri stroških s petdesetodstotno dotacijo.
- Je osnova za sodobno izobraževanje na področju elektronike. V razvitejših deželah vsak študent na podiplomskem študiju realizira najmanj eno vezje po lastni zasnovi.
- Omogoča kvalitetnejši razvoj načrtovalske metodologije.
- Predstavlja kompletno ponudbo od zasnove vezja do delujočih prototipov, ki so optimizirani za ceneno velikoserijsko proizvodnjo. Ta faza razvoja elektronskega sistema namreč predstavlja konkurenčno prednost in potrebno zaščito industrijske lastnine za domačo industrijo.

Načrtovalska znanja, ki so potrebna za nastanek integriranega vezja kot direktnega materialnega rezultata tretje tehnološke revolucije lahko uspešno gojimo le v sredini, ki poleg sistemskih znanj obvlada tudi zapletene tehnološke korake za realizacijo teh vezij.

Laboratoriju je nekako uspelo, da je dokaj posrečeno iskal ravnotežje med vsemi potrebnimi aktivnostmi in finančnimi možnostmi.

Želja laboratorija kot tudi industrije, s katero je povezan je, da taka možnost živi tudi v bodoče.

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PRIKAZI DOKTORATOV, LETO 1992

Naslov naloge: **Metodologija načrtovanja topoloških in geometrijsko snovnih lastnosti integriranih struktur CMOS**

Avtor: **Vinko Kunc**
Mentor: **prof. dr. Janez Trontelj**
Univerza v Ljubljani, Fakulteta za elektrotehniko in računalništvo

Namen dela je bil oceniti možnosti razširitve dinamičnega območja standardne CMOS tehnologije in dobljene izsledke tudi aplicirati v praksi.

V ta namen smo analizirali napetostne omejitve standardne CMOS tehnologije in pokazali možnost realizacije treh tipov visokonapetostnih tranzistorjev brez spremembe tehnoloških korakov. Te smo tudi preizkusili na testnem vezju. Kot primer uporabe visokonapetnostnih elementov smo realizirali izhodne stopnje in serijske aktivne napajalne zaščitne strukture. Pri tem smo naleteli na mnogo problemov, ki jih povzročajo parazitni elementi in razlika v krmilnih nivojih standardnih in visokonapetnostnih elementov. Te probleme smo identificirali in pokazali na možnosti njihove eliminacije. V tem sklopu smo rešili tudi probleme vezja ob negativnih napajalnih konicah. Rezultat teh raziskav je znanje, ki omogoča uporabo standardne CMOS tehnologije in vseh njenih znanih prednosti, v delu področja, ki so ga do sedaj pokrivala izključno "smart power" in bipolarna vezja.

Drugi del pa analizira degradacijske mahanizme, ki zmanjšujejo občutljivost integriranega vezja. Našteli smo glavne vzroke in analizirali njihov vpliv na občutljivost vezja. Analiza je zasnovana kompleksno, saj pokriva vplive geometrijskih lastnosti tranzistorjev in sklopov do sistemskih vplivov. Rezultati analize služijo za optimizacijo topoloških in geometrijskih značilnosti vezja. Poleg tega pa smo vpeljali še nove sklope, ki zmanjšujejo vpliv degradacijskih mehanizmov. Med temi gre še posebej omeniti sistem za izničevanje napetosti ničenja ojačevalnika, ki uporablja povečanje pasovne širine za izboljšanje resolucije in sistem za zmanjšanje sistemsko generiranega šuma časovno nezveznega integratorja. Tudi te raziskave so bile verificirane s testnim vezjem visoke resolucije in integratorjem kot vhodnim elementom.

Naslov naloge: **Metodologija sinteze integriranih operacijskih ojačevalnikov**

Avtor: **Andrej Vodopivec**
Mentor: **prof. dr. Janez Trontelj, dipl. ing.**
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Integracija kompleksnih analognih in mešanih sistemov na monolitnem integriranem vezju zahteva boljša orodja za načrtovanje analognih integriranih vezij. Razvoj metod in algoritmov na tem področju zaostaja za metodami sinteze digitalnih vezij, zato je načrtovanje analognih

sklopov še vedno domena ekspertov za načrtovanje analognih integriranih vezij. To delo obravnava metode in algoritme za sintezo analognih integriranih sklopov s poudarkom na sintezi operacijskih ojačevalnikov, ki jih je mogoče uporabiti v orodju, ki zaradi svoje hitrosti omogoči načrtovalcu v kratkem času možnost ovrednotiti več različnih topologij s podobnimi lastnostmi.

Metodologija sinteze analognih sklopov v tej disertaciji se zgleduje po sistemu, ki ga za načrtovanje uporabljajo eksperti za načrtovanje analognih integriranih vezij. Temelji na predlagani poenostavitvi - skaliranju podsklopov vezja. Skaliranje razdeli elemente v vezju v dve skupini. Aktivni elementi vplivajo na zunanje lastnosti vezja, pasivni elementi pa skrbijo za tokovne preslikave, stabilnost delovne točke in podobno. Vezje je nadalje razbito na podsklope, ki vsebujejo največ en neodvisen aktiven element. Pri optimizaciji vezja glede na sintezi zahtevane specifikacije vezja se spreminja le velikosti neodvisnih in odvisnih aktivnih elementov v tistih podsklopih, ki le-te vsebujejo. Na ta način se zmanjša prostostna stopnja sistema, ki ga je potrebno optimizirati, poenostavi pa se tudi analiza in kompilacija geometrije.

Obravnavana metoda pa sintetizira analogen sklop v treh korakih: izbira ene ali več topologij s pomočjo pravil v decizijskem drevesu, optimizacija sklopov v izbranih topologijah z enim od treh opisanih algoritmov ter ocena in razvrstitev izbranih rešitev. Dva algoritma za določitev optimalne kombinacije velikosti elementov v izbrani topologiji temeljita na zelo hitri analizi vezja. To omogoča modeliranje skalirnih analognih vezij s pravili in zapis le teh v preprostem programskem jeziku. Karakteristike vezja se lahko določi z nekaj deset vrsticami programa, ki ne potrebuje zank in zato nima konvergenčnih problemov.

Pomemben korak pri načrtovnju integriranih vezij je tudi izdelava geometrične baze podatkov, ki je v procesiranju integriranih vezij preslikana v strukture na siliciju. Skaliranje poenostavi kompleksen problem kompilacije geometričnega opisa na zlaganje interaktivno optimiziranih podcelic. Ker predlagana metoda naredi celotno bazo samo z zlaganjem podcelic, ni težav s presluhi med povezavami, parazitni pojavi pa so dostopni že v procesu analize in sinteze. Površina na siliciju geometrične baze sklopa kompiliranega z novo metodo je primerljiva s površino istega sklopa pri ročni optimizaciji geometričnega opisa.

Naslov naloge: **Načrtovanje, modeliranje in optimizacija integriranih vezij SC**
Avtor: **Slavko Starašinič**
Mentor: **prof. dr. Janez Trontelj, dipl. ing.**
Univerza v Ljubljani, Fakulteta za elektrotehniko in računalništvo

V delu je obravnavan celovit pristop k šumni analizi vezij *SC*, kakor tudi algoritmi za njegovo avtomatizacijo. Prav tako so podani algoritmi za sintezo posameznih gradnikov vezij SC za doseganje ustreznih šumnih lastnosti.

Izgodišče za analizo šumnih lastnosti vezij SC je obravnava le- teh v prostoru stanj. V ta namen smo izdelali šumne modele, ki opisujejo obnašanje posameznih gradnikov. S pomočjo osnovnih spoznanj o prenosu šuma od posameznega šumnega izvora do izhoda vezja je izdelana metoda za šumno analizo univerzalne bikvadratne stopnje. Ločeno so obravnavani posamezni šumni izvori v bikvadratni stopnji, kakor tudi njihov prispevek k celotnemu šumu.

Osnovna spoznanja o prenosu šuma v bikvadratni stopnji so uporabljena pri obravnavi poljubnih filtrov *SC*. Kot osnova te analize je uporabljena integratorska stopnja s poljubnim številom vhodnih priključkov. S takšno stopnjo je mogoča realizacija različnih vrst filtrov kot so lestvičasti, kaskadni, filtri z več povratnimi zankami itd. Vse te analize temeljijo na tem, da je šum operacijskih ojačevalnikov konstanten. Da bi natančneje upoštevali šumne prispevke operacijskih ojačevalnikov, smo izdelali model, ki upošteva tudi nizkofrekvenčni $1/f$ šum. Poleg šumnih izvorov v samih filtrih so obravnavani tudi dodatni izvori šuma ter drugih motenj na itegriranem vezju, hkrati pa so podane tudi rešitve za njihovo zmanjšanje. Izdelana je tudi metoda za sintezo šumnih lastnosti ojačevalnikov in za velikost kondenzatorske enote. Pri sintezi šumnih lastnosti osnovnih gradnikov je bilo izkodišče zahtevan šumni nivo celotnega vezja.

Matematični opis šumnih dogajanj v filtrih *SC* je mogoče avtomatizirati, zato smo izdelali algoritme za računalniški pristop k takšni analizi. Kot izhodišče je služil topološki opis vezja za enega od simulacijskih programov za vezja *SC*. Iz tega opisa je mogoče zapisati diferenčne enačbe, ki opisujejo celotno dogajanje v filtru *SC*.

Naslov naloge: **Vpliv mikroelektronike in informacijskih tehnologij na produkcijsko moč sistema**
Avtor: **Marko Gliha**
Mentor: **prof.dr. Lojze Trontelj**
Univerza v Ljubljani, Fakulteta za elektrotehniko in računalništvo

Že dve desetletji smo priča splošni preobrazbi industrije v razvitih deželah, ki je v nacionalnih okvirih pomenila opustitev značilnosti klasične industrijske družbe in hkrati prevzemanje novih proizvodnih in socialnih odnosov, značilnih za informacijsko družbo. Te spremembe so vplivale na splošne delovne in življenske odnose in bile so zavestno generirane s selektivnimi razvojnimi politikami. Te so sprva težile k uravnovešenju celotne industrijske in gospodarske reprodukcije na novih proporcih vrednotenja smotrne izrabe energije in surovin.

Človeštvo se je zavedalo omejenosti naravnih dobrin. Spoštovanje do Zemlje in do ohranitve življenskih pogo-

jev je vzpodbudilo mnoga družbena gibanja in jih z inštrumenti delovanja civilne družbe aktiviralo v političnem delovanju.

Vzporedno se je iskal in našel odgovor, kako in na kakšen način je mogoče bistveno vplivati na potratnost surovinskih in energetskih tokov z informatizacijo tehnoloških postopkov:

- s krmiljenjem proizvodnih in upravljalskih procesov v eksaktni in zato smotrni skladnosti,
- z razvijanjem vedno bolj učinkovitih računalnikov,
- z globalizacijo učinkovitih telekomunikacij, ki s snopi razsežnih prenosnih sposobnosti ob Zemlji in nad njo zvišujejo učinkovitost informacijskih storitev,
- z uveljavljanjem alternativnih energetskih izvirov in novih materialov,
- z industrijsko aplikacijo dosežkov visokih tehnologij, od katerih so mikroelektronske tehnologije ključne za razvoj vseh naštetih razvojnih politik.

Generične tehnologije so zato v pretežni meri mikroelektronske. Mikroprocesor, realiziran v monolitni mikroelektronski tehnologiji, je postal ključni sestav za krmiljenje procesov, za vzpostavljanje teleinformacijskih povezav in ključni člen za računalniško presojanje naravnih pojavov.

Zaradi splošnosti in mnogoternih aplikacij je mikroelektronika zavzela funkcijo učinkovite tehnologije za izjemno gospodarno proizvajanje v vseh industrijskih panogah in ne samo v matični elektronski industriji. Glede na raziskovanja in mnenja o razvojnih možnostih slovenskega gospodarstva /1/ po izbranih kriterijih (kot: delež v družbenem proizvodu, udeležba v celotni akumulaciji, možnost udeležbe v izvozu, in dr.), bi bilo smotrno prioritetno aplicirati (med drugim) krmilne, merilne in varnostne sklope visoko integrirane elektronike v industrijskih panogah, kot so:

strojegradnja,
proizvodnja prometnih sredstev,
proizvodnja električnih strojev in aparatov,
predelava kemičnih izdelkov,
proizvodnja obutve in galanterije

ter tudi v posamičnih podjetjih iz drugih sektorjev, ki izkazujejo zelo visoke performanse.

Stališče /1/ pa tudi poudarja, da bo imela aplikacija mikroelektronskih tehnologij ključno vlogo pri preobrazbi slovenskega gospodarstva. Vendar bo uspeh možen le, če bo ob tem razvita tudi ustrezna informacijska in izobraževalna infrastruktura.

Visoka učinkovitost mikroelektronskih tehnologij torej ni le v obvladovanju tehnologije same, temveč v sposobnosti izrabljanja mikroelektronskih tehnologij v široki industrijski praksi ter v relativnih družbenih in gospodarskih dejavnostih. Slovenska mikroelektronika bo zato morala biti v stalnem raziskovalnem in razvojnem stiku s svetom. Le tako bo mogoče integrirati slovensko gospodarstvo s svetovnim.

Pričujoče delo se posredno opredeljuje do vprašanj razvoja mikroelektronike na Slovenskem ter išče odgovore na vprašanja o politiki, ki naj jih država uveljavlja za pospešitev apliciranja mikroelektronskih tehnologij v industrijskih ter splošni praksi. Delo se navezuje na model razvoja tehnološkega sistema (podjetja, industrijske panoge ali industrije v celoti) /2/ ter išče v njem razvidne efekte v razvoju produkcijske učinkovitosti z gibanji v dodani vrednosti kot sestavini družbenega proizvoda. Model kaže tudi na povečano energetsko smotrnost spremenjene industrije. Poseben poudarek je dan modelu razvoja lastnega inovacijskega podsistema v industrijskih podjetjih ter oceno razvojnih trendov v spremljajoči znanosti.

Avtor se odgovorno zaveda, da so lahko izsledki raziskovanj, oz. prognoziranja na temelju predloženega razvojnega modela v veliki meri statični, da jih v gospodarski praksi lahko močno preobrača tržišče, naklonjenost ali nenaklonjenost v svetovnih razvojnih politikah, ki jih danes razvidno diktira TRIADA. Vendarle model indicira pojave ter ocenjuje moč teh pojavov, ki jih lahko z izvedbenimi politikami slovenske države spodbudimo, da bodo izkazali svojo možno razvojno moč.

Naslov naloge: **Funkcionalna semantika in formalna verifikacija sinhronih vezij**
Avtor: **Zmago Brezočnik**
Mentor: **red.prof.dr. Bogomir Horvat, dipl.ing.**
Univerza v Mariboru, Tehniška fakulteta, Elektrotehnika, računalništvo in informatika

V disertaciji predlagamo funkcionalno semantiko za sinhrona sekvenčna vezja. Temelji na monotonih funkcijah, ki preslikujejo končne nize na vhodih vezja v enako dolge izhodne nize. V tej semantiki smo definirali tri relacije skladnosti med sinhronimi vezji: ekvivalenco, relacijo "cevovod" in časovni homomorfizem. Dokažemo tudi, da je zunanja notacijska semantika ekvivalentna preprosti operacijski semantiki. Za specifikacijo zapletenega časovnega obnašanja sinhronih vezij uporabljamo TPDL funkcije.

Teoretične raziskave smo podkrepili s programskim paketom VERSYC za avtomatično verifikacijo funkcionalne pravilnosti sinhronih vezij tako na osnovi notacijske kot tudi operacijske semantike. Z njim smo uspešno verificirali že pestro množico vezij z različno stopnjo kompleksnosti, v kateri je najkompleksnejši računalnik z mikrokodirano kontrolno enoto. Primerjava doseženih rezultatov z rezultati drugih avtorjev po našem mnenju kaže na obetavnost pristopa.

Naslov naloge: **Napovedovanje časovnega obnašanja sprotnih sistemov**
Avtor: **Matjaž Colnarič**
Mentor: **red.prof.dr. Bruno Stiglic**
Univerza v Mariboru, Tehniška fakulteta, elektronika, računalništvo in informatika

Glavni predmet disertacije je napovedljivost časovnega obnašanja, ki je najpomembnejša lastnost sistemov za delo v trdem dejanskem času. Določljivost časovnega obnašanja sistemov mora biti zagotovljena na vseh nivojih njihovega snovanja. Posebej nižji nivoji, kot sta aparaturni in nivo sistemske arhitekture, so trenutno slabše obdelani, zato je poudarek dela osredotočen nanje.

Najprej smo postavili smernice za razvoj arhitekture. Poleg napovedljivosti vplivajo nanj še dosežki v razvoju polprevodniške tehnologije, razkrinkanje nekaterih predstav (npr. o hitrosti, zmogljivosti in izkoriščenosti sistema, ki nimajo pomena v okolju trdega dejanskega časa) ter zahteva po preprostosti.

V nadaljevanju je podrobneje razdelan obstoječi asimetrični arhitekturni model. Sestavljen je iz hierarhično zgrajenega procesorja jedra operacijskega sistema, ki izvaja njegove funkcije vključno z razvrščanjem opravil ter procesorja opravil, kjer se le-ta obdelujejo. Glavni poudarek naloge je na razvoju slednjega. Predstavlja celoto dveh tesno povezanih, čeprav samostojno delujočih delov, enote za krmiljenje poteka programa in enote za obdelavo podatkov.

V enoti za nadzor programa je vgrajen programski pomnilnik. Prevzeti ukazi se dekodirajo in tisti, ki krmilijo potek izvajanja programa, se tudi izvedejo. Ukazi za obdelavo podatkov se pošljejo v ustrezno enoto, kjer so le-ti dosegljivi. Lokalne spremenljivke vzdržujemo v posebej zasnovani lokalni shrambi. Zunanji podatki, kot so globalne spremenljivke ali podatki s perifernih naprav, pa so dosegljivi prek kazalcev, ki so prav tako lokalne spremenljivke. Ker pošiljamo ukaze v enoto za obdelavo podatkov v linearnem zaporedju, nam tam ni treba vzdrževati programskega števca ali drugih programskih naslovov. Operacije se izvajajo blizu njihovih objektov, nepotrebno in neproduktivno prenašanje podatkov je minimizirano.

Moduli med seboj komunicirajo prek medsebojnih točkastih (point- to-point) serijskih povezav, s čimer se izognemo očitnim problemom, ki jih vnaša skupno vodilo. Zunanje podatke prevzamemo na enotni način iz globalnega pomnilnika oz. s perifernih naprav prek za to namenjene enote. Ta omogoča tudi ustrezni način neposrednega dostopa do pomnilnika.

Predlagana arhitektura se obnaša povsem časovno napovedljivo in predstavlja temelj za nadaljnje raziskave na področju trdega dejanskega časa. Na njeni osnovi je bila narejena analiza lastnosti jezikov za programiranje aplikacij v dejanskem času. Predlagali smo nekatere modifikacije jezikov ter razvili metodo za ocenjevanje najdaljšega časa izvajanja programa, ki dokazuje, da je slednje mogoče.

Na koncu je obdelana strežba izjem, ki predstavlja resno oviro za napovedljivost časov obdelave programov. Zaradi tega skušamo preprečiti, da bi se zgodile oz. da bi prekinile delovanje programa. Za primere, ko to ni mogoče, smo razvili metodo za dosledno reševanje katastrof.

Naslov naloge: **Združevanje osnosimetričnega curka naelektrenih delcev s pomočjo toka velike gostote v osi simetrije**
Avtor: **Bojan Jenko**
Mentor: **Prof.dr. Alojz Paulin**
Univerza v Mariboru, Tehniška fakulteta, elektrotehnika, računalništvo in informatika

Hipotetična vodilnica naelektrenih delcev je izvedena s tanko superprevodno žico speljano v vakuum po osi predvidene poti snopa delcev. Namenjena je vodenju in omejevanju oziroma fokusiranju brzečih naelektrenih delcev, ki jih omejuje magnetno polje ustvarjeno zaradi toka velike gostote v žici. S tako konfiguracijo bi se izognili obsežnim elektromagnetom.

Izdelali smo matematični model, ki je omogočil računalniško simulacijo hipotetične vodilnice naelektrenih delcev.

Tirnica posameznega delca je določena analitično oziroma numerično v ravnini simetrijske osi v prostoru. Z ustrezno izbiro parametrov se krožne, cikloidam podobne tirnice naelektrenih delcev ne dotikajo tokovnega vlakna v osi simetrije. Pri tem se tirnice sekajo in tvorijo zgostitve.

Za začetno poenostavitev smo zanemarili vpliv prostorskega naboja. Najprej smo postavili matematični model za izračun neskončno dolge linearne vodilnice. V nadaljevanju smo obravnavali problem tirnic naelektrenih delcev v ravnini krožne tokovne zanke, ki je zaradi osne simetrije, z ustrezno izbranim koordinatnim sistemom, le dvodimenzionalen problem. Pri izračunu magnetne poljske jakosti v bližini krožne tokovne zanke moramo uporabljati popolne eliptične integrale v področju, ki se približuje singularnosti. Za izračun tirnic naelektrenih delcev v prostoru ob krožni tokovni zanki smo morali pripraviti nov matematični model z vektorskim pristopom. Nov model smo testirali s predhodnim modelom za primer tirnic v ravnini.

Za oceno celotne napake numeričnega izračuna smo vpeljali normo vektorja, ki najkrajše povezuje tokovodnik in delec, ki mu računamo tirnico. Pomik se prilagaja trenutnemu krivinskemu radiju, zato smo računali funkcijske vrednosti v neekvidistančnih točkah.

Dokazali smo združevalni karakter postavljenega modela ravne in krožne vodilnice. Poljubno obliko vodilnice moremo aproksimirati s krožnimi in ravnimi deli.

Prikaz doktorske disertacije: **Model visokodopiranog emitera i primjena u numeričkoj analizi bipolarnog tranzistora, avtora Željka Butkovića**

Tokom protekle, 1992. godine, na Elektotehničkom fakultetu u Zagrebu obranjen je veći broj doktorskih disertacija iz područja elektronike. Neke od njih sadrže nadprosječno vrijedne rezultate te zaslužuju širu pažnju i publicitet. Jedna od tih disertacija je disertacija gospodina Željka Butkovića s Elektrotehničkog fakulteta u Zagrebu. Disertacija je obranjena pred komisijom u sastavu prof. Petar Biljanović koji je ujedno i mentor, prof. dr. Leo Budin , prof. dr. Slavko Amon, prof. dr. Franc Runovc, prof. dr. Borivoj Modic. Naslov disertacije je "Model visokodopiranog emitera i primjena u numeričkoj analizi bipolarnog tranzistora".

Disertacija sadrži 222 stranice teksta, 92 sliku, 7 tablica i 17 stranica priloga. Disertacija ima pet poglavja, zaključak, popis referenci, te četiri dodatka. Na osnovni sadržaj disertacije upućuju naslovi poglavja:

1. Uvod
2. Visokodopirani silicij
3. Polisilicijski emiter
4. Numerička analiza bipolarnih tranzistora
5. Rezultati analize.

Dajemo kratki rezime gornjih poglavlja.

U uvodu se definira osnovna tehnološka struktura bipolarnog tranzistora u sklopovima vrlo visokog stupnja integracije s polisilicijskim emiterom dobivena primjenom metode samopodešavanja u izvedbi polisilicijskih kontakta baze i emitera. Ova struktura je danas temeljna u VLSI području integracije. Vertikalne dimenzije ovoga tranzistora vrlo su male, te je i baza vrlo uska. Dominirajući utjecaj u definiranju fizikalnih svojstava tranzistora za to pripada emiteru za razliku od " klasičnog" tranzistora gdje je dominirao utjecej pojava u bazi. Da bi se osigurao potreban iznos faktora injekcije emiter je visokodopiran donorima, međutim, on ima visoki nivo koncentracije baznih akceptorskih primjesa. Visoki nivo koncentracije primjesa u emiteru, bez obzira da li su oni donori ili akceptori, dovodi do niza pojava koji ne postoje u niskodopiranom poluvodiču. Efekt suženja zabranjenog pojasa dovodi do porasta intrinsične koncentracije s porastom koncentracije primjesa. Pri tome visoka koncentracija većinskih nosilaca djelomično deionizira dio koncentracije primjesa. Također se povećava udio Augerove rekombinacije u rekombinacijskim procesima. Ovi i slični efekti značajno reduciraju faktor strujnog pojačanja tranzistora u spoju zajedničkog emitera u odnosu na iznos kojeg bi dala klasična teorija. Situacija s emiterom postaje još složenija kada je na n^+ - dio emitera deponiran polisilicijski dio. Dobiva se veće strujno pojačanje nego u slučaju direktnog aluminijskog kontakta na n^+ - emiteru. U polisilicijskom djelu emitera dolazi do reduciranja pokretljivost nosilaca što smanjuje struju manjinskih nosilaca u emiteru i povećava strujno pojačanje tranzistora. Smanjenju struje manjinskih nosilaca pridonosi i tanki oksidni sloj između monokristalnog dijela emitera koji se stvara prilikom depozicije polisilicija.

Predmet drugog poglavlja je definiranje metoda vezanih za fizikalne efekte visokodopiranog silicija. Analiza je jednostavnija kada se analiziraju efekti visokog dopiranja u materijalu dopiranom samo jednim tipom primjesa. Međutim, realni emiteri uvijek se difundiraju ili implantiranju u relativno visoko dopirani dio baze, te se radi o djelomično kompenziranom materijalu. Kandidat zato analizira stvarnu dijelom kompenziranu strukturu n^+ - emitera. Na temelju teorijskih modela određeno je suženje zabranjenog pojasa, te udio pomaka donje i gornje njegove granice ka valentnom i vodljivom pojasu. Rezultati potrebni za proračun koncentracije slobodnih nosilaca aproksimirani su analitičkim relacijama pogodnim za primjenu u numeričkoj analizi. Definirani su modeli pokretljivosti za oba tipa nosilaca. Također su definirani i modeli rekombinacije nosilaca na bazi SRH rekombinacije i Augerove rekombinacije. Uticaj Augerove rekombinacije nosilaca ilustriran je promjenom efektivnih vremena života manjinskih nosilaca pri porastu koncentracije primjesa.

U trećem poglavju dat je prikaz svojstava polisilicija. Radi različitosti u građi u odnosu na monokristalni silicij, električka svojstva polisilicija značajno se razlikuju od električkih svojstava monosilicija. To značajno utječe na svojstva emitera kada se u njegovu strukturu u površinskom djelu ugradi polisilicijski visokodopirani dio. Za pravilan opis rada tranzistora treba odrediti model vođenja struje u polisiliciju i za većinske i za manjinske nosioce. Analiziran je utjecaj granice monokristalnih zrna u polisiliciju na zahvačanje većinskih i rekombinaciju manjinskih nosilaca. Komparirana je točnost modificiranog u odnosu na osnovni i prošireni model. Ustanovljen je utjecaj pojedinih parametra rekombinacije na struju manjinskih nosilaca. Radi narušenosti pravilnosti kristalne strukture u polisiliciju dolazi do reduciranja iznosa struja i elektrona i šupljina. Rezultat je smanjenje injekcije manjinskih nosilaca iz baze tranzistorja u emiter što dovodi do porasta iznosa faktora strujnog pojačanja, ali i do porasta parazitnog serijskog otpora emitera.

Radi karaktera kemijskih reakcija koje dovode do rasta polisilicija na monokristalnom emiteru, stvara se vrlo tanki nanometarski sloj silicij-dioksida između polikristalnog i monokristalnog dijela emitera. Nosioci kroz taj sloj prolaze tuneliranjem kroz potencijalnu barijeru. Dan je prikaz tuneliranja, te su uspoređeni rezultati dobiveni za dva oblika potencijalnih barijera.

Četvrto poglavlje prezentira rezultate provedene numeričke analize npn bipolarnog tranzistora s metalnim i polisilicijskim kontaktom. Izabrani su tehnološki profili plitkih submikrometarskih struktura tipični u VLSI sklopovima. U npn tranzistoru s metalnim emiterskim kontaktom naročita je pažnja posvećena utjecaju efekata visokog dopinga na električke karakteristike. Posebno je analizirani utjecaj kompenzacije primjesa na iznos intrinsične koncentracije, te utjecaj razlike pokretljivosti većinskih i manjinskih nosilaca. Pokazan je velik utjecaj efekata visokog dopinga na točnost određivanja faktora strujnog pojačanja. Situaciju u degeneriranom emiteru čini još složenijom sloj polisilicija na strukturi emitera. Uključivanjem modela polisilicijskog sloja i oksidnog sloja između polisilicijskog i monosilicijskog dijela emitera u program za numeričku analizu omogućen je znatno realniji proračun utjecaja oba sloja na rad tranzistora. Dobiveni rezultati pokazuju da je utjecaj oksidnog sloja na rad tranzistora znatno jači od utjecaja polisilicijskog sloja. Polisilicijski sloj povećava faktor strujnog pojačavanja u spoju zajedničkog emitera oko 3 puta, dok oksidni sloj debeljine 1,5 nm unosi porast oko 14 puta, u odnosu na strukturu tranzistora s metalnim kontaktom.

Disertacija kandidata Željka Butkovića predstavlja vrijedan znanstveni rad s originalnim doprinosom u području numeričke analize i modeliranje svojstava bipolarnih tranzistora. Pri tome su korištena najnovija saznanja o strukturi tranzistora i brojni eksperimentalni rezultati niza autora koji su dobra priloga za provjeru točnosti ugrađenih modela. Kompleksnim pristupom analizi i cjelovitošću dobivenih rezultata autor pokazuje da je sposoban rješavati najsloženije probleme iz analize i modeliranja integriranih bipolarnih tranzistora.

Odlukom znanstveno-nastavnog vijeća Elektrotehničkog fakulteta u Zagrebu disertacija je na sjednici Vijeća do 12.12. 1992. nagrađena Srebrnom plaketom "Josip Lončar" koja se jednom godišnje dodjeljuje za najbolju doktorsku disertaciju u području elektrotehnike i računarstva obranjena u toj godini na fakultetu. Nagrada je uročena na Svečanoj sjednici Vijeća 15. siječnja 1993.

Iskoristimo ovu priliku da gospodinu Želju Butkoviću čestitamo u ime MIDEM-a i na lijepoj disertaciji i na nagradi "Josip Lončar".

Prof. dr. Petar Biljanović
Elektrotehnički fakultet Zagreb
Prikaze doktoratov sta pripravila
R. Babič in I. Šorli

VESTI

NEW HANDSFREE MONITOR AMPLIFIER WITH TONE RINGER CIRCUIT

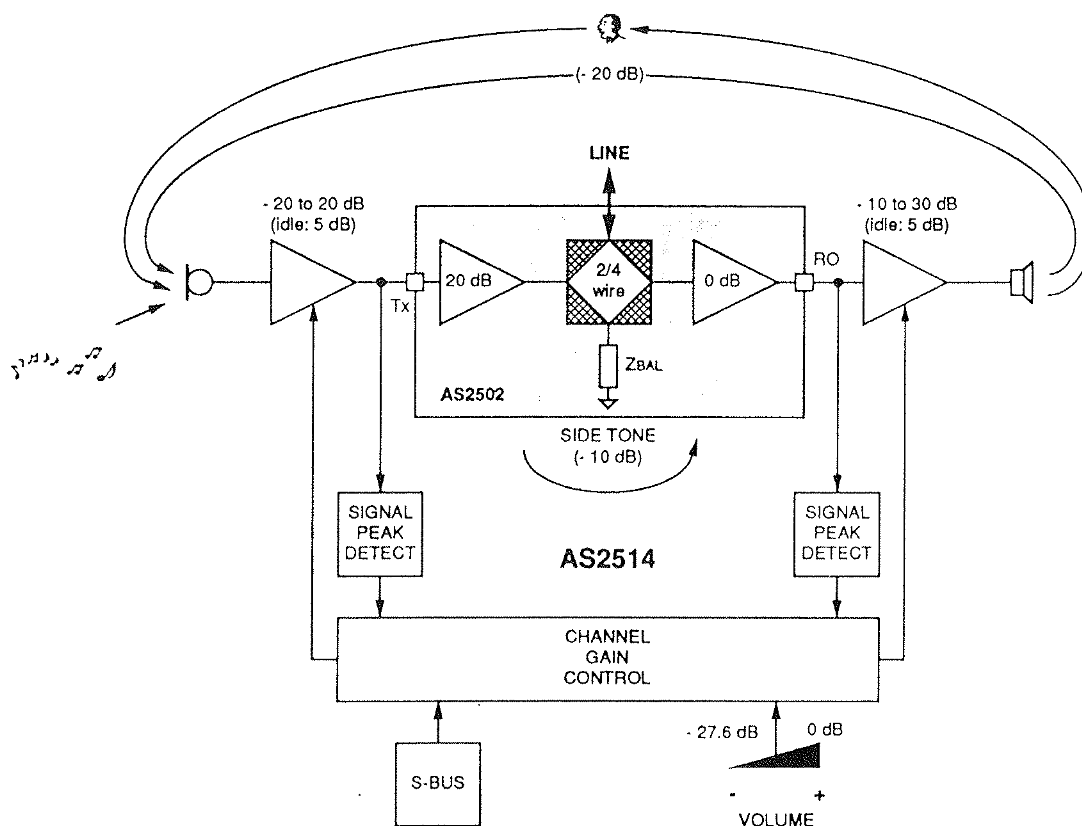
AMS announces the immediate availibility of a completely new ASIC for the telecommunications market - the AS 2514, a handsfree monitor amplifier with tone ringer circuit. The AS2514 is an integrated circuit in CMOS technology that performs three main functions: loudhearing, handsfree and tone ringing.

The device which operates from 4V to 6V contains a high performance loudspeaker amplifier with a voice switching circuit and enhanced tone ringer circuit with serial interface. The loudspeaker amplifier incorporates an anti-clipping circuit (AGC) to provide low distortion when the required output level exceeds the capabilities of the available supply current. The voice switching circuit prevents acoustic feedback, so-called howling, between the loudspeaker and microphone.

The combination of handsfree and tone ringer using the same monitor amplifier allows common use of the loudspeaker - both for handsfree and tone ringing.

A switching converter is used to extract the available power from the ring signal. The frequency comparator assures that the melody generator is activated only when a valid ring signal is applied. The device, available in 28 pin DIP or PLCC packages, is programmed via a serial bus or by pin options.

The AS2514 is compatible with the AMS AS2575D or AS2577 diallers and the AMS AS2502A line adapter circuit. Together, these circuits - the use of an EEPROM is optioonal - provide a fully electronic analogue telephone adaptable to various national PTT requirements.



This new highly integrated AMS product with its novel features is a part of an AMS Telecom IC Family that provides telephone manufacturers with a cost-efficient and flexible concept. For a free data sheet and futher information please contact your local AMS Sales Office or AMS Corporate Communications, Schloss Premstätten, A-8141 Unterpremstätten, Austria.

AMS Press Release
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NEW AMS PROCESS TECHNOLOGIES FOR TELECOMMUNICATIONS PRODUCTS

AMS announces the introduction of new process evolutions specially suited for telecom applications:

- ☐ 0.8 and 1.2 micron BICMOS processes for mobile telecommunications-e.g. high speed digital and RF applications
- ☐ 1 micron double--metal 5V CMOS process
- ☐ 1 micron double-metal CMOS process for mixed analogue digital signal processing
- ☐ 1.2 micron double-metal double-poly 5V CMOS process
- ☐ 2 micron double-metal 35 V CMOS process

Lowest power consumption, high speed, noise immunity and applicability to a wide range of telecommunication design requirements are the key benefits of the advanced CMOS processes. And, with the introduction of mixed mode BiCMOS processes, AMS is well prepared for the high growth market segments of broadband transceivers (SONET, SDH, ATM) and wireless voice/data communications.

The new processes complement AMS' traditional processes for telecom products:

- ☐ 2 micron 5V double-metal twin tub CMOS process for high speed digital signal processing applications
- ☐ 2 micron 5V double-poly double-metal CMOS process for analogue/digital applications
- ☐ 3 micron double-poly double-metal CMOS process for mixed analogue and digital applications
- ☐ 5 micron 15V silicon-gate double-poly CMOS process for mixed analogue and digital applications

Since all AMS processes are compatible to processes run by major manufacturers, alternative sourcing can be accomodated at minimal effort. Because of AMS' parallel support of new, traditional and mature process technologies, AMS' process flexibillity guarantees the duration of any one process as long as a specific telecommunication product is required, enabling a long-term availability of the telecom circuit. Not AMS but the customer decides when he wishes to migrate to an advanced process technology and AMS will guarantee a smooth migration of any product without any risk.

AMS now has over 40 proven BiCMOS and CMOS processes.

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SUPERCONDUCTORS MAKE MULTICHIP MODULE FAST

Using superconducting interconnects on MCMs reduces interchip delays to nothing

When superconductivity burst onto the scene in 1986, pundits predicted it would revolutionize computation, transportation, energy, medicine, and a host of other applications. Six years later, it remains a somewhat obscure techology.

But there are signs that superconductivity may be finding a place in commercial applications. Today, Semiconductor Technologies, Inc. of Santa Barbara, Calif., announced it had successfully fabricated the first multichip module containing superconducting interconnects.

The company constructed a 2-in.-square lanthanum aluminate wafer, and deposited 10 micron-wide superconductor interconnects on this substrate. To this prototype. STI added gold contacts for connecting CMOS die. Then, it connected 10 CMOS units-inverters and counters-to the substrate.

"We're nine months into a three-year program says Jim Bybokas, vice president of product marketing at STI. The $6 million contract from DARPA, the Defense Advanced Research Projects Agency in Arlington, Va., aims to produce commercial multichip modules for military computing applications.

Bybokas explains that MCMs with superconductor interconnects solves a number of the bottlenecks confronting high speed digital circuits. Superconductor traces can be very small and tightly spaced. The STI project's goal is to achieve two micron-wide traces spaced 2 μm apart.

Thus CMOS die with large numbers of I/0s can be connected up with no performance penalty and no trace-to-trace signal interference. A superconductor exhibits no stray capacitance or inductance.

At 77 degrees Kelvin (minus 200 °C)-the temperature of liquid nitrogen - the trace is a perfect conductor. By bokas says another benefit is that cooling CMOS chips to this low temperature also improves the performance of these circuits fourfold.

As for cooling superconductor MCMs, Bybokas says the technology is well understood and points to extensive use of cryogenically cooled microwave electronics in the Desert Storm Campaign.

For all of its benefits, STI's innovation is three to five years from practical commercial use. Nevertheless, this first step points the way for superconductors into computer systems.

Electronics, 10 August 1992

By Jonah McLeod, Santa Barbara, Calif.

A TAIWAN FIRST : 0.7 - micron ICs

Taiwan produced its first 0.7-micron resolution chips on an 8- inch wafer with more than 70 percent yield, marking a milestone in the island's continuous endeavor in the development of submicron-resolution technology for IC fabrication.

C.Y. Lu, head of the team on Submicron ULSI (ULTRA-LARGE SCALE INTEGRATION) IC Development, announced in mid-November the successful test of the pilot-line sub-micron facility for 8-inch wafers.

The new US $ 120 milion 30.000-square meter facility located inside the Hsinchu Science-based Industrial Park, Taiwan's flagship high-tech industrial zone, is part of the island's ambitions 1991 - 1995 project to push the IC resolution to 0.5- micron and to catch up with the industrially advanced nations.

"We aim to bring Taiwan's industry from "post-peak era" to "pre- peak era" said Lu, whose official position is the Deputy General Director of the Electronics Research & Service Organization (ERSO), a branch of the government-subsidized Industrial Technology Research Institute located in Hsinchu.

The project started as a consortium undertaking to distribute the risk. ERSO, Taiwan Semiconductor Manufacturing Co. (TSMC), United Microelectronics Corp. (UMC) and several other companies put up the venture capital in exchange for the early-licensing privileges, the priority to use the facility and technology.

Lu said the technology is comparable to that of the medium-sized National Semiconductor Corp. of Santa Clara, Calif., and Advanced Micro Devices Inc. of Sunyvale, Calif., as well as Europe's Philips Electronics NV of Eindhoven, the Netherlands, and SGS- Thomson Microelectronics NV of Agrate Brianza, Italy.

"We'll be catching up with the technology of (Munich) Germany's Siemens (AG) in the near future" said Lu.

TSMC and UMC already expressed interest in transferring the technology to their own production lines. Five other consortium members-Mosel Vitelic Inc., Winbond Electronics Corp., Holtek Microelectronics Inc., Macronix International Co., Ltd. and Eltron Technology Inc.- will be served by the ERSO facility. All seven companies and the processing facility are located in the Hsinchu Industrial Park.

Electronics, 14 December 1992

By Charlene Huang, Taipei, Taiwan

TI's Prism achieves on-resistance breakthrough

With the problem of isolating the logic circuits from power transistor noise solved, the challenge to smart power developers has been to design ever-smaller power transistors with ever-lower on-resistance. Texas Instruments Inc. of Dallas has answered that challenge with its new Prism smart power process, announced last month.

TI says the Prism smart power process achieves 310 ohms of on- resistance-nearly half of the 600 ohms that had been considered state-of-the-art-using an 0,8-micron process.

To do this, the company developed a lateral DMOS (double-diffused metal-oxide semiconductor) transistor structure to replace the vertical structure IC manufacturers have used until now. Other IC vendors use a vertical transistor structure to reduce the silicon real estate in the 2- and 3- μm processes they employ to make their smart power devices. These smart power devices contain a large silicon area-over 70 percent of the total area - containing the power transistor and a smaller area with logic circuits.

Because TI uses the smaller 0.8- μm, it can use the lateral transistor structure.

To reduce on-resistance and thus increase the efficiency of a Prism device, TI developed patented features in the transistor structure.

Electronics, 26 October 1992

By Jonah McLeod, Dallas

IBM's tiny transistor opens way for 4-Gb DRAMs

An experimental transistor - the world's smallest ever-developed by IBM researchers, indicates that scaling of conventional memory and logic devices can be carried much further than previously thought posible. The transistor, measuring only 700 nm by 150nm, is a silicon n-channel MOS FET with conventional characteristics. According to IBM, the technology ultimately could lead to 4-Gbit or even denser memories. **And the researchers claim the device can be shrunk by another factor or two.**

Previously, it was thought that structures of these dimensions would exhibit or require quantum effects or unique properties that could be exploited in so-called quantum devices to achieve electronic functions. But according to Fritz Hohn, program manager for lithography technology at IBM's Research division in York-town Heights, N.Y., quantum devices are nowhere near real commercial applications. The ability to scale conventional well-understood devices down to nanometer dimensions - not previously imagined - could provide new approaches to very dense memories and logic chips.

Up to now, the devices have only been tested manually for their static I - V characteristics. They operate at less than 2 V. Hohn says that the research team hopes to report switching times and other dinamic performance characteristics at the next International Electron Devices Meeting in the fall.

The researchers conservatively project commercial production of devices using this technology at somewhere in the first decade of the 21st century. But Hohn says that the novel technology features that have been demonstrated may be applicable to less ambitious devices than 4-Gbit memories.

Electronics, 13 July 1992

· *By Samuel Weber, Yorktown Heights, N.Y.*

RESEARCH ADVANCES TOWARD THE "ULTIMATE SWITCHING DEVICE"

The most miniature of electronic devices, the single-electron transistor may become a reality - but not for about ten years. So predicts Pierre Gueret of IBM's Zurich Research Laboratory in Ruschlikon, Switzerland, who presented a paper outlining the design of just such a device at Hitachi's Central Research Laboratory in Kokubunji.

The work of Gueret and his co-researchers at IBM is based on a classical- regime phenomenon, known as Columb blockade, in which a single electron is transferred across the plates of a capacitor. (In this realm of the very small, the key mechanism by which charge transport occurs is tunneling-that is, the transfer of an electron across what would normally be viewed as a non-conductive barrier.) They apply this concept to the fabrication of a submicron size three-terminal structure in which a 1000-nanometer quantum dot (a region which confines electrons) is fabricated in a semicondutor substrate by growing successive layers using molecular beam epitaxy. The single electron tunnels through the quantum dot.

"This would be the ultimate switching device", Gueret told Electronics. "However, when working with one electron, there is a problem with speed". With logic, other gates and circuits must be switched through the current sent over the connecting transmission lines, since there's not much current associated with a single electron. To solve this, very short transmission lines are needed. "In principle, this can be done", asserts Gueret adding, in terms of capacity,**a shift from the currently - used 0.1- μm technology to 0,01 μm fabrication could result in 1 terabit (trillion bit) memory devices.**

Electronics, 28 September 1992

By Stuart M. Dambrot, Kokubunji, Japan

3-Volt IC Market
Strategies and Forecast

Why 3-Volt ?

The market for new-design 3-volt integrated circuits is growing at a compound average rate of over 150 % trough 1997, according to this new report. Meanwhile, the overall IC market is predicted to grow at a more sedate 14,5 % average rate trough that period.

Clearly 3-volt ICs present an opportunity for the agile IC vendor to grow far faster than the industry norm

Consumer demand for longer battery life in portable electronics and industrial demand for reduced power consumption are coinciding with the need to maintain device reliability as IC geometries continue to shrink. From a practical standpoint, reduction of IC power supply voltages from the traditional 5-volt supply to a new 3-volt standard fulfils these needs. The industry conversion is occurring in two steps.

- ☐ **Existing 5-Volt ICs are being quickly recharacterized and derated for lower-performance 3V operation**
- ☐ **New 3-Volt designs of yet higher performance are slowly beginning to supplant earlier 5V designs**

Although new portable applications like notebook computers and cellular subscriber phones get most of the press, **the biggest motivator to move quickly to 3 volts proved to be the overall lower power consumption** rather than portability. Yet, **portability** was a strong **number-two** reason for the move.

The overall lower power consumption not only improves portability but enables **dramatic IC price reduction in some cases.** That is because cheaper plastic **quad flatpack** (QFP) packaging can often replace expensive ceramic **pin grid arrays** (PGAs) which enables use of cheaper all-surface-mount motherboards and at the same time leads to simpler, cheaper cooling systems.

Other observations from the survey conclude that:

- ☐ The **greatest need** for low-voltage ics was for **low-power MPU/MCUs & DSPs.**
- ☐ Suppliers **thing low-voltage PLDs are nearly as important as MPU/MCUs, but** users **saw them as being** one of the least important elements.
- ☐ Cost and reliability were not **factors of** major concern **to users.**
- ☐ Major **inhibitors** to low-voltage IC use are **device availability and compatibility** with existing systems.

The user demands of the truly portable PC have changed the **classical** order of IC **development priorities** from **performance, density, cost and power** to **power, density, cost and performance.** Meanwhile hig-speed CPUs are demanding high density and high performance which will only be met by power supply voltage reduction. **For instance, if all the core logic in a PC motherboard is designed for 3-volt operation, it will save its designer 60 percent of the power of an equivalent 5-volt design, just through the device physics. Power management techniques can enable even greater power savings.**

Forces Driving to 3 Volt Devices

- ☐ Device physics effects demand reduced voltage to maintain reliability. Device issues addressed include.
- – **short-channel effects - hot electron injection - subthreshold turn-on**
- ☐ Power dissipation reduces as the square of the supply voltage
- ☐ Switching noise is reduced with lower voltage

Mixed-Voltage Systems

Not system components will immediately be available for low- voltage operation. This means that mixed-voltage electronic systems are, and will continue to be required. Many schemes can be used to accommodate these mixed voltage systems, but each comes with a price. Some **Options** described include:

- ☐ **Buffering 5V ICs to a 3V main bus with voltage transducers or vice versa.**
- ☐ **Run 5V parts at 3V and possibly a lower clock rate.**
- ☐ **Design ICs for 5V I/O but run them internally at 3V-an early DRAM design choice made by some vendors.**
- ☐ **Recharacterize a 5V part for 3V operation, then run it at 5V when high speed is required and at 3V when power savings are required.**

Designing an IC at 3 V for full-speed operation has been found to be difficult and often results in expensive chips. ASICs were among the first to convert to 3V, followed by MPUs/MCUs and finally by memory. Analog devices are trailing the conversion trends.

The Worldwide IC Wafer Fabrication Foundry Market

The cost of establishing an IC fab with a capacity of 10.000 wafer starts per month will increase tenfold from $200 milion in 1992 to $2 bilion by the year 2000. Submicron fab costs are forecasted to exceed $2 billion by the end of this decade (attaining 0,12 micron pitches).

As a result more and more companies have turned to third party foundries to do their IC fabrication. **At last count more than 100 companies use IC wafer fab foundry services.**

Electronic Trend Publications'newest report, **"The Worldwide IC Wafer Fabrication Foundry Market"** forecasts the total Worldwide IC foundry service business will grow from $2.2 bilion in 1992 to $7.7 bilion by the year 1997.

In 1992, the U.S. represented 36% of the worldwide IC fab foundry market; Europe 25%, 16% in Japan and 23% rest of the world (ROW).

The reasons why semiconductor companies purchase IC fab foundry capacities are primarily fourfold:

1. They do not have their own fabs (they are fabless).
2. To add required additional short term fab capacity.
3. They do not have the type of process required.

4. While old fab facilities are shut down and being upgraded to meet their advanced fab process requirements.

More than forty semiconductor companies worldwide with a total of twice as many fab sites currently offer foundry services and are profiled in the report.

Fabless companies use foundries for all kinds of devices, including memories and microprocessors. Other companies use foundry services mainly to produce application specific integrated circuits (ASICs) and application specific standard products (ASSPs). These are devices used for a specific application and are typically produced in relatively limited series. As users stay away from standard semiconductor devices for these applications for economic or political reasons, they have to rely on ASICs and ASSPs made in limited series.

Foundry services are typically used for the fabrication of telecommunications, microprocessor, memory and embedded computer devices. High quality, speed and reliability are also frequent selection criteria.

From IPI Presents

POSLOVNE NOVOSTI

POLUVODIČKA INDUSTRIJA U ČEŠKOJ I SLOVAČKOJ

Čehoslovačka poluvodička industrija uspješno je slijedila svjetski razvoj negdje do kraja šezdesetih godina. Poslije toga zaostajala je sve više i više. Zaostatak je nastao prvenstveno zbog nedovoljnoga investiranja u razvoj i zbog zatvorenosti prema većemu dijelu svijeta. Uočivši problem država ga je početkom osadesetih pokušala riješiti osnivanjem federalnoga ministarstva elektrotehničke industrije. Međutim i dalje se razvoj temeljio na konceptu zatvorene ekonomije i zahtjevu samodovoljnosti u pogledu asortimana i količina.

Českoslovačka poluvodička industrija izgubila je priključak na svjetski razvoj usprkos znatnim državnim investicijama osamdesetih godina. Spomenimo da je u razdoblju 1987-1989 u tvornici TESLA-Pieštani izgrađivan čisti prostor ukupne površine 5000 m^2 za standardne klase 1000, 100 i 10. Bilo je predviđeno procesiranje pločica 100 mm promjera s litografijom 1.2 μm. Taj projekt nije nikada dovršen, jer je država poslije društvenog prevrata 1989. prekinula financiranje.

Českoslovačka poluvodička industrija bila je ranije orijentirana na zadovoljavanje potreba domaćega tržišta i izvoz u druge istočnoevropske zemlje. Poslije društvenih promjena dogodilo se da su tržišta u tim zemljama odumrla. Posebno se to odnosi na raniji Sovjetski savez i DDR. Doda li se tome da je domaća proizvodnja finalnih elektroničkih proizvoda znatno smanjena, da su granice otvorene uvozu iz razvijenijih zemalja nije iznenađujuće da je proizvodnja i plasman domače poluvodičke industrije u velikome padu. U tvornici TESLA-Pieštani, na primjer, proizvodnja u odnosu na 1989. godinu pala je na jednu trećinu, a broj zaposlenih s 5000 na 2500. Neke firme su potpuno prestale proizvoditi poluvodiče orijentirajući se na druge proizvode, a druge firme reorganizirale su se u nekoliko nezavisnih kompanija sa smanjenim brojem uposlenih. Tako je postupljeno u najvećem českoslovaćkom poduzeću za proizvodnji poluvodiča firmi TESLA-Rožnov. Sve tvornice traže nova tržišta u zapadnim zemljama i traže zapadne partnere. Tako je tvornica TESLA-Pieštani uspostavila suradnju s Motorolom Evropa u proizvodnji integriranih sklopova, dioda i tranzistora.

Motivi zapadnim firmama za suradnju s bivšom češkoslovačkom poluvodičkom industrijom su jaki timovi poluvodičkih specijalista, proizvodni prostori, infrastruktura i relativno niske plaće u Češkoj i Slovačkoj.

Podjela Čehoslovačke na dvije države zaplašila je neke potencijalne zapadne partnere. U plus Češkoj i Slovačkoj može se upisati da kod njih situacija nije ni približno kao na prostorima bivše Jugoslavije i da se kod njih situacija razvija tako da investicije neće biti ugrožene. Bivša čehoslovačka poluvodička industrija mogla bi uspješno preživjeti teško razdoblje revitalizacije i mogla bi ubuduće zauzeti svoje mjesto na svjetskome tržištu.

(Uz neznatne izmjene članak je preuzet iz "European Semiconductor", oktobar 1992.)

NOVI KAPACITETI MOTOROLE U ŠKOTSKOJ

U toku je velika investicija Motorole u tvornici u "East Killbride" u Škotskoj. Radi se o nabavci nove opreme koja će biti instalirana u postojećim pogonima MOS 1 i MOS 9. Od ukupne investicije od približno 75 miliona $ približno polovica će se potrošiti u pogonu MOS 9, gdje će biti instalirana oprema za procesiranje litografijom 0.5 µm. na pločicama promjera 150 mm. Sada rade s litografijom 1.5 µm. S tom litografijom proizvode mikroprocesore i memorije. Proizvodi u tehnologiji 0.65 µm pojaviti će se na tržištu ove godine. Planiraju proizvoditi 6/24 bit signal procesore, 16 i 32 bitne modularne mikrokontrolere, digitalno analogne MOS komponente po zahtjevu kupca i brze statičke RAMove. Statički RAMovi bi u 1994. trebali preći na litografiju 0.5 µm, a ostale komponente to isto u 1995.godini.

Pogon MOS 1 će biti osposobljen za proizvodnju u geometriji 1µm. Do sada je pogon MOS 1 proizvodio u geometrijama 1.8 µm do 8 µm. Taj pogon postavljen je još 1972.godine, ali je još uvijek operativan.

Od ukupne investicije svega 10% će biti utrošeno za nabavku opreme u Evropi, a ostatak u SAD i Japanu. U Motoroli smatraju da u Evropi ne postoji industrija proizvodne opreme za procesiranje s litografijom 0.5 µm. Takva industrija je danas u SAD i Japanu.

Vrijednost opreme za testiranje, koja se nabavlja predstavljati će oko 20% ukupne investicije. Motorola naručuje dva ili tri najsuvremenija 3324 ATE sistema. Teradyne J971 sistem nabavljen je prošle godine i postavljen u posebno klimatiziranoj prostoriji.

Kapaciteti montaže neće se povećavati ali će biti proširen asortiman kućišta. Kupci sve više traže QFP (quad flat pack), pa motorola kupuje QFP dodavače za testere.

Istovremeno s unapređenjem tehnologije u Motoroli moraju povećati kapacitet proizvodnje, da bi udovoljili povećanim zahtjevima. Porast prodaje kod Motorole je 1992. godine u odnosu na predhodnu godinu iznosio oko 20%. Modernizirani pogoni iz East Killbride isporučivati će čipove za Philips, Bosch, Siemens, Blaupunkt, Fiat, VW i ostale kupce u Evropi. Jasno da će dio proizvodnje plasirati i van Evrope.

Nova investicija omogućiti će povećanje broja zaposlenih u "East Killbride" za 150.

Očekuje se da će tvornica u "East Killbride" biti prva u Evropi koja u tehnologiji 0.5 µm može pružiti kompletan servis od projektiranja čipa do finalnog testiranja.

DEC GRADI NOVE POGONE

"Digital Equipment Corp." započela je prošle godine izgradnju novih pogona za proizvodnju slijedeće generacije Alfa familije 64 bitnih mikroprocesora. Proizvodnja čipova u novoj tvornici trebala bi započeti 1996.g. U DEC-u vjeruju da će nova tvornica biti jedna od najmodernijih, u svijetu. Tvornica će biti trokatna građevina s približno 40.334 m površine plus posebno izgrađenih 7600 m i 818 m podzemnih tunela. Proizvodnja će biti smještena u čistom prostoru, klasa 1, površine 5950 m. Koristiće pločice promjera 200 mm. Prilikom projektiranja i izgradnje tvornice posebna pažnja poklonjena je zaštiti okoline. Zahvaljujući najsuvremenijoj tehnologiji prečišćavanja i recikliranja otpadnih materijala tvornica neće ispuštati u okolinu nikakave štetne ili opasne materije. Planira se da će tvornica jednom pokrenuta raditi neprekidno 24 sata dnevno, 7 dana tjedno.

SVJETSKO TRŽIŠTE POLUVODIČA PO REGIJAMA

U tablici je pokazan pregled stanja i predviđanja svjetskog tržišta poluvodiča po glavnim regijama. Uočljiv je prilično stabilan porast prodaje u svim regijama osim u Japanu, gdje je 1992. zabilježen pad. Ipak Japan i nadalje ostaje najveće tržište s približno 35% svjetske potrošnje poluvodiča.

USA	15.376	17.572	20.136
Evropa	10.115	11.023	12.071
Japan	20.935	19.526	21.631
Ostatak svjeta	8.181	10.224	12.08
Svijet ukupno:	54.607	58.345	65.919

(Podaci preuzeti iz "European Semiconductor", septembar 1992.)

ELEKTRONIKA 92 - MÜNCHEN

Jedan posjetilac izložbe ELEKTRONIKA 92 rekao je da se izložba najbolje može opisati riječima "VEĆE" i "BOLJE". Za ovaj broj časopisa napravili smo zabilješku o nekoliko novih modernih komponenata, koje su se mogle vidjeti na sajmu.

Hal-efekt senzor u CMOS tehnologiji

U laboratorijima ITT-Semiconductor (Intermetall Gmbh Div. Freiburg, BRD) razvijen je prvi Hal-efekt senzor u CMOS tehnologiji. Senzor je namijenjen za rad pri temperaturama od -40°C do 150°C. Ovaj senzor je projektiran da bi bio superiorna zamjena uobičajenim bipolarnim i hibridnim Hal-efekt senzorima, koji su skuplji i netočniji.

Primjenjen je 1.2 μm CMOS proces. Na čipu su smješteni: osjetilni elemenat, predpojačalo, ofset kompenzacioni sklop, komparator i interni stabilizator napona.

Nove diode

Zetex Plc, Oldham, UK je razvio diode srednje snage koje nude neke prednosti pred šotki diodama a koštaju pola cijene. Diode su prvenstveno namijenjene projektantima DC-DC pretvarača.

Ista kopanija izložila je naponsku referencu visokih performansi i tri- terminal naponski regulator za površinsku montažu.

Zanimljiv je "semicustom gate array", koji se može prilagoditi posebnoj primjeni sa softverom definiranim od korisnika.

Spomenimo da je kompanija Zetex izložila i 1 W PNP verziju vrlo poznatoga NPN tranzistora s najvišim performansama ZTX 950.

TEHNOLOŠKE NOVOSTI

POWER ASIC TECHNOLOGY MOLDS 1-MHZ SWITCHERS

A practical power ASIC technology has created the first high-power IC pulse-width-modulated (PWM), 1-MHz switching-regulator chips: the HIP 5060, the dual HIP 5062, and HIP 5063. Jointli developed by Harris Semiconductor, Melbourne, Flo.; IBM Còrp. Endicott, N.Y.: and Cadence Design Systems, San Jose, Calif., the chips, when combined with IBMs power-IC packaging technology (now available to the outside world), enable 50-to-100-W Dc-Dc converters to be constructed with power densites exceeding 50 W/in^3. IBM designed the basic circuits of the switchers using the Harris Power ASIC cell library and the CAE tools in Hariss mixed-signal Fastrack ASIC design system. Although Fastrack is available for use with all Harris power and mixed-signal ASIC processes, IBM chose the Harris PASIC-1 (Power ASIC-1) technology and helped develop its cell library. The proccess builds 60V lateral DMOS n-channel power FETs, 15-V p and n chanel MOSFETs; vertical NPNs with an f_T of 1500 MHz; slow lateral PNPs; and 5-V to 15-V CMOS logic.

Though the three chips are similar, each has its own unique applications. When designed into a power supply, the lateral power FETs in oll three can switch 10 A at 60 V in under 3 ns at 1 MHz. The 3 ns switching time minimizes switching loses, eliminating the need to go to resonant-mode converter topologies. At present, only die are avaliable from Harris. But they can be used with the IBM termal-carrier technology. Harrris is considering several multi-pin surface mountable packages that can dissipate up to 40 W. For Harris regulator-IC information call Dean Henderson at (070) 755-4526 or 1(800)4-Harris ext.7048. For IBM power die packaging technology information call (607)775-6937.

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(Popis knjiga preuzet je iz časopisa "Electronic Design", a na osnovu podataka od "Stacey's Bookstore", 219 University Ave., Palo Alto, CA 94301: (415)325-0681; fax (415)326-0693.)

Zbrali in uredili
Iztok Šorli
Miroslav Turina
Rudi Ročak

DRUŠTVO ZA VAKUUMSKO TEHNIKO SLOVENIJE
SLOVENIAN SOCIETY FOR VACUUM TECHNIQUE

INŠTITUT ZA ELEKTRONIKO IN VAKUUMSKO TEHNIKO, Ljubljana, Teslova 30

IZOBRAŽEVALNI TEČAJI v letu 1993

Vse uporabnike vakuumske tehnike obveščamo, da so v letu 1993 predvideni naslednji strokovno izobraževalni tečaji:

VZDRŽEVANJE VAKUUMSKIH NAPRAV - 11. in 12. maj ter 13. in 14. oktober 1993

Obravnavana bo predvsem tematika, ki jo srečujemo v tehniki grobega vakuuma. To je: delovanje, vzdrževanje in popravila rotacijskih črpalk, pregled in uporaba različnih črpalk, ventilov in drugih elementov, meritve vakuum, hermetičnost in odkrivanje netesnosti v vakuumskih sistemih, materiali za popravila, tehnike čiščenja in spajanja, skupno 16 ur, od tega tretjina praktičnih prikazov in vaj. Cena tečaja je 15.000 SIT. Vsak tečajnik prejme tudi brošuro "Vzdrževanje vakuumskih naprav" in potrdilo o opravljenem tečaju.

OSNOVE VAKUUMSKE TEHNIKE - 8., 9. in 10 junij ter 9., 10. in 11. november 1993

Ta tečaj je popolnejši od prvega, obravnava podrobneje vsa prej omenjena področja in poleg tega še: pomen in razvoj vakuumske tehnike, fizikalne osnove, črpalke za visoki vakuum, tankoplastne in druge vakuumske tehnologije, čiste postopke, analize površin ter doziranje, čiščenje in preiskave plinov - skupno 20 ur z vajami in ogledom Inštituta. Cena tečaja je 13.500 SIT. Udeleženci prejmejo zbornik predavanj "Osnove vakuumske tehnike" in potrdilo o opravljenem tečaju.

Vsi tečaji se pričnо v torek ob 8.00 uri v knjižnici Inštituta za elektroniko in vakuumsko tehniko, Teslova 30, Ljubljana. Prosimo interesente, da se informativno javijo čimprej, za dokončno potrdilo udeležbe pa velja kopija položnice o plačilu - najkasneje tri dni pred pričetkom tečaja na naslov: Društvo za vakuumsko tehniko Slovenije, Teslova 30 61111 Ljubljana (štev. ŽR: 50101 - 678 - 52240). Prijave sprejema organizacijski odbor (Koller, Spruk, Mozetič, Nemanič), ki daje tudi vse dodatne informacije (tel.)61 263 - 461).

KOLEDAR PRIREDITEV 1993

JUNE

02.06-04.06.1993 TECHNOVA INTERNATIONAL
GRAZ, Austria

15.06.-19.06.1993 BIOWASTE
HERNING, Denmark

JULY

12.07.-15.07.1993 1st EUROPEAN CONFERENCE ON HARD COATINGS
ALICANTE, Spain

SEPTEMBER

05.09.-09.09.1993 IMEKO XIII FROM MEASUREMENT TO INNOVATION
TORINO, Italy

06.09.-09.09.1993 EuMC'93 EUROPEAN MICROWAVE CONFERENCE
MADRID, Spain

06.09.-10.09.1993 VLSI 93
GRENOBLE, France

06.09.-10.09.1993 ICTF 9 9th EUROPEAN CONFERENCE ON THIN FILMS
VIENA, Austria

13.09.-17.09.1993 EPE'93 5th EUROPEAN CONFERENCE ON POWER ELECTRONICS AND APLICATIONS
BRIGHTON, England

29.09.-01.10.1993 MIEL-SD 93 21 th INTERNATIONAL CONFERENCE ON MICROELECTRONICS
BLED, Slovenia

OCTOBER

05.10.-098.10.1993 SODOBNA ELEKTRONIKA 93
LJUBLJANA, Slovenia

06.10.-08.10.1993 44.POSVETOVANJE O METALURGIJI IN KOVINSKIH GRADIVIH IN 1.POSVETOVANJE O MATERIALIH
PORTOROŽ, Slovenia

07.10.-08.10.1993 ISPE 93 INTERNATIONAL SYMPOSIUM ON ELECTRONICS IN TRAFFIC
LJUBLJANA, Slovenia

07.10.-08.10.1993 VAES 93 INTERNATIONAL SYMPOSIUM ON CONTROL AND AUTOMATION OF ELECTROENERGETIC SYSTEMS

19.10.-23.10.1992 SITEF
TOULOUSE, France

NAVODILA AVTORJEM

Informacije MIDEM je znanstveno-strokovno-društvena publikacija Strokovnega društva za mikroelektroniko, elektronske sestavne dele in materiale-MIDEM. Časopis objavlja prispevke domačih in tujih avtorjev, še posebej članov MIDEM, s področja mikroelektronike, elektronskih sestavnih delov in materialov, ki so lahko:

izvirni znanstveni članki, predhodna sporočila, pregledni članki, razprave z znanstvenih in strokovnih posvetovanj in strokovni članki.

Članki bodo recenzirani.

Časopis objavlja tudi novice iz stroke, vesti iz delovnih organizacij, inštitutov in fakultet, obvestila o akcijah društva MIDEM in njegovih članov ter druge relevantne prispevke.

Strokovni prispevki morajo biti pripravljeni na naslednji način

- 1. Naslov dela, imena in priimki avtorjev brez titul.
- 2. Ključne besede in povzetek (največ 250 besed).
- 3. Naslov dela v angleščini.
- 4. Ključne besede v angleščini (Key words) in podaljšani povzetek (Extended Abstract) v angleščini.
- 5. Uvod, glavni del, zaključek, zahvale, dodatki in literatura.
- 6. Imena in priimki avtorjev, titule in naslovi delovnih organizacij, v katerih so zaposleni.

Ostala splošna navodila

1. V članku je potrebno uporabljati SI sistem enot oz. v oklepaju navesti alternativne enote.

2. Risbe je potrebno izdelati s tušem na pavs ali belem papirju. Širina risb naj bo do 7.5 oz. 15 cm. Vsaka risba, tabela ali fotografija naj ima številko in podnapis, ki označuje njeno vsebino. Risb, tabel in fotografij ni potrebno lepiti med tekst, ampak jih je potrebno ločeno priložiti članku. V tekstu je potrebno označiti mesto, kjer jih je potrebno vstaviti.

3. Delo je lahko napisano in bo objavljeno v kateremkoli jugoslovanskem jeziku v latinici in v angleščini.

Uredniški odbor ne bo sprejel strokovnih člankov, ki ne bodo poslani v dveh izvodih.

Avtorji, ki pripravljajo besedilo v urejevalnikih besedil, lahko pošljejo zapis datoteke na disketi (360 ali 1,2) v formatih ASCII, wordstar (3.4, 4.0), wordperfect, word, ker bo besedilo oblikovano v programu Ventura 2.0. Grafične datoteke so lahko v formatu HPL, SLD (AutoCAD), PCX ali IMG/GEM.

Avtorji so v celoti odgovorni za vsebino objavljenega sestavka. Rokopisov ne vračamo.

Rokopise pošljite na naslov

Uredništvo Informacije MIDEM
Elektrotehniška zveza Slovenije
Dunajska 10, 61000 Ljubljana

UPUTE AUTORIMA

Informacije MIDEM je znanstveno-stručno-društvena publikacija Stručnog društva za mikroelektroniku, elektronske sestavne dijelove i materijale - MIDEM. Časopis objavljuje priloge domaćih i stranih autora, naročito članova MIDEM, s područja mikroelektronike, elektronskih sastavnih dijelova in materijala koji mogu biti:

izvorni znanstveni članci, predhodna priopćenja, pregledni članci, izlaganja sa znanstvenih i stručnih skupova i stručni članci.

Članci će biti recenzirani.

Časopis takoder objavljuje novosti iz struke, obavijesti iz radnih organizacija, instituta i fakulteta, obavijesti o akcijama društva MIDEM i njegovih članova i druge relevantne obavijesti.

Stručni članci moraju biti pripremljeni kako slijedi

- 1. Naslov članka, imena i prezimena autora bez titula.
- 2. Ključne riječi i sažetak (najviše 250 riječi).
- 3. Naslov članka na engleskom jeziku.
- 4. Ključne riječi na engleskom jeziku (3Key Words) i produženi sažetak (Extended Abstract) na engleskom jeziku.
- 5. Uvod, glavni dio, zaključni dio, zahvale, dodaci i literatura.
- 6. Imena i prezimena autora, titule i naslovi institucija u kojima su zaposleni.

Ostale opšte upute

1. U prilogu treba upotrebljavati SI sistem jedinica od. u zagradi navesti alternativne jedinice.

2. Crteže treba izraditi tušem na pausu ili bijelom papiru. Širina crteža neka bude do 7.5 odnosno 15 cm. Svaki crtež, tablica ili fotografija treba imati broj i naziv koji označuje njen sadržaj. Crteže, tabele i fotografije nije potrebno lijepiti u tekst, već ih priložiti odvojeno, a u tekstu samo naznačiti mjesto gdje dolaze.

3. Rad može biti pisan i biti će objavljen na bilo kojem od jugoslavenskih jezika u latinici i na engleskom jeziku.

Autori mogu poslati radove na disketama (360 ili 1,2) u formatima tekst procesora ASCII, wordstar (3.4. i 4.0), word, wordperfect pošto će biti tekst dalje obrađen u Venturi 2.0. Grafičke datoteke mogu biti u formatu HPL, SLD (AutoCAD), PCX ili IMG/GEM.

Urednički odbor će odbiti sve radove koji neće biti poslani u dva primjerka.

Za sadržaj članaka autori odgovaraju u potpunosti. Rukopisi se na vraćaju.

Rukopise šaljite na adresu:

Uredništvo Informacije MIDEM
Elektrotehnična zveza Slovenije
Dunajska 10, 61000 Ljubljana
Slovenija

INFORMATION FOR CONTRIBUTORS

Informacije MIDEM is professional-scientific-social publication of Professional Society for Microelectronics, Electronic Components and Materials. In the Journal contributions of domestic and foreign authors, especially members of MIDEM, are published covering field of microelectronics, electronic components and materials. These contributions may be:

original scientific papers, preliminary communications, reviews, conference papers and professional papers.

All manuscripts are subject to reviews.

Scientific news, news from the companies, institutes and universities, reports on actions of MIDEM Society and its members as well as other relevant contributions are also welcome.

Each contribution should include the following specific components:

- 1. Title of the paper and authors' names.
- 2. Key Words and Abstract (not more than 250 words).
- 3. Introduction, main text, conclusion, acknowledgements, appendix and references.
- 4. Authors' names, titles and complete company or institution adress.

General information

1. Authors should use SI units and provide alternative units in parentheses wherever necessary.

2. Illustrations should be in black on white or tracing paper. Their width should be up to 7.5 or 15 cm. Each illustration, table or photograph should be numbered and with legend added. Illustrations, tables and photografphs are not to be placed into the text but added separatelly. Hower, their position in the text should be clearly marked.

3. Contributions may be written and will be published in any Yugoslav language and in english.

Authors may send their files on formatted diskettes (360 or 1,2) in ASCII, wordstar (3.4 or 4.0), word, wordperfect as text will be formated in Ventura 2.0. Graphics may be in HPL, SLD (AutoCAD), PVX or IMG/GEM formats.

Papers will not be accepted unless two copies are received.

Authors are fully responsible for the content of the paper. Manuscripts are not returned.

Contributions are to be sent to the address:

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Dunajska 10, 61000 Ljubljana,
Slovenia

TERMINOLOŠKI STANDARDI

2.6 Karakteristike

1	2	3	4
2.6.1	• Granična frekvencija • Granična frekvencija • Гранична фреквенција • Mejna frekvenca	147–0/0–6.1 • Cut-off frequency • Fréquence de coupure	Frekvenca, pri kateri se absolutna vrednost parametra zmanjša za $1/\sqrt{2}$ njegove nizkofrekvenčne vrednosti. Opomba: Pri transistorju se mejna frekvenca navadno uporabi za tokovno ojačenje malih signalov za vezavo s skupno bazo ali s skupnim emitorjem.

3 Seznami v jezikih jugoslovanskih narodov

3.1 Abecedni seznam izrazov v srbohrvatskem jeziku

B

Bipolarni tranzistor 2.2.14

Č

Čelija, fotonaponska 2.2.20
Čelija, fotoprovodna 2.2.19

D

Difundovani spoj 2.1.9
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Dioda, poluprovodnička 2.2.2
Dioda, protivsmerna 2.2.10
Dioda referentnog napona 2.2.3
Dioda, signalna 2.2.9
Dioda s lavinskim probojem, ispravljačka 2.2.11
Dioda s prinuđenim lavinskim probojem, ispravljačka 2.2.12
Dioda, tunelska 2.2.7
Dioda za stabilizaciju napona 2.2.4
Direktni smer (PN spoja) 2.3.3

E

Efekat, fotoelektrični 2.1.25
Efekat, fotonaponski 2.1.26
Efekat, Holov 2.1.23
Efekat, tunelski 2.1.21
Ekvivalentna temperatura, unutrašnja 2.5.4
Ekvivalentna toplotna kapacitivnost 2.4.7
Ekvivalentna toplotna otpornost 2.4.8
Ekvivalentna toplotna šema 2.4.6
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F

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Foto-dioda 2.2.8
Fotoelektrični efekat 2.1.25
Fotonaponska ćelija 2.2.20
Fotonaponski efekat 2.1.26
Fotoprovodna ćelija 2.2.19
Foto-tranzistor 2.2.17
Frekvencija, granična 2.6.1

G

Granična frekvencija 2.6.1
Granična snaga disipacije, toplotni faktor smanjenja 2.5.3

H

Holov efekat 2.1.23
Holov koeficijent 2.1.24

I

Impedansa za impulsnu struju, prelazna toplotna 2.4.10
Impedansa za konstantnu struju, prelazna toplotna 2.4.9
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Inverzni smer (PN spoja) 2.3.4
Ispravljačka dioda, poluprovodnička 2.2.5
Ispravljačka dioda s lavinskim probojem 2.2.11
Ispravljačka dioda s prinuđenim lavinskim probojem 2.2.12
Ispravljački blok (slog), poluprovodnički 2.2.6
Izvlačeni spoj 2.1.10

K

Kapacitivnost, ekvivalentna toplotna 2.4.7
Kapacitivnost (poluprovodničke komponente), toplotna 2.4.5
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Komponenta, poluprovodnička 2.2.1
Kućište, temperatura 2.5.1

L

Lavinski napon 2.1.17
Lavinski proboj (poluprovodničkog PN spoja) 2.1.16
Lebdeći napon 2.4.2
Legirani spoj 2.1.8

M

Manjinski nosioci (u nekoj oblasti poluprovodnika) 2.1.13

N

Napon, inverzni 2.4.1
Napon, lavinski 2.1.17
Napon, lebdeći 2.4.2
Napon, probojni 2.4.3
Napon, Zenerov 2.1.20
Nosilac 2.1.11
Nosilac naelektrisanja 2.1.11
Nosioci (u nekoj oblasti poluprovodnika), manjinski 2.1.13
Nosioci (u nekoj oblasti poluprovodnika), većinski 2.1.12

O

Odvodnik prenapona, selenski 2.2.21
Osiromašeni sloj 2.1.14
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Otpornost (poluprovodničke komponente), toplotna 2.4.4

P

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Poluprovodnik I-tipa (sopstveni) 2.1.5
Poluprovodnik N-tipa 2.1.3
Poluprovodnik, primesni 2.1.2
Poluprovodnik P-tipa 2.1.4
Poluprovodnička dioda 2.2.2
Poluprovodnička ispravljačka dioda 2.2.5
Poluprovodnička komponenta 2.2.1
Poluprovodnički ispravljački blok (slog) 2.2.6
Prelaz (spoj) 2.1.6
Prelazna toplotna impedansa za impulsnu struju 2.4.10
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Priključak (poluprovodničke komponente) 2.3.1
Primesni poluprovodnik 2.1.2
Proboj (inverzno polarisanog PN spoja) 2.1.15
Proboj (poluprovodničkog PN spoja), lavinski 2.1.16
Proboj (poluprovodničkog PN spoja), termički 2.1.18
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S

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Skladištenje, temperatura 2.5.2
Slog (blok), poluprovodnički ispravljački 2.2.6
Sloj, osiromašeni 2.1.14
Smer (PN spoja), direktni 2.3.3
Smer (PN spoja), inverzni 2.3.4
Spoj, difundovani 2.1.9
Spoj, izvlačeni 2.1.10
Spoj, legirani 2.1.8
Spoj, PN 2.1.7
Spoj (prelaz) 2.1.6

Š

Šema, ekvivalentna toplotna 2.4.6

T

Temperatura kućišta 2.5.1
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Temperatura, unutrašnja ekvivalentna 2.5.4
Temperatura, virtuelna 2.5.4
Termički proboj (poluprovodničkog PN spoja) 2.1.18
Tiristor 2.2.18
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Toplotna impedansa za konstantnu struju 2.4.9
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Toplotna kapacitivnost, (poluprovodničke komponente) 2.4.5
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Toplotna otpornost (poluprovodničke komponente) 2.4.4
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U

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Unutrašnja ekvivalentna temperatura (virtuelna temperatura) 2.5.4

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V

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Z

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3.2 Abecedni seznam izrazov v hrvatskem knjižnem jeziku

B

Bipolarni tranzistor 2.2.14
Blok, poluvodički ispravljački 2.2.6

C

Ćelija, fotonaponska 2.2.20
Ćelija, fotovodljiva 2.2.19

D

Difundirani spoj 2.1.9
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Dioda, poluvodička 2.2.2
Dioda, protusmjerna 2.2.10
Dioda referentnog napona 2.2.3
Dioda, signalna 2.2.9
Dioda s lavinskim probojem, ispravljačka 2.2.11
Dioda s prisilnim lavinskim probojem, ispravljačka 2.2.12
Dioda, tunelska 2.2.7
Dioda za stabilizaciju napona 2.2.3

E

Efekt, fotoelektrični 2.1.25
Efekt, fotonaponski 2.1.26
Efekt, Hallov 2.1.23
Efekt, tunelski 2.1.21
Ekvivalentna temperatura, unutrašnja 2.5.4
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F

Faktor smanjenja granične disipacije, toplinske 2.5.3
Foto–dioda 2.2.8
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Fotonaponska ćelija 2.2.20
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Fotovodljiva ćelija 2.2.19
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Frekvencija, granična 2.6.1

G

Granična frekvencija 2.6.1

H

Hallov efekt 2.1.23
Hallov koeficijent 2.1.24

I

Impedancija za impulsnu struju, prijelazna toplinska 2.4.10
Impedancija, prijelazna toplinska 2.4.9
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Ispravljačka dioda, poluvodička 2.2.5
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Ispravljačka dioda s prisilnim lavinskim probojem 2.2.12
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Izvlačeni spoj 2.1.1

K

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Kapacitivnost (poluvodičke komponente), toplinska 2.4.5
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L

Lavinski napon 2.1.17
Lavinski proboj (poluvodičkog PN--spoja) 2.1.16
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Legirani spoj 2.1.8

M

Manjinski nosioci (u nekom području poluvodiča) 2.1.13

N

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Nadomjesni toplinski otpor 2.4.8
Nadomjesna toplinska shema 2.4.6
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Napon, lavinski 2.1.17
Napon, plivajući 2.4.2
Napon, probojni 2.4.3
Napon, Zenerov 2.1.20
Nosilac 2.1.11
Nosilac naboja 2.1.11
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O

Odvodnik prenapona, selenski 2.2.21
Osiromašeni sloj 2.1.14
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P

PN–spoj 2.1.7
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Poluvodič tipa I (intrinsični) 2.1.5
Poluvodič tipa N 2.1.3
Poluvodič, primjesni 2.1.2
Poluvodič tipa P 2.1.4
Poluvodička dioda 2.2.2
Poluvodička ispravljačka dioda 2.2.5
Poluvodička komponenta 2.2.1
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Propusni (direktni) smjer (PN–spoja) 2.3.3
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S

Selenski odvodnik prenapona 2.2.21
Signalna dioda 2.2.9
Sloj, osiromašeni 2.1.14
Smjer (PN–spoja), propusni, (direktni) 2.3.3
Smjer PN--spoja, zaporni (inverzni) 2.3.4
Spoj, difundirani 2.1.9
Spoj, izvlačeni 2.1.10
Spoj, legirani 2.1.8
Spoj Pn 2.1.7
Spoj, (prijelaz) 2.1.6

Š

Shema nadomjesna toplinska 2.4.6

T

Temperatura kućišta 2.5.1
Temperatura uskladištenja 2.5.2
Temperatura, unutrašnja nadomjesna 2.5.4
Temperatura, virtualna 2.5.4
Toplinski proboj (poluvodičkog PN–spoja) 2.1.18
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Toplinska kapacitivnost, nadomjesna 2.4.7
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Toplinski otpor nadomjesni 2.4.8
Toplinski otpor (poluvodičke komponente) 2.4.4
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Tranzistor 2.2.13
Tranzistor, bipolarni 2.2.14