

# GAIN CONTROL LOOP FOR A 2.4 GHz VARIABLE GAIN LOW NOISE AMPLIFIER (VGLNA)

Lini Lee, Roslina Mohd Sidek, Sudhanshu Shekhar Jamuar and \*Sabira Khatun

Department of Electrical and Electronic Engineering,

\*Department of Computer System and Communication Engineering, Faculty of Engineering, University Putra Malaysia (UPM), Selangor, Malaysia.

**Key words:** continuous gain variation, high gain, linearity, low NF, radio frequency, variable-gain LNA

**Abstract:** The most critical point of a integrated receiver is the radio frequency (RF) input and the first stage of the receiver is a low noise amplifier (LNA). Thus, LNAs with low power consumption and excellent properties in terms of gain, noise and linearity are highly in demand. Moreover, a variable-gain LNA which can prevent saturation in the receiver when the input signal becomes relatively large has the advantage of no additional attenuator or variable gain amplifier is required. Thus, power consumption, chip size and cost can be minimized at the same time. Hence, this work proposes a two-stage variable gain LNA with large and continuous gain variation. By introducing a simple gain-control loop at the second stage of a cascade LNA, a continuous gain tuning range of approximately 14 dB is achieved. The VGLNA is designed using 0.18  $\mu\text{m}$  CMOS technology and targeted for applications at 2.4 GHz. The maximum gain and NF of this VGLNA are 23 dB and 1.12 dB respectively. The DC power consumption is reported to be 12.4 mW from a 1 V power supply. Comparison is made with available circuits to show that this VGLNA has the advantage of a continuous tuning range and low NF, and this is accomplished without degrading its performance.

## Kontrolna zanka ojačanja za 2.4GHz nizkošumni ojačevalnik s spremenljivim ojačanjem (VGLNA)

**Ključne besede:** spreminjanje ojačanja, visoko ojačanje, linearnost, nizko šumno število, radijske frekvence, ojačevalniki s spremenljivim ojačanjem

**Izveček:** Najbolj občutljiva točka integriranega sprejemnika je RF vhod z nizkošumnim ojačevalnikom (LNA). Zatorej je povpraševanje po LNA ojačevalnikih z nizko porabo ter drugimi odličnimi lastnostmi, kot so ojačanje, nizek šum in linearnost, veliko. Prednost imajo predvsem LNA ojačevalniki s spremenljivim ojačanjem, ki ne grejo v zasičenje, ko zunanji signal postane relativno močan. Zatorej lahko porabo, velikost čipa in ceno hkrati zmanjšamo. V prispevku opišemo dvostopenjski LNA ojačevalnik z velikim in nepretrganim ojačanjem. Z uvedbo kontrolne zanke ojačanja v drugo stopnjo stopničastega LNA dosežemo nastavljivo nepretrgano ojačanje v območju 14dB. Tak VGLNA je načrtan v 0.18 $\mu\text{m}$  CMOS tehnologiji s ciljno uporabo na frekvenci 2.4GHz. Največje ojačenje in šumno število sta 23dB in 1.12dB. DC poraba je 12.4mW pri napajalni napetosti 1V. Primerjava s podobnimi vezji pokaže prednosti tako načrtanega VGLNA.

### 1. Introduction

The ceaseless advance of Complementary Metal-Oxide Semiconductor (CMOS) technology such as the shrink of the gate length and the improvement of the cutoff frequency makes CMOS more and more attractive for many radio frequency (RF) circuits in the several GHz range /1-3/. There is no doubt that a complicated RF system can be realized in CMOS and some chips have been fabricated and reported /4-7/.

The first block of wireless receiver following the antenna is a low noise amplifier (LNA) which plays a significant role as its noise figure (NF) sets a lower bound on the NF of the entire system. Moreover it should be able to accommodate large signals without distortion and must match the input impedance. A good input impedance match is more critical if a pre-select filter precedes the LNA since the transfer characteristics of many filters are sensitive to the quality of the termination. The additional requirement is the low

power consumption which plays an important role in the applications of portable communications systems /8/.

It is not a simple task to design a LNA with high gain and low NF by considering both linearity and input impedance match, with low power consumption. Inductive degeneration is adopted as the LNA architecture popularly because it does not introduce extra noise source and it uses a source degenerative inductor to realize input impedance match. The theoretical analysis and calculation of NF of this topology has been done using an extended MOS noise model /8/. If the gain of LNA block is too low, noise level of this block might dominates the overall NF and if it is too high, the input signal would create nonlinearity. Inversely, if the gain is too low, the mixer noise dominates the overall NF and if it is too high, the input signal to the mixer creates large intermodulation products. For these reasons, the design of the LNA with a variable gain stage or termed as variable gain low noise amplifier (VGLNA) is adopted not only to achieve high gain and low noise but also high linearity. The function of the controllable gain is to prevent sat-

uration in the receiver when the input signal becomes relatively large.

Conventional design techniques for VGLNA can be seen in using bypass switch [9], which achieves gain variation by on-off control of the bypass switch. However, continuous gain control is difficult with this method. Thus unnecessary power would be consumed at low gain mode. Other gain variation methods reported is the current variation according to target gain [10-12]. These methods reduce its power consumption at low gain mode by controlling its biased current of a LNA. However, this method suffers from small gain variation or discontinuous gain control.

This paper focuses on the CMOS VGLNA designed for 2.4 GHz with a gain-control loop. The VGLNA can operate from 2.1 GHz to 2.5 GHz and can be used for Wideband Code Division Multiple Access (WCDMA) and IEEE 802.11b/g Wireless Local Area Network (WLAN) applications. By introducing a simple gain control loop composed of a gain control transistor and a capacitor, a continuous gain tuning range of approximately 14 dB is achieved.

## 2. Variable gain block of a LNA

Fig. 1 shows the fundamental architecture of proposed gain control LNA. The gain control loop is composed of a gain control transistor ( $M_{gc}$ ) and a capacitor  $C_f$ . If the  $M_{gc}$  is turned off, the gain control loop is like an open circuit and the VGLNA operates with minimum gain. On the other hand, if  $M_{gc}$  is turned on with sufficiently high voltage (like  $V_{DD}$ ), then  $M_{gc}$  operates as a bypass switch and it operates at maximum gain. Therefore, a large gain variation range similar to that of the bypass switch method is achieved.

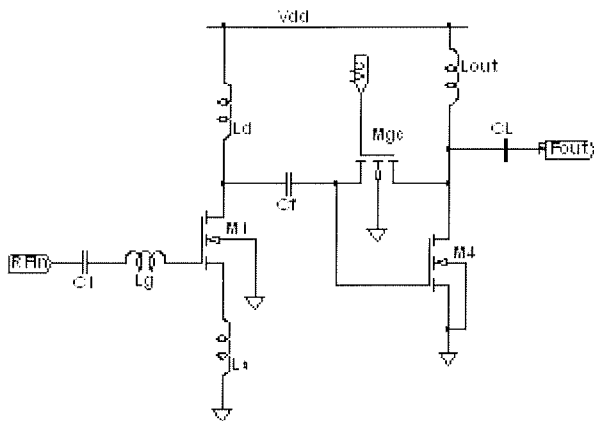


Fig. 1. Fundamental architecture of proposed variable gain LNA.

The control voltage of the  $M_{gc}$  is between threshold voltage and  $V_{DD}$  with  $M_{gc}$  operating as a variable resistor. This resistance value is equal to the channel resistance  $R_{gc}$  which can be expressed as

$$R_{gc} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_c - V_{gs4} - V_{th-gc})} \quad (1)$$

where  $V_c$  and  $V_{th-gc}$  are the control or gate voltage and threshold voltage of  $M_{gc}$  respectively.  $V_{gs4}$  is the gate-to-source voltage of  $M_4$ . From (1),  $R_{gc}$  varies inversely proportional to the variation of  $V_c$ . As  $V_c$  increases, the impedance of the gain control loop becomes smaller, thus the inter-stage matching changes. Therefore, the gain of the second stage increases continuously as  $V_c$  increases. This is verified in the simulation results in Section 4.

The capacitor  $C_f$  is added to support the operation of  $M_{gc}$  as a variable resistor. It operates as a DC blocking capacitor, making sure that the  $V_{DS}$  of  $M_{gc}$  stays small. With the  $V_{DS}$  stays small, the  $M_{gc}$  operates as a variable resistor.

## 3. Design of a Variable Gain LNA

Based on the variable gain block described in Section 2, a 2.4 GHz VGLNA is designed. The VGLNA is composed of a cascode stage and variable gain block. Fig. 2 shows the cascode stage of the designed VGLNA. The cascode stage is made of transistors  $M_1$  and  $M_2$ . On-chip inductors of  $L_g$  and  $L_s$  are used respectively for matching the input stage of the cascode stage and as a degeneration inductor to suppress the NF of the VGLNA.

Fig. 3 shows the schematic of the variable gain block in a VGLNA. The gain control characteristics of designed variable gain block depends on the size of  $M_{gc}$ . Large size of  $M_{gc}$  gives large gain variation. However, too large of gain variation would changes too rapidly making continuous control difficult. Moreover, large size of  $M_{gc}$  increases parasitic capacitance and may reduce the maximum gain. On the other hand, if the size of the  $M_{gc}$  is very small, the gain variation would become small. This result might not satisfy the linearity requirement of the following stage in a receiver such as a mixer. Therefore, the size of the  $M_{gc}$  must be selected within the proper gain variation range.

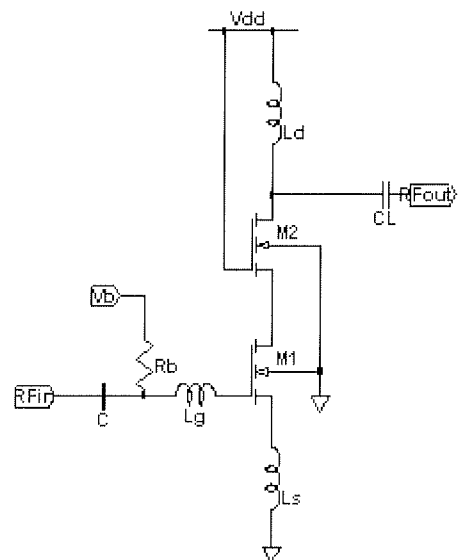


Fig. 2. The cascode stage of the designed VGLNA.

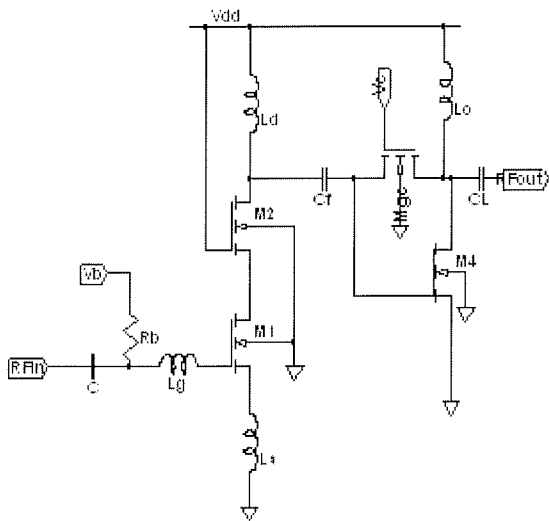


Fig. 3. The variable gain block in the proposed VGLNA.

#### 4. Simulation results

The VGLNA has been designed for WCDMA and 802.11b/g WLAN applications in 0.18  $\mu\text{m}$  CMOS technology. The design has been simulated using Agilent's Advanced Design System (ADS).

Fig. 4 and 5 show the  $S_{21}$ ,  $S_{11}$  and NF of the designed VGLNA at high gain mode. With the power consumption of 12.4 mW from a supply voltage of 1.0 V, the VGLNA achieves power gain of 23.29 dB at 2.4 GHz. The gain is maximized at 2.4 GHz because input matching is optimum at 2.4 GHz. The input return loss is -20 dB. The NF of the designed VGLNA is 1.116 dB at 2.4 GHz for the maximum gain mode.

As for the minimum gain mode,  $S_{21}$  and  $S_{11}$  are reported to be 9.54 dB and -21 dB as shown in Fig. 6. Fig. 7 shows the NF of the VGLNA at low gain mode which is slightly higher with 1.123 dB. This result is acceptable in comparison with other VGLNAs [13-15]. The designed VGLNA can achieve low NF because the gain of cascode stage mitigates the influence of NF at the gain control block.

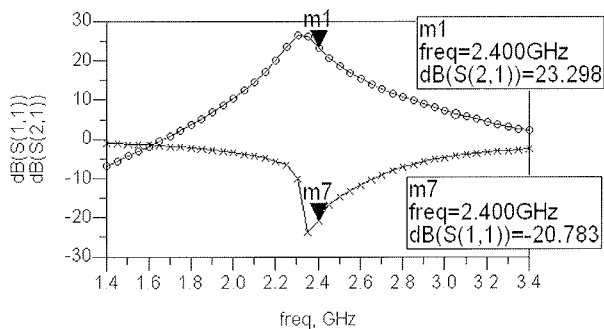


Fig. 4.  $S_{21}$  and  $S_{11}$  of the designed VGLNA at high gain mode.

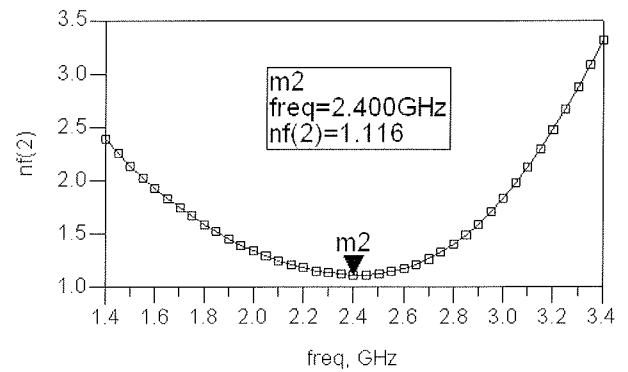


Fig. 5. NF of the proposed VGLNA at high gain mode.

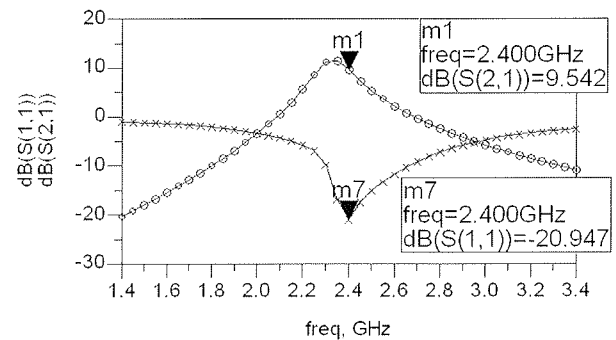


Fig. 6.  $S_{21}$  and  $S_{11}$  of the designed VGLNA at low gain mode.

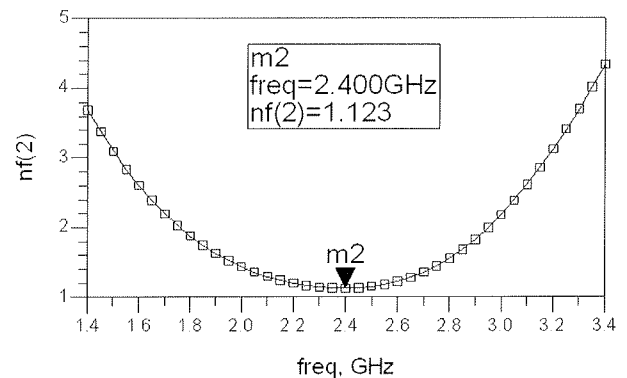


Fig. 7. NF of the proposed VGLNA at low gain mode.

As shown in Fig. 8, the VGLNA achieves continuous gain tuning range of 13.75dB from 23.29 dB to 9.54 dB at 2.4 GHz. The gain variation is similar to that of the LNA with the bypass switch method [9]. In addition, the power consumption of the following stages in a receiver such as mixer and automatic gain control (AGC) can be further reduced by achieving the continuous gain control. The NF varies from 1.116 dB to 1.123 dB at minimum gain mode. NF varies very little in comparison with the gain changes because the increase of NF is minimized by the gain of the first stage.

As for the linearity, the third order input intercept point (IIP3) is simulated at low gain mode and it is -2.18 dBm at 2.4 GHz. Thus, the LNA can receive maximum input power of 802.11b WLAN without much distortion.

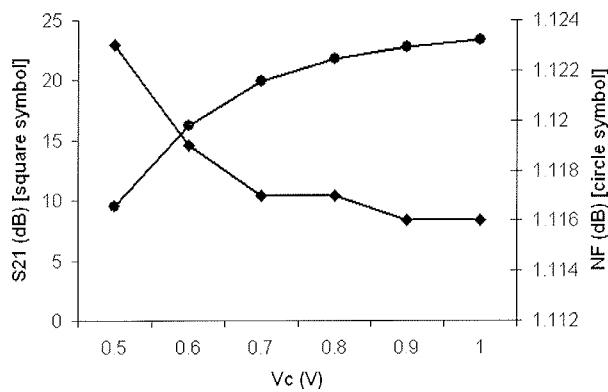


Fig. 8. Gain and NF variation of the VGLNA.

Table 1 shows the comparison of performances for the designed VGLNA with other variable gain LNAs. Though gain variation range of proposed VGLNA is smaller than other VGLNAs /9-11/ but it has a much better NF and continuous gain control is achieved. Therefore, overall performance of the proposed VGLNA is better in terms of continuous tuning range and NF.

Table 1 Comparison of Variable Gain LNA Performances

	This work (CMOS)	[9]	[10]	[11]	[12]	[13]
Technology (um)	0.18	0.25	-	0.25	0.18	0.18
Operating frequency (GHz)	2.4	2.4	0.9	5.6	5.7	5.2
Gain (dB)	23.29	14.7	26	19.5	16.5	20
Gain variation (dB)	13.75	29	29	19.5	8	20
Continuous gain control	Yes	No	No	No	Yes	Yes
Minimum NF (dB)	1.12	2.88	2.1	3.1	3.5	3.5
Biased current (mA)	12.4	11.7	15	10	3.2	17

## 5. Conclusion

In this paper, a VGLNA for WCDMA and 802.11b/g is presented. The designed VGLNA composed of a cascode stage and a variable gain block. The VGLNA achieves low NF of 1.12 dB, gain of 23 dB and power consumption of 12.4 mW from 1.0 V power supply. By adding a simple gain control loop composed of a transistor  $M_{gc}$  and a capacitor, the VGLNA achieves a gain tuning range of 13.75 dB with continuous gain control. This is accomplished with a low NF which is reported to be only 1.12 dB. This VGLNA is able to mitigate the dynamic range and linearity requirement of the stages that followed such as mixer and AGC.

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## References

- /1/ T. H. Lee, *The Design of CMOS Radio Frequency Integrated Circuit*, Cambridge University Press, Cambridge (1998).
- /2/ L. E. Larson, "Integrated circuit technology options for RFIC's - present status and future directions," *IEEE Journal of Solid-State Circuits*, vol. 33 no. 3, March 1998, pp. 387-399.
- /3/ E. Abou-Allam, T. Manku, M. Ting and M. S. Obrecht, "Impact of Technology scaling on CMOS RF devices and circuits," *IEEE Custom Integrated Circuits Conference (CICC 2000)*, 2000, pp. 361-364.
- /4/ T. Kadoyama, N. Suzuki, N. Sasho, H. Iizuka, I. Nagase, H. Usukubo and M. Katakura, "A complete single-chip GPS receiver with 1.6-V 24-mW Radio in 0.18-um CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 4, April 2004, pp. 562-568.
- /5/ G. Gramegna, M. Franciotta, V. Mandara, N. G. Bellantone, M. Vaiana, M. Paparo, M. Losi, S. Das and P. Mattos, "23mm<sup>2</sup> single-chip 0.18um CMOS GPS receiver with 28mW-4.1 mm<sup>2</sup> radio and CPU/DSP/Ram/ROM," *IEEE Custom Integrated Circuits Conference (CICC 2004)*, 2004, pp. 81-84.
- /6/ R. Ahola, et. al, "A single-chip CMOS transceiver for 802.11a/b/g wireless LANs," *IEEE Journals of Solid-State Circuits*, vol. 39, no. 12, Dec. 2004, pp. 2250-2258.
- /7/ L. Leung and et. al, "A 1V Low-power Single-Chip CMOS WLAN IEEE 802.11a Transceiver," *Proc. Solid-State Circuits Conf. 2006 (ESSCIRC 2006)*, Sept. 2006, pp. 283-286.
- /8/ D. K. Shaeffer and T. H. Lee, "A 1.5 V, 1.5 GHz CMOS low noise amplifier," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 2, 1999, pp. 745-759.
- /9/ R. Point, M. Mendes and W. Foley, "A differential 2.4 GHz switched-gain CMOS LNA for 802.11b and Bluetooth," *Radio and Wireless Conferences 2002 (RAWCON)*, 2002, pp. 221-224.
- /10/ S. Pennisi, S. Scaccianose and G. Palmisano, "A new design approach for variable-gain low noise amplifier," *Radio Frequency Integrated Circuits (RFIC) Symposium 2000*, June 2000, pp. 11-13.
- /11/ M. Rajashekharaiyah, P. Upadhyaya and Heo Deukhyoun, "A compact 5.6 GHz low noise amplifier with new on-chip gain controllable active balun," *IEEE Workshop on Microelectronics and Electron Devices 2004*, 2004, pp. 131-132.
- /12/ Y. S. Wang and L. -H. Lu, "5.7 GHz low-power variable-gain LNA in 0.18 um CMOS," *Electronics Letters*, vol. 41, no. 2, Jan. 2005, pp. 66-68.
- /13/ M. -D. Tsai, R.-C. Liu, C. -S. Lin and H. Wang, "A low-voltage fully-integrated 4.5-6-GHz CMOS variable gain low noise amplifier," *33<sup>rd</sup> European Microwave Conference 2003*, vol. 1, Oct. 2003, pp. 13-16.

Lini Lee, Roslina Mohd Sidek, Sudhanshu Shekhar Jamuar and \*Sabira Khatun  
 Department of Electrical and Electronic Engineering,  
 \*Department of Computer System and  
 Communication Engineering, Faculty of Engineering,  
 University Putra Malaysia (UPM),  
 43400 UPM Serdang, Selangor, Malaysia.  
 Corresponding e-mail: linilee@gmail.com