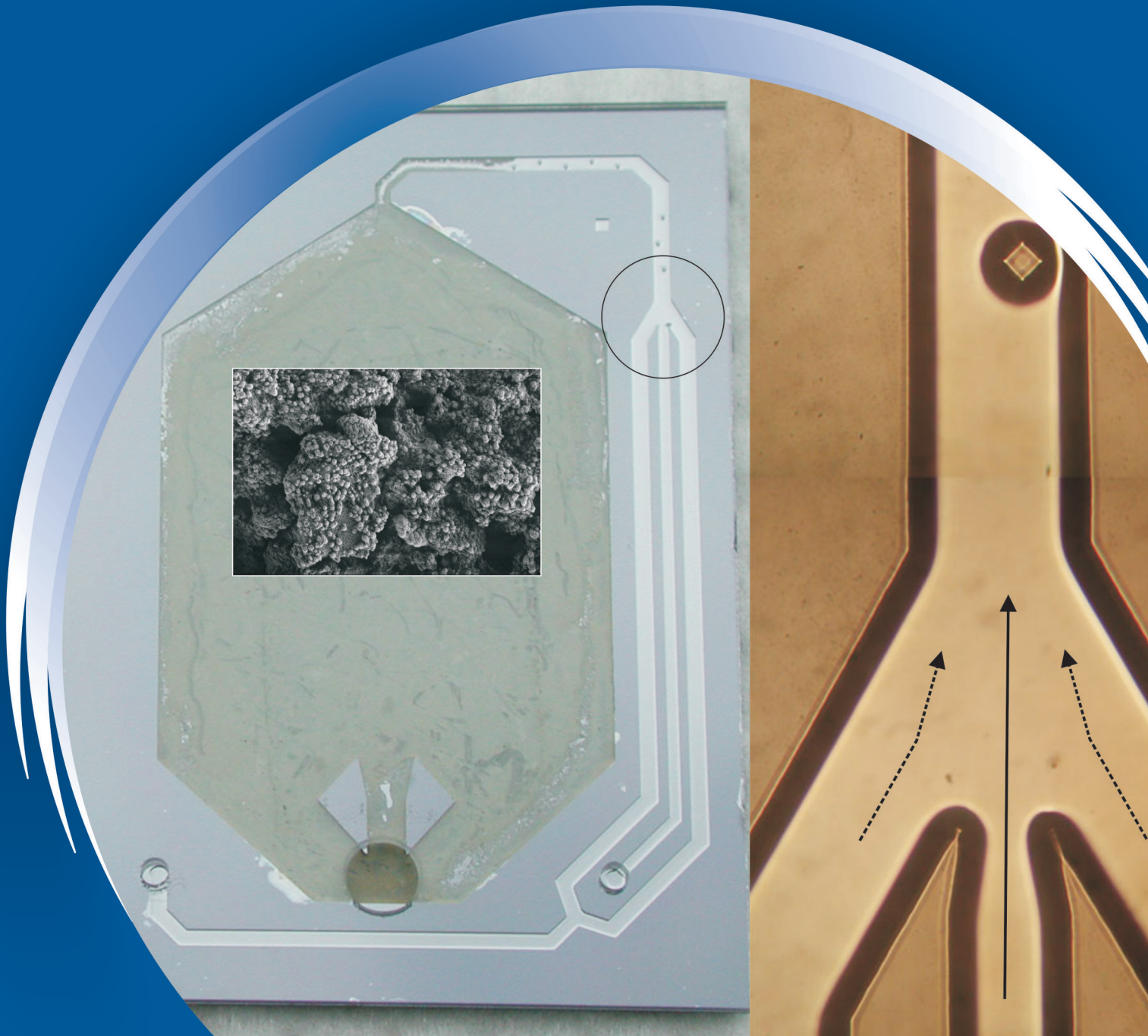


ISSN 0352-9045

Informacije MIDEM

*Journal of Microelectronics,
Electronic Components and Materials*
Vol. 42, No. 3 (2012), September 2012

*Revija za mikroelektroniko,
elektronske sestavne dele in materiale*
letnik 42, številka 3 (2012), September 2012



Informacije MIDE M 3-2012

Journal of Microelectronics, Electronic Components and Materials

VOLUME 42, NO. 3(143), LJUBLJANA, SEPTEMBER 2012 | LETNIK 42, NO. 3(143), LJUBLJANA, SEPTEMBER 2012

Published quarterly (March, June, September, December) by Society for Microelectronics, Electronic Components and Materials - MIDE M.
Copyright © 2012. All rights reserved. | Revija izhaja trimesečno (marec, junij, september, december). Izdaja Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale – Društvo MIDE M. Copyright © 2012. Vse pravice pridržane.

Editor in Chief | Glavni in odgovorni urednik

Marko Topič, University of Ljubljana (UL), Faculty of Electrical Engineering, Slovenia

Editor of Electronic Edition | Urednik elektronske izdaje

Kristijan Brecl, UL, Faculty of Electrical Engineering, Slovenia

Associate Editors | Odgovorni področni uredniki

Vanja Ambrožič, UL, Faculty of Electrical Engineering, Slovenia

Slavko Amon, UL, Faculty of Electrical Engineering, Slovenia

Danjela Kuščer Hrovatin, Jožef Stefan Institute, Slovenia

Matjaž Vidmar, UL, Faculty of Electrical Engineering, Slovenia

Andrej Žemva, UL, Faculty of Electrical Engineering, Slovenia

Editorial Board | Uredniški odbor

Mohamed Akil, ESIEE PARIS, France

Giuseppe Buja, University of Padova, Italy

Gian-Franco Dalla Betta, University of Trento, Italy

Martyn Fice, University College London, United Kingdom

Ciprian Iliescu, Institute of Bioengineering and Nanotechnology, A*STAR, Singapore

Malgorzata Jakubowska, Warsaw University of Technology, Poland

Marc Lethiecq, University of Tours, France

Teresa Orłowska-Kowalska, Wrocław University of Technology, Poland

Luca Palmieri, University of Padova, Italy

International Advisory Board | Časopisni svet

Janez Trontelj, UL, Faculty of Electrical Engineering, Slovenia - Chairman

Cor Claeys, IMEC, Leuven, Belgium

Denis Đonlagić, University of Maribor, Faculty of Elec. Eng. and Computer Science, Slovenia

Zvonko Fazarinc, CIS, Stanford University, Stanford, USA

Leszek J. Golonka, Technical University Wrocław, Wrocław, Poland

Jean-Marie Haussonne, EIC-LUSAC, Octeville, France

Marija Kosec, Jožef Stefan Institute, Slovenia

Miran Mozetič, Jožef Stefan Institute, Slovenia

Stane Pejovnik, UL, Faculty of Chemistry and Chemical Technology, Slovenia

Giorgio Pignatelli, University of Perugia, Italy

Giovanni Soncini, University of Trento, Trento, Italy

Iztok Šorli, MIKROIKS d.o.o., Ljubljana, Slovenia

Headquarters | Naslov uredništva

Uredništvo Informacije MIDE M

MIDE M pri MIKROIKS

Stegne 11, 1521 Ljubljana, Slovenia

T. +386 (0)1 513 37 68

F. + 386 (0)1 513 37 71

E. info@midem-drustvo.si

www.midem-drustvo.si

Annual subscription rate is 100 EUR, separate issue is 25 EUR. MIDE M members and Society sponsors receive current issues for free. Scientific Council for Technical Sciences of Slovenian Research Agency has recognized Informacije MIDE M as scientific Journal for micro-electronics, electronic components and materials. Publishing of the Journal is cofinanced by Slovenian Book Agency and by Society sponsors. Scientific and professional papers published in the journal are indexed and abstracted in COBISS and INSPEC databases. The Journal is indexed by ISI® for Sci Search®, Research Alert® and Material Science Citation Index™. |

Letna naročnina je 100 EUR, cena posamezne številke pa 25 EUR. Člani in sponzorji MIDE M prejema posamezne številke brezplačno. Znanstveni svet za tehnične vede je podal pozitivno mnenje o reviji kot znanstveno-strokovni reviji za mikroelektroniko, elektronske sestavne dele in materiale. Izdajo revije sofinancirajo JAKRS in sponzorji društva. Znanstveno-strokovne prispevke objavljene v Informacijah MIDE M zajemamo v podatkovne baze COBISS in INSPEC. Prispevke iz revije zajema ISI® v naslednje svoje produkte: Sci Search®, Research Alert® in Materials Science Citation Index™.

Po mnenju Ministrstva za informiranje št.23/300-92 se šteje glasilo Informacije MIDE M med proizvode informativnega značaja.

Content | Vsebina

<i>Scientific original papers</i>		<i>Izvirni članki</i>
Editorial	136	Uvodnik
N. Janković, V. Radonić, V. Crnojević-Bengin: Ultra-Compact Dual-Band 3-D Hilbert Resonator in LTCC Technology	137	N. Janković, V. Radonić, V. Crnojević-Bengin: Ultra kompakten dvopasovni resonator v LTCC tehnologiji
U. Legat: On-Line Testing and Recovery of Systems on SRAM-Based FPGA	144	U. Legat: Sprotno testiranje in popravljanje sistemov osno- vanih na vezjih FPGA
I. Fajfar, T. Tuma, J. Puhan, J. Olenšek, Á. Búrmen: Towards Smaller Populations in Differential Evolution	152	I. Fajfar, T. Tuma, J. Puhan, J. Olenšek, Á. Búrmen: K majšim populacijam v diferencialni evoluciji
D. Resnik, S. Hočevar, M. Možek, I. Stegel, S. Amon, D. Vrtačnik: Microfabrication and Characterization of Micro- combustor on (100) Silicon /glass Platform	164	D. Resnik, S. Hočevar, M. Možek, I. Stegel, S. Amon, D. Vrtačnik: Karakterizacija mikrogorilnika izdelanega na Si (100)/Pyrex steklo podlagi
K. Górecki, J. Zarębski: The Influence of Diodes and Transistors Made of Silicon and Silicon Carbide on the Nonisothermal Characteristics of Boost Converters	176	K. Górecki, J. Zarębski: Vpliv diod in tranzistorjev iz silicija in silicijevega karbida na neizotermične karakteristike stikalnega pretvornika navzgor
L. Nagy, J. Radic, A. Djugova, M. Videnovic-Misic: Ultra Low-Power Low-Complexity Tunable 3-10 GHz IR-UWB Pulse Generator	185	L. Nagy, J. Radic, A. Djugova, M. Videnovic-Misic: Enostaven in spremenljiv 3-10 GHz IR-UWB pulzni generator nizke moč
O. Diallo, E. L. Clezio, M. Lethiecq, G. Feuillard: Electrical Excitation and Mechanical Vibration of A Piezoelectric Cube	192	O. Diallo, E. L. Clezio, M. Lethiecq, G. Feuillard: Električno vzbujanje in mehanske vibracije piezoelektrične kocke
A. Vasić, M. Vujisić, K. Stanković, P. Osmokrović: Aging of Overvoltage Protection Elements Caused by Past Activations	197	A. Vasić, M. Vujisić, K. Stanković, P. Osmokrović: Staranje elementov za prenapostno zaščito zaradi premostitev
Front page : Si-Pyrex based methanol-air microcombustor. (D. Resnik et. al)		Naslovnica: Mikro gorilnik metanol-zrak izdelan na (100) Si- Pyrex osnovi. (D. Resnik et. al)

Editorial | Uvodnik

Dear Reader,

This is the third issue of our renewed journal. With the first issue 2012 we have completed the renewal of the journal design. This (3rd) issue finishes the renewal of Editorial Board (EB) adding an additional EB member. We have internationalized the EB with distinguished researchers across Europe to cover five areas of research and development:

- Technologies and Materials (Associate Editor: Asst. Prof. Dr. Danjela Kuščer Hrovatin)
- Sensors and Actuators (Associate Editor: Prof. Dr. Slavko Amon)
- Electronics (Associate Editor: Prof. Dr. Andrej Žemva)
- Power Engineering (Associate Editor: Prof. Dr. Vanja Ambrožič)
- Communications (Associate Editor: Prof. Dr. Matjaž Vidmar)

related to Microelectronics, Electronic Devices and Materials. We succeeded in very short time to ramp up the whole wheels of journal publishing that is now already in full swing. The renewed Editorial Board counts 16 members (above are named five Associate Editors) has agreed to increase high quality standards for all types of papers being published in our journal (order of appearance in each quarterly issue):

- review scientific paper (pregledni znanstveni članek)
- original scientific paper (izvirni znanstveni članek)
- professional paper (strokovni članek)

Since we publish papers only quarterly we see no purpose to publish letter papers or short communication papers. All submitted manuscripts undergo peer-review process with up to two reviewers and 2012 has so far brought the following statistics of submitted manuscripts:

- accepted 22 % (most of them after minor revision)
- rejected 22 % (most of them after revised version)
- out-of-scope: 11 % (before undergoing peer-review)
- under review 44 %

that reflects sound peer-review process.

The whole EB is committed to shorten the review process and we cordially thank all reviewers, past, present and future, for their dedicated work in due time (usually 4 weeks). We have not calculated the time between submission and decision of submitted manuscripts yet, but the time spread is big and mainly depends on the willingness of potential reviewers to accept a manuscript for peer-review. In these modern times when nobody has time it is hard to find reviewers, but a broad international network of experts that members of editorial board have makes our peer-review process objective and time efficient. I sincerely thank all members of editorial board for numerous e-mails in search for reviewers.

In this issue we publish the first professional paper, while we still wait and ask for a review paper solicited to the above areas to be published. Some short news may appear at the end of each issue as it used to be in the previous volumes.

Enjoy reading of the 3rd issue!

Marko Topič
Editor-in-Chief

P.S.

All papers published in Informacije MIDEM (since 1986) can be access electronically at <http://midem-drustvo.si/journal/home.aspx>.

Ultra-Compact Dual-Band 3-D Hilbert Resonator in LTCC Technology

Nikolina Janković, Vasa Radonić and Vesna Crnojević-Bengin

University of Novi Sad, Faculty of Technical Sciences, Novi Sad, Serbia

Abstract: An ultra-compact dual-band resonator is presented based on a three-dimensional Hilbert fractal curve, with the overall dimensions equal to only $\lambda_g/25 \times \lambda_g/25 \times \lambda_g/25$, where λ_g denotes the guided wavelength at the first resonant frequency. Although in essence being a conventional half-wavelength resonator, 3-D Hilbert resonator can also be used as a dual-band resonator since its first and second harmonic resonances can be independently controlled due to its multilayer geometry. The resonator has been fabricated in Low Temperature Co-fired Ceramics (LTCC) technology using DuPont 951 Green Tape and a very good agreement between the simulated and measured responses has been obtained, proving LTCC to be very suitable for the fabrication of multilayer microwave passive devices.

Keywords: microwave resonator, fractal curve, multilayer structure, LTCC, dual-band filter

Ultra kompakten dvopasovni resonator v LTCC tehnologiji

Izveček: Predstavljen je ultra kompakten dvopasovni resonator, ki temelji na tridimenzionalni Hilbertovi fraktalni krivulji. Velikosti so le $\lambda_g/25 \times \lambda_g/25 \times \lambda_g/25$, kjer λ_g predstavlja vodilno valovno dolžino pri prvi resonančni frekvenci. Čeprav je 3D Hilbertov resonator v osnovi klasičen pol-valoven resonator se ga, zaradi večplastne strukture in možnosti ločenega kontroliranja druge in tretje harmonične frekvence, uporablja kot dvopasovni resonator. Resonator je bil izdelan v tehnologiji DuPont 951 Green Tape nizkotemperaturne sočasno sintrane keramike (LTCC). Dobra ujemanja rezultatov simulacij z meritvami potrjujejo uporabnost LTCC postopka za izdelavo večslojnih mikrovalovnih pasivnih elementov.

Ključne besede: mikrovalovni resonator, fraktalne krivulje, večslojna struktura, LTCC, dvopasovni filter

* Corresponding Author's e-mail: nikolina@uns.ac.rs

1. Introduction

Due to the rapid development of various wireless communication systems, there is an ever-increasing demand for low-cost, high-performance and compact microwave devices such as filters and their building blocks - resonators. The most common approach to miniaturisation of microwave resonators is based on folding the conventional straight-line resonator in order to fit it in a smaller area. However, this also reduces performances of the resonator and the final filter.

Recently, deployment of fractal curves has been suggested as the most prominent way to reduce the size of a resonator, while preserving its performance, [1]. Due to their unique space-filling property, fractal curves theoretically allow the design of infinite-length lines on a finite substrate area. Different fractal geometries, most often Hilbert and Peano fractals, have been uti-

lized in the design of miniaturized antennas [2-7], high impedance surfaces, [8-9], left-handed metamaterials, [10], RFID tags, [11], and filters, [12-15]. In [16] we have shown that a planar resonator based on two-dimensional (2-D) Hilbert fractal curve is superior to all other non-fractal configurations, both in terms of the circuit size as well as in terms of the quality factor.

Resonators based on the three-dimensional (3-D) Hilbert fractal curve and several other multilayer geometries have been analysed and compared in [17]. 3-D Hilbert resonator has been proven to be superior to its 2-D counterparts as well as to other 3-D geometries.

On the other hand, beside compact size modern wireless systems also demand passive devices that simultaneously operate at two or more arbitrary (non-harmonically related) frequencies. This cannot be easily achieved by using conventional half-wavelength or

quarter-wavelength resonators since their harmonics cannot be independently controlled. In this paper, we show that 3-D Hilbert resonator can be used as a dual-band resonator, with arbitrarily positioned operating frequencies. Namely, mutual coupling between the adjacent conductive layers strongly affects the response of the resonator and the positions of the first and second resonant frequency can be almost independently controlled by proper variation of certain geometrical parameters.

The optimized resonator has been fabricated in Low Temperature Co-fired Ceramics (LTCC) technology. LTCC originates from microelectronics but is more and more used today in microwave engineering, since it involves single-step lamination and firing which makes it very reliable and particularly advantageous for fabrication of complex structures with many conductive layers.

2. Configuration and Results

Fractal curves are generated in an iterative manner by successive repetition of one geometrical shape with the other (that often is a collection of scaled copies of the first shape). After each iteration a fractal curve of the higher order is obtained, longer than the previous one, which better fills the space in which it is generated. This space-filling property of fractal curves offers high potentials for miniaturization of passive microwave circuits because, theoretically, the application of fractal curves allows the design of infinite-length lines on a finite substrate area. Fractal curves are characterized by the fractal (i.e. non-integer) dimension. The dimension of every fractal curve is a number between 1 and 2, and can be understood as a measure of the space-filling ability of the fractal curve. The higher the fractal dimension, the better the fractal curve fills the given area, therefore achieving higher compactness. Only a fractal curve with the maximal possible fractal dimension will after infinite number of iterations entirely fill the rectangular space in which it is designed. Three 2-D fractal curves are known that have maximal fractal dimension: square Sierpinski, Peano, and Hilbert fractals [18]. Unlike Peano and Hilbert, Square Sierpinski fractal has ends on the same side of the line, thus being unsuitable for the design of end-coupled microstrip resonators. Due to the specific shape of the line, Hilbert resonator exhibits larger inductance and therefore larger miniaturization potential than its Peano counterpart, and that is why Hilbert fractal has been chosen as the basis for this work.

3-D Hilbert fractal line can be designed analogously to its 2-D counterpart. In Fig. 1, 3-D Hilbert fractal curve

of the third order is shown that is used for the design of the 3-D Hilbert resonator. The proposed fractal resonator, shown in Fig. 2, consists of four conductive and five dielectric layers, placed over the common ground. DuPont 951 Green Tape has been used with dielectric constant and loss tangent of $\epsilon_r=7.8$ and 0.006, respectively. The thickness of each dielectric layer is initially chosen to be $H=400 \mu\text{m}$. The resonator is made of the conductive line whose width w and spacing g are equal in all layers, $w=g=200 \mu\text{m}$. Adjacent conductive layers are connected by vias whose diameters are equal to the width of the lines to achieve impedance matching. The resonator is capacitively coupled to 50Ω feed lines by using $50 \mu\text{m}$ gaps. The feed lines are positioned on the top (fourth) conductive layer. The role of the top dielectric layer is to provide that the conductive lines in the fourth layer have approximately the same characteristic impedance as those in the lower layers.

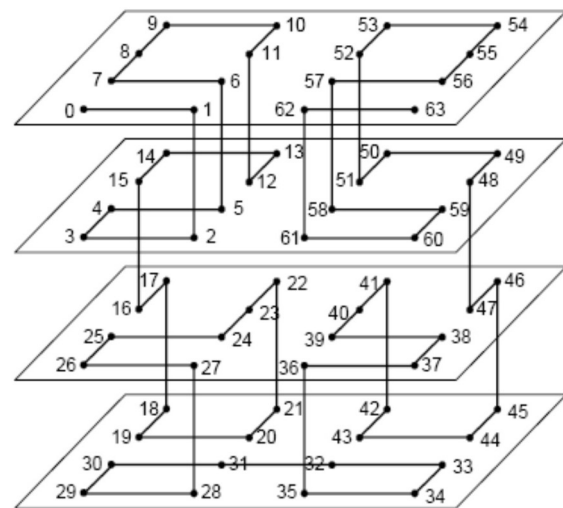


Figure 1: Schematic view of 3-D Hilbert fractal curve of the third order. The line starts at the node denoted with 0 and ends at the node denoted with 63.

Simulated response of the proposed resonator is shown in Fig. 3. The simulations have been carried out using Ansoft HFSS full-wave simulator. From the positions of maximums of H-field at the first and second resonant frequency, it is evident that the resonator behaves as a conventional half-wavelength resonator. The first resonance occurs at 3.32 GHz which corresponds well to the theoretical half-wavelength resonance on a given substrate, taking into account the mutual inductance between the adjacent layers that reduces the total inductance of the 3-D Hilbert resonator. The first resonance is characterized by high selectivity and low insertion loss of 1.85 dB. As expected, the second harmonic occurs at 7.23 GHz, i.e. at approximately twice the frequency of the fundamental resonance. It is also characterized by low insertion loss of 1.21 dB.

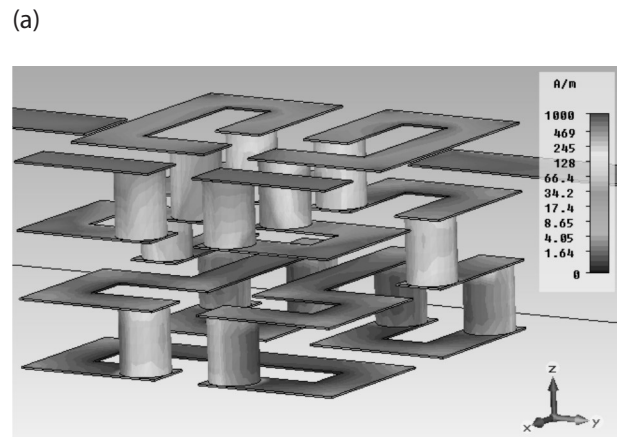
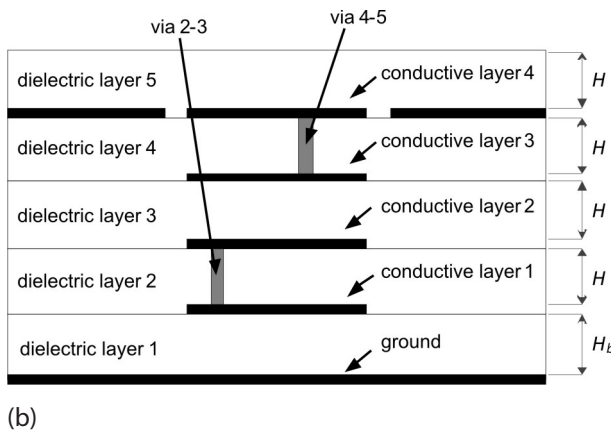
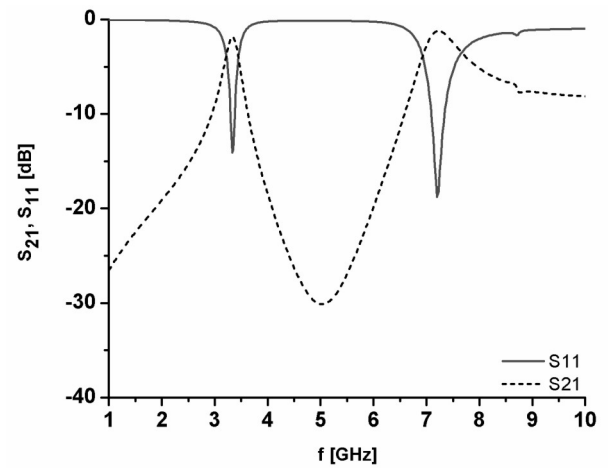
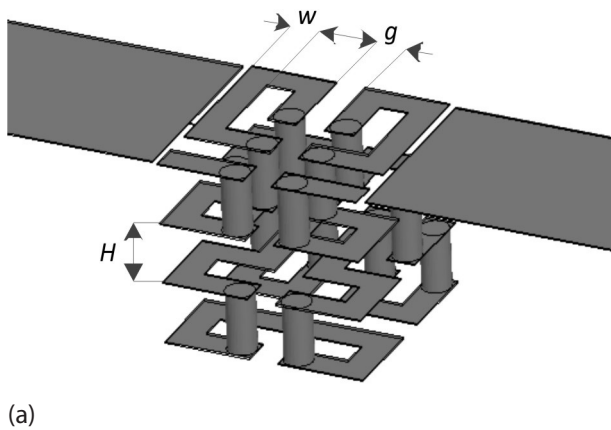


Figure 2: (a) 3-D Hilbert resonator. (b) Cross sectional view of the 3-D Hilbert resonator.

3. Influence of Different Geometrical Parameters on 3-D Hilbert Performances

In order to investigate influence of different geometrical parameters on the performance of the proposed resonator, firstly the fractal resonator line width and spacing have been simultaneously varied between $w=g=200\ \mu\text{m}$ and $w=g=350\ \mu\text{m}$, Fig. 4. As expected, both resonant frequencies are lowered as w and g are increased, due to changed inductance and capacitance of the resonator. At the same time, insertion losses are increased and the selectivity of the passbands is improved.

Dielectric layers in LTCC technology are made up of a number of Green tape layers. Therefore, they can have almost arbitrary overall thickness. We have investigated the influence of dielectric layer thickness on performance of 3-D Hilbert resonator by simultaneously varying thickness of all dielectric layers from $H=100\ \mu\text{m}$ to $H=400\ \mu\text{m}$. Fractal line width and spacing were

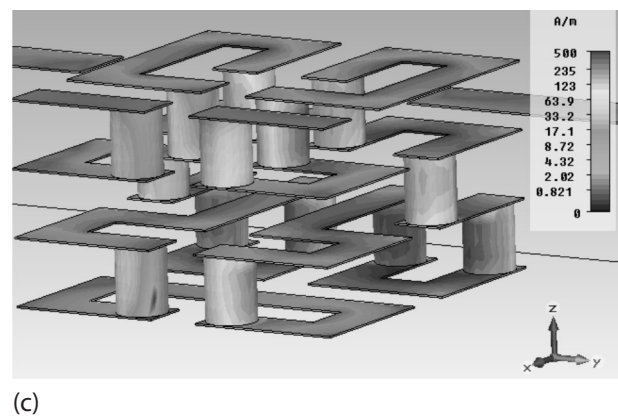


Figure 3: Simulated response of the 3-D Hilbert resonator: (a) Scattering parameters, (b) H-field at the first resonant frequency, (c) H-field at the second resonant frequency.

kept equal to $200\ \mu\text{m}$ in all cases, Fig. 5. Decreasing H enhances mutual coupling between the adjacent layers. Since maximums of E and H fields at the first and second resonance are located on different conductive layers of 3-D Hilbert, Fig. 3 (b) and (c), they are differently affected by changing the dielectric layer thickness: when H is decreased, the first resonance is shifted

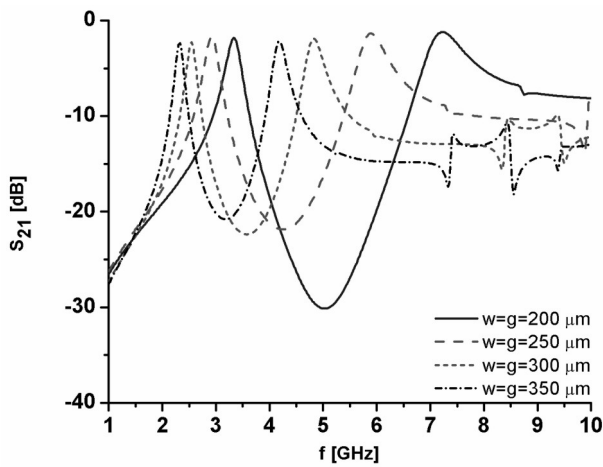


Figure 4: Influence of the line width w and spacing g of the 3-D Hilbert resonator on its performance.

towards higher frequencies while the second harmonic remains almost unaffected. Although decrease in layer thickness degrades the insertion losses, it represents a mechanism that can be used to change the position of the first resonance and, at the same time, keep the second harmonic unaffected, thus opening up possibilities to use 3-D Hilbert resonator as a dual-band resonator with independently positioned passbands.

It is also interesting to note how a change in the thickness of the bottom dielectric layer only, denoted with H_b in Fig. 2(b), affects the response of the resonator. A configuration with thickness of all dielectric layers equal to $H=H_b=400 \mu\text{m}$ has been compared to the one where the thickness of the lowest dielectric layer is reduced to $H_b=100 \mu\text{m}$. Decreasing H_b increases the capacitance between the resonator and the ground. The maximum of E field is located in the top conductive layer in the case of the first resonance, and in the bottom conductive layer in the case of the second resonance. Therefore, only the second resonance is significantly affected by changing H_b which results in a shift of the second harmonic towards lower frequencies, Fig. 6, while the first resonance remains unchanged. This presents additional mechanism for independent control of positions of the two passbands of 3-D Hilbert dual-band resonator.

It can be concluded that changing the layer thickness, i.e. changing the mutual coupling between the layers is the key mechanism to vary relative position of the first and second resonance, i.e. to independently control the positions of the passbands. Therefore, 3-D Hilbert resonator can be used as a dual-band resonator, where relative position of two resonances can be changed in the range from 1.29 to 2.18, as seen in Fig. 5 and Fig. 6.

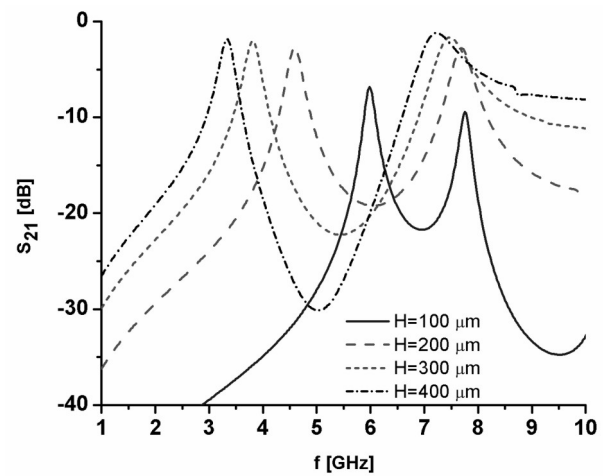


Figure 5: Influence of the thickness of the dielectric layers H on the performance of 3-D Hilbert resonator. Thickness of all dielectric layers H is varied simultaneously. Fractal line width and spacing are equal to 200 μm in all cases.

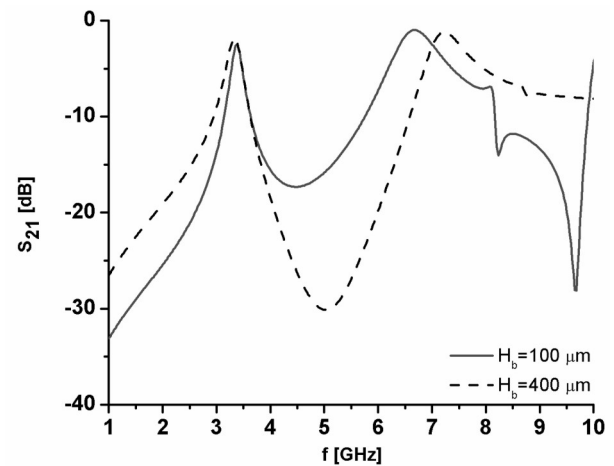


Figure 6: Influence of the thickness of the bottom dielectric layer, H_b . All upper dielectric layers are $H=400 \mu\text{m}$ thick. Fractal line width and spacing are equal to 200 μm .

4. Fabrication and Measurement Results

Analysis presented above also reveals that various optimisation goals used in the design of dual-band 3-D Hilbert resonator, namely minimisation of insertion losses at both resonances, maximisation of the attenuation in the stop band and selectivity of the passbands, are contradictory and thus a trade-off is needed. The configuration with $H=H_b=400 \mu\text{m}$ and $w=g=300 \mu\text{m}$ offers the best trade-off and it has been selected for fabrication. The first and second resonances are positioned

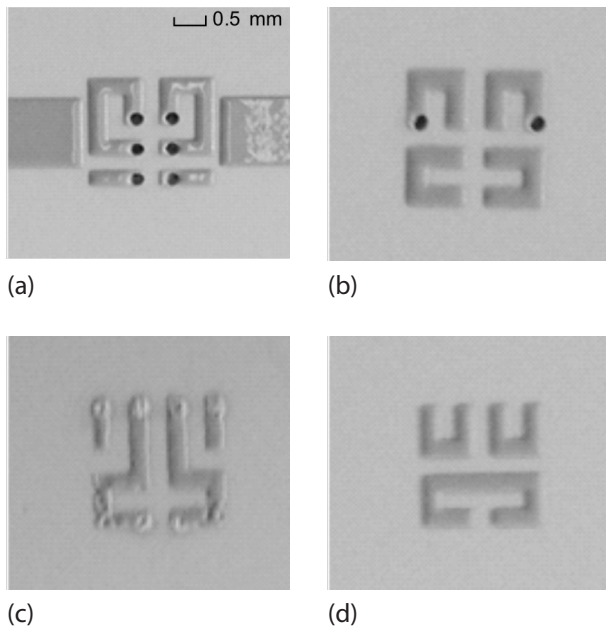


Figure 7: Photographs of the conductive layers of the resonator after conductor printing: (a) conductive layer 4 (top), (b) conductive layer 3, (c) conductive layer 2, (d) conductive layer 1 (bottom).

at 2.55 GHz and 4.83 GHz and corresponding insertion losses are -2.28 dB and -1.88 dB, respectively. The overall dimensions of the resonator are ultra-compact: They are equal to only $2.1 \times 2.1 \times 2 \text{ mm}^3$ i.e. $\lambda_g/25 \times \lambda_g/25 \times \lambda_g/25$, where λ_g is the guided wavelength.

To validate the simulation results, the optimised 3-D Hilbert resonator has been fabricated in LTCC technology. Since the minimum available spacing between two lines in the fabrication process available to us was 120 μm , the resonator with 120 μm gaps to the feed lines has been fabricated, instead of 50 μm used in simulations to characterize the resonator. This change is not crucial, since it practically influences only the insertion losses. Furthermore, it should be noted that gaps of 50 μm are achievable in standard LTCC technology by using screens with higher resolution or by laser trimming.

Standard LTCC procedure that includes several well-known steps was used. DuPont 951 Green Tape has been used for the fabrication of dielectric layers, with thickness equal to 114 μm . Since dielectric layers of the resonator should be 400 μm thick, and since shrinking of approximately 14% was specified, four green tapes have been used for each layer.

After preconditioning of the tapes, via holes were patterned and filled, and conductors in all four conductive layers were printed. For via filling and printing of the conductive layers, DuPont 6141 and 6142D silver pastes compatible with Green tape have been used.

Since the via diameter is equal to the line width, a great degree of precision during the process of via processing was required. Also, considerable attention was paid to via filling to ensure a good connection between adjacent conductive layers. Fig. 7 shows photographs of the conductive layers of the resonator after conductor printing. It can be seen that all lines and spacings have been accurately reproduced, using standard LTCC procedure and with no laser trimming. This proves the potential of LTCC technology for fabrication of compact microwave passive devices. Fig. 8 shows microscopic view of the filled via holes that connect the third and fourth conductive layer. All vias were filled entirely, resulting in minimized losses observed in the measured response.

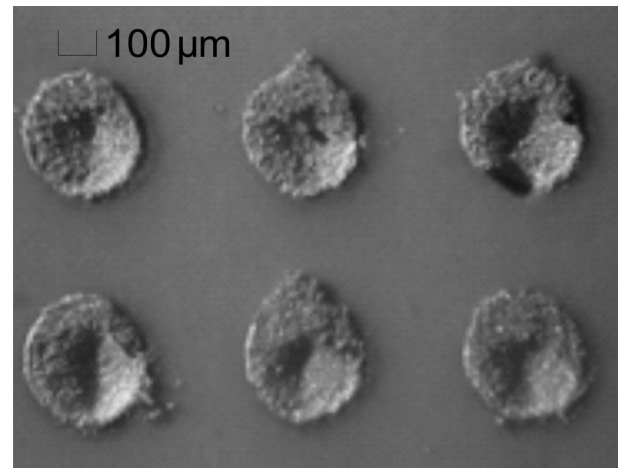


Figure 8: Microscopic view of the filled via holes that connect the third and fourth conductive layers.

In lamination process all layers were stacked together, placed in a vacuum sealed package, and pressed in water in an isostatic press at around 70°C and 3 MPa during 5 minutes. Afterwards, the laminated circuit has been fired in the furnace according to a firing profile given by the manufacturer [19]. After firing and shrinkage of the green tapes, the desired thickness of the layers has been achieved.

In order to enable soldering of connectors to the fabricated circuit, 3 mm x 3.5 mm slits in the top dielectric layer above the feed lines have been made. A special attention was paid to soldering the connectors: it was performed on a pre-heated circuit to avoid defects which might occur due to non-uniform heating of the structure.

Comparison of simulated and measured responses reveals a very good agreement, Fig. 9. The fabricated dual-band 3-D Hilbert resonator exhibits insertion losses of 3.7 dB and 3.8 dB at 2.63 GHz and 5.09 GHz, respectively, while the attenuation between the passbands is more than 27 dB. Fractional bandwidths are 6.8% and

5.3%, respectively. The obtained measurement results also prove that LTCC technology can straightforwardly be used for fabrication of ultra-compact microwave multilayer structures.

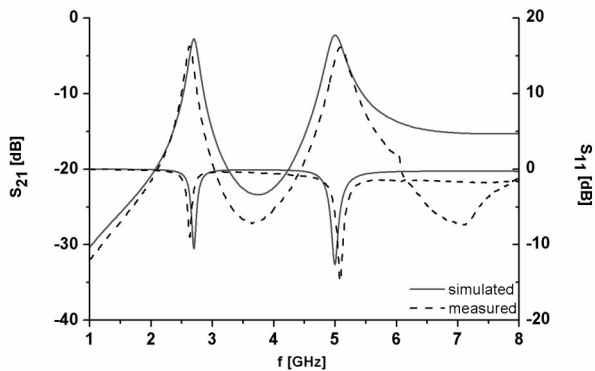


Figure 9: Simulated (red fullline) and measured (black dashed line) responses of the 3-D Hilbert resonator in LTCC technology.

5. Conclusion

In this paper, an ultra-compact dual-band multilayer microstrip resonator with overall dimensions equal to $\lambda_g/25 \times \lambda_g/25 \times \lambda_g/25$ based on 3-D Hilbert fractal curve has been proposed. The influence of different geometrical parameters to its performances has been analysed in detail.

Although the resonator is basically a conventional half-wavelength resonator, it has been shown that it can be used as a dual-band resonator that operates at arbitrary (non-harmonic) frequencies, due to the fact that its multilayer configuration provides a mechanism for independent control of the first and second resonance.

The resonator that offers the best trade-off between the insertion losses, attenuation and selectivity has been designed to operate at 2.55 GHz and 4.83 GHz with insertion losses of -2.28 dB and -1.88 dB, respectively. The resonator has been fabricated in LTCC technology using DuPont 951 Green Tape. The simulated and measured responses agree very well, proving the potential of LTCC technology for fabrication of ultra-compact multilayer microwave passive devices.

Acknowledgement

The authors thank Prof. George Goussetis and Yves Lacrotte from Heriot-Watt University, United Kingdom, for their help with fabrication of the circuit in LTCC technology.

References

1. P. Jarry and J. Beneat, Design and realization of miniaturized fractal RF and microwave filters. New Jersey, John Wiley, 2009.
2. K.J. Vinoy, K.A. Jose, V.K. Varadan, and V.V. Varadan, "Hilbert curve fractal antenna: A small resonant antenna for VHF/UHF applications," Microwave and Optical Technology Letters, vol. 29, pp. 215–219, 2001.
3. J. Anguera, C. Puente, E. Martínez, and E. Rozan, "The fractal Hilbert monopole: A two-dimensional wire," Microwave and Optical Technology Letters, vol. 36, pp. 102–104, 2003.
4. J. Zhu, A. Hoorfar, and N. Engheta, "Bandwidth, cross-polarization, and feed-point characteristics of matched Hilbert antennas," IEEE Antennas Wireless Propagation Letters, vol. 2, pp. 2–5, 2003.
5. J. Zhu, A. Hoorfar, and N. Engheta, "Peano antennas," IEEE Antennas Wireless Propagation Letters, vol. 3, pp. 71–74, 2004.
6. W. Chen, G. Wang, C. Zhang, "Small-size microstrip patch antennas combining Koch and Sierpinski fractal shapes," Antennas and Wireless Propagation Letters, vol. 7, pp. 738–741, July 2008.
7. L. Yousefi, O.M. Ramahi, "Miniaturised antennas using artificial magnetic materials," Electronics Letters, vol. 46, pp. 816–817, June 2010.
8. J. McVay, N. Engheta, and A. Hoorfar, "High-impedance metamaterial surfaces using Hilbert-curve inclusions," IEEE Microwave and Wireless Components Letters, vol. 14, no. 3, pp. 130–132, March 2004.
9. J. McVay, A. Hoorfar, and N. Engheta, "Peano high-impedance surfaces," Radio Sci, 40, RS6S03, 2005.
10. J. McVay, N. Engheta, and A. Hoorfar, "Numerical study and parameter estimation for double-negative metamaterials with Hilbert-curve inclusions," Proceedings of 2005 IEEE Antennas Propagation Society International Symposium, Washington, DC, vol. 2B, pp. 328–331, July 2005.
11. J. McVay, A. Hoorfar, and N. Engheta, "Space-filling curve RFID tags," Proceedings of IEEE Radio and Wireless Symposium, San Diego, CA, pp. 199–202, January 2006.
12. N. Janković, V. Radonić and V. Crnojević-Bengin, "Novel bandpass filters based on grounded Hilbert fractal resonators," 3rd International Congress on Advanced Electromagnetic Materials in Microwaves and Optics, London, UK, August 2009.
13. W. Chen, G. Wang, "Effective design of novel compact fractal-shaped microstrip coupled line bandpass filters for suppression of the second harmonic," Microwave and Wireless Component Letters, vol. 19, pp. 74–76, February 2009.

14. D. Oloumi, A. Kordzadeh, A. Neyestanak, "Size reduction and bandwidth enhancement of a waveguide bandpass filter using fractal-shaped irises," *Antennas and Wireless Propagation Letters*, vol. 8, pp. 1214-1217, October 2009.
15. H. Xu, G. Wang, C. Zhang, "Fractal-shaped UWB bandpass filter based on composite right/left handed transmission line," *Electronics Letters*, vol. 46, pp. 285-287, February 2010.
16. V. Crnojević-Bengin, "Novel compact microstrip resonators with multiple 2-D Hilbert fractal curves," *Microwave and Optical Technology Letters*, vol. 48, no.2, pp.270-273, February 2006.
17. V. Crnojević-Bengin and Đ. Budimir, "Novel 3-D Hilbert microstrip resonators," *Microwave and Optical Technology Letters*, vol. 46, no. 3, pp. 195-197, August 2005.
18. V. Crnojević-Bengin, V. Radonić and B. Jokanović, "Fractal Geometries of Complementary Split-Ring Resonators," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 10, pp. 2312- 2321, Oct. 2008.
19. http://www2.dupont.com/MCM/en_US/assets/downloads/prodinfo/951LTCCGreenTape.pdf

Arrived: 16. 08. 2012

Accepted: 12. 11. 2012

On-line Testing and Recovery of Systems on SRAM-based FPGA

Uroš Legat

Jožef Stefan Institute, Ljubljana, Slovenia

Abstract: This paper outlines the techniques of on-line testing, error-mitigation and error recovery for SRAM-based FPGAs and gives guidelines how to make a small and efficient error recovery mechanism. The mechanism checks the configuration memory of the FPGA and reconfigures the FPGA if the error occurs. Triple-modular redundancy was applied to the mechanism to increase its reliability. The error recovery mechanism was implemented in Virtex 5 FPGA and verified on two user applications.

Keywords: *FPGA, single-event upset, on-line testing, error-mitigation, error-recovery*

Sprotno testiranje in popravljanje sistemov osnovanih na vezjih FPGA

Izveček: Uvodoma članek razloži tehnike sprotnega testiranja, izogibanja napak in popravljanja napak na vezjih FPGA osnovanih na statičnem pomnilniku, kasneje pa poda navodila za izdelavo majhnega in učinkovitega mehanizma za sprotno popravljanje napak. Mehanizem sprti pregleduje konfiguracijski spomin vezij FPGA in reprogamira vezje na mestu, kjer najde napako. Mehanizem je implementiran po metodi trojne modularne redundance, s čemer mu povečamo zanesljivost. Mehanizem za popravljanje napak je narejen in preverjen za Virtex 5 FPGA, vendar ga z manjšimi modifikacijami lahko prenesemo tudi na druge tipe FPGA vezij.

Ključne besede: *FPGA, napake SEU, sprotno testiranje, izogibanje napakam, popravljannje napak*

* *Corresponding Author's e-mail: uros.legat@ijs.si*

1. Introduction

SRAM-based FPGAs have become an attractive solution for many applications where a short development time, low-cost for low-production volumes and in-the-field-programming ability are important issues. The flexibility of SRAM-based FPGAs comes from the adoption of a configuration memory that defines the operations of the circuit that the FPGA implements. It is therefore fundamental that the content of the configuration memory preserves the correct values during the FPGA operation. An important concern for the reliability and dependability of SRAM-based FPGAs are radiation-induced soft-errors that corrupt the configuration memory (produce bit-flips). These errors often occur in the space environment; however, because of increasing integration density they are also not uncommon at sea-level.

Different fault-tolerance techniques have been developed to increase the reliability and dependability of applications on FPGAs [1]. These techniques function concurrently (on-line) with the system to monitor its

operation. On-line testing techniques detect the errors in the system, error mitigation techniques are able to enhance the system to work despite faults, and error-recovery techniques recover the faults from the system. The goals of the fault-tolerance techniques are to minimize the hardware, timing, and power overhead, and maximize the reliability of the system.

The paper is organized as follows. Section 2 describes how soft-errors corrupt the operation of SRAM-based FPGAs. Section 3 explains the state of the art fault tolerance techniques. In section 4 error recovery mechanism (ERM) in different FPGAs is described. Section 5 shows the implementation of the ERM in Xilinx Virtex 5 FPGA and section 6 concludes the paper.

2. Soft errors in SRAM-based FPGAs

SRAM-based FPGAs are susceptible to radiation-induced soft-errors. The main FPGA reliability concern is a type of soft-error called single-event upset (SEU).

A SEU occurs when a charged particle strikes a memory cell and changes its state. For example, a typical SRAM memory cell is comprised of four transistors shown in Figure 1. A memory cell has two stable states that represent one bit of stored information. In each state two transistors are turned off (SEU target drains). When a charged particle strikes a drain in an off state transistor as in Figure 1, it can generate a transient current pulse to turn the gate of the opposite transistor on, which changes the state of the memory cell.

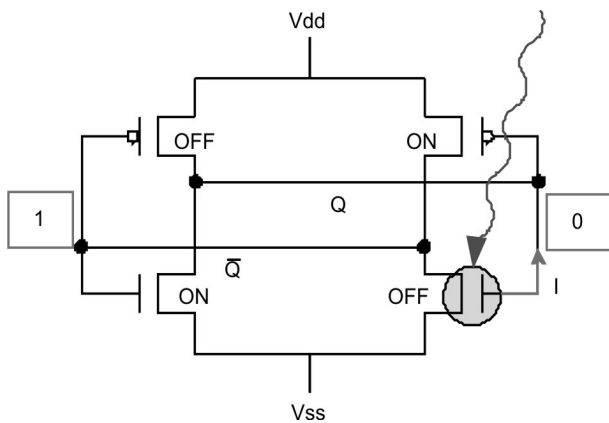


Figure 1: SEU in a SRAM memory cell

Configuration memory of a SRAM-based FPGA is comprised of SRAM memory cells. A charged particle can cause a bit-flip in the configuration memory cell and consequently alter the FPGA functionality.

A configuration bit is associated with a particular part of the FPGA. It can be a part of an internal memory of the device like an internal RAM or flip-flop, or it can represent a functional part of the design, like a Logic Block (LB), or internal routing [4].

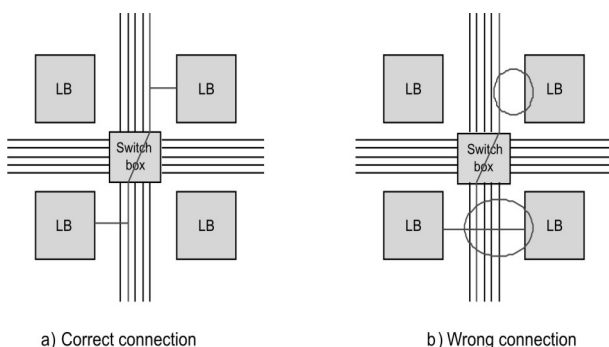


Figure 2: SEU in an internal FPGA routing

The internal routing interconnects the LBs, I/O blocks and other functional blocks of the FPGA. The routing consists of switch boxes that connect the main wires and smaller wiring segments that connect the main wires to LBs, shown in Figure 2 a. These connections are determined by the logic state of their configuration

bits. A SEU affecting these configuration bits could disconnect the original LB connection, or in another case, connect wrong LBs. For illustration, some typical faults are marked in Figure 2 b.

The simplified structure of a LB is shown in Figure 3. The LB in Xilinx FPGA consists of a number of look-up tables, flip-flops and internal carry and control logic. The SEU can alter the logic function of the LUT, alter the connections inside the Carry and control logic, change the contents of the flip-flop, etc.

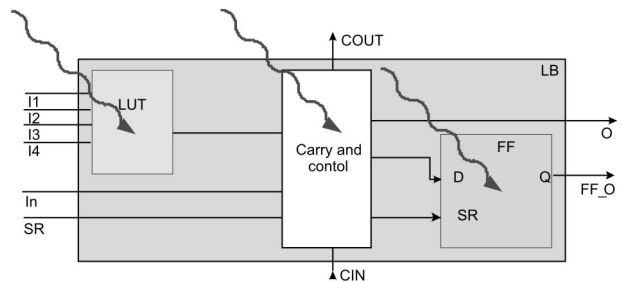


Figure 3: SEU in Logic Block

3. On-line testing and fault tolerance techniques

Different techniques have been proposed to test and protect SRAM FPGAs from SEU. On-line testing techniques detect errors during the normal operation of the system. On-line detection of errors shortens fault-detection latency, which is very important in order to prevent the fault from propagating further through the system. On the other hand, error-mitigation techniques can tolerate faults that occur during the system operation. If a fault occurs in one part of the circuit, then a redundant part of the circuit is used to provide the correct and uninterrupted operation of the system. When a fault is detected inside a system it can be repaired (recovered) by error-recovery techniques.

On-line testing techniques

On-line testing is performed while the circuit is performing its assigned task. Two types of on-line test are distinguished in the literature: the concurrent and the non-concurrent on-line test.

A non-concurrent on-line test is usually triggered in phases of system inactivity or in periodic and scheduled times when the normal function of the system is interrupted. Non-concurrent testing is used to detect permanent faults (SEU) and cannot detect transient faults (SET), whose effects disappear quickly. The non-concurrent on-line test is performed only virtu-

ally in parallel to system operation. Therefore, it is in some literature classified as an off-line technique. We give some examples of non-concurrent on-line testing techniques. The authors in [5] used scan chains to periodically check the system while [6] used logic BIST. Authors in [7] implemented a periodic on-line test in an embedded microprocessor.

A concurrent on-line test runs in concurrence with the system and does not interrupt its normal operation. The concurrent testing techniques use different kinds of redundancies to detect errors. Time redundancy is normally used to detect a transient faults in combinational circuits, while hardware redundancy is used to detect a SEU in sequential circuits or configuration memory. The on-line testing principle is depicted in Figure 4. Test vectors are generated by the normal operational inputs. Besides the original circuit there is a redundant part of the circuit that produces additional encoded outputs. A checker is monitoring these outputs and thus performs error detection.

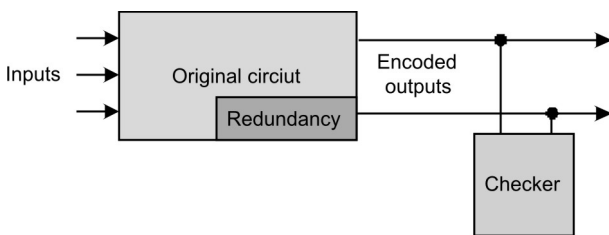


Figure 4: Concurrent on-line testing principle

A system protected with the concurrent on-line testing technique is also called a self-checking system [8]. The desirable goal of self-checking systems is to achieve the so-called totally self-checking property. This property requires that every fault in the system is detected before or at the time this fault produces an erroneous output. To achieve this goal the system has to meet the following criteria [9]:

- Fault secure criterion requires that any fault in the system produces erroneous outputs that can be detected at the output. This criterion assures that every single fault can be detected.
- Self-testing criterion requires that for each fault there is at least one input vector, occurring during normal operation of the circuit, which detects it.

The most straight forward hardware redundancy technique is duplication and comparison. The principle of the technique is that we make two copies of the circuit which run in parallel. The duplicates receive identical inputs. The outputs of the both circuits are compared by the comparator circuit. This technique increases the hardware cost by more than 100%. Duplication and comparison is used in a variety of different systems. In

this way, on-line testing of embedded processor cores was improved by [10]. Processor cores are duplicated and a checker monitors whether the outputs of both cores match. If the outputs mismatch the processor state is restored from the previously saved states (checkpoint and rollback recovery method). Applicability of duplication and comparison in asynchronous circuits was investigated in [11]. Testing of finite-state machines using a technique similar to duplication and comparison was proposed in [12].

To reduce hardware cost, other more elaborate techniques are employed. These techniques use error-detecting codes (EDC) with costs lower than the duplication. The EDCs are used in sequential circuits and in memories. The codes that are used for error detection are: Parity codes, Hamming codes, Dual-rail codes, m out of n codes, Berger codes, and Arithmetic codes.

The most commonly used codes for error detection in FPGA configuration memories are the so called Single-error detection double-error correction (SEC-DED) Hamming codes [13] and Cyclic Redundancy Check (CRC) [14].

Error-mitigation techniques

For mission-critical systems it is sometimes not enough to only detect a fault, but also to operate in the presence of a fault which is possible by applying error-mitigation techniques. These techniques are also based on different kinds of redundancies.

The best-known hardware-redundancy mitigation technique is Triple Modular Redundancy (TMR). This technique is one of the n-modular redundancy techniques which were derived by [15]. The basic TMR technique triplicates the entire circuit into three modules and places the majority voter at the output of the modules. This method is effective against SETs and SEUs that occur in a single design module. However, if the upset occurs in the majority voter circuit the basic TMR is ineffective and a wrong value will be presented at the output. The hardware overhead of this method is three times the original design plus the voter circuit. While the hardware overhead is large, some have proposed partial TMR techniques which are focused only on tripling the specific sensitive logic [16].

The basic TMR solution does not avoid the accumulation of upsets. The FPGAs cope with this problem by implementing an on-line error-recovery technique.

To apply the TMR technique effectively in the FPGA device additional restrictions have to be considered. The triplicated modules have to be placed isolated from

each other (different clock regions) and the internal signals have to be carefully routed to limit the possibility that an upset would affect more than one module. All the modules have to have separate clock and input signals. Routing the TMR design in the FPGA is a particularly hard problem. Various algorithms and design methods have been proposed to reduce the number of such errors [17,18].

For Xilinx FPGAs a special hardened TMR architecture has been proposed in [19]. This architecture can also be automatically generated by their tool (Xilinx TMRTool). The XTMR is exploited based on the states recovery TMR method and uses specific FPGA resources to implement the majority voters. The Xilinx TMR is depicted in Figure 5:

- Inputs are connected outside of the FPGA and separated inside the FPGA.
- Combinational logic is triplicated.
- Sequential logic is implemented with majority voters and feedback loops.
- Outputs are implemented using tri-state output buffers in combination with minority voters.

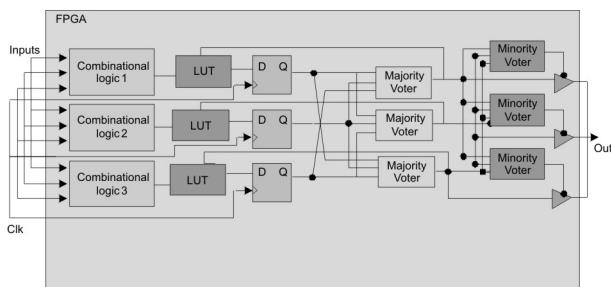


Figure 5: The architecture of Xilinx TMR

Error-recovery techniques in SRAM-based FPGAs

The configuration memory of the FPGA determines the functionality of the FPGA. The original configuration is downloaded into an FPGA at the power-up. During the operation of the device a SEU can occur, which changes the configuration of the FPGA. The error-recovery techniques are used to recover the original state of the configuration memory.

Simple error-recovery techniques (scrubbing techniques) only periodically reconfigure the whole device from the external memory. The external memory has to be radiation hardened and reliable to assure the correctness of the original (“Golden copy”) configuration memory. The scrubbing period has to be adjusted to be less than the estimated mean time between two SEUs.

More advanced error-recovery techniques check whether the configuration memory is correct during the normal operation of the user application and can

be regarded as on-line recovery techniques. These techniques require an error-recovery mechanism that monitors the configuration memory and in the case of an error recovers only the faulty bits using the partial runtime reconfiguration of the FPGA.

The recovery mechanism uses different ECCs to check the configuration memory. In [20, 21] Hamming code is used. The Hamming check bits are stored within the configuration of the Xilinx FPGAs. Asadi et al. [22] used Cyclic Redundancy Check (CRC) of the configuration memory. The CRC values are stored separately inside the internal memory of the FPGA.

Depending on which FPGA configuration interface is used to reconfigure the device, the recovery techniques are classified as either external or internal. The external techniques use one of the external configuration ports (i.e., JTAG, SelectMap). The external recovery technique requires a reliable recovery mechanism. Hulme et al. [23] proposed a radiation-hardened processor to control the recovery process, Asadi et al. [22] used a small auxiliary FPGA to check the main FPGA for errors, and Berg et al. [24] implemented a controller in ASIC.

An external recovery mechanism produces extra implementation costs. Hence, internal SEU-recovery techniques were proposed. They use internal configuration interface (for example, the internal-configuration-access-port-ICAP). The internal recovery controller is implemented in the FPGA along with the user application. It has to be small, fast and reliable. Heiner et al. [20] and Chapman [21] use an embedded microprocessor (PisoBlaze) as a configuration controller while Legat et. al. [25] use a small hardware mechanism based on finite state machine (FSM).

4. Mechanism for on-line test and recovery of errors in SRAM based FPGAs

In this section the knowledge of on-line testing, error mitigation and error recovery are used to show how to develop an efficient internal error-recovery mechanism (ERM) for SRAM FPGAs. The ERM will be able to test the configuration memory of SRAM FPGAs during the operation of the device (on-line) and recover errors through reconfiguration. The mechanism will be implemented in TMR to increase its reliability.

On-line test of the FPGA configuration memory

The functionality of a SRAM FPGA is determined by the state of its configuration memory (i.e., the SRAM cells).

The configuration memory in Xilinx, Atmel or Altera FPGA devices is organized in a network of configuration frames that are laid out on a device according to their frame address. A configuration frame is the smallest reconfigurable part of an FPGA. The content of the configuration memory is loaded through the configuration interface at the initial configuration of the device and must remain unchanged during its operation.

The basic idea of the mechanism is to continuously read the contents of the configuration memory during the operation of the device through a configuration port and check its integrity. Some of the SRAM-based FPGA devices have an internal configuration port which can be directly accessed by the mechanism; other devices have to use an external connection to configuration pins.

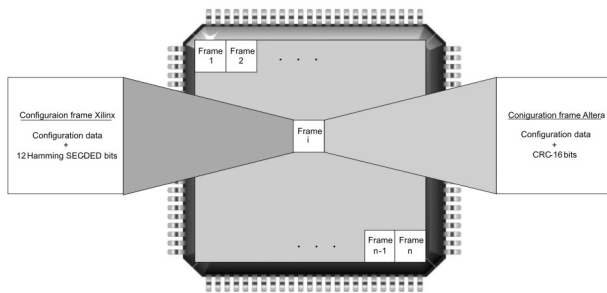


Figure 6: The structure of configuration memory in SRAM-based FPGAs

To validate the integrity of the configuration memory the mechanism reads the configuration memory frame by frame and checks the frame data using an ECC. Different FPGAs use different ECCs in their configuration frames. Figure 6 shows the structure of the configuration frames of Xilinx and Altera FPGAs.

Xilinx FPGAs

Each configuration frame in Xilinx FPGA device contains 12 parity bits. These are the parity bits of the Hamming SEC-DED Error Correction Code (ECC). The parities are pre-calculated and stored with the configuration data. To perform the error-detection we have to implement a *Hamming decoder*. As the configuration frame is read through the configuration port the Hamming decoder calculates a syndrome value. The syndrome is calculated from the 12 parity bits and the rest of the read frame data. The first 11 bits of the syndrome value identify the location of a single erroneous bit within the frame (including the errors in the parity bits), while the last bit of the syndrome value indicates the double error in the frame.

Altera FPGAs

Each configuration frame in Altera FPGA device contains a CRC-16. The 16 check bits are pre-calculated

and appended to the configuration data. For error-detection we have to implement a LFSR. The LFSR uses 16 flip-flops and three XOR gates placed at the positions determined by the generator polynomial $(x^{16}+x^{15}+x^2+1)$. As the frame is read the configuration frame data is shifted through the LFSR and the output of the LFSR is checked at the end of the readback. The CRC can detect single and multiple faults in the frame, but it cannot determine the position of the error.

Error-recovery procedure

When an error is detected in a configuration frame, the mechanism triggers error recovery procedure. The error recovery is the process of correcting the configuration memory through configuration port. The FPGA devices that do not have partial reconfiguration capabilities have to stop and reconfigure the whole configuration memory. Some of the FPGA devices enable partial runtime reconfiguration (newer Xilinx, Altera, and Atmel FPGAs). These devices can recover a single faulty frame during the operation of the device. The recovery procedure goes as follows:

In Xilinx FPGAs (Virtex family) the ERM does not require an external memory for the recovery of single faults. The SEC-DED Hamming ECC determines the location of a single error inside the configuration frame. The ERM corrects the faulty bit in the read configuration frame and reconfigures it. If a double error occurs in a configuration frame the recovery procedure is only possible from the external memory.

In Altera FPGAs (Stratix and Cyclone families) the location of the error inside the frame is unknown; therefore the original frame data has to be stored in the external memory. The corrupted frame is read from the external memory and reconfigured using partial runtime reconfiguration.

Implementation of error recovery mechanism

The hardware architecture of ERM is shown in Figure 7. It consists of *configuration port, ECC core, internal FPGA RAM, and control logic*.

The FPGA device is configured by writing the configuration commands into the configuration registers. The configuration user guides of particular FPGA devices give a detailed description of the register types and commands to perform the configuration operations.

The configuration port can be internal or external. It has direct access to the configuration registers and configuration data. The error-recovery mechanism uses the port to read and write a configuration frame.

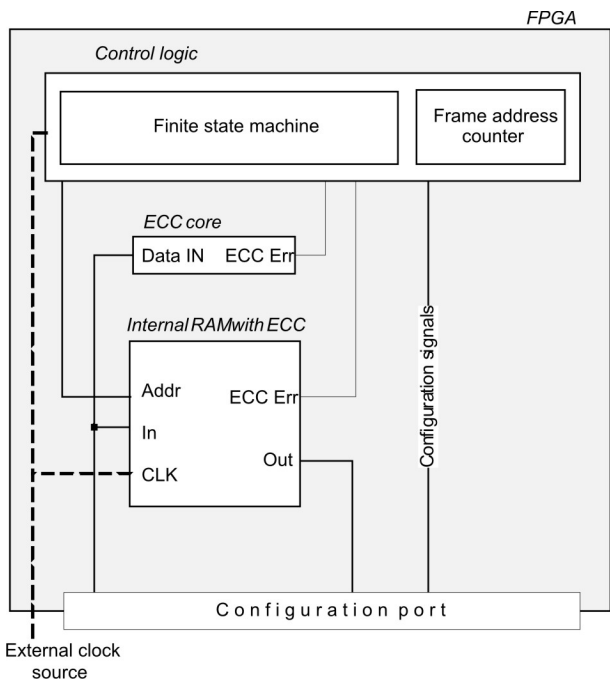


Figure 7: Hardware architecture of the error-recovery mechanism

The readback and reconfiguration operations are performed using an appropriate sequence of configuration commands sent to the inputs of the port. These commands are predefined and stored in the internal FPGA memory.

The ECC core is used to detect errors inside the FPGA configuration frame. Depending on the FPGA family this can be a Hamming decoder or a CRC LFSR. The ECC device checks the configuration frame while the frame is read through the configuration port.

The internal FPGA RAM contains the configuration commands and temporarily stores the current configuration frame. The internal RAM is also susceptible to SEU. To protect the integrity of the RAM content most of the FPGAs devices have an embedded Hamming SEC-DED ECC circuit.

The control logic manages the error detection-and-correction process. The controller is composed of a *Finite State Machine (FSM)* and a *Frame address counter*. The FSM controls the operation of the mechanism. When the next frame address is required the Frame address counter is incremented. When the frame address reaches the last frame, the counter is reset back to the initial value pointing to the first frame.

TMR implementation of the error recovery mechanism

The internal error-recovery mechanism is also susceptible to SEUs. A critical fault in the mechanism could cause a system-wide corruption of the configuration data. Therefore, it is essential that the logic of the ERM is protected by some SEU-mitigation technique.

The ERM can be implemented in TMR. The hardware architecture of the TMR is depicted in Figure 8. The TMR structure can be applied to the control logic, ECC core and the internal RAMs. These components of the ERM are triplicated in three design modules. A majority voter is placed at the inputs of the configuration port. The outputs of the configuration port are triplicated outside the FPGA are connected to the three design modules inside FPGA. The triplicated design modules are clocked by separate synchronous clock signals.

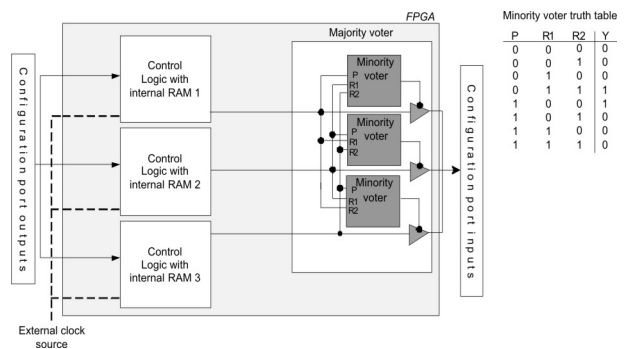


Figure 8: Hardware architecture of the TMR version of the error-recovery mechanism

The majority voter can be regarded as a single point of failure. The recommended implementation of the majority voter in FPGAs is shown in Figure 8. This majority voter implementation is immune to the single points of failures. The majority voter is implemented using three output tri-state buffers that are a part of the FPGA OI blocks, and three minority voters. The operation of the voter is as follows: If the primary signal (P) of the minority voter is a part of the majority (see the minority voter truth table in Figure 8), then the minority voter will enable the corresponding (active low) output buffer allowing the data on the output. If the primary path is not a part of the majority, then the output buffer is disabled placing its output in a high-impedance state allowing the redundant outputs to drive the correct data.

To apply the TMR technique effectively in the FPGA device additional restrictions have to be considered. The triplicated modules have to be placed in such a way that they are isolated from each other and the internal signals have to be carefully routed to limit the possibility that an upset would affect more than one module.

5. Implementation details and operation of ERM

The proposed ERM was implemented in Xilinx Virtex 5 (XC5VLX30) FPGA [25]. An internal-configuration access-port (ICAP) was used to access the configuration memory. A frame ECC device was used to check the frame data and a FSM was built to control the process of configuration scan and recovery. The ERM was also implemented in TMR.

Implementation details of original ERM vs. TMR design

Implementation details of the ERM implemented in Virtex 5 are shown in Table 1. It occupies just 72 slices, 115 Flip-flop registers and 1 internal block RAM. A total of 36 kb of RAM is used with embedded ECC. The mechanism utilizes less than 1% of the resources available on the FPGA. Implementation can differ slightly when different options are selected in the synthesis tools. In comparison with the original version of the recovery mechanism TMR increases the number of occupied resources by some more than three times.

The power consumption of both versions of ERM was analyzed using Xilinx XPower tool on Virtex 5 FPGA at 100 MHz clock rate. The dynamic power consumption of the ERM is negligible in comparison with the static leakage of the FPGA. The TMR version of the mechanism has approximately three times higher dynamic power consumption than the original mechanism. On the other hand, due to the high static power consumption of the FPGA the total power consumption of the TMR version is only 4% higher than the power consumption of the original mechanism.

Table 1: Comparison of resources, power, and timing of the original and TMR version of ERM

Virtex 5	Original mechanism	TMR mechanism
Resources		
Slices	72	321
Flip-flops	115	345
BRAM	1	3
Power consumption		
Dynamic (mW)	20	56
Static leakage (mW)	894	895
Total (mW)	914	951
Timing		
Max Clock (MHz)	282	261

Timing analysis was done using Xilinx ISE tool. The maximum clock frequency of the TMR version of the error recovery mechanism is 8% lower than the clock frequency of the original version. The decrease of the maximum clock frequency is the result of a slightly longer critical path. The frequency 261 MHz is still more than enough since the ICAP circuit which is used by the mechanism is recommended to run below 100 MHz.

Error-recovery time

The error-recovery time of the mechanism depends on the size of the configuration memory of particular FPGA device. One configuration frame is checked in 41 clock cycles and recovered in 210 clock cycles. In our case the Virtex 5 (XC5VLX30) FPGA was used. This device has 5515 configuration frames. The worst case error detection time is 226115 clocks or with 100 MHz clock rate 2.3 ms.

Verification of ERM

The operation of error-recovery mechanism was verified by injecting faults into tested user applications and checking if the ERM recovered the errors. The fault injection was performed by our fault injection tool [26].

Two user applications were used. The first device under test was an Advanced Encryption Standard (AES) implementation from [27]. The AES core occupies 537 LUTs, 165 Flip Flops and 3 internal RAM blocks. 337184 single faults were injected in the part of FPGA where the AES was placed. The ERM recovered all the injected faults. The second device under test was a hardware implementation of a secure IEEE 1148.1 standard from [28]. The boundary scan core occupies 65 LUTs and 119 Flip Flops. 181056 single faults were injected in this device and all the injected faults were recovered by the ERM.

6. Conclusions

An error-recovery mechanism for SRAM-based FPGAs was proposed. The guidelines for its implementation in different FPGA families are given including the implementation in triple-modular redundancy. The mechanism was verified on Xilinx Virtex 5 FPGA using two case study applications.

Future work includes a detailed analysis of TMR structure of the ERM. By performing a fault injection experiment possible points of failure will be identified and further hardening solutions will be proposed.

References

1. Lima Kastensmidt, F.; Carro, L.; Reis, R. *Fault-Tolerance Techniques for SRAM-Based FPGAs* (Springer, Dordrecht, 2006).
2. Schrimpf, R. D.; Fleetwood, D. M. *Radiation Effects And Soft Errors In Integrated Circuits and Electronic Devices* (World Scientific, London, 2004).
3. Messenger, G. C. Collection of charge on junction nodes from ion tracks. *IEEE Trans. On Nuclear Science* 29, 2024 (1982).
4. Rebaudengo, M.; Sonza Reorda, M.; Violante, M. A new functional fault model for FPGA Application-Oriented testing. In: *Proceedings of Defect and Fault Tolerance in VLSI Systems*. 372–380 (2002).
5. Al-Asaad, H.; Shringi, M. On-line built-in self-test for operational faults. In: *Proceedings of IEEE AUTOTESTCON*. 28–32 (2000).
6. Yang, F.; Chakravarty, S.; Devta-Prasanna, N.; Reddy, S. M.; Pomeranz, S. M. R. An Enhanced Logic BIST Architecture for Online Testing. In: *Proceedings of 14th IEEE Int. On-Line Testing Symp-IOLTS*. 10–15 (2008).
7. Paschalis, A.; Gizopoulos, D. Effective software-based self-test strategies for on-line periodic testing of embedded processors. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 24, 88 (2005).
8. Nicolaidis, M.; Zorian, Y., On-Line Testing for VLSI-A Compendium of Approaches. *Journal of Electronic Testing* 12, 7 (1998).
9. Carter, W. C.; Schneider, P. R. Design of dynamically checked computers. In: *Proceedings of 4th IFIP Congress*. 878–883 (1968).
10. Violante, M.; Meinhardt, C.; Sonza Reorda, M.; Reis, R. A Low-Cost Solution for Deploying Processor Cores in Harsh Environments. *IEEE Transactions on Industrial Electronics* 58, 2617 (2011).
11. Verdel, T.; Makris, Y. Duplication-based concurrent error detection in asynchronous circuits: shortcomings and remedies. In: *Proceedings of 17th IEEE Int. Symp. Defect and Fault Tolerance in VLSI Systems-DFT*. 345–353 (2002).
12. Drineas, P. and Makris, Y. SPaRe: selective partial replication for concurrent fault-detection in FSMs. *IEEE Transactions on Instrumentation and Measurement* 52, 818733 (2003).
13. Hamming, R. W. Error detecting and correcting codes. *Bell System Technical Journal* 29, 147 (1950).
14. Peterson, W. *Error-correcting codes* (The Mit Press, Cambridge, 1980).
15. Von Neumann, J. Probabilistic logics and synthesis of reliable organisms from unreliable components. In: *Automata Studies*. 43–98 (NJ: Princeton Univ. Press, New York, 1956).
16. Pratt, B. et al., Fine-Grain SEU Mitigation for FPGAs Using Partial TMR, *IEEE Transactions on Nuclear Science* 55, 2274 (2008).
17. Lima Kastensmidt, F.; Sterpone, L.; Sonza Reorda, M.; Carro, L. On the Optimal De-sign of Triple Modular Redundancy Logic for SRAM-Based FPGAs. In: *IEEE Proc. Design, Automation and Test in Europe Conference*. 1290–1295 (2005).
18. Sterpone, L.; Violante, M. A New Algorithm for the Analysis of the MCUs Sensitiveness of TMR Architectures in SRAM-Based FPGAs. *IEEE Transactions on Nuclear Science* 55, 2019 (2008).
19. Carmichael, C. Triple Module Redundancy Design Techniques for Virtex® Series FPGA. *Xilinx Application manual XAPP 197* (2000).
20. Heiner, J.; Collins, N.; Wirthlin, M. Fault Tolerant ICAP Controller for High-Reliable Internal Scrubbing. In: *IEEE Aerospace Conf*. 1–10 (2008).
21. Chapman, K. SEU strategies for Virtex-5 Devices. *Xilinx Application manual XAPP864* (2010).
22. Asadi, H.; Tahoori, M. B. Soft error mitigation for SRAM-based FPGAs. In: *23rd IEEE VLSI Test Symp*. 207–212 (2005).
23. Hulme, C. A.; Loomis, H. H.; Ross, A.; Rong Yuan, A. Configurable fault-tolerant processor (CFTP) for spacecraft onboard processing. In: *Proc. IEEE Aerospace Conf*. 2269–2276 (2004).
24. Berg M. et al. Effectiveness of Internal Versus External SEU Scrubbing Mitigation Strategies in a Xilinx FPGA: Design, Test, and Analysis. *IEEE Transactions on Nuclear Science* 55, 2259 (2008).
25. Legat, U.; Biasizzo, A.; Novak, F. Self-reparable system on FPGA for single event upset recovery. In: *Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC)*. 1–6 (2011).
26. Legat, U.; Biasizzo, A.; Novak, F. Automated SEU fault emulation using partial FPGA reconfiguration. *Design and Diagnostics of Electronic Circuits and Systems (DDECS)*. 24–27 (2010).
27. Legat, U.; Biasizzo, A.; Novak, F. A compact AES core with on-line error-detection for FPGA applications with modest hardware resources. *Microprocessors & Microsystems* 35, 405 (2011).
28. Novak, F.; Biasizzo, A. Security Extension for IEEE Std 1149.1. *Journal of Electronic Testing* 22, 301 (2006).

Arrived: 16. 08. 2012

Accepted: 23. 09. 2012

Towards Smaller Populations in Differential Evolution

Iztok Fajfar, Tadej Tuma, Janez Puhon, Jernej Olenšek, and Árpád Bűrmen

Faculty of Electrical engineering, University of Ljubljana, Ljubljana, Slovenia

Abstract: Differential evolution is a simple algorithm for global optimization. Basically it consists of three operations: mutation, crossover and selection. Despite many research papers dealing with the first two operations, hardly any attention has been paid to selection nor is there a place for this operation in the algorithm basic naming scheme. In the paper we show that employing certain selection strategies combined with some random perturbation of population vectors notably improves performance in high-dimensional problems. Further analysis of results shows that the improvement is statistically significant. The application of the approach on a real-world case of a simple operating amplifier circuit exhibits a similar behaviour and improvement as observed with the Quartic noisy test function. Due to the nature of the circuit objective function this was expected.

Key words: global optimization, direct search methods, differential evolution, heuristic, parallelization

K majšim populacijam v diferencialni evoluciji

Povzetek: Diferencialna evolucija je preprost algoritem za globalno optimizacijo. Algoritem v osnovi sestavljajo tri operacije: mutacija, križanje in izbor. Čeprav obstaja množica znanstvenih prispevkov, ki obravnava prvi dve operaciji, je tretji operaciji namenjeno komaj kaj pozornosti, niti ni zanjo namenjenega mesta v izvornem načinu poimenovanja različic postopka. V prispevku pokažemo, da lahko z uporabo različnih postopkov izbora, ki jih kombiniramo z naključno perturbacijo populacijskih vektorjev, opazno izboljšamo delovanje postopka na večrazsežnostnih problemih. S podrobnejšo analizo rezultatov pokažemo, da so izboljšave statistično pomembne. S preizkusom postopka na resničnem primeru preprostega operacijskega ojačevalnika ugotovimo, da se algoritem vede podobno kot na preizkusni funkciji četrtega reda s superponiranim šumom. Glede na naravo kriterijske funkcije vezja smo to pričakovali.

Ključne besede: globalna optimizacija, direktni iskalni postopki, diferencialna evolucija, heuristični postopki, paralelizacija

* Corresponding Author's e-mail: iztok.fajfar@fe.uni-lj.si

1. Introduction

Differential Evolution (DE) is a simple yet powerful algorithm for global real parameter optimization proposed by Storn and Price [1]. Through the last decade, the algorithm has gained on popularity among research as well as engineering circles due to its extreme implementation simplicity and good convergence properties. The DE algorithm belongs to a broader class of Evolutionary Algorithms (EA), whose behavior mimics that of the biological processes of genetic inheritance and survival of the fittest. One outstanding advantage of EAs over other sorts of numerical optimization methods is that the objective function needs to be neither differentiable nor continuous, which makes them more flexible for a wide variety of problems.

A DE starts out with a generation of NP randomly generated D -dimensional parameter vectors. New parameter vectors are then generated by adding a weighted

difference of two population vectors to a third vector. This operation is called mutation. One then mixes the mutated vector parameters with the parameters of another vector, called the target vector, to obtain the so-called trial vector. The operation of parameter mixing is usually called crossover in the EA community. Finally, the trial vector is compared to the target vector, and if it yields a better solution, it replaces the target vector. This last operation is referred to as selection. In each generation, each population vector is selected once as the target vector.

There exist several variants of the DE algorithm [2, 3, 4, 5, 9], of which the most commonly used is *DE/rand/1/bin* which we explore in this paper. Before using the algorithm, one has to decide upon the values of three parameters affecting the behavior of a DE. The first is the population size NP , the other two are control parameters – a scaling factor F , and a crossover rate CR . Choosing the values of these parameters is usually

a problem-dependent task requiring a certain user expertise. Researchers have attempted to tackle the problem using several adapting and self-adapting strategies to govern the values of the control parameters F and CR [6, 7, 8, 9 and the references within] and even the population size NP [10, 11, 12, 13, 14]. Others have proposed and studied different mutation and crossover strategies [15, 16, 17, 18]. No explicit research work has been done so far on the third of the DE operators, the selection, neither is there any intended place in the algorithm variant naming scheme (i.e. DE/x/y/z) for this operator. In this paper we investigate how different selection schemes affect the behavior of the DE algorithm, in particular its ability to escape the local minima or stagnation. In addition to that we applied what would in genetic algorithm be called mutation, i.e. we randomly changed the population vector parameters with a fixed probability. Since the term mutation is already reserved in DE, we named this operation a random perturbation.

In the next section, we shortly describe the functioning of the basic DE algorithm, and in Section 3 we propose a random vector perturbation and different selection algorithms that we investigate. Finally, we present some results of optimizing test functions and a real electronic circuit in Sections 4 and 5, respectively.

2. Differential Evolution Overview

Consider the objective (criterion) or *fitness* function $f: \mathbb{R}^n \rightarrow \mathbb{R}$, where one has to find a minimum $\mathbf{a} \in \mathbb{R}^n$ so that $\forall \mathbf{b} \in \mathbb{R}^n : f(\mathbf{a}) \leq f(\mathbf{b})$. In this case \mathbf{a} is called a global minimum. It is rarely possible to find an exact global minimum in real problems, so for practical reasons one must accept a candidate with a reasonable good solution.

In order to search for a global minimum, differential evolution utilizes NP D -dimensional parameter vectors $\mathbf{x}_{i,G}$, $i=1,2,\dots, NP$ as a population in generation G . NP does not change from generation to generation. The initial population is chosen randomly and – if no prior information about the fitness function is known – it should cover the entire search space uniformly.

During the optimization process, the new parameter vectors are generated by adding a weighted difference of two randomly chosen population vectors to a third vector: $\mathbf{v}_{i,G+1} = \mathbf{x}_{r_1,G} + F \cdot (\mathbf{x}_{r_2,G} - \mathbf{x}_{r_3,G})$ with integer, mutually different, random indices $r_1, r_2, r_3 \in \{1, 2, \dots, NP\}$, which must all be different from i as well, and a real constant factor $F \in [0, 2]$. This operation is called *mutation* and the thus obtained vector the *mutated* vector.

The mutated vector parameters are then mixed with another vector, the so-called *target* vector, in order to produce a *trial* vector $\mathbf{u}_{i,G+1} = (u_{1,G+1}, u_{2,G+1}, \dots, u_{D,G+1})$ where

$$u_{j,i,G+1} = \begin{cases} v_{j,i,G+1} & \text{if } (\text{randb}(j) \leq CR) \text{ or } j = \text{rnbr}(i) \\ x_{j,i,G} & \text{if } (\text{randb}(j) > CR) \text{ and } j \neq \text{rnbr}(i) \end{cases} \quad j = 1, 2, \dots, D. \quad (1)$$

Here, $\text{randb}(j) \in [0, 1]$ is the j th execution of the uniform random generator, $CR \in [0, 1]$ is user-determined constant, and $\text{rnbr}(i) \in \{1, 2, \dots, D\}$ is a random index. The latter insures that the trial vector gets at least one parameter from the mutated vector. This operation of parameter mixing is usually called *crossover* in evolutionary search community.

Finally, a *selection* is performed in order to decide whether or not the trial vector should become a member of generation $G+1$. The value of the fitness function at the trial vector $\mathbf{u}_{i,G+1}$ is compared to its value at the target vector $\mathbf{x}_{i,G}$ using the greedy criterion. Only if the trial vector yields a better fitness value than the target vector, the target vector is replaced. Otherwise the trial vector is discarded and the target vector retained.

3. Random Perturbation and Different Selection Strategies

We focus our work on the stage of the DE algorithm after crossover, i.e. on the stage when the trial vector is already fully formed.

The idea for our modification came first from a simple observation that with a crossover rate CR approaching 1 not much of the target vector survives in its offspring (trial vector). In that sense one can argue that the search direction from the target to the trial vector can be as good (or as bad) as any other direction. The hypothesis we want to test is that there might exist some other (possibly better) candidate for replacement than the target vector itself.

In what follows, we propose and separately test three different rules for selecting the candidate to replace the trial vector. We select that candidate according to one of the three selection algorithms.

Algorithm 1: Replace the vector closest to the target vector.

```

Input: trial vector  $u_{i,G+1}$ , target vector  $x_{i,G}$  Gth generation of  $NP$  parameter vectors  $x_{n,G}$ ,  $n=1,2,\dots, NP$ 
 $c = -1$ 
 $d_{\min} = \infty$ 
for  $n = 1$  to  $NP$  do
    if  $f(u_{i,G+1}) < f(x_{n,G})$  and  $d(x_{i,G}, x_{n,G}) < d_{\min}$  then
         $c = n$ 
         $d_{\min} = d(x_{i,G}, x_{n,G})$ 
    endif
endfor
if  $c \neq -1$  then
     $x_{c,G}$  is replaced by  $u_{i,G+1}$ 
endif

```

The notation $d(\cdot, \cdot)$ in Algorithm 1 denotes an Euclidean distance. The algorithm replaces, of all the vectors that yield a worse fitness value than the trial vector, the one that is geometrically closest to the target vector. Notice that this strategy, the same as the original algorithm, always replaces the target vector as long as it is worse than the trial vector. Otherwise, it seeks after the candidate which is closest possible to the target vector to replace it. If no such vector is found, then the trial vector is discarded. As in the original algorithm, the target vectors with a relatively bad fitness value will be replaced more likely, while those with a better fitness value will survive. In addition to that, however, some near vector is moved to the place where the target vector would move if the target vector were not worse than the trial vector. This speeds up the clustering of the population members around the members with generally better fitness values. On one hand this can accelerate the convergence significantly, on the other hand, however, there is a danger of losing a necessary diversity too soon and thus not finding a global solution.

Algorithm 2: Replace the vector closest to the trial vector.

```

Input: trial vector  $u_{i,G+1}$ , Gth generation of  $NP$  parameter vectors  $x_{n,G}$ ,  $n=1,2,\dots, NP$ 
 $c = -1$ 
 $d_{\min} = \infty$ 
for  $n = 1$  to  $NP$  do
    if  $f(u_{i,G+1}) < f(x_{n,G})$  and  $d(u_{i,G+1}, x_{n,G}) < d_{\min}$  then
         $c = n$ 
         $d_{\min} = d(u_{i,G+1}, x_{n,G})$ 
    endif
endfor
if  $c \neq -1$  then
     $x_{c,G}$  is replaced by  $u_{i,G+1}$ 
endif

```

The approach with Algorithm 2 is quite different in that it searches for the candidate that is geometrically closest to the trial vector instead of the target vector. In that sense replacements are made that favor smaller jumps and encourage searching over less promising areas as well.

Algorithm 3: Replace either the target vector or the first one of the first half of the population that is worse than the trial vector.

```

Input: trial vector  $u_{i,G+1}$ , target vector  $x_{i,G}$  Gth generation of  $NP$  parameter vectors  $x_{n,G}$ ,  $n=1,2,\dots, NP$ 
if  $f(u_{i,G+1}) < f(x_{i,G})$  then
     $c = i$ 
else
     $c = -1$ 
    for  $n = 1$  to  $NP/2$  do
        if  $f(u_{i,G+1}) < f(x_{n,G})$  then
             $c = n$ 
            exit_for_loop
        endif
    endfor
endif
if  $c \neq -1$  then
     $x_{c,G}$  is replaced by  $u_{i,G+1}$ 
endif

```

The construction of Algorithm 3 is not so obvious at the first glance. Similarly to the original algorithm and Algorithm 1, one first checks whether the target vector is to be replaced, i.e. if the trial vector yields a better fitness value than the target vector. Otherwise we replace the first member of the first half of the population whose fitness value is worse than that of the trial vector. The idea behind that is to have one half of the population evolve under the original DE rules while accelerating the other half with further replacements. Even these additional replacements are applied asymmetrically with the members with a smaller index affected more often. That way we wanted to induce as little a change to the original method as possible, while inducing a relatively strong drag on a limited number of population members. The 1:1 ratio between both parts of the population was chosen arbitrarily. It should be noted that more frequent replacements lead towards a faster loss of diversity in population, which in turn lessens a chance to find the global minimum, and we wanted to find the equilibrium between two usually conflicting goals, namely fast convergence and high probability of finding the global optimum. The randomization introduced in the remainder of this section is supposed to make up for the before mentioned loss of diversity and in the same time indirectly to fine tune the ratio between two parts of the population.

Before going into experiments, let us introduce one more tiny though important modification to the algorithm. It is interesting to notice that although the algorithm itself belongs to a class of metaheuristics and stochastic optimization, the randomness in the original concept is only used for the selection of the vectors from which the mutated vector will be formed and for mixing the mutated and target vector parameters. The vector parameters themselves are changing randomly only indirectly through the mutation and crossover, and the obtained values are limited to a set of linear combinations of parameters already contained in a population. Some authors have already introduced some more randomness into DE, either directly by randomization of the vector parameters [19, 20] or indirectly by randomizing the algorithm control parameters F and CR [14, 21, 22], thus increasing the explorational potential of the algorithm, and even making it possible to prove the convergence [20].

In our study we decided simply to mutate every single parameter of the trial vector with a fixed probability just before the selection procedure takes place:

$$u_{ji,G+1} = \begin{cases} rand(j), & \text{if}(randb(j) \leq 0.005) \\ u_{ji,G+1}, & \text{otherwise} \end{cases}, j = 1, 2, \dots, D, \quad (2)$$

where $rand(j)$ is the call of the random generator that returns the uniformly distributed values along the entire j th axis of the parameter space. The constant probability of 0.005 was obtained empirically by a few preliminary test runs of the algorithm, which also indicated that the uniform distribution over the whole parameter space yielded somewhat superior performance compared to a normal distribution around the current parameter value often used in literature. We call this operation *perturbation*.

4. Experiments on test functions

Overall Performance

In order to get an overall picture and the first impression of the impact of the three proposed selection strategies and random vector perturbations, we carried out a simple test. For testing purposes, fourteen standard benchmark functions from [23] were selected, thirteen high-dimensional ($D=30$) and one low-dimensional ($D=4$) function. Then we randomly selected the three parameters from the intervals $NP \in \{10, \dots, 100\}$, $F \in [0, 1]$, and $CR \in [0, 1]$, and initialized a random population of the NP parameter vectors lying within the boundaries given for the test function in question. Next we ex-

ecuted eight optimization runs of the 150,000 criterion function evaluations (CFEs) with the same parameter values and initial vector population, but each time applying either the original or one of the three proposed selection schemes, once without and once with a random perturbation. We repeated this 5,000 times for each test function, each time with different control parameter values and initial vector population. The results are summarized in Table 1.

Table 1: Comparison of different modifications of the algorithm with the original

Selection Method	Without Perturbation		With Perturbation	
	50,000 CFEs	150,000 CFEs	50,000 CFEs	150,000 CFEs
Original	–	–	44.1/51.7	43.7/44.1
Algorithm 1	53.5/43.4	45.1/48.0	69.9/26.9	63.1/29.0
Algorithm 2	52.8/44.1	45.7/47.4	62.4/34.4	57.3/35.4
Algorithm 3	61.4/34.6	53.0/37.1	75.2/20.6	68.5/20.5

The fourteen pairs of the numbers in the table stand for the seven different comparisons (each of the modifications separately compared to the original) at two different times of the algorithm run: after 50,000 CFEs and after 150,000 CFEs. The numerator represents the percentage of cases in which the corresponding modification yielded a better fitness value (at the precision of 6 significant digits) than the original, while the denominator speaks of the percentage of cases in which the original method performed better. The sum is generally smaller than 100, because in some cases both variants gave the same result. The counting was carried out over all runs regardless of the control parameter setting or the selected test function. In real-life problems, often the practitioner has little or no knowledge about the fitness function and consequently about the best control parameter settings. Therefore, it seems that averaging over a range of different test functions and control parameter settings, selected in the Monte-Carlo manner, is an appropriate measure of the algorithm overall performance.

In the table, the pairs of the numbers in the white cells represent the state after 50,000 CFEs. We conjectured that at this optimization stage the convergence is generally not yet fully reached. Consequently, those pairs of the numbers indicate the convergence speed rather than the overall ability to find a global minimum.

The numbers in the shaded cells represent the state after 150,000 CFEs, when we assume that the number of the cases reaching the final solution is considerably larger than of those after 50,000 CFEs. Hence we con-

sider these results to reflect the ability of the algorithm to find a good final solution.

From the table one can infer some quite interesting observations. Replacing – instead of target vector – the candidate closest to target (Algorithm 1) or closest to trial vector (Algorithm 2) without using perturbation performed just slightly better after 50,000 CFEs (1st column, 2nd and 3rd row, respectively) and slightly worse after 150,000 CFEs (2nd column, 2nd and 3rd row, respectively). That implies that the more frequent replacements in both cases speed up the convergence as expected but, in general, they cause the algorithm more often to stuck in one of the local minima or to reach stagnation in the end. That is, however, not the case with the selection strategy using Algorithm 3. This strategy outperformed the original for almost twice more cases after 50,000 CFEs and still remained much better after 150,000 CFEs (4th row, 1st and 2nd column, respectively). It is important to note that with this kind of modification the algorithm still performs more replacements than the original one, which obviously speeds-up the convergence. The main difference here is that we perform these additional replacements only on a limited number of the population members, the others still undergoing the original selection scheme. Technically, we can speak of two different schemes running in parallel.

Comparing the original method with and without perturbations gives us no noticeable difference (1st row, 3rd and 4th column). As reasonably expected, random perturbations slow down convergence to some extent (1st row, 3rd column), but in the long run no variant outperforms the other (1st row, 4th column). It is quite interesting to notice that while perturbation seems to have no observable effect when applied to the original algorithm, it improves the other three variants noticeably. It seems that in these cases perturbation not only makes up for the loss of the population variance – which might have occurred due to a too fast convergence induced by more frequent replacements – but also improves the overall performance. It seems that the changed selection schemes and random perturbations support each other. Nevertheless, comparing the results of the selection algorithms 1, 2, and 3 with perturbation after 50,000 and 150,000 CFEs shows that in all the three cases, in the long run, the original method compensates a little for the much worse performance during the first part of the run. This leaves us, possibly, some room for improvement by balancing the factors that affect the convergence speed and the rate of change in the population diversity.

A Closer Look

Let us now focus a little closer on Algorithm 3 combined with vector perturbation exhibiting the best overall improvement in the previous analysis. In order to get a more accurate picture, we made the same comparisons as before, only this time for each test function separately. The results are summarized in Table 2. The table shows comparisons of the original method with the original method with perturbation, and with Algorithm 3 with and without perturbation. The numbers in normal writing represent the state after 50,000 CFEs, while the ones in boldface the state after 150,000 CFEs.

Table 2: Comparison of different modifications by separate test functions

Test Function	Modification Compared to the Original Algorithm		
	Original with Perturbation	Algorithm 3	Algorithm 3 with Perturbation
f_1 (Quadratic)	34.72/65.28 31.60/68.40	70.83/29.17 68.75/31.25	80.21/19.79 76.39/23.61
f_2 (Schwefel 2.22)	33.45/66.55 31.71/68.29	70.73/29.27 66.90/33.10	74.22/25.78 70.03/29.97
f_3 (Schwefel 1.2)	51.04/48.26 54.51/45.49	75.35/23.96 70.49/29.51	77.08/22.57 78.47/21.53
f_4 (Schwefel 2.21)	49.48/48.08 48.43/49.83	63.07/34.49 59.58/39.72	83.97/12.80 79.79/18.82
f_5 (Generalized Rosenbrock)	49.83/50.17 52.96/47.04	58.19/41.81 56.10/43.90	77.00/23.00 73.87/26.13
f_6 (Step)	31.36/24.39 29.97/9.76	31.36/27.87 18.12/26.48	47.04/6.62 35.19/3.48
f_7 (Quartic noisy)	46.50/53.50 49.30/50.70	70.28/29.72 67.83/32.17	77.97/22.03 77.62/22.38
f_8 (Generalized Schwefel 2.26)	57.14/42.86 58.54/29.62	49.83/50.17 36.59/58.19	82.58/17.42 78.75/11.15
f_9 (Generalized Rastrigin)	50.69/48.96 49.65/43.40	66.67/33.33 57.64/39.24	80.90/19.10 79.17/15.28
f_{10} (Ackley)	48.26/50.69 48.96/33.33	60.07/39.24 43.75/41.67	81.60/17.36 68.40/15.63
f_{11} (Generalized Griewank)	32.17/61.19 31.47/36.71	63.99/29.72 42.31/29.02	73.08/20.28 53.50/17.83
f_{12} (Generalized penalty function 1)	43.36/56.29 36.01/45.80	68.53/31.12 52.45/33.22	81.47/18.53 65.38/20.63
f_{13} (Generalized penalty function 2)	45.10/54.90 42.66/43.01	62.59/37.06 50.35/37.06	82.17/17.48 72.03/15.03
f_{13} (Kowalik)	44.41/52.45 45.80/46.50	48.25/47.55 50.70/45.10	52.80/45.80 49.65/45.80

The first and foremost important observation here is that the modification combined with perturbation shows noticeably and consistently better performance

in all cases except for the Kowalik test function where there is no observable difference. Again we see that perturbation alone does not really improve performance of the original method, two notable exceptions being the Schwefel 2.26 and Step functions.

The Schwefel function is somehow tricky in that the global minimum is placed geometrically remote from the next few best local minima. The original method exhibits quite a good convergence at the beginning, while later on perturbations help find the global minimum as without them the original method would be stuck in a local minimum (see the 1st column, Schwefel 2.26 function). Interestingly enough, modification without perturbation in that case performs much worse than the original method. This probably stems from the fact that this method replaces candidates of one half of the population excessively, thus additionally forcing the population in one of the local minima. The modified method with perturbation, however, performs much better in this case.

The same goes for the step function. This function, too, poses some difficulties for the original algorithm because it consists of many plateaus and discontinuities. All points within a small neighborhood will have the same fitness value, making it very difficult for the process to move from one plateau to another. Perturbations seem to help here significantly.

Up to now we were only interested in the number of cases in which one method is better than the other. What about the fitness values they actually produce? In Table 3 one finds the best fitness values averaged over all runs, comparing the original algorithm with the one using Algorithm 3 with perturbations. Notice that the values are quite large. One must not forget that these values were obtained by running the optimization using completely random optimization parameters. So many of the parameter values were used that were not even close to the recommendations in the literature. But as we are interested only in the differences between different algorithm variants, this is not an issue.

In the first and second column of Table 3 one finds the average minimums for each of the two variants, while in the last column there are the results of paired two-sampled two-tailed t-test of comparing the modified approach with the original.

Table 3: Comparison of the average best fitness obtained by the original algorithm and Algorithm 3 with perturbation

Test Function	Original (Average Best Fitness)	Algorithm 3 with Perturbation (Average Best Fitness)	T-Test Values	Analytical (actual) best fitness
f_1 (Quadratic)	1.694659×10^3	2.338428×10^2	$p < 0.01$ $t = 5.09$	0
f_2 (Schwefel 2.22)	6.908752	2.819474	$p < 0.01$ $t = 5.47$	0
f_3 (Schwefel 1.2)	1.429065×10^4	8.331654×10^3	$p < 0.01$ $t = 13.95$	0
f_4 (Schwefel 2.21)	17.24446	7.910773	$p < 0.01$ $t = 10.69$	0
f_5 (Generalized Rosenbrock)	2.407282×10^6	2.566153×10^5	$p < 0.01$ $t = 3.17$	0
f_6 (Step)	1.315575×10^3	2.352474×10^2	$p < 0.01$ $t = 4.11$	0
f_7 (Quartic noisy)	1.747322	0.1379149	$p < 0.01$ $t = 4.40$	0
f_8 (Generalized Schwefel 2.26)	-1.069594×10^4	-1.167699×10^4	$p < 0.01$ $t = 10.75$	-12569.5
f_9 (Generalized Rastrigin)	71.73974	49.26490	$p < 0.01$ $t = 11.05$	0
f_{10} (Ackley)	6.395496	2.192476	$p < 0.01$ $t = 10.63$	0
f_{11} (Generalized Griewank)	10.83875	1.257148	$p < 0.01$ $t = 4.22$	0
f_{12} (Generalized penalty function 1)	4.372791×10^6	7.482104×10^5	$p = 0.02$ $t = 2.27$	0
f_{13} (Generalized penalty function 2)	9.736573×10^6	1.050585×10^6	$p < 0.01$ $t = 2.786$	0
f_{15} (Kowalik)	1.358227×10^{-3}	1.836926×10^{-3}	$p = 0.11$ $t = -1.61$	0.0003075

The test further confirms our speculations about the modification bringing significant advantages over the original DE. In twelve out of the fourteen test functions the modification performs significantly better at a 99% significance level. Again, an exception is the Kowalik function where the test actually indicates a degradation of performance (observe the negative t-value), although not a significant one.

Parameter Impact

In our experiments so far we didn't pay any attention to the actual control-parameter or population-size selection. The values were picked up completely randomly

within the set intervals. In this section we want to investigate the effect of different parameter settings on the algorithm performance with the proposed modifications. We compare the original algorithm to the one using Algorithm 3 with perturbation. In this paper we summarize the results only for the case of Generalized Schwefel 2.26 function. It should be noted, however, that we observed a similar behavior elsewhere as well [28].

We started out by choosing the control parameter settings most commonly found in literature, i.e. $F = 0.5$ and $CR = 0.9$. Our experimenting showed that at these values the best fitness (assuming a fixed number of 150,000 CFEs) is generally obtained at the population size $NP = 40$. The results in this section are obtained by changing one of the three values while keeping the other two fixed. The best fitness values were averaged over 25 independent runs.

Figure 1 shows that the original method completely failed to reach the global minimum in the Schwefel 2.26 function (at -12569.5) safe for the lowest values of CR . Interesting, however, is that the modification enables DE to find the global minimum at lower and higher values of CR , but not at the values around 0.7. A similar behavior can be observed in other functions as well [28], where the modification brings an improvement at the smaller and bigger values of CR .

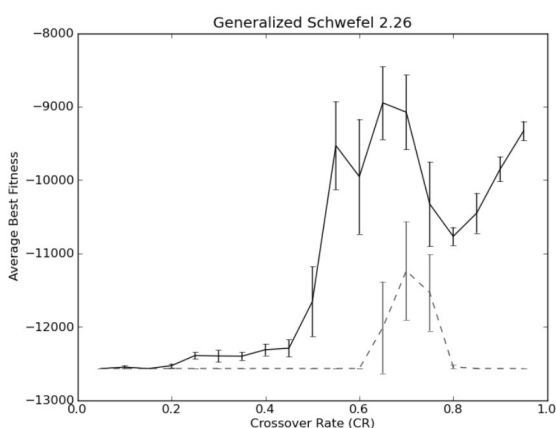


Figure 1: Impact of the crossover rate (CR) on the algorithm performance. The solid (black) line shows the best fitness values averaged over 25 runs, as obtained by the original DE. The dashed (red) line shows the results produced by DE with Algorithm 3 and perturbation. The graph shows a situation at the fixed $F=0.5$ and $NP=40$.

Figure 2 shows the results for the same test function using constant $CR=0.9$ and $NP=40$, while changing F from 0.05 to 0.95. The general pattern that is to be

observed is somewhat different from the observations with the changing parameter CR . We observe the major improvement at the smaller F values. It has been mentioned in the literature that F must not be too small in order to be able to find a minimum [25]. A small F means a small difference vector and hence a small displacement of a mutated vector. It seems that too big a displacement is not good for the convergence either. An interesting observation is that our modification improves the results more at the end of smaller F values, and often to the extent that outperforms the original algorithm at any other F value. It seems that small displacements – which seem to produce a slow but stable convergence – go hand in hand with the anticipated speed up caused by our modification, together producing a more stable and faster convergence.

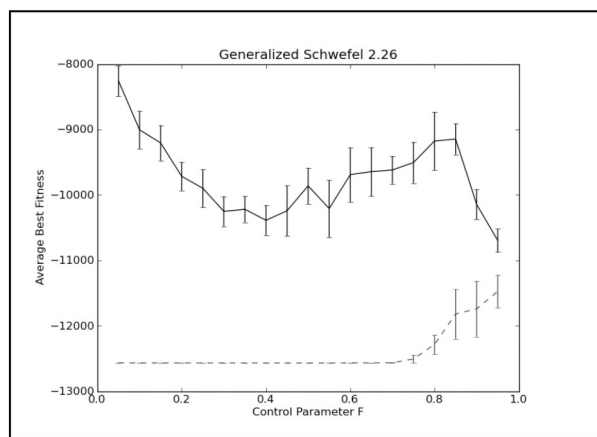


Figure 2: Impact of the control parameter F in the Generalized Schwefel 2.26 function. The graph shows a situation at the fixed $CR=0.9$ and $NP=40$.

In Figure 3, which depicts the impact of the population size, we can see that the major improvement is achieved at lower population sizes. This effect is especially evident in case of Schwefel 2.26 function when the minimum is reached with our modification but not with the original method.

The large population size in DE usually guarantees a larger probability of finding the global minimum and, originally, the proposed population size was $NP = 10D$ [24]. Other sizes were proposed later but were all considerably greater than the fitness function dimensionality D . As clearly seen from Figure 3 and the graphs in [28], at larger population sizes our modification does not bring any improvement over the original method whatsoever. That is somehow expected since the DE should be quite stable at larger NP . The problem however is that the stability is of no great practical use if after a relatively large number of CFEs the algorithm is still very far from the actual solution. We see one of the

strongest values of our modification in having instead of one large population many smaller ones running in parallel which could bring together the ability to actually find the global minimum and speed up of convergence.

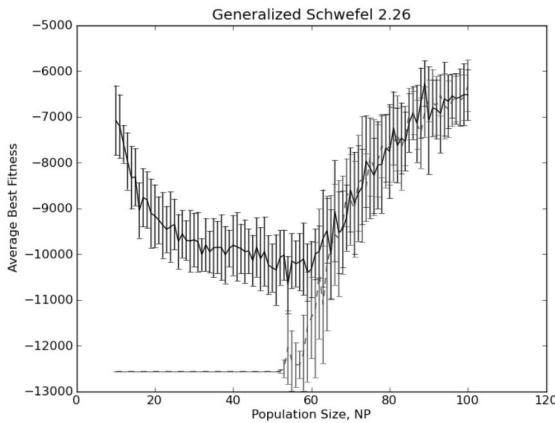


Figure 3: Impact of the population size in the Generalized Schwefel 2.26 function. The graph shows a situation at the fixed $CR=0.9$ and $F=0.5$.

5. Test runs on a simple operating amplifier circuit

The Circuit

After successfully testing the proposed algorithm on standard benchmark functions, we wanted to see

whether the method behaved in the same fashion on a real circuit as well. As an example we look at a simple two-stage operating amplifier, whose circuit diagram is shown in Fig 4. The amplifier is designed in a $0.18\ \mu\text{m}$ CMOS process with $1.8\ \text{V}$ supply voltage.

The operating point of the amplifier is determined by the input bias current flowing into the drain terminal of $Xmn1b$. $Xmn1$ and $Xmn4$ mirror this current to set the bias of the differential pair ($Xmn2$ and $Xmn3$) and output amplifier ($Xmp3$). Transistors $Xmp1$ and $Xmp2$ act as active load to the differential pair. Frequency compensation is introduced by R_{out} and C_{out} . Ports inp , inn , and out represent the noninverting input, inverting input, and output of the amplifier, respectively. Transistors $Xmn1s$ and $Xmp1s$ power down the amplifier when signals slp ($slpx$) are pulled high (low).

The testbench circuit shown in Fig 5 provides supply voltage (V_{dd}) to the amplifier along with a $100\ \mu\text{A}$ bias current. Feedback is introduced by resistors R_{fb} and R_{in} . R_{load} and C_{load} represent the load resistance and capacitance. Because the supply voltage is single-ended, the input signal (V_{in}) requires a common mode bias ($V_{com}=V_{dd}/2$).

During the optimization we simulated the circuit across three corners: nominal (nominal PMOS and NMOS model, 25°C , $V_{dd}=1.8\ \text{V}$), worst power (fast NMOS and PMOS model, 100°C , $V_{dd}=2.0\ \text{V}$), and worst speed (slow NMOS and PMOS model, 0°C , $V_{dd}=1.8\ \text{V}$). In each of the corners we performed the following analyses: operating point, DC sweep of input voltage (from $-2\ \text{V}$ to $2\ \text{V}$), DC sweep of common mode bias (from $0.7\ \text{V}$ to V_{dd}

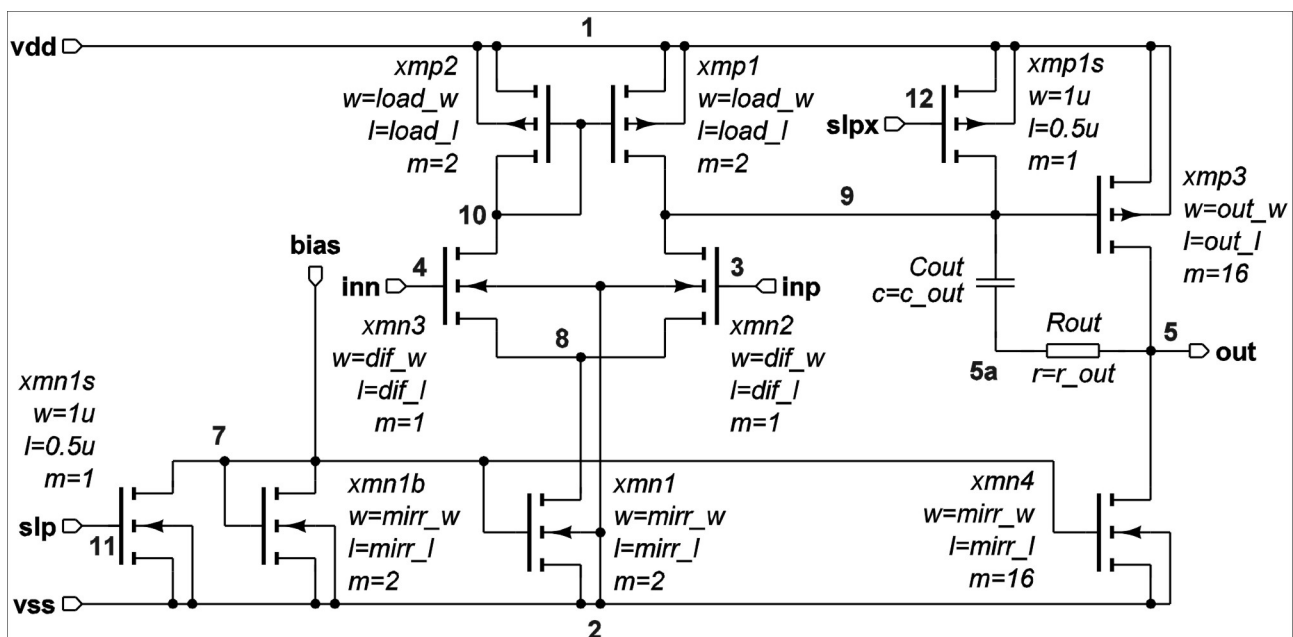


Figure 4: The circuit diagram of a simple two stage operating amplifier.

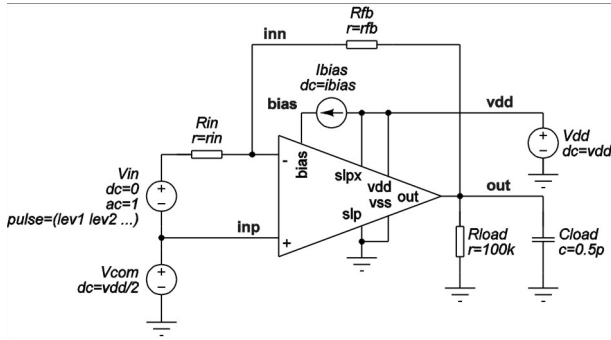


Figure 5: The testbench circuit for the operating amplifier from Fig 4.

– 0.1 V), small signal AC analysis, and transient analysis of the response to a ± 0.5 V step in input voltage. R_{fb} and R_{in} were both set to 1 M Ω , except in transient analysis where R_{in} was set to 100 k Ω .

From the obtained results of above analyses the following performance measures were derived:

- V_{gs} and V_{ds} overdrive voltage (i.e. $V_{gs} - V_t$ and $V_{ds} - V_{dsat}$) for all transistors, except Xmn1s and Xmp1s, at operating point and at all points analyzed in the DC sweep of common bias,
- output voltage swing where DC gain is above 50% of maximal gain,
- gain, unity-gain bandwidth (UGBW), and phase margin,
- overshoot, undershoot, 10% - 90% rise and fall time, 5% settling time, and slew rate of transient response,
- total gate area of all transistors (except Xmn1s and Xmp1s).

Next, from these performance measures, we constructed the cost function [26] consisting of the following requirements:

- overdrive voltage should be at least 1m V,
- output voltage swing must be greater than 1.6 V,
- gain, UGBW, and phase margin must lie above 75 dB, 60 MHz, and 60° , respectively,
- overshoot and undershoot must be below 10%, rise and fall time below 100 ns, settling time below 300 ns, and slew rate above 10 V/ μ s,
- total gate area should be less than 1500 μ m².

Thus constructed cost function was used for guiding the optimization algorithm which should find optimal adjustment of the 10 circuit parameters listed in Table 4.

Table 4: Definitions of the circuit parameters subject to optimization

Parameter	Description	Range	Unit
dif_w	channel width of Xmn2 and Xmn3	[1, 95]	μ m
dif_l	channel length of Xmn2 and Xmn3	[0.18, 4]	μ m
load_w	channel width of Xmp1 and Xmp2	[1, 95]	μ m
load_l	channel length of Xmp1 and Xmp2	[0.18, 4]	μ m
mirr_w	channel width of Xmn1b, Xmn1 and Xmn4	[1, 95]	μ m
mirr_l	channel length of Xmn1b, Xmn1 and Xmn4	[0.18, 4]	μ m
out_w	channel width of Xmp3	[1, 95]	μ m
out_l	channel length of Xmp3	[0.18, 4]	μ m
c_out	capacitance of C_{out}	[0.01, 10]	pF
r_out	resistance of R_{out}	[0.001, 200]	k Ω

Performance measures were evaluated in all corners, except for the V_{gs} and V_{ds} overdrive voltages, which were evaluated only in the nominal corner. The cost function was expressed as a sum of contributions

$$F = \sum_{i=1}^m f_i$$

where m is the number of performance measures. Every performance measure resulted in one contribution f_i , which was obtained by transforming its worst value observed across all corners ($y_i(\mathbf{x})$) using a piecewise-linear function $f(y_i(\mathbf{x}), g_i, n_i, p_i, c_i)$. Here g_i , n_i , p_i , and c_i denote the goal, the norm, the penalty factor, and the tradeoff factor, respectively. For requirements of the form $y_i(\mathbf{x}) \leq g_i$ the contribution was computed as

$$f_i = \begin{cases} \frac{p_i(y_i(\mathbf{x}) - g_i)}{n_i} & \text{if } y_i(\mathbf{x}) > g_i \text{ (i.e. a requirement is not fulfilled)} \\ f(y_i(\mathbf{x}), g_i, n_i, p_i, c_i) = \frac{t_i(y_i(\mathbf{x}) - g_i)}{n_i} & \text{if } y_i(\mathbf{x}) \leq g_i \text{ (i.e. a requirement is fulfilled)} \end{cases}$$

For requirements of the form $y_i(\mathbf{x}) \geq g_i$ the contribution was

$$f_i = \begin{cases} \frac{p_i(g_i - y_i(\mathbf{x}))}{n_i} & \text{if } y_i(\mathbf{x}) < g_i \text{ (i.e. a requirement is not fulfilled)} \\ f(y_i(\mathbf{x}), g_i, n_i, p_i, c_i) = \frac{t_i(g_i - y_i(\mathbf{x}))}{n_i} & \text{if } y_i(\mathbf{x}) \geq g_i \text{ (i.e. a requirement is fulfilled)} \end{cases}$$

The tradeoff factor for overdrive voltages was set to $t_i = 0$, because we are not interested in improving them beyond their respective goals. All other tradeoff factors were set to $t_i = 0.001$ and the penalty factors were set to $p_i = 1$. The norms were set to $g_i / 10$ for all performance measures, except for the area, where $n_i = 100 \mu$ m² was used.

Optimization Results

We ran the circuit optimization using the same DE parameters as with the test functions in the previous section. Simple circuits such as the one in question often exhibit unimodal objective function contaminated with numerical noise. Therefore we expected the results to be reminiscent of those obtained with the Quartic noisy test function [28].

During each optimization run we performed, as with test functions, 150,000 CFEs. We run the optimizations on 20 2.66 Ghz Core i5 (4 cores per machine) machines, and it took approximately 3 weeks to complete the computation. Unlike with most test functions, the study of the results showed us that already after 20,000 CFEs there were no observable changes neither in obtained average fitness values nor standard errors. From relatively flat lines with almost zero standard error at fitness value of 0.56 we conclude that the minimum actually lies at that value (cf. Figs 6 to 8).

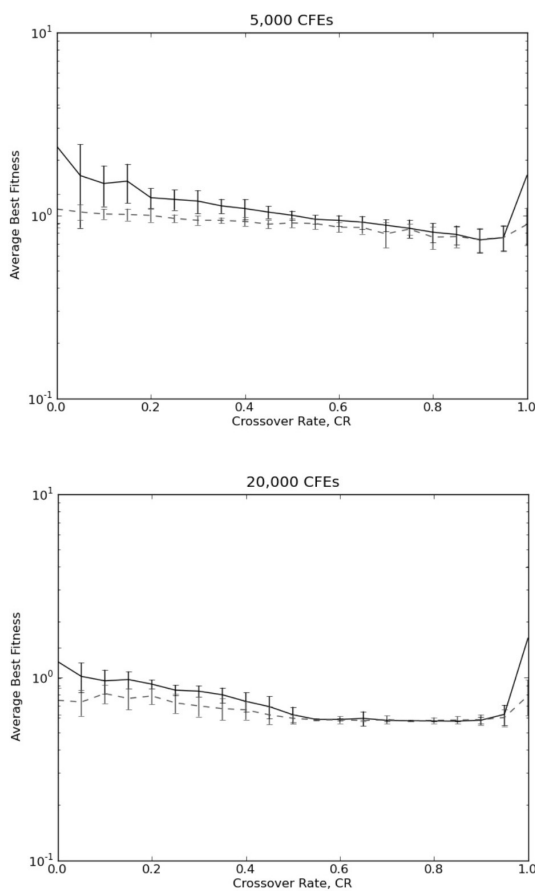


Figure 6: Impact of the crossover in optimizing the simple operating amplifier circuit, after 5,000 CFEs (left) and 20,000 CFEs (right). The graph shows a situation at the fixed $F=0.5$ and $NP=40$.

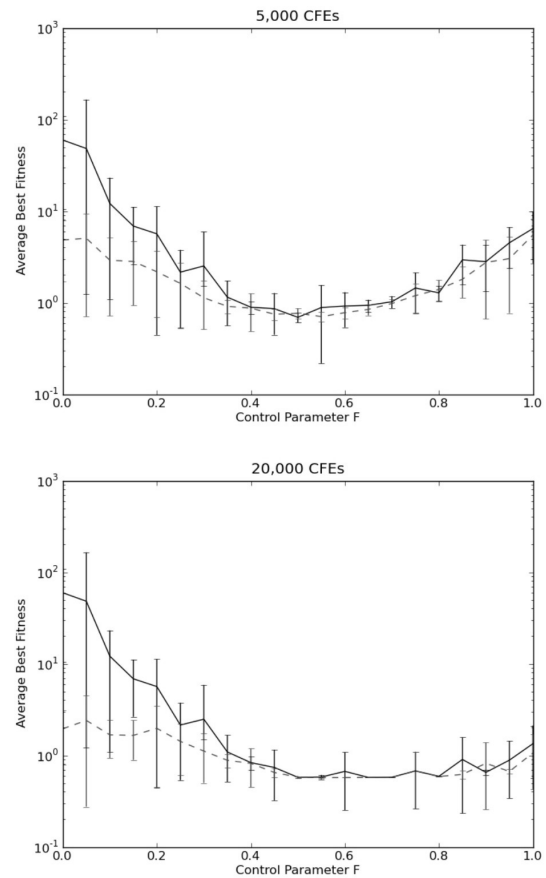


Figure 7: Impact of the control parameter F in optimizing the simple operating amplifier circuit, after 5,000 CFEs (left) and 20,000 CFEs (right). At the values of $F=0.2$ and below there was practically no change after 5,000 CFEs with the original algorithm, while some further improvement could be observed with Algorithm 3 with perturbation. The graph in this case is comparatively flat, showing lessened sensitivity to control parameter F . The graph shows a situation at the fixed $CR=0.9$ and $NP=40$.

Similarly to the results with Quartic noisy function, our modification does not improve the best results obtained with the original DE. The very important observation however, is the fact that it does not worsen the best results either, and the resulting fitness values are quite better at the control parameter values where the original DE did not perform very well. In that sense one can argue that applying Algorithm 3 with perturbation lessens the algorithm sensitivity to control parameter values. Although the differential evolution algorithm itself is surprisingly simple to implement there is still much bewilderment among scientists about setting the values of the control parameters. So any step towards parameter insensitiveness of the DE is welcome.

As seen in Fig 8, one still needs a relatively large population in order to stand a fair chance of finding the glo-

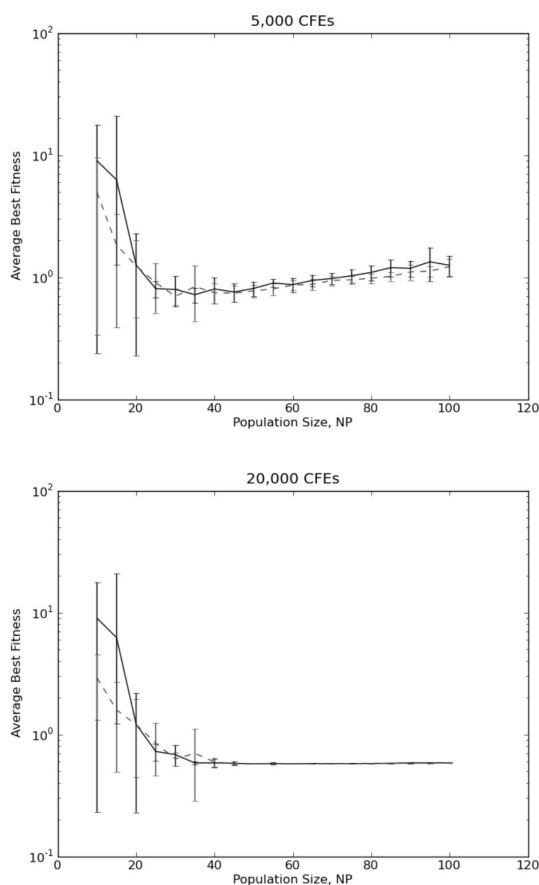


Figure 8: Impact of the population size in optimizing the simple operating amplifier circuit, after 5,000 CFEs (left) and 20,000 CFEs (right). At the smaller population sizes, the original algorithm was soon stuck (no change from 5,000 CFEs to 20,000 CFEs), while Algorithm 3 with perturbation still improved the outcome. The graph shows a situation at the fixed $CR=0.9$ and $F=0.5$.

bal minimum. It seems that innumerable local minima introduced by the intensive numerical noise could only be overcome with relatively large populations. At the same time we observe that our proposed modification quite improves results at small populations, i.e. $NP < 20$. Even though the improvement itself does not lead us to the global minimum at that small population sizes, it could be crucial for reducing the sizes of sub-populations in the multi-population model of parallel differential evolution [27 and the references within].

6. Conclusion

In the paper we studied different replacement schemes in the DE algorithm combined with additional random perturbation of vector parameters. By experimenting with a suite of standard test functions we observed that only one replacement scheme provided observ-

ably better results than the original algorithm. It was somehow surprising to note that perturbation did not improve behavior of the original replacement scheme while it improved all the others.

Studying the performance of Algorithm 3 combined with random perturbation showed a statistically significant improvement in all higher dimensional test functions. We also saw that the improvement is greater at certain values of the control parameters and population sizes, i.e. at lower values of F and NP , and at lower as well as higher values of CR .

Especially outstanding was the improvement in smaller population sizes. According to the outcomes of the experiments with both the Quartic noisy function and the real-world circuit we believe it is worthwhile to aim some research effort in the direction of DE parallelization using sub-populations of sizes below 20.

One of the advantages of the approach proposed in this paper is the fact that its intervention with the original method does not interfere with any other operation and can therefore be applied independently and combined with many other approaches proposed in literature.

All in all, the beauty of the original DE algorithm is its utmost implementation simplicity. Our research tried not to stray away from this simplicity and we showed that it is possible to improve the algorithm performance by only changing the rule for replacing the population members combined with simple random perturbation. We believe that further work in this direction is worthwhile.

Acknowledgement

This work has been supported by the Ministry of Education, Science, Culture and Sport of Republic of Slovenia within the research program P2-0246 – Algorithms and optimization methods in telecommunications.

References

1. R. Storn and K. Price, "Differential evolution – a simple and efficient heuristic for global optimization over continuous spaces," *J. Glob. Optim.*, vol. 11, pp. 341–359, 1997.
2. K. Price, "An introduction to differential evolution," in *New ideas in optimization*, D. Corne, M. Dorigo, and F. Glover, Eds. London (UK): McGraw-Hill Ltd., 1999, pp. 79–108.

3. D. Jiang, H. Wang, and Z. Wu, "A variant of differential evolution based on permutation regulation mechanism," in *International Symposium on Intelligence Computation and Applications (ISICA): 2010*, pp. 76–85.
4. E. Mezura-Montes, J. Velázquez-Reyes, and C. A. Coello Coello, "A comparative study of differential evolution variants for global optimization," in *Proceedings of the 8th Annual Conference on Genetic and Evolutionary Computation (GECCO): 2006*, vol. 1, pp. 485–492.
5. Y. Wang, Z. Cai, and Q. Zhang, "Differential Evolution With Composite Trial Vector Generation Strategies and Control Parameters," *IEEE Trans. Evol. Comput.*, vol. 15, pp. 55–66, 2011.
6. J. Brest, S. Greiner, B. Bošković and M. Mernik, "Self-adapting control parameters in differential evolution: a comparative study on numerical benchmark problems," *IEEE Trans. Evol. Comput.*, vol. 10, pp. 646–657, 2006.
7. J. Liu and J. Lampinen, "A fuzzy differential evolution algorithm," *Soft Comput.*, vol. 9, pp. 448–462, 2005.
8. D. Zaharie, "Control of population diversity and adaptation in differential evolution algorithms," in *Proceedings of 9th International Conference on Soft Computing*, R. Matoušek, P. Ošmera, Eds. Brno (Czech Republic): Mendel 2003, pp. 41–46.
9. J. Zhang and A. C. Sanderson, "JADE: Adaptive Differential Evolution With Optional External Archive," *IEEE Trans. Evol. Comput.*, vol. 13, pp. 945–958, 2009.
10. J. Brest and M. Sepesy Maučec, "Population size reduction for the differential evolution algorithm," *Appl. Intell.*, vol. 29, pp. 228–247, 2008.
11. J. Teo, "Exploring dynamic self-adaptive populations in differential evolution," *Soft Comput.*, vol. 10, pp. 673–686, 2006.
12. C. Zhang, J. Chen, B. Xin, T. Cai, and C. Chen, "Differential evolution with adaptive population size combining lifetime and extinction mechanisms," in *Proceedings of 8th Asian Control Conference (ASCC): 2011*, pp. 1221–1226.
13. H. Wang, S. Rahnamayan, and Z. Wu, "Adaptive differential evolution with variable population size for solving high-dimensional problems," in *Proceedings of the IEEE Congress on Evolutionary Computation (CEC): 2011*, pp. 2626–2632.
14. J. Brest and M. S. Maučec, "Self-adaptive differential evolution algorithm using population size reduction and three strategies," *Soft Comput.*, vol. 15, pp. 2157–2174, 2011.
15. H. Y. Fan and J. Lampinen, "A trigonometric mutation operation to differential evolution," *J. Glob. Optim.*, vol. 27, pp. 105–129, 2003.
16. S. Das, A. Abraham, U. K. Chakraborty, and A. Konar, "Differential evolution using a neighborhood-based mutation operator," *IEEE Trans. Evol. Comput.*, vol. 13, pp. 526–553, 2009.
17. D. Zaharie, "Influence of crossover on the behavior of differential evolution algorithms," *Appl. Soft Comput.*, vol. 9, pp. 1126–1138, 2009.
18. S. M. Islam, S. Das, S. Ghosh, S. Roy, and P. N. Suganthan, "An adaptive differential evolution algorithm with novel mutation and crossover strategies for global numerical optimization," *IEEE Trans. Syst., Man and Cybern. (SMC)*, part B, vol. 42, pp. 482–500, 2012.
19. Z. Yang, J. He, and X. Yao, "Making a difference to differential evolution," in *Advances in metaheuristics for hard optimization*, Z. Michalewicz and P. Siarry, Eds.: Springer, 2007, pp. 415–432.
20. J. Olenšek, Á. Bűrmen, J. Puhani, and T. Tuma, "DESA: a new hybrid global optimization method and its application to analog integrated circuit sizing," *J. Glob. Optim.*, vol. 44, pp. 53–77, 2009.
21. J. Brest, S. Greiner, B. Bošković, M. Mernik, and V. Žumer, "Self-adapting control parameters in differential evolution: a comparative study on numerical benchmark problems," *IEEE Trans. Evol. Comput.*, vol. 10, pp. 646–657, 2006.
22. S. Das, A. Konar, and U. K. Chakraborty, "Two improved differential evolution schemes for faster global search," in *Proceedings of GECCO*, Washington D.C.: 2005, pp. 991–998.
23. X. Yao, Y. Liu, and G. Lin, "Evolutionary programming made faster," *IEEE Trans. Evol. Comput.*, vol. 3, pp. 82–102, 1999.
24. R. Storn, "On the usage of differential evolution for function optimization," in *Biennial Conference of the North American Fuzzy Information Processing Society (NAFIPS)*, Berkeley: 1996, pp. 519–523.
25. R. Gämperle, S. D. Müller, and P. Koumoutsakos, "A parameter study for differential evolution," in *Proc. WSEAS NNA-FSFS-EC*, Interlaken, Switzerland: 2002, pp. 293–298.
26. A. Bűrmen, D. Strle, F. Bratkovič, J. Puhani, I. Fajfar, and T. Tuma, "Automated robust design and optimization of integrated circuits by means of penalty functions," *AEÜ Int. J. Electron. Commun.*, vol. 57, pp. 47–56, 2003.
27. W. Zhu, "Massively parallel differential evolution—pattern search optimization with graphics hardware acceleration: an investigation on bound constrained optimization problems," *J. Glob. Optim.*, vol. 50, pp. 417–437, 2011.
28. I. Fajfar, "Selection strategies and random perturbations in differential evolution," in *Proc. IEEE Congress on Evolutionary Computation*, Brisbane, Australia: 2012.

Arrived: 25. 07. 2012

Accepted: 09. 10. 2012

Microfabrication and characterization of microcombustor on (100) silicon /glass platform

D. Resnik^{1,2}, S. Hočevar^{3,4}, M. Možek^{1,2}, I. Stegel⁵, S. Amon^{1,2} and D. Vrtačnik^{1,2}

¹University of Ljubljana, Faculty of Electrical Engineering, Laboratory of Microsensor Structures and Electronics,

²Centre of Excellence Namaste, Jamova 39, Ljubljana 1000, Slovenia

³National Institute of Chemistry, Laboratory of Catalysis and Chemical Reaction Engineering, Hajdrihova 19, SI-1000 Ljubljana, Slovenia

⁴Centre of Excellence for Low Carbon Technologies (CoE LCT), Hajdrihova 19, SI-1000 Ljubljana, Slovenia

⁵Ministry of Defense of the Republic of Slovenia,

Abstract: Design, microfabrication process steps and characterization of catalytic microcombustors built on (100) silicon-glass platform are presented. Investigation of catalytic combustion regimes for three distinct energents (H₂+O₂, methanol+O₂, methanol+air), fed into the combusting microcavity via pre-mixing through the bubbler or via in-situ mixing on the platform was carried out. Thermodynamic properties, dependent on ignition parameters, light-off temperature and thermal response for various input flow conditions in the temperature range between 80-320 °C were investigated and the results are discussed. It was determined that two-phase flow in microchannels can cause significant pressure oscillations which may degrade the performance of the microcombustor under certain feed conditions. Catalytic combusting via thin film nanodispersed Pt/CeO₂ catalyst proved very efficient, showing light-off for combusting H₂-O₂ already at room temperature and in case of methanol-air combusting reagents at 80 °C. Under optimal conditions, assembled microcombustor was able to provide continuously 4.6 W thermal power, reaching the temperature of 290 ± 1 °C, with 1.1 ml/h consumption of liquid methanol.

Key words: Si-glass micromachining, methanol catalytic combustion, light-off temperature, thermal response

Karakterizacija mikrogorilnika izdelanega na Si (100)/Pyrex steklo podlagi

Povzetek: Predstavljeni so načrtovanje, tehnološki procesi mikroobdelave (100) silicija in stekla ter karakterizacijski postopki za ovrednotenje delovanja mikrosežigalnika. Raziskani so bili pogoji uvajanja in gorenja treh različnih vstopnih energentov (H₂+O₂, metanol+O₂, metanol+air) preko tankoplastnega Pt/CeO₂ katalizatorja. Prikazani so vplivi posameznih parametrov (pretoki, razmerja pretokov, tlaki, temperature) na delovanje in odzivnost mikrogorilnika. Raziskali smo možnosti dveh različnih načinov uvajanja energentov in določili ustrezen nabor parametrov za delovanje mikrogorilnika. Prikazana sta primera uvajanja energentov s predmešanjem metanola in kisika/zraka ter uvajanjem ločenih energentov in mešanje na sami platformi. V slednjem načinu doziranja energentov je bil opazen močan vpliv dvofaznega toka tekočinskega toka kot posledica uparjanja metanola v mikrokanalih pred vstopom v katalitsko izgorovalno komoro. Z uporabo nanodispergirane platine na mezoporozni cerijeви podlagi kot katalizatorja smo dosegli vžig H₂-O₂ energentov že pri sobni temperature, vžig metanola in zraka pa pri temperature 80 °C. Pri optimalnih pogojih smo dosegli stabilno in kontinuirano delovanje načrtanega in izdelanega mikrogorilnika pri temperaturah tudi do 290 ± 1 °C ob izredno nizki porabi tekočega metanola 1.1 ml/h.

Ključne besede: mikroobdelava, Si-steklo podlage, katalitsko gorenje metanola, vžigna temperature, termični odziv

* Corresponding Author's e-mail: Drago.Resnik@fe.uni-lj.si

1. Introduction

Electronic portable applications require extended period of power supply autonomy. Battery technology

can not always satisfy the power demands for the portable electronics [1]. One of the advanced approaches to overcome this problem is the application of proton exchange membrane fuel cells (PEMFC) cells as a port-

able power source [2, 3]. As the input energent, PEMFC require high purity supply of hydrogen. Hydrogen rich gas can be generated from liquid fuel such as gasoline or methanol-water usually by steam reforming (SR) process. In many cases methanol (MetOH) is preferred since it can be efficiently converted into hydrogen at moderate temperatures ($<300\text{ }^{\circ}\text{C}$). Methanol has high H:C (4:1) ratio and no C-C bonds, what minimizes the risk of soot formation which degrades the catalyst performance [4].

The hydrogen fuel processor shown in Fig.1 comprises usually several units in series: evaporizer for methanol-water input energent, SR unit, and preferential oxidation (PrOx) unit. PrOx unit is used to clean-up the hydrogen rich stream by reducing CO amount below e.g. 50 ppm range since higher amount of CO can be poisonous for proton exchange membrane and consequently for fuel cell operation. In certain cases when CO content is too high, water-gas-shift unit (WGS) is included between the SR and PrOx unit. The steam reforming is an endothermic process. Therefore, energy must be provided on board for both, evaporation of fuel and SR reaction. For this purpose methanol combustor can be used as an appropriate indirect heat source, providing heat to support and maintain the required reactions taking place in fuel processor. This is typically attained by burning a small amount of hydrocarbon fuel. Micro-combustors as heat providers are also met in other applications such as in thermophotovoltaic power generators [5] or thermoelectric devices [1, 6].

The leading idea in our case is to utilize the same fuel source (MetOH) for both, SR and catalytic combusting. In the case of excess production of H_2 from SR unit or unexploited H_2 from FC, the methanol is replaced partially or fully with H_2 to maintain catalytic reaction and providing required heat as indicated in Fig. 1.

In the following paper a detailed investigation of a microcombustor unit is carried out. Catalytic (flameless) combustion is taking place in the combusting chamber over the catalyst layer with specific properties. Combusting thermodynamic process in the presence of catalyst is dependent strongly on contact or residence time and activity of catalyst itself. Different types of catalyst and the support material are met in the literature, such as Pt/ZrO₂ [7], Pt-Sn/Al₂O₃ [8], Pt/TiO₂ [9], Pt/Al₂O₃ [1, 10, 11] Pt/CNT [12]. Heterogeneous catalysts are not sufficiently active at room temperature and require external heat for ignition of the fuel [13]. This preheating is a drawback since it requires additional source of energy. A method to achieve spontaneous self-ignition and self-supporting combustion of pre-mixed methanol-air at room temperature (RT) with nanosized Pt catalytic particles has been reported by Ma

et al. [14] for glass tube reactors. Nanosized catalytic particles are significantly more reactive than their bulk counterparts, exhibit high specific surface areas and can significantly increase the performance of catalytic combustors. In this work, developed nanodispersed Pt catalyst on mesoporous CeO₂ support was applied with specific surface areas exceeding 130 m²/g providing even RT ignition in the case of H_2+O_2 combusting.

The main objectives of the presented study were to develop a catalytic microcombustor with Pt/CeO₂ catalyst and to evaluate its thermal performance, with respect to various input energents (H_2+O_2 , MetOH+O₂, MetOH+air), their flow ratio and flow rates. For this purpose, a Si platform with microchannels, mixers and combusting cavity were designed, fabricated and hermetically sealed by Pyrex 7740 glass with anodic bonding technique to provide fluid connections between the pump and microchannels. Besides, advanced DRIE silicon bulk micromachining and newly developed thin film deposition technique for catalyst layer were applied to realize functional microcombustor microfluidic system.

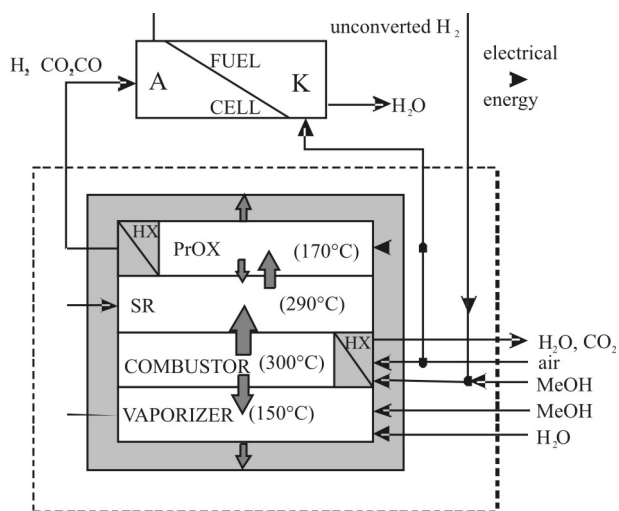


Figure 1: Conceptual integration of components and heat flow in methanol-to-hydrogen fuel processor for PEMFC.

2. Experimental work

Microfabrication process

Basic fabrication steps are presented in Fig. 2. Silicon microfabrication was performed on low resistivity (10-15 Ωcm), n-type, single side mechanically polished float zone (FZ) silicon wafers with {100} crystal orientation.

The masking layer during etching was a 9 μm thick film of AZ 9562 photoresist (Fig.2a). Etching of micro-

channels and cavity in Si (Fig.2b) was performed by deep reactive ion etching (DRIE) process in Plasmalab 80 etcher. The depth of input channels and cavity was 140 μm and width of the inlet channels was 600 μm . After performing DRIE process, the resist was removed in the oxygen plasma reactor Tegal 412 and the wafers were diced into individual Si platforms (35x27 mm^2) and deposition of Pt/CeO₂ catalyst was performed. The Pt (2.0 wt.%)/CeO₂ catalyst precursor was prepared as described elsewhere [15, 16].

A special technique of depositing thinner films in several consecutive depositions was applied to avoid the catalyst film cracking problems. It was determined experimentally that the deposition of a single, thick film has to be avoided due to the cracking of the film, which is later usually peeled off after drying or after calcinations. As the last step, the calcination of cumulative catalyst layer was performed in air ambient at 600 °C for 10 hours (Fig. 2c).

The quantity of Pt catalyst in the cavity was determined after the calcination and was 4 and 7 mg (balance Kern ABJ120-4MJ with 0.1 mg resolution) for depositing three or five layers, respectively. Thickness measurements of catalysts layer were performed by depth focus measurements and cross-sectioning revealing a value of 20-30 μm . The cavity area where catalyst was deposited was 360 mm^2 .

Cleaning and removal of any particles prior to Si-glass bonding is essential for good hermetic sealing of the cavity, since during several deposition steps of catalyst it is very likely that some slurry is dragged toward the bonding surface, despite the hydrophobic nature of the latter. Prior to the anodic bonding operation, Si and Pyrex surfaces were cleaned thoroughly by 2-propanol and DI water, dried by nitrogen and brought into intimate contact under cleanroom environment.

To observe and characterize the flow behavior and ongoing reactions, a transparent cover made of Pyrex 7740 (Dow Corning) glass, 700 μm thick, anodically bonded onto silicon microchannel platform was provided. To enable fluid connections, Pyrex glass had prefabricated inlet and outlet through holes (Fig. 2d). Through holes in Pyrex glass (diameter 800 μm) were fabricated by micro-drilling technique. A special fixture was developed to align Pyrex and Si platform, to obtain accurate positioning ($\pm 10 \mu\text{m}$) of through holes of Pyrex and in/out connections of microchannels. Pyrex was then bonded to silicon by anodic bonding at 385 °C and applied anodic voltage of 1000 V (Fig. 2e).

Prior to testing, catalyst treatment in a reduction ambient (H₂ at 180 °C for 2 hours) was carried out. After the

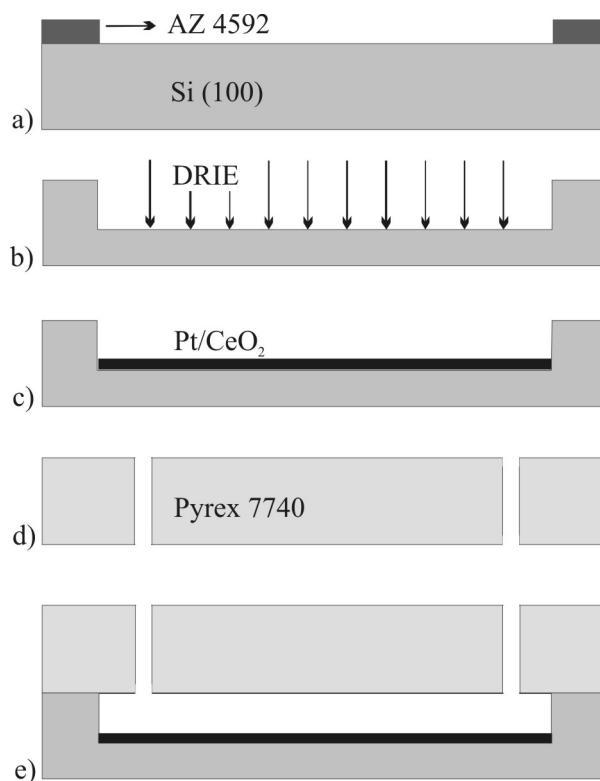


Figure 2: Microcombustor fabrication steps; a) Si microchannel, mixer and cavity patterning, b) DRIE Si deep etching (150 μm), c) deposition of catalyst, d) Pyrex microdrilling and micropositioning of in/out ports, e) aligning and anodic bonding of Si and Pyrex.

microreactor was completed the mounting in a packaging case was performed. Stainless steel (SS) (thermal conductivity $\lambda = 17 \text{ W/mK}$ @ 25 °C) housing with fluidic connection were designed rigid enough to enable reliable packaging, fast replacement of device under test and hermeticity at working temperature. Explicitly, PTFE housing with low thermal conductivity ($\lambda = 0.25 \text{ W/mK}$ @ 25 °C) was used for initial tests for H₂-O₂ combustion experiments only. In Fig. 3 SS case is shown, consisting of two separate parts, top one with laser welded SS tubes for fluidic connections and bottom one with the recessed seat for combustor platform (Fig.3). Rock wool insulation BS15, 25mm thick with thermal conductivity $\lambda = 0.093 \text{ W/mK}$ @ 200 °C was used for thermal insulation during tests, unless otherwise mentioned. Inset in Fig. 3 reveals detail of a gas distributor design enabling homogeneous distribution of vaporized input reagents across the entire cavity thus providing uniform temperature.

Characterization setup

In order to cover a wide range of variables and to maintain good process control of various parameters, the characterization setup was conceived in a modular

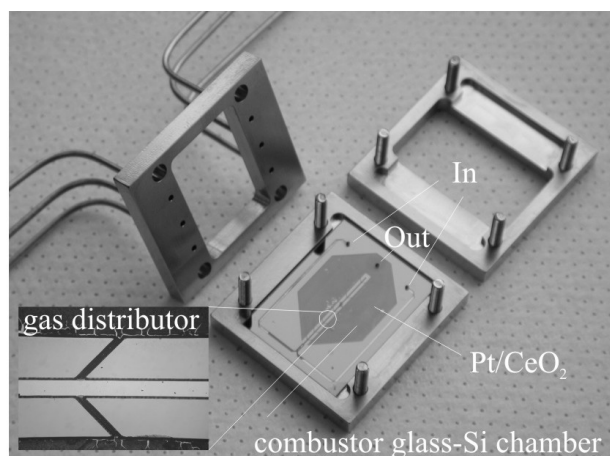


Figure 3: Stainless steel housing with in/out fluid connections and combustor microreactor.

way. This approach enabled fast and reliable multiple measurements with exchangeable combustor platforms and easy switching between different inlet fuel streams.

The temperature measurements were performed by measuring the combustor cover glass temperature and the reactor housing temperature with Pt-100 and K-type temperature sensors, respectively. During experiments the reactor was surrounded by rock wool insulation and the temperature measured on the housing equals to average combustor platform temperature after a certain period. The temperature is a direct indicator of reaction intensity and the measured amount of output water can be taken as a figure of merit and

correlated to overall reaction efficiency. The setup also included pressure and flow controllers for the input quantities.

3. Results and discussion

The designed and fabricated microcombusting platforms were characterized with respect to two different types of combustor fuel (H_2+O_2 or MeOH +air/oxygen) and with respect to two different modes of applying MeOH+ air/oxygen fuel, i.e. by two separate inputs and mixing on the platform or by premixing of methanol and air/oxygen in the bubbler and introducing mixed vapor phase via a single input into the combustor. Characterization was performed by the developed setup shown in Fig. 4.

Characterization of combustor with H_2+O_2 energetics

In this mode of combustor, separate input microchannels for hydrogen and oxygen were designed and fabricated. Mixing of both gases occurs in the microreactor, just prior to reaching the catalyst zone. The mixers were Y type or nozzle type, the same as used for experiments in subsection 3.2 and 3.3.

Total oxidation i.e. combustion of hydrogen and oxygen via catalyst is described by the following equation:

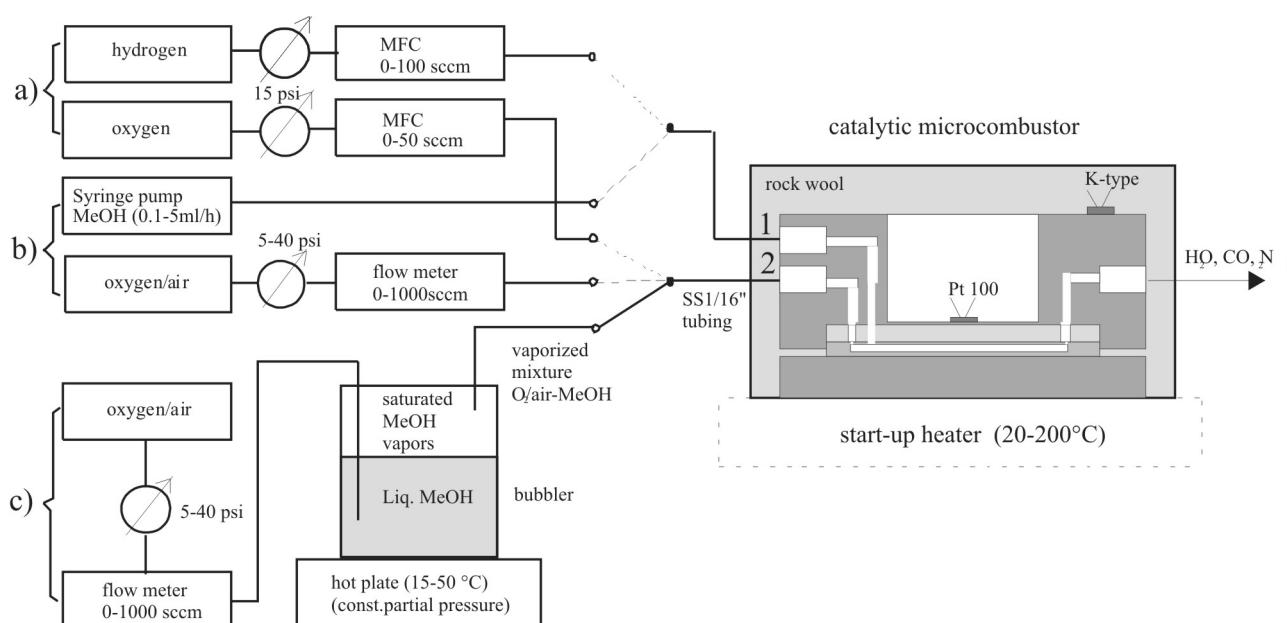


Figure 4: Characterization setup enabling three configurations of input reagents and feed modes: a) combustor of H_2 and O_2 , b) combustor of MeOH and O_2 /air and c) combustor of premixed MeOH+ O_2 /air.

where enthalpy of combustion $\Delta H = 286 \text{ kJ/mol}$ is the higher heating value (HHV). For the case shown below (Fig. 5), e.g. for inlet flow of $\text{O}_2 = 20 \text{ sccm}$ and $\text{H}_2 = 40 \text{ sccm}$, the output of $\Phi_{\text{H}_2\text{O}} = 32 \text{ }\mu\text{l/min}$ and calculated heat power of $P_{\text{th}} = 8.5 \text{ W}$ can be obtained in stoichiometry by assuming the 100% efficiency of the combustor.

It is shown in Fig. 5 that the spontaneous ignition for reaction of H_2 and O_2 can take place on the catalyst successfully already at room temperature, however, the amount of water product shows efficiency slightly above 50%. Nevertheless, this is strong evidence that the prepared nanodispersed Pt on mesoporous ceria oxide is highly active and appropriate type of catalyst, since it starts the reaction at such low light-off temperature. The temperature where reaction takes place is called a light-off temperature and is defined as the temperature at which a catalytic converter achieves 50% conversion rate.

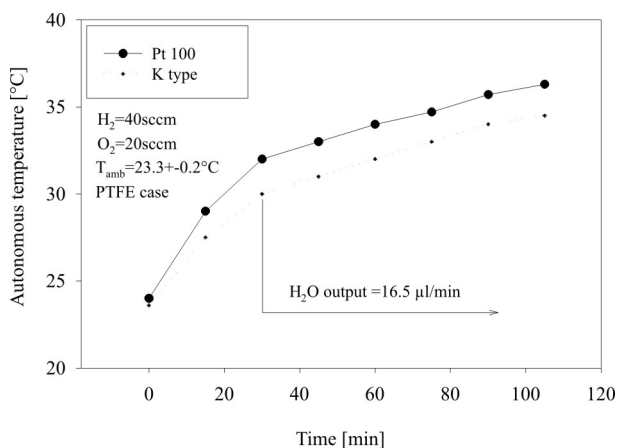


Figure 5: Microcombustor spontaneous ignition obtained at room temperature

Due to high mass load of the combustor PTFE housing (170 g) and slow transition from heterogeneous reaction, the reached final temperature is low, but the reaction is self-sustained. The combustor efficiency in this case was correspondingly low (<50%) regarding the measured amount of the output water.

By increasing the light-off temperature to 100 °C (Fig. 6), the rise time was decreased and the self-sustained process increased and maintained the temperature of the combustor system at 135 °C and also responded instantly on the increased flow rate of both reagents to new value of 50 and 25 sccm for H_2 and O_2 , respectively. The amount of output water was increased compared to RT ignition from 16.5 to 18 $\mu\text{l/min}$ (efficiency 56%). No additional insulation was put around the PTFE housing in this case. Due to PTFE thermal limitation and material softening (loss of rigidity), it was observed that latter can not provide sufficient hermeticity above 180 °C. Therefore, despite having much lower thermal

conductivity, PTFE housing was replaced for all further experiments by SS housing as shown in Fig. 3.

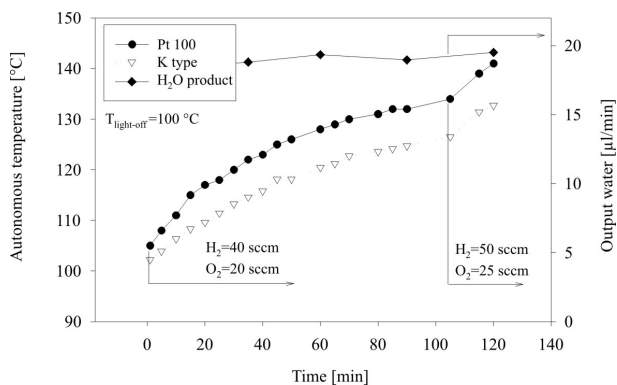


Figure 6: Combustor temperature and amount of output water vs. time for $\text{H}_2\text{-O}_2$ reagents at light-off temperature 100 °C (PTFE case)

By designing new, SS housing with smaller outer dimensions and lower mass (100 g) as well as using 20 mm thick rock wool insulation, the temperature rise time (Fig.7) was actually not improved. This is attributed to higher thermal conductivity compared to PTFE. However, with the implemented heat insulation and reduced heat losses, the final temperature reached 205 °C under the same feed conditions, while combustor efficiency increased to 63%. $\text{H}_2\text{-O}_2$ experiments were conducted mainly to prove the catalyst reactivity at RT and increased fuel flow rate experiments were not considered further in this study due to limited measuring range of available MFC flow controllers.

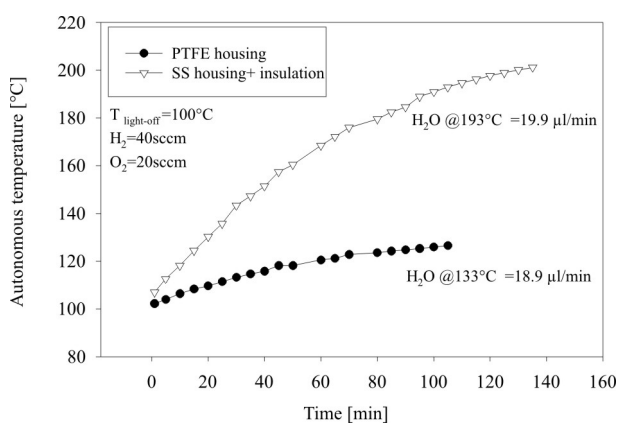


Figure 7: Comparison of the same reactor platform in PTFE and SS housing and with improved isolation, for the same feed conditions.

Estimated error in acquisition of output water was in the range of 10-15%, due to losses of water vapor prior to reaching the cold trap rather than at weighing procedure, so the efficiency is actually higher.

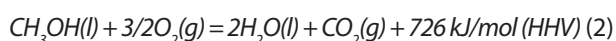
By measuring the quantity of output water, it is shown that at higher start up temperatures, increased amount of output water is obtained, which is closer to theoretical value, meaning that the combusting efficiency is increased.

Since the outlet gas stream from the combustor (water vapor, unreacted gas) is nearly at the temperature of combustor and the condensing heat is delivered to the surrounding after exit, it should be recuperated in a proper way. One way of recuperation is used in our design and consists of placing output near the inlet ports so part of downstream heat is transferred to the cold incoming gas. Another way to recuperate the condensation heat of the exit water vapor to the inlet H₂ and O₂ gas stream is to put in physical contact inlet H₂ and O₂ tubes with exiting hot tube in a manner of counter flow heat exchanger (depicted as HX in Fig.1).

Characterization of combustor with internal mixing of MeOH + O₂

To start the exothermic reaction, certain conditions must be fulfilled: efficient catalyst layer, appropriate dimensions of cavity to stay well below explosion limits and start up temperature for ignition. Methanol-oxygen catalytic ignition requires high activation energy (high energy input is required). After ignition, the reaction proceeds with a higher rate constant and has lower activation energy compared to the one for ignition. Once ignited, the reaction is sustained as long as fuel and oxygen (air) is available in proper ratio and quantity.

According to work of Hu et al. [13], two distinctive combusting regimes are met (two different reaction mechanisms), depending on different fuel ratio, a slower, heterogeneous-only catalytic reaction on the catalyst surface and a faster, mixed reaction regimes that includes both, hetero catalytic reaction on the nano-particle surfaces and a homogeneous combustion of the methanol + air in gas phase above the catalyst surface, supported by radicals. Combusting of methanol in presence of oxygen is described by the following overall reaction:



where exothermic heat of 726 kJ/mol (higher heat value, HHV), is produced in reaction with oxygen at stoichiometry. Overall, the heat obtained by combustion has to satisfy the following equation if the combustor is used for SR applications:

$$Q_{\text{comb}} > [Q_{\text{heat-up}} + Q_{\text{vap}}]_{\text{comb}} + [Q_{\text{heat-up}} + Q_{\text{vap}}]_{\text{SR}} + Q_{\text{SR}} + Q_{\text{loss}} \quad (3)$$

where first part is to heat up and evaporize the methanol for combusting, the second part is to heat up and evaporize the methanol-water mixture SR feed, the third is to cover the enthalpy of SR process and the fourth is to cover mostly the convective losses toward ambient, due to limited thermal insulation.

E.g. for input flow rate of 1ml/h of liquid methanol MeOH and 13.8 sccm of O₂, the output rate of $\Phi_{\text{H}_2\text{O}} = 14.8 \mu\text{l/min}$ is obtained in stoichiometry and the heat power produced is $4.97 \text{ W}_{\text{th}}$.

Separate input ports and mixing inside the reactor were applied in this type of combusting (Fig. 8c). Two important parameters should be fulfilled for this type of fuel applications: complete evaporation of the liquid methanol and sufficient degree of mixing methanol vapors and oxygen or air before entering the catalytic zone.

The liquid methanol entering hot zone has to vaporize fully before reaching the mixing point, otherwise it can flood the catalyst cavity and extinct the reaction. This can be fulfilled by increased microchannel length to provide sufficiently long path to fully evaporize the liquid methanol and heat up reactant gas, respectively, before they reach the mixing point.

Sufficient mixing is a prerequisite condition prior to introduction of reactants into the catalyst covered combustor cavity. Due to laminar flows in microchannels this is a demanding task, particularly when it has to be performed along a short path. Two approaches were undertaken to support better mixing; one being the introduction of a nozzle to introduce methanol at the point where the reactant gas is added (oxygen or air) and the other is the introduction of mixing obstacles in the microchannel leading toward the combusting cavity (Fig. 8b), similar to [17]. Mixing of two flow streams in microchannels, where usually laminar flow prevail is rather difficult to obtain. The dispersion of solutes occurs by diffusion which is a slow process [17] and in case of geometrically splitting and recombining flow streams with obstacles also by convection in lateral direction. Passive mixing principle was used in our design which does not contribute to pressure drop and also does not introduce any dead volumes [17]. The obstacles, i.e. pillars, were placed asymmetrically in the main microchannel at certain positions, determined preliminary by ANSYS simulating tool (Fig. 8a). The chosen design of mixing pillars also had to comply with the micromachining process for simultaneous fabrication of the whole silicon structure in a single DRIE step and a single mask (Fig. 2b).

Once these conditions are fulfilled, the final temperature (delivered heat energy) of such microcombustor

depends on the following parameters: i) input flow of reagents, ii) type, efficiency and quantity of catalyst, iii) thermal isolation, boundary conditions (wall heat transfer) and iv) design issues of microchannels, mixer, cavity and exhaust path (defining pressure drop).

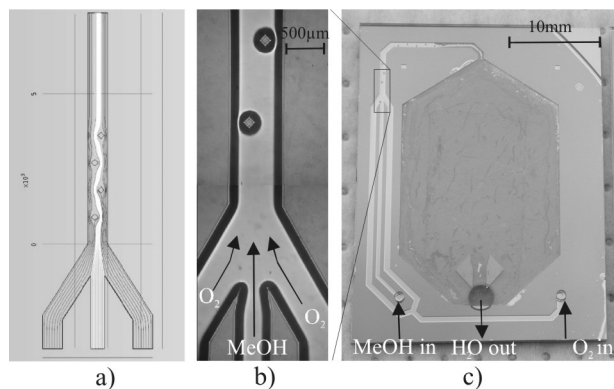


Figure 8: Combustor type 1 with designed separate inputs, mixer and micromachined obstructions for improved mixing in the microchannel: a) Ansys modeling, b) top view of a mixer detail, c) completed microcombustor.

In the first set of experiments, performed on microcombustor platforms (mounted into the SS housing and insulated by rock wool) without sufficient mixing efficiency, only insignificant temperature rise was sensed due to the fact that heat losses toward ambient exceeded the generated heat. The only indication that the reaction was taking place was the output water. In certain cases, when mixing was insufficient or fuel rich mixture was applied, the output product was sensed as a mixture of water and unreacted methanol as shown by gas chromatography analyses or with analyzing the contact angle and by comparing it with the reference DI water droplet. Another problem associated with liquid methanol on board evaporation was encountered during experimental work as strong, periodic pressure oscillations.

Pressure oscillations were determined to be a consequence of methanol evaporation process in the microchannel. As observed by Wu et al. [18], this is a common phenomenon for two-phase flow in microchannels. The liquid-vapor interface oscillates as some of the already formed vapor condenses back, causing change of volume and even a reverse flow can be expected in some cases.

In the microcombusting process, similar oscillation of the system was observed as a consequence of the above mentioned phenomenon and/or due to back-pressure caused by condensation of water in the exit line. The water product at the exit was observed to be pushed out periodically, when the exit line becomes

clogged with the droplet across the pipe diameter. This reflects also on the input feed conditions as a shattering of inlet liquid methanol silicone tube. The coupling of output and input exist via the backpressure oscillations, which may cause the damping and/or extinction of the reaction process in the combustive cavity.

Pressure oscillation during evaporation was also measured in separate experiments for the case of MeOH-DI water (2:1 volumetric) in meandered microchannels, 600 μm wide, 150 μm deep and total length of 150 mm. The pressure oscillations are well observed in Fig. 9, particularly at higher flow rates. The evaporizer was supplied with constant heat power, so the temperature decreased by increasing the amount of input liquid. Besides, as can be seen in illustrations above the graph, the point of fully evaporated liquid moves downstream. The oscillation period was around 60 s for a specific case and the amplitude is increasing by the flow rate of input medium up to 50 mbar at 9 ml/h as shown in the Fig. 9. In this particular case, the electrical heat power of 8.5 W was required to maintain the evaporation and cover heat losses. However, in the presented study of combustive, where the flow rate of liquid methanol never exceeded 1.5 ml/h, the oscillations were of shorter period. Oscillation in pressure is strongly correlated to water droplet formation (condensation) at the exit which in turn influences back the input feed conditions.

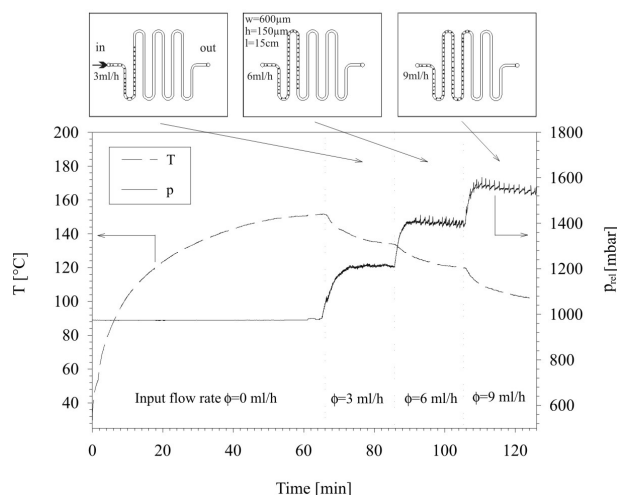


Figure 9: Evaporation of MeOH:DI (2:1 vol.) in meandered microchannel: temperature and pressure vs. time for three input flow rates, at constant heating power of 8.5W.

Autonomous combustive for internal mixing of MeOH and oxygen /air was obtained within narrow range of feed parameters. Fig. 10 presents the successful performance of combustive and the obtained temperature in full autonomy once the ignition started at light-off

temperature 200 °C (diamond symbols). In the next experiment, the input ports were exchanged. In this case, mixing was presumably improved and higher efficiency as well as higher final temperature (square symbols) was obtained and maintained. Temperature stability in the first case was 200 ± 2 °C in time interval 20-190 min (after which the fuel feed was changed) and 185 ± 3 °C (considering time interval from 15-190 min).

One of the reasons for low increase of temperature in autonomous self-sustained combusting process is that additional heat to evaporize the amount of introduced methanol ($Q_{\text{heat-up}} + Q_{\text{evap}}$) must be provided.

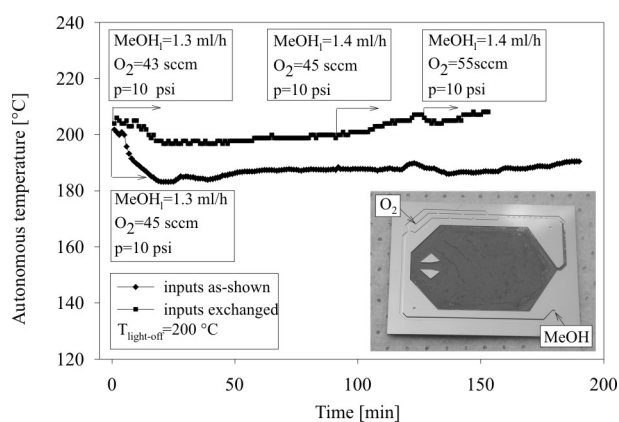


Figure 10: Autonomous combustor temperature with separate oxygen and methanol inputs and internal mixing on the platform for two modes of reagent supply.

In certain cases the generated heat was insufficient to rise the temperature and the output contained some unreacted methanol in particularly when the reaction was under fuel rich conditions or the mixing was insufficient. The residence time of MeOH-air/oxygen mixture in the cavity has to be longer than the time required for the chemical reaction. This is described by a Damkohler number and should be >1 . It is assumed that in certain cases this condition was not fulfilled. On the other hand, excessive amounts of input methanol cause that the catalyst is no longer capable of proper function and simultaneously, the unreacted components are expelled to the outside ambient by the pressure difference. The reactor could even become flooded with liquid methanol if the evaporation is not fully completed.

It was also observed that when a certain oxygen flow rate is exceeded, the methanol pressure from the syringe pump was actually insufficient for introduction into the microchannel due to oxygen pressure interference. This was the limitation for increasing further the methanol feed. Therefore, at this point we were just able to maintain the reaction and the temperature, but

could not increase it by increasing the feed rate. Limitations for achieving autonomous combustion can be found in specific geometry of the chamber, efficiency of mixing unit, exhaust orifice size, co-dependency of inlet pressures of both reagents and the reaction type taking place (heterogeneous only or transition toward homogeneous).

Table 1 and 2 shows conditions corresponding to two input configurations also presented in Fig. 10, indicating successful self-sustaining combusting parameters and the output products.

Table 1: Combustor input conditions and output products in separate feed mode-standard input ports.

MeOH [ml/h]	O2 [sccm]	H2O [$\mu\text{g}/\text{min}$]	H2O+MeOH	autonomy
1	35	6,7		no
1,2	43		11,8	no
1,3	45	13,8		yes

Table 2: Combustor input conditions and output products in separate feed mode-exchanged input ports.

MeOH [ml/h]	O2 [sccm]	H2O [$\mu\text{g}/\text{min}$]	H2O+MeOH	autonomy
1	35	10,5		no
1,2	35		13,21	no
1,2	43	13,5		no
1,3	43	15,05		no
1,3	43	16,16		yes
1,4	45	17,3		yes

Characterization of combustor with premixed MeOH + O₂/air fuel

For this mode of fuel delivery, bubbler principle was used to feed the microcombustor, which was mounted into the SS housing and insulated by rock wool. As shown schematically in Fig. 4c, oxygen or air stream carrier gas enters the liquid methanol vessel and bubbles rise through the methanol into the vapor phase above where it is further mixed with saturated methanol vapors and then exit into the feeding line toward reactor. When it reaches the catalyst covered chamber, the reaction (eq.1) takes place after the proper ignition conditions are met such as light-off temperature, sufficient catalyst activity and fuel to oxygen ratio.

Combustor temperature vs. partial pressure of methanol and carrier gas flow rate

The bubbler temperature determines the partial pressure of saturated methanol vapors and must be well

controlled. If the volume above the methanol liquid level is saturated, the inlet oxygen or air flow mixes with methanol vapors and transports it toward the outlet, thus depleting the methanol concentration in the bubbler. Dynamic process of forming the vapor phase above the surface of the liquid methanol has to maintain equilibrium with the carrier gas at certain temperature. Carrier gas has actually two functions, i.e. promotes the mass transport of methanol vapors into the combustor cavity and also takes a part in the combustor reaction, and therefore has to be carefully adjusted to meet both requirements.

As discussed also by Ma et al. [14], when the carrier gas velocity increases (i.e. inlet flow rate is increased), methanol concentration slightly decreases (i.e. ratio $F = \text{Fuel}/\text{Air}$, decreases), indicating that the residence time in bubbler is increasingly too short for the air to fully saturate with methanol at higher flow rates.

At a constant flow of carrier gas through the bubbler, the quantity of methanol vapor entering the combustor is increased by the temperature of bubbler and so is the temperature of the combustor (Fig. 11). Therefore also carrier gas amount has to be sufficient to fulfill the stoichiometric ratio for the reaction or to be slightly above it (fuel lean conditions). By this means the entire methanol will be reacted (oxidized) and no unreacted methanol will appear at the exit of combustor. In this case only water and CO_2 will be the byproduct. This is actually a good indicator of complete reaction taking place in the cavity. If we obtain the unreacted (surplus) methanol at the exit, this indicates the reaction was not complete due to mixture ratio or geometrical and catalyst efficiency limitations for the overall quantity of input energent, as discussed also in previous section.

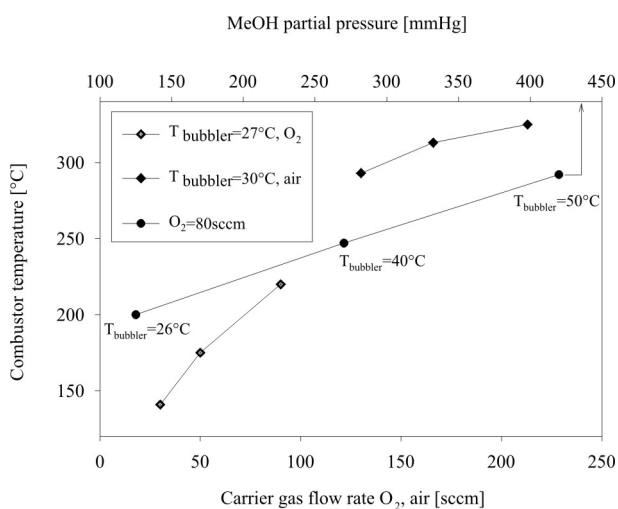


Figure 11: Dependency of methanol partial pressure (bubbler temperature) and carrier gas flow rate on the combustor temperature.

As shown in Fig. 11, adjusting the combustor temperature can be performed by controlling partial pressure of methanol vapor or by adjusting the carrier gas flow rate within the reasonable range, limited by the combustor design and thermodynamic issues such as residence time or reaction mode. Fig. 12 shows the heat up curve of the combustor in autonomous regime, followed by instant combustor response to reduced carrier gas flow rate and steady state temperature that could be obtained after prolonged period. The transient is rather long (>100 min) due to the high thermal load of the combustor housing. For oxygen as a carrier gas, the combustor efficiency of 85-90% was determined by measuring the amount of output water from the combustor process, with respect to calculated stoichiometric water product. The combustor efficiency with air was determined to be 80-85 %, which is slightly lower compared to oxygen carrier gas.

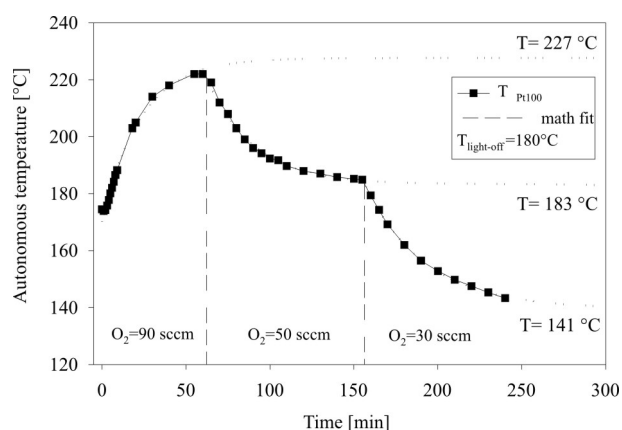


Figure 12: Influence of oxygen flow rate on the combustor temperature in autonomous regime.

Fig.13 presents the influence of the some additional insulation details on the obtained final temperature of the combustor when fed with constant amount of input fuel. For the given input parameters, the temperature reached was 280 °C when the combustor was insulated by 20 mm thick rock wool shield. During experiments, the exhaust hood was mounted above the reactor due to safety reasons if unreacted methanol exits. This causes forced convection around the combustor. When it was removed, the temperature slightly increases up to 286 °C. By lifting the rock wool insulated combustor from the table and putting it on the three small posts (decreasing thus the conductive heat losses) additional slight increase of temperature was obtained. To further reduce heat losses caused by radiation, the system was enclosed with Al foil and the temperature was increased to 293 °C. All three steps cumulatively contributed to rise of temperature (e.g. 13 °C or 4.6%). The insulation issues need to be considered further in order to reduce heat losses and achieve

faster thermal response. Though it is desirable to have fast thermal response of the system, this also means that the system will be sensitive to undesired ambient changes. As shown in Fig.13, the consumption of liquid methanol during 6 hours period was as low as 1.1 ml/h to maintain the combustor temperature between 280 and 293 °C.

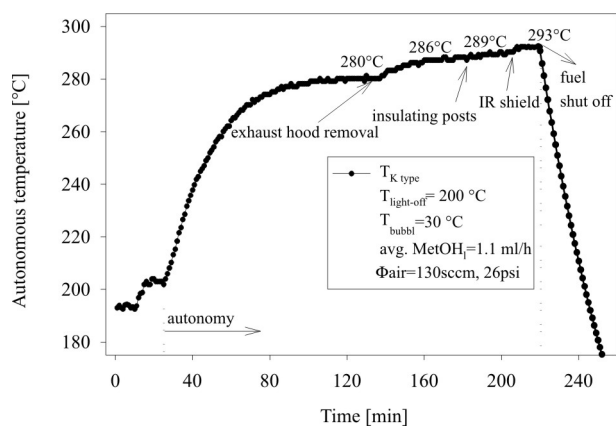


Figure 13: Influence of additional insulating steps on the steady state temperature of combustor.

In the case of air carrier gas, the reaction reagents are diluted by additional nitrogen. Equilibrium between the introduction of methanol vapors and needed oxygen from the air carrier gas has to be established. The outgoing products contain also inert N_2 carrier gas. If the flow rate of air is too high, the amount of unreacted methanol over the catalyst can exceed the ability of catalyst to support the reaction (residence time is too short) and some methanol can leave the combustor unreacted.

The influence of light-off temperature in the range 80–200 °C on temperature rise time was studied in more details in a previous work [16]. It was shown that the combustion was successful for light-off temperature of 100 °C and above. At 80 °C, the ignition level was too low and the reaction did not take place at all. By providing higher light-off temperatures and implementing oxygen carrier gas instead of air, the transition of heterogeneous type of reaction to self-sustained homogeneous was found to decrease.

Fig. 14a presents SEM top view of mesoporous ceria and nanodispersed Pt and Fig. 14b presents cross-section of catalyst layer on the Si substrate. The catalyst layer was examined after performing several experiments (cumulatively >100 h) under different feed conditions. No changes in morphology or carbonaceous deposits were found on the catalyst layer, indicating that the catalyst layer can withstand severe overloading or fuel rich conditions.

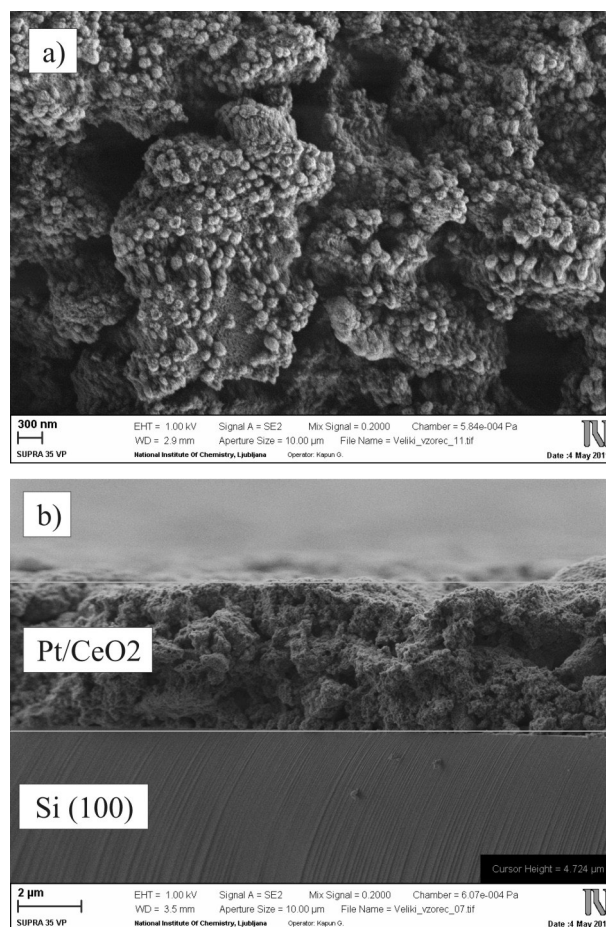


Figure 14: Deposited Pt/CeO₂ catalyst within the combustor chamber: a) top view and b) cross section.

Discussion on the presented combusting approaches:

Each of the presented approaches in this study offer certain advantages and disadvantages. The applicability of individual approach depends strongly on the field of application, type of available or required energent, light-off temperature, range of aimed working temperature and similar. Table 3 summarizes some results obtained during this study. Due to the fact that parameters for each approach were different the data given correspond only to given process conditions and type of combustor design.

Though the advantageous self-ignition can be obtained already at RT as shown in Fig. 5, H_2 - O_2 energent is eventually not a practical type of fuel for portable applications, because it is not widely available in field operations, nor as a separate storage tanks neither from anode of fuel cell as the excessive hydrogen. For fast start up from RT, all three presented approaches actually require additional energy, usually heating by e.g. thin film Pt electrical heaters [19]. More efficient tem-

perature time response at RT light-off could eliminate need for electrical heating.

As shown in the table 3, combustor with in-situ mixing showed relatively good efficiency, however the fuel evaporation and mixing realized on the same Si platform is a rather demanding task. There is a strong interplay between geometrical issues, evaporation paths, mixing efficiency as well as precise control of the amount and ratio of mixed fuel reaching the catalyst surface [20]. The consequence is that combustion process and final temperature are not easy to control independently. Further work is still required to optimize the combustor design for higher performance. Important fact that was determined by our experimental work was that certain combustor design covers only a limited range of working parameters where optimal efficiency is obtained; once out of range, the ignition is not reached or the oxidation process is not completed (unreacted products are detected) or the combustion is completely ceased.

Our experimental results show that for the type of designed reactors, the most suitable methanol feed approach is by premixing air or oxygen and methanol via bubbler. It was shown that final temperature can be well controlled with adjusting the input parameters and by proper heat loss management. From the point of repeatability, combusting of premixed MeOH-O₂/air showed superior results compared to H₂-O₂ or in-situ mixing.

Long-term stability tests with bubbler type autonomous combusting over prolonged period also revealed the best performance as shown in our previous work [16]. In that study the measured average consumption rate of liquid methanol to maintain 320 °C temperature over 7 hour period was below 1.45 ml h⁻¹ and the stability 320 ± 1 °C. Taking into account the determined combusting efficiency of 90%, the delivered average thermal power in that case was 6.5W [16]. Unfortunately, bubbler type of dosing is not practical in the field due to drawbacks such as required tight control of bubbler temperature and being also position sensitive. The so-

lution of internal mixing is still preferred for field operation, therefore abovementioned problems require further attention.

4. Conclusions

Design, microfabrication process and characterization of silicon-glass based microcombustor with Pt/CeO₂ catalyst, as a heat provider for various endothermic processes, were presented. The influence of some important parameters, such as input flow rate of reagents, premixing regime, pressure and light-off temperature were presented and discussed. Three different types of fuel application were presented and each characterized by means of thermal response characteristics and heat provisions. The prepared Pt/CeO₂ catalyst proved very efficient, providing the ignition of H₂-O₂ energets already at room temperature. Bubbler type of methanol air/oxygen fuel delivery exhibited the most promising results regarding the provided heat, temperature control and methanol consumption. This type of microcombustor exhibited average consumption rate of liquid methanol typically 1.1 ml h⁻¹ to maintain temperature 290 ± 1 °C.

Acknowledgments

This work was supported by the Ministry of Defense of the Republic of Slovenia (Grant No. MORS 345/2007-RR) and Slovene Research Agency (No. P2-0152). The authors would like to extend their gratitude to dr. J. Batista from National Institute of Chemistry, Slovenia, for catalyst preparation.

References

1. A.M. Karim, J.A. Federici, D.G. Vlachos, Portable power production from methanol in an integrated thermoelectric/microreactor system, *J. Power Sources* 179 (2008) 113-120.

Table 3: Summarized performances at specific parameters for the presented combusting approaches.

Energent type	Light-off temperature [°C]	Efficiency %	Final temperature [°C]	Fuel consumption
H2-O2	100	63	210	40/20 sccm
MeOH+O2 (pre-mixed)	180	89	225	0.9 ml/min MeOH 90 sccm O2
MeOH+air (pre-mixed)	160	84	293	1.1ml/h MeOH 130sccm air
MeOH+O2 (in-situ mix)	200	86	200	1.3ml/h MeOH 43sccm O2

2. J.D. Morse, Micro-fuel cell power sources, *Int. J. Energy Res.* 31 (2007) 576–602.
3. K. Shah, R.S. Besser, Key issues in the microchemical systems-based methanol fuel processor: Energy density, thermal integration, and heat loss mechanisms, *J. Power Sources* 166 (2007) 177–193.
4. B. Lindström, L.J. Pettersson, Catalytic oxidation of liquid methanol as a heat source for an automotive reformer, *Chem. Eng. Technol.* 26 (2003) 473–478.
5. J.F. Pan, W.M. Yang, A.K. Tang, S.K. Chou, L. Duan, X.C. Li, H. Xue, Micro combustor in sub-millimeter channels for novel modular thermophotovoltaic power generators, *J. Micromech. Microeng.* 20 (2010) 125021 (8pp).
6. J.A. Federici, D.G. Norton, T. Brüggemann, K.W. Voit, E.D. Wetzel, D.G. Vlachos, Catalytic micro combustors with integrated thermoelectric elements for portable power production, *J. Power Sources* 161 (2006) 1469–1478.
7. J. Y. Won, H. K. Yun, M. K. Yeon, S. I. Woo, Performance of micro channel reactor combined with combustor for methanol reforming, *Catal. Today* 111 (2006) 158–163.
8. S.-K. Ryi, J.-S. Park, S.-H. Choi, S.-H. Cho, S.-H. Kim, Novel micro fuel processor for PEMFCs with heat generation by catalytic combustion, *Chem. Eng. J.*, 113, (2005), 47–53.
9. K. Yoshida, S. Tanaka, H. Hiraki, M. Esashi, A micro fuel reformer integrated with a combustor and a micro channel evaporator, *J. Micromech. Microeng.* 16 (2006) S 191–197.
10. J.D. Morse, R.S. Upadhye, R.T. Graff, C. Spadaccini, H.G. Park, E.K. Hart, A MEMS-based reformed methanol fuel cell for portable power, *J. Micromech. Microeng.* 17 (2007) S237–S242.
11. G.-G. Park, S.-D. Yim, Y.-G. Yoon, C.-S. Kim, D.-J. Seo, K. Eguchi, Hydrogen production with integrated micro channel fuel processor using methanol for portable fuel cell systems, *Catal. Today* 110 (2005) 108–113.
12. D.-E. Park, T. Kim, S. Kwon, C.-K. Kim, E. Yoon, Micromachined methanol steam reforming system as a hydrogen supplier for portable proton exchange membrane fuel cells, *Sens. Actuators A* 135 (2007) 58–66.
13. Z. Hu, V. Boiadjev, T. Thundat, Nanocatalytic spontaneous ignition and self-supporting room-temperature combustion, *Energ. Fuel.* 19 (2005) 855–858.
14. Y. Ma, C. Ricciuti, T. Miller, J. Kadlowec, H. Pearlman, Enhanced catalytic combustion using sub-micrometer and nano-size platinum particles, *Energ. Fuel.* 22 (2008) 3695–3700.
15. P. Djinović, J. Batista, J. Levec, A. Pintar, Comparison of water–gas shift reaction activity and long-term stability of nanostructured CuO-CeO₂ catalysts prepared by hard template and co-precipitation methods, *Appl. Catal. A* 364 (2009) 156–165.
16. D. Resnik, S. Hočevár, J. Batista, D. Vrtačnik, M. Možek, S. Amon, Si based methanol micro combustor for integrated steam reformer applications *Sens. Actuators A* (2012).
17. A.A.S. Bhagat, E.T.K. Peterson, I. Papautsky, A passive planar micromixer with obstructions for mixing at low Reynolds numbers, *J. Micromech. Microeng.* 17 (2007) 1017–1024.
18. H. Wu, M. Yu, P. Cheng, X. Wu, Injection flow during steam condensation in silicon microchannels, *J. Micromech. Microeng.* 17 (2007) 1618–1627.
19. D. Resnik, D. Vrtačnik, M. Možek, B. Pečar, S. Amon, Experimental study of heat-treated thin film Ti/Pt heater and temperature sensor properties on a Si microfluidic platform, *J. Micromech. Microeng.* 21 (2011) 025025 (10pp).
20. B. Pečar, M. Možek, D. Resnik, D. Vrtačnik, U. Aljančič, S. Penič, S. Amon, Microflow generator for fuel cell methanol hydrogen microreactor, *Informacije MIDEM = Journal of microelectronics, electronic components and materials* ISSN: 0352-9045.- Letn. 40, št. 3 (sep. 2010), str. 208–217.

Arrived: 17. 08. 2012

Accepted: 5. 11. 2012

The Influence of Diodes and Transistors Made of Silicon and Silicon Carbide on the Nonisothermal Characteristics of Boost Converters

Krzysztof Górecki, Janusz Zarębski

Gdynia Maritime University, Department of Marine Electronics, Poland

Abstract: In the paper the results of simulations and measurements of the boost converter operating with silicon and silicon carbide devices are presented. SPICE simulations were performed with the use of electrothermal hybrid models of unipolar transistors and Schottky diodes. The influence of the input voltage, the pulse-duty factor and the load resistance of the boost converter including silicon MOSFET, silicon Schottky diode, silicon carbide Schottky diode and silicon carbide MESFET on characteristics of this converter are analysed. The simulation results are verified experimentally. On the basis of obtained results of calculations and measurements, the influence of selection of the considered semiconductor devices on the boost converter characteristics is discussed.

Key words: Boost converter, SiC semiconductor devices, steady state characteristics, modelling

Vpliv diod in tranzistorjev iz silicija in silicijevega karbida na neizotermične karakteristike stikalnega pretvornika navzgor

Povzetek: V članku so predstavljeni rezultati in meritve stikalnega pretvornika navzgor z elementi iz silicija in silicijevega karbida. Izvedene so bile SPICE simulacije z uporabo elektrotermičnih hibridnih modelov unipolarnega tranzistorja in schottkyjevih diod. Analiziran je vpliv vhodne napetosti, razmerja med pulzom in premorom in upornosti bremena stikalnega pretvornika navzgor s silicijevim MOSFET, silicijevo schottky diodo, schottky diodo iz silicijevega karbida in MESFET iz silicijevega karbida na karakteristike pretvornika. Simulacije so eksperimentalno preverjene. Na osnovi izračunov in meritev je obrazložen vpliv izbranih elementov na lastnosti stikalnega pretvornika.

Ključne besede: stikalni pretvornik, polprevodniški elementi iz SiC, statična karakteristika, modeliranje

* Corresponding Author's e-mail: gorecki@am.gdynia.pl

1. Introduction

The non-isolated boost converter – NBC (Fig.1) belongs to a class of power electronic circuits most often used. The NBC is applied both in supplying circuits and power factor correction (PFC) circuits [1 - 7]. Properties of the considered converter depend on parameter values of the component elements, especially – semiconductor power devices, e.g. [6 - 12].

Typically, silicon power devices are used in boost converters, but recently more and more papers describe

such circuits with silicon carbide (SiC) devices [2 – 4, 10 - 17]. The properties of silicon carbide power semiconductor devices are presented in many papers, e.g. in [7, 18 – 25]. In the cited papers, it is underlined that SiC power semiconductor devices can operate in higher temperature and with higher switching frequency than classical silicon semiconductor devices. In the papers [2 – 4, 10 – 15, 17] the switching converters including SiC Schottky diodes, power JFETs, power BJTs or power MOSFETs are described. The considered converters are utilized in PFC circuits, photovoltaic (PV) systems, inverters for IPM traction drive or other high frequency

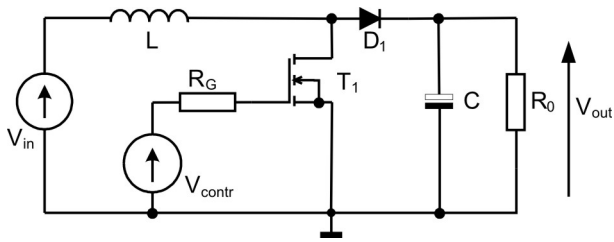


Figure 1: The non-isolated boost converter

and high voltage power networks. The authors of the cited papers proved that using SiC semiconductor power devices make possible to reduce power losses in high voltage switching converters [26].

Nowadays, specialist computer programs along with devices models are used in the process of analysing and designing electronic circuits. SPICE is one of the most popular tools used for this purpose [1, 27-30].

One of the essential physical phenomena influencing the devices and dc-dc converters characteristics is selfheating [1, 8, 27, 30 - 35]. To take into account such a phenomenon in the circuits' analysis, the device electrothermal models have to be used. Due to some properties of pulse circuits, the electrothermal models have to model, first of all, the device ON and OFF states. Apart from this, such models should have possibly relative short time of calculations. Unfortunately, the so called global electrothermal models (GETM) [24, 36 - 41] do not possess such properties and therefore GETMs are not suitable to analyse dc-dc converters. The GETMs are the complex model, which describe properties of semiconductor devices very accurately using the network form composed of passive components and controlled current or voltage sources. For example, some attempts to use the GETM of Schottky diode [36] and MESFET [37] lead to unconvergency of calculations.

In turn, as it was shown in [8, 30, 42, 43, 47], the hybrid electrothermal models (HETM) assure both high accuracy and acceptable time of calculations. Such models consist of two parts. First of them is the isothermal model built-in in SPICE whereas the second part includes controlled current or voltage sources modelling the influence of the increase of the internal device temperature on its terminal currents and voltages. Forms of such models for the considered devices are presented in the next section.

In this paper, which is the extended version of the paper [44], properties of boost converters with unipolar transistors and Schottky diodes made of silicon and silicon carbide are compared. The theoretical considerations are illustrated by some results of the calculations and measurements.

2. Electrothermal hybrid models of unipolar transistors and diodes

The hybrid electrothermal models of semiconductor devices dedicated for SPICE were presented for example in [8, 30, 43, 44]. HETM consists of the isothermal device model built-in in SPICE, the controlled voltage sources modelling the additional voltage drops between the device terminals resulting from selfheating and the compact device thermal model making it possible to calculate the device internal temperature, based on the device dissipated power course and the course of the device transient thermal impedance.

Fig. 2 illustrates the network representation of the hybrid linear model of the diode, in which the influence of the temperature on the voltage drop across the forward biased junction and the series resistance is taken into account.

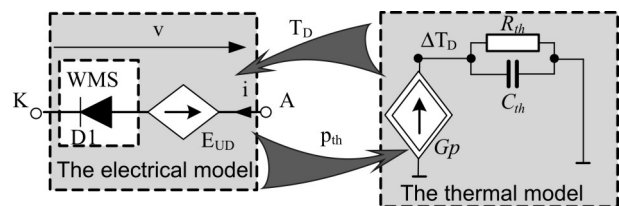


Figure 2: The circuit representation of the hybrid electrothermal model of the diode

In this model D1 represents the isothermal diode model built-in in the SPICE program [45], the controlled voltage source E_{UD} models the temperature changes of the voltage across the forward biased junction and on the diode series resistance.

The value of the source E_{UD} is given by the formula

$$E_{UD} = i \cdot RS \cdot \alpha_{RS} \cdot (T_D - T_0) + \alpha_U \cdot (T_D - T_0) \quad (1)$$

where RS designates the series resistance of the diode at the reference temperature T_0 , α_{RS} is the temperature coefficient of relative changes of this resistance, α_U is the temperature coefficient of the voltage changes on the forward biased junction, whereas T_D denotes the internal temperature of the diode.

The compact thermal model is composed of the source Gp , the current of which is equal to the device thermal power p_{th} and the two-terminal R_{th} , C_{th} modelling the device transient thermal impedance. To reduce the time of calculations only one thermal time constant of the non-physical value characterizing the device transient thermal impedance was used in the model [8, 30]. The power model is given by the formula

$$p_{th} = v \cdot i \tag{2}$$

In turn, the circuit representation of the electrothermal hybrid linear model of the unipolar transistor, in which the dependence of the series resistance of the drain on the temperature is taken into account, is shown in Fig.3.

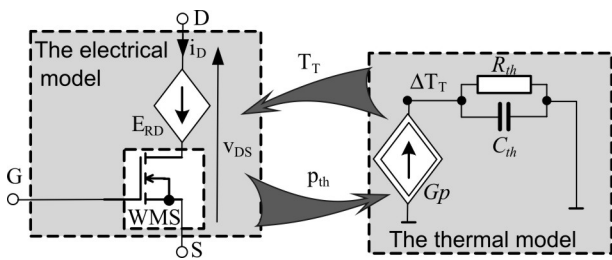


Figure 3: The circuit representation of the hybrid electrothermal model of the MOSFET transistor

In Fig.3 WMS stands for the isothermal model of the MOSFET transistor built-in in the SPICE software [45], the controlled voltage source E_{RD} models the dependence of the series resistance of the drain on temperature.

The value of the source E_{RD} is given by the formula

$$E_{RD} = i_D \cdot R_{ON} \cdot \alpha_{RD} \cdot (T_T - T_0) \tag{3}$$

where R_{ON} designates the value of the transistor on-state resistance at the reference temperature T_0 , α_{RD} is the temperature coefficient of the relative changes of this resistance, whereas T_T denotes the internal temperature of the transistor.

The power model is given by the formula

$$p_{th} = v_{DS} \cdot i_D \tag{4}$$

where the voltage v_{DS} and the current i_D are marked in Fig.3.

In both the presented models the internal device temperature (T_T for the transistor and T_D for the diode) is the sum of the ambient temperature T_a and the temperature excess (ΔT_T for the transistor and ΔT_D for the diode) calculated from the thermal model.

3. Results

In this Chapter the results of experimental verification of the electrothermal hybrid models of the diode and the unipolar transistor (see Chapter 2) as well as the boost converter with these devices are presented. The investigations were performed for four devices: the silicon Schottky diode 1N5822, the silicon carbide Schott-

ky diode SDP04S60, the silicon MOSFET IRF540 and the silicon carbide MESFET CRF24010.

The parameter values of the electrothermal hybrid models of the considered devices are collected in Appendix.

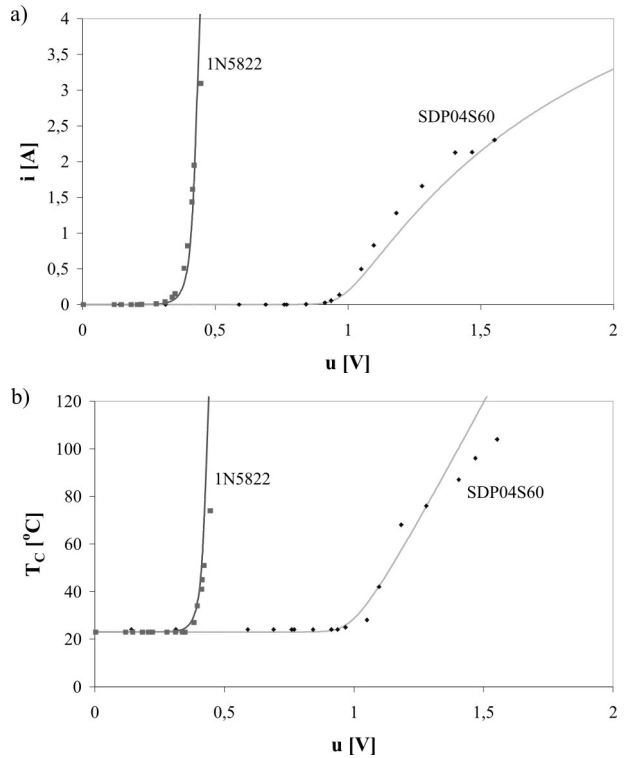


Figure 4: The nonisothermal dc characteristics of the considered Schottky diodes (a) and the dependence of the case temperature of these diodes on their voltage-drop (b)

In Figs.4-5 the nonisothermal dc characteristics of the forward biased diodes (Fig.4) and the transistors in the non-saturation region (Fig.5) are presented. In these figures points denote results of measurements, whereas lines denote results of calculations. As seen, a good agreement between the calculated and measured characteristics was obtained, which confirms high correctness of both the proposed models and the procedure of model parameters values estimation. It is worth mentioning that the voltage drops on the SiC devices switched-on are much greater than on their silicon counterparts. For example, the voltage drop on the forward biased silicon carbide diode is twice higher than on the silicon one. Apart from this, the SiC diode possesses several times higher value of the series resistance than their silicon counterpart. Consequently, the voltage drop on the SiC diode at the forward current equal to 2.5 A is over four times higher than that on the silicon diode.

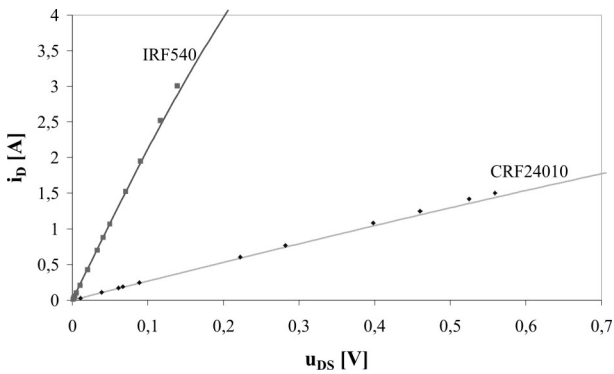


Figure 5: The nonisothermal dc output characteristics of the considered unipolar transistors operating in the non-saturation range

In turn, as it is seen in Fig.5, the slope of the output characteristic $i_D(v_{DS})$ equal to the transistor channel resistance is hardly ten times smaller for the silicon transistor than for the SiC MESFET. This difference of the voltage-drop causes directly much higher energy losses in the switched-on SiC MESFET than in the comparable silicon transistor.

Using the investigated devices, the influence of their properties on the boost converter characteristics was examined.

The investigated boost converter contains: the coil $L = 330 \mu\text{H}$, the capacitor $C = 220 \mu\text{F}$ and three sets of semiconductor switching devices. The first set, called here the converter CONV1, consists of the silicon power MOSFET (IRF540) and the silicon Schottky diode (1N5822). The second set (CONV2) consists of the silicon MOSFET (IRF540) and the SiC-Schottky diode (SDP04560). The third set (CONV3) consists of the power transistor SiC-MESFET (CRF24010) and the SiC-Schottky diode (SDP04560). The control signal, represented in Fig.1 by the voltage source V_{contr} is generated by the monolithic PWM controller (UC3842). The MOSFET transistor is controlled directly by this controller, whereas to control the MESFET transistor the circuit shifting the control voltage [13] is additionally used. During investigations, both the transistors were situated on the heat-sink of dimensions $50 \times 100 \times 10 \text{ mm}$, whereas both the diodes operated without any heat-sink.

Using the electrothermal SPICE models of the considered devices shown in Figs. 2, 3 the characteristics of the boost converter at the steady state were simulated with the use of the analysis method described in [46]. Moreover, such characteristics were measured. The following dependences were considered: the dependence of the output voltage and the watt-hour efficiency of the converter and the case temperature of the semiconductor devices (transistors and diodes) on the input

voltage, the load resistance and the pulse duty factor of the control signal. The investigations were performed at the typical control signal frequency equal to 100 kHz. The output voltage was measured directly using digital voltmeter, the watt-hour efficiency was obtained indirectly based on the measured RMS values of the converter input and output currents and voltages, whereas the case temperatures of the transistor and the diode were measured using the thermo-hunter.

In Figs.6-8 some results of the investigations are presented. In these figures, the results of calculations and measurements are marked by lines and points, respectively. As seen, the obtained characteristics have a very similar shape for all the considered converters - only the quantitative differences between the characteristics are observed.

It is worth mentioning that on the dependence $V_{\text{out}}(d)$ the maximum is observed, whereas the dependence $\eta(d)$ is a monotonically decreasing function. As it was proved in [35] the value of this maximum depends on the on-resistance R_{ON} of the power transistor channel. In the considered case, R_{ON} for the MOSFET is 10 times lower than for the MESFET and the maximum value of the output voltage V_{out} of the converter CONV1 is of about 25% higher than the output voltage of the converter CONV3. This difference causes also the lower value of the watt-hour efficiency of the converter CONV3. On the other hand, the forward voltage-drop of the silicon Schottky diode is much lower than the forward voltage-drop of the silicon carbide Schottky diode. This differences causes, that the case temperature of SiC Schottky diodes operating in the converters CONV2 and CONV3 is much higher than the case temperature of silicon Schottky diode operating in the converter CONV1.

In turn, it results from the dependence $V_{\text{out}}(R_o)$ that the converters CONV1 and CONV2 operate in the continuous conducting mode in all the considered range of changing of the load resistance R_o , whereas the converter CONV3 starts operating in the discontinuing current mode for $R_o > 800 \Omega$. For all the considered converters the increasing functions $V_{\text{out}}(R_o)$ and $\eta(R_o)$ is observed. On the other hand, the case temperatures of the diodes and transistors are the monotonically decreasing functions of the load resistance. The load resistance cannot be lower than 10Ω , because at this value of the resistance R_o , the diode case temperature is nearly the catalogue admissible value. Note, that much higher energy losses existing in the transistors as compared with diodes do not cause the essentially higher values of the transistor internal and case temperatures due to the fact that the value of the diode thermal resistance is of much higher value than the value of the

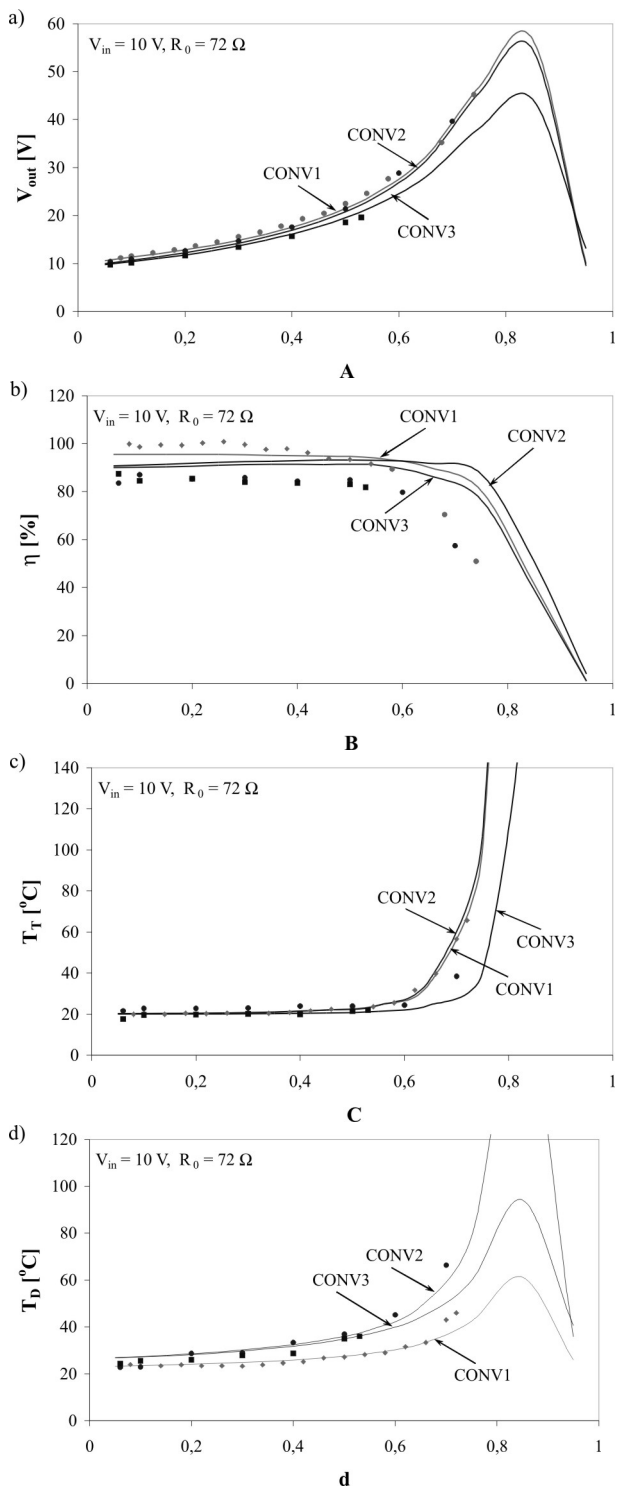


Figure 6: Dependences of the converter output voltage (a), the watt-hour efficiency (b), the transistor case temperature (c) and the diode case temperature (d) on the pulse duty factor d of the control signal

transistor thermal resistance. As it is seen, for all the investigated converters a good agreement between the results of measurements and analyses was obtained for the load resistance $R_0 > 10\ \Omega$, which confirms the correctness of the device models used in the analyses.

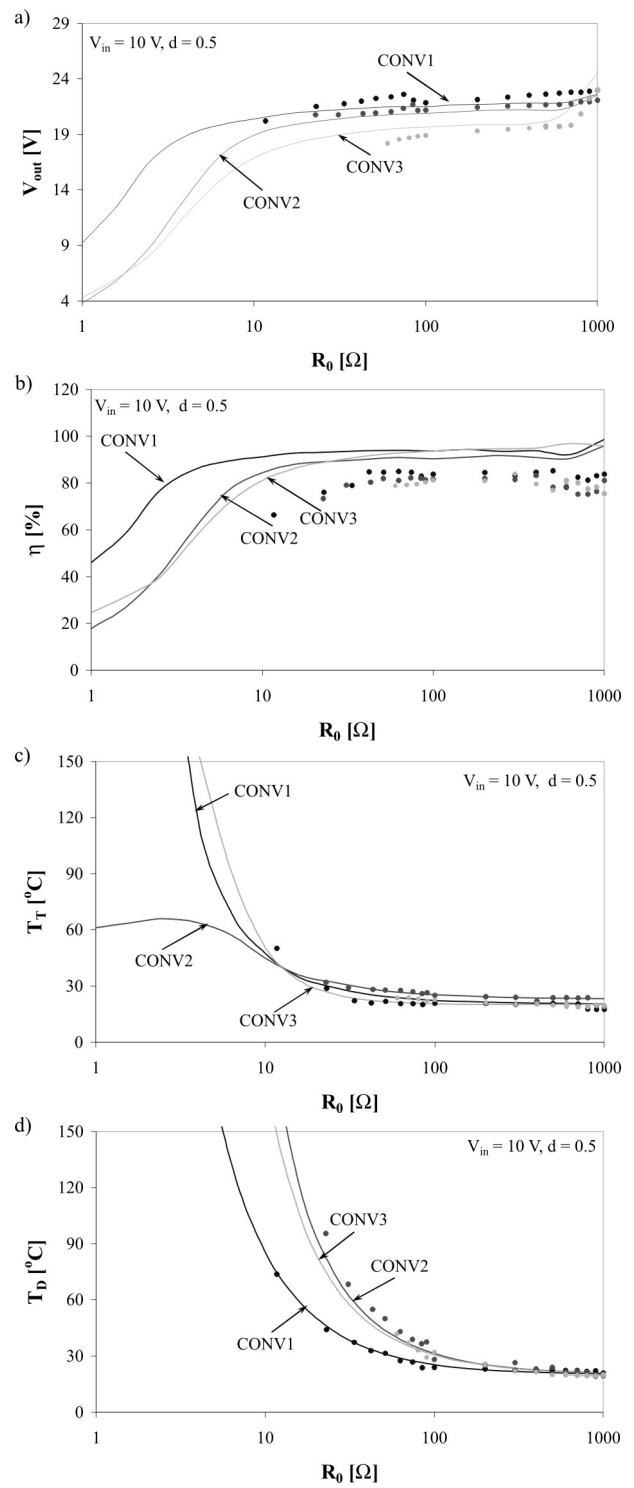


Figure 7: Dependences of the converter output voltage (a), the watt-hour efficiency (b), the transistor case temperature (c) and the diode case temperature (d) on the load resistance

Additionally, the influence of the input voltage of the considered parameters of the boost converter was investigated. The range of change of the converter input voltage was limited by the admissible drain-source voltage of the SiC MEFET. In the range of this voltage

from 3 to 12 V the output voltage of all the investigated converters increase nearly linearly. Note, that the dependences $\eta(V_{in})$, $T_T(V_{in})$ and $T_D(V_{in})$ are the increasing functions too.

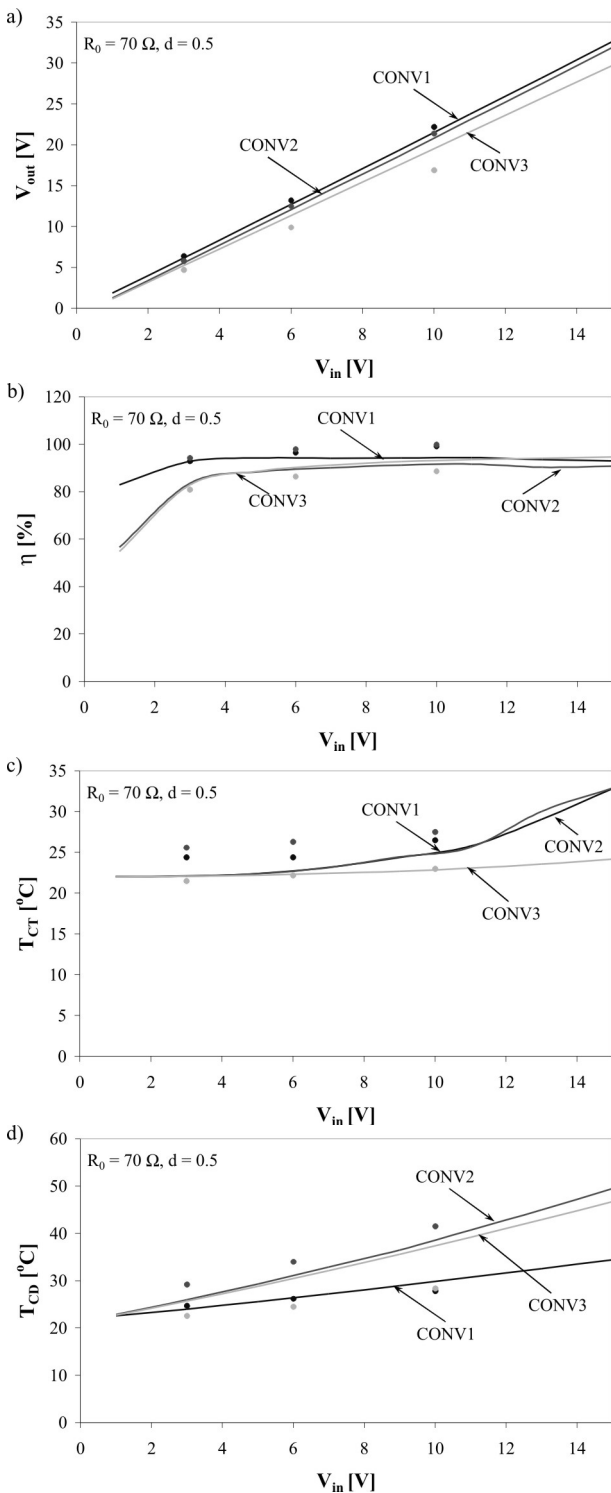


Figure 8: Dependences of the converter output voltage (a), the watt-hour efficiency (b), the transistor case temperature (c) and the diode case temperature (d) on the input voltage

In Figs.6-8 one can observe that the highest values of the converter output voltage and the watt-hour efficiency are observed for the converter CONV1 including silicon devices analysis. On the contrary, the highest values of transistor case temperature are observed for the converter CONV3, whereas the highest value of the diode case temperature was obtained for the converter CONV2. After using the SiC-MESFET, the considerable reduction of the output voltage and the watt-hour efficiency is observed. The described relationships were observed in a wide range of the pulse duty factor of the control signal and in a wide range of load resistance.

4. Conclusions

In the paper the results of the analyses and measurements of the characteristics of the boost converter with silicon and silicon carbide devices are presented. Due to the higher value of the resistance of the switched-on SiC transistor channel and a higher voltage drop on the SiC diode, the converter operating parameters have worse values when silicon devices are used. Therefore, the use of the SiC-devices in low-voltage dc-dc converters is unjustifiable.

The use of the hybrid electrothermal models of Schottky diodes and unipolar transistors allow obtaining a good agreement between the results of the analyses and measurements for all types of semiconductor devices (Si and SiC). This confirms the usefulness of these kinds of models in the analysis of the considered class of converters.

References

1. M. H. Rashid, Power Electronics Handbook, Elsevier, 2007.
2. R. Seyezhai, B.L. Mathur, Design and implementation of interleaved boost converter for fuel cell systems, International Journal of Hydrogen Energy, Vol. 37, No. 4, 2012, pp. 3897-3903.
3. D. Peftitsis, J. Rabkowski, G. Tolstoy, H.-P. Nee, Experimental comparison of dc-dc boost converters with SiC JFETs and SiC bipolar transistors, 14th European Conference on Power Electronics and Applications, EPE 2011; Birmingham, 2011.
4. A. Hensel, C. Wilhelm, D. Kranzer, Development of a boost converter for PV systems based on SiC BJTs, 14th European Conference on Power Electronics and Applications, EPE 2011, Birmingham, 2011.
5. M.M. Hernando, A. Fernández, J. García, D.G. Lamar, M. Rascón, Comparing Si and SiC diode

- performance in commercial AC-to-DC rectifiers with power-factor correction, *IEEE Transactions on Industrial Electronics*, 2006, 53 (2), pp. 705-707.
6. V.P. Galigekere, M.K. Kazimierzczuk, Effect of SiC Schottky and Si junction diode reverse recovery on boost converter, Electrical Insulation Conference and Electrical Manufacturing Expo, EEIC 2007; Nashville, 2007, pp. 294-298.
 7. B. Ray, R.L. Spyker, High temperature design and testing of a DC-DC power converter with Si and SiC devices, 39th Annual Meeting IEEE Industry Applications Society, Seattle, Vol. 2, 2004, pp. 1261-1266.
 8. K. Górecki, J. Zarębski, Modeling Nonisothermal Characteristics of Switch-Mode Voltage Regulators, *IEEE Transactions on Power Electronics*, 23 (4), 2008, pp. 1848 – 1858.
 9. C.N.M. Ho, H. Breuninger, S. Pettersson, G. Escobar, F. Canales, A comparative performance study of an interleaved boost converter using commercialized Si and SiC diodes for PV applications, 8th International Conference on Power Electronics - ECCE Asia: "Green World with Power Electronics", ICPE 2011-ECCE Asia 2011, 2011, pp. 1190-1197.
 10. J. Biela, M. Schweizer, S. Waffler, J.W. Kolar, SiC versus Si - Evaluation of potentials for performance improvement of inverter and DCDC converter systems by SiC power semiconductors, *IEEE Transactions on Industrial Electronics*, Vol. 58 (7), 2011, pp. 2872-2882.
 11. M.G.H. Aghdam, T. Thiringer, Comparison of SiC and Si power semiconductor devices to be used in 2.5 kW dc/dc converter, 2009 International Conference on Power Electronics and Drive Systems, PEDS 2009, Taipei, 2009, pp. 1035-1040.
 12. J. Biela, D. Aggeler, S. Inoue, H. Akagi, J.W. Kolar, Bi-directional isolated DC-DC converter for next-generation power distribution - Comparison of converters using Si and SiC devices, *IEEE Transactions on Industry Applications*, 128 (7), 2008, pp. 901-909.
 13. J. Zarębski, K. Górecki, K. Posobkiewicz, Influence of the use of silicon carbide semiconductor devices on characteristics of buck converters, *Przegląd Elektrotechniczny*, 86 (11a), 2010, pp. 229-231.
 14. J. Rąbkowski, R. Barlik, Three-phase inverter with SiC JFETs and Schottky diodes. *Przegląd Elektrotechniczny*, 86 (11a), 2010, pp. 116-119.
 15. A. Kadavelugu, V. Baliga, S. Bhattacharya, M. Das, A. Agarwal, Zero voltage switching performance of 1200V SiC MOSFET, 1200V silicon IGBT and 900V CoolMOS MOSFET, 3rd IEEE Energy Conversion Congress and Exposition ECCE 2011, Phoenix, 2011, pp. 1819-1826.
 16. A.M. Abou-Alfotouh, A.V. Radun, H.-R. Chang, C. Winterhalter, A 1-MHz hard-switched silicon carbide dc-dc converter, *IEEE Transactions on Power Electronics*, 2006, 21 (4), pp. 880-889.
 17. D. Aggeler, J. Biela, J.W. Kolar, A compact, high voltage 25 kW, 50 kHz DC-DC converter based on SiC JFETs, IEEE Applied Power Electronics Conference and Exposition - APEC 2008, Austin, pp. 801-807.
 18. M. Bhatnagar, B. J. Baliga, Comparison of 6H-SiC, 3C-SiC, and Si for power devices, *IEEE Transactions on Electron Devices*, 1993, 40 (3), pp. 645-655.
 19. R. Singh, J.A. Cooper, M.R. Melloch, T.P. Chow, J.W. Palmour, SiC power Schottky and PiN diodes, *IEEE Transactions on Electron Devices*, 2002, 49 (4), pp. 665-672.
 20. K. Lawson, S.B. Bayne, Transient performance of SiC MOSFETs as a function of temperature, *IEEE Transactions on Dielectrics and Electrical Insulation*, 18 (4), 2011, pp. 1124-1129.
 21. K. Sheng, Maximum junction temperatures of SiC power devices, *IEEE Transactions on Electron Devices*, 2009, 56 (2), pp. 337-342.
 22. P. Friedrichs, Silicon carbide power devices - status and upcoming challenges, *2007 European Conference Power Electronics and Applications*, 2007, pp. 1-11.
 23. T. Funaki, J.C. Balda, J. Junghans, A.S. Kashyap, F.D. Barlow, H.A. Mantooth, T. Kimoto, T. Hikiyara, Power conversion with SiC devices at extremely high ambient temperatures, IEEE Annual Power Electronics Specialists Conference PESC, 2005, pp. 2030-2035.
 24. J. Zarębski, J. Dąbrowski, Investigations of SiC merged pin Schottky diodes under isothermal and non-isothermal conditions, *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, 24 (3), 2011, pp. 207-217.
 25. A. Elasser, T.P. Chow, Silicon carbide benefits and advantages for power electronics circuits and systems, *Proceedings of the IEEE*, 2002, 90 (6), pp. 969-986.
 26. M. Sekikawa, T. Funaki, T. Hikiyara, A study on power device loss of DC-DC buck converter with SiC Schottky barrier diode, 2010 International Power Electronics Conference - ECCE Asia, IPEC 2010, Sapporo, 2010, pp. 1941-1945.
 27. N. Mohan, W.P. Robbins, T.M. Undeland, R. Nilssen, O. Mo, Simulation of Power Electronic and Motion Control Systems – An Overview, *Proceedings of the IEEE*, 82 (8), 1994, pp. 1287-1302.
 28. D. Maksimovic, A.M. Stankovic, V.J. Thottuvelil, G.C. Verghese, Modeling and simulation of power electronic converters, *Proceedings of the IEEE*, 89 (6), 2001, pp. 898-912.

29. Ch. Basso, *Switch-Mode Power Supply SPICE Cookbook*, McGraw-Hill, New York 2001.
30. K. Górecki, J. Zarębski, Electrothermal analysis of the self-excited push-pull dc-dc converter, *Microelectronics Reliability*, 2009, 49 (4), pp. 424-430.
31. K. Górecki, Electrothermal compact model of CoolSET voltage regulators for SPICE, *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, 20 (4), 2007, pp. 181 – 195.
32. M. K. Kazimierczuk, *Pulse-width Modulated DC-DC Power Converters*, John Wiley & Sons, 2008.
33. L.T. Su, D.A. Antoniadis, N.D. Arora, B.S. Doyle, D.B. Krakauer, SPICE model and parameters for fully-depleted SOI MOSFET's including self-heating, *IEEE Electron Device Letters*, 1994, 15 (10), pp. 374-376.
34. K. Górecki, Non-linear average electrothermal models of buck and boost converters for SPICE, *Microelectronics Reliability*, 49 (4), 2009, pp. 431-437.
35. K. Górecki, A New Electrothermal Average Model of the Diode-Transistor Switch, *Microelectronics Reliability*, 48 (1), 2008, pp. 51-58.
36. J. Zarębski, K. Górecki, J. Dąbrowski, Modeling SiC MPS diodes. *Proceedings of the International Conference on Microelectronics, ICM, Sharjah, 2008*, art. no. 5393829 , pp. 192-195.
37. J. Zarębski, D. Bisewski, DC characteristics of the SiC MESFETs, *Proceedings of International Conference Modern Problems of Radio Engineering, Telecommunications and Computer Science, TCSET 2006, Slavske, 2006*, art. no. 4404453 , pp. 87-89.
38. J. Zarębski, K. Górecki, SPICE-aided modelling of dc characteristics of power bipolar transistors with selfheating taken into account, *International Journal of Numerical Modelling Electronic Networks, Devices and Fields*, 22 (6), 2009, pp. 422-433.
39. P.A. Mawby, P.M. Igic, M.S. Towers, Physically based compact device models for circuit modelling applications, *Microelectronics Journal*, 2001, 32 (5-6), pp. 433-447.
40. M.A. Imam, M.A. Osman, A.A. Osman, Simulation of partially and near fully depleted SOI MOSFET devices and circuits using SPICE compatible physical subcircuit model, *Microelectronics Reliability*, 44 (1), 2004, pp. 53-63.
41. J. Zarębski, K. Górecki, The electrothermal large-signal model of power MOS transistors for SPICE, *IEEE Transaction on Power Electronics*, 25 (5-6), 2010, pp. 1265 – 1274.
42. F.N. Masana, SiC Schottky diode electrothermal macromodel, *17th International Conference - Mixed Design of Integrated Circuits and Systems, MIXDES 2010, Wrocław, 2010*, pp. 371-374.
43. E. Schurack, T. Latzel, A. Gottwald, SPICE-simulation of Nonlinear Effects in Filed-Effect-Transistors Caused by Thermal Power Feedback, *IEEE International Symposium on Circuits and Systems ISCAS 1993, Chicago, Vol. 2*, pp. 1116-1119.
44. J. Zarębski, K. Górecki, Influence of semiconductor devices on characteristics of the boost converter, *IX International Conference on Microtechnology and Thermal Problems in Electronics Microtherm 2011, Łódź, 2011*, pp. 279-284.
45. B.M. Wilamowski, R.C. Jaeger, *Computerized circuit Analysis Using SPICE Programs*, McGraw-Hill, New York 1997.
46. J. Zarębski, K. Górecki: A SPICE Electrothermal Model of the Selected Class of Monolithic Switching Regulators. *IEEE Transactions on Power Electronics*, Vol. 23, No. 2, 2008, pp. 1023 – 1026.
47. K. Górecki, J. Zarębski: Influence of MOSFET Model Form on Characteristics of the Boost Converter. *Informacije MIDEM*, 41, (1) 2011, pp. 1-7.

Appendix

The parameter values of the hybrid electrothermal models of the considered diodes and transistors are collected in Tables 1-4.

Table 1: Parameters values of the hybrid electrothermal model of the Si-MOSFET (IRF540)

Parameter name	Level	Gamma	Delta	Eta	Theta	Kappa	Vmax	Xj	Tox	Uo	Phi
Parameter value	3	0	0	0	0	0	0	0	100nm	600 cm ² /V/s	0.6 V
Parameter name	Rs	Kp	W	L	Vto	Rd	Rds	Cbd	Pb	Mj	Fc
Parameter value	16 mΩ	20.71 μA/V ²	0.94 m	2 μm	3.136 V	22 mΩ	444.4 kΩ	2.408 nF	0.8 V	0.5	0.5
Parameter name	Cgso	Cgdo	Rg	Is	N	Tt	R _{ON}	a _{RD}	R _{th}		
Parameter value	1.153 nF/m	445.7 pF/m	5.557 Ω	2.859 pA	1	142 ns	38 mΩ	0.012 K ⁻¹	12 K/W		

Table 2: Parameters values of the hybrid electrothermal model of the Si-Schottky diode (1N5822)

Parameter name	Is	Rs	Ikf	N	Xti	Eg	Cjo	M
Parameter value	100 nA	34.63 mΩ	2.37 A	1	0	1.11 V	1.032 nF	0.6736
Parameter name	Vj	Fc	Isr	Nr	a _u	a _{rs}	R _{th}	
Parameter value	0.75 V	0.5	9.599 mA	2	-2 mV/K	0.003 K ⁻¹	60 K/W	

Table 3: Parameters values of the hybrid electrothermal model of the SiC-Schottky diode (SDP04S60)

Parameter name	IS	RS	IKF	N	XTI	EG	BV	IBV	ISR
Parameter value	0.27 fA	190 mΩ	0	1.099	2.2	1.319 V	670 V	0.2 A	1.9 pA
Parameter name	NBV	NR	VJ	M	TRS1	TRS2	α _{rs}	α _u	R _{th}
Parameter value	1500	2.36	0.75 V	1	0.004 K ⁻¹	30x10 ⁻⁶ K ⁻²	0.005 K ⁻¹	-1.5 mV/K	30 K/W

Table 4: Parameters values of the hybrid electrothermal models of the SiC-MESFET (CRF24010)

Parameter name	Level	B	ALPHA	VTO	LAMBDA	BETA	VTOTC	RD	RS	RG	IS
Parameter value	2	26.6 V ⁻¹	0.135 V ⁻¹	-13.84 V	0.0085 V ⁻¹	0.5 A/V ²	-0.002 V/K	0.17 Ω	0.1 Ω	10 Ω	70 fA
Parameter name	N	CGS	CGD	CDS	VBI	VMAX	VDELTA	R _{ON}	α _{RD}	R _{th}	
Parameter value	1.25	6.7 pF	0.3 pF	1.3 pF	1.8 V	0.1 V	3 V	0.37 Ω	0.006 K ⁻¹	10 K/W	

Arrived: 16. 08. 2012

Accepted: 15. 10. 2012

Ultra Low-Power Low-Complexity Tunable 3–10 GHz IR-UWB Pulse Generator

Laszlo Nagy, Jelena Radic*, Alena Djugova, Mirjana Videnovic-Misic

Department for Power, Electronics and Communications Engineering, Faculty of Technical Sciences, University of Novi Sad, Novi Sad, Serbia

Abstract: A new very low power impulse radio ultra-wideband (IR-UWB) pulse generator is investigated in the paper. The low complexity and tunable architecture is composed of a glitch generator, a switched ring oscillator, a two-stage energy efficient buffer and a pulse shaping filter (two versions). It is designed and simulated in low-cost 0.18 μm UMC CMOS technology. Post-layout simulation results showed spectrum that covers whole UWB band and fully complies with the corresponding FCC spectral mask. The pulse duration is around 0.5 ns, and the peak-to-peak amplitude is 211 mV on 50 Ω output load. Since the impulse radio-based generator operates in burst mode with low duty cycle, it has ultra low power consumption of 0.89 mW corresponding to energy consumption of 8.9 pJ per pulse for 100 MHz pulse repetition frequency (PRF). For the output filter with additional off-chip inductor and PRF of 200 MHz, Power Spectral Density reaches the maximum value of -41.33 dBm/MHz at 6.4 GHz, consuming average power of 2 mW. The peak-to-peak amplitude in this case is 250 mV with pulse duration of around 0.75 ns. The chip occupies very small area of only $558 \times 556 \mu\text{m}^2$ mainly due to simple pulse generator architecture.

Key words: CMOS technology, impulse radio ultra-wideband (IR-UWB) communications, pulse generator, radio frequency integrated circuits (RFIC), ultra-wideband systems.

Enostaven in spremenljiv 3–10 GHz IR-UWB pulzni generator nizke moči

Povzetek: V članku je obravnavan ultra-širokopasovni (IR-UWB) pulzni generator z impulzi zelo nizkih moči. Enostavno in spremenljivo arhitekturo sestavljajo generator motečih impulzov, preklopni zankasti oscilator, dvostopenjski energijsko učinkovit ojačevalnik in filter za oblikovanje impulzov (v dveh različicah). Načrtovan in simuliran je na nizkocenovni 0.18 μm UMC CMOS tehnologiji. Rezultati simulacij so prikazali spekter, ki pokriva celotno nizko UWB območje in popolnoma ustreza ustreznim FCC maski. Dolžina impulza je okoli 0.5 ns z vrh-vrh amplitudo 211 mV pri 50 Ω bremenu. Kljub kontinuitetnemu delovanju generator izkazuje zelo nizko porabo 0.89 mW, kar ustreza porabi energije 8.9 pJ na impulz pri ponavljajoči frekvenci (PRF) 100 MHz. Pri 200 MHz spektralna gostota moči doseže maksimum -41.33 dBm/MHz pri 6.4 GHz in porabi 2 mW. V tem primeru je vrh-vrh amplituda 250 mV in dolžina impulza 0.75 ns. Čip zaseda le $558 \times 556 \mu\text{m}^2$ prostora, kar je posledica enostavne arhitekture pulznega generatorja.

Ključne besede: CMOS tehnologija, pulzna radio ultra-širokopasovna (IR-UWB) komunikacija, pulzni generator, integrirano vezje radijskih frekvenc (RFIC), ultra-širokopasovni sistemi.

* Corresponding Author's e-mail: jelenar_@uns.ac.rs

1. Introduction

Since the Federal Communications Commission (FCC) allocated the 3.1 – 10.6 GHz unlicensed spectrum for commercial ultra wideband (UWB) application in February 2002, several technologies have been developed to satisfy the communication market requirements [1]. Multiband orthogonal frequency division multiplexing (MB-OFDM) UWB and direct-sequence (DS) UWB protocols are mainly focused on the high data rate commu-

nications such as streaming multimedia applications. However, these techniques do not utilize efficiently the whole UWB frequency range (3.1 – 10.6 GHz) because they divide it into several sub-bands/channels in system design [2], [3]. This reduces the data throughput capacity and demands complex digital-signal processing, modulation and deep compression for achieving necessary data rate. As the carrier-based transmission approaches require mixers and power amplifiers (usually noisy, power hungry and complex blocks), such UWB

transceivers apparently increase the complexity, power and costs of the UWB chip. Impulse Radio Ultra Wide Band (IR-UWB) technique is a carrier-less approach that transmits extremely short pulses (pulse duration is less than 1 ns) occupying the full UWB frequency spectrum. It has advantageous features such as low complexity (without mixer and power amplifier), low-cost and energy efficient UWB transmitter architecture allowing simple modulation scheme (e.g. on-off keying – OOK). Additionally, the protocol offers high fading margin for communication systems in multipath environments [4]. The IR-UWB appears to be good candidate for very high data rate short-range communication, and low data rate communication related to localization or/and positioning systems [5], [6]. Nowadays, it is mostly used in the IEEE 802.15.3a high data rate and IEEE 802.15.4a low data rate standards, sensor networks, tag networks and biomedical applications.

A pulse generator plays the core role in an IR-UWB system design because it produces pulse train which spectrum, with sufficient power level, has to satisfy all FCC requirements. Therefore, it is extremely challenging to design UWB transmitter that satisfies such difficult demands while achieving low-power and high-throughput operation to enable low-cost systems. Recently reported UWB pulse generators have generally used all-digital [7 – 9], analogue-digital [10] or all-analogue [10], [11] design approach. Digital solutions offer higher integration, lower power consumption and better controllability whereas all-analogue techniques demonstrate circuit simplicity. In some cases, the all-digital architectures require power amplifier (PA) at the output to provide sufficient signal strength increasing the total power consumption and further degrading system complexity by introducing additional PA design constraints. The analogue designs that generate the UWB pulses by LC resonant circuits require considerable die area, making these architectures less suitable for area constrained applications. The slow transient response of the pulsed LC oscillators restricts the bandwidth and the pulse amplitude, as the oscillation is not able to settle sufficiently in a short time.

In this paper, a new low-power and low-complexity pulse generator, addressing the whole FCC spectrum band, is proposed. The presented topology, designed in low cost 0.18 μm UMC CMOS technology, is analyzed in Section III. Due to not high enough speed of CMOS inverters available in the used technology, it was necessary to increase the ring oscillator frequency by introducing negative feedback in each inverter stage. One of them was chosen even to be variable to provide adjustment of the output signal central frequency. Post-layout simulations results are given in Section IV followed by discussion and comparison with the other

published pulse generator designs. The Section V concludes the paper.

2. FCC spectral mask and UWB pulse design

The UWB transmitter power level in the FCC allocated frequency range (3.1 – 10.6 GHz) should be lower than -41.3 dBm/MHz [1], in order not to interfere with the already existing communication systems such as WiMax, Bluetooth and GSM. In the GPS band (0.96 – 1.61 GHz), there is even more stringent regulation: less than -75.3 dBm/MHz is needed to avoid interference problem. The Power Spectral Density (PSD) in frequency interval from 1.61 GHz to 3.1 GHz depends on the type of application (indoor, outdoor, GPS, wall & medical imaging, through-wall imaging & surveillance system). Fig. 1 shows the FCC mask for the indoor and outdoor UWB communications (including the Part 15 limit) [1] that pulse spectrum has to meet.

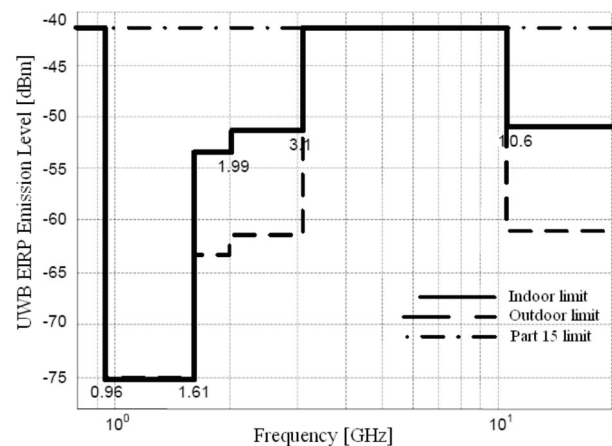


Figure 1: The FCC indoor and outdoor mask for UWB [1].

The FCC rules define only the frequency bands and the radiated PSD but there are no requirements on the time-domain wave shape. However, as the shape of the pulse generator signal determines its spectrum characteristic and effectively dictates specific system (UWB transmitter) requirements, its generation is one of the essential considerations in the UWB design. Pulse shapes usually used in the impulse radio UWB technology are based on the Gaussian pulse and its derivatives. For indoor systems, the 5th or higher order derivative of the Gaussian pulse should be used to comply with the allocated indoor spectrum mask [8].

3. Proposed IR-UWB pulse generator design

The proposed topology is shown in Fig. 2. It is composed of a glitch generator, a switched oscillator, a two-stage buffer, and a pulse shaping filter. Two versions of the output filter (without and with off-chip inductor L_b) are presented in Fig. 3. It should be noted that enhancement-mode transistors have been used in the design.

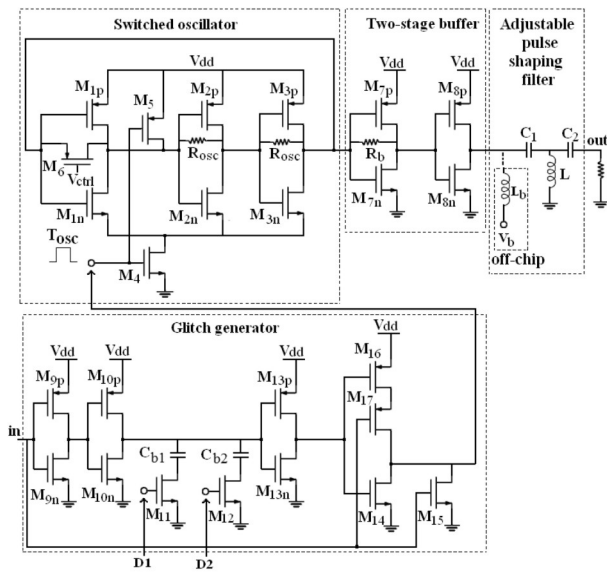


Figure 2: Proposed IR-UWB pulse generator.

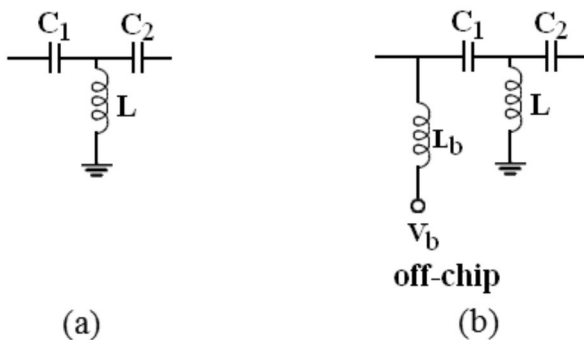


Figure 3: Two versions of pulse shaping filter: (a) without off-chip inductor L_b , and (b) with off-chip inductor L_b .

The switched oscillator consists of a three-stage ring oscillator, (inverter stages $M_1 - M_3$), two feedback resistors R_{osc} , a control transistor M_6 , and a pair of oscillation-enabling switches (transistors M_4 and M_5). The ring oscillator is one of the most commonly used topology in the pulse generator design due to its simple architecture occupying small chip area (without passive components). Furthermore, it offers fast transient response as it has short start-up time and small resistance at each

inverter feedback nod. The resistors R_{osc} feedbacks in the second and third inverter stage, increase the ring oscillating frequency by decreasing the input (Miller) capacitance [12]. PMOS transistor M_6 is used for the frequency tuning to enable compensation due to the process-voltage-temperature (PVT) variations and additional spectrum fitting within the FCC spectral mask [12]. This can be accomplished by changing the transistor M_6 gate control voltage V_{ctrl} .

The oscillation-enabling switches control the oscillation process in accordance with the T_{osc} signal state (produced by the glitch generator). The ring oscillator is turned on by transistor M_4 at the T_{osc} signal rising edge, and the inverter stages output voltage values are determined by the size ratio of the corresponding PMOS and NMOS transistors. The transistor M_4 is switched off and transistor M_5 is switched on while the T_{osc} signal is "low". During this interval, the inverter stages are turned off, while the transistors M_6 (operating in linear region) and M_5 connect the ring oscillator output (the buffer input) to supply voltage. The exact voltage value of the nod (1.6 V) is determined by the voltage divider consisting of four resistors in series: resistor R_b and channel resistances of transistors M_5 , M_6 , and M_{7n} . This results in negligible power consumption of the first buffer stage having output voltage close to zero. As M_{8n} transistor is turned off, the power consumption of the second buffer stage can also be neglected minimizing the total power consumption. Since the M_1 transistor output (the M_2 transistor input) is connected to V_{dd} by the transistor M_5 , at the next rising edge of the T_{osc} signal the oscillation starts from the same initial state.

It can be noticed that the ring oscillator output signal length and thus its bandwidth are approximately defined by the duration of the T_{osc} signal. The shorter the control impulse, the wider the output signal bandwidth is obtained. To cover the whole FCC frequency range (3.1 GHz – 10.6 GHz), the T_{osc} signal should be short and narrow (duration less than 1 ns). As a microcontroller could not produce such a short signal, the oscillation-enabling pulse is created by the glitch generator considering the input trigger *in* signal usually controlled by a microcontroller. The glitch generator consists of three inverters, a digitally controlled capacitor bank and a NOR gate. The duration of the generated signal is determined by the digitally controlled capacitor bank, composed of capacitors C_{b1} and C_{b2} , and transistor switches M_{11} and M_{12} . To provide sharp both rising and falling edge of produced signal, the capacitor bank was introduced between the inverter stages. Digital signals D_1 and D_2 switch off/on adequate capacitors determining the total bank capacitance that is directly proportional to the T_{osc} signal duration. This provides indirectly control of the pulse generator output signal

length and bandwidth. By the bank capacitance digitally tuning, the duration of the control signal can be adjusted from 250 ps to 660 ps.

The two-stage buffer isolates the ring oscillator from the high-pass filter load (the inductor L and two capacitors C_1 and C_2 , Fig. 3a) and improves the pulse generator current driving capability. The first buffer stage has small gain and low input impedance due to resistive feedback used to increase the ring oscillator frequency. The second stage prevents this effect to change the output filter shaping characteristics and simultaneously amplifies the signal. Although the buffer seems to be some kind of output power amplifier, it does not endanger the IC design requirements as it occupies very small area and has negligible power consumption. The off-chip inductor L_b connected to constant voltage (the second type of the output filter presented in Fig. 3b) is used only in case better suppression at low frequencies is required. For its realization, a bond-wire can be used. It can be noticed that this inductor could be integrated on chip to create the on-chip band-pass filter, but this would increase the die-area and thus the fabrication costs.

4. Post-layout simulation results and comparison

The proposed topology has been designed in mixed mode/RF UMC 0.18 μm CMOS technology with supply voltage of 1.8 V. Simulations have been performed using SpectreRF Simulator from Cadence Design Environment. It should be emphasized that this software is one of the most commonly used for IC design. In order to perform post-layout simulations, the Assura (Cadence parasitic extractions) tool has been used. Furthermore, the obtained results have been checked with Calibre (Mentor Graphics) tool as well.

Since one of the portable system's biggest issues is battery life, the pulse generator was optimized with the main aim to minimize the power consumption and meet efficiently the FCC spectrum demands while still keeping acceptable values for remaining Figures of Merits (FOMs). Regarding the circuit's spectrum characteristics or the spectrum center frequency, the main problem was limited set of transistor sizes available in the used technology as the ring oscillator frequency depends directly on transistors sizes. The period of the oscillation T rises proportionally with increase in transistors sizes, while the oscillating frequency decreases ($f_0=1/T$). For the standard three-stage ring oscillator design with the smallest NMOS transistors ($W/L=25\ \mu\text{m}/0.18\ \mu\text{m}$) and approximately two times larger

PMOS transistors ($W/L=45\ \mu\text{m}/0.18\ \mu\text{m}$), the oscillation frequency of 3.77 GHz has been obtained. Although the resistive feedbacks have been used in the ring oscillator and the first buffer stage to increase the oscillating frequency, its value has not been large enough to utilize efficiently the whole UWB band in the spectrum domain. Therefore, a new approach of the pulse generation is proposed to overcome the technology constraint. The output high-pass filter frequency has been chosen to have around two times higher value than the ring oscillating frequency and the signal with the spectrum center frequency (6.25 GHz) in the middle of the UWB range has been obtained (shown in Fig. 4). It can be seen that spectrum covers the whole UWB frequency band and fully complies with the FCC spectral mask. The post-layout simulation results for the generated UWB pulse in the time domain is given in Fig. 5. The pulse duration is around 0.5 ns and the peak-to-peak amplitude V_{pp} on a 50 Ω output load is 211 mV. The pulse generator operates in burst mode with low duty cycle and pulse repetition frequency (PRF) of 100 MHz, and thus has very low power dissipation. The average power consumption including the glitch generator, the buffer stages and the filter is only 0.89 mW, corresponding to 8.9 pJ energy consumption per pulse (for the PRF of 100 MHz). In general, the nature of the IR-UWB communication allows saving power between every two adjacent pulses and consuming power just at the moment when the pulse is generated.

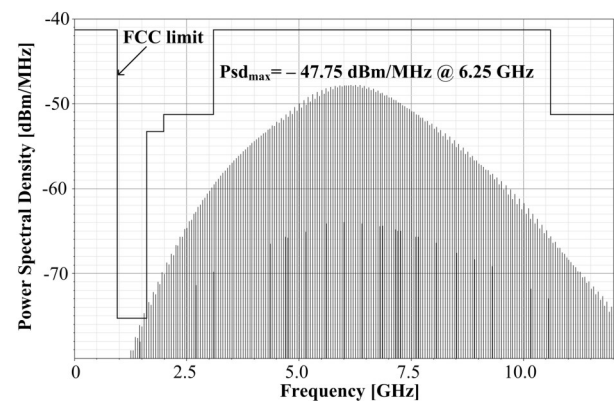


Figure 4: Post-layout simulations of the output signal in the spectral domain.

The circuit components values and transistors sizes are given in Table 1 and 2, respectively. The transistors channel length, fixed by the manufacturing process, is 0.18 μm .

Since transistors are made as multi-finger devices, the total transistors gate width is calculated by $W=ng\cdot 5\ \mu\text{m}$, where 5 μm represents the gate finger width, and parameter ng , the gate finger number, is in the range from 5 to 21. Additional technology recommendation

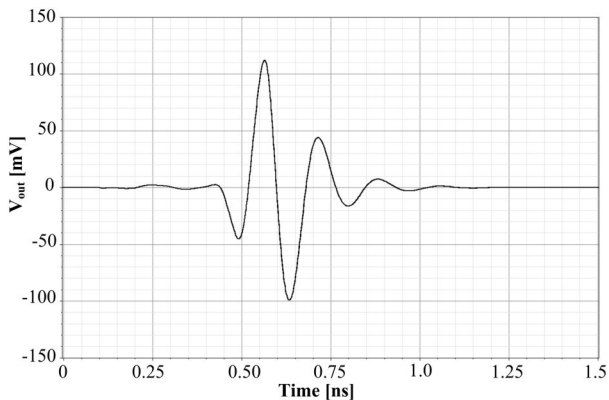


Figure 5: Post-layout simulation of the output signal in the time domain.

Table 1: Values of the circuit components.

Component	Rosc	Rb	C1	C2	L	Cb1	Cb2
Value	530 Ω	1500 Ω	0.20 pF	0.13 pF	1.6 nH	1 pF	2 pF

Table 2: Transistors sizes.

Transistor	M1-3n	M1-3p	M4	M5	M6	M7,8n	M7,8p	M9,10n	M9,10p	M11	M12	M13n,p	M14,15	M16,17
Width [μm]	25	45	105	35	25	25	45	25	25	75	95	25	25	75

is to use only odd values for parameter ng . It can be noticed that transistor M_6 has the largest size because it has to provide enough current for the three-stage ring oscillator.

The photograph of the pulse generator layout is shown in Fig. 6. The integrated circuit (IC) occupies a die area

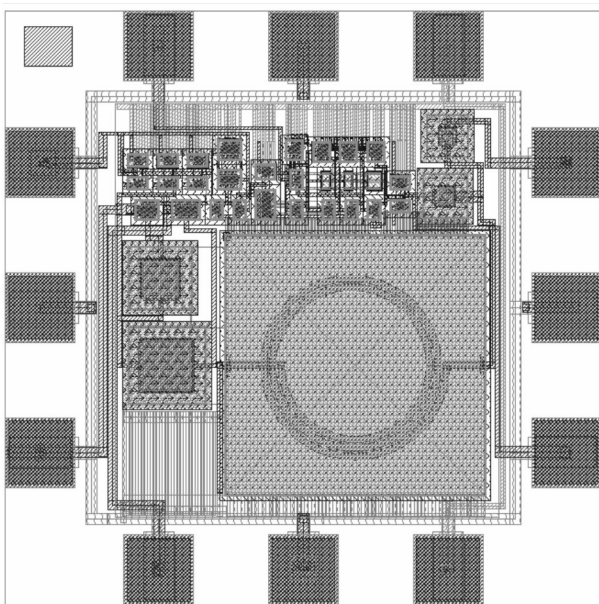


Figure 6: Photograph of the IR-UWB pulse generator layout.

of $558 \times 556 \mu\text{m}^2$ including bonding pads, and the active circuit area is only $352 \times 378 \mu\text{m}^2$. It supports the on-off keying (OOK) modulation. This type of the modulation is chosen because of its simplicity and thus less complex transmitter realization.

It can be seen from Fig. 4 that the pulse generator PSD must be lower than the maximum value allowed by the FCC due to very large bandwidth to avoid emission in the forbidden frequency band around 1 GHz. Moreover, even wider bandwidth can be achieved with smaller value of bank capacitance in the glitch generator, but the lower part of the FCC mask would be slightly unsatisfied. To overcome the problem of emission at frequencies around 1 GHz, the off-chip inductor L_b is added in

the output filter (Fig. 3b, or shown with dashed line in Fig. 2). The post-layout simulation results (in time and spectrum domain) for $L_b = 2.3 \text{ nH}$ and $V_b = 0.25 \text{ mV}$ are shown in Figs. 7 and 8. It can be observed that the signal spectrum is significantly improved (flatter response and higher 10 dBm bandwidth have been obtained). Furthermore, the spectrum components at lower frequencies close to the most critical band around 1 GHz are suppressed as expected. The pulse duration is about 0.75 ns with the V_{pp} parameter of 248 mV. There was a small increase in the power consumption 1.41 mW (corresponding to energy consumption of 14.1 pJ/pulse). However, this does not represent a problem as the ef-

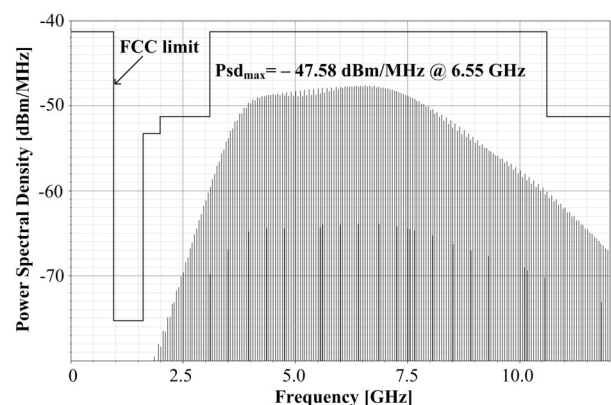


Figure 7: Pulse generator spectrum in the case of the output band-pass filter includes the off-chip inductor L_b .

efficiency remained the same (the total signal power was also increased). Additionally, in the case of the pulse generator signal power around the maximum allowed value is required, the spectrum value can be enlarged by increasing the PRF. The pulse generator PSD for the pulse repetition frequency of 200 MHz is given in Fig. 9. It can be seen that the FCC spectrum mask is fully satisfied with the maximum PSD of -41.33 dBm/MHz at 6.4 GHz. The energy consumption is a little decreased and is around 10 pJ/pulse.

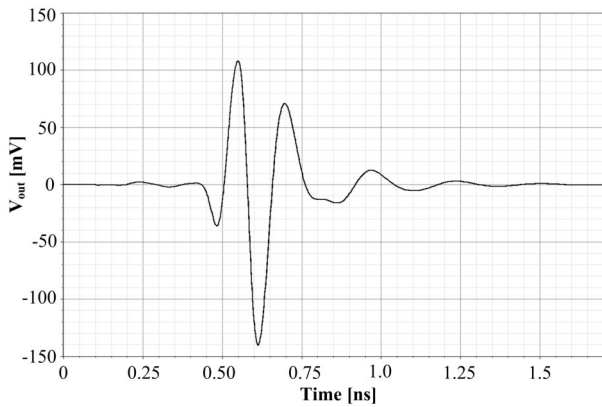


Figure 8: Pulse generator time response in the case of the output band-pass filter includes the off-chip inductor L_b .

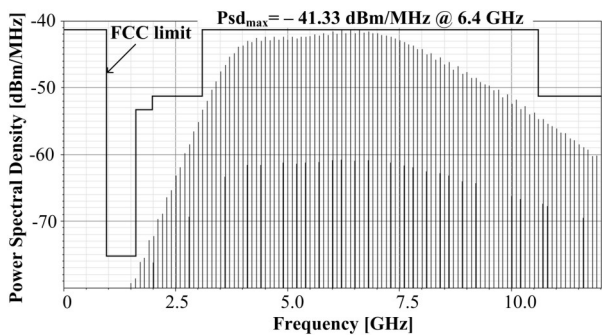


Figure 9: Pulse generator PSD in case $PRF=200$ MHz.

Table 3: Performance comparison of the IR-UWB pulse generators.

Reference	Power cons. [mW]	BW (-10 dB) [GHz]	V _{pp} [mV]	Pulse width [ns]	Die area [mm ²]	PRF [MHz]	Technology
/13/	N/A	3.1 – 10.6	68	0.45	0.27	200	90 nm CMOS
/14/	27.0	3.6 – 10.2	127	0.31	N/A	50	0.18 μm BiCMOS
/15/	3.8	3.0 – 6.0	150	0.5 – 0.9	0.44	910	0.13 μm CMOS
/16/	23.0	N/A	300	0.75	0.50	50	0.18 μm CMOS
This work*	2.0	3.1 – 10.6	250	0.75	0.31	200	0.18 μm CMOS
This work**	0.89	3.3 – 9.3	211	0.50	0.31	100	0.18 μm CMOS

* with the off-chip inductor L_b .

** without the off-chip inductor L_b .

Table 3 summarizes the performance of the proposed IR-UWB pulse generator compared to the FOMs of the recently published works. Although, it can be difficult to make fair comparisons when different specifications and technologies are used, it is clear that the proposed circuit is more efficient than the other design as it has by far the lowest power consumption and the peak-to-peak amplitude higher than in Refs [13], [14], and [15]. The pulse generator presented in Ref [16] has higher V_{pp} parameter, but consumes significantly more power compared to the presented design. Other FOM achieved in the work are comparable to the results given by the authors. The proposed architecture is suitable for low voltage and ultra-low power UWB wireless applications.

5. Conclusion

A new energy-efficient tunable pulse generator is developed in 0.18 μm UMC CMOS technology for high data rate 3.1 – 10.6 GHz UWB applications. The time and spectrum domain signal adjustment is proved by applying the adequate PMOS gate control voltage and tuning capacitance of the digitally controlled capacitor bank. Additional spectrum suppression at lower frequency (especially in the 1 GHz to 1.6 GHz band where tight limits are imposed for GPS systems) is enabled with the off-chip inductor inserted. The post-layout simulation results demonstrate that the proposed ring oscillator-based architecture has significantly lower power consumption compared to the previously reported UWB pulse generators. Moreover, it was shown that the design has high peak-to-peak amplitude and small chip area.

Acknowledgments

This work was supported in part by the Ministry of Education and Science, Republic of Serbia (the project

contract No. III-43008) and by FP7 project (contract No. 256615).

References

1. First Report and Order: Revision of Part 15 of the Commission's Rules Regarding Ultra-Wideband Transmission Systems Federal Communications Commission (FCC), ET Docket 98-153, Adopted February 14, 2002, Released Apr. 22, 2002.
2. Multi-Band OFDM Physical Layer Proposal for IEEE 802.15 Task Group 3a, IEEE P802.15-03/268r2, Sep. 14, 2004.
3. DS-UWB Physical Layer Submission to 802.15 Task Group 3a, IEEE P802.15, Mar. 2004.
4. J. R. Fernandes and D. Wentzloff, "Recent Advances in IR-UWB Transceivers: An Overview", Proceedings of the IEEE International Symposium on Circuits and Systems, pp. 3284–3287, 2010.
5. M. Ghavami, L. B. Michael, and R. Kohno, Ultra Wideband Signals and Systems in Communications Engineering, John Wiley&Sons Ltd, 2004.
6. K. Siwiak and D. McKeown, Ultra-Wideband Radio Technology, John Wiley&Sons Ltd, 2004.
7. V. V. Kulkarni, M. Muqsith, K. Niitsu, H. Ishikuro, and T. Kuroda, "A 750 Mb/s, 12 pJ/b, 6-to-10 GHz CMOS IR-UWB transmitter with embedded on-chip antenna", IEEE Journal of Solid-State Circuits vol. 44, no. 2, pp. 394–403, 2009.
8. H. Kim, Y. Joo, and S. Jung, "A tunable CMOS UWB pulse generator", Proceedings of the IEEE International Conference on Ultra-Wideband, pp. 109–112, 2006.
9. P.P. Mercier, D. C. Daly, and A. P. Chandrakasan, "An Energy-Efficient All-Digital UWB Transmitter Employing Dual Capacitively-Coupled Pulse-Shaping Drivers", IEEE Journal of Solid-State Circuits, vol. 44, no. 6, pp. 1679–1688, 2009.
10. S. Sim, D. W. Kim, and S. Hong, "A CMOS UWB pulse generator for 6–10 GHz applications", IEEE Microwave and Wireless Components Letters, vol. 19, no. 2, pp. 83–85, 2009.
11. O. Novak, and C. Charles, "Low-power UWB pulse generators for biomedical implants", Proceedings of the IEEE International Conference on Ultra-Wideband, pp. 778–782, 2009.
12. J. Radic, A. Djugova, L. Nadj, and M. Videnovic-Misic, "Feedback Influence on Performance of Ring Oscillator for IR-UWB Pulse Generator in 0.18um CMOS technology", Proceedings of the IEEE 28th International Conference on Microelectronics, pp. 357–360, 2012.
13. J.C. Li, S. Jung, and H. Moon, "A Fully Integrated 3-10 GHz IR-UWB CMOS Impulse Generator", Microwave and Optical Technology Letters, vol. 53, no. 8, pp. 1887–1890, 2011.
14. J.C. Li, S. Jung, M. Lu, P. Gui, and Y. Joo, "A Current-Steering DAC-Based CMOS Ultra-Wideband Impulse Generator", Proceedings of the IEEE International Conference on Communications and Information Technology, pp. 971–975, 2009.
15. A.M. El-Gabaly, C.E. Saavedra, "A 5-GHz energy-efficient tunable pulse generator for ultra-wideband applications using a variable attenuator for pulse shaping", International Journal of Circuit Theory and Applications, doi: 10.1002/cta.792, 2011.
16. J. He, Y.P. Zhang, W.M. Lim, Y.Z. Xiong, "A fully integrated differential impulse radio transmitter", Analog Integrated Circuits and Signal Processing, vol. 70, no. 1, pp. 47–56, 2012.

Arrived: 13. 09. 2012

Accepted: 09. 11. 2012

Electrical excitation and mechanical vibration of a piezoelectric cube

Oumar Diallo¹, E. Le Clezio², M. Lethiecq¹, G. Feuillard¹

¹ Laboratoire GREMAN UMR CNRS 7347. École Nationale d'Ingénieurs du Val de Loire, Université François Rabelais de Tours, Rue de la Chocolaterie BP 3410 41034 BLOIS, CEDEX, France

² Institut d'Electronique du Sud UMR CNRS 5214 IES - MIRA case 082, Université Montpellier 2 Place Eugène Bataillon, 34095 MONTPELLIER CEDEX 5, France

Abstract: This work deals with the electromechanical power conversion in piezoelectric materials. In this study we will use the reverse piezoelectric effect to determine the tensorial properties of piezoelectric ceramics. The eigen vibration modes of a piezoelectric cube are modelled and characterized using resonant ultrasound spectroscopy. This method, which examines the vibration modes of a piezoelectric cube, relates mechanical resonances that can be measured by Laser interferometry to electromechanical properties. The direct problem is first solved; the resonance modes of a piezoelectric cube are modelled and mechanical displacements are calculated as functions of frequency and boundary conditions. Because the geometry of the sample is fixed, the vibrations depend only on the material properties and the electrical excitation. The displacement response of a PMN-34.5PT piezoelectric ceramic cube is investigated using a coherent optical detection. According to properties determined by electrical impedance measurements, the cube presents a first resonance around 125 kHz. Results on the amplitude of the detected velocities versus the frequency of the input excitation voltage are reported and compared to theoretical predictions. This validates the electrical modelling of the cube vibrations.

Key words: Vibration-Piezoelectricity-Spectroscopy-Eigen-frequency-Materials

Električno vzbujanje in mehanske vibracije piezoelektrične kocke

Povzetek: Delo obravnava elektrokemijsko pretvorbo energije v piezoelektričnih materialih. Za določevanje tenzijskih lastnosti piezoelektričnih keramik je uporabljen obraten piezoelektričen efekt. Načini eigenovih vibracij piezoelektrične kocke so modelirani in karakterizirani z resonančno ultrazvočno spektroskopijo. Ta metoda preko merljive mehanske resonancije z lasersko interferometrijo ugotavlja elektromehanske lastnosti. Modelirani so resonančni načini piezoelektrične kocke. Mehanični premiki so računani kot funkcija frekvence in robnih pogojev. Zaradi fiksne geometrije vzorca so vibracije odvisne le od lastnosti materiala in električne vzbujenosti. Odziv premika pmn-34.5pt piezoelektrične keramične kocke je raziskan s pomočjo koherentne optične detekcije. Prva resonančna frekvenca kocke 125 kHz je določena s pomočjo impedančnih meritev lastnosti kocke. Rezultati amplitude detektiranih hitrosti glede na frekvenco vzbujevalne napetosti so predstavljeni in primerjani s teoretičnimi ocenami, kar potrjuje električen model vibracij kocke.

Ključne besede: vibracije, piezoelektričen efekt, spektroskopija, eigen, frekvenca, materiali

* Corresponding Author's e-mail: oumar.diallo@univ-tours.fr

1. Introduction

Several models of one-dimensional vibrations of a piezoelectric sample can be found in the literature, such as Mason's [1] and KLM [2] which can predict the electromechanical behaviour of a piezoelectric material. However, these methods are not applicable for a 3D specimen such as a cube. Until now, conventional techniques use several samples for parameter identifications [3]. Recently, Delaunay *et al.* proposed an

ultrasonic characterization method allowing the determination of these properties using a single sample. This method, referred to as Resonant Ultrasound Spectroscopy [4], examines the vibration modes of a piezoelectric cube and relates mechanical resonances measured by Laser interferometry to electromechanical properties. This method is here modified to obtain the electromechanical properties taking into account

the boundary conditions. First the eigenfrequencies of a piezoelectric cube with two electrodes are calculated and compared to the eigenfrequencies of the same piezoelectric cube with only one electrode and of the sample with no electrode. Then, the velocity spectra are calculated and compared to experimental results.

2. Lagrangian minimization

From classical mechanics the general form of a Lagrangian L is expressed as:

$$L = \iiint_V (E_c - E_{def} - E_p - E_e) dV \quad (1)$$

where E_c is the kinetic energy, E_{def} is the deformation energy, E_p is the potential energy and E_e is the electrostatic energy.

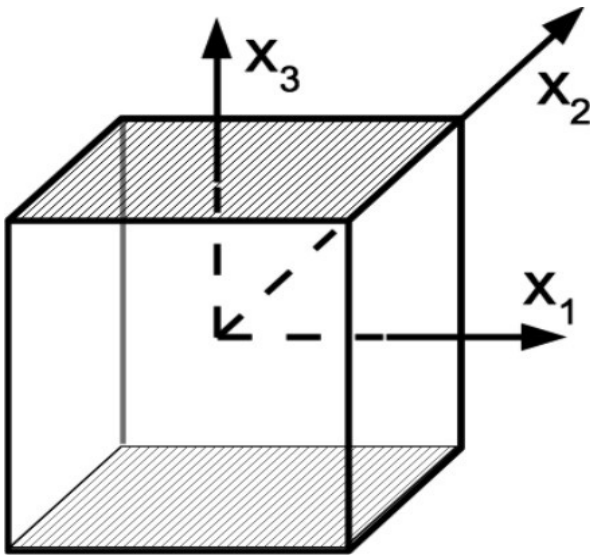


Figure 1: Piezoelectric parallelepiped of PMN-34.5PT with dimensions A,B and C poled along x_3

We consider a piezoelectric parallelepiped with dimension A, B and C (figure1). If we suppose that the origin of the axes is at the center of the cube, $L_1=A/2$, $L_2=B/2$ and $L_3=C/2$ where A,B and C are the edges of the cube. There are two electrodes on the planes $x_3=L_3$ and $x_3=-L_3$. The general Lagrangian can be expressed as [5 & 6]:

$$L = \iiint_V \frac{1}{2} (u_{i,j} C_{ijkl}^E u_{k,l} - \rho \omega^2 u_i u_i) dV + \iiint_V \frac{1}{2} (2\phi_{,m} e_{mkl} u_{k,l} - \phi_{,m} \varepsilon_{mn}^S \phi_{,n}) dV - \sum_{s=1}^2 \iint_S N_m \phi (e_{mkl} u_{kl} - \varepsilon_{mn}^S \phi_{,n}) dS, \quad (2)$$

where ρ and components C_{ijkl}^E , e_{mkl} and ε_{mn}^S are respectively, the density, the elastic stiffness tensor measured at constant electrical field, the piezoelectric tensor and the dielectric tensor measured at constant strain of the material. The summation on indices runs from 1 to 3, corresponding to the three directions in the coordinate space. u is the displacement field and ϕ is the potential.

To minimize the Lagrangian (and hence find the equilibrium configuration of the system), the Rayleigh-Ritz method is used. In accordance with this method the displacement and potential may be expressed as a linear combination of the trial functions:

$$u_i = \sum_{p=1}^N a_p \psi_p, \quad (3)$$

$$\phi = \sum_{r=1}^M b_r \varphi_r. \quad (4)$$

The $(\psi_p)_{p=1}^N$ and $(\varphi_r)_{r=1}^M$ functions are chosen to be orthonormal.

If these relations are injected in equation (2), the Lagrangian becomes:

$$L = \frac{1}{2} \left[\sum_p a_p a_p' (\Gamma_{pp} - \rho \omega^2 \Omega_{pp}) \right] + \left[\sum_p a_p b_r (\Omega_{pr} - A_{pr}) \right] - \frac{1}{2} \left[\sum_r b_r b_r' (\Lambda_{rr} - 2B_{rr}') \right] \quad (5)$$

Where

$$\begin{aligned} \Gamma_{pp'} &= \iiint_V \psi_{p,i,j} C_{ijkl}^E \psi_{p',k,l} dV \\ \Omega_{pr} &= \iiint_V \varphi_{r,m} e_{mkl} \psi_{p,k,l} dV, \\ \Lambda_{rr'} &= \iiint_V \varphi_{r,m} \varepsilon_{mn}^S \varphi_{r',n} dV, \\ A_{pr} &= \sum_{s=1}^2 \iint_S \varphi_r N_m e_{mkl} \psi_{p,k,l} dS, \\ B_{rr'} &= \sum_{s=1}^2 \iint_S \varphi_r N_m \varepsilon_{mn}^S \varphi_{r',n} dS \end{aligned} \quad (6)$$

with

$$\psi_{p,i,j} = \frac{1}{2} \left(\frac{\partial \psi_{pi}}{\partial x_j} + \frac{\partial \psi_{pj}}{\partial x_i} \right) \quad \text{and} \quad \varphi_{r,m} = \frac{\partial \varphi_r}{\partial x_m}. \quad (7)$$

Γ , Ω and Λ are respectively elastic, piezoelectric and dielectric interaction matrices. A_{pr} and $B_{rr'}$ are the contributions of the work of the electrostatic forces. Coefficients a_p and b_r are obtained by calculating the stationary points of the Lagrangian (i.e. $\partial L = 0$). This yields the following eigenvalue system:

$$\begin{aligned}
 (\Gamma + (\Omega - A)(\Lambda - 2B)^{-1}(\Omega - A)^t)a &= \rho\omega^2 a, \\
 b &= (\Lambda - 2B)^{-1}(\Omega - A)^t a.
 \end{aligned}
 \tag{8}$$

The eigenvectors of this equation system give us the coefficients of the expansion of the actual displacement and the electrical functions in terms of the basis functions. The eigenvalues correspond to the actual resonance frequencies.

3. Eigen vibration modes of a piezoelectric cube

Choice of the basis functions

In 1971 H. Demarest introduced the use of Legendre polynomial to determine the elastic constants of a solid [7]. A few years later I. Ohno extended this use to the study of free vibrations of a crystal [6]. Recently, Delaunay *et al.* proposed basis functions for a piezoelectric specimen with an electrode on one face of a parallel-pipedic crystal [4]. In this study, two electrodes are placed on the cube: one on the face $x_3=-L_3$ and one on the face $x_3=L_3$. These faces are normal to the poling direction and the chosen basis function must verify:

$$\delta_{pp'} = \begin{cases} 1 & \text{if } p = p' \\ 0 & \text{otherwise} \end{cases}
 \tag{9}$$

The displacement basis functions defined by Demarest are unchanged. These functions were verified by Ohno and Delaunay *et al.*. The electrical function is here modified to simulate the short-circuit boundary conditions, *i.e.* the potential on face $x_3=-L_3$ must be equal to the potential on face $x_3=L_3$. We suppose that the potential on the electrodes null in order to set to zero the A_{pr} and B_{rr} matrices and thus minimize the computation time. The chosen basis functions of the displacements and electrical potential are respectively:

$$\psi_p = \frac{1}{\sqrt{L_1 L_2 L_3}} P_\lambda \left(\frac{x_1}{L_1} \right) P_\mu \left(\frac{x_2}{L_2} \right) P_\nu \left(\frac{x_3}{L_3} \right) e_i,
 \tag{10}$$

$$\varphi_r = \frac{1}{\sqrt{L_1 L_2 L_3}} P_\xi \left(\frac{x_1}{L_1} \right) P_\zeta \left(\frac{x_2}{L_2} \right) f_\eta \left(\frac{x_3}{L_3} \right)
 \tag{11}$$

With $f_\eta \left(\frac{x_3}{L_3} \right) = \sin \left((\eta + 1) \left(1 + \frac{x_3}{L_3} \right) \right) P_\eta \left(\frac{x_3}{L_3} \right)$ where the p^{th} and r^{th} basic functions ψ_p and φ_r are defined by the triplets, (λ, μ, ν) and (ξ, ζ, η) , respectively. $P_\alpha(x)$ is the normalized Legendre function of order α and e_i is the

unit displacement vector in x_i direction, $\frac{1}{\sqrt{L_1 L_2 L_3}}$ is a normalization term [4, 6, 7].

Simulation Results

Table 1 shows the resonance frequencies of a PMN-34.5PT cube calculated using this theory and its comparison with Demarest's and Delaunay's theories. The elastic, piezoelectric and dielectric constants were taken from [4]. They are $C_{11}=174.7$, $C_{12}=116.6$, $C_{13}=119.3$, $C_{33}=154.8$, $C_{44}=26.7$, $C_{66}=29$ in GPa; $e_{15}=17.1$, $e_{31}=-6.4$, $e_{33}=27.3$ in C/m²; $\epsilon_1=21.0105$, $\epsilon_3=25.0125$ in pF/m.

Table1: Resonant for a PMN 34,5PT with Delaunay coef. (in Hz)

Demarest Basis Functions Order=7	Delaunay Basis Functions Order=7	Our Basis Functions Order=5	Error (1&2)	Error (1&3)
82966	86778	87007	-4.59%	-4.87%
89241	90037	89145	-0.89%	0.11%
109147	107743	104243	1.29%	4.49%
118057	117423	113436	0.54%	3.91%
119489	121678	116894	-1.83%	2.17%
126991	122818	120120	3.29%	5.41%
129809	134243	122440	-3.42%	5.68%
134243	137977	124276	-2.78%	7.42%
139246	139264	133209	-0.01%	4.34%
142298	143193	134259	-0.63%	5.65%
145232	147165	145273	-1.33%	-0.03%
153129	153961	154155	-0.54%	-0.67%
160024	156405	156825	2.26%	2.00%
161706	163513	160742	-1.12%	0.60%

Table 1 presents the comparison between the resonant frequencies computed with the basis functions corresponding to different boundary conditions showing that the presence of the electrodes can greatly affect the resonances. Note that the volume of the electrodes has been neglected in theoretical studies. The modes with maximum displacements along the x_3 axis are the most sensitive to the presence of electrodes. The maximum difference between Demarest and Delaunay cases is 4.59% and the maximum difference between Demarest and our case is 7.42%. Increasing the degree of the approximate polynomial functions does not reduce the discrepancy in the prediction of resonant frequencies between Demarest basis function and our basis function. They are due to the new boundary conditions (short circuit electrodes). The order of the basis functions in our case is lower than in Demarest and Delaunay's cases; the convergence is improved and the computing time is around 2.2 seconds against 22.4 seconds for Demarest.

4. Experimental results

Experimental set-up

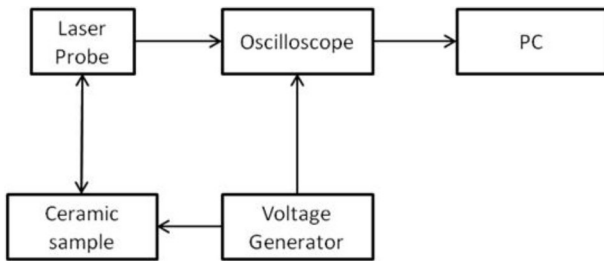


Figure 2: Experimental set-up

The experimental set-up is presented on figure 2. It allows the measurement of vibration velocities versus frequency. The electrical excitation is delivered by a voltage generator. It has a very large bandwidth and the delivered electrical power is adjustable. The sample is set on a plastic holder and the electrical contact is ensured by a metallic strip fixed on a spring so that free mechanical boundary conditions at the surfaces of the cube are fulfilled. Velocities at the surface of the sample are measured by means of a Laser vibrometer (Polytech OFV-505) that allows the detection of the resonance frequencies and the identification of the associated mode shapes. The interferometer is positioned at 50 cm from the sample. The velocity decoder sensitivity is respectively 5 mm/s/V and 25 mm/s/V, depending on the cut-off frequency, respectively 250 kHz and 1.5 MHz. The measured signals are sent to a computer via a digital oscilloscope.

Results and discussions

The resonance spectrum of the PMN-34.5PT (10mm×10mm×10mm) sample was measured by the described above experimental set-up.

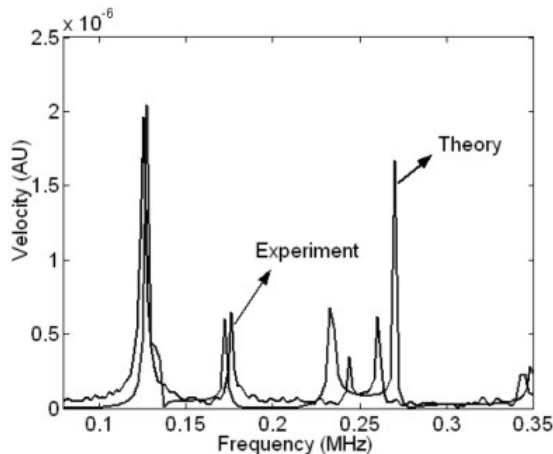


Figure 3: Comparison between the theoretical and experimental velocity spectra of the PMN-34.5PT cube (at the center of the face $x_{3=L3}$)

Experimental and theoretical results are compared in Figure 3. The theoretical velocity is computed using the eigen frequencies and the expression of the displacement, the velocity being the time derivative of the displacement. In the frequency domain, this implies: $v = j\omega u$.

For the first two resonances, agreement is satisfactory. The discrepancies between measurements and predictions for the two other peaks could be due to the lack of precision in the functional properties used for the theoretical modeling. A sensitivity study of the resonance location to input parameters has shown that these two peaks were very sensitive to C_{13} and C_{33} . Further studies will deal with the application of the model to material characterization.

5. Conclusion

This paper studied the natural frequencies of a piezoelectric ceramic. A numerical method is developed to predict the resonance spectrum of the PMN-34.5PT cube and a comparison with the experimental spectrum shows that all the eigenfrequencies are not piezoelectrically coupled. In future work, the inverse problem will be solved for this and other piezoelectric ceramics in order to extract the functional properties of piezoelectric ceramics from their resonant spectra.

Appendix

A. Description of interaction matrices: elastic Γ , piezo-electric, Ω , and dielectric Λ

Table2: Matrix of elastic interaction: Γ .

i, j	Γ'_{pp}
1,1	$C_{11}^E G_1 + C_{66}^E G_2 + C_{55}^E G_3 + C_{56}^E G_4 + C_{56}^E G_5 + C_{15}^E G_6 + C_{15}^E G_7 + C_{16}^E G_8 + C_{16}^E G_9$
2,2	$C_{66}^E G_1 + C_{22}^E G_2 + C_{44}^E G_3 + C_{24}^E G_4 + C_{24}^E G_5 + C_{46}^E G_6 + C_{46}^E G_7 + C_{26}^E G_8 + C_{26}^E G_9$
3,3	$C_{55}^E G_1 + C_{44}^E G_2 + C_{33}^E G_3 + C_{14}^E G_4 + C_{14}^E G_5 + C_{35}^E G_6 + C_{35}^E G_7 + C_{36}^E G_8 + C_{36}^E G_9$
2,3	$C_{56}^E G_1 + C_{24}^E G_2 + C_{34}^E G_3 + C_{44}^E G_4 + C_{22}^E G_5 + C_{36}^E G_6 + C_{45}^E G_7 + C_{25}^E G_8 + C_{46}^E G_9$
3,1	$C_{15}^E G_1 + C_{46}^E G_2 + C_{35}^E G_3 + C_{36}^E G_4 + C_{45}^E G_5 + C_{55}^E G_6 + C_{13}^E G_7 + C_{14}^E G_8 + C_{56}^E G_9$
1,2	$C_{16}^E G_1 + C_{26}^E G_2 + C_{45}^E G_3 + C_{25}^E G_4 + C_{46}^E G_5 + C_{14}^E G_6 + C_{56}^E G_7 + C_{66}^E G_8 + C_{12}^E G_9$

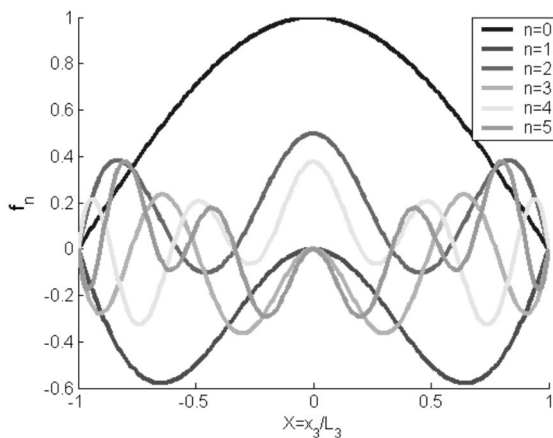
Table3: Matrix of piezoelectric interaction: Ω

i	Ω_{pr}
1	$e_{11} G_1 + e_{26} G_2 + e_{35} G_3 + e_{25} G_4 + e_{36} G_5 + e_{31} G_6 + e_{15} G_7 + e_{16} G_8 + e_{21} G_9$
2	$e_{16} G_1 + e_{22} G_2 + e_{34} G_3 + e_{24} G_4 + e_{32} G_5 + e_{36} G_6 + e_{14} G_7 + e_{12} G_8 + e_{26} G_9$
3	$e_{15} G_1 + e_{24} G_2 + e_{33} G_3 + e_{23} G_4 + e_{34} G_5 + e_{35} G_6 + e_{13} G_7 + e_{14} G_8 + e_{25} G_9$

Table4: Matrix of dielectric interaction: Λ

Λ'_{rr}
$\varepsilon_{11}^S G_1 + \varepsilon_{22}^S G_2 + \varepsilon_{33}^S G_3 + \varepsilon_{23}^S G_4 + \varepsilon_{32}^S G_5 + \varepsilon_{13}^S G_6 + \varepsilon_{31}^S G_7 + \varepsilon_{12}^S G_8 + \varepsilon_{21}^S G_9$

B. presentation of the f_h functions:



References

1. W. P. Mason, N. J. Princeton & V. Nostrand, Eds. Physical Review (2nd Edition, Vol. **72**) (1948)
2. R. Krimholtz, D. A. Leedom, & G. L. Matthaei, *Electronic Letters*, **6**, 398–399 (1970).
3. ANSI/IEEE Standard 176-1987 on piezoelectricity, IEEE Trans. Ultrason., Ferroelect., Freq. Contr. **43**, 717 (1996).
4. T. Delaunay et al., IEEE Trans. on UFFC control **55**, 476 (2008).
5. R. Holland et al, IEEE Trans. on Sonics and Ultrasonics, 119 (1968)
6. I. Ohno, J. Phys. Earth, **24**,355(1976)
7. H. Demarest, J. Acous. Soc. Am., **49**, 768 (197

Arrived: 11. 09. 2012

Accepted: 13. 11. 2012

Aging Of Overvoltage Protection Elements Caused By Past Activations

Aleksandra Vasić¹, Miloš Vujisić², Koviljka Stanković², Predrag Osmokrović^{2*}

¹ Faculty of Mechanical Engineering, University of Belgrade, Belgrade, Serbia

² Faculty of Electrical Engineering, University of Belgrade, Belgrade, Serbia

Abstract: This paper investigates the ageing process of some common elements used for overvoltage protection. Tested elements are overvoltage diodes, varistors and gas filled surge arresters. Ageing process is considered as a function of previous number of element activations. Experiments are performed both with voltage and current transients. Statistical analysis of experimental data has shown that all elements investigated are subjected to the ageing during their functional operation. After 1000 overvoltage diode activations, the volt-ampere characteristic curve "breaking" has been noticed in the range of higher currents, while the breakdown voltage value is reduced. In the case of varistor, it is determined that with higher number of activations comes an increase in the value of breakdown voltage and the shift of volt-ampere characteristics in the field of higher voltage. As for the aging of gas filled surge arresters, it has been shown that past activations reduce the value of dc breakdown voltage and lead to narrowing the area bounded by the 0.1% and 99.9% quintiles of the impulse characteristics.

Key words: overvoltage diodes, varistors, gas filled surge arresters, ageing, transients.

Staranje elementov za prenapetostno zaščito zaradi premostitev

Povzetek: V članku je raziskan proces staranja nekaterih tipičnih elementov za prenapetostne zaščite. Testni elementi so prenapetostne diode, varistorji in plinsko polnjeni prenapetostni odvodniki. Proces staranja je upoštevan kot funkcija števila predhodnih aktivacij. Opravljeni so bili testi tako napetostnih kot tokovnih prehodov. Statistične analize merilnih podatkov so pokazale, da so vsi elementi podvrženi staranju v obdobju normalnega obratovanja. Po 1000 aktivacijah diode je bil opažen »zlom« tokovno-napetostne karakteristike v območju velikih tokov in znižanje prebojne napetosti. Pri večkratnem proženju varistorja je bil opažen dvig prebojne napetosti in premik napetostno-tokovne karakteristike pri višjih napetostih. Pri plinsko polnjenih prenapetostnih odvodnikih je bilo opaženo, da predhodne aktivacije znižujejo prebojno DC napetost in vodijo v ožjenje območja omejenega med 0.1 % in 99.9 % kvantila karakteristike impulza.

Ključne besede: prenapetostne diode, varistorji, plinski polnjeni prenapetostni odvodniki, staranje, prehodi.

*Corresponding Author's e-mail: opredrag@verat.net

1. Introduction

All the overvoltage protection elements are subjected, to a lesser or greater extent, to the changes of operational characteristics under the influence of overvoltages which occur during the exploitation of the protective circuit. Effects of aging occur because of the design and materials imperfection, while the changes of elements' parameters in this process are irreversible. The nature of the aging effect is cumulative as well as the damages caused by radiation [1]. Initial element damages may not always significantly degrade the functional characteristics of the circuit, however, their accumulation during

the time degrade characteristics of protection elements to a greater extent, so that protective circuit can eventually become completely dysfunctional. Duration of the proper functioning of protective circuit depend not only on the properly selected protective elements (in terms of nominal voltage), but on the design of protective circuit which must be adapted to conditions in which the protected device operate (number of overvoltages in the time unit, their expected values and shapes). In term of determining the optimal design of the protective circuit, it is of interest to investigate the basics of elements aging process, exposed to current or voltage transients, so that is the subject and the aim of this paper.

2. The aging of overvoltage diode

Overvoltage diode combining in itself the three parts: contact systems, crystal of semiconductor and polarization conjunction. Degradation phenomena during exploitation are caused by the processes at phase boundaries. Degradation of the contact system is caused by the phenomena such as electromigration, creation of intermetallic phases and chemical compounds on the contact points between the metallization and the adsorbed components, etc [2]. The reasons that lead to changes in diode characteristics can be very different. When forming the diode structure, many processes of interaction and redistribution of generic defects, which are introduced in the process of technological operations, flow in the crystal. The result of these operations is the occurrence of certain defect structures whose evolution during exploitation causes aging and degradation characteristics of such specific components. These defects are: distributed and associated point defects, the local mechanical stresses and dislocated systems.

In the general case, defective structure, created in the technological cycle, is metastable and relaxes during the time. The basic physical mechanisms that cause its relaxation processes are generation and migration of lattice defects as well as specific processes of structural transformation in the boundary layers [3].

The process of exploitation (effects of overvoltages) results in a spatial redistribution of electrical charge and electrical field, changes of polarity centers as well as continuous relaxation and the generation of electronic excitation. The changed defect atomic configurations, impurity profile, and other structures of various complexes appear as a result of aforementioned processes. In the bases of these processes are micro-mechanisms such as the type "electronic excitation - atom-displacement". Specific outcome of these mechanisms, in the diode aging process, determines the diode functional characteristics. The formation of electronic excitation in the case of overvoltage diodes is caused by the striking ionization processes. The described changes in the electronic subsystem lead to deformation of the charge density image for atoms displacement, while in certain cases lead to barriers reduction or elimination for atomic transition. If the mechanical stress gradients exist in certain parts of the semiconductor then a directed movement of point defects occurs, which cause the redistribution of impurities. In the same time, different transformation processes of point defects occurs: formation and deformation of the complex composed of displaced atoms vacancy, creation and annihilation of fine precipitates [4]. In this way, the aging kinetics is determined by the nature of low-temperature mecha-

nisms, in this case by the number of activations, which cause changes in defect structure of materials [5,6].

In this paper, the aging of the overvoltage diode was measured against the influence of previous number of activation on its volt-ampere characteristic, volt-ohm characteristics and the breakdown voltage value. Tested overvoltage diodes were with nominal breakdown voltage of 250 V and with the maximum dc current of 1 A. Diodes were tested with 1000 current pulses ($I_{max} = 13A$, $T_r/T_2 = 8/20\mu I$). Measurements of diode characteristics were performed in its inverse polarization, within the plateau area of volt-ampere characteristics. Experiment was performed at temperature of 20°C in well-controlled laboratory conditions. For all tests the type B measurement uncertainty was less than 5 % [7,8].

Figure 1 shows the diode volt-ampere characteristics at the beginning and the end of the experiment, while the corresponding volt-ohm characteristic is given in Figure 2. Based on the results shown in Figures 1 and 2 it can be noticed that the diode aging process is weakly expressed. The breakdown voltage at start was 259.4 V, while at the end of testing, the value was 262.2 V. In the volt-ampere characteristics, after 1000 activations, "breaking" the curve was observed in range of high currents, which can be explained by degradation of the diode electrodes (metallization). Figure 2 shows the increase of dynamic resistance after the test completion.

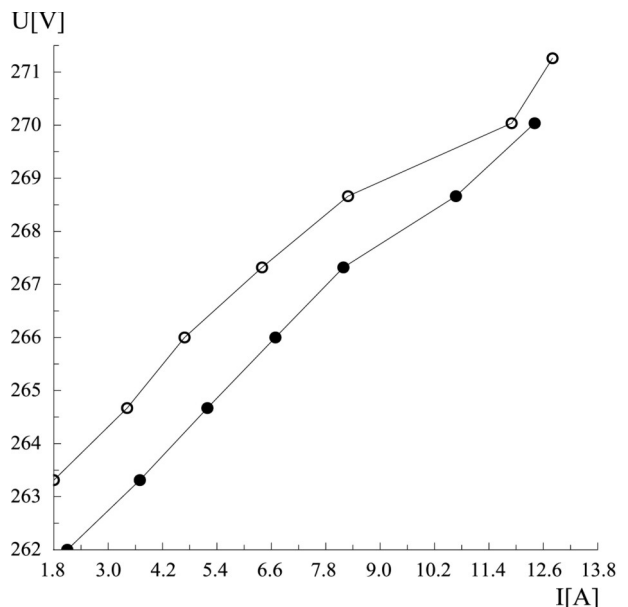


Figure 1: Volt-ampere characteristics depending on the diode activation number (● – 1 pulse; ○ – 1000 pulses).

3. Aging of the varistor

The aging process of the varistor can be described by the irreversible changes of its volt-ampere characteristics. There are two basic causes of varistors aging, and that are the constant current through the varistor, which exists when the voltage is loaded, and the pulse current due to occurrence of overvoltage pulses. These facts indicate that the aging process of varistor begins with its connection in the circuit, regardless whether the overvoltage pulses occur or not. The temperature has a great influence on the aging process caused by the loaded voltage, while the process is less expressed in case of the overvoltage occurrences. Due to the continuous flow of direct current through the varistor the resistance drop can be observed, resulting from the merging of the elementary grains of zinc-oxide, which occurs due to thermal effects [9]. This effect is already noticeable with the current of 1 mA. Specifically, the varistor subjected to the mentioned current value at the temperature of 40°C has the operating voltage reduction of 80%. Research showed [3,4] that varistor exposed to the critical overvoltage impulse remains in the circuit brake while the varistor exposed to the long-term effect of constant current, at destruction, act as a short circuit.

It is necessary to say that the effect of varistors aging, which is caused by the influence of constant current, can be effectively minimized by selecting the proper varistor for a protected device. However, changes in varistor characteristics caused by the transients are the real interest, and that was examined within this paper.

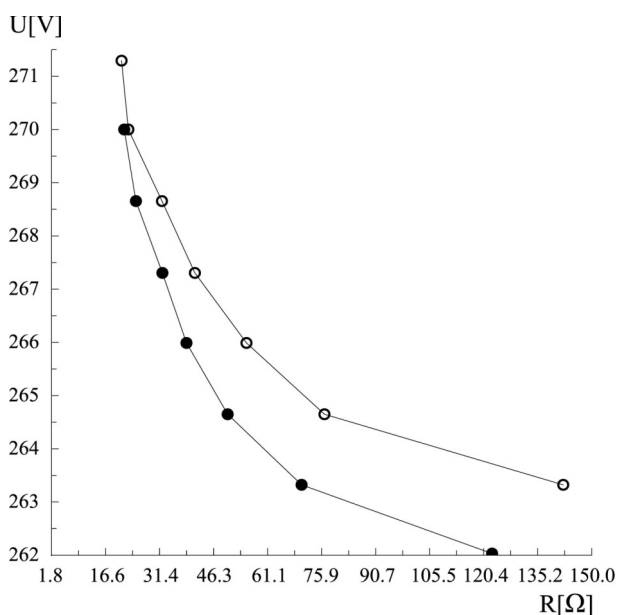


Figure 2: Volt-ohmic characteristics depending on the diode activation number (● – 1 pulse; ○ – 1000 pulses).

Two different types of varistor were investigated, with disc diameter 10 mm and 14 mm, respectively. Both varistors were designed for permanent alternating voltage load $V_{eff} = 230 V$, with a maximum current value $(8 \times 20\mu s)$ 2500 A for the first varistor, and 4500 A for the other. Varistors were subjected to 1000 current test pulses, while after the sequence of 100 test pulses the recording of varistor characteristics was done (by using the same test pulse). For both type of varistors, changes in volt-ampere and volt-ohmic characteristics were measured, as well as changes in the breakdown voltage value. All these changes are given as a function of previous varistor activations. Since the varistors with smaller disc diameter are more susceptible to aging, shown diagrams are related to this type of varistor.

The Figure 3 shows the volt-ampere characteristics changes, while the changes in volt-ohmic characteristic are given in Figure 4, both depending on varistor activation number. The Figure 5 shows the change of varistor breakdown voltage value in dependence of varistor activation number. From the results obtained, it can be concluded that the increase of varistor activations imply increase in the breakdown voltage and the shift of volt-ampere characteristics in the range of higher voltages. From the diagram shown in Figure 4 it can be concluded that the slope change of volt-ampere characteristic is relatively low, i.e. that the coefficient of nonlinearity α is not changed significantly. Change of the varistor coefficient of nonlinearity α depending on the varistor activation number is shown in Figure

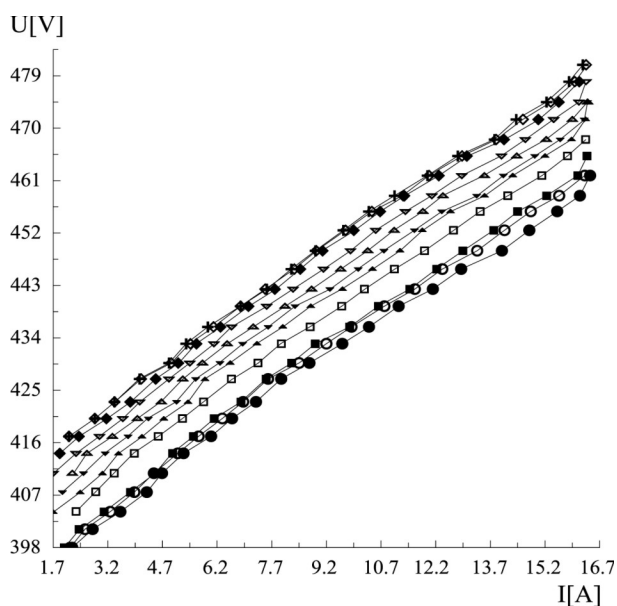


Figure 3: Volt-ampere characteristics depending on varistor activation number (● – 1 pulse; ○ – 100 pulses; ■ – 200 pulses; □ – 300 pulses; ▲ – 400 pulses; ▼ – 500 pulses; △ – 600 pulses; ▽ – 700 pulses; ◆ – 800 pulses; ◇ – 900 pulses; + – 1000 pulses;).

6. These changes can be explained by “breaking” some elementary chains at position of elementary varistor with a minimal dissipation, due to the effect of current pulses, which reduces the effective varistor surface for current conducting, and thereby its resistance and breakdown voltage increase. So, therefore, the noticeable effects in decreasing of the nonlinearity coefficient α with the number of activation could be expected in the current domain.

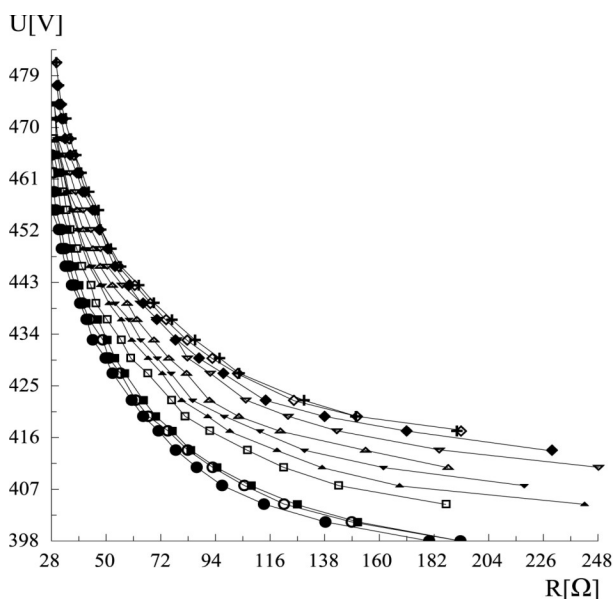


Figure 4: Volt-ohmic characteristics depending on varistor activation number (● – 1 pulse; ○ – 100 pulses; ■ – 200 pulses; □ – 300 pulses; ▲ – 400 pulses; ▼ – 500 pulses; △ – 600 pulses; ▽ – 700 pulses; ◆ – 800 pulses; ◇ – 900 pulses; + – 1000 pulses).

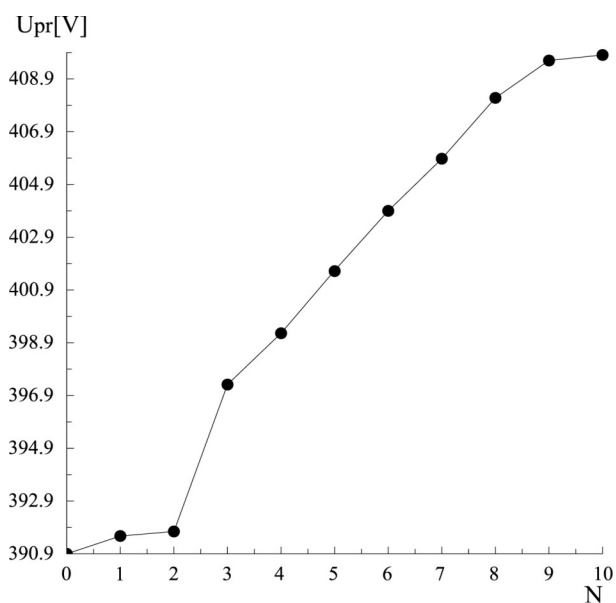


Figure 5: Varistor breakdown voltage depending on activation number (number of pulses = $N \cdot 100$).

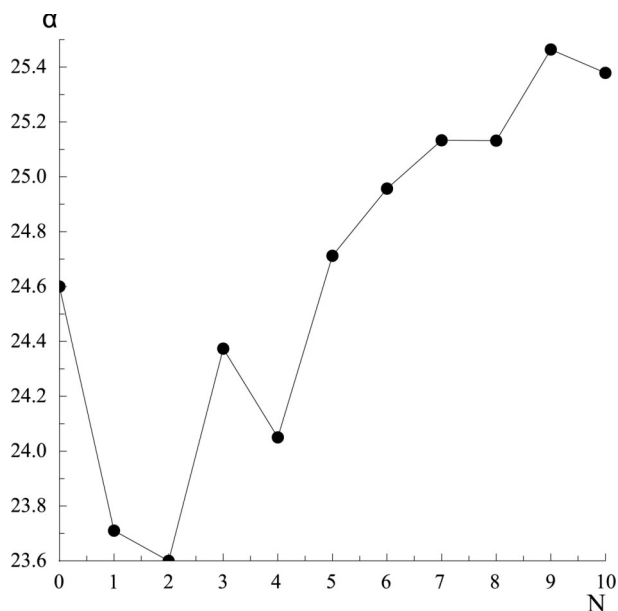


Figure 6: Varistor coefficient of nonlinearity α depending on activation number (number of pulses = $N \cdot 100$).

4. Aging of gas filled surge arresters

For gas filled surge arresters the characteristic process of aging (irreversible changes) arises due to changes of electrode topography [10,11].

Testing the irreversible characteristics of gas filled surge arresters was performed on arresters with the nominal voltage of 470 V, 230 V and 145 V. The aim of the test performed was to determine the change in the statistical sample of the random variable impulse breakdown voltage depending on the number of past breakdowns. This effect was investigated on a series of 1000 measurements both with dc breakdown voltage and pulse breakdown voltage. During the experiments the discharge energy was constant. The results are divided into 20 successive groups with 50 measurements of breakdown voltage. Each of these groups was tested statistically. By using the graphic, χ - square, and Kolmogorov test the random variable belonging to one of the following distributions was examined: normal, exponential, double exponential and the Weibull distribution [12-15]. By using the U-test each group was tested on belonging to the same random variable, with a 5% significance level [16].

The influence of past breakdowns on the volt-second characteristic was tested in the same way. Measurements were divided in 20 successive groups with 50 values of impulse breakdown voltage. Then, for each group the theoretical statistical distribution was determined with 99.9% and 0,1% quintiles ($U_{99,9}$ and $U_{0,1}$).

Starting from the values of $U_{99,97}$ and $U_{0,1}$ and the corresponding values of dc breakdown voltage the volt-second characteristic is constructed based on the Area law [17-19]. Comparisons of pulse characteristics of the experimentally obtained values, divided in successive groups, allowed the determination of past impulse breakdown effects on the volt-second characteristic.

Figure 7 shows chronological range of the first series of measurement values of dc breakdown voltage of the gas filled surge arrester with nominal voltage 470V. Figure 8 provides chronological range of the last series of measurements. Figure 9 shows the values of the U-test variables, with the 5% level of significance, depending on the random variable dc breakdown voltage. Based on results presented, it is clear that during the exploitation of the gas surge arresters the irreversible changes have been manifested. Statistical analysis showed that groups of measurements with lower number follow the normal distribution. With the increasing of the group number the distribution becomes Weibull. This effect is more pronounced if the discharge energy increases. The observed effect of irreversible changes of the gas filled surge arresters with dc breakdown voltage can be explained by changes within the topography of electrode surface. Small changes of the interelectrode gap distance can greatly affect the value of dc breakdown voltage (in the case of gas filled surge arrester, since its interelectrode gap is small). As a result of breakdown there is a decrease in the interelectrode gap distance as a consequence of the breakdown craters on the electrode surface. Reducing the interelectrode gap distance causes the decrease of dc breakdown voltage value.

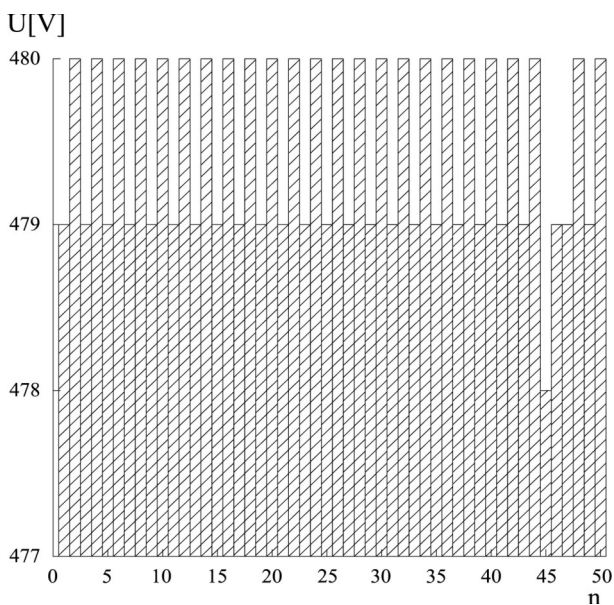


Figure 7: Chronological range of the first series of measurement values of dc breakdown voltage.

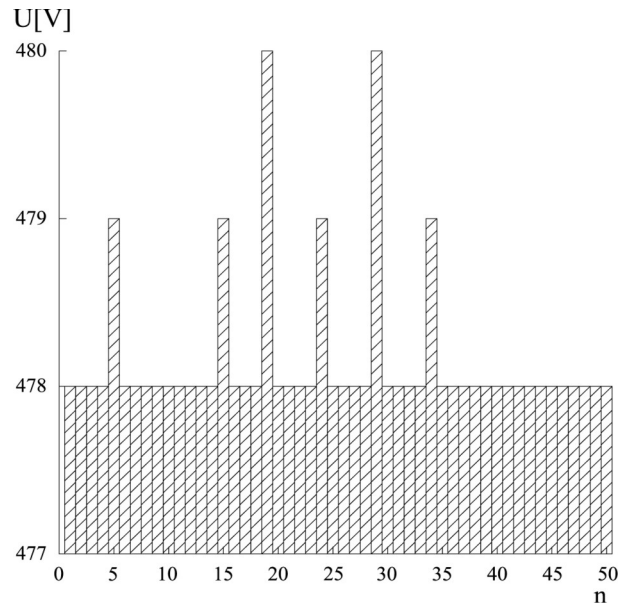


Figure 8: Chronological range of the last series of measurement values of dc breakdown voltage.

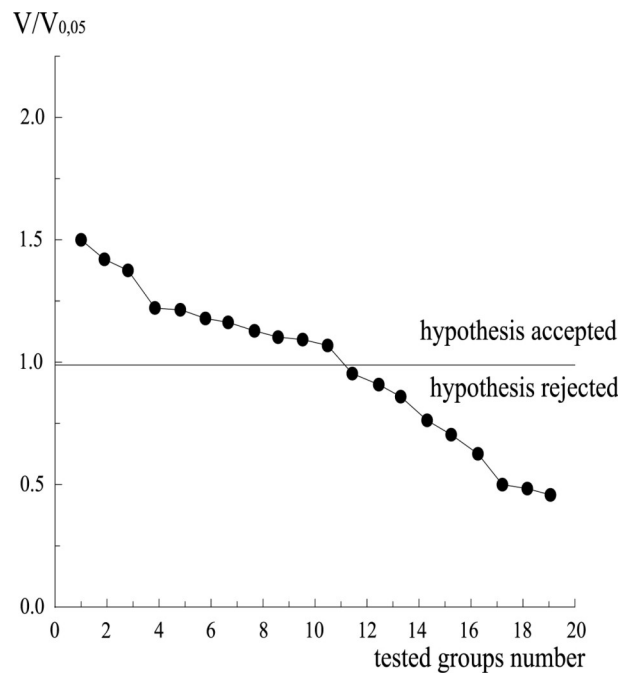


Figure 9: Value of the U-test variables with the 5% level of significance depending on the random variable dc breakdown voltage.

Decreasing the dc breakdown voltage value (Figures 7 and 8) is the consequence of increased number of initiation centers caused by past breakdowns. The change of the random variable distribution, what is noticeable with increasing the group number of measurements, i.e. transition from normal to Weibull distribution, can be explained by the phenomenon of “weak spots” in the electrodes surfaces. These weak spots are not in equilibrium with the “strong spots” so that there is a

loss of distribution symmetry, so it becomes asymmetric Weibull distribution [20].

Similar irreversible effect was observed in the case of a random variable "impulse breakdown voltage" which is reflected in the change of pulse characteristics. The consequence of the previous discharges in this case is the smoothing and narrowing of the volt-second characteristic, Figures 10 and 11. Figures 12 and 13 shows photos of electrode surface after the 1000 impulse breakdowns voltage.

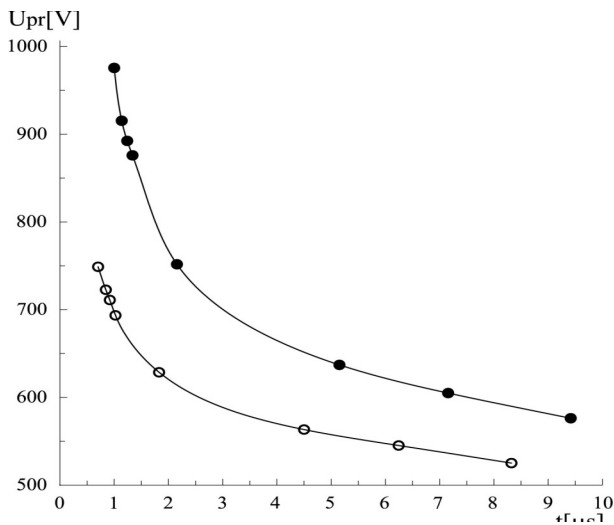


Figure 10: Volt-second characteristics after first series of breakdowns.

Based on the obtained results it can be concluded that the gas filled surge arresters are exposed to the irreversible changes during their exploitation. These changes are caused by changing the topography of electrode surfaces during operation.

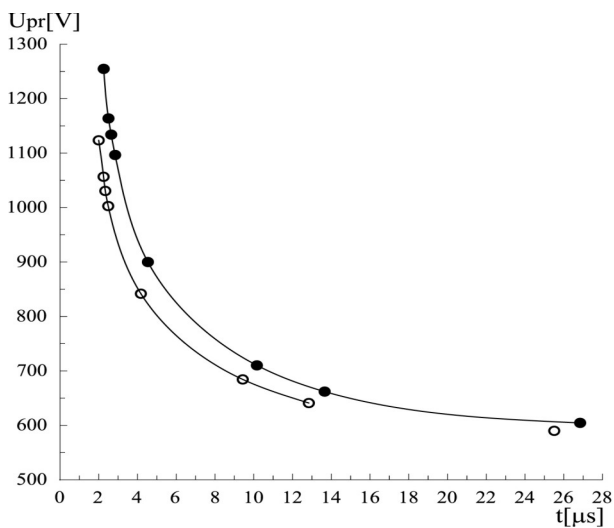


Figure 11: Volt-second characteristics after last series of breakdowns.

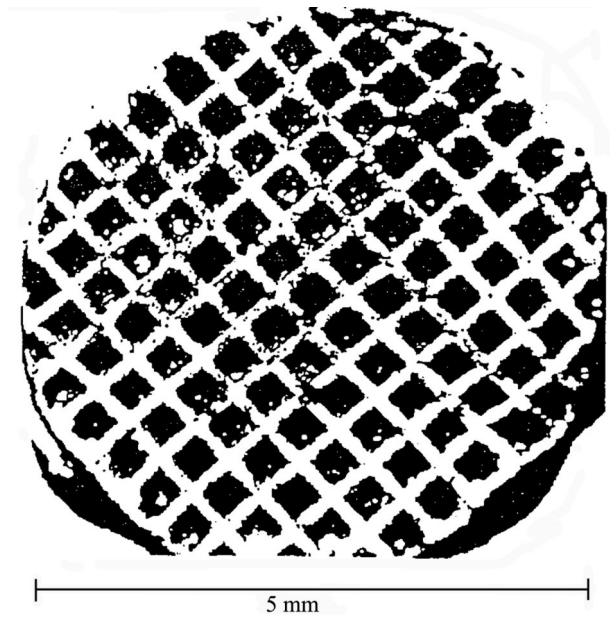


Figure 12: Topography of the electrode surface after 50 completed impulse voltage breakdowns.

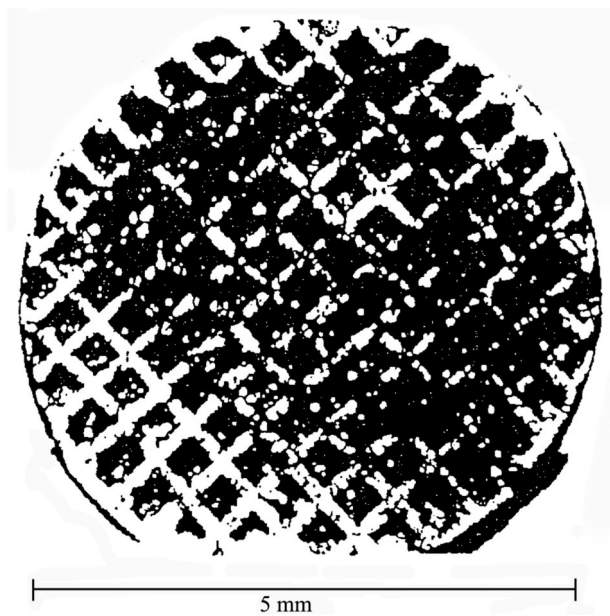


Figure 13: Topography of the electrode surface after 1000 completed impulse voltage breakdowns.

5. Conclusion

This paper presents the results obtained within the functional ageing investigation of elements for overvoltage protection. It has been shown that the past activations reduce the breakdown voltage value of the overvoltage diode. It was noticed that there is an increase in dynamic resistance after larger number of activation. After 1000 activations, the volt-ampere characteristic curve "breaking" can be noticed in the range

of higher currents, which can be explained by degradation changes in diode electrodes.

In the case of varistor, it is shown that with higher number of activations comes an increase in the value of breakdown voltage and the shift of volt-ampere characteristics in the range of higher voltage. Also, it is found that the number of previous activations does not significantly affect the varistor coefficient of linearity. This phenomenon can be explained by “breaking” some chains of elementary varistor at the place of elementary varistor with the lowest power dissipation due to the effects of current pulses, which reduces the effective varistor surface for electricity conducting, and thereby its resistance and breakdown voltage increase.

As for the aging of gas filled surge arresters, it has been shown that past activations reduce the value of dc breakdown voltage and lead to narrowing of the area bounded by the 0.1% and 99.9% quintiles of the impulse characteristics. This phenomenon is explained by the created craters caused by previous activations. The resulting craters significantly reduce the interelectrode distance of the order of 0.1 mm and lead to increased electronic emission centers. As a result, there is reduction in the dc breakdown voltage value, i.e. increase in the number of free electrons, which leads to said consequences on the macroscopic characteristics. Established irreversible changes in characteristics of elements for overvoltage protection due to previous activations are of concern in designing and life assessment of overvoltage protection in conditions of high electromagnetic contamination.

Acknowledgment

The Ministry of Education and Science of the Republic of Serbia supported this work under contract 171007.

References

1. K. Stanković, M. Vujisić, E. Dolićanin, Reliability of Semiconductor and Gas-filled Diodes for Over-voltage Protection Exposed to Ionizing Radiation, Nucl. Technol. Radiat. 24(2009)2 132-137.
2. S. Parker, Solid-State Physics Source Book, McGraw-Hill, New York, 1988.
3. D.A. Neamen, Electronic Circuit Analysis and Design, University of New Mexico, 2001.
4. Charles A. Schuler, Electronics: Principles and Applications, Sixth Edition, The McGraw-Hill Companies, 2003.
5. M. Richter, M. Wackerle, S. Kibler, Technology and Applications of Microdosing Systems, Informacije MIDEM 41(2011)4 253-256.
7. M. Vujisić, P. Osmokrović, K. Stanković, B. Lončar, Influence of working conditions on over-voltage diode operation, J. Optoelectron. Adv. M. 9(2007) 12 3381-3884.
8. K. Stanković, M. Vujisić, Lj. Delić, Influence of Tube Volume on Measurement Uncertainty of GM Counters, Nucl. Technol. Radiat. 25(2010)1 46-50.
9. K. Stanković, Influence of the plain-parallel electrode surface dimensions on the type A measurement uncertainty of GM counter, Nucl. Technol. Radiat. 26(2011)1 39-44.
10. B. Lončar, M. Vujisić, K. Stanković, P. Osmokrović, Stability of metal-oxide varistor characteristics in exploitation conditions, Acta Phys. Pol. A 116(2009)6 1081-1084.
11. B. Lončar, P. Osmokrović, S. Stanković, Temperature Stability of Components for Over-voltage Protection of Low-voltage Systems, IEEE Trans. Plasma Sci. 30(2002)5 1881-1885.
12. M. Bizjak, Contact materials for low-voltage power switching devices, Informacije MIDEM 40(2010)2 93-100.
13. K. Stanković, M. Vujisić, D. Kovačević, P. Osmokrović, Statistical analysis of the characteristics of some basic mass-produced passive electrical circuits used in measurements, Measurement 44(2011)2 1713-1722.
14. M. Vujisić, K. Stanković, P. Osmokrović, A statistical analysis of measurement results obtained from nonlinear physical laws, Appl. Math. Model. 35(2011)2 3128-3135.
15. P. Osmokrović, S. Đekić, K. Stanković, M. Vujisić, Conditions for the applicability of the geometrical similarity law to gas pulse breakdown, IEEE Trans. Dielectr. El. Insul. 17(2010)4 1185-1195.
16. P. Osmokrović, R. Marić, K. Stanković, D. Ilić, M. Vujisić, Validity of the Space-Time Enlargement Law for vacuum breakdown, Vacuum 85 (2010) 221-230.
17. Č. Dolićanin, K. Stanković, D. Dolićanin, B. Lončar, Statistical treatment of nuclear counting results, Nucl. Technol. Radiat. 26(2011)2 164-170.
18. P.Osmokrovic, G. Ilic, C. Dolicanin, K. Stankovic, M. Vujsic, Determination of Pulse Tolerable Voltage in Gas-Insulated Systems, Jpn. J. Appl. Phys. 47(2008)12 8928-88934.
19. K. Stanković, M. Pešić, P. Osmokrović. M. Vujisić: Surface-Time Enlargement Law for Gas Breakdown, IEEE Trans. Dielectr. El. Insul. 15(2008)4 994-1005.
20. K.Stankovic, P.Osmokrovic, C.Dolicanin, M.Vujsic, A.Vasic, Time enlargement low for gas pulse bre-

akdown, Plasma Sources Sci. T. 18(2009)2 art.no. 025028.

21. P. Osmokrović, M. Vujisić, K. Stanković, A. Vasić, B. Lončar, Mechanisms of electrical breakdown of gases for pressures from 10^{-9} to 1 bar and inter-electrode gaps from 0.1 - 0.5 mm, Plasma Sources Sci. T. 16(2007) 4 643-655.

Arrived: 16. 08. 2012

Accepted: 31. 10. 2012



Strokovno društvo za mikroelektroniko,
elektronske sestavne dele in materiale

MIDEM pri MIKROIKS | Stegne 7 | SI - 1000 Ljubljana | Slovenia
t. +386 (0)1 513 37 78, +386 (0)1 513 37 68 | f. +386 (0)1 513 37 71
e. info@midem-drustvo.si | www.midem-drustvo.si

Midem Society registration form

FIRST NAME: _____ LAST NAME: _____ TITLE: _____

ADDRESS: _____

CITY: _____ POSTAL CODE: _____

COUNTRY: _____

DATE OF BIRTH: _____

EDUCATION (please, circle whichever appropriate)

PhD	MSc	BSc	High School	Student
-----	-----	-----	-------------	---------

PROFESSION (please, circle whichever appropriate)

Electronics	Physics	Chemistry	Metallurgy	Material Sciences
-------------	---------	-----------	------------	-------------------

COMPANY: _____

ADDRESS: _____

CITY: _____ POSTAL CODE: _____

COUNTRY: _____

TELEPHONE: _____ FAX: _____

E-MAIL: _____

YOUR PRIMARY JOB FUNCTION (please, circle whichever appropriate):

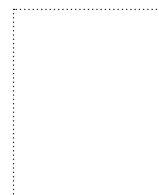
Fabrication	Engineering	Facilities	QA/QC
Management	Purchasing	Consulting	Other

Please, send mail to (please, circle): a) company address b) home address

I will regularly pay the annual MIDEM membership fee (25,00 EUR/year in 2012).

MIDEM members receive printed version of Journal »Informacije MIDEM - Journal of Microelectronics, Electronic Components and Materials« (ISSN 0352-9045) for free!!!

SIGNATURE: _____ DATE: _____



MIDEM at MIKROIKS

Stegne 11
SI-1521 Ljubljana
Slovenia

Instructions for authors | Navodila avtorjem

Informacije MIDEM - Journal of Microelectronics, Electronic Components and Materials is a scientific-professional-societal publication of Professional Society for Microelectronics, Electronic Components and Materials – MIDEM Society. In the Journal, scientific and professional contributions are published covering the fields of microelectronics, electronic components and materials, including but not limited to Electronics, Technologies & Materials, Sensors and Actuators, Power Engineering and Telecommunications.

Authors should suggest to the Editorial board the classification of their contribution such as: original scientific paper, review scientific paper, professional paper...

Scientific and professional papers are subject to peer review.

Each scientific contribution should include the following:

1. Title of the manuscript, authors' names, name of the institution/company.
2. Key Words (5-10 words) and Abstract (200-250 words), stating how the work advances state of the art in the field.
3. Introduction, main text, conclusion, acknowledgements, appendix and references following the IMRAD scheme (Introduction, Methods, Results and Discussion).
4. At the end add full authors' names, titles and complete company/institution address, including Tel./Fax/Email.
5. Manuscripts should be prepared in MS Word format (.doc or .docx) or any OpenDocument format (.odt or .fodt) in single column format and font size 12pt. Recommended length of manuscript (figures not included) is 12-15 pages.
6. Slovene authors writing in English language must submit title, key words and abstract also in Slovene language.
7. Authors writing in Slovene language must submit title, key words and extended abstract (500-700 words) also in English language.

Other types of contributions such as popular science papers, application papers, scientific news, news from companies, institutes and universities, reports on actions of MIDEM Society and its members as well as other relevant contributions, of appropriate length, are also welcome.

General informations

1. Authors should use SI units and provide alternative units in parentheses wherever necessary.
2. Figures should be included in the text and provided separately in TIFF, PCX, JPG or GEM format.
3. Contributions may be written and will be published in Slovene or English language.
4. Authors are fully responsible for the content of the paper.

Contributions are to be sent electronically to:

editor@midem-drustvo.si

Informacije MIDEM - Journal of Microelectronics, Electronic Components and Materials je znanstveno-strokovno-društvena publikacija Strokovnega društva za mikroelektroniko, elektronske sestavne dele in materiale - MIDEM. Revija objavlja prispevke s področja mikroelektronike, elektronskih sestavnih delov in materialov. Ob oddaji člankov morajo avtorji predlagati uredništvu razvrstitev dela v skladu s tipologijo za vodenje bibliografij v okviru sistema COBISS.

Znanstveni in strokovni prispevki bodo recenzirani.

Znanstveno-strokovni prispevki morajo biti pripravljene na naslednji način:

1. Naslov prispevka, imena in priimki avtorjev brez titula, imena institucij in podjetij.
2. Ključne besede in povzetek (največ 250 besed).
3. Naslov dela v angleščini.
4. Ključne besede v angleščini (Key words) in podaljšani povzetek (Extended Abstract) v angleščini, če je članek napisan v slovenščini.
5. Uvod, glavni del, zaključek, zahvale, dodatki in literatura v skladu z IMRAD shemo (Introduction, Methods, Results And Discussion).
6. Na koncu dodajte polna imena in priimki avtorjev s titulami, naslovi institucij in firm, v katerih so zaposleni ter tel./Fax/Email podatki.
7. Prispevki naj bodo napisani v MS Word (.doc ali .docx) ali OpenDocument (.odt ali .fodt) formatu v enem stolpcu z velikostjo črk 12pt. Priporočena dolžina članka je 12-15 strani brez slik.

Ostali prispevki, kot so poljudni članki, aplikacijski članki, novice iz stroke, vesti iz delovnih organizacij, inštitutov in fakultet, obvestila o akcijah društva MIDEM in njegovih članov ter drugi prispevki so dobrodošli.

Ostala splošna navodila

1. V prispevkih je potrebno uporabljati SI sistem enot oz. v oklepaju navesti alternativne enote.
2. Risbe in slike naj bodo vključene v tekst in priložene ločeno v formatu TIFF, PCX, GEM ali JPG.
3. Prispevek je lahko napisan in bo objavljen v slovenščini ali v angleščini.
4. Avtorji so v celoti odgovorni za vsebino objavljenega sestavka.

Prispevke pošljite po elektronski pošti na:

editor@midem-drustvo.si

Boards of MIDEM Society | Organi društva MIDEM

MIDEM Executive Board | Izvršilni odbor MIDEM

President of the MIDEM Society | Predsednik društva MIDEM

Prof. Dr. Marko Topič, University of Ljubljana, Faculty of Electrical Engineering, Slovenia

Vice-presidents | Podpredsednika

Prof. Dr. Barbara Malič, Jožef Stefan Institute, Ljubljana, Slovenia

Dr. Iztok Šorli, MIKROIKS, d. o. o., Ljubljana, Slovenija

Secretary | Tajnik

Olga Zakrajšek, UL, Faculty of Electrical Engineering, Ljubljana, Slovenija

MIDEM Executive Board Members | Člani izvršilnega odbora MIDEM

Prof. Dr. Slavko Amon, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia

Darko Belavič, In.Medica, d.o.o., Šentjernej, Slovenia

Prof. Dr. Bruno Cvikl, UM, Faculty of Civil Engineering, Maribor, Slovenia

Prof. Dr. Leszek J. Golonka, Technical University Wroclaw, Poland

Leopold Knez, Iskra TELA d.d., Ljubljana, Slovenia

Dr. Miloš Komac, UL, Faculty of Chemistry and Chemical Technology, Ljubljana, Slovenia

Prof. Dr. Marija Kosec, Jožef Stefan Institute, Ljubljana, Slovenia

Prof. Dr. Miran Mozetič, Jožef Stefan Institute, Ljubljana, Slovenia

Jožef Perne, Zavod TC SEMTO, Ljubljana, Slovenia

Prof. Dr. Giorgio Pignatelli, University of Perugia, Italia

Prof. Dr. Janez Trontelj, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia

Supervisory Board | Nadzorni odbor

Prof. Dr. Franc Smole, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia

Mag. Andrej Piriš, Iskra-Zaščite, d. o. o., Ljubljana, Slovenia

Dr. Slavko Bernik, Jožef Stefan Institute, Ljubljana, Slovenia

Court of honour | Častno razsodišče

Emer. Prof. Dr. Jože Furlan, UL, Faculty of Electrical Engineering, Slovenia

Prof. Dr. Radko Osredkar, UL, Faculty of Computer and Information Science, Slovenia

Franc Jan, Kranj, Slovenia

Informacije MIDE

Journal of Microelectronics, Electronic Components and Materials

ISSN 0352-9045

Publisher / Založnik:

MIDEM Society / Društvo MIDE

Society for Microelectronics, Electronic Components and Materials, Ljubljana, Slovenia

Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale, Ljubljana, Slovenija

www.midem-drustvo.si