

INFLUENCE OF MOSFET MODEL FORM ON CHARACTERISTICS OF THE BOOST CONVERTER

Krzysztof Górecki, Janusz Zarębski

Department of Marine Electronics, Gdynia Maritime University, Poland

Key words: MOS transistors, BOOST converters, modelling

Abstract: In the paper boost converter characteristics at the steady state obtained from SPICE analysis with the use of selected kinds of MOSFET models of various complexity and accuracy are compared. The dependencies of the converter output voltage, the watt-hour efficiency and the MOSFET inner temperature on the frequency and the duty cycle of the MOSFET control signal as well as the converter load resistance are considered. The correctness of the calculation results was verified experimentally. The duration time of the analyses corresponding to all the considered models of the MOS transistor are compared, too.

Vpliv modela MOSFET tranzistorja na karakteristike ojačitvenega pretvornika

Ključne besede: V članku primerjamo statične karakteristike pretvornika pridobljene s SPICE simulacijo z uporabo izbranih MOSFET modelov različnih kompleksnosti in natančnosti. Opišemo odvisnost izhodnih napetosti, učinkovitost ter MOSFET temperaturo od frekvence kontrolnega signala in bremenske upornost. Pravilnost dobljenih rezultatov smo preverili tudi eksperimentalno. Primerjali smo tudi čase simulacije v odvisnosti od uporabljenih modelov.

Izveček: MOS tranzistorji, pretvorniki, modeliranje

1. Introduction

Dc-dc converters are commonly used in power supply systems /1/. The boost converter is the most popular in the class of step-up converters of the output power up to 1 kW. The network representation of the boost converter with the MOS power transistor operating as the switch is shown in Fig.1.

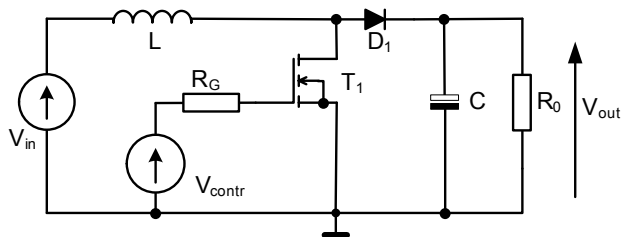


Fig. 1. The diagram of a boost converter

The analysis and design of electronic circuits e.g. dc-dc converters requires the use a proper computer tool (algorithms). To this end SPICE is the appropriate tool /2, 3/. The accuracy and duration time of calculations depend among others on the form of models of semiconductor devices and elements existing in the considered circuit.

The characteristics describing dc-dc converters at the steady state have a fundamental significance for the engineer-designer of such a class of circuits. Two groups of methods of the analysis of dc-dc converters at the steady

state can be distinguished. The first method is based on the dc analysis with average models of the analysed circuit taken into account /4-8/, whereas in the other method based on the transient analysis, the large-signal dynamic models of devices operating in the circuit are used /2, 4, 7, 9/. As it was shown in /10/, the second method allows obtaining much better consistency between the calculation and measuring results, but the analysis duration time can be much longer than in the first method.

There are models of different accuracy, among of both kinds of models mentioned before. For example, in the paper /11/ the results of the analysis of the isolated dc-dc converter obtained by nonlinear inertial models of the Schottky diode and the MOS transistor are presented. In turn, the paper /12/ presents the results of a small-signal analysis of the buck-boost converter obtained with the use of devices models of the form of ideal switches. In the paper /13/ the results of the analysis of the dc-dc converter obtained by the SPICE built-in models of the diode and the MOS transistor were used as the reference results to verify the correctness of the new method of calculations of converter characteristics. The description of the behavioral dc-dc converter models of different accuracy dedicated to the system level analysis can be found in /14/. The similar meaning is to be found in the models presented in the paper /15/, whose parameters values can be estimated with the use of the catalogue data of converter devices. The paper /16/ describes the method of estimation of the electrothermal characteristics of dc-dc converters with the

use of the method of the separated iteration with the use of nonlinear semiconductor devices models. The nonlinear models of semiconductor devices were also used in the analysis of a dc-dc converter in the small-signal /17/ and large-signal /18/ case, respectively. The average models of dc-dc converters with nonlinearities of semiconductor devices taken into account are described in /19, 20/.

The aim of this paper, being of the extended version of the paper /21/, is to estimate the influence of the form of the MOS transistor model on the boost converter characteristics at the steady state obtained by the transient analysis. The analyses were performed by SPICE with the use of SPICE built-in linear models of: the inductor L, the capacitor C, the resistors R_0 , R_G , the voltage sources V_{in} , V_{contr} and the model of the diode D1 described in /22/. Five various models of MOS transistor were tested. Namely: the model of the ideal switch, the Dang's model built-in in SPICE, the two-value resistor model, the electrothermal model of the two-value resistor /23/ and the electrothermal hybrid model of the considered device /24/. The results of the analysis of the form of the proper characteristics of the boost converter and the duration time of the analyses performed with the use of the above mentioned MOS transistor models are presented and compared. The calculations were performed in the wide range of variations of the duty cycle D and the frequency f of the control signal as well as the load resistance R_0 . Some results of the analyses were compared with the results of measurements.

2. MOSFET models used in analyses

The simplest model of the MOS transistor, among the considered models, is the ideal switch model, whose switch-on and switch-off resistances are equal to zero and infinity, respectively. The main drawback of this model is discontinuity of their characteristics, which can result in the problem of the lack of calculations convergence. Such a model cannot be directly implemented in SPICE. On the other hand, the SPICE built-in model of the voltage controlled switch (VSWITCH) with switch-on and switch-off resistances of the values, which tend to be zero and infinity respectively, can be used.

The second in turn considered model is the two-value resistor model, which possesses non-zero value resistance in the on-state (R_{ON}) and the finite value of the resistance in the off-state (R_{OFF}). In this model the values of the resistances R_{ON} and R_{OFF} are independent of temperature.

These models are formulated in SPICE with the use of the model of the voltage controlled switch, the characteristics of which are described by the four parameters: the resistances R_{ON} , R_{OFF} and the voltages V_{ON} , V_{OFF} – representing the device gate-source voltage at the device on-state and off-state, respectively.

The third model of the MOS transistor is the electrothermal model of the switch /24/. This model is an improved version

of the two-value resistor model, in which the influence of the ambient temperature and the selfheating phenomenon on the resistance R_{ON} are included. This model, the network representation of which is shown in Fig.2, is composed of two elements connected in series: the SPICE built-in model of the voltage controlled switch S1 (the two-values resistor) and the voltage controlled source E_{RON} described by the formula

$$E_{RON} = V_{S1} \cdot \alpha_{RON} \cdot (R_{th} \cdot I \cdot V_S - T_0 + T_a) \quad (1)$$

where V_S denotes the voltage on the two-values resistor, V_{S1} – the voltage on the switch S_1 , T_a – ambient temperature, R_{th} – the thermal resistance of the transistor, I – the current of the two-value resistor, α_{RON} – the temperature coefficient of variations of the on resistance of the two-values resistor. The resistance of the switched-on switch S_1 is equal to the resistance R_{ON0} corresponding to the on-resistance of the two-values resistor at the reference temperature T_0 .

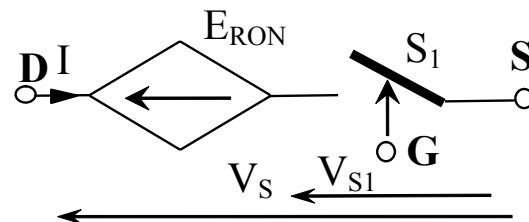


Fig.2. The network representation of the two-values resistor model

Both the electrical inertia and nonlinearity of the device current-voltage characteristics are not included in the presented models.

The next is the Dang's isothermal model of the MOS transistor built-in in SPICE, described e.g. in /22/. This model takes into account the nonlinear d.c. characteristics and the inertia of the considered device, whereas the selfheating phenomenon is not taken into account in this model. There are 28 parameters describing the Dang's model /22/. These parameters are: model index (LEVEL), default channel length (L), default channel width (W), drain ohmic resistance (RD), source ohmic resistance (RS), gate ohmic resistance (RG), bulk/substrate ohmic resistance (RB), zero-bias bulk-drain junction capacitance (CBD), zero-bias bulk-source junction capacitance (CBS), bulk junction saturation current (IS), Bulk junction saturation current per sq-meter of junction area (JS), Bulk junction saturation current per length of sidewall area (JSSW), bulk junction emission coefficient (N), bulk junction potential (PB), bulk junction sidewall potential (PBSW), gate-source overlap capacitance per meter channel width (CGSO), gate-drain overlap capacitance per meter channel width (CGDO), gate-bulk overlap capacitance per meter channel length (CGBO), drain and source diffusion sheet resistance (RSH), Zero-bias bulk junction bottom capacitance per square meter of junction area (CJ), zero-bias bulk junction sidewall capacitance per length of sidewall (CJSW),

bulk junction bottom grading coefficient (MJ), zero-bias bulk junction sidewall capacitance per meter of junction perimeter (CJSW), bulk junction sidewall grading coefficient (MJSW), bulk junction transit time (TT), flicker noise coefficient (KF), flicker noise exponent (AF), coefficient for forward-bias depletion capacitance formula (FC), zero-bias threshold voltage (VTO), transconductance parametr (KP), bulk threshold parameter (GAMMA), surface potential (PHI), oxide thickness (TOX), substrate doping (NSUB), surface state density (NSS), fast surface state density (NFS), type of gate material (TPG), metallurgical junction depth (XJ), lateral diffusion (LD), lateral diffusion width (WD), surface mobility (UO), critical field for mobility degradation (UCRIT), critical field exponent in mobility degradation (UEXP), transverse field coefficient (UTRA), maximum drift velocity of carriers (VMAX), total channel charge coefficient (NEFF), thin-oxide capacitance model flag and a fraction of channel charge attributed to drain (XQC), width effect on threshold voltage (DELTA), mobility modulation (THETA), static feedback (ETA) and saturation field factor (KAPP).

The last one is the electrothermal hybrid model of the MOS transistor proposed by the authors in [24], the network representation of which is shown in Fig.3. This model consists of the Dang's model (SBM) and two controlled voltage sources E_G and E_{RD} modelling the influence of selfheating on the device threshold voltage and its drain resistance, respectively. The voltages on these sources are expressed by

$$E_{RD} = i_D \cdot R_D \cdot \alpha_{RD} (T_j - T_0) \quad (2)$$

$$E_G = \alpha_U (T_j - T_0) \quad (3)$$

In the analytical description of these sources (Eqs (2-3)) the temperature coefficients of variations of both the threshold voltage α_U and the drain series resistance α_{RD} , appear. The internal temperature T_j of the transistor is given by

$$T_j = T_a + R_{th} \cdot v_{DS} \cdot i_D \quad (4)$$

where i_D denotes the drain current and v_{DS} is the drain-source voltage.

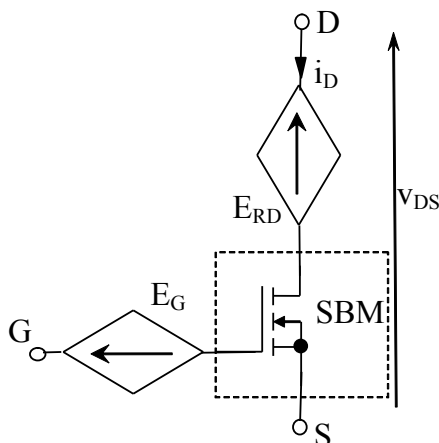


Fig.3. The circuit representation of the electrothermal hybrid model of the MOSFET transistor

The boost converter (Fig.1) with transistor IRF840, the diode BY229, the inductor of inductance 650 μ H, and the capacitor of capacitance 47 μ F was investigated.

In the considered MOS transistors models the values of the parameters collected in Table 1 were used.

Table 1. The values of parameters of the considered MOS transistor IRF840 models

Dang's model (curve b)							
parameter	LEVEL	KAPPA	TOX	UO	PHI	RS	KP
value	3	0.2	100 nm	600 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$	0.6 V	6.382 m Ω	20.85 $\mu\text{A}/\text{V}^2$
parameter	W	L	VTO	RD	TT	RDS	CBD
value	0.68 m	2 μm	3.879 V	0.6703 Ω	710 ns	2.222 M Ω	1.415 nF
parameter	PB	MJ	IS	CGSO	CGDO	RG	
value	0.8 V	0.5	56 pA	1.625 nF/m	133.4 pF/m	0.6038 Ω	
Additional parameters of the electrothermal hybrid model (curve a)							
parameter	α_U	α_{RD}					
value	-3 mV/K	10 ⁻² K ⁻¹					
Twovalue-resistor model (curve d)							
parameter	R _{ON}	R _{OFF}	V _{ON}	V _{OFF}			
value	0.67 Ω	1 M Ω	14 V	1V			
ideal switch model (curve c)							
parameter	R _{ON}	R _{OFF}	V _{ON}	V _{OFF}			
value	1 $\mu\Omega$	1 M Ω	14 V	1V			
Electrothermal model of a two-values resistor (curve e)							
parameter	R _{ONO}	R _{OFF}	V _{ON}	V _{OFF}	α_{RON}		
value	0.67 Ω	1 M Ω	14 V	1V	10 ⁻² K ⁻¹		

To estimate the correctness of the considered models, in Fig.4 the calculated and measured output characteristics $i_D(v_{DS})$ of the transistor IRF840 at $v_{GS} = 15$ V are presented. In this figure (and in the further ones) the points denote the measuring results, whereas the lines – the results of the analysis. In Fig.4 the following notations are used: a – the electrothermal hybrid model of the considered transistor, b – the isothermal built-in in SPICE Dang's model, c – the ideal switch model, d – the isothermal model of the two-

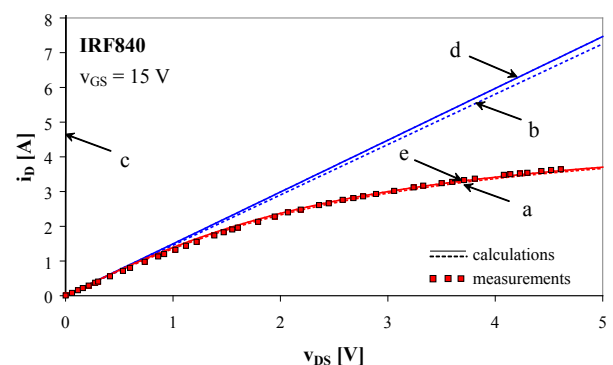


Fig. 4. Calculated and measured dc output characteristics of the transistor IRF840

value resistor, e – electrothermal model of the two-value resistor.

As seen from Fig.4, the characteristic corresponding to the ideal switch (the characteristic c covers the vertical axis of ordinates) differ essentially from the remaining characteristics (curves a, b, d, e). In turn, the characteristics calculated with the device isothermal model (curve b) and with the model of two-value resistor (curve d) are practically identical and linear in the considered range of variations of the drain current. The characteristics corresponding to the models including selfheating (the curves a and e) are nonlinear and practically overlap. The characteristics a and e show that selfheating evidently results in an increase of the device resistance R_{ON} .

3. Results

Using the considered models of the MOS transistor (Section II) the transient analysis of the boost converter (Fig.1) up to the steady state for various values of the load resistance R_0 , the duty cycle D and the frequency f of the device control signal, was performed. The influence of these parameters (R_0 , D , f) on the output voltage and the watt-hour efficiency of the converter as well as the MOS transistor case temperature was investigated. During the measurements the MOS transistor and the diode were situated on the heat-sinks. The value of the thermal resistance of the MOS transistor measured with the use of the measuring method from /25/ and the measuring set described in /26/ is equal to 5.5 K/W. The measurements of characteristics were carried out by typical multimeters at the thermal steady-state, whereas the device case temperature was measured by the pyrometer ST-3. In the analysis the SPICE built-in isothermal model of the p-n diode with the following parameter values (corresponding to the diode BY229): $I_s = 53.4 \text{ pA}$, $N = 1.185$, $R_S = 0.12 \text{ } \Omega$, $\text{trs1} = 3 \cdot 10^{-3} \text{ K}^{-1}$, $I_{kf} = 3.5 \text{ mA}$, $C_{jo} = 325 \text{ pF}$, $M = 0.3333$, $V_j = 0,75 \text{ V}$, $F_c = 0.5$, $I_{sr} = 100 \text{ pA}$, $N_r = 2$, $TT = 145 \text{ ns}$ was used. In the analysis the inductor series resistance of the value equal to $0.1 \text{ } \Omega$ was taken into account.

The transient analyses of the considered circuit until the steady-state were performed with the use of all the models described in Chapter III. The calculated values of the converter output voltage V_{out} , the watt-hour efficiency η , and the case temperature T_{cr} are shown in Figs. 5 -7.

In Fig.5 the results of the calculated and measured dependences of the output voltage and the watt-hour efficiency of the considered converter and the MOS transistor case temperature on the duty cycle D of the gate control signal at the frequency $f = 108.7 \text{ kHz}$ and the load resistance $R_0 = 20 \text{ } \Omega$ are presented.

As seen from Fig.5, the results of analysis with the use of the electrothermal hybrid model of the MOS transistor (curve a) and the electrothermal model of the two-values resistor (curve e) fit well to the measuring results. Neglecting the

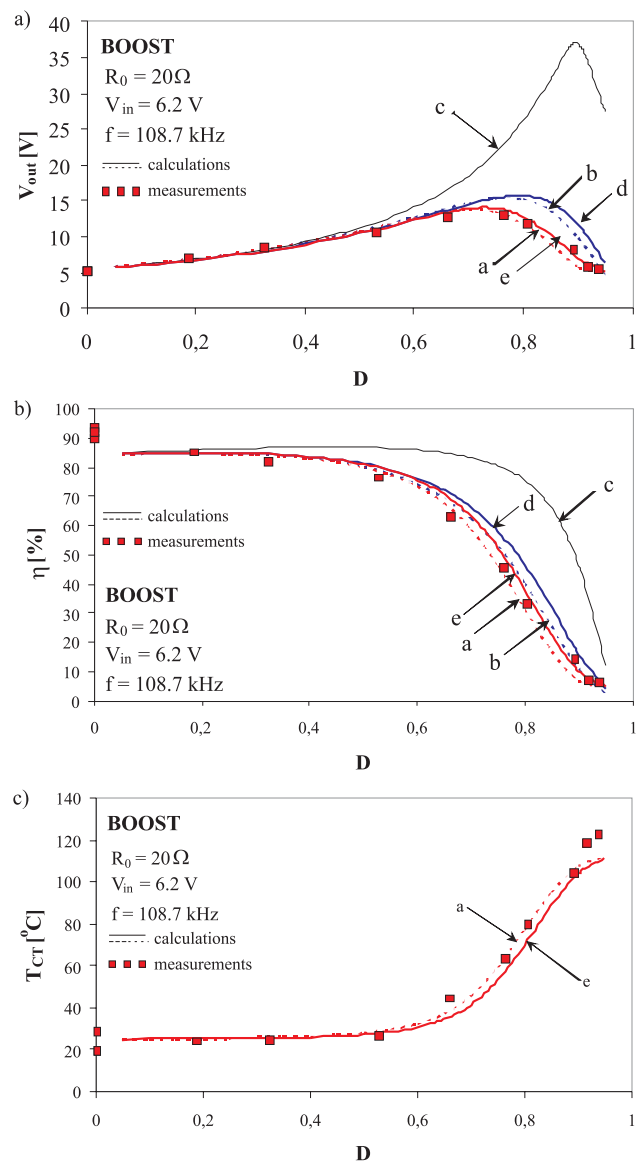


Fig. 5. The calculated and measured dependences of the output voltage (a), the watt-hour efficiency (b) of the converter and the transistor case temperature (c) on the duty-factor of the control signal

selfheating phenomenon in the MOS transistor (curves b and d) results in too high values of the converter output voltage and shifts of the maximum on the characteristic $V_{out}(D)$ towards the higher values of the coefficient D . In turn, neglecting conducting losses in the transistor (curve c) results in a considerable increase of the converter output voltage. It is worth mentioning that the differences between the values of the voltage V_{out} obtained with the use of all the considered models are hardly visible at small values of the coefficient D ($D < 0.4$). Moreover, these differences increase with an increase of D .

As seen from Fig.5b the dependence $\eta(D)$ is a decreasing function. The best agreement between the analysis and measuring results is assured by the MOS transistor models with a electrical inertia and selfheating taken into account

(curves a, b, d, e). Disregarding conducting losses in the MOS transistor results in a considerable increase of the watt-hour efficiency of the converter.

It results from Fig.5c that the case temperature T_{CT} of the MOS transistor is an increasing function of the coefficient D and the values of T_{CT} obtained with the use of the both electrothermal models (curves a and e) fit well to the measurements.

In Fig.6 the calculated and measured values of the converter output voltage (Fig.4a) and the watt-hour efficiency (Fig.4b) as well as the MOS transistor case temperature (Fig.4c) on the converter load resistance at $D = 0.5$ and $f = 100$ kHz are presented.

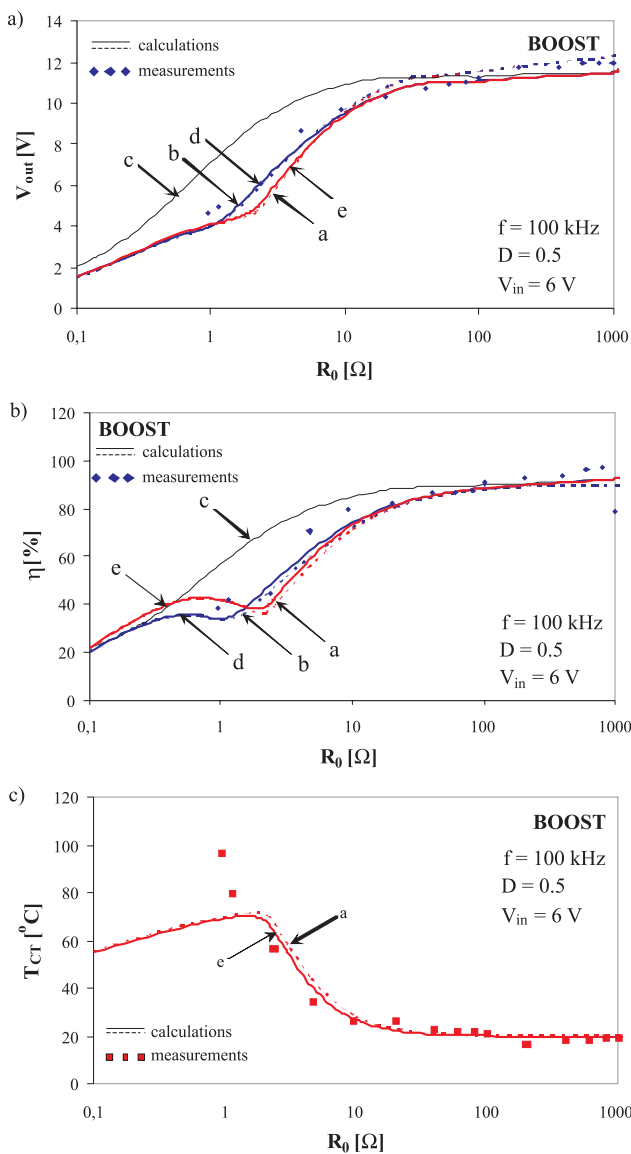


Fig. 6. The calculated and measured dependences of the converter output voltage (a) and the watt-hour efficiency (b), as well as the transistor case temperature (c) on the load resistance.

Fig. 6a shows that the converter output voltage is an increasing function of the resistance R_0 . In the range of small

values of the load resistance ($R_0 < 2 \Omega$) the considered converter operates incorrectly, that means that $V_{out} < V_{in}$.

It results from Fig.6b that a decrease of the resistance R_0 leads to a decrease of the converter watt-hour efficiency. It is worth mentioning that the dependences $\eta(R_0)$ obtained with the use of the models taking into account the MOS transistor conducting losses (curves a, b, d, e) have local minimums and local maximums (peaks) at the load resistance values in the range from 0.5Ω to 2Ω . Neglecting the conducting losses in the MOS transistor results in an increase of both the output voltage and the watt-hour efficiency of the converter even more than 50%.

Fig.6c shows that the measured values of the case temperatures of the MOS transistor fit well to the calculated values at $R_0 < 1.5 \Omega$ only. The measured characteristic $T_{CT}(R_0)$ is a monotonically decreasing function, whereas the same characteristic obtained from the calculations has the peak at $R_0 = 1.5 \Omega$.

In Fig.7 the influence of the frequency f of the signal controlling the MOS transistor on the converter output voltage (Fig.7a) and the watt-hour efficiency (Fig.7b) as well as the case temperature of the MOS transistor (Fig.5c) is presented. The calculations and measurements were performed at $D = 0.75$ and $R_0 = 20 \Omega$.

It results from Fig.7a that the voltage V_{out} is a decreasing function of the frequency f . This dependence is described correctly by the electrothermal hybrid model of the MOS transistor (curve a) only. The values of the voltage V_{out} obtained from the remaining models are inflated. For the signal frequency $f > 1$ MHz the investigated converter does not operate correctly due to too high values of the MOS transistor inner capacitances, which make the proper switching of the MOS transistor impossible. The values of the voltage V_{out} corresponding to this range of the signal frequency are equal to the difference of the converter input voltage and the voltage drop on the forward biased diode D . As seen, the model of the two-value resistor ensures the correct values of the voltage V_{out} if the signal frequency is less than 150 kHz only.

It results from Fig.7b that increasing of the signal frequency f causes increasing of the converter watt-hour efficiency up to a few percentage only in the range of the frequency $f > 1$ MHz. This phenomenon is observed from the calculation results obtained with the use of all the considered models, because in all the analyses the diode inertia is taken into account.

Fig.7c shows that the electrical power dissipated while switching the MOS transistor influences substantially the device case temperature T_{CT} in the range of higher values of the frequency of the MOS transistor controlling signal. The values of the temperature T_{CT} obtained with the use of both the considered electrothermal models differ from each other even more than 30%. The temperature T_{CT} doubles when the signal frequency f increases from 100 kHz to 5 MHz.

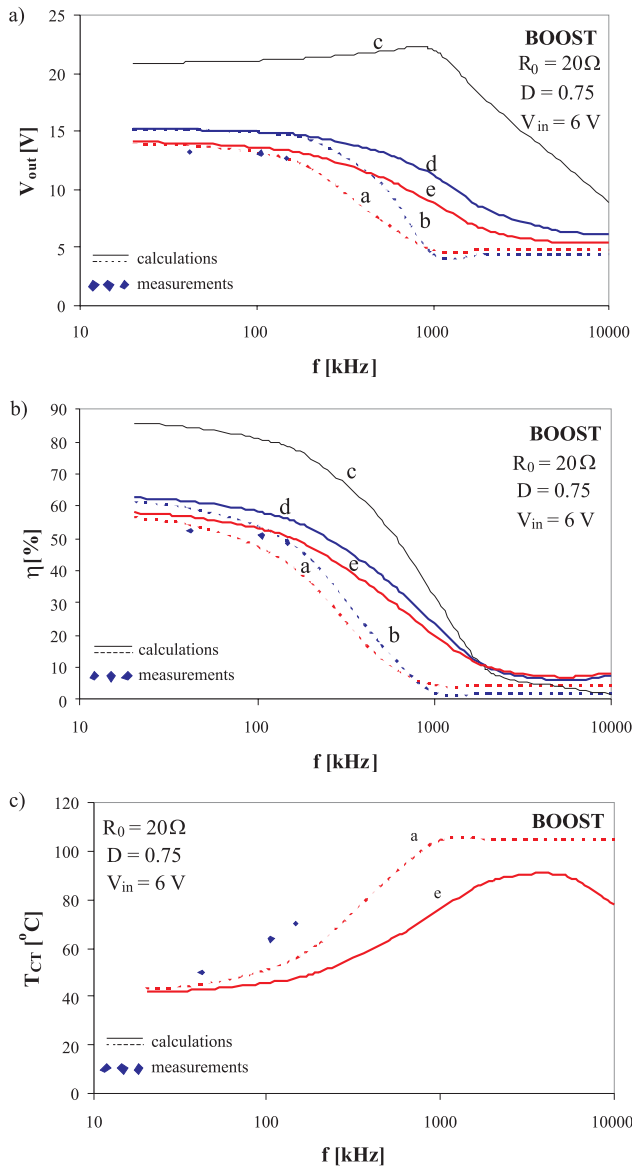


Fig. 7. The calculated and measured dependences of the converter output voltage (a) and the watt-hour efficiency (b) as well as the transistor case temperature (c) on the frequency of the control signal

Apart from the model accuracy, the time of the converter analysis with the use of these models gives also very important information about the usefulness of the models. Table 2 compares the times (in seconds) of the analysis of the boost converter with the use of the considered MOS transistor models.

As seen from Table 2, in the range of small values of the frequency of the control signal, the isothermal model of the two-value resistor ensures the shortest time of the analysis – more than twice shorter than the analysis time with the use of the hybrid electrothermal model. In turn, in all the considered range of variations of the frequency f , the isothermal built-in model of the MOS transistor is the best from the point of view of the analysis rate. In this case the time indispensable for the analysis is twice lower than in the case, when the models of the ideal switch or two-values resistance are used. It is worth mentioning that the model of the worst accuracy (the model of the ideal switch) does not ensure the shortest time of the analysis. This results from the fact, that during switching of the non-inertia switch, very fast changing of the currents and voltages are observed. In a consequence, the time derivatives of currents and voltages of the high values appear, what results in shortening of the calculating step. Finally, the time of analysis have to be increased.

4. Conclusions

In the paper the influence of the model form of the MOS transistor on the characteristics of the boost converter is investigated. As results from the investigations performed by the authors, using the device electrothermal hybrid model ensures a good agreement between the calculated and measured characteristics of the considered dc-dc converter in the wide range of variations of the load resistance, the duty-factor and the frequency of the control signal of the MOS transistor.

If the control signal frequency is less than 150 kHz, then the electrothermal model of the two-value resistor ensures a good agreement between the calculation and measurement results and moreover the analysis time is twice shorter than in the case of the use of the electrothermal hybrid model of the MOS transistor.

For the low values of the MOS transistor control signal frequency and small values of the converter load resistance, selfheating has to be included in the model, whereas it is indispensable for the high values of the control signal frequency to take to account the MOS transistor electrical inertia.

The presented results of the boost converter investigations show that for the control signal frequency less than 150 kHz the inertia can be omitted in the devices models, whereas the static losses in these devices at the on-state

Table 2. Times of the boost converter analysis with the use of the considered MOS transistor models

Characteristic	Hybrid electrothermal model	Isothermal built-in model	Ideal switch	Two-value resistor	Electrothermal two-value resistor
$V_{out}(D)$	161.77 s	125.83 s	70.28 s	67.11 s	87.17 s
$V_{out}(R_0)$	366.05 s	289.55 s	148.10 s	126.06 s	165.24 s
$V_{out}(f)$	281.08 s	232.69 s	513.84 s	418.22 s	504.78 s

play the essential role. Therefore a very important challenge would be working out an electrothermal large-signal model of the transistor switch with the inertia phenomena taken into account.

References

- /1/ M.H. Rashid, "Power Electronic Handbook", Academic Press, Elsevier, 2007.
- /2/ N. Mohan, W. P. Robbins, T. M. Undeland, R. Nilssen, O. Mo, "Simulation of Power Electronic and Motion Control Systems - An Overview", Proceedings of the IEEE, Vol. 82, 1994, pp. 1287-1302.
- /3/ M.H. Rashid, H. M. Rashid, SPICE for Power Electronics and Electric Power, Taylor & Francis, 2006.
- /4/ Górecki K.: Non-linear average electrothermal models of buck and boost converters for SPICE. Microelectronics Reliability, Vol. 49, no.4, 2009, pp. 431-437.
- /5/ R. Ericson, D. Maksimovic, "Fundamentals of Power Electronics", Norwell, Kluwer Academic Publisher, 2001.
- /6/ D. Maksimovic, A. M. Stankovic, V.J.Thottuvelil, G.C. Verghese, "Modeling and simulation of power electronic converters", Proceedings of the IEEE, Vol. 89, No. 6, 2001, pp. 898-912.
- /7/ Ch. P. Basso, "Switch-Mode Power Supply SPICE Cookbook", New York, McGraw-Hill, 2001.
- /8/ S. Ben-Yaakov: Average simulation of PWM converters by direct implementation of behavioural relationships. International Journal of Electronics, Vol. 77, No. 5, 1994, pp. 731-46.
- /9/ J. Vlach, A. Opal: Modern CAD methods for analysis of switched networks. IEEE Transactions on Circuits and Systems - I: Fundamental Theory and Applications, Vol. 44, No. 8, 1997, pp. 759-762.
- /10/ K. Górecki, J. Zarębski: Investigations of the Usefulness of Average Models for Calculations Characteristics of Buck and Boost Converters at the Steady State. International Journal of Numerical Modelling Electronic Networks, Devices and Fields, Vol.23, No.1, 2010, pp. 20-31.
- /11/ R. Simanjorang, H. Yamaguchi, H. Ohashi, T. Takeda, H. Murai, M. Yamasaki, "Estimating performance of high output power density 400/400V isolated DC/DC converter with hybrid pair SJ-MOSFET and SiC-SBD for power supply of data center", 31st International Telecommunications Energy Conference, INTELEC 2009, 2009. pp. 1-5.
- /12/ A. Reatti, M. Balzani, "Computer aided small-signal analysis for PWM DC-DC converters operated in discontinuous conduction mode", 48th Midwest Symposium on Circuits and Systems, 2005, Vol. 2, pp. 1561 - 1564.
- /13/ B.P. Divakar, K.W.E. Cheng, D. Sutanto, Shi Zhanghai K.F. Kwok, "The use of power factor and K-factor as goodness factors in the analysis of dc-dc converters", Australasian Universities Power Engineering Conference, AUPEC '08, 2008, pp. 1 - 6.
- /14/ R. Prieto, L. Laguna-Ruiz, J.A. Oliver, J.A. Cobos, "Parameterization of DC/DC converter models for system level simulation", 2007 European Conference on Power Electronics and Applications, 2007, pp. 1-10.
- /15/ R. Prieto, L. Laguna, J.A. Oliver, J.A. Cobos, "DC/DC Converter Parametric Models for System level Simulation", Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, APEC 2009, pp. 292-297.
- /16/ M. Vellvehi, X. Jorda, P. Godignon, J. Millan, "Electro-thermal Simulation of a DC/DC Converter using a Relaxation Method", 7th International Conference on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, EuroSime 2006, pp. 1-7.
- /17/ J.H. Ly, K. Siri, "Frequency response analysis for DC-DC converters without small-signal linearization", Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition APEC '03, 2003., Vol. 2, pp. 1008-1013.
- /18/ F. Alonge, F. D'Ippolito, F. M. Raimondi, S. Tumminaro, "Non-linear Modeling of DC/DC Converters Using the Hammerstein's Approach", IEEE Transactions on Power Electronics, Vol. 22, No. 4, 2007, pp.1210 - 1221.
- /19/ S. Abid, A. Ammous, "Average modeling of DC-DC and DC-AC converters including semiconductor device non-linearities", International Conference on Design and Test of Integrated Systems in Nanoscale Technology DTIS 2006, pp. 384 - 389.
- /20/ P. Chrin, C. Bunlaksananusorn, "Large-Signal Average Modeling and Simulation of DC-DC Converters with SIMULINK", Power Conversion Conference - Nagoya PCC '07, 2007, pp. 27-32.
- /21/ K. Górecki, J. Zarębski: Influence of MOSFET Model Form on Boost Converter Characteristics at the Steady State. 16th International Conference Mixed Design of Integrated Circuits and Systems MIXDES 2009, Łódź, 2009, p. 162.
- /22/ B.M. Wilamowski, R.C. Jaeger, "Computerized circuit Analysis Using SPICE Programs", McGraw-Hill, New York, 1997.
- /23/ K. Górecki, "A New Electrothermal Average Model of the Diode-Transistor Switch", Microelectronics Reliability, Vol. 48, No. 1, 2008, pp. 51-58.
- /24/ K. Górecki, J. Zarębski, "Modeling Nonisothermal Characteristics of Switch-Mode Voltage Regulators", IEEE Transactions on Power Electronics, Vol. 23, No. 4, 2008, pp. 1848 - 1858.
- /25/ F. F. Oettinger, D. L. Blackburn, "Semiconductor Measurement Technology: Thermal Resistance Measurements", U. S. Department of Commerce, NIST/SP-400/86, 1990.
- /26/ K. Górecki, J. Zarębski, „System mikrokomputerowy do pomiaru parametrów termicznych elementów półprzewodnikowych i układów scalonych”, Metrologia i Systemy Pomiarowe, t. VIII, Nr 4, 2001, ss. 379-396. (in Polish)

*Prof. Krzysztof Górecki
Prof. Janusz Zarębski*

*Gdynia Maritime University
Department of Marine Electronics
Morska 83, 81-225 Gdynia, POLAND,
Tel. ++48 58 6901448, ++48 58 6901599,
fax ++48 58 6217353
E-mail: gorecki@am.gdynia.pl, zarebski@am.gdynia.pl*

Prispelo: 17.03.2010

Sprejeto: 03.03.2011