FLEXIBLE LOW COST ASIC DESIGN VERIFICATION TOOL WITH GUIDELINES FOR GENERATION OF STDF FOR MULTI PROJECT WAFER SORT

Janez Trontelj jr.

Faculty of Electrical Engineering, Ljubljana, Slovenia

Key words: Wafer sort, ASIC, ATDF, STDF, DAQ Card

Abstract: This article describes practical, low cost approach for sensitive, analog or mixed signal application specific integrated circuit (ASIC) design verification. Step by step is described how to solve the problems about wafer sort on multi-project wafers, how to select appropriate low cost test hardware and suitable operating system platform. All these actions are performed with one main goal in mind to speed up the measurements. It is also described in detail how to achieve test data compatibility with several commercial automatic statistical analysis tools. Entire critical parameter verification process was also practically implemented on very high sensitive ASIC for industrial application and complies with strict automotive standards.

Hitro prilagodljiv in cenovno ugoden testni system za analizo ustreznosti vezij ASIC s priporočili za generiranje STDF datotek na več projektnih silicijevih rezinah

Kjučne besede: Testiranje silicijevih rezin, Vezja po naročilu, ATDF, STDF, DAQ kartica

Izvleček: Članek opisuje praktičen, nizko cenovni pristop za merjenje občutljivih, analognih oziroma analogno-digitalnih sklopov na integriranih vezjih po naročilu. Korak za korakom so opisane tudi rešitve problema testiranja več projektnih silicijevih rezin, kako izbrati primerne testne naprave z ustreznimi operacijskimi sistemi za pospešitev hitrosti zajemanja meritev. Podrobno je opisan tudi način, kako generirati testne podatke, ki so kompatibilni z večino orodij za avtomatsko statistično analizo izmerjenih parametrov. Celoten proces raziskave kritičnih parametrov visoko občutljivega integriranega vezja po naročilu za industrijsko aplikacijo je bil praktično preizkušen in ustreza strogim standardom, ki so predpisani za avtomobilsko industrijo.

1. Introduction

A proper operation of sensitive, analog or mixed signal application specific integrated circuits for microelectronic systems is often influenced by so many parameters that sometimes can't be predicted only by expertise and simulation tools. In such cases, it is a good practice to utilize low cost multi-project wafer production service, which is offered by major semiconductor houses. Schedules for nowadays microelectronics projects are by default very tight. Quick response is critical, when such multi-project wafer is received for design specification evaluation. Usually several ten thousand parts must be evaluated, before new design corrections may be justified and determined. Evaluation time for each part should be well below one second and total control of measurement process is required. It is quite common that several thousand measurements are necessary just for one part characterization in less than one second time frame. The most time efficient way to accomplish this goal is to do measurements directly on silicon wafer /1//2/, to eliminate the device packaging delay. Of course sometimes also package effect must be considered. This even further confirms the described approach, because results on the wafer sort can be later easily compared to the packaged parts measurement results.

There are certainly several software packages for test and automated measurements available on the market. The problem is that in general they are too universal and therefore too bulky. The outcome is relatively slow data acquisition. Sometimes only preparation for one measurement task takes approximately 100 times more time than it is requested for both - preparation and measurement. In this article our approach will be described for low cost and fast wafer sort measurements on multi-project wafers. At the end we will also introduce how to achieve test data compatibility with commercial automatic statistical analysis tools.

2. Adopting wafer sort to multi-project wafers

The most obvious visible characteristic of the multi-project wafer (MPW) is that all devices for different projects are disposed within one small square area on the silicon wafer. The areas are then distributed over the wafer. Example of such different die images on a multi-project reticle is presented in figure1. There may be one or even more than ten identical devices on the same die image.

In general, fully automatic wafer probers are not adapted to the unique layout of multi-project wafers. There are actually two solutions to solve this problem. We may load and run one wafer as many times as there are identical parts to test

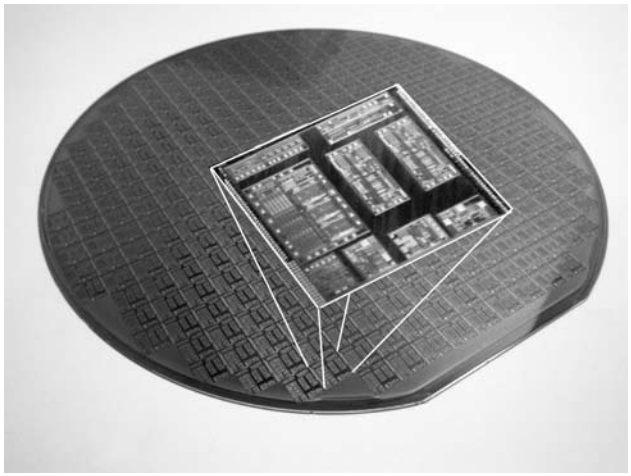

Fig. 1: Multi-Project wafer with emphasized die image.

on one die image. This is not an optimal solution, because it spends quite some time on wafer handling. Better solution is to write a special control software code for the wafer prober. Usually an ordinary personal computer with the suitable interface for wafer prober will do the job. Here we should take care about software compatibility. In case that the same computer is used to control wafer prober and our measurement acquisition system, it is always a good practice to check for the eventual driver and software library compatibility issues.

To teach the wafer prober to march upon the multi-project reticle, we need to adjust device X and Y dimensions to the dimensions of the die image in the multi-project reticle. After that we can use automatic wafer prober features like auto alignment, initial test square area recognition and automatic wafer map generation. Basically, all we need to do to test all devices on one die image is to use relative coordinate control commands of the wafer prober. This enables us to create required wafer prober chuck movements to all identical parts within the same die image that are relating to one project. When all parts on one die image are tested, relative coordinates for return back to the initial position on currently tested die image must be calculated. Than a simple "jump to next die" command can be used to continue with measurements on the next die image.

For marking bad or good parts on multi-project wafers inking is preferred to the wafer map. On the other hand, similar algorithms may also be used to convert original wafer map data from the wafer prober to the packaging company wafer map format.

3. How to select proper measurement equipment

The most crucial point in test program development is to select the right gear to do it. The selection is huge, but from the low cost point of view, it is a very good idea to use multifunction data acquisition cards (DAQ). They do have several limitations, but with proper design of the load board, most of them can be easily removed. As a matter of fact, load board can be connected directly on the DAQ card and everything together can be placed almost on the top of the probe card. This means very low signal degradation and improves signal measurement accuracy. Figure 2 represents such combination of DAQ card and load board that can be simply attached (with connectors) to DAQ card. Figure 3 shows assembled load board and DAQ card with very short wires to probe card on the wafer prober.

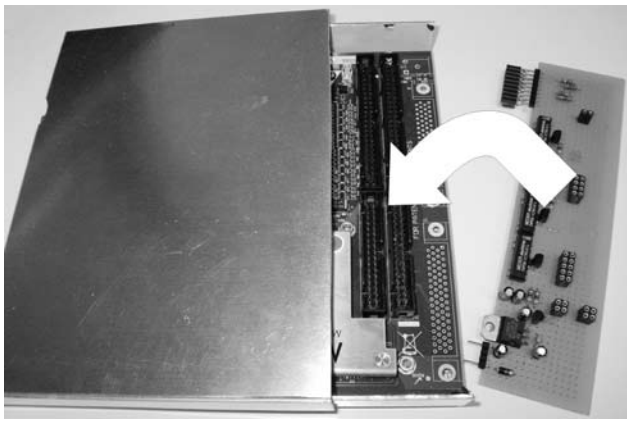

Fig. 2: DAQ card with load board.

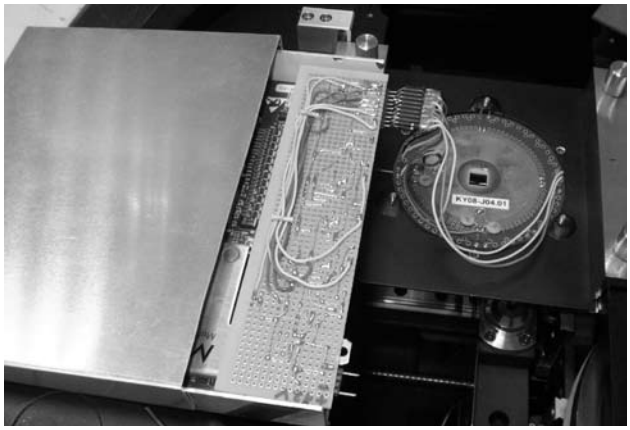

Fig. 3: Assembled DAQ card and load board connected to the probe card on wafer prober.

It is quite common to have a DAQ card with 32 or even more analog inputs (several of them may be also differential), 32 digital inputs/outputs, 4 analog outputs and two or three counters. So each pin of the ASIC that needs to be measured or triggered can be connected directly to its dedicated pin. If the number of pins is insufficient, we may simply add some extra cards to the USB (Universal Serial Bus) port. This method eliminates the need for expensive and time consuming switching matrix. It is well known that in general the switching matrix suffers from poor reliability when huge number of commutations is in question and they also degrade the signals due to longer switching paths.

To achieve high speed, control and flexibility of the DAQ cards we should go to the lowest possible level of program-

ming, which is usually limited by the driver and software library availability. Most of the DAQ cards still support writing subroutines in some kind of programming language like C or C++. A modern DAQ card actually enables us to utilize its own memory and processing power to run data acquisition independently from the control computer. Only trigger, sweep frequency setup and measured data must be transferred between the DAQ card and control computer. On the other hand, the latency may be the problem. Our tests show, that with such configuration the latency across the USB is approximately 20 miliseconds. Consecutive output set and measure time afterwards may be even faster than 1 micro second per repetition. In the case that we need a lot of configuration settings, the latency may be avoided by switching from windows platform to DOS or Windows 98 platform. There are still several DAQ cards available on the market, which are still supported in DOS mode. They also come in CardBus PC card shape and can be easily used with a laptop computer. In this case our test showed almost no latency and output set and measure time took approximately 5 micro seconds. In general, Linux is not widely supported by the DAQ card manufacturers, but the situation is improving.

This brief survey shows us, what kind of compromises must be made. Data acquisition may become even faster, if raw digital data are used for analog output configuration or voltage measurement wherever possible. In this case for unipolar operation the following formula should be used:

$$binaryValue = \frac{Voltage}{referenceVoltage} * \max\ BinaryValue \qquad (1)$$

Where max BinaryValue for 16 bit card is 65536 and referenceVoltage corresponds to the previously selected voltage range. On some cards with gain settings also gain should be considered. Therefore we have for unipolar operation:

$$binary\ Value = Voltage * \left(gain * \left(\frac{\max Binary\ Value}{reference\ Voltage} \right) \right) \qquad (2)$$

4. Generation of STDF file

After we have selected a suitable test platform and created a stable ASIC wafer sort test environment, we would like to do a fast measurement data evaluation. In the beginning of the test program development, acquired test results are usually nicely organized in plain ASCII data files. It is always possible to load such data files into various software tools and do some basic statistical analysis, plot charts and similar.

The problem arises with the growing amount of test data and tested wafers. Suddenly, such approach becomes quite time consuming and the lack of suitable, professional analysis tool is evident. There are several available on the market. In general, they will not accept our specific ASCII data file, but they will definitely accept STDF (Standard Test Data Format)/3/. STDF is a proprietary file format for semiconductor test information, originally developed by Teradyne, as a test result output of all of Teradyne UNIX operating system based testers. Teradyne derives no direct commercial benefit from propagating this standard. Now it is widely used throughout the semiconductor industry, since it is a commonly employed format. It is also produced by automatic test equipment platforms from all leading companies. STDF is a binary format, and specifications are available on the internet. It can be converted either to ASCII format known as ATDF (ASCII Test Data Format) or to a tab delimited test file. Working with STDF variable length binary field data format is not trivial, since it involves a detailed comprehension of over 100 pages long specification document.

Fortunately, conversion from STDF to ATDF does not lose any information and tools are available to do the conversion in both directions - from STDF to ATDF and vice versa. Such tool is called "STDFUtilTools" and it is also available on the internet as well as detailed ATDF specification /4/. ATDF is actually much easier to implement than STDF, so it shouldn't be a big problem for any test programmer using whichever programming language to do it. So we can conclude that STDF test data files may be produced from ATDF data files to conform to one single standard.

Anyway, ATDF specification is also quite extensive and it takes quite some time to determine the required sequence of the necessary record types. So let us give some additional information about sequence of the ATDF record types:

1. First record type should be "FAR" (File Attributes Record). It determines ATDF and STDF format versions and scaling flag.
2. "ATR" (Audit Trail Record) is second record type and it is used to record all operations essential to contents of the file.
3. "MIR" (Master Information Record) record is needed for all global information of the file.
4. "SDR" (Site Description Record) describes information about presence of test sites and test heads.
5. Then we may have several "PMR" (Pin Map Record) type records.
6. "PGR" (Pin Group Record) is used to associate a pin name with a group of pins.
7. "WIR" (Wafer Information Record) is used to mark the beginning of wafer test.
8. "PIR" (Part Information Record) acts as a marker to indicate where testing of a particular DUT (Device under Test) started. It is followed by "BPS" (Begin Program Section Record) type record. Then we can have several "PTR" (Parametric Type Record), "FTR" (Functional Type Record) and other similar record types to store measurement data. After all measurement data for one DUT is stored, we insert "EPS" (End Program Section Record) record type. The last record type is "PRR" (Part Result Record) that contains the results information relating to each part tested by the

test program. Point 8 is then repeated for all parts that were tested.

9. Then we have all necessary "TSR" (Test Synopsis Record) type records. They contain statistics for one parametric or functional test.
10. After "TSR" type record we may have several "HBR" (Hardware Bin Record) type records. They store a count of parts placed in a particular bin after testing. Here we may have "pass", "fail" or similar bins.
11. "PCR" (Part Count Record) type record includes part count totals for one or all test sites.
12. "WRR" (Wafer Results Record) type record includes results for each wafer tested by the test program.
13. "MRR" (Master Results Record) is the last type record in the ATDF file and is a logical extension of the "MIR" type record.

Above 13 points actually describe the ATDF file structure. Further details about all ATDF type records used here are shown in ATDF file specifications /4/. Figure 4 represents a small cut off from the beginning of the ATDF file. Unfortunately some lines are too long and they will not fit on one page to represent them completely.

```
FAR:A|4|2
ATR:14:13:43 23-Mar-2010|created with mx330textfile2ATDF_Ver_6.0
MIR:cxc231-1|mx330_117|mx330_117_S02010001|DAQ1|L-D630|10:30:00 8
SDR:1|0|0|TSK-APM90A|2|TIPS|1|MXldb12|1|Universal|0|0
PMR:1|2|GND|VSS|1|0
PMR:2|3|AICH1|L2|1|0
PMR:3|3|AICH0|L2|1|0
PMR:4|2|VDD|VDD|1|0
PMR:5|3|AICH5|L3|1|0
PMR:6|3|AICH7|REXT|1|0
PMR:7|3|AICH4|OUTA|1|0
PMR:8|4|AICH0|PROG|1|0
PMR:9|5|PC5|COIL|1|0
PGR:0||0
PGR:0||0
WIR:1|18:43:23 08-Nov-2009|0|1
PIR:1|0
BPS:mx_330_wafer_sort
PTR:10|1|0|0.0092|P||CUR|||A|0.0070|0.0110|%f|%f|%f|||3|3|3
PTR:11|1|0|0.8228|P||OUTA8M50|||V|0.5400|1.2700|%f|%f|%f|||3|3|3
PTR:12|1|0|0.3887|P||OUTA8P50|||V|0.1200|0.8000|%f|%f|%f|||3|3|3
PTR:13|1|0|0.4341|P||OUTA50DIF|||V|0.3000|0.6000|%f|%f|%f|||3|3|3
```

Fig. 4: Small cut off from ATDF file.

After ATDF file is generated we may use previously mentioned "STDFUtilTools" tool to create a valid STDF file. This file can be used for an automatic statistical analysis for entire population of tested devices. Usually one STDF file per silicon wafer is required, but we may also join results from several wafers into one STDF file.

5. Conclusions

In this article the most critical parts of the low cost and high precision fully automatic test system development for multi-project wafers evaluation is described. The most important features of such system are respectful test speed and accuracy to low cost ratio, easy adaptation to new ASIC versions and STDF test data compatibility. All aspects of this approach were practically implemented and tested on several wafers.

High precision magnetic micro system that was recently designed and developed in our laboratory was also successfully characterized with such system. Test demands were about 2300 accurate voltage measurements, 18 precise frequency measurements and selective trimming, setting or reading of 250 OTP (one-time programmable) fuses per part at two different temperatures. Unique serial number was also written via OTP fuses to each part. This enables later measurement comparison of packed parts and identification of wafer sort measurement data from the STDF file. Average test time per part was approximately 850 miliseconds and could be even faster, if no DUT settling delays were necessary. Wafer prober moving time is half a second per part, so wafer sort time was a little bit less than 1.5 second. For the time being about one quarter of a million parts were successfully tested.

6. References:

/1/ J. Trontelj-jr, Precise Analog Automatic Testing on Silicon wafer, Midem Proceedings, 2006.

/2/ J. Trontelj-jr, Development of a Dedicated Low Cost ASIC Test System for Fully Automatic Wafer Prober, Midem Proceedings, 2007.

/3/ Web site for STDF specifications< http://freestdf.git.sourceforge.net/git/gitweb.cgi?
p=freestdf/freestdf-DEAD;a=blob_plain;f=docs/stdf-spec.pdf>, accessed on 23/03/2010.

/4/ Web site for ATDF specifications < http://freestdf.git.sourceforge.net/git/gitweb.cgi?
p=freestdf/freestdf-DEAD;a=blob_plain;f=docs/atdf-spec.pdf>, accessed on 23/03/2010.

Dr. Janez Trontelj jr.

University of Ljubljana, Faculty of Electrical Engineering
Laboratory of Microelectronics
Tržaška 25, SI-1000 Ljubljana, Slovenia
Tel.: +386(0)14768471
e-mail: janez.trontelj-jr@fe.uni-lj.si

Prispelo: 25.03.2010 *Sprejeto: 03.03.2011*