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STUDY OF CORRELATION AMONG DIFFERENTIAL NONLINEARITY, NONLINEARITY AND NOISE OF THICK FILM RESISTORS

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Keywords: electrical thick film resistors, nonlinearities of electrical thick film resistors, noise of electrical thick film resistors, thick resistive films, electrical conductivity of thick resistive films, I-V characteristics, current-voltage characteristics, V-I characteristics, voltage-current characteristics, linear I-V characteristics, linear current-voltage characteristics, nonlinear I-V characteristics, nonlinear voltage-current characteristics, theory of nonlinearity, differential nonlinearity of current-voltage characteristics, noise index, second harmonics index, third harmonics index correlation, laser trimming

Abstract: Typical parameters which make assessment of reliability of thick film resistors possible are noise and nonlinearity of a current vs. voltage characteristic. Both the parameters are strongly influenced by mechanisms of conductivity of the film and by mechanisms of conductivity which appear inside a transient area between the resistive film and its conductive contact. A study of correlation among nonlinearity, differential nonlinearity and noise of the thick film resistors was carried out. It was investigated an influence of the form and trimming of the resistors on these parameters. It was found that the form of the resistors influences these parameters by the same way. Trimming of the resistors influences their noise substantially but its influence on the nonlinearity is very low.

Študij povezave med diferencialno nelinearnostjo, nelinearnostjo in šumom debeloplastnih uporov

Ključne besede: upori električni debeloplastni, nelinearnosti uporov električnih debeloplastnih, šum uporov električnih debeloplastnih, plasti uporovne debele, prevodnost električna plasti debelih uporovnih, I-U karakteristike tok-napetost, U-I karakteristike napetost-tok, I-U karakteristike tok-napetost linearne, I-U karakteristike tok-napetost nelinearne, teorija nelinearnosti, nelinearnost diferencialna I-U karakteristike tok-napetost, indeks šumni, indeks harmonskih drugih, korelacija indeksov harmonskih tretjih, doravnavanje lasersko

Povzetek: Tipična parametra, s pomočjo katerih lahko ovrednotimo zanesljivost debeloplastnih uporov sta šum in nelinearnost tokovno-napetostne karakteristike. Na oba parametra močno vplivata mehanizem prevajanja znotraj filma, kakor tudi mehanizem prevajanja na prehodnem področju med uporovnim filmom in njegovim prevodnim kontaktom.

Študirali smo povezavo med nelinearnostjo, diferencialno nelinearnostjo in šumom debeloplastnih uporov, kakor tudi vpliv oblike in laserskega doravnavanja na omenjene parametre. Ugotovili smo, da oblika uporov vpliva enako na vse tri parametre, med tem ko lasersko doravnavanje močno vpliva na šum in dosti manj na nelinearnost uporov.

1. INTRODUCTION

When an electrical current is fed through a component a voltage drop appears across it. If the amplitude of the current will be changed and the voltage drop will change in proportion to the change of the current the component is linear. If the relationship between the current and the voltage drop is of an another type the component is nonlinear. It is evident that the denotation „the linear component" is related to the component with a linear current vs. voltage characteristic (C-V characteristic) and vice versa.

There are two groups of electronic components used in electronics - the nonlinear components and the linear ones. However, the basic assumption about the linear component can be accomplished theoretically only. In practice a higher or lower difference between a straight line and the C-V characteristic of the linear component can be found. Therefore the better denomination for the linear component is „the nominally linear component". The level of nonlinearity of these components is substantially lower than the level of nonlinearity of the nonlinear components. The measurement of nonlinearity can be very useful for users as well as producers of electronic components because this parameter makes evaluation of production quality and assessment of reliability possible.

The typical linear electronic components are resistors, some types of capacitors, air cored inductors, electrical contacts and leads. The typical nonlinear components are diodes, transistors, iron-cored inductors etc. Nonlinearity of the nominally linear component is usually caused by defects inside its electrically functional part. The defects originate as a consequence of errors in a design of the component (e.g. when materials with substantially different coefficients of thermal expansivity are put together) or errors which were made during its fabrication (e.g. when cleanliness of environment is insufficient) /1/.

Thick film resistors are the components made of resistive paste applied on an insulating substrate by screen printing. That is to say that the material of the thick film is not the homogenous material because it consists of two components after firing: of a functional conductive component and of an insulating one. A better description of this structure is that one component has the low resistivity and the second one has the high resistivity /2/. Therefore different mechanisms of conductivity take part in the process of conducting of the current through the film. Some of these mechanisms are linear and some mechanisms are nonlinear. The combination of them influences the final shape of the C-V characteristic. When the linear mechanisms dominate (phonon-elec-

tron interaction, elastic tunneling) the characteristic is slightly nonlinear only, when the nonlinear mechanisms have a more significant influence nonlinearity of the component is higher.

Nonlinearity is usually investigated using a modulating technique. The component is powered by the sinusoidal current and the voltage drop of third harmonic component which arises across it is measured /3/. When the dependence between the fundamental voltage and the third harmonic voltage is a cubic one the relation would be said to be of the third degree. When this dependence is quadratic the component is qualified as the component with the second degree of nonlinearity. It is a limited number of electronic components only which have this type of nonlinearity, majority of the components have the third degree of nonlinearity.

Nonlinearity of the resistors is often correlated with their noise. Noise also reflects inhomogenity and defects inside the electrically functional part of the component but sources of 1/f noise probably differ from sources of nonlinearity. Nevertheless it was found a good correlation between the noise index and the nonlinearity index of thin metallic films. The results which were found for thick films are presented in this paper.

2. BASIC IDEAS ABOUT NONLINEARITY

A simplified explanation can be given concerning the basic physical mechanisms which give rise to noise. Majority of theories is centered around the modulation in conductivity which arises when current carriers pass into and out of the conduction bands.

Such the theories can not be accepted for description of nonlinearity as there is no reason why any such interchange of carriers should be dependent upon the magnitude of the applied voltage. The basic idea about a rise of nonlinearity is that it occurs due to the existence of surface states or junctions within the material. Such the idea is compatible with the structure of the thick film. However, a single junction has an asymmetrical C-V characteristic. The symmetrical characteristic can be found for the antiparallel connected junctions. This characteristic can also be synthesized by many other arrangements, e.g. by the parallel connection of the serial combinations of the opposite polarized junctions.

The basic theory of nonlinearity was given by J. C. Anderson and V. Ryšánek /4/ for the thin films but its conclusions can be generalized. This theory describes a relationship among inhomogenities and other defects inside the film, its resistivity and nonlinearity of its current vs. voltage characteristic. The basic assumption of the theory is given by the Matthiessen's rule

$$R_T = R_D + R \qquad (1)$$

where R_T is the total film resistance and R is a constant portion of it that arises from normal scattering processes. R_D represents nonlinear scattering processes due to barriers among the conductive areas which causes nonlinearity of the C-V characteristic.

If i-th boundary between two conductive cubic areas represents the potential barrier of V_i volts to conduction electrons then, under thermal equilibrium, the current I_i across the barrier in any direction will be given by equation (2) where A is a constant depending on the material of the film. It was derived that the net increase in the total current I_D across the N_t barriers can be described by equation (3) where V is the voltage applied across the barriers. It is assumed that all the barriers are of the same type.

Expanding of the sinh term in a series a dependence of the total current I_D on the harmonic components of the applied voltage can be found. The terms of the series are given by odd powers of the applied voltage only. Therefore the C-V characteristic is symmetrical and its nonlinearity can be evaluated according to the amplitude of third harmonic component.

$$I_i = A\exp\left(\frac{-eV_i}{kT}\right) \qquad (2)$$

$$I_D = 2N_t A\exp\left(\frac{-eV_i}{kT}\right)\sinh\left(\frac{eV}{kT}\right) \qquad (3)$$

$$I_D \approx \left(\frac{eV}{kT} + \frac{e^3V^3}{3!(kT)^3} + \ldots\right) \qquad (4)$$

Let us assume now that the insulating barrier between two conductive cubic areas is very thin and that the electron, when a voltage is applied between these areas, passes through this barrier by tunneling. There are two basic types of tunneling: elastic tunneling and inelastic one. Inelastic tunneling can be neglected as a mechanism of conductivity inside the resistive thick film because probability of an interaction of the electron with an energetic quantum inside the insulating barrier is very low here. Therefore elastic tunneling will dominate. The basic equation which describes the C-V characteristic of such the tunneling junction is as follows:

$$I_D = aV + bV^3 \qquad (5)$$

where a, b are constants. The second term of this equation is very low in comparison with the first one. Nevertheless it causes a slight cubical shape of the C-V characteristic.

It was shown that the overcoming of the potential barrier as well as the tunnelling through the barrier causes the slight cubical shape of the C-V characteristic. Other mechanisms also participate in the conductivity of the resistive thick films (Shottky emission, diffusion etc.) but it is possible to assume that the mechanisms mentioned above are very significant.

The conductivity of thick resistive films was also described by the use of the percolation theory, by the theory of insulating and conductive particles and by the theory of less and more conductive particles /7/, /8/. All these theories make a detailed analysis of nonlinearity possible.

3. MEASUREMENT OF NONLINEARITY AND DIFFERENTIAL NONLINEARITY

Let us assume that a component with the cubic shape of the C-V characteristic is powered by the sinusoidal current i. The periodical voltage v(t) across the component can be expressed by the Fourier series

$$v(t) = V_0 + \sum_{1}^{\infty} V_n \cos n\omega t \qquad (6)$$

where n = 1, 3, 5, ... The amplitude of third hamonic component V_3 is used for evaluation of nonlinearity of the C-V characteristic.

An arrangement for measurement of nonlinearity is very simple. The sinusoidal current applied to the component shall be provided by an oscillator having minimum distortion of the signal. The amplitude of the current is changed and the voltage of third harmonic component is measured by a selective voltmeter or by a lock-in amplifier.

Differential nonlinearity is measured by the use of modulating technique. The component under test is powered by the pure sinusoidal current of a constant low amplitude (the amplitude of the current is chosen to achieve the amplitude of the voltage drop across the component of 20-50 mV). This sinusoidal signal is added with the dc offset voltage. The dc voltage and its polarity is changed to investigate nonlinearity of the C-V characteristic in different working points in a whole range of the accepted voltage. The differential nonlinearity is investigated according to the level of the second harmonic component of the periodical voltage drop which is measured across the component during its powering by the sinusoidal current. When the characteristic is symmetrical the level of the measured harmonic component has to be the same for both the polarities of the bias voltage. The specimens are measured in a four-point arrangement.

4. EXPERIMENTAL

Samples were prepared on alumina substrates of paste HS 8031 (10^3 Ω/□). The topology of the specimens was chosen with respect to the request to have the samples of oblong form of the same resistance (that means with the same ratio of length/width) but with the different area. It makes evaluation of influence of sample area on noise, nonlinearity and differential nonlinearity possible. The measurements were carried out by the equipment Quantec (measurement of noise) and CLT 1 (measurement of nonlinearity). Differential nonlinearity was measured on a special nonlinearity meter designed and realized at the CTU in Prague, Department of Electrotechnology. The basic arrangement described above was completed by the Wien bridge to achieve higher quality of the sinusoidal current and by the Wheatstone bridge to avoid problems caused by a limited dynamic range of the lock-in amplifier.

The nonlinearity meter consists of the Wien bridge, the Wheatstone bridge, a lock-in amplifier (EG&G SR 830), a programmable DC supply (HP E3631A) and a sinusoidal oscillator with the very low distortion (G 212). The measured component is connected in one branch of the Wheatstone bridge and powered by the sinusoidal current. Current bonds of the component are separated from voltage bonds (four-point arrangement). The Wheatstone bridge is connected in a diagonal of the Wien bridge. The level of the second or third harmonics is measured in a diagonal of the Wheatstone bridge by the lock-in amplifier. All equipment except of the generator of the sinusoidal signal are controlled by the use of a GPIB interface and a SW product HP VEE and are carefully screened. Earth connections are made to avoid to earth loops. A schematic diagram of this equipment was published elsewhere /5/, /9/.

5. MEASURED RESULTS

Groups of 30 thick film resistors with different topology were measured with the aim to analyze influence of the shape and area of the resistors on noise, nonlinearity and differential nonlinearity. The typical characteristics of the noise index are shown in Fig. 1.

Nonlinearity of the same groups of the resistors was also investigated. The level of the measuring voltage U1 was carefully controlled to avoid to nonlinearity caused by increasing of the temperature of the resistors by measuring voltage. The maximum amplitude of U1 was calculated according to the value of the resistor and its estimated maximum load. The used voltage was substantially lower. The fact that the measuring voltage does not influence the temperature of the resistor during its measurement was verified by the measurement when the value of the voltage of the third harmonic component was measured for more than 20 sec. When this value did not change for the whole time of this measurement it was assumed that the measuring signal is sufficiently low and does not influence the temperature of the resistor under test.

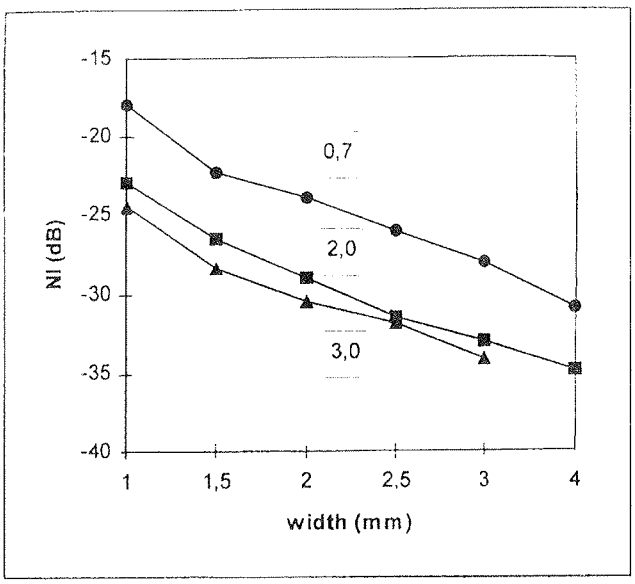

Fig. 1. Noise index of the resistors with the same ratio of length/width and with the different width. The characteristics for the ratio 0,7; 2,0 and 3,0 are shown.

The measurement of nonlinearity is more comfort than the measurement of noise and it is also less time consuming /6/. The price of the equipment for measurement of nonlinearity is comparable with the price of the equipment for measurement of noise.

The comparison of the results obtained by the measurement both the parameters could be interesting. Nonlinearity of the resistors expressed in THI is shown in Fig. 2

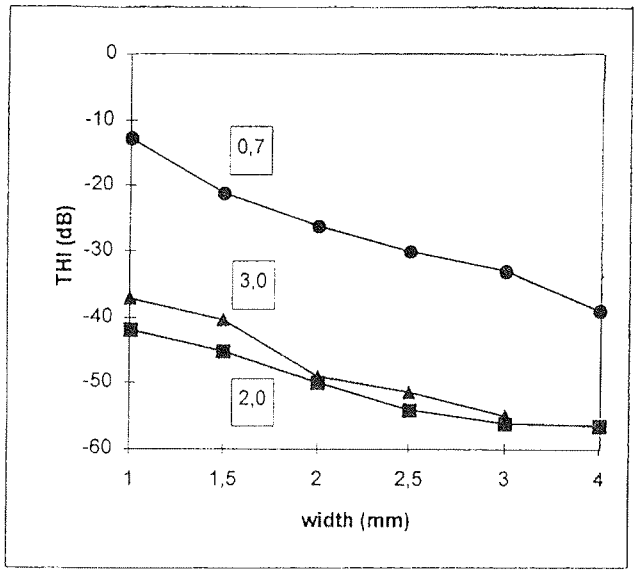

Fig. 2. Third harmonics index of the resistors with the same ratio of length/width and with the different width. The characteristics for the ratio 0,7; 2,0 and 3,0 are shown. The amplitude of the voltage U_1 was 5V.

Differential nonlinearity was investigated by the measurement of the second harmonic component of the periodical voltage generated by the sinusoidal current flowing through the resistor. The amplitude of the current was adjusted to achieve the voltage drop 50 mV across the resistor. This signal was added by the bias voltage 5 V. In contrast to the measurement of the THI the measured part of the C-V characteristic is nonsymmetrical. Even terms will dominate in the Fourier series for this type of nonlinearity. Therefore the second harmonic component was measured. We did not meet such the measurement in the literature. Therefore we defined for evaluation of this measurement a "Second harmonic index" (SHI) by the equation:

$$SHI = 20 \log \frac{U_2}{U_1^2} \qquad (7)$$

where U_2 is the amplitude of the second harmonic component in μV and U_1 is the voltage of the first harmonic component in mV. This definition corresponds to the definition of the "Third harmonic index" (THI) which is used for evaluation of the nonlinearity measurement when the third harmonic component is evaluated. In eq. (7) the second harmonic component U_2 is evaluated and instead the third power of U_1 used for calculation of THI the second power of U_1 is used here. The results of this measurement are shown in Fig. 3.

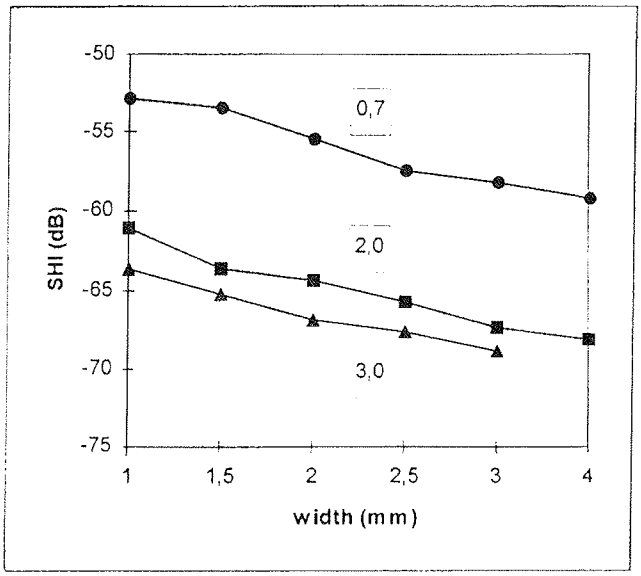

Fig. 3. Second harmonics index of the resistors with the same ratio of length/width and with the different width. The characteristics for the ratio 0,7; 2,0 and 3,0 are shown The amplitude of the modulating voltage U_1 was 50 m V. The bias voltage was 5V.

The influence of laser trimming of the resistors on values of NI and THI was also investigated. Trimming was carried out by a YAG laser, the resistance value increased by 50 % by trimming. NI and THI were compared before and after trimming. A typical example of their changes is presented in Fig. 4. It was found that

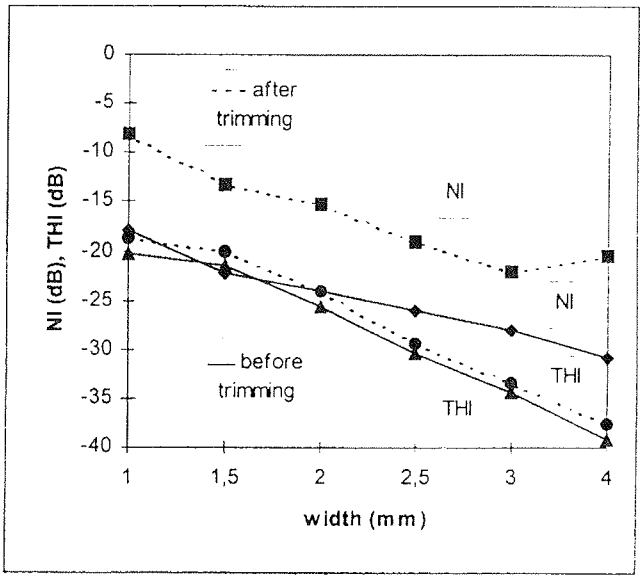

Fig. 4. Typical dependence of noise index NI and third harmonics index THI before and after trimming of the resistors. The resistance change after trimming was 50 %.

noise is substantially more influenced by trimming than nonlinearity of the resistors.

6. CONCLUSIONS

It was found that the noise index, the third harmonics index as well as the second harmonics index depend on the ratio of length/width of the resistors. All these parameters increase when the ratio length/width decreases. It could be caused by the higher influence of a transient area between the resistive thick film of the resistor and the conductive thick film of the contact. Therefore it is possible to recommend, from the point of view of investigated parameters, to prefer a higher ratio of length/width in the topology of the resistors when the resistors are an oblong form.

It was also found that the all investigated parameters of the resistors (NI, THI and SHI) reflect to the shape of the resistors with a comparable sensitivity. It makes the use of them with comparable efficiency possible.

Noise and nonlinearity differ in their sensitivity to laser trimming of the resistors. Noise increases after laser trimming, the changes of nonlinearity caused by laser trimming can be neglected. The matter of trimming is evaporation of the film from the area of an incidence of the laser beam. Borders of the laser beam track which were not evaporated were melted during trimming and therefore their structure, and probably distribution of conductive particles in the insulating matrix, differs in comparison with the structure of the film. This situation could contribute to the increase of the noise level of trimmed resistors. On the other hand nonlinearity could be also influenced by trimming from the same reason, but we found low changes of nonlinearity only.

The authors assume that the investigation of relations among NI, THI a SHI could contribute to deeper understanding of the mechanisms /7/ of thick resistive films conductivity.

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MEASURING THE WEIGHTED POWER OF CMOS LATCHING CIRCUITS

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Key words: microelectronics, IC, integrated circuits, integrated circuits design, weighted powers, power measuring, CMOS digital integrated circuits, latching circuits, CMOS latching circuits, low-power design, circuit optimization, performance evaluation, PDP, Power-Delay Product, EDP, Energy-Delay Product, flip-flop circuits, Hspice simulators, energy metrics

Abstract: We propose a method for power consumption evaluation of CMOS latching circuits, based on the weighting of individual energy-related parameters. By assigning appropriate weighting factors for clock and data inputs the circuit evaluation can be carried out in the context of overall system performance. The clock weighting factor is defined as the power ratio of a complete clocking system and the power needed to drive the clock inputs in the circuit. This factor is found to be ≈1.8 for a representative CMOS technology with optimally designed clock driver. We show how power parameters of a circuit can be measured and weighted in Hspice environment to evaluate the circuit power, PDP or EDP products. Finally we present comparative results for some well-known CMOS latching circuit types.

Merjenje porabe moči v pomnilnih strukturah CMOS

Ključne besede: mikroelektronika, IC vezja integrirana, IC snovanje vezij integriranih, moči utežene, merjenje moči, CMOS vezja integrirana digitalna, vezja držalna, CMOS vezja držalna, snovanje za moči male, optimiranje vezij, vrednotenje zmogljivosti, PDP produkt odloga moči, EDP produkt odloga energije, vezja prevesna, Hspice simulatorji, metrika energije

Povzetek: Predlagamo metodo za ocenjevanje porabe moči v pomnilnih strukturah CMOS na osnovi utežnostnih faktorjev za posamezne kategorije moči. Uporaba utežnostnih faktorjev omogoča ocenjevanje vezja v luči lastnosti celega sistema. Utežnostni faktor za vhod urinega signala definiramo kot razmerje med porabo moči celotnega podsistema za krmiljenje ure in med močjo, ki jo potrebujemo za krmiljenje vseh urinih vhodov. Za ta faktor ugotovimo, da se giblje okoli vrednosti ≈1.8 za tipično tehnologijo CMOS ob uporabi optimalno načrtovanega ojačevalnika signala ure. Prikazano tehniko za mejenje utežene povprečne porabe moči, faktorjev PDP in EDP ilustriramo s stavki iz simulatorja Hspice. Na koncu prilagamo izmerjene vrednosti za nekatere znane izvedbe pomnilnih celic CMOS.

1. Introduction

Memory cells determine to a large degree the speed and power characteristics of digital systems. They represent relatively large cells that are repeated many times, consume considerable power because of the clock activity and underlay the key architectural decisions of the system (clock distribution scheme, static/dynamic operation, pipelining, etc). In order to improve the speed and power consumption, a number of CMOS latching schemes have been analyzed and new design concepts have been proposed in recent years. However, it is frequently very difficult to compare the design efficiency of these solutions because we are faced with many parameters that are hard to match. The ultimate common cost function is therefore the energy that must be spent to complete the desired function within the limits of the design specification. Similar problems as with the circuit comparison are addressed also when we try to formulate the cost function for the circuit optimization. In fact the technique described in this work can be applied in both cases.

When authors compare new concepts with known circuit techniques they rely either on hand calculated data /5/,/10/ or on a number of simulation runs with different data statistics /12/,/13/. The details of power measuring technique are frequently not well documented so that it is hard to reproduce the results.

In the present work we try to provide a realistic measure of circuit performance based on power consumption that is weighted against the overall system performance. Different circuit techniques can be therefore compared with a single quantitative measurement.

The first section presents a short discussion of performance measurement based on power-delay and energy-delay products. We proceed with individual power consumption components of CMOS circuits and show how they can be monitored in the Hspice environment. Further attention is devoted to the power that is needed to drive the clock and data inputs of the latching cells. We calculate the clock weighting factor and show how the data activity can be used as the data weighting factor to reflect signal statistics on the cell performance evaluation. In the last section we show the implementation details and Hspice code fragments to calculate the weighted PDP, EDP or average circuit power. Experimental results are presented for some representative latching circuits.

2. The energy metrics

The most common quality measure for logic gates is the energy consumed by the circuit per switching event, usually called the Power-Delay Product (PDP).

$$PDP = E_{sw} = \int_0^T P(t)dt \qquad (1)$$

where T is the duration of the switching event. The switching event is normally defined as the low to high and high to low signal transition /1/,/6/. In an ideal CMOS gate without the second order effects this is equal to

$$PDP = C_L \cdot V_{dd}^2 \qquad (2)$$

The problem with PDP is that it ignores the actual speed of the circuit. For a circuit designer the name "power delay" can be misleading as the calculated value has no direct relation with the signal delay in the circuit; it is related to the duration of the switching event that sets the limits for the power integration interval. Faster circuits have larger PDP values because of higher currents involved in the switching process. PDP can be used as an adequate circuit quality measure only under the assumption that the duration of the switching event fits the design specifications and needs no modification. A typical example are ring oscillators that are usually used to measure the PDP and speed limits of a logic family.

To combine the circuit speed (or the "specification" speed), characterized by the signal delay T_{spec} with the power consumption it is better to use the Energy-Delay Product (EDP) as proposed in /4/:

$$EDP = \frac{\text{energy}}{\text{switching event}} \cdot \frac{\text{signal delay}}{\text{switching event}} = PDP \cdot T_{spec} \qquad (3)$$

The EDP definition implies that the quality of a circuit with PDP_a and T_{sa} is equal to the quality of another circuit with $PDP_b = PDP_a/k$ and $T_{sb} = k\,T_{sa}$. In general the speed/power tradings are not linear /11/ and allow various circuit techniques with different topologies to compete for the best solution of a design case.

As the power supply voltage is constant the switching energy can be calculated from the total charge flow on the power supply:

$$PDP = \int_0^T P(t)dt = V_{dd}\int_0^T I_{dd}(t)dt = V_{dd} \cdot Q_{sw} \qquad (4)$$

The procedure to measure Q_{sw} in Hspice simulation is presented in section 3. T_{spec} is measured with standard *.measure* statements for delays relevant to the circuit application.

The power consumption of a CMOS cell can be considered as the sum of 3 components:

- Internal power (node parasitics and DC currents)
- Power to drive the inputs
- Power to drive the loads

Of course it is possible to measure the sum of all power components from the power supply current I_{dd}, but this would eliminate the possibility to weight individual components. As we deal with the latching circuits it is of particular interest to weight separately the power consumed by the clock and data inputs. This can be realised by monitoring some internal circuit currents. In Hspice the easiest way to do this is to insert dummy voltage sources of 0 DC volts in the circuit branches, as presented on fig 1.

All loads associated with core CMOS logic cells are combinations of some capacitive parasitics to V_{dd} (C_p) and to Vss (C_n). Figure 2 shows currents associated with the switching event on such loads. As we see from table 1, the power to drive the load can be calculated either from the power supply current I_{dd} or from the measurement of the driver current I_d. The third possibility is to measure the input current to the load I_i. Because of opposite polarization the average value of this current is 0. However in Hspice it is also possible to measure the absolute current value which would in our case provide the double of the load power.

As the capacitive load power is reflected on the cell supply current, the measurement of the I_{pp} on fig. 1 provides the sum of internal cell power and the load

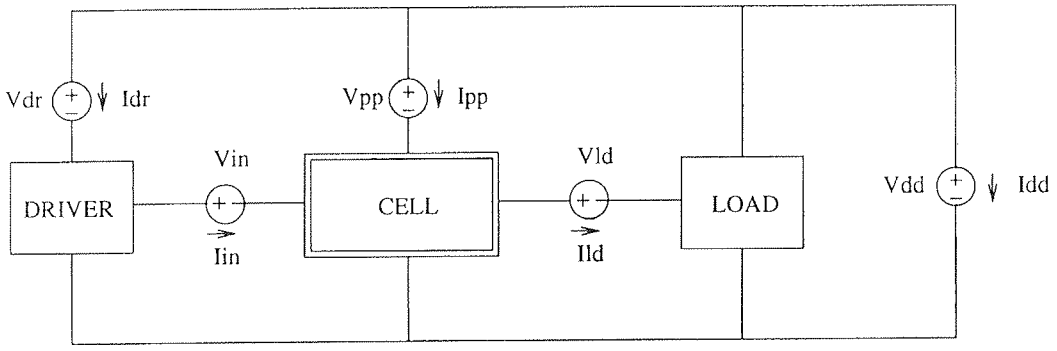

Fig. 1: Dummy voltage sources (Vdr,Vpp,Vin,Vld) to determine individual cell power components

Table 1: Power consumption on the CMOS load

Power monitor	$0 \rightarrow 1$	$1 \rightarrow 0$	$\sum$
$-I_{dd} \cdot V_{dd}$	$V_{dd}^2 \cdot C_n$	$V_{dd}^2 \cdot C_p$	$V_{dd}^2 \cdot (C_n + C_p)$
$I_d \cdot V_{dd}$	$V_{dd}^2 \cdot (C_n + C_p)$	0	$V_{dd}^2 \cdot (C_n + C_p)$
$I_i \cdot V_{dd}$	$V_{dd}^2 \cdot (C_n + C_p)$	$-V_{dd}^2 \cdot (C_n + C_p)$	0
$\lvert I_i \rvert \cdot V_{dd}$	$V_{dd}^2 \cdot (C_n + C_p)$	$V_{dd}^2 \cdot (C_n + C_p)$	$2 \cdot V_{dd}^2 \cdot (C_n + C_p)$

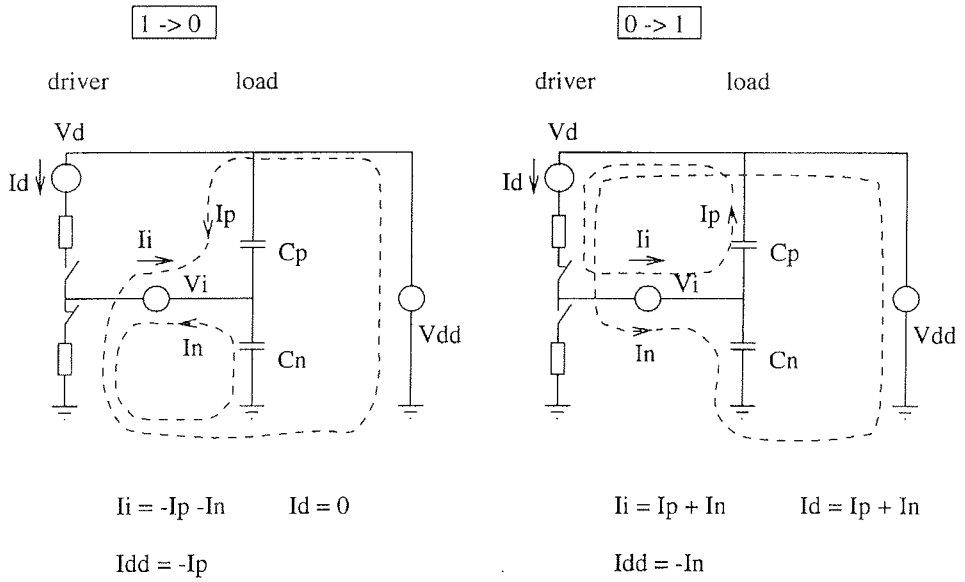

Fig. 2: Current flows on the capacitive CMOS load

power. The measurement of I_{Id} is therefore not needed. To calculate the last component, the cell input power, we have two possibilities. One is to build an ideal driving stage without parasitics that consumes no internal power and calculate the power from the supply current I_{dr} of that driver. The second possibility is to measure the absolute value of the input current I_{in} and divide the result by 2. This is more convenient as we don´t need extra device models and can use real circuit components to simulate the switching event.

3. Weighting the input power components

If we look at the circuit performance from the system level we must recognize that the price for various power components is not the same. To reflect the global system features such as the clock distribution scheme and signal statistics, the circuit evaluation function must be formulated with weighted input power components.

To drive clock inputs in synchronous systems we normally need special drivers and distribution networks. The system power penalty is therefore much higher than the sum of locally measured powers on clock inputs. To make an assessment of the real power requirement, consider the internal capacitance of an optimally designed N-stage buffer /6/ with tapering factor u and input capacitance C_i. The equivalent gate capacitance is

$$C_{gate} = C_i + u \cdot C_i + u^2 \cdot C_i + ... + u^{N-1} \cdot C_i = C_i \frac{u^N - 1}{u - 1} \quad (5)$$

We get a similar expression for internal diffusion capacitance if we assume that it is equal to δ times the buffer input gate capacitance:

$$C_{diff} = \delta \cdot C_{gate} \quad (6)$$

The optimal buffer drives the load $C_L = u^N \cdot C_i$ and dissipates the power

$$P_{driver} = \left(C_{gate} + C_{diff} + C_L\right) V_{dd}^2 \cdot f = \quad (7)$$

$$= \left((1+\delta) \frac{u^N - 1}{u - 1} + u^N \right) C_i \cdot V_{dd}^2 \cdot f$$

The measured input power in the cells would be that of the driver load C_L:

$$P_{cells} = C_L \cdot V_{dd}^2 \cdot f = u^N \cdot C_i \cdot V_{dd}^2 \cdot f \quad (8)$$

The ratio between the total power consumed by the driver and the measured power on clock inputs is defined as the clock weighting factor w_c:

$$w_c = \frac{P_{driver}}{P_{cells}} = 1 + \frac{\left(u^N - 1\right) \cdot (1+\delta)}{u^N \cdot (u-1)} \quad (9)$$

The number of stages N depends on the size of the clock network, while the optimum tapering factor u is known to be close to 3.6 for technologies with $\delta \approx 1$. For N values greater than 2 we can then assume $u^N - 1 \approx u^N$ so that the clock weighting factor can be approximated to

$$w_c \approx 1 + \frac{1+\delta}{u-1} \quad (10)$$

With $\delta=1$ and $u=3.6$ the calculated value is 1.77. It must be pointed out that this is still an optimistic value since we have neglected the wiring capacitance of the clock distribution network and have assumed an optimal driver.

Another important issue regarding the input power measurements is the signal activity alpha, defined as the number of complete signal transitions per clock cycle /13/. The clock itself has $\alpha = 1$ while other input signals may have various values depending on the nature of the system. If the signal comes from another latching cell the maximum value for alpha is 0.5, as data can change once per clock cycle at maximum. A random binary signal has $\alpha = 0.25$. The natural tendency of binary coded signals is that high-order bits have lower activity than low-order bits.

The signal activity depends also on the circuit structure: adder outputs for example may have activities much higher than 1 due to the carry propagation transients. If such signals are connected to the data inputs of flip-flops the toggle power can significantly influence the selection of the optimal latching circuit.

When we simulate the switching event of a latching circuit we apply one logic-high and one logic-low state to the data input for each clock cycle. The signal activity of the data input in the switching event is therefore equal to 0.5 (fig. 5). To compensate for the difference between the real application and the calculated input power in the switching event we define the data input weighting factor as

$$w_d = \frac{\alpha_{system}}{0.5} \qquad (11)$$

It is obvious that some statistical properties of system signals must be known to make better cell comparisons. If this is not the case, $w_d = 1$ can be used as worst case input power weight. Methods to determine alpha are described elsewhere /14/, /15/.

4. The power measurement technique

According to (4) the measurement of average power consumption of CMOS cells with constant power supply is reduced to the calculation of the equivalent charge flow across the power supply. Figure 3 shows the necessary setup to automate this procedure in the Hspice simulator /6/. We insert a new node qt, connected to the measuring capacitor C_q and the current-controlled current source F_p. The later is controlled by the cell supply current (measured on V_p), multiplied by the gain factor.

C_q and the gain must be set to scale the voltage V_{qt} on node qt in the range of reasonable values for the given circuit type, otherwise we will experience difficulties with the numeric precision of the simulator. A good choice is to use gain = 1 and C_q = 1fF, which scale V_{qt} to 1V for 1fC of charge flow. The voltage on node qt is then given by

$$V_{qt}(t) = \frac{1}{C_q}\int_0^t \text{gain}\cdot I_p(t)dt = \frac{\text{gain}}{C_q}Q_p(t) \qquad (12)$$

The total charge flow across V_p during the switching event with the duration Tfin is given by

$$Q_{sw} = \int_0^{T_{fin}} I_p(t)dt = Q_p(T_{fin}) = \frac{C_q}{\text{gain}}V_{qt}(T_{fin}) \qquad (13)$$

As we see, Q_{sw} can be measured as the voltage on node qt at the end of the switching event, multiplied by the scaling factor C_q/gain. One should not forget to set the initial condition on C_q to 0 volts. The whole procedure requires four Hspice statements:

```
Cq qt 0 1f
Fp 0 qt Vp 'gain'
.ic V(qt) 0
.measure tran Qsw max V(qt) from=0 to='Tfin'
```

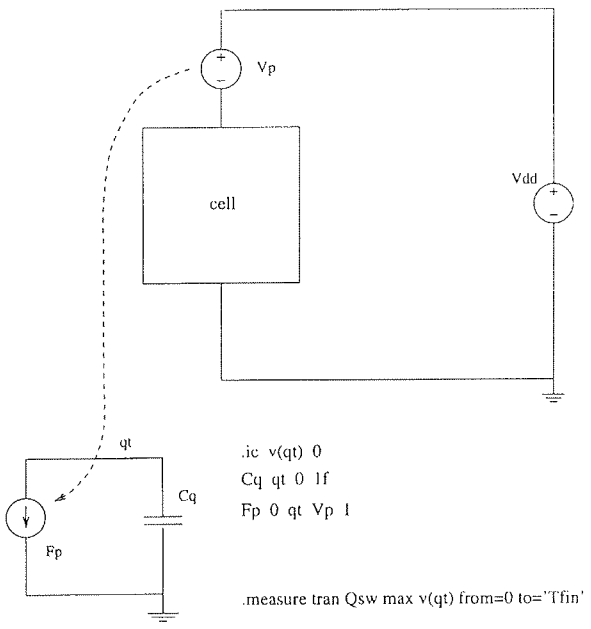

Fig. 3: Measuring the equivalent charge flow of a cell

Similar technique can be used to measure the charge flow into the cell inputs. In this case we use the absolute value of the controlling current and divide the result by 2. This is done inside the 'F' statement by the 'abs=1' modifier and the gain multiplied by 0.5. Referring to fig. 4, the charge flow for input CI would be modeled by

```
Fc 0 qt Vc 'gain*0.5*wc' abs=1
```

We can get the sum of all charge flows needed for the cell power calculation if we connect the relevant current-controlled current sources to the same node qt.

When weighting is required, the gain in the F statement is multiplied by the corresponding weighting factor. In this case the voltage $V_{qt}(T)$ represents the total weighted switching charge of the circuit. Once Q_{sw} is known, one can calculate the average power, PDP or EDP from (3) and (4). The appropriate 'measure' statements would be

.measure PWR param = 'Vdd*Qsw*Sq/Tfin'

.measure PDP param = 'Vdd*Qsw*Sq'

.measure EDP param = 'Vdd*Qsw*Sq*Tspec'

With gain=1 the scaling factor S_q is equal to C_q.Tfin is the duration of the simulated switching event. If EDP is needed, Tspec is measured within the same simulation as some combination of the delay times of interest.

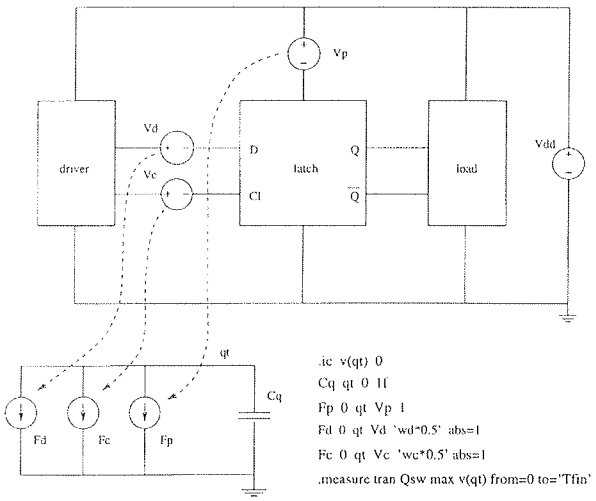

Fig. 4: Measuring the weighted charge flow of a CMOS latch

To characterize flip-flops and latches the switching experiment must assure both high → low and low → high transitions of the outputs which means that input signals must exhibit certain waveforms. We recommend the following rules for the switching experiment:

- The circuit must be loaded with realistic loads.
- The initial states of all nodes must be equal to the final states so that an even number of state transitions is involved.
- Inputs must be driven by realistic drivers. In spite of the fact that input currents are measured and contribute to the total power consumption the rise and fall times of ideal voltage sources do not change with loading. Measurement of circuit speed based on heavy loading of ideal input signals would give unrealistic EDP values because of the nonlinear speed-power trading in real drivers.

The power measuring setup for a CMOS latching cell is presented on fig. 4. Typical waveforms for signals, power supply current and the simulated switching charge are presented on figure 5.

Table 2 presents illustrative results for four different M/S static flip-flop structures: the switched inverter or C^2MOS type /6/ (fig. 6 a), the pass-transistor type /17/ (fig. 6 b), a variant of the RAM cell type /18/ (fig. 6 c) and the SSTC type /10/ (fig. 6 d). All circuits were simulated with minimum size transistors. To make meaningful evaluations some optimization should be done in the given system environment. This is especially true for the flip-flop types c and d.

Table 2: Simulation results for some minimum-size static flip-flops

	Conditions:
technology	0.6u, typical mean
w/l	0.8u/0.6u, all transistors
V_{dd}	3V
T	25 deg. C
C_l	8 fF
w_c	1.77
w_d	1

measured value	type A	type B	type C	type D
avg. power	12.46E-6 W	10.62E-6 W	15.48E-6 W	42.10E-6 W
PDP	1.12E-12 J	0.95E-12 J	1.39E-12 J	3.79E-12 J
EDP	1.40E-21 Js	0.93E-21 Js	1.85E-21 Js	3.50E-21 Js

5. Conclusion

The proposed evaluation technique for CMOS latching circuits is based on weighting the energy-related parameters.

Special attention has been paid to the power required to drive the clock and data inputs. We show how this power can be weighted to reflect the overall system performance on the circuit under investigation. Fragments of Hspice code illustrate the calculation of average power, PDP and EDP products. All these parameters are measured by the simulation of a simple switching event along with the delay times.

The technique can be used to simplify the optimization process and to improve the comparison of different latching schemes.

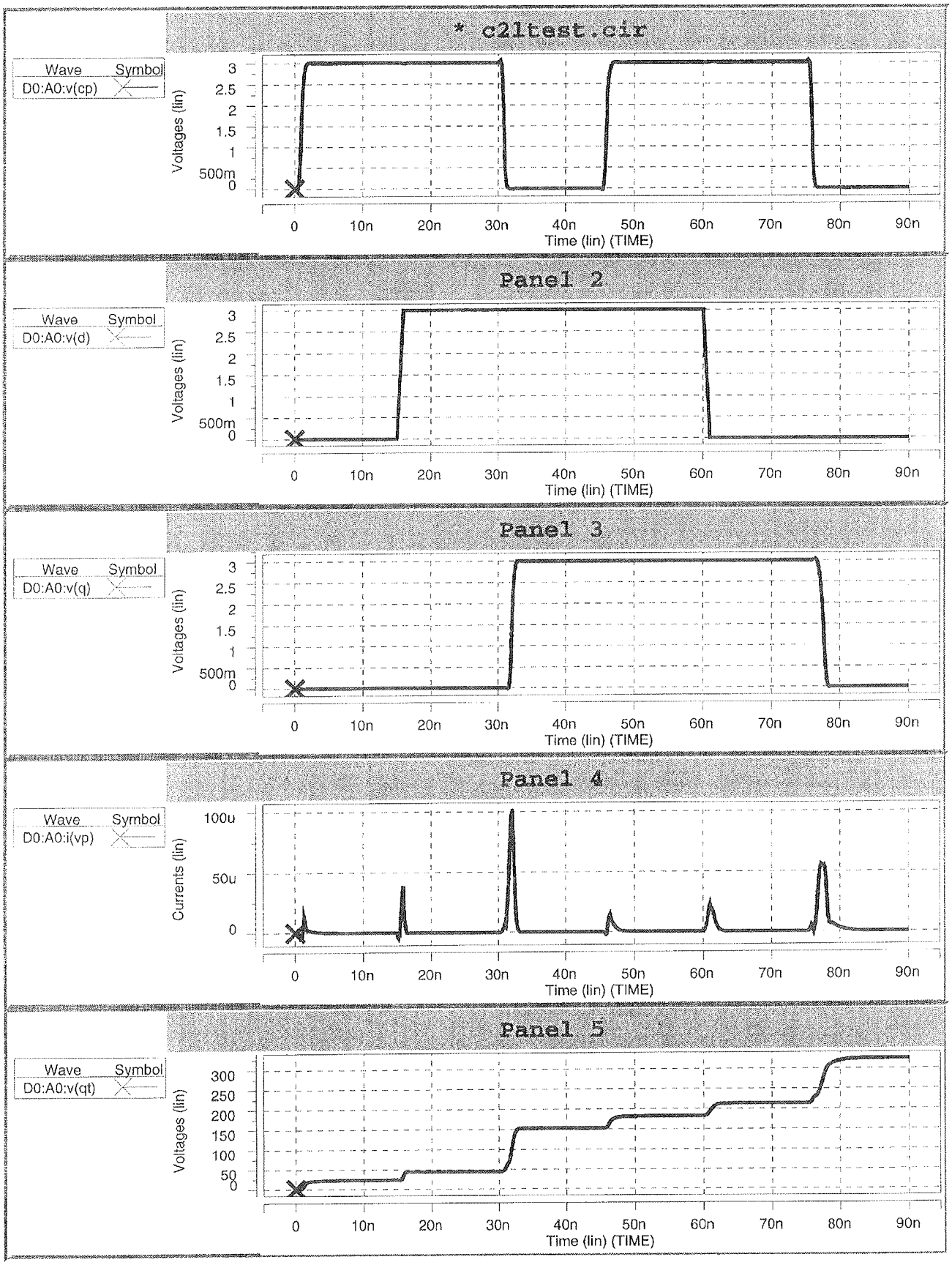

Fig. 5: Simulation of the weighted charge flow in a CMOS latch

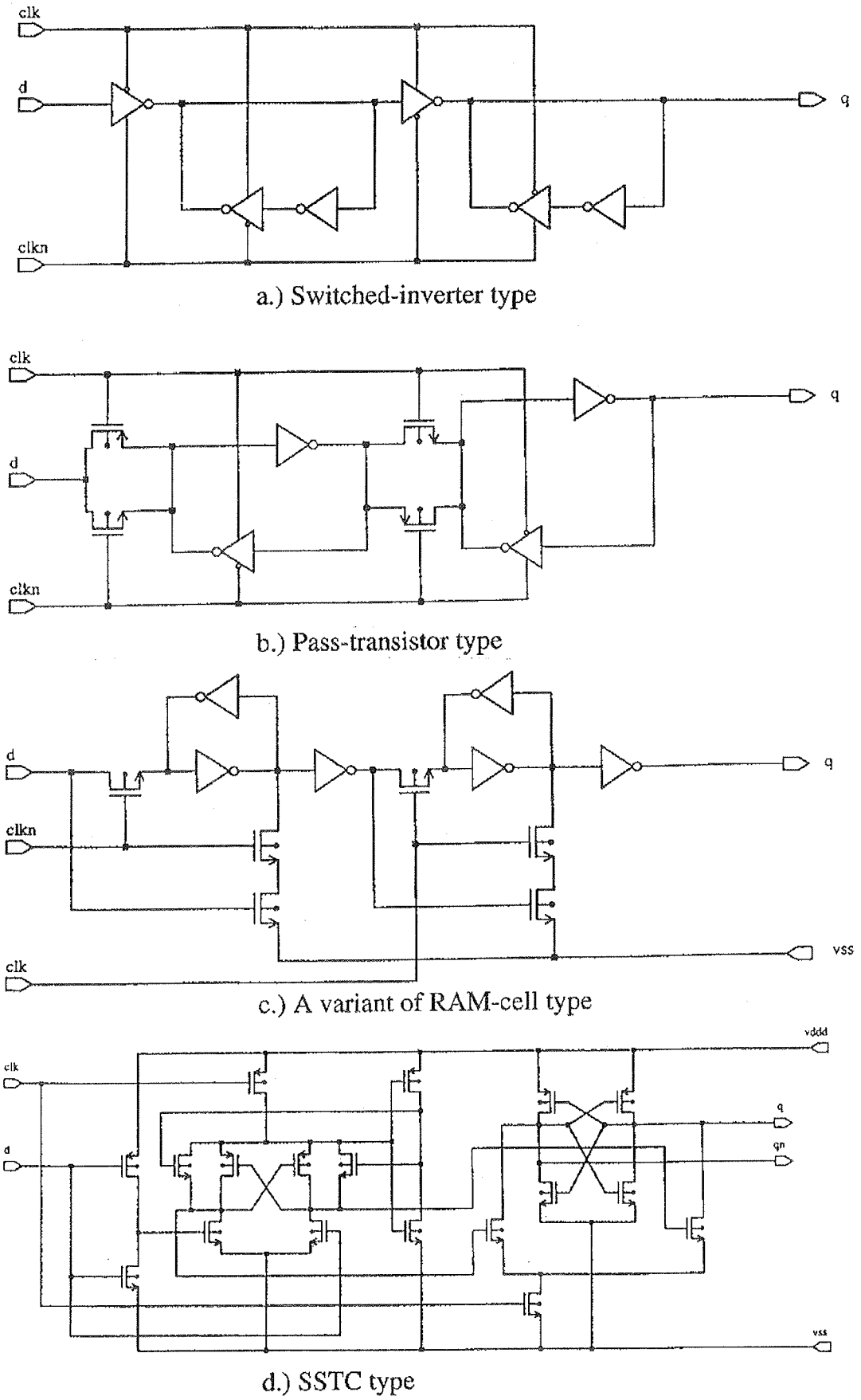

Fig. 6: Examples of CMOS static MS flip-flops

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AUDIO VMESNIK ZA RAČUNALNIK

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Ključne besede: računalništvo, vmesniki avdio, vmesniki avdio računalniški, mikroprocesorji, SCSI vmesniki sistemski inteligentni računalnikov, SCSI vodila, A-D pretvorniki analogno-digitalni, D-A pretvorniki, zajemanja podatkov, sheme blokovne

Povzetek: Področji računalništva in telekomunikacij se vse bolj povezujeta. Telekomunikacijsko omrežje je vse bolj "inteligentno" in omogoča vedno večje hitrosti prenosa informacij. Tako je omogočen prenos jezikovnih, slikovnih in podatkovnih informacij. Računalniki sami pa postajajo vse bolj "naprave za izmenjavo informacij". Na pohodu je večpredstavnost. Za potrebe študija večpredstavnosti in jezikovnih komunikacij je bil razvit audio vmesnik za delovno postajo. V pričujočem članku so predstavljene glavne značilnosti tega audio vmesnika.

Audio Interface for Workstation

Key words: computer science, audio interfaces, audio interfaces for computers, microprocessors, SCSI interfaces, Smart Computer System Interfaces, SCSI busses, A/D converters, analog-digital converters, D/A converters, digital/analog converters, data acquisition, block diagrams

Extended abstract: Telecommunications and computing are more and more tied together. Telecommunication network offers higher and higher bit rates and behaves more and more intelligent. It is possible to transmit speech, movies and data over this network. Computers are more and more machines for exchange of information. The era of multimedia is begun. For studying multimedia and speech communication we develop an audio interface for workstation. It can be used for acquisition, conversion and reproduction of speech information, as a measurement system, etc.

In the process of designing we had to decide which material is the most suitable for audio interface. The most important decision was the decision which microprocessor to use. After detailed analysis we chose a 32 bit processor MC68020. After that we choose type and quantity of Memory. For storing basic program we chose to use 256kB of EPROM memory and for storing data 1-3MB of fast (35ns) SRAM. Next vital components were A/D and D/A converters. Because we wanted to design the audio interface, which can offer acquisition and distribution of audio signal in CD quality, we chose AD676 for A/D and AD669 for D/A converter.

In the process of designing we divided the audio interface into some basic blocks:

- Microprocessor with bus interface and clock generation
- SCSI bus interface
- RAM
- EPROM
- Frequency generator
- A/D converter
- D/A converter
- Analog input interface
- Analog output interface and
- Power supply unit

Functionality of these blocks can be described through four basic phases:

- Power up sequence
- Communication with initiator trough SCSI bus
- Acquisition of analog signals and conversion into digital data
- Conversion from digital data into analog form and distribution of analog signal

After extensive testing, we realize that audio interface fulfill all our expectations. We use it very well in our research of speech recognition.

1. Uvod

Računalniška in telekomunikacijska tehnologija in tehnika sta doživeli izreden razvoj. Prvim 4 in 8 bitnim enoprocesorskim računalnikom so sledili 16 in 32 bitni računalniki z enim ali več mikroprocesorji, vse do 64 in 128 bitnih večopravilnih računalniških sistemov z velikimi procesnimi močmi.

Raziskovalci pa poizkušajo računalnikom še bolj povečati procesno moč in zmanjšati dimenzije, ter porabo energije.

Vzporedno z računalniki se hitro razvijajo tudi telekomunikacije. Namesto analognih visokofrekvenčnih sistemov s frekvenčnim multipleksom se vse bolj uporabljajo digitalni sistemi s časovnim multipleksom in skoraj neomejenimi prenosnimi zmogljivostmi. Viden je napredek tudi pri načrtovanju in uporabi prenosnih poti, saj kable z bakrenimi vodniki kot prenosne medije polagoma nadomeščajo kabli s steklenimi optičnimi vlakni. Vse to pogojuje uporabo novih linijskih sistemov in razvoj novih tehnologij ter storitev.

Obe področji se med seboj vedno bolj prepletata. Računalniki niso več samo naprave za računanje, ampak tudi naprave za izmenjavo informacij. Z večanjem prenosnih zmogljivosti računalniških omrežij se spreminjajo tudi informacije, ki se prenašajo med računalniki. Najprej so se prenašale samo tekstovne informacije, sedaj pa se prenašata tudi zvok in slika. Pri prenašanju in računalniški obdelavi teh informacij pa je potrebno te informacije pretvoriti v primerno obliko.

Zato potrebujemo dodatne vmesnike za zajemanje in pretvorbo podatkov v ustrezno obliko.

V pričujočem članku predstavljava značilnosti in osnovno zgradbo audio vmesnika, ki omogoča zajemanje in distribucijo audio signala v večpredstavnostnih sistemih.

2. Značilnosti audio vmesnika

Audio vmesnik omogoča zajemanje analognih signalov in pretvorbo v digitalne ter pretvorbo digitalnih signalov v analogne. Zaradi tega ga lahko uporabljamo za zajemanje, pretvorbo in reprodukcijo govornih informacij, kot merilni sistem, kot vmesnik za krmiljenje naprav z analognim signalom itn.

Vmesnik je načrtovan tako, da so uporabljeni elementi večinoma dostopni v prosti prodaji. Priključimo ga na vodilo SCSI. Zasnova audio vmesnika omogoča:

- 16 bitno A/D pretvorbo na dveh ločenih kanalih
- 16 bitno D/A pretvorbo na dveh ločenih kanalih
- izbiro vzorčevalne frekvence 8, 14.7, 16, 25, 29.4, 32, 44.1 in 48 kHz
- krmiljenje preko vodila SCSI - II (kabel A)
- dva dvokanalna audio vhoda:
  - mikrofon občutljivosti 3mV / 68 kΩ
  - kasetofon občutljivosti 300mV / 10kΩ
- dva dvokanalna audio izhoda:
  - zvočnik izhodnega nivoja 1VPP / 10 kΩ
  - kasetofon izhodnega nivoja 300mV / 10kΩ
- prenos podatkov po vodilu SCSI zlog za zlogom ali blok naenkrat
- programsko izbiro vhodov in izhodov
- nastavitev naslova audio vmesnika z mostički
- priključitev 1 - 3 MB pomnilnika RAM

Vmesnik je skupaj z napajalnikom vgrajen v ohišje dimenzij 500 x 250 x 90 mm.

2.1 Splošen opis delovanja

Audio vmesnik je relativno kompleksna naprava. Njegovo delovanje lahko najboljše ponazorimo z opisom po fazah:

2.1.1 Vklop

Ob vklopu audio vmesnika drži vezje za reset linijo RESET* na nivoju logične ničle okoli 0.5s. V tem času se stabilizirajo napajalne napetosti, pri A/D pretvorniku pa se izvede cikel interne kalibracije. Ko linija RESET* preide na logično enico, mikroprocesor naloži v kazalec sklada vrednost na naslovu $0, v programski števec pa vrednost na naslovu $4. Fizično sta ti vrednosti zapisani v pomnilniku EPROM. S tem začne mikroprocesor izvajati program. Najprej ugotovi koliko pomnilnika RAM je prisotnega in ga preveri. Nato prepiše program iz pomnilnika EPROM v pomnilnik in nadaljuje z izvajanjem programa v pomnilniku RAM.

2.1.2 Komunikacija preko vodila SCSI

Po zagonu mikroprocesor preverja kontrolne linije vodila SCSI vse dokler iniciator ne izbere audio vmesnika. Ko je audio vmesnik izbran, mikroprocesor zaseže vodilo SCSI, poskrbi za izmenjavo sporočil in prebere ukaze. Ukazi, ki jih lahko izvrši audio vmesnik so:

- prenos podatkov z audio vmesnika byte za bytom (A/D pretvorba)
- prenos podatkov z audio vmesnika blok za blokom (A/D pretvorba)
- prenos podatkov v audio vmesnik byte za bytom (D/A pretvorba)
- prenos podatkov v audio vmesnik blok za blokom (D/A pretvorba)

Mikroprocesor na audio vmesniku kontrolira podatkovni del in kontrolni del vodila SCSI.

Po fazi selekcije in prenosu sporočil ter ukazov se navadno začne faza prenosa podatkov preko vodila SCSI. Cikel prenosa podatkov preko vodila SCSI je za mikroprocesor audio vmesnika praktično enak kot pomnilniški cikel. Po prenosu vseh podatkov preko vodila SCSI, mikroprocesor pošlje sporočilo iniciatorju, da je delo končal, in sprosti vodilo. Mikroprocesor nato spet ciklično preverja kontrolne linije vodila SCSI.

2.1.3 Zajemanje podatkov in pretvorba v digitalno obliko

Po sprejemu ukaza za začetek zajemanja analognih podatkov mikroprocesor najprej vpiše ustrezne vrednosti v statusni register A/D in D/A pretvornika. Z biti D0 - D3 je določena frekvenca vzorčenja, z bitom D5 se izbere zajemanje podatkov z vhoda za mikrofon ali vhoda za kasetofon, bit D7 pa omogoči A/D pretvorbo.

Generator frekvenc začne v skladu z vrednostmi v D0 - D3 generirati pravokotni signal želene frekvence. Ta signal vodimo na A/D pretvornik. Ob postavljenem bitu D7 za začetek pretvorbe in signalu iz generatorja frekvenc se A/D pretvorba začne. Po končani pretvorbi A/D pretvornik postavi izhod BUSY* na nizek nivo. Ko je končana pretvorba na obeh kanalih, kontrolno vezje A/D pretvornika s postavitvijo linije IPL1* na nizek nivo prekine mikroprocesor. Le-ta izvede avtovektorizirani cikel potrditve prekinitve in izvede prekinitveno rutino. V njej mikroprocesor iz A/D sklopa prebere digitalno vrednost signala z audio vhoda in jo zapiše v pomnilnik ali prenese preko vodila SCSI do iniciatorja. Po končani prekinitveni rutini mikroprocesor nadaljuje z "opazovanjem" kontrolnih linij vodila SCSI.

Pri novem impulzu iz generatorja frekvenc se postopek ponovi.

Ko se prebere želeno število digitalnih vrednosti z A/D pretvornika, se postavi bit D7 v statusnem registru A/D in D/A pretvornika na 0, s čemer se A/D pretvorba konča.

2.1.4 Pretvorba digitalnih vrednosti v analogne

Mikroprocesor na začetku D/A pretvorbe v statusnem registru A/D in D/A pretvornika izbere frekvenco D/A pretvorbe (biti D0 - D3), izhod iz D/A pretvornika (bit D4 omogoča izbiro med izhodom na močnostni ojačevalnik ali kasetofon) in omogoči D/A pretvorbo (bit D6).

Signal iz generatorja frekvenc aktivira linijo IPL1* in s tem prekine mikroprocesor. Le-ta izvede avtovektorizi-

rani cikel potrditve prekinitve in izvede prekinitveno rutino. V njej najprej vpiše v A/D pretvornik digitalno vrednost, ki naj bi se pretvorila v analogno, nato pa omogoči D/A pretvorbo.

Po izvedeni prekinitveni rutini mikroprocesor "servisira" vodilo SCSI in čaka na novo prekinitev.

2.1.5 A/D in D/A pretvorba hkrati

Vezje audio vmesnika je zasnovano tako, da je mogoča "hkratna" pretvorba analognega signala v digitalni in digitalnega signala v analognega. V tem primeru je pomnilnik, rezerviran za podatke, razdeljen na del za vhodne in del za izhodne podatke. Iniciator preko vodila SCSI pošlje izhodne podatke v izhodni del pomnilnika, bere pa jih iz vhodnega dela pomnilnika.

Mikroprocesor na audio vmesniku v skladu z zahtevo iniciatorja v statusnem registru A/D in D/A pretvornika izbere frekvenco pretvorbe (biti D0 - D3), ki je enaka tako za A/D kot za D/A pretvorbo in s postavitvijo bitov D6 in D7 omogoči obe pretvorbi. Signal iz generatorja frekvenc začne A/D pretvorbo. Po izvedbi te pretvorbe vezje A/D pretvornika prekine mikroprocesor s postavitvijo linije IPL1* na nizek nivo. Mikroprocesor na enak način kot v točki 4.1.3 izvede avtovektorizirani cikel potrditve prekinitve in izvede prekinitveno rutino. V prekinitveni rutini prebere vrednost iz A/D pretvornika in jo shrani v vhodni del pomnilnika. Iz izhodnega dela pomnilnika nato prenese digitalno vrednost v D/A pretvornik in omogoči D/A pretvorbo.

Po končani prekinitveni rutini mikroprocesor nadaljuje s pošiljanjem podatkov po vodilu SCSI.

Ob prihodu vsakega impulza iz signalnega generatorja se postopek ponovi. A/D in D/A pretvorba se končata, ko mikroprocesor postavi bita D6 in D7 na nizek nivo.

3. Izbira elementov

Pri načrtovanju audio vmesnika je bilo potrebno izbrati elemente mikroračunalniškega sistema tako, da je delovanje vmesnika optimalno. Poglejmo, po katerem kriteriju so izbrane posamezne komponente.

3.1 Mikroprocesor

Mikroprocesor je srce audio vmesnika. Skrbeti mora za pravočasno A/D pretvorbo, pravočasno zajemanje podatkov z A/D pretvornika, pravočasno pisanje podatkov v D/A pretvornik in komunikacijo po vodilu SCSI.

Hitrost zajemanja podatkov z A/D pretvornika kot tudi hitrost pisanja podatkov v D/A pretvornik mora biti po specifikaciji najmanj 48 kS/s. Ker je pri audio vmesniku pretvorba 16 bitna, je potrebno vsakih 20.8 µs prenesti do D/A ali A/D pretvornika 4 zloge ali eno dolgo besedo.

Po odločitvi, da se v audio vmesniku uporabi Motorolin mikroprocesor, se je potrebno odločiti samo še glede tipa mikroprocesorja. Na razpolago so 16 bitni (MC68000) in 32 bitni mikroprocesorji (MC68020, MC68030). Da bi lahko v oba A/D ali D/A pretvornika hkrati vpisali ali prebrali informacijo, se je potrebno odločiti za 32 bitni mikroprocesor. V poštev prideta torej mikroprocesorja MC68020 in MC68030.

Mikroprocesor komunicira z drugimi napravami preko zunanjega vodila. Hitrost komunikacije se lahko meri v urinih ciklih. Oba 32 bitna mikroprocesorja potrebujeta za en cikel na vodilu 3 urine cikle. Za izvršitev enega ukaza branja ali pisanja v periferno napravo pri indirektnem naslavljanju pa je potrebnih najmanj 6 in največ 8 urinih ciklov, kar je odvisno od zadetka v interni cache pomnilnik mikroprocesorja oz. od internega načina izvajanja ukazov. V času A/D ali D/A pretvorbe naj bi bil mikroprocesor sposoben izvesti čim več ukazov, saj mora poleg kontrole pretvorbe komunicirati še preko vodila SCSI. Zaradi tega smo se odločili za uporabo mikroprocesorja MC68020, ki deluje z največjo frekvenco ure 25 MHz, medtem ko je ta pri MC68030 "le" 20 MHz. Izvršitev enega ukaza branja ali pisanja na zunanjo vodilo pri MC68020 traja lahko pri indirektnem naslavljanju največ 320 ns. V času ene pretvorbe lahko mikroprocesor izvrši 65 takih instrukcij. Ker pa ne gre samo za izvršitev instrukcij READ ali WRITE z indirektnim načinom naslavljanja, ampak tudi drugih, je število instrukcij med dvema pretvorbama še manjše. Izkaže se, da zadošča, če se lahko med dvema A/D in D/A pretvorbama izvrši najmanj 50 instrukcij. Torej MC68020 temu kriteriju "komaj" zadošča.

3.2 Pomnilnik

Pri izbiri pomnilnika se je bilo potrebno odločiti predvsem za tip, hitrost in kapaciteto. V mikroprocesorskem sistemu sta potrebna dva tipa pomnilnika: pomnilnik v katerem je spravljen program in ostane v njem tudi ob izklopu napajanja in pomnilnik namenjen shranjevanju podatkov med delovanjem. Pri pomnilnikih iz prve skupine je mogoče izbirati med pomnilniki ROM, EPROM, EEPROM, FLASH RAM... Pomnilnika iz druge skupine pa sta statični in dinamični pomnilnik RAM.

Zaradi relativne cenenosti in razširjenosti za pomnilnik, v katerem bo shranjena programska koda, izberemo pomnilnik tipa EPROM.

Dinamični pomnilniki tipa RAM so enostavnejši, imajo večje kapacitete, vendar potrebujejo osveževanje, kar pomeni dodatna vezja in v določenih pogojih tudi dodatne zakasnitve pri prenosu informacij. Statični pomnilniki so glede izdelave zahtevnejši, porabijo malce več energije, so hitrejši in ne potrebujejo dodatnih vezij za osveževanje. Predvsem zaradi hitrosti in enostavnejše izvedbe drugih vezij smo se odločili za uporabo statičnih vezij RAM.

3.2.1 Pomnilnik EPROM

Pri izbiri pomnilnika igra pomembno vlogo hitrost. Dostopni časi za pomnilnike tipa EPROM so relativno veliki. Gibljejo se od 120 ns do 300 ns. To je za naš primer preveč, saj mikroprocesor v najslabšem primeru zahteva dostopni čas 45 ns. Zato se v vezju audio vmesnika ob vklopu napajanja ves program iz pomnilnika EPROM prepiše v hitrejši pomnilnik RAM in se izvaja tam. Torej nam hitrost pomnilnika EPROM določa samo še čas, potreben od vklopa vmesnika do njegove pripravljenosti za delovanje, na samo delovanje pa nima vpliva.

Izbrali smo pomnilnik organizacije 64k x8 in oznako 27512. Zaradi 32 bitne širine podatkovnega vodila potrebujemo 4 integrirana vezja 27512. To nam da

velikost pomnilnika 256kB, kar zadošča za kontrolni program audio vmesnika.

3.2.2 Pomnilnik RAM

Najvažnejša lastnost, ki jo pri audio vmesniku zahtevamo od pomnilnika, je njegova hitrost. Če naj bi mikroprocesor deloval s polno hitrostjo, morajo imeti integrirana vezja pomnilnika RAM dostopni čas manjši od 45ns.

Za pomnilnik RAM smo izbrali pomnilniške čipe proizvajalca HITACHI z oznako 624256. Kapaciteta le-teh je 256kB x 4 z dostopnim časom 45 ali 35 ns, odvisno od verzije. Za izvedbo audio vmesnika potrebujemo hitrejšo verzijo. Zaradi zunanjega podatkovnega vodila širine 4 bitov in podatkovnega vodila mikroprocesorja širine 32 bitov je potrebno uporabiti 8 integriranih vezij. To pomeni 1 MB pomnilnika.

Pri delovanju audio vmesnika je pomembna tudi količina pomnilnika. V primeru, če bi se samo program izvajal v pomnilniku RAM, bi zadoščalo za delovanje do 512kB pomnilnika. Če pa pomnilnik RAM uporabljamo tudi kot vmesni pomnilnik za podatke, se potrebna količina pomnilnika poveča. Zato je na audio vmesniku predvideno, da količino lahko spreminjamo v odvisnosti od potreb. Predvidene so tri pomnilniške banke po 1MB. Za samo delovanje je potrebno vstaviti na ploščo audio vmesnika 1 pomnilniški modul - 1MB. Postopek prenosa podatkov preko vodila SCSI v načinu "zlog naenkrat", kjer je za vsak prenesen zlog potreben postopek ponovne izbire iniciatorja, največkrat ni izvedljiv (novi podatek iz A/D pretvornika je na razpolago vsakih 20.8 μs, ponovna izbira pa lahko traja tudi nekaj sekund), zato je potrebno prenos podatkov opravljati v blokih. 1MB pomnilnika se pri vzorčevalni frekvenci 48 kHz in dvokanalnem vzorčenju s 16 biti napolni v 5.4 s. Torej je potrebno najmanj vsake 5.4s izvesti preko vodila SCSI prenos bloka podatkov dolžine 1 MB. S povečevanjem pomnilnika RAM se ta interval lahko podaljša in znaša pri pomnilniku velikosti 3 MB okrog 15 s. Torej je priporočljivo napolniti s pomnilnikom vse tri pomnilniške banke.

3.3 A/D pretvornik

Od A/D pretvornika se zahteva 16 bitna A/D pretvorba s frekvenco vzorčenja najmanj 48kHz. Zaradi uporabe standardnega mikroprocesorja za krmiljenje A/D pretvornika in za manipulacijo s podatki mora imeti A/D pretvornik paralelno zunanje podatkovno vodilo.

Glede na zgornje zahteve je popolnoma ustrezal A/D pretvornik proizvajalca Analog devices z oznako AD676.

To je 16 bitni A/D pretvornik z največjo hitrostjo vzorčenja 100kS/s in s paralelnim izhodom. Vhodno območje pretvorbe je enako $\pm V_{REF}$.

3.4 D/A pretvornik

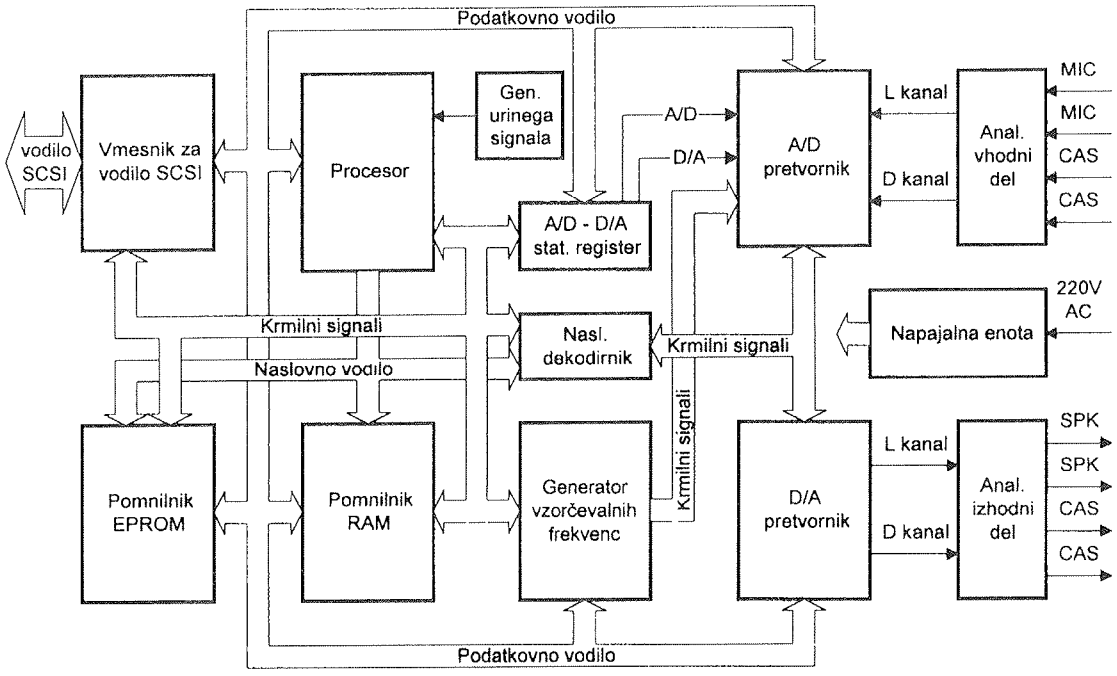
Od D/A pretvornika je pričakovati, da 16 bitno besedo pretvori v analogno vrednost. Hitrost D/A pretvorbe mora biti najmanj 48kS/s. Zaradi priključitve na vmesnik mikroprocesorja je zahtevano paralelno podatkovno vodilo.

V skladu s temi zahtevami smo izbrali D/A pretvornik z oznako AD669, proizvajalca Analog devices.

To je 16 bitni D/A pretvornik s paralelnim vhodom. Največji čas D/A pretvorbe je 13 μs, izhodno analogno območje pa do ±10V.

3.5 Vhodni in izhodni multiplekser

Na vhod audio vmesnika lahko priključimo mikrofon in kasetofon. Med tema dvema izbiramo s postavitvijo ustreznega bita v statusnem registru A/D - D/A pretvornika. Postavitev tega bita pomeni preklop vhodnega multipleksorja v želeni položaj.



Slika 1. Blokovni diagram audio vmesnika

Pri izbiri vhodnega multipleksorja sta v splošnem pomembna predvsem dva parametra:

- hitrost preklopa in
- električne stikalne karakteristike (R_{ON}, R_{OF})

Z uporabo dveh A/D in D/A pretvornikov smo se izognili kritičnim hitrostim preklopa in smo za vhodne in izhodne multipleksorje lahko zaradi idealnih stikalnih karakteristik izbrali stikala, izvedena z miniaturnimi releji. Le-ti so preko ustreznih tranzistorjev krmiljeni s postavitvijo ustreznega bita v statusnem registru A/D - D/A pretvornika.

4. Blokovna shema audio vmesnika

Sam audio vmesnik smo pri načrtovanju razdelili na več enot:

- mikroprocesor z gonilniki za vodilo in generatorjem urinega signala
- naslovni dekodirnik
- vmesnik za vodilo SCSI
- pomnilnik RAM
- pomnilnik EPROM
- generator vzorčevalnih frekvenc
- A/D pretvornik
- D/A pretvornik
- analogni vhodni del
- analogni izhodni del
- napajalno enoto

Povezavo enot prikazuje blokovna shema na sliki 1.

Naloge zgoraj naštetih enot so naslednje:

- Mikroprocesor izvaja program, zapisan v pomnilniku. S tem koordinira delovanje vseh enot in izvršuje naloge, ki jih preko vodila SCSI zahteva iniciator.
- Naslovni dekodirnik razvrsti enote audio vmesnika v naslovni prostor mikroprocesorja in poskrbi za pravilne časovne poteke krmilnih signalov na vodilu audio vmesnika.
- Vmesnik za vodilo SCSI pretvarja signale na vodilu SCSI v interne signale audio vmesnika (mikroprocesor) in obratno.
- V pomnilniku RAM se izvaja program in v njem shranjujejo rezultati A/D pretvorbe kot tudi podatki za D/A pretvorbo.
- V pomnilniku EPROM je shranjen program audio vmesnika.
- Generator vzorčevalnih frekvenc generira vse potrebne frekvence za A/D in D/A pretvorbo.
- A/D pretvornik je s svojimi dodatnimi vezji namenjen za vzorčenje, kvantiziranje in kodiranje analognega signala na izhodu analogne vhodne enote v digitalno obliko.
- D/A pretvornik pretvarja digitalne vrednosti v analogne in jih posreduje analogni izhodni enoti.
- Analogna vhodna enota amplitudno in impedančno prilagodi signal na vhodu audio vmesnika na vhod A/D pretvornika. Vrši tudi izbiro med signalom iz mikrofona in kasetofona.
- Analogna izhodna enota omogoča izbiro močnostnega ojačevalnika ali kasetofona na izhodu in prilagodi signal z izhoda D/A pretvornika na vhoda močnostnega ojačevalnika ali kasetofona.
- Napajalna enota zagotavlja vse potrebne napetosti za delovanje audio vmesnika.

5. Sklep

Opisani audio vmesnik smo izdelali v laboratoriju za telekomunikacije. Po začetnem testiranju in odpravi otroških bolezni v programski kodi se je pokazal kot zelo dobro orodje pri zajemanju audio signalov in ga uporabljamo tako v raziskovalne namene kot v pedagoškem procesu. V prihodnosti bi mogoče bilo potrebno razmisliti o nadgradnji vmesnika še z DSP procesorjem.

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A 500 DPI FINGERPRINT SENSOR IC IN CMOS TECHNOLOGY

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Keywords: biometrics, fingerprints, monolithic silicon sensor systems, CMOS, Complementary Metal Oxide Semiconductors, passwords, PIN codes, Personal Identification Number codes, security systems, identification systems, identification devices, authorization, pattern recognition, chip cards

Abstract: A monolithic fingerprint sensor has been implemented in a CMOS technology. This new sensor has a spatial resolution of 50 μm and translates the fingerprint pattern into a gray scale image of 256 x 256 pixels with 8 bit resolution. The sensor chip measures about 160 mm^2, together with a pattern recognition software, which extracts characteristic features, it forms a low cost system, which is well suited for a variety of applications as e.g. access control for buildings, computer networks and many other services.

CMOS integrirano vezje za senzor prstnih odtisov z ločljivostjo 500 dpi

Ključne besede: biometrika, odtisi prstni, sistemi senzorjev silicijevih monolitnih, CMOS polprevodniki kovinskooksidni komplementarni, gesla, PIN kode številčne identifikacijske osebne, sistemi varnostni, sistemi identifikacijski, naprave identifikacijske, odobritev, razpoznavanje vzorcev, chip kartice

Povzetek: Izdelali smo senzor prstnih odtisov v CMOS tehnologiji. Njegova prostorska ločljivost je 50 μm pri prevajanju oblike prstnega odtisa v sivo sliko velikosti 256x256 pik z 8 bitno ločljivostjo. Površina senzorskega vezja je 160 mm^2. Skupaj s programsko opremo za prepoznavanje oblik sestavlja sistem, katerega nizka cena omogoča različne uporabe, kot so nadzor vstopa v objekte, računalniške mreže in podobno.

1. Introduction

For a long time keys, made from metal in a more or less sophisticated way, have been a well accepted measure to protect property and the private sphere of people and organizations. But these keys can be stolen or lost, copying of the keys may reduce the security or privacy level to zero. Besides those well known key systems, which are based on the possession of a key also knowledge based systems are used. These systems substitute the physical keys by agreements of secret codes. Many of today's systems as e.g. mobile phones, credit cards, computers require special passwords or PIN-codes (personal identification number). The access to sensible areas of corporations and government agencies has to be restricted, but also electronic banking and electronic commerce in general need a proper identification and authorization, so that only the legitimate user may initiate transactions. If passwords and/or PIN codes are forgotten, the respective service is no longer available.

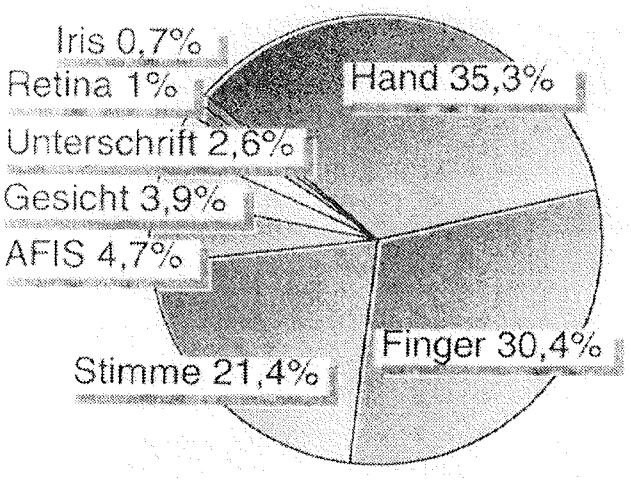

Fig.1: The global biometrics market, share of different systems

For the identification of the legitimate users biometric methods are best suited, which are based on constant features of the user's human body. Examples are the human speech, some characteristics of the face, the signature, structures of the human eye (pattern of the retina and iris) and many more. According to (Fig.1, /1/) most applications use pattern of the hand and fingers (65,7%) followed by voice recognition systems (21,4%). All other systems only have a small share of the overall biometrics market, either because of a high complexity of the systems needed, or because of the somehow invasive character of the measurement (e.g. illumination of the eye needed for the evaluation of the retina patterns). Simple, reliable and cheap systems are needed for the emerging security market for applications in PCs, telecommunication systems and electronic commerce applications.

2. The fingerprint as a unique characteristic of human beings

A typical fingerprint, covering an area of ca. 100 mm^2, shows about 12 characteristic positions, the so called minutia (Fig. 2). These minutia can be used as unique features for the identification of people. If compared to other methods, the fingerprint recognition systems offer several advantages:

- Since about 150 years the criminal science has carried out exhaustive theoretical and practical investigations on the use of fingerprints
- An almost infinite number of variations ($>>10^{22}$) enable the reliable and unique identification of all living people and even future generations
- The characteristics of the fingerprint do not change over the lifetime of a human being, even after most injuries the skin recovers in exactly the same pattern.
- The use of fingerprint identification systems is easy and pleasant, compared e.g. to systems based on the retina patterns and needing illumination and camera systems.

Fig. 2: Fingerprint record, features marked

The fingerprint recognition system described in this paper is based on the well established knowledge about the characteristics of fingerprints. The monolithic silicon sensor delivers a grayscale image and contains the significant characteristics (minutia) for each fingerprint, as e.g. ending lines, branching lines and characteristic turns and eddies. The features and characteristics and their relative position to each other are stored in a feature list. Such the overall memory needed can be reduced from 64 Kbytes for the whole gray scale image to a few hundreds of bytes for the still unique feature list. Due to this reduction, the whole system including a limited archive of legitimate users eventually will be implemented on a chip card.

If the system has to learn the features of a new person (enrollment procedure) several fingerprints have to be recorded and their respective features be stored in the feature list. Usually several fingers are stored at a time for each person, so that in case of an injury the access to the system is still possible. The available system can act in two different ways, depending on the planned application:

- Authentication: The person enters his/her ID, afterwards the system verifies the identity and rejects the access in the case of a mismatch.
- Identification: The system identifies the person based on the fingerprint presented and rejects all not previously stored persons.

Up to now the recording and the evaluation of finger prints was a costly procedure using very sophisticated equipment. With the availability of the monolithic „Fingertip-Sensor-System" it is now possible to record fingerprints very easily and to evaluate and identify the respective persons in a very short time. The whole process takes only a few seconds. Only if the extracted features correspond to the previously stored ones the protected device, system or transaction is released for the desired operation.

3. The Fingertip Sensor Chip - Hardware

A prototype of the sensor chip, fabricated in a 0,8 μm CMOS technology with 2 layers of metalization has been produced and evaluated; first product samples are shipped to the customers now. This is an important basis for a low cost mass production of fingerprint based identification and authorization systems. The sensor area consists of an array of 256 by 256 sensor electrodes with a grid of 50 μm and such cover an area of about 160 mm^2 with a spatial resolution of 500 dpi (dots per inch). The sensor electrodes are covered with a special dielectric layer, which protects the surface of the chip from the direct contact with the outside world. The finger has to touch the chip surface and depending on the local structure of ridges and valleys different capacitance values in the range of a few femtofarads (10^{-12} F) can be read out from the individual electrodes in the array. Such the information on the whole structure of the finger print is available as 65.536 coded capacitance values. A schematic cross section through the sensor array with a finger in contact can be seen in fig. 3, the block diagram of the whole sensor chip in fig.4. Besides the sensor array, the chip contains a direct analog-to-digital conversion of the capacitance values, a control unit based on a 1 MHz clock generator and an interface for the transmission of the gray scale image, which is coded as 8 bit/pixel.

For the prototypes a parallel interface for an easy connection to a PC has been chosen, later on standard interfaces for different microcontrollers or customized versions will be available. Fig. 5 shows a view of finished wafer of sensor chips with a finger applied.

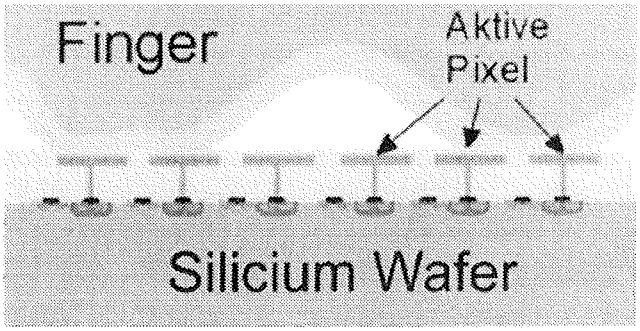

Fig. 3: Schematic cross section of sensor

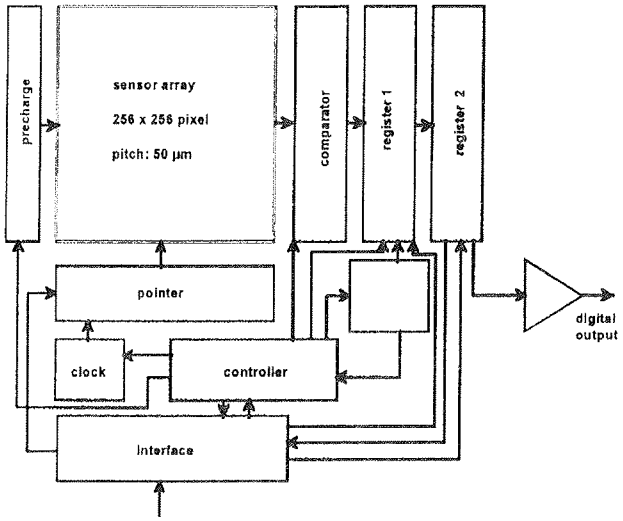

Fig. 4: Block diagram of the integrated finger print sensor.

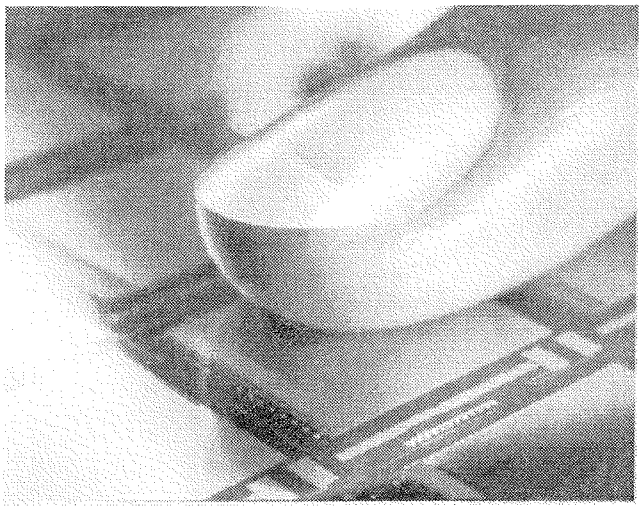

Fig. 5: Microphotograph of silicon sensor wafer with a finger applied

4. The Software for the Pattern Recognition Process

Since 1992 the PSE group in Graz is working on algorithms for the detection and identification of fingerprints. For this task conventional techniques of pattern recognition have been applied, in recent time new techniques as e.g. neural networks have been successfully applied. The software for this project has been developed within two years by a 5 person team. The processing chain (fig. 6) starts with the preprocessing of the sensor data and the transformation of these data into a normalized image. Then the identification of line structures, the completion of these lines and the extraction of the pure line structures is carried out. Then the characteristic features are extracted and classified using a neural

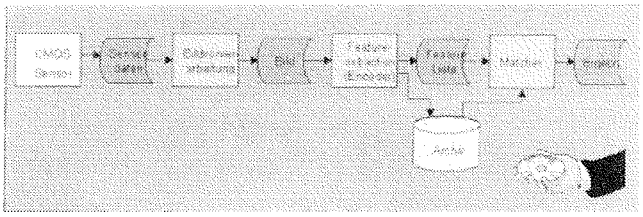

Fig. 6: Structure of software

network, the archive then stores only the result of these processes. When searching for a match later on, only the characteristic features are used. The compare algorithm is able to compensate for eventual translatorial or rotational changes in the pattern.

The recording and identification process for finger prints was a very complex procedure and requeired expensive instruments up to now. The new system can be used for a much broader range of applications, even in the low cost market segments. Almost every man - machine interface may use a fingerprint recognition system for increased security. The access to various types of computers, chipcards, immobilizer systems for vehicles, access control for buildings.

At the CeBit exhibition 1998 application examples have been demonstrated: a chip card incorporating a sensor, a prototype of a mobile phone and a PC keyboard (fig. 7, 8).

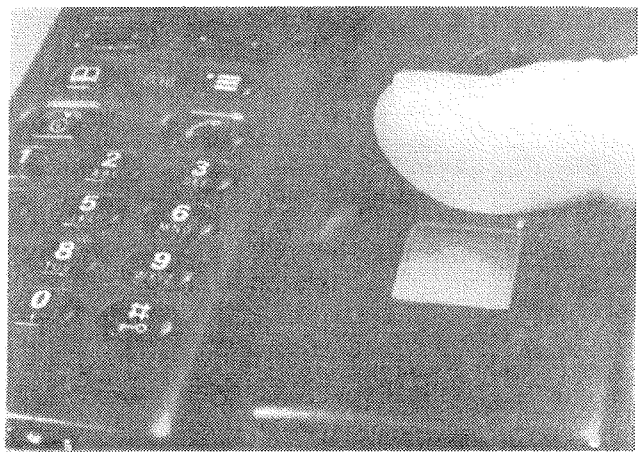

Fig. 7: Prototype of a GSM mobile phone with fingerprint authorization.

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/2/ S.Jung, R.Thewes, T.Scheiter: CMOS Fingerprint Sensor with Automatic Local Contrast Adjustment and Pixel-Parallel Encoding Logic, submitted to the ISSCC'99, San Francisco, 2/99.

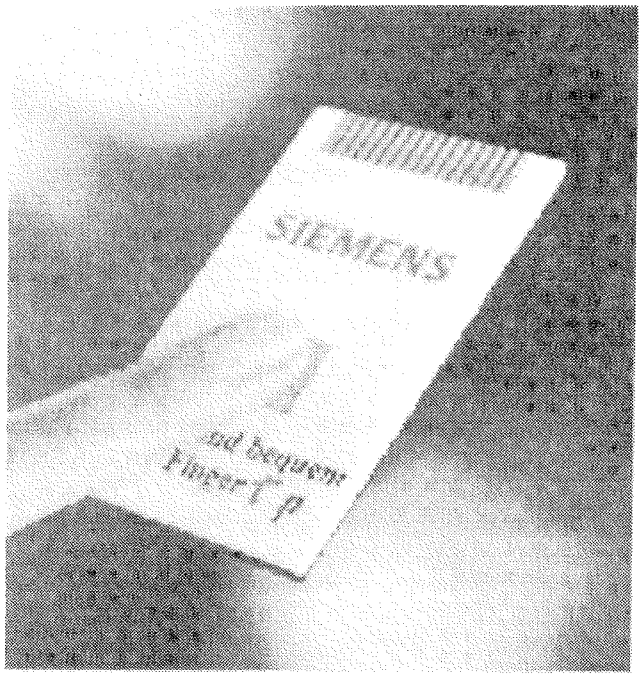

Fig. 8: Sample of a chip card with integrated fingerprint sensor

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INTERACTION OF HYDROGEN PLASMA WITH CORRODED SILVER SURFACE

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Key words: materials for electrical contacts, cleaning of contacts, surface cleaning, cleaning of contact surfaces, cleaning of metals, plasma cleaning, discharge cleaning, electrical discharges, H-plasma, hydrogen plasma, archeological artifacts, H-plasma interaction with surface, corroded surfaces, material corrosion, surface corrosion

Abstract: Experimental investigation on discharge cleaning of corroded silver surface has been performed. Samples of silver with a thin and thick corroded layer were used. In the case of a thin layer, the surface of pure silver was contaminated with fingerprints. AES analysis showed that the layer with the thickness of 20 nm consisting of O, S, Cl and C was formed. In the case of a thick layer, a well corroded silver coin from 19th century was used. In this case, the thickness of the corroded layer was of the order of 0.1 mm and the EMPA investigation showed it was an agglomerate consisting of O, S, Cl, Si, C, Fe, Ti. All samples were exposed to a low pressure weakly ionized hydrogen plasma at the pressure of 1 mbar. Plasma parameters were measured with a double Langmuir probe and a catalytic probe. The electron temperature was 6eV, plasma density $2.10^{16}m^{-3}$, and the degree of dissociation of hydrogen moleculs about 1%. Samples with the thin corroded layer were exposed to plasma for 10 minutes. AES analysis of the treated samples showed that all impurities were completely removed from the surface. The coin was exposed to hydrogen plasma at the same conditions, and the EMPA analysis showed that concentration of oxidizing impurities was lowered but other impurities still persisted.They could not be removed solely by treatments in plasma, but successive treatment in plasma and ultrasound bath. By the combination of both treatment we were able to decrease the concentration of any impurities below the detection limit of the EMPA.

Interakcija vodikove plazme s korodirano površino srebra

Ključne besede: materiali kontaktov električnih, čiščenje kontaktov, čiščenje površin, čiščenje površin kontaktov, čiščenje kovin, čiščenje plazemsko, čiščenje razelektritveno, razelektritve električne, H-plazma vodikova, artefakti arheološki, interakcija H-plazme vodikove s površino, površine korodirane, korozija materialov, korozija površin

Povzetek: Prikazujemo rezultate eksperimentalne preiskave plazemskega čiščenja korodirane površine srebra. Uporabili smo srebrne vzorce s tanko in debelo korodirano plastjo. V primeru tanke korodirane plasti smo površino čistega srebra kontaminirali s prstnimi odtisi. AES preiskava teh vzorcev je pokazala, da je na površini prisotna tanka plast nečistoč debeline 20 nm, ki vsebuje poleg srebra še O, S, Cl in C. V primeru debele plasti smo izbrali močno korodiran srebrni kovanec iz 19. stoletja. V tem primeru je bila debelina korodirane plasti reda velikosti 0,1 mm. Preiskava vzorca z elektronskim mikroanalizatorjem je pokazala, da površinski aglomerat vsebuje naslednje elemente: O,S,Cl,Si,C,Fe in Ti.

Vsi vzorci so bili izpostavljeni nizkotlačni šibkoionizirani vodikovi plazmi pri tlaku 1mbar. Plazemske parametre smo merili z dvojno Langmuirjevo sondo in katalitično sondo. Elektronska temperatura je bila 6 eV, gostota plazme $2x10^{16}$ m^{-3} in stopnja disociiranosti vodikovih molekul okoli 1%. Vzorci s tanko korodirano plastjo so bili izpostavljeni vodikovi plazmi za 10 minut. AES preiskava tako obdelanih vzorcev je pokazala, da smo odstranili vse nečistoče površin. Kovanec je bil izpostavljen vodikovi plazmi pri enakih pogojih in analiza z elektronskim mimkroanalizatorjem je pokazala, da je po obdelavi koncentracija oksidativnih nečistoč bistveno zmanjšana, medtem ko so ostale nečistoče na površini še vedno prisotne. Slednje nismo uspeli odstraniti samo z plazemskim čiščenjem temveč smo jih uspešno odstranili s kombinacijo plazemskega in ultrazvočnega čiščenja. S kombinacijo obeh metod smo uspeli kovanec tako dobro očistiti, da je koncentracija katerih koli nečistoč na površini manjša kot je meja detekcije elektronskega mikroanalizatorja.

1 Introduction

Discharge cleaning has become a widely used method for removing surface impurities. Active particles which are created in plasma, interact with surface impurities forming volatile molecules which are easily desorbed and pumped away. By creating plasma in a mixture of various gases, it is possible to remove different types of impurities. For reduction of surface layers of oxides, hydrogen or a mixture of a noble gas and hydrogen is usually used. In the past decade, this method has been widely investigated as it is of a great scientific and commercial importance. The method has been successfully applied in cleaning of stainless steal surfaces of tokamaks /1,2,3/, silicon in microelectronic devices /4,5,6,7/ and a variety of metals and alloys archaeological artifacts are made from /8,9,10/. Although hydrogen plasma can be created by different DC and high frequency discharges, the radio frequency (RF) and microwave (MW) discharges are the most suitable for this application. This is due to the fact that a plasma with a smal space potential can be created with a high frequency discharge, and it penetrates fairly well in gaps between samples. The degree of ionization in a high frequency discahrge is usually low (between 10^{-6} and 10^{-2}) /11,12/, except in the case the electron cyclotrone resonance (ECR) conditions are met /13/. In the latter case, the degree of ionization can be more than 10% /14/. In any case, the degree of dissociation of hydrogen molecules is more than 1% /12/ and can approach unity if a plasma is created in a discharge vessel made of material with a low recombination coefficient for the reaction $2H \rightarrow H_2$, i.e. different glasses, alumina, some ceramics /14/.

Despite the discharge cleaning of silver and its alloys is of a great importance in electronic industry as it is an excellent method of final treatment of contact materials, little work on this subject has been published. In the present paper, we describe experimental work recently done at our laboratories on discharge cleaning of silver with a thin and a thick layer of impurities.

2 Experimental

Experiments were carried out in a vacuum system, which consisted of a discharge vessel, a liquid nitrogen cooled trap and a two stage mechanical rotary pump.

The base pressure in the system was 10^{-3} mbar. The discharge vessel was a glass cylindrical tube with the lenght of 80 cm and the diameter of 4 cm. Plasma in the discharge vessel was created at the pressure of 0.5 mbar by an inductively coupled RF generator with the frequency of 27.12 MHz and the maximum output power of 700 W. Plasma parameters were measured with a double Langmuir probe /15/, and a catalytic probe /14,16/. The electron temperature in plasma was 6eV, while the plasma density was 2.10^{16} m^{-3}.

The use of a liquid nitogen cooled trap was found to be very important not only as a trap for oil form the rotary pump, but especially as a trap for aggresive gases forming during the discharge treatment of well corroded samples. Namely, during the treatment of archeological artifacts, a rather large amounts of H_2S and HCl were produced, and both of the gases could have been harmful to the pump.

Two types of samples were prepared: i) strips made of pure silver, and ii) old silver coins. The strips were first cleaned with freon and than touched well with fingers in order to obtain a thin layer of different impurities on the surface. The coins were discovered recently, and only the layer of sand and soil was removed by an archeologist. We treated them in ultrasound bath in a mixture of water and detergent in order to remove weakly bonded impurities from the samples, mostly hydrocarbonaceus compounds.

Samples with a thin layer of surface impurities were analyzed with an Auger electron spectroscopy (AES) depth profiling. We used a scanning Auger microprobe (Physical Electronics Ind. SAM 545 A) with a static primary electron beam with the energy of 5 keV, the beam current of 0.5 μA, and the beam diameter of about 10 μm. The incidence angle of the electron beam with respect to the normal of the surface plain was 30°. In order to obtain depth profile, samples were sputtered with Ar^+ ions with the energy of 1keV, rastered on a surface area larger than 10 x 10 mm^2. Atomic concentrations were calculated by taking into account relative sensitivity factors according to the literature /17/. The concentrations are plotted against ion gun sputter time instead of the depth, and 1 minute sputter time corresponds to the depth of about 2 nm.

The thickness of the layer of impurities on silver coins was too large to be analyzed with AES depth profiling, and the method is destructive anyway. The concentration of elements on the surface of these samples was determined with an electron microprobe analysis (EMPA). A scanning electron microscope JEOL JSM 35 with an energy dispersive X ray microanalyser (EDX-TRACOR TN 2000) was used to determine the concentration of elements in the surface layer. An electron beam with the voltage of 20 kV and current of approx. 0.5 mA was focused at the sample in a spot of about 1 x 1 μm^2. The thickness of the layer analyzed by EDX was about 1 μm.

3 Results

The composition of the surface layer of industrial cleaned silver strips and those contaminated with fingerprints was analyzed with AES depth profiling and is shown in Figure 1 and 2, respectively. It is noticeable that both samples contain a surface layer of impurities with the thickness of the order 0.1 μm . The composition of the impurity film on the samples is only slightly different. Both samples contain mostly carbon (probably an organic compound), oxygen, chlorine, sulphur and potassium.

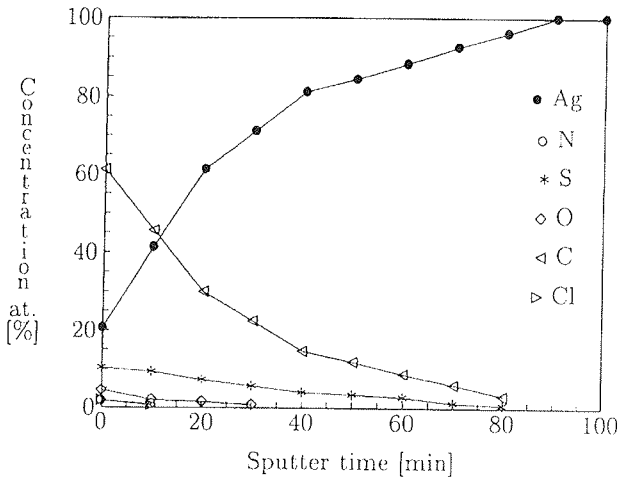

Fig. 1. AES depth profile of the surface layer of the industrial cleaned silver strip.

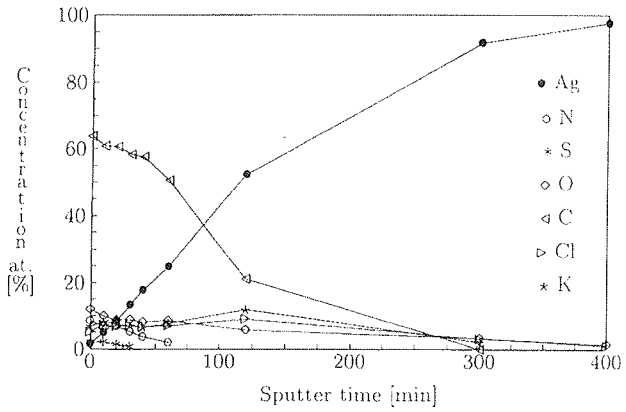

Fig. 2. AES depth profile of the surface layer of the silver strip cleaned with freon and later contaminated with finger prints.

Both samples were mounted in the middle of the discharge vessel and treated with hydrogen plasma for 10 minutes. Due to the recombination of atomic hydrogen on the sample surfaces, the absorption of UV light from plasma, and the bombardment of the surfaces with charged particles, the temperature of the samples raised to about 150°C. After the treatment the samples were exposed to air for a short time and analyzed with AES sputter depth profiling again. The composition of the surface of the samples is shown in Figure 3 and 4. It is noticeable that the surface of both samples is clean except of traces of oxygen and sulphur which were probably adsorbed on the surface during the exposure of the samples to air.

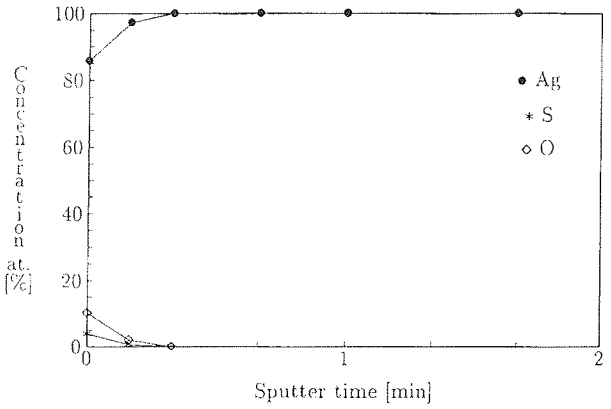

Fig. 3. AES depth profile of the surface layer of an industrial cleaned silver strip which was exposed to hydrogen plasma for 10 minutes.

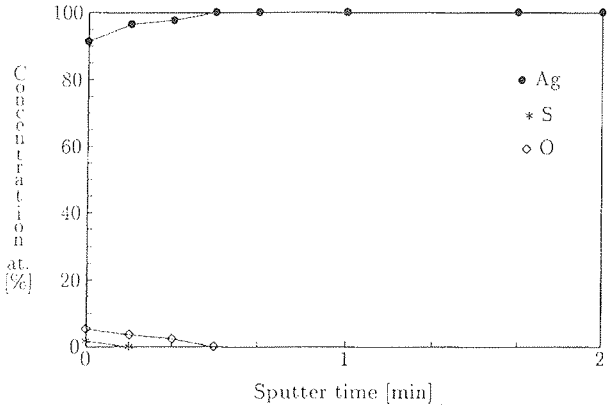

Fig. 4. AES depth profile of the surface layer of a silver strip first cleaned with freon, than contaminated with finger prints and exposed to hydrogen plasma for 10 minutes.

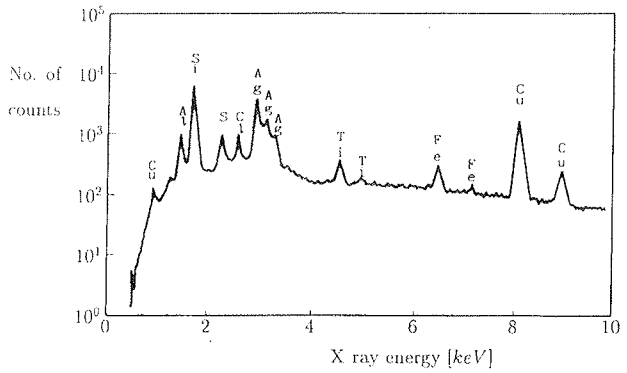

Fig. 5. EDX spectrum of the surface layer of the silver coin before discharge cleaning.

Before the plasma treatment, a silver coin was analyzed with EMPA (Figure 5). Apart from oxygen and carbon, which cannot be detected with our microprobe, the layer of impurities of the surface consisted of silver, iron, copper, silicon, sulfur, and chlorine.

The sample was treated with plasma for 10 minutes. After the treatment it was analyzed with the electron microprobe. The only change was a substantial enlargement of iron peak. It was also found that, after the plasma treatment, the layer of impurities on the surface can be rather easily removed mechanically by the use of a needle. Since we did not want to make any scratch on the sample, we rather treated it in the ultrasound bath and some impurities were released. Microprobe analyses showed that the concentration of iron fell to the original value. The sample was then treated again with plasma for 10 minutes. After this treatment, a part of the surface became clean, while most of the surface was still covered with a layer of impurities. The microprobe analyses showed that the clean part of the surface consisted of silver and about 10% of copper (which is actually the structure of the bulk), and the dirty part of the surface consisted of iron, silver, copper, sulfur and chlorine. After repeating the plasma cleaning and the ultrasound cleaning for four times, all the surface became clean. The microprobe analyses showed only silver and cooper, while the concentration of other elements was below the detection limit of the microprobe which was about 01. at.% (Figure 6).

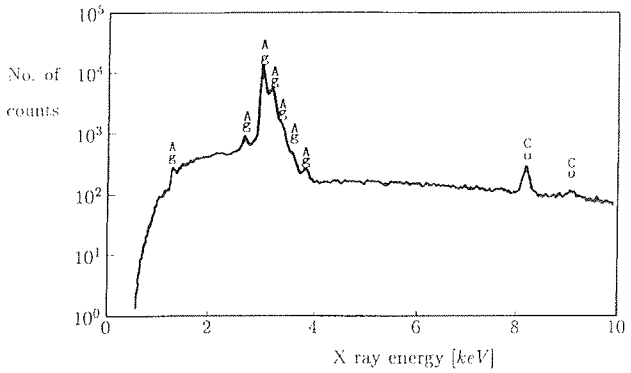

Fig. 6. EDX spectrum of the surface layer of a silver coin after successful cleaning in hydrogen plasma and ultrasound bath.

4. Discussion

The experiments described above showed that active particles produced in hydrogen plasma react with the impurities bonded to the surface of the samples. Since the density of plasma is low it is obvious that hydrogen ions do not contribute much to the cleaning efficiency. It is probably atomic hydrogen which reacts with the surface impurities. Hydrogen atoms react with chemically bonded oxygen, chlorine, and sulfur to form molecules, which are easily pumped from the discharge vessel: OH, H_2O, HCl, H_2S, etc. These gases are then trapped by the liquid nitrogen cooled trap.

The appearance of iron in the impurity layer after the plasma treatment can not be due to a deposition of iron since plasma was not in a contact to any material composed of iron. A small amount of iron was presented within the layer of impurities already before the

treatment. The original concentration of iron is rather low. During the discharge treatment, most of other impurities were removed from the surface, so the relative concentration of the iron in the surface layer was increased substantially.

Iron cannot be removed from the surface with mild hydrogen plasma cleaning. Further-more, a layer of iron on the surface probably causes intensive recombination of atomic hydrogen on the surface and thus prevents successful removal of other impurities from deeper layers. Luckily, the layer of iron is weakly bonded to the surface, so it can be successfully removed mechanically either by the use of a needle or even by the use of ultrasound treatment. Once the layer of iron is removed, further removal of other impurities in hydrogen plasma can take place, so that after repeating the discharge cleaning and the ultrasound cleaning for several times, the surface of the samples became free of any impurities.

5. Conclusion

Discharge cleaning experiments on silver samples were carried out in low pressure weakly ionized hydrogen plasma. It was shown that most impurities can be removed from the samples by treatment in hydrogen plasma with the density of 2.10^{16} m^{-3} and the electron temperature of 6 eV. In the case of a thin layer of impurities, the samples were analyzed with AES depth profiling and it was shown that a layer of chemically bonded oxygen, chlorine, sulfur, carbon and silicon can be completely removed in ten minutes. Discharge cleaning of well corroded silver coins took nearly an hour. In this case, it was shown that iron, which was also presented in the layer of impurities, could not be removed by treatment in hydrogen plasma. Furthermore, it prevented sucessful removal of other impurities. A successful procedure of removal iron from the surface was found to be the ultrasound tretament. By repeating the discharge and ultrasound cleaning procedures it was possible to remove a thick layer of impurities as well.

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REACTIONS ON CATALYTIC PROBE SURFACE DURING OXYGEN PLASMA TREATMENT OF POLYETHER SULPHONE

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Keywords: catalytic probes, nickel catalytic probes, surface reactions, plasma treatment, oxygen plasma, polyether sulphone, surface activation, plasma etching, plasma dry etching, RF discharges, RadioFrequency discharges, T-t temperature-time characteristics

Abstract: Experiments on the behavior of a nickel catalytic probe during activation of the surface of polyether sulphone in oxygen plasma are described. The temperature of the probe mounted 30 cm apart from inductively coupled RF oxygen plasma was measured for the case of empty discharge vessel and the case a sample with the dimensions of 8 cm x 1.2 cm x 0.4 cm was mounted in the middle of the discharge coil. It was found that both the maximum temperature and the first time derivative of the probe was much higher in the case of loaded discharge vessel than in the case of empty vessel. Both effects were described in terms of a higher probability for recombination of radicals such as CO on the probe surface than the recombination of neutral oxygen atoms.

Reakcije na površini katalitične sonde med plazemsko obdelavo polieter sulfona

Ključne besede: sonde katalitične, sonde katalitične nikljeve, reakcije površinske, obdelava s plazmo, plazma kisikova, polieter sulfon, aktiviranje površine, jedkanje plazemsko, jedkanje suho plazemsko, RF razelektritve radiofrekvenčne, T-t karakteristike temperatura-čas

Povzetek: Prikazujemo obnašanje nikljeve katalitične sonde med aktivacijo površine polieter sulfona v kisikovi plazmi. Merili smo temperaturo sonde, ki je bila nameščena 30 cm od induktivno sklopljene RF kisikove plazme v primeru prazne razelektritvene komore in v primeru, ko smo v sredino razelektritvene tuljave namestili vzorec z dimenzijami 8 cm x 1.2 cm x 0.4 cm. Ugotovili smo, da sta tako navečja temperatura, ki jo doseže sonda, kot tudi prvi časovni odviod temperature sonde po vklopu RF generatorja, precej večja v primeru, ko je v razelektritveni komori nameščen vzorec, kot v primeru, ko je komora prazna. Oba pojava smo tolmačili z večjo verjetnostjo za rekombinacijo radikalov kot je CO na površini sonde, kot je verjetnost za rekombinacijo nevtralnih atomov kisika.

1. Introduction

Oxygen plasma has become widely used for low temperature treatment of organic materials in research laboratories and industry. Technologies based on application of oxygen plasma include degreasing of different components /1/, plasma dry ashing /2/, activation of polymer surfaces for painting/printing /3/, and plasma ashing of biological samples /4/. Oxygen plasma for surface treatment of different samples is created in low-pressure discharges, such as microwave discharge (both non-magnetized and ECR modes), RF discharge (inductively and capacitively coupled) and a variety of DC discharges. Discharges are usually created in vacuum chambers made of a material with a low recombination coefficient for the reaction $2O \rightarrow O_2$, such as metals, which form thin films of stable oxides, glasses and ceramics. For different application, oxygen plasma with different parameters is used. By changing the type of the discharge, the discharge power, dimensions of the discharge vessel, pressure and pumping speed, one can obtain oxygen plasma with different parameters, i.e. the density and energy distribution of various particles created in plasma. In any case, the plasma is thermodinamical non-equilibrium. In most cases, the energy distribution function of each type of particles is close to Maxwellian, so the temperature is defined according to the rules of statistical mechanics. The electron temperature in plasma is usually several 10000°C (average kinetic energy of several eV), while the temperature of heavy particles is often close to the temperature of the inner wall of the discharge vessel.

Due to inelastic collisions with hot electrons, the density of excited states of oxygen molecules in the discharge differs significantly from the values found in thermodinamical equilibrium gas. The density of electrons and positive ions is often within 10^{15} - 10^{17} m^{-3} bracket, the density of negative oxygen ions is usually an order of magnitude lower, the density of neutral oxygen atoms is often around 10^{20} m^{-3} and sometimes even one or two orders of magnitude higher. The same applies for the density of ozone molecules (O_3). Many particles are found in excited states. Molecules are found in high rotational and vibrational states and also in single electron excited states. Excited states are usually relaxed by photon emission so plasma is an effective source of radiation ranging from IR to UV light.

Several techniques have been used for determination of plasma parameters including electrical probes, magnetic probes, mass spectrometry, spectral intensities, line broadening, optical and ultra violet techniques, X - ray spectroscopy, far infra - red techniques, optical interferometry and microwave techniques /5/. For determination of the density of neutral atoms catalytic probes proved useful /6/.

Many oxygen particles created in plasma react with the organic samples treated. Oxygen atoms, for instance, can react with the surface of hydrocarbons either by being trapped on the surface causing oxidation of the material or forming volatile molecules (such as CO and OH) which leave the surface. In any case, plasma parameters are altered by the presence of organic

samples in the discharge vessel. It is clear that the density of oxygen atoms in the presence of samples is lower than in an empty discharge vessel. Some atoms are lost since they remain in the surface layer of the samples, and more are lost because they form light molecules (radicals as CO and OH finally form stable molecules - carbon dioxide and water). The change of the density of neutral reactive particles can be monitored by the use of a catalytic probe. In the present paper we show how the presence of a polymer sample alters the behavior of a catalytic probe.

2. Experimental

Experiments were performed in a glass discharge tube with the inner diameter of 36 mm and the length of 60 cm. Oxygen plasma was created at one side of the discharge vessel within a coil with the length of 15 cm, which was connected to an RF generator with the frequency of 27.12 MHz and the nominal power of 700 W. A catalytic probe was mounted on the other side of the discharge vessel. The probe is shown in Figure 1. The distance between the coil and the probe was 30 cm. The temperature of the probe after turn on of the RF generator was measured at different pressure. For the case of an empty discharge vessel, the temperature versus time is shown in Figure 2, 3 and 4.

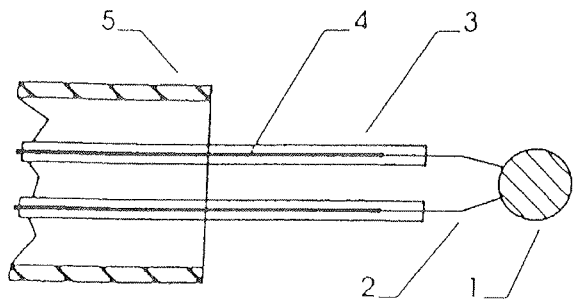

Fig. 1. Catalytic probe. 1 - nickel disc with the radius of 1 mm and the thickness of 0.2 mm, 2 - chromel - alumel thermocouple wires with the radius of 0.0625 mm and the length of 20 mm, 3 - thin glass tube with the outer diameter of 1.8 mm, 4 - kovar wire with the radius of 0.6 mm, 5 - glass tube with the outer diameter of 7 mm.

After the experiments with the empty vessel, a sample was mounted in the middle of the RF coil. The sample was made of polyether sulphone (PES) of a rectangular shape with the length of 8 cm, the width of 1.2 cm and the thickness of 0.4 cm. The temperature of the probe during the first 10 s after turn on the RF generator is shown in Figure 5, 6 and 7.

3. Results

Measurements of the temperature of the catalytic probe summarized in Figure 2 - 7 show that exotermic reactions take place on the probe surface when the RF generator is on. For the first few seconds after turn on the generator, the temperature increases linearly with time, and after some time, a constant temperature is obtained. The time needed for reaching the steady temperature depends on the pressure in the vacuum system. In the case of empty discharge vessel, the constant temperature is obtained in 20 s at the pressure of around 100 Pa, and in 40 s at the pressure of about 10 Pa. When the sample is mounted in the discharge vessel, the measurements of the temperature were performed only during the first 10 s so not in all cases the constant temperature is obtained. Still, comparison of Figures 4 and 7 show, that the time needed to reach the constant temperature of the probe depends on what's in the discharge vessel. In the case of the PES sample in the discharge vessel, the time needed to reach the constant temperature is at least for a factor of 2 smaller than for the empty discharge vessel.

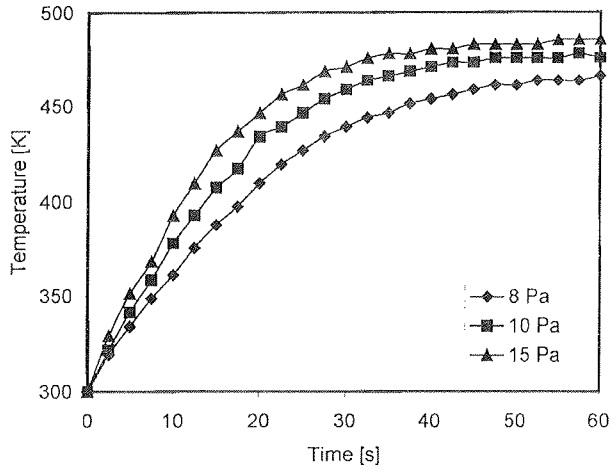

Fig. 2. Temperature of the nickel catalytic probe in empty discharge vessel during the first 60 s after turn of the RF generator at low pressure.

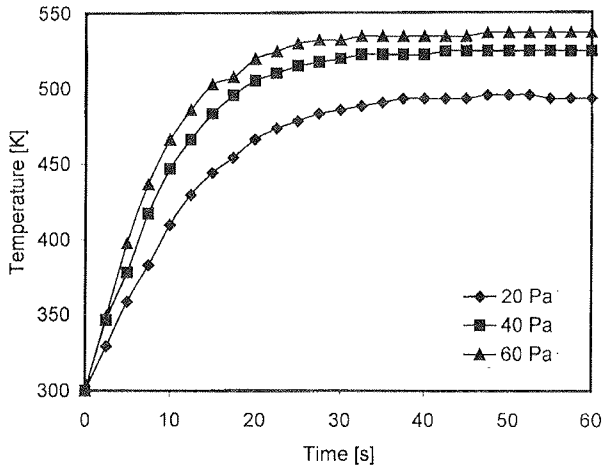

Fig. 3. Temperature of the nickel catalytic probe in empty discharge vessel during the first 60 s after turn of the RF generator at medium pressure.

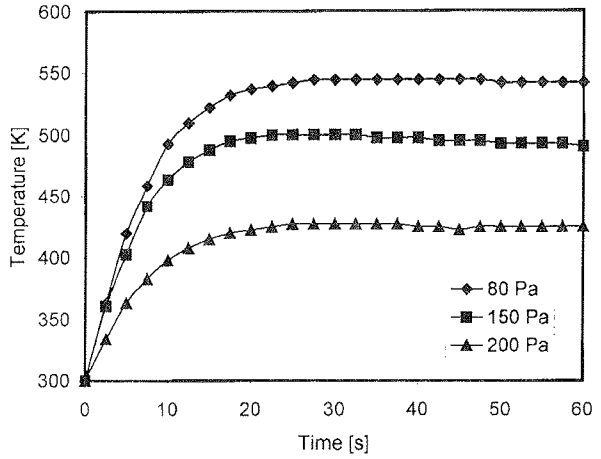

Fig. 4. Temperature of the nickel catalytic probe in empty discharge vessel during the first 60 s after turn of the RF generator at high pressure.

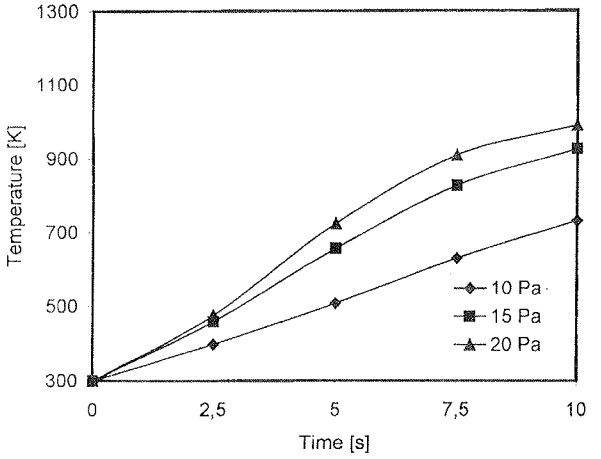

Fig. 5. Temperature of the nickel catalytic probe in loaded discharge vessel during the first 60 s after turn of the RF generator at low pressure.

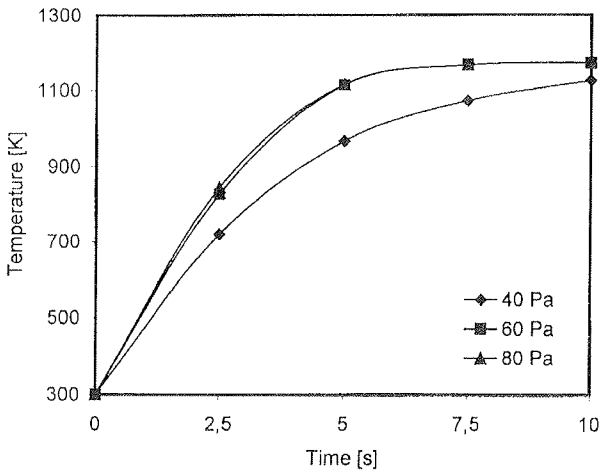

Fig. 6. Temperature of the nickel catalytic probe in loaded discharge vessel during the first 60 s after turn of the RF generator at medium pressure.

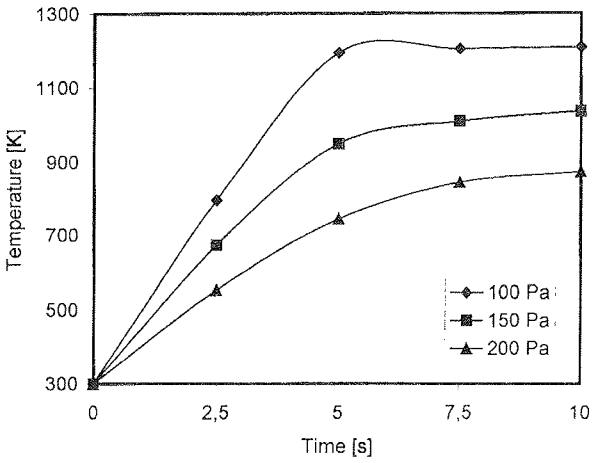

Fig. 7. Temperature of the nickel catalytic probe in loaded discharge vessel during the first 60 s after turn of the RF generator at high pressure.

From the curves of the probe temperature versus time (Figure 2 - 7) the fist time derivative after turn on the RF generator is calculated. The results are summarized in Figure 8. In the case of empty discharge vessel, the first derivative of the probe temperature is of the order of 10 K/s, while in the case of the discharge vessel with the sample it is an order of magnitude higher. In both cases, the derivative at low pressure increases with increasing pressure, reaches the maximum at the pressure of about 80 Pa and decreases with further increase of the pressure.

4. Discussion

Measurements of the first time derivative of the probe temperature give valuable data on the state of the gas in the vicinity of the probe /7,8/. If the gas is in the state of thermodinamic equilibrium, the temperature of the probe will remain unchanged, as the discharge vessel near the probe remains at room temperature. The rate of heating of the probe is therefore a measure of the non-equilibrity of gas in its vicinity. The higher the first derivative, the higher non-equilibrium of the gas. In the case of pure gas, the first time derivative of the probe gives semi-quantitative values on the density of neutral oxygen atoms in the gas /7/:

$$n_O = \frac{4Mc_p}{v\gamma W_D \pi r^2}\frac{dT}{dt},$$

where n_O is the O density near the probe, M the probe mass, c_p the thermal capacity of the material the probe is made of, v the average thermal velocity of oxygen atoms, γ the recombination coefficient for oxygen atoms on the probe surface, W_D the dissociation energy of oxygen molecule, r the probe radius and dT/dt first time derivative of probe temperature just after turn on of the RF generator. For the case the probe is made of nickel and its surface is covered with a thin film of nickel oxide, the constants in equation (1) are as follows: M = 5.6 x 10^{-6} kg, c_p = 444 J/kgK, v = 700 m/s, γ = 0.04,

W_D = 5.12 eV, r = 1 mm. Taking into account the measured values of dT/dt, which are about 10 K/s, the density of oxygen atoms in the vicinity of the probe is 1.4 x 10^{21} m^{-3} what is a reasonable result.

When a sample is placed in the discharge vessel, the density of oxygen atoms drops according to the discussion in chapter 1. However, the first derivative of the probe temperature did not drop at all. Moreover, the derivative increased for an order of magnitude, as can be seen in Figure 8. The result is certainly worth a discussion.

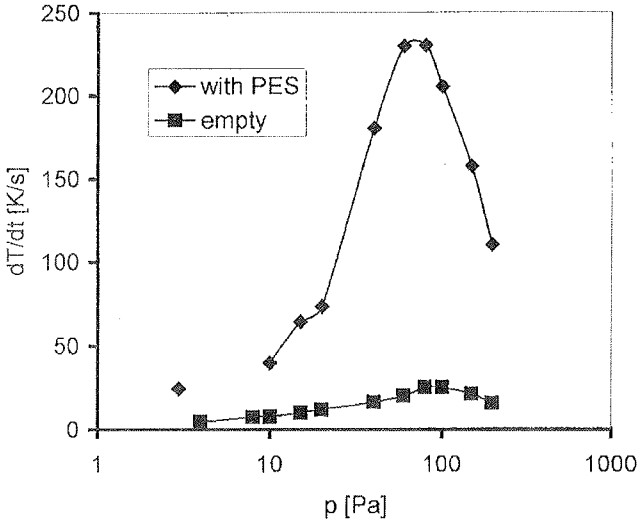

Fig. 8. Time derivative of the temperature of the catalytic probe after turn on the RF generator at different pressure in the case of empty and loaded discharge vessel.

In the case of empty discharge vessel, the probe is heated mainly due to recombination of neutral oxygen atoms on its surface. The probability of recombination (i.e. the recombination coefficient) for this reaction is rather low: γ = 0.04 /9/ and the O concentration in the vicinity of the probe rather high (of the order of 10^{21} m^{-3}, as calculated above).

When the sample is mounted into the discharge vessel, the density of neutral oxygen atoms drops as they react chemically on the sample surface forming molecules like OH and CO. So one would expect that the derivative of the probe temperature would drop as well. However, newly formed molecules may also chemisorb on the probe surface and react with other particles reaching the surface. The most probable reaction taking place on the probe surface is CO + O → CO_2. Other exothermic reactions may also occur on the probe surface. Due to all these reactions, the energy dissipation on the probe remains high although the density of O atoms is lowered.

The energy dissipated on the probe surface at the reaction O + O → O_2 is similar to the energy dissipated at the reaction CO + O → CO_2, i.e. few eV. If the probability of both reactions is the same, the time derivative of the probe temperature will not change much for the cases of empty and loaded discharge vessel. The experimental results, however, showed that the derivative of the probe temperature increased for an order of magnitude when the sample was mounted into the discharge vessel. Therefore, one can conclude that the probability of oxidation of carbon monoxide on the probe surface is much higher than the probability of the recombination of oxygen atoms.

5. Conclusions

Experiments on the behavior of nickel catalytic probe placed in the discharge vessel were described. The time dependence of the temperature of the nickel catalytic probe was measured at different pressure for the case of empty discharge vessel and the vessel loaded with a sample of polyether sulphone of a rectangular shape with the length of 8 cm, the width of 1.2 cm and the thickness of 0.4 cm. The measurements showed that for the first few seconds after turn on the plasma source the temperature of the disc rised linearly with time, and after about 10 s the constant temperature was obtained. The constant temperature of the probe depended on pressure and whether the discharge vessel was loaded with the sample or not. For the case of the loaded vessel, the constant temperature of the probe rised over 1000 K at any pressure between 40 and 150 Pa, while at higher and lower pressure the constant temperature was less than 1000 K. For the case of the empty discharge vessel, the maximum temperature of nearly 550 K was obtained at the pressure of 80 Pa. The first time derivative of the probe temperature after turn on the plasma source was of the order of 10 K/s for the case of empty discharge vessel, and of the order of 100 K/s when the sample was mounted into the discharge vessel. In both cases, the derivative increased with increasing pressure up to the pressure of about 80 Pa where the maximum value of about 25 and 230 K/s, respectively, was reached, and decreased with further increase of the pressure. It was suggested that the higher rate of heating of the probe in the case of the sample placed in the discharge vessel was due to a higher probability of reaction of CO and OH molecules on the probe surface than the probability of recombination of oxygen atoms on the same surface.

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APLIKACIJSKI PRISPEVKI - APPLICATION ARTICLES

Novitete iz razvoja podjetja Iskre Žarnice Elvelux

Uvod

Podjetje Iskra Žarnice 10 let ni imelo novitet iz lastne proizvodnje. V zadnjih dveh letih pa je vložila kar precej sredstev v ustrezne kadre, opremo in v razvojna prizadevanja.

Odprte in potrjene ima tri večje razvojne projekte z Ministrstvom za znanost in tehnologijo.

Stanje tehnike v svetu

V svetu obstojajo dve osnovni smeri v proizvodnji žarnic.

Prva smer deluje z zastarelo opremo in številno delovno silo. Na posamezni proizvodni liniji, ki je praviloma namenjena eni vrsti žarnic, v več razredih napetosti, je v eni izmeni 10 do 60 zaposlenih. Mesečni osebni dohodki neposrednih delavk v taki proizvodnji so na nivoju 75 do 100 Dem, inženirjev pa 125 do 150 Dem. Cena proizvodov je zaradi minimalne amortizacije zastarele strojne opreme in nizke cene delovne sile nizka. Končna kontrola je osebna in nestabilna. Doseženi vakuum v žarnicah je za 10-krat ali več nižji od zahtevanega. Kvaliteta je slaba, uporabljani so ceneni materiali.Proizvodi niti zdaleč ne odgovarjajo standardom. Take avtomobilske žarnice hitro pregorijo. Svetijo celo manj kot 10 % od zahtevanih standardiziranih časov. Nikoli ne dosegajo nivoja kvalitete prve vgradnje pri proizvajalcu vozil. Uporabljajo se le v trgovanju kot rezervni deli. Žal kupci največkrat gledajo le na ceno in kaj malo na kvaliteto. Zato je možno žarnice take kvalitete kupiti tudi pri nas. Resne organizacije kot so Petrol in OMV jih ne nudijo. Zastarela oprema za proizvodno linijo stane v nivoju 15.000 do 30.000 Dem.

Druga smer je v visoki avtomatizaciji proizvodnje z vpeljano robotiko, pnevmatiko, hidravliko, senzoriko in elektroniko. Regulacija plinov in vakuuma je natančna in avtomatska. Oprema za novo proizvodno linijo, na kateri pa je mogoče delati le en tip žarnice, stane od 3 do 7 milijonov Dem. Na posamezni liniji sta največ do dva zaposlena v vsaki izmeni. Vsa končna kontrola je avtomatska. Firme s tako opremo proizvajajo žarnice vrhunske kvalitete v 3 izmenah dnevno in s po dvemi 12-urnimi izmenami v soboto in nedeljo. Linije delujejo cca 3-4 hitreje kot pri nas. Produktivnost ene moderne linije je med 3000 in 6000 žarnic kosov na uro. Izmet je minimalen, pod 2 %.

Seveda pa je delovna sila v Nemčiji, Franciji in Italiji kar 4-krat dražja kot pri nas in amortizacija opreme zelo visoka. Oprema, ki jo poseduje podjetje Iskra Žarnice, je nekje vmes, žal močno bližje prvi skupini proizvajalcev. Najmlajša proizvodna linija je stara preko 22 let. Slične linije imajo na Poljskem in Češkem.

Povsem nove razvojne usmeritve zahtevajo žarnice z daljšo življenjsko dobo. Serijsko se še ne vgrajujejo.

Kako dalje v Iskri Žarnice

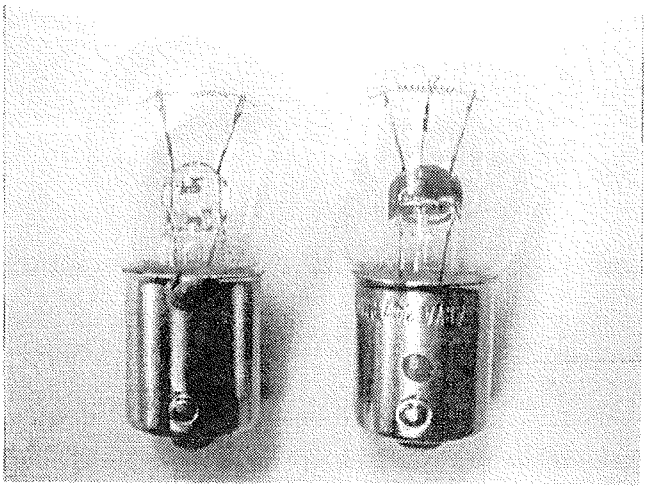
Za najnižji nivo cen žarnic, ki prihajajo iz proizvodnje po prvi usmeritvi, je delovna sila v Sloveniji predraga. Zato smo se zavestno usmerili v kvaliteto prve vgradnje za proizvajalce vozil, kjer je trg sicer 5 x manjši, a so cene za vsaj 50 % višje. Tu proizvajamo za velike svetovne firme kot so Osram, Philips, Narva in Hella pod njihovimi zahtevami kvalitete in njihovimi imeni.

Prav tako smo se usmerili v žarnice in na trge, ki zahtevajo spoštovanje IEC predpisov ter proizvajamo žarnice pod tujo blagovno znamko za zahtevne kupce pod njihovimi imeni. Ti so iz Nemčije, Francije, Italije in Španije in so nekoč proizvajali avtožarnice in jih je konkurenčna tekma v produktivnosti izločila iz lastne proizvodnje, ne pa iz tržišča.Tu je dosežena cena še na robu rentabilnosti. Z modernizacijo obstoječih linij bo postala tudi ta proizvodnja dobičkonosna.

Tretja usmeritev je v nove žarnice posebnih izvedb, kvalitete v specifičnih tehnologijah, ki niso splošne in višje cene. Potrebujemo proizvodne linije s specifično tehnologijo, ki jo moramo zagotoviti z lastnim razvojem, kar dosežemo tako, da z dodatki in lastnim znanjem in znanjem bližnje okolice predelamo stare linije. Te pretežno kupujemo pri nekdanjih proizvajalcih žarnic naših partnerjih ali pa gre za že obstoječe linije, ki z razvojnimi postopki tako dobe več funkcij.

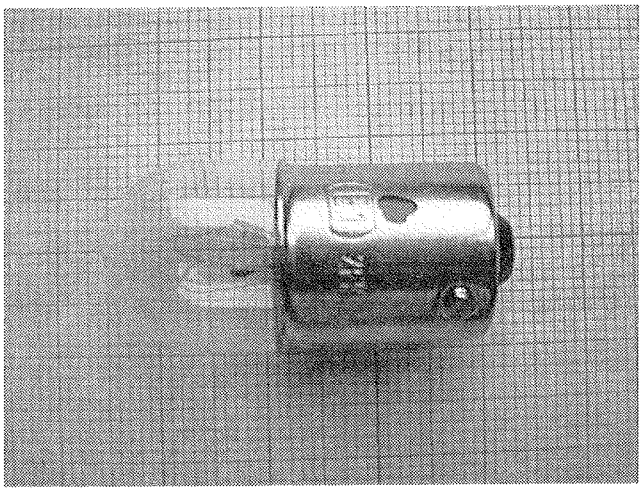
Povsem novi proizvodi v Iskri Žarnice so:

1.- Žarnice za težke pogoje dela za tovornjake, avtobuse, terenska vozila, gradbene stroje, ladje in namenska vozila.



Slika 1: Žarnice za težke pogoje dela HD 24 V 21 W. Razlika med konvencionalno žarnico in haevy duty HD žarnico. Lepo se vidi dodatni nosilec pri spremenjeni geometriji.

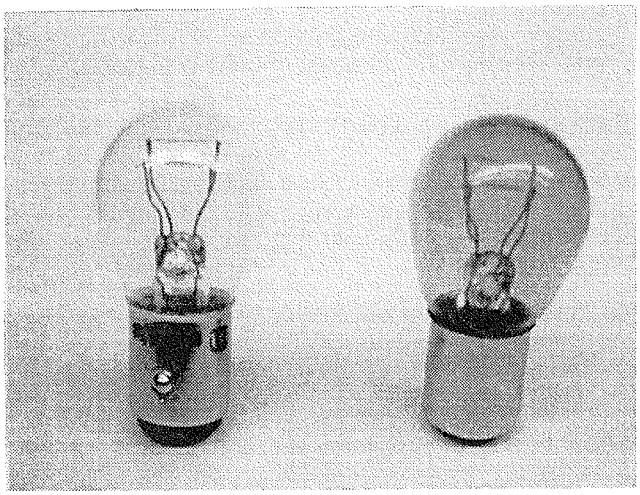
Gre skupno za 6 žarnic za 24 in 28 Voltne izvedbe, moči 21 W, 10 W ali 5 W na kovinskih podnožjih dimenzije s premerom 15 mm z različnimi dimenzijami balonov. Cena je od 40-50 % višja od cen žarnic iz iste proizvodne linije, ki so proizvedene na običajen način. Zaradi posebnih materialov za svetilne spirale, posebne geometrije in podpornih nosilcev so take žarnice 10 x bolj odporne na specifične vibracije kot navadne žarnice istih oblik in moči.



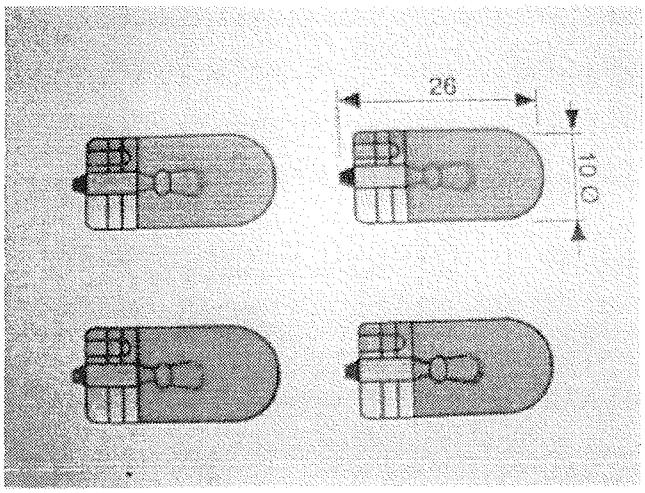
Slika 2: Žarnice za težke pogoje dela 24 V 10 W in 24 V 5 W

2. - Žarnice za smerokaze v jantar barvi. V Evropi so v množičnem vzponu. V prvi vgradnji jih bo v letu 1999 vgrajenih skupaj 12 milijonov kosov.

Izvedbe so predvsem enonitne žarnice 12 V 21 W s premerom 15 mm, ali dvonitne 12 V in 24 V z močjo 21/5W s premerom 15 mm ter žarnice brez podnožja v jantar barvi s premerom 10 mm v izvedbi Wolfram navitij 12 V 5 W. Cene so za sedaj 2 x višje od žarnic iz iste linije, ki niso barvane. Barva mora biti zelo obstojna na temperaturo nad 240° in vlago.

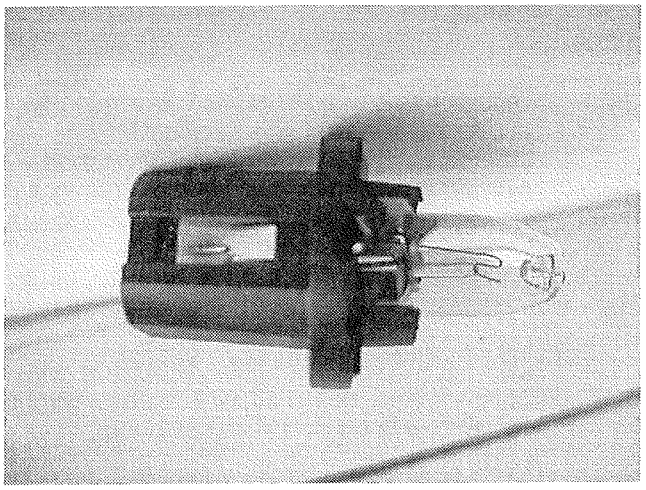


Slika 3: Prozorna žarnica in žarnice jantar barve za smerokaze



Slika 4: Jantar žarnice T10 za smerokaze in drugih barv za dekor v vozilu, modre, rdeče in zelene barve. Modre žarnice T10 se uporabljajo skupaj s halogenskimi žarnicami iste barve, ki so sedaj na pohodu v glavnih žarometih.

3. - Žarnice premera 4,8 in 5 mm za armaturno ploščo s plastičnim podnožjem. Uporabljajo se za osvetlitve merilnika hitrosti in vrtljajev, radijskih aparatov, števil nih instrumentov, klimatske naprave, vtičnic za vžigalnik in napajalne naprave kot je mobilni telefon in za osvetlitve kontrolnih točk. Cene so zaenkrat zelo visoke.V Evropi so te žarnice v silnem porastu. Le en proizvajalec jih potrebuje 120 milijonov kosov.

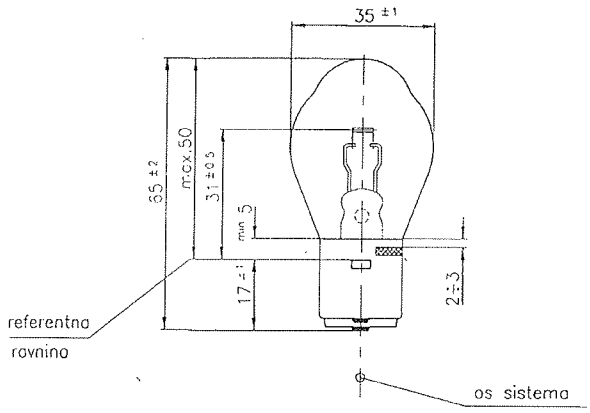


Slika 5: Osvetlitvene žarnice s plastičnim podnožjem za vgradnjo v armaturno ploščo

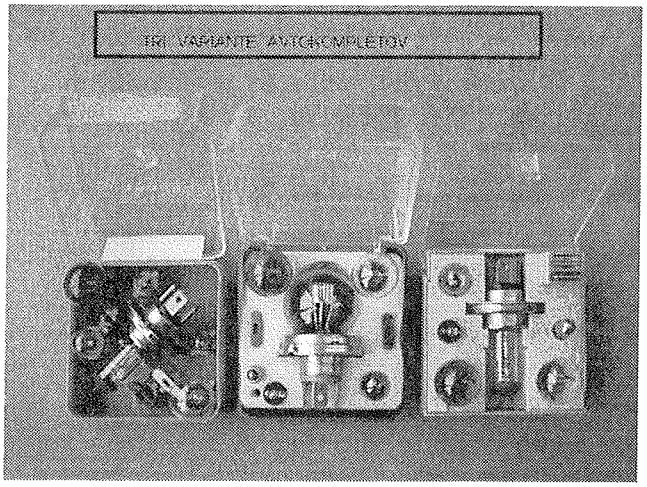
4. - Dekorativne žarnice za vozila z izvedenkami na steklenem podnožju T10 modre, rumene in rdeče barve

5. - Signalne žarnice za 4000 ur življenjske dobe, ki se proizvajajo na liniji za bilux žarnice. Imajo posebno obdelane spirale, visoko geometrijo in so polnjene s posebnimi plini. Največ uporabe je na železnici, v svetlobnih sirenah in v semaforizaciji.

Tipična življenjska doba žarnic za vozila je 250 ur.



Slika 6: Signalne žarnice s 15 x povečano življenjsko dobo



Slika 7: Večnamenski komplet žarnic v novem ohišju za obešanje kot pri blister embalaži za različne kombinacije žarnic v rezervi glede na vrsto vozila

6. - Dopolnilni program v širši paleti halogenskih žarnic. Zlate, ksenonske.

7. - Dopolnilni program za žarnice za solarije.

8. - Elektronika, ki omogoča cca 2 višjo izrabo energije v svetlobne namene in daljšo življenjsko dobo.

Sedanji izplen pretvorbe energije v svetlobo je od 8-12%.

9. - Nove prozorne škatle z notranjimi plastičnimi penastimi deli za različne žarnice za glavne žaromete H1, H4 in H7 z nastavkom za obeso kot za blister embalažo.

10. - Lastni komplet za registracijo, ki vsebuje komplet za avtožarnice za določeno vozilo, prvo pomoč in varnostni trikotnik

11. - Elektronika z vzvratnim žarometom (Saturnus) z našimi žarnicami in sireno

12. - Na področju dekorativnih žarnic smo v letu 1998 že osvojili izvedbe Piselli žarnic 24 in 28 V večinoma 1,2 W, v beli, rdeči, modri in zeleni barvi z različnimi dolžinami priključkov. Slede 1V in 1,3 V izvedbe ter še 6 V in 12 V. Uporabljajo se v religioznih dekoracijah, gondolicah z osvetlitvijo, v verigah za novoletno jelko, dekoracijah izložb in stanovanj in reklamnih napisih.

Osvajamo še 14 V 5 W izvedbo na Edisonovem navoju E 14 mm v različnih barvah.

Na področju tehnologij:

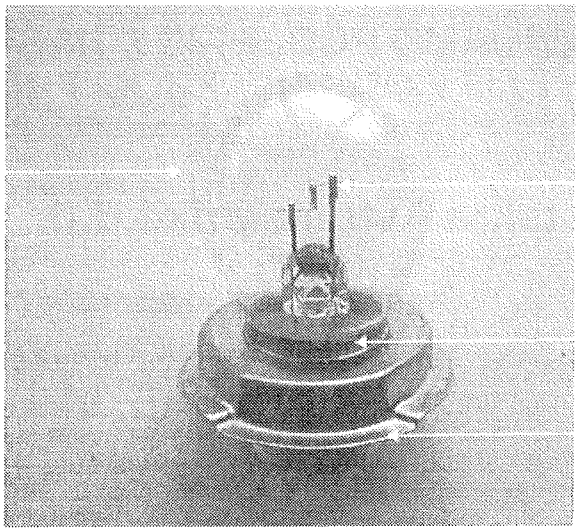
- smo osvojili lastni senčnik za 6 in 12 V žarometno dvonitno bilux simetrično žarnico za motorna vozila.
- osvajamo lastno 35 W omega spiralo, ki smo jo do sedaj uvažali. Vzorčne količine izdelanih žarnic z lastno tovrstno spiralo so zadovoljile tehničnim zahtevam. Slede 25 W izvedbe.
- povečali smo kapaciteto lastne špiralizacije z dodatno opremo in novimi izvedbami spiral
- avtomatizirali smo postopek vgrajevanja spirale za enonitno žarometno žarnico s podnožjem P26 S, kar omogoča nastop v prvi vgradnji v žaromete mopedov.
- obnovili smo proizvodnjo na zapuščeni liniji žarnic brez podnožja, kjer proizvajata v eni izmeni le dva zaposlena. Z inoviranjem dodajanja wolframove žice s posebnimi napravami in podajanja sistemov na liniji žarnic brez podnožja ter zniževanjem škarta, smo po dveh letih in pol mirovanja te linije ponovno vzpostavili veliko serijsko proizvodnjo. Izmet je, iz prejšnjih nerentabilnih tudi 50% za prvo vgradnjo, padel na rentabilnih 2-4 %.
- pri nemškem preizkusnem inštitutu smo pridobili na novo dve 24 V izvedbi žarnic T 10
- vzpostavili smo skupaj z zunanjim domačim partnerjem linijo za barvanje žarnic za smerokaze
- usposobili smo staro nakupljeno linijo za dekorativne žarnice tipa piselli za veliko serijsko proizvodnjo, kjer bo v bodoče proizvajal v eni izmeni le en polovično zaposlen strokovnjak. Imel bo še druge zadolžitve.
- znižali smo na stalno delujočih linijah letni škart v povprečju za 4 %. Izjema je linija za bilux žarnice, ki je sedaj v teku prenove. Prenova te linije je prednostna naloga razvoja in tehnologije.
- s tehnološkimi postopki smo povečali produktivnost posameznih linij. Pospešili smo linije za dvo nitne žarnice, za miniaturne žarnice asimetrične žarnice in eno nitne žarnice, ki sedaj dnevno proizvajajo več.

Sledi linija za proizvodnjo bilux žarnic,kjer se mora dnevna kapaciteta do konca leta dvigniti za 10 % in produktivnost na zaposlenega za 18 % ter izmet pasti za 3÷4% ter linija za asimetrične žarnice, kjer moramo produktivnost na zaposlenega do srede marca leta 1999 dvigniti za 15 %.

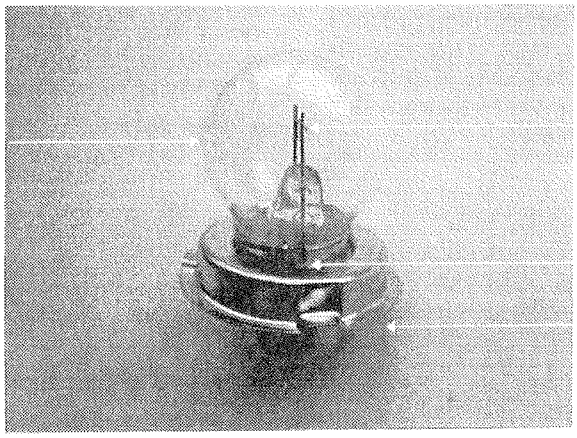
Na liniji za eno nitne žarnice se mora produktivnost na zaposlenega dvigniti po načrtih za 30 % ob uvedbi treh novih proizvodov.

V obnovi je stara kupljena linija za miniaturne žarnice.

Po modernizaciji bo produktivnost na zaposlenega 2-krat višja kot na obstoječi liniji za enake proizvode in izmet nižji za 50 %. Dosežke s te linije bomo prenesli še na obstoječo delujočo linijo.



P 26 s žarnica - nova

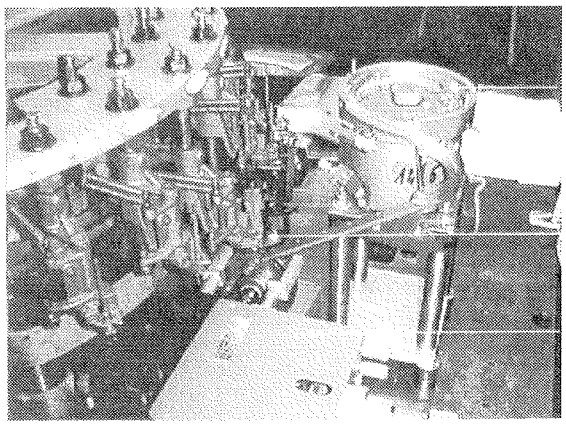


P 26 s žarnica - stara

Slika 8: Žarnice za žaromete za mopede P26 S 15 W v novi geometriji

Sledi še linija za dvonitne moped žarnice

Linija za halogenske žarnice za žaromete folij mora počakati na obnovo, ker so stroški obnove trenutno večji od naših finančnih možnosti.



Slika 9: Nov način dodajanja spiral in nove varilne glave krmili ustrezno razvita elektronika

Prenovili smo informacijski sistem, ki je sedaj zasnovan tako, da je lažje spremljati planiranje, zaloge, tržna, finančna, bilančna in proizvodna dogajanja.

Vse skupaj je rezultat lastnega slovenskega znanja. Dragih novih linij iz tujine si ne moremo privoščiti. Žal se bodo rezultati vlaganj poznali pozitivno le malo konec leta 1998, več v letu 1999 in polno v letu 2000 in naprej.

Trženje zahteva stabilno tehnologijo, homologacije proizvodov, kvaliteto, čas, zagonske stroške in dodatne napore, čeprav so nam kupci v 90 % za nove proizvode in njihovi nabavni pogoji znani.

Razvojni dosežki lahko omogočijo dolgoletno proizvodnjo novih osvojenih proizvodov, rast tržišča in soliden dobiček.

Vladimir Murko
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PREDSTAVLJAMO PODJETJE Z NASLOVNICE
REPRESENT OF COMPANY FROM FRONT PAGE

Iskra Avtoelektrika,d.d.

Šempeter pri Gorici

Iskra Avtoelektrika Šempeter se lahko pohvali s skoraj 40-letno tradicijo. Ustanovljena je bila leta 1960, ko se je začela prva proizvodnja avtoelektričnih izdelkov. Sledila so leta hitrega razvoja, ob vedno večjih potrebah domače avtomobilske industrije in ob uveljavljanju na tujih tržiščih. Hiter razvoj proizvodnje in prodaje je spremljal tudi razvoj drugih dejavnosti.

Danes je podjetje organizirano kot koncern, ki v celoti in samostojno obvladuje vse faze poslovnega procesa od razvoja in proizvodnje do trženja. Obvladujoča družba je Iskra Avtoelektrika d.d., kot odvisne družbe v koncernu pa poslujejo štiri proizvodne in šest trgovskih družb.

92-odstotni izvoz

Tradicionalnim tržiščem zahodne Evrope so se pridružila tržišča ZDA, Južne Amerike, Vzhodne Evrope, Japonske ter nekatera tržišča Bližnjega in Daljnega vzhoda. Na te trge podjetje izvozi 92% vse proizvodnje. Vrednost prodaje v minulem letu je bila 172 milijonov DEM.

Med vodilnimi svetovnimi izdelovalci

Jasno zastavljena je tudi njihova vizija - želijo namreč biti med vodilnimi svetovnimi izdelovalci motorjev, krmilnikov in električnih pogonskih sistemov za mobilno hidravliko v svetu, postati drugi proizvajalec zaganjalnikov in alternatorjev za gospodarska vozila v Evropi ter proizvajalec izbranih tehnologij: plastični deli, hladno oblikovani jekleni deli, aluminjasti odlitki, orodjarstvo in posebna oprema. Poglavitna cilja pa sta dolgoročni razvoj koncerna in večja donosnost kapitala.

Izdelki - plod lastnega razvoja podjetja

Večina izdelkov Iskre Avtoelektrike je plod lastnega razvojnega dela kot na primer novi pogonski sistemi, ki vključujejo tehnologijo brezkontaktnih trifazno elektronsko komutiranih motorjev. Krmilnik motorja vsebuje mikroprocesor, ki skupaj z možnostjo spreminjanja parametrov za nadzor motorja naredi nove sisteme uporabne povsod tam, kjer se zahteva nadzorovan pomik ali nadzorovano gibanje. Tako so sistemi najprimernejši za pogon baterijsko napajanih vozil, kot so viličarji, čistilni stroji, električni skuterji in invalidski vozički. V primerjavi s klasičnimi pogonskimi sistemi, ki so vključevali običajne kolektorske motorje, so največje prednosti novega sistema predvsem dolga življenjska doba brez vzdrževanja, večji izkoristek, ki povečuje avtonomijo delovanja za 20%, tišje delovanje in možnosti vračanja energije ob zaviranju, saj motor deluje kot generator. Za konkretne aplikacije imajo v Iskri Avtoelektriki razvitih več družin motorjev premerov od 78 mm do 132 mm in moči 300 W do 3000 W.

Krmilniki so prilagojeni posameznim močem motorjev s primernim številom sodobnih močnostnih tranzistorjev v tehnologiji mosfet, medtem ko je procesorski del vezja z ustreznim softwareom enoten za vse sisteme.

Več kot tisoč tipov izdelkov

Sicer pa sestavlja program Iskre Avtoelektrike več kot tisoč tipov izdelkov v 24 družinah. Posebno vlogo v programih pa imajo izdelki z najsodobnejšimi tehnološkimi rešitvami, kot so zaganjalniki z reduktorjem, alternatorji z notranjim ventilatorjem in brezkontaktni elektromotorni pogoni.

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POROČILA - REPORTS

XXII IMAPS - POLAND CHAPTER CONFERENCE AND EXHIBITION
Zakopane, October 1 - 3, 1998

V dneh od 1. do 3. oktobra je bila v Zakopanih na Poljskem 22. konferenca poljske podružnice združenja IMAPS (International Microelectronics And Packaging Society). Na konferenci je bilo približno 140 udeležencev iz devetih držav. Manj kot 20% udeležencev je bilo iz industrije. Konferenco je organiziral "Institute za razvoj hibridne mikroelektronike in uporov" iz Krakova. Na konferenci je bilo ustno predstavljenih 14 vabljenih referatov in 84 prispevkov predstavljenih s posterji. Iz Slovenije smo bili štirje udeleženci konference. Predstavili smo tri dela s posterji in za "Long term stability of pressure transducers" dobili prvo nagrado. Slovenski udeleženci smo imeli na konferenci sledeče tri posterje:

- D. Ročak, K. Bukat, J. Fajfar-Plut; "Investigation of new no-clean fluxes"
- D. Belavič, M. Hrovat, D. Ročak; "Investigation of the novel thick film resistor series"
- S. Šoba, D. Belavič, M. Pavlin, I. Lahne; "Long term stability of pressure transducers"

V poročilu je kratek opis nekaterih prispevkov. Povzetki vseh prispevkov, tako ustni kot posterjev so objavljeni v zborniku abstraktov, ki je na razpolago v HIPOT, Šentjernej in na Institutu Jožef Stefan, Ljubljana. Zbornik referatov pa bo izšel naslednje leto v času konference.

Paul Collander iz Nokie, Helsinki je v referatu "Tehnologije za obstoječe in prihodnje mobilne telefone" opisal tri pomembne tehnologije, katere se uporabljajo za izdelavo mobilnih telefonov. To so CSP (chip scale packaging), MCM (multichip modules) in integracija pasivnih elementov. Za CSP je značilna nadaljevanje usmeritve zmanjševanja dimenzij in s tem v zvezi problem bondiranja. Od MCM tehnologij se uporablja samo MCM-L, kot najcenejša in MCM-D, ki omogoča največjo stopnjo integracije. Predavatelj je posebej izpostavil tudi problem miniaturizacije pasivnih elementov. Medtem ko je miniaturizacija aktivnih elementov v elektroniki dosegla zavidljive rezultate se vse bolj postavlja vprašanje, kako zmanjšati dimenzije pasivnim elementom, in jih integrirati v elektronsko vezje.

Tadeusz Pisarkiewicz iz Univerze v Krakovu je v referatu "Pametni senzor ozona" opisal delovanje inteligentnega senzorja za ozon. Za procesiranje senzorskega signala je razvil "fuzzy" elektroniko. Na ta način je obvladal neželen vpliv spremembe temperature in vlage okolice na selektivnost in občutljivost senzorja.

Pavel Mach iz Tehnične univerze v Pragi je predstavil, kako z meritvami šuma in nelinearnosti določiti kvaliteto debeloplastnih uporov. Proučevali so vpliv oblike uporov na šum in nelinearnost uporov. Analizirali so tudi vpliv laserskega doravnavanja na kvaliteto uporov. Na tankoplastnih superprevodnikih so z meritvami šuma in nelinearnosti proučeval prehod iz normalnega v superprevodno stanje. Ugotovili so, da na prehod največ vpliva nelinearnost stika. Meritve šuma in nelinearnosti so uporabili tudi za raziskave kvalitete povezave električne komponente s pomočjo električno prevodnega lepila. Polimerna lepila povzročajo povišanje šuma in nelinearnosti elektronskih komponent zaradi nehomogenosti materiala.

Heiko Thurst iz Tehnične univerze v Ilmenau je v svojem referatu "Vpliv tehnologije na lastnosti pokopanih debeloplastnih uporov pri "green tape" večplastnem vezju" opisal postopek izdelave debeloplastnih uporov med dvema plastema zelene keramične folije (green tape). Debeloplastni upori so žgani skupaj s keramičnimi folijami. Upori, žgani skupaj z zeleno folijo, morajo imeti podobne linearne koeficiente raztezka in morajo biti kompatibilni z materialom folije. Steklo v uporovnih materialih reagira s steklom v foliji, kar prinaša spremembo razmerja med steklenim in prevodnim delom debeloplastnih uporov, ter s tem spremembo upornosti in temperaturnega koeficienta (TKR) uporov. V referatu so pokazali rezultate meritve upornosti in TKR uporov po večkratnem žganju in po staranju 100 ur na 85%RV, 85°C. Opisali so tudi postopek doravnavanja pokopanih uporov z impulzi visoke napetosti.

Ian Wilckock iz Renishaw, Velika Britanija, je opisal novi model Raman spektroskopa, za širšo uporabo kot do sedaj; za rutinske analize in raziskave materialov. Ni potrebna posebna priprava vzorcev za analizo, ter s pomočjo opazovanja z belo svetlobo je možna hitra meritev s prostorsko razločljivostjo <1 μm.

Krystina Bukat iz Tele and Radio Research Institute v Varšavi je z meritvami lepljivosti natiskane pastozne spajke primerjala vplive različnih parametrov tiskanja in materialov na kvaliteto natiskane blazinice za spajkanje elektronskih komponent. Uporabili so novo metodo za meritve sile, potrebne za ločenje stika med merilno konico in natiskano spajko. Vpliv parametrov na kvalitetno blazinico za spajkanje komponent so proučevali s pomočjo Taguchieve metode preizkusov.

Andrzej Dziedzic iz Tehnične univerze, Wroclaw je prikazal rezultate meritev debeloplastnih uporov izdelanih s standardno, polimerno ali z "green tape" tehnologijo po preizkusu na visoko napetostne impulze. Rezultati kažejo, da se pri vseh uporih upornost zmanjšuje, sprememba upornosti je pa odvisna od upornosti uporov, geometrije in karakteristike impulza. V drugem posterju je nadaljeval z meritvami debeloplastnih uporov, narejenih na in pod površino zelene folije v odvisnosti od temperaturnega območja (-180 do 130 °C).

Torsten Kirchner iz Tehnične univerze v Ilmenau je uporabil nov postopek za izdelavo prevodnikov za visoke gostote električnega toka pri nekaterih elektronskih vezij. Ta nov postopek vsebuje lasersko izdelavo vdolbine v "green tape" substratu in s posebnim postopkom tiskanje debeloplastne prevodne paste v vdolbino.

Ryszard Kisiel iz tehnične univerze v Varšavi je z meritvami omočljivosti kovinskih substratov s spajko primerjal pastozne spajke, katere ne vsebujejo svinca (SnZn, SnAgCu in SnCuBi). Pastozne spajke vsebujejo "no clean" flukse, razvite v "Tele and Radio Research Institute". Vpliv parametrov spajkanja, tip substrata, vrsta fluksa, temperatura spajkanja, staranja površine substrata, so proučevali s pomočjo Taguchieve metode preizkusov.

Roland Reicher, Tehnična univerza na Dunaju, je s sodelavci razvil novo prevodno debeloplastno pasto na osnovi TiCuAg za tiskanje na AlN substrat. Prevodna pasta vsebuje steklo, ki ne reagira z AlN substratom. Po tiskanju, sušenju in žganju prevodne blazinice so dobili zadovoljivo adhezijo na substrat. Z numerično analizo temperaturne in mehanske razporeditve stika AlN substrata z natiskanim prevodnikom so primerjali novi material s standardnim debeloplastnim prevodnikom.

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Deutsche ISHM-Konferenze 1998
München, 12./13.10.1998

V dneh 12. in 13. oktobra 1998 je bila v Münchnu v Nemčiji jubilejna 25. nemška konferenca za hibridno tehnologijo (ISHM-D´98). Med letošnjo konferenco se je tudi nemška podružnica združenja IMAPS (International Microelectronics And Packaging Society) preimenovala iz ISHM v IMAPS. Na konferenci, ki jo je vodil prof. Osterwinter, je bilo predstavljenih petnajst referatov. Na konferenci je bilo registriranih 132 udeležencev iz štirih držav. Več kot 80% udeležencev je bilo iz industrije. Zbornik referatov je izdan samo na CD-ROMu in je na razpolago v HIPOT, Šentjernej oz. na Institutu Jožef Stefan, Ljubljana. V poročilu je kratek opis referatov po posameznih področij.

Nekaj referatov je obravnavalo trg in tehnološke trende za hibridno mikroelektroniko. Svetovni trg hibridnih vezij je bil leta 1997 vrednostno 11,6 milijard DEM. Od tega je bil delež NAFTA 5 milijard DEM, Azija 4,6 milijard DEM in Europa 2 milijardi DEM. Največji svetovni proizvajalci po velikosti so Sanyo (J), Hitachi (J), Mitsubishi (J), Sanken (J), Rohm (J), NEC (J), Fujitsu (J), Bosch (D), Philips (D), Teledyne (USA), Siemens (D). Prognoza za leto 1998 je vrednostno 12,4 miljard DEM. Tehnološki trendi za hibridno mikroelektroniko so usmerjeni predvsem na področja multičip modulov, hibridnih vezij večjih gostot, hibridnih vezij za višje frekvence, močnostnih modulov, senzorike ter mikrosistemske tehnike in mehatronike. Najbolj verjetna področja aplikacij so avtomobilska elektronika (kontrola motorja, "airbag", ABS, različni senzorji in aktuatorji, itd.), telekomunikacije (VF aplikacije, PON in GPS sistemi, itd.), medicinska elektronika (srčni vzpodbujevalci, implantati, endoskopija, itd.) ter letalska in vesoljska elektronika (senzorski sistemi, radarji, sonarji, itd.).

Referati na področju tehnologije so bili usmerjeni na področja, ki imajo največje tehnološke trende.

Predstavljene so bile raziskave submikronskih prahov žlahtnih kovin za debeloplastne prevodnike. Te kovine so Ag, Pd, Au in Pt. Uporaba submikronskih prahov za izdelavo debeloplastnih past omogoča tiskanje manjših dimenzij, boljšo resolucijo tiskanja, manjša debelina plasti, manjša poraba materiala, itd.

Na področju močnostnih modulov je bila predstavljena raziskava različnih AlN keramičnih materialov namenjenih za substrate ter obnašanje uporovne in Ag/Pd prevodne plasti na takem substratu. Predstavljen je bil tudi postopek predukrivljanja keramičnega substrata (alumine) pri izdelavi DCB močnostnih vezij.

Kot nova tehnologija sta bila prikazana dva principa izdelave elektroluminiscenčne svetlobne celice z debeloplastnimi materiali, ki so jih preskušali in na osnovi njih izdelali nekaj aplikacij. Prvi princip je izdelava na prozornem substratu, kjer celica sveti skozi substrat. Pri drugem principu pa je fosforjeva pasta prekrita s transparentnim prevodnikom in celica sveti navzgor.

Na področju multičip modulov so predstavili LTCC (Low Temperature Cofired Ceramics) tehnologijo in možne aplikacije na področju mikroelektronike, mikromehanike, mikrooptike, mikrosenzorike, mikrofluidike in mikroaktuatorjev.

Na področju pritrjevanja in povezovanja elektronskih komponent so bile predstavljene tehnologije keramične CSP (Chip Scale Package) za miniaturne aplikacije; BGA (Ball-Grid-Array) ohišja in postopke so testirali za uporabo v avtomobilski elektroniki; nov postopek "reflow" spajkanja v parni fazi, ki omogoča zanesljivo obvladovanje spajkalnega procesa in istočasno zmanjšuje možnosti napak na visoko-kompleksnih vezjih; uporabo mikro-elektronskih vezij v različnih plastičnih karticah in papirjih (bankovci, vrednostni papirji, identifikacija predmetov, identifikacija oseb, elektronske plombe, itd); pritrjevanje z epoksidnim sistemom, ki ima podobne lastnosti kot spajka.

Na področju zanesljivosti je bilo prikazano vrednotenje zanesljivosti mikroelektronskih konstrukcij z uporabo matematičnega modeliranja na osnovi končnih elementov. Z omenjenim računalniškim orodjem simulirajo temperaturne in/ali mehanske razmere v gradnikih hibridnega modula. Ti podatki v korelaciji z modelom odpovedi, ki temeljijo na relevantnih mehanizmih odpovedi, rezultirajo v napovedani življenjski dobi izdelka oziroma stopnji zanesljivosti. Na področju senzorike, elektronike in mikro-sistemov se velikokrat uporabljajo plastična ohišja, ki morajo zdržati v agresivnih okoljih. Zato je pomembno tudi preskušanje pronicanja vlage v plastično ohišje, ki ga je avtor izvedel na osnovi standarda MIL-STD-883D.

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NOVICE - NEWS

AMS News

Explanatory comments on the development of business and operating results

GROUP

In the first nine months of 1998, the sales revenues of the group dropped slightly by 0.9% to 1,208.5 MATS (last year: 1,219.1 MATS). Thus the development of the group was better than that of the world-wide market in this industry that suffered a drop of 5%, but worse than the relevant market in Europe which enjoyed a slight growth rate of 4% during this period. The development of the Industrial and Automotive market segments was above average with sales revenues being 13.1 % and 9.9% higher than last year. The Communications segment showed a poorer performance compared to last year both in absolute (-12.3%) and relative figures (the proportion of the overall turnover dropped from 36% to 31 %). The market segments contributed the following percentages to the overall sales of the Group (comparative period 1997): Automotive 18% (17%), Communications 31% (36%), Industrial 31% (28%), Semiconductors 9% (11%), Consumer Electronics 1 % (2%), Others 10% (6%). Sales revenues by geographical areas: Europe 78% (74%), Asia 8% (8%), Americas 14% (18%).

The number of incoming orders received by the Group dropped by 7.8% to 1,204.7 MATS in the reporting period (last year: 1,307.3 MATS). Incoming orders in the third quarter, 370.8 MATS, were below the number of the second quarter (404.4 MATS). The main reason is above all the lacking replacement of discontinued products by new projects ready for volume production.

The result development of the Group in the first three quarters was not to our satisfaction. Stagnating sales revenues were confronted with considerably higher expenditures for external services and subcontracting as well as costs connected with the strategic project of the Group. In addition, increasing costs for the development of standard products and new processes, as well as research and development expenditure in this context, meant a further burden on the result. The result of ordinary business was at a -104.1 MATS in the reporting period and thus considerably below last year's level (-18.3 MATS). The group result was -45.9 MATS (13.5 MATS last year).

A positive development was the number of project starts which will be the basis for further sales and proceeds development. Compared to last year, the number of new projects increased by 13% and at the same time project sales rose by 10% compared to last year.

The Group's equity was 1,820.1 MATS as per 30.9.1998. This corresponds to an equity ratio of 60.9%, which means that Austria Mikro Systeme Group has a sound basis of capital resources. The group has no net debts as per the reporting date, the gearing being -0.4%.

AUSTRIA MIKRO SYSTEME

Due to the unsatisfying developments of incoming orders in the third quarter, it was not possible to maintain the positive development of the first six months of this year (+7.2%). The sales revenues rose by only 1.1 % to 916.6 MATS in the first three months of this year (same period last year: 910.0), which means that the increase in expenditures mentioned above are fully reflected in the development of the result. In addition to this, the continued price pressure on the single chip telephone circuit reduced the achieved gross profit margin. Markedly higher license expenditures mean a further burden on the result situation. A positive result factor stems from the financial result which increased by approx. 6 MATS thanks to income from investment in shares of subsidiaries and associated companies. The profit from ordinary activities fell to 19.8 MATS (last year: 96.1 MATS).

THESYS

The overall result development in the reporting period at THESYS was not satisfactory, either. The main reason for the continued negative development of the company's result is the unchanged low utilisation of the production line.

The 3.4% higher sales revenues were not sufficient to compensate for increased expenditures for subcontracting and other external services.

OUTLOOK FOR THE FULL YEAR

The unsatisfying development of incoming orders in the 3rd quarter is going to continue in the next few months. From today's point of view, a decline can be expected for the remaining months of 1998. Hand in hand with this development, we are expecting to see a reduction of sales revenues in 1998 by 5% compared to last year. The group result will be significantly below last year's due to the burdening factors described above, and due to the expected development of proceeds in view of the reduced number of incoming orders. In order to improve this difficult situation, a far-reaching cost saving and optimising programme has been implemented for quite some time now. This will have positive effects on the result development in the current quarter, but from today's point of view, we are still expecting a negative group result of -80 Mill. ATS for 1998.

Strategic Reorientation

The ability to offer sound manufacturing methods in the mixed signal field which allowed major growth in the first half of the nineties is no longer decisive in international competition. It has become a prerequisite. Those semiconductor companies which create products out of ideas in close cooperation with their customers will be the only successful ones in future. Therefore Austria Mikro Systeme Group is going to focus entirely on the market and its customers in future. These reflections form the basis for the strategic business units (SBU´s) which will be independently controlling the business development in the Automotive, Communications, Customer Own Tooling (COT) and Industrial field. This concentration of resources ensures optimised implementation on the market.

A few years ago, Austria Mikro Systeme was still a relatively small company. Strong growth and company acquisitions have turned it into a group of companies. This development calls for a new way of thinking with regard to organisational procedures. In order to be successful in future, too, the Group will be managed as one unit and clear rules, responsibilities and competencies will be defined in order to profit from the advantage of size.

Focusing on the market and its customers as well as creating clear-cut areas of responsibilities and competencies are the primary goals of the new organisation.

Many colleagues have contributed their share to the strategic project and the re-organisation and we would like to take this opportunity to thank them for their tremendous efforts. The wide support of staff ensures fast and efficient implementation.

Research and Development

We have concluded a license agreement with a North American technology company for the joint development of the siliciumgermanium BiCMOS technology. This technology has triggered extensive research and development activities all over the world and is used for high frequency applications in the telecommunications and automobile industry. Austria Mikro Systeme aims at becoming one of the first commercial suppliers of silicium-germanium layer structures for the integration of high speed bipolar transistors in the traditional CMOS technology.

The development work for the analogue capable 0.35 micrometer CMOS technology has been continued according to schedule. The 0.35 micrometer CMOS-technology is offered within the multi-product-wafer train schedule 1999.

The harmonisation of the technological bases of Thesys and Austria Mikro Systeme has been further strengthened through the release of the analog/digital 0.6 CMOS technology. First customer projects have already been successfully launched in Erfurt.

Several expertises established on the projects organised in the framework of the strategic research of the European Union, ESPRIT (joint research projects of leading European semiconductor companies) showed positive results so that these projects can be further pursued according to plan.

PRESS REELEASE: Austria Mikro Systeme International AG: Dipl. Ing. Dr. Wolfgang Pribyl becomes technical manager of the group

The Board of Management of Austria Mikro Systeme International AG is to be enlarged. As of 1 January 1999, Dipl. Ing. Dr. Wolfgang Pribyl - formerly in an executive position at Siemens - will become technical manager of the Austria Mikro Systeme group to back up the top management under Hans Jörg Kaltenbrunner. The competence and responsibility of the internationally renowned semiconductor specialist will include design and process development, research and the production process comprising manufacturing, assembly and testing.

The 45-year-old Styrian was formerly sole manager of Siemens Entwicklungszentrum für Mikroelektronik, responsible for the locations in Villach and Graz, and focused on the development of integrated circuits for the telecommunications, automobile and industrial electronics industries. The experienced specialist gained international expertise at Silicon Valley and as a top manager at the Siemens group. Dr. Pribyl is on numerous international research and project committees. The little spare time he has is devoted to his wife and two children. He is an ardent amateur photographer and has been fascinated by Tai Chi for several years.

The prime aim of the new member of the board is a cross-group clustering of existing technical expertise and an orientation of pure research to future customer requirements. "I see my new task as a challenge to push ahead the vast technical strenghts of the group in the field of customer specific circuits and to consolidate the group's position as one of the leading European manufacturers of semiconductors in the mixed analog/digital sector. The aim is to implement our excellent technical know-how in market-oriented development of standard products (ASSPs) to an even greater extent", Dr. Wolfgang Pribyl emphasises.

Mag. Hans Jörg Kaltenbrunner, Chairman of the Board, "We are very pleased to have won such an experienced specialist for our company. Thanks to our orientation to the market and customer wishes and the decisive technical edge the appointment of Dr. Pribyl will give to the group, Austria Mikro Systeme will continue on its course of growth".

Austria Mikro Systeme Group announces its 1999 MPW-Wafer Train with 3 new Process Technologies

The multi-product-wafer train schedule for 1999 enables cheap prototyping service due to shared costs for masks and wafers. The customer delivers GDSII at fixed dates (TAPE-IN) and receives untested packaged samples within a lead time of typically 7 weeks for CMOS processes and 10 weeks for BiCMOS processes.

In addition to the proven 0.6 µm, 0.8 µm and 2.0 µm CMOS and 0.8 µm BiCMOS technologies the Austria Mikro Systeme group is offering for the first time 0.35 µm CMOS, 0.6 µm BiCMOS and 0.8 µm HBT-CMOS (SiGe) technologies within this MPW service.

Process	DATA TO:	Wafer size	Tape in	Preliminary** Samples out
2.0 µm CMOS High Voltage				
CBT/CBY/CBZ	UPS	4"	22.01.99	12.03.99
CBT/CBY/CBZ	UPS	4"	09.04.99	28.05.99
CBT/CBY/CBZ	UPS	4"	09.07.99	27.08.99
0.8 µm 5V CMOS				
CYE	UPS	4"	26.02.99	16.04.99
CYE	UPS	4"	21.05.99	09.07.99
CYE	UPS	4"	27.08.99	15.10.99
CXQ/CX08AI	UPS	6"	26.02.99	13.04.99
CXQ/CX08AI	ERF	6"	26.03.99	11.05.99
CXQ/CX08AI	UPS	6"	21.05.99	06.07.99
CXQ/CX08AI	ERF	6"	02.07.98	17.08.99
CXQ/CX08AI	UPS	6"	27.08.99	12.10.99
CXQ/CX08AI	UPS	6"	22.10.99	07.12.99
CXQ/CX08AI	ERF	6"	10.12.99	25.01.00
0.8 µm CMOS High Voltage				
CXZ/CX08HI	UPS	6"	05.02.99	02.04.99
CXZ/CX08HI	ERF	6"	19.03.99	14.05.99
CXZ/CX08HI	UPS	6"	07.05.99	02.07.99
CXZ/CX08HI	UPS	6"	06.08.99	01.10.99
CXZ/CX08HI	ERF	6"	17.09.99	12.11.99
CXZ/CX08HI	UPS	6"	05.11.99	07.01.00
0.8 µm CMOS HV/EEPROM				
CX08EA/CX08NA	ERF	6"	12.03.99	
CX08EA/CX08NA	ERF	6"	18.06.99	
CX08EA/CX08NA	ERF	6"	24.09.99	
CX08EA/CX08NA	ERF	6"	26.11.99	
0.6 µm CMOS				
CUP/CX06AT	UPS	6"	29.01.99	26.03.99
CUP/CX06AT	UPS	6"	19.03.99	14.05.99
CUP/CX06AT	UPS	6"	28.05.99	23.07.99
CUP/CX06AT	UPS	6"	30.07.99	24.09.99
CUP/CX06AT	UPS	6"	01.10.99	26.11.99
CUP/CX06AT	ERF	6"	03.12.99	28.01.00
0.35 µm CMOS				
CSD	UPS	8"	15.01.99	
CSD	UPS	8"	30.04.99	
CSD	UPS	8"	13.08.99	
CSD	UPS	8"	12.11.99	
0.8 µm BiCMOS				
BYE/BYQ	UPS	4"	19.02.99	30.04.99
BYE/BYQ	UPS	4"	16.04.99	25.06.99
BYE/BYQ	UPS	4"	16.07.99	24.09.99
BYE/BYQ	UPS	4"	24.09.99	03.12.99
BYE/BYQ	UPS	4"	10.12.99	18.02.00
0.8 µm SiGe				
BYS*	UPS	4"	16.07.99	
BYS*	UPS	4"	10.12.99	
0.6 µm BiCMOS				
BX06AD	ERF	6"	18.06.99	27.08.99
BX06AD	ERF	6"	10.09.99	19.11.99
BX06AD	ERF	6"	03.12.99	11.02.00

* Preliminary! Confirmation in Q1/99 through update in Internet.

** Sample out date will be definitely fixed in January 99.

Possible changes or additional process variants will be published through the Internet.

The 0.35 μm CMOS process is realised on 8" and provides 3 layers of metal and 2 layers of polysilicon which are used as linear capacitors and resistors for mixed-signal applications. Digital standard cell libraries for the core running at 3.3 V and periphery cells for 3.3 V or 5.0 V are available for all major CAE platforms. Very fast static RAMs can be ordered; compilers for dual-port RAMs and ROMs are in preparation. First qualified analog cells and macros (8bit,10bit ADC and DAC) are available within the analog design kit.

The 0.6 μm BiCMOS process is a scaled version of the proven 0.8 μm BiCMOS process offering high density design rules and a 3rd layer of metallisation. The main advantage of this process is the integration of high speed analog circuits together with complex digital functions on one single device.

The 0.8 μm Silicon-Germanium heterojunction-bipolar-transistor process (HBTCMOS) is a new development offering highest speed (ft > 35GHz) npn-transistors in combination with a proven 0.8 μm mixed-signal CMOS process. Design rules, process parameters with first simulation models for the npn-transistors and digital CMOS libraries are available for this new technology.

DSP Technology at Austria Mikro Systeme

Thanks to the compilation of an assembler software library, Austria Mikro Systeme now has a sophisticated DSP (Digital Signal Processor) technology for a wide range of applications at its disposal.

DSP technology is based on the GEPARD signal processor family developed at Austria Mikro Systeme. The parameterizable GEPARD architecture makes short-term provision of DSP cores possible which can be perfectly adjusted to individual applications. The development of circuits is supported by suitable simulation models for the Austria Mikro Systeme HIT kit (High Performance Interface Tool Kit) available for CAD tools from Mentor Graphics, Cadence Design Systems and Synopsys. A suitable assembler, a code simulator as well as a comprehensive, handoptimised assembler software library are available for programming of the GEPARD DSP cores.

DSP technology takes the progressive digitalisation of mixed signal applications into account. Austria Mikro Systeme has for several years been setting milestones in digital signal processing in the development and production of mixed analogue-digital circuits. In addition to GEPARD DSP cores, highly-optimised, hard-wired signal processor modules, such as digital filters, FFT and DCT modules, are applied. High performance A/D and D/A converters as well as tested analogue modules complement the product range of Austria Mikro Systeme. Application areas include coder-decoders, modems, circuits for audio and speech processing, as well as measuring and sensor signal analysis. The circuits are produced in submicron-CMOS technologies, and the transfer to subhalfmicron-CMOS technologies is currently being prepared.

The GEPARD DSP core technology was presented at the leading European Conference in this line of industry, the "Design, Automation and Test in Europe Conference 1998" (D.A.T.E. '98), and awarded the "Best ASIC Prize".

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IMEC News

OCAPI, a new IC design environment

This design environment tries to bring the circuit designer closer to the system designer and increase the design productivity of complex signal processing systems. A DECT transceiver ASIC was designed using OCAPI.

OCAPI is based on object-oriented C++ and advanced synthesis methods that enable integrated systems design, simulation and synthesis of advanced signal processing. The system specification is automatically transferred from C++ to VHDL or a compilable C++ code. OCAPI also enables to refine the design gradually. The object-oriented methodology offers a solution to the re-use of previously designed building blocks. OCAPI offers a number of benefits, such as mixed-mode design evaluation, state-of-the-art synthesis script, elaborated verification strategy, object-oriented modeling for hardware (resulting in faster design of new functions) and the single C++ design environment from the highest untimed level to the bit-true, clock cycle true level. This completely new design environment was applied for the design of a DECT transceiver ASIC which will significantly improve the signal quality between base station and mobile system. The chip processes DECT burst signals, received through a radio frequency front-end RF. These signals are equalized to remove the multi-path distortions introduced in the radio link. The chip has a 194 mm^2 die area in 0.7 μm CMOS technology.

New IMEC Industrial Affiliation Programs (IIAP) in telecommunications

High-speed wireless local area networks

The objective of this program is to achieve an overall network capacity up to high bitrates. For this purpose, accurate design of all parts of the system, from high level networking down to the hardware implementation of the functional blocks, is required. At the moment, a prototype OFDM (orthogonal frequency division multiplexing) modem ASIC is under development and a

demonstration setup based on the WLAN modem chip will be realized by end 1998. Target customers are system houses and microelectronics companies with an interest in WLAN or indoor communication.

Multimedia image compression

A first-of-a-kind MPEG-4 architecture will be developed, optimized for high performance and low power. In addition to the system-on-chip MPEG-4 architecture, tools supporting the design flow of this family of applications will be developed. Target customers for this program are system houses and multimedia component providers that want to extend their existing expertise with MPEG4 specific implementation knowledge.

IMEC cooperates with industry to enhance ASIC and system design skills

A program is being set up to increase the number of trained engineers, and to transfer state-of-the-art research experience in the development of embedded systems towards design groups from industry. This initiative tries to give an answer to a number of problems, such as the booming complexity of ICs, the rapid changes in design methodology for complex systems and the important shortage in the market of skilled engineers. The training program consists of 3 classes of training courses:

- Use of standard EDA tools, currently available in the market (e.g. VHDL, synthesis, test-pattern generation, DSP systems...)
- Concepts for the development of complex embedded systems, such as hardware/software codesign, C++ based hardware design and real-time operating systems.
- Custom courses

All regular courses are being announced on the website: www.imec.be/training/Welcome.html
or Bart De Mey, Tel. +32 16 28 12 49
Fax +32 16 28 15 84

Postacademic Interuniversity Course in Telecommunications

Nearly 500 students enrolled in this *videoconference* course.

The initiative, started in September last year, is an excellent example of cooperation between Flemish universities, polytechnical schools and industry The program is spread over two years and intended for renewing and upgrading the knowledge of engineers working in industry The course can be followed simultaneously through videoconferencing at 7 places in Flanders and some sites in the rest of Europe. In the beginning of 1998, IMEC's infrastructure was expanded to enable other organizations with videoconferencing capabilities to participate as a site.

For more information, please contact:
Tanja Gouverneur, course coordinator
Tel. +32 16 28 13 70, Fax: +32 16 28 15 10
e-mail gouverne@imec.be
www.imec.be/seminars/itc

New semiconductor assembly foundry settles in Flanders

A new European semiconductor assembly foundry company that will be active in advanced packaging technologies has been set up. Custom Silicon Configuration Services NV (CS2) has been established through IT Partners, the private IT oriented venture capital fund. The company has chosen its location at Zaventem, near Brussels, in the vicinity of IMEC.

The new company CS2 will provide semiconductor assembly services to major European semiconductor manufacturers, and to US and Asian wafer fabrication plants with products destined for European Original Equipment Manufacturers. The nature of the business will be subcontract manufacturing with a high level of service.

Market opportunities

Today new packaging and assembly technologies are much more application specific and therefore need full flexibility, rapid cycle time and high reliability This is in contrast with older, higher volume technologies that are traditionally manufactured from a central base in the Far East. The close proximity of a subcontract packaging and assembly company will offer distinct advantages to traditional offshore operations in areas such as overall cost due to time savings and the presence of design services close to the end user.

Assembly in Europe or the USA can offer a number of benefits to the semiconductor industry. In state-of-the-art microelectronics technology, labor rates are no longer the competitive edge, but rather flexible automation and rapid cycle times. Time is money especially for custom-designed services. "The extra cost for high-end products to be assembled or packaged in the Far East, amounts to upwards of 15%", says Steve Lerner, CEO of CS2. "The total packaging and assembly cycle time can be weeks for Asian plants, with the actual manufacturing time of maybe 4-5 days, but CS2 can deliver within 72 hours (maybe even 12 hours for small lots of a few hundred), a service that can't be matched by others halfway around the world." Finally, subcontracting, or out sourcing as a part of the overall electronics industry, shows a healthy growth market as shown by the forecast in Fig. 1.

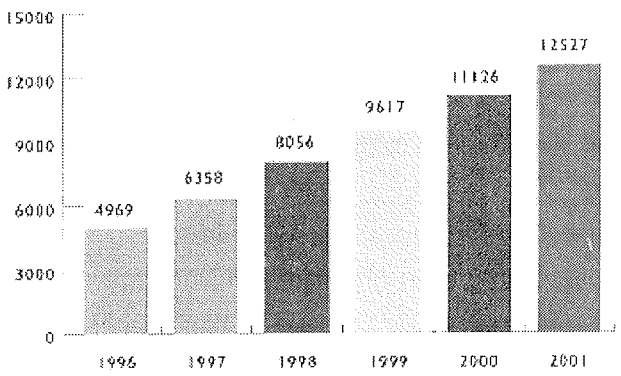

Fig. 1: Evolution of subcontracting in the electronics industry (source: Electronic trends Publication)

Technology evolution

From Fig. 2 it is clear that the following years will be characterized by a significant growth in array packages such as ball grid arrays (BGA) (64% per year) and chip-scale packages (CSP) (215%). In addition, flip-chip technology, where the bare die is attached to a substrate upside down after the attachment of solder bumps, will grow at a compound annual rate of 26% in the period 1996-2001.

CS2 will focus on area-array technologies, such as BGA, Flex based area arrays, CSP and multi-chip modules using both wirebonded and flip-chip interconnect technologies.

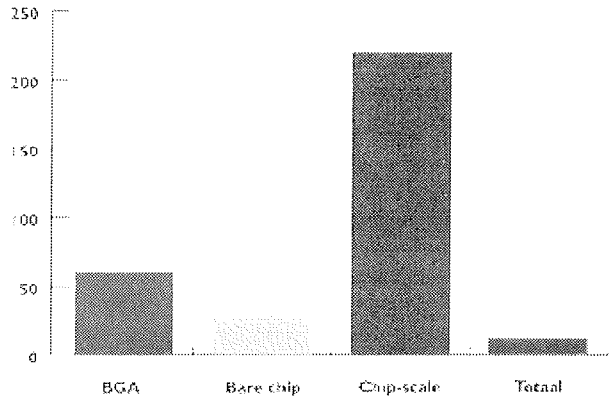

Fig. 2: Worldwide IC packaging market forecast (in units for 1996-2001 (source: Dataquest))

Custom Silicon Configuration Services

The new company will provide services to European manufacturers that include design and characterization of packages, reliability testing, assembly and selected R&D. "The strategic alliance with IMEC allows us to leverage a worldclass engineering and research organization with our extensive experience in the assembly services", Steve Lerner said. The company was established by the financial backing of IT-Partners, the private IT-oriented venture capital fund (see Newsletter 19), with approximately 10 million USD in the first round. CS2 is currently building the first module of its facility, expects packaging by the beginning of 1999 and will be operating at full capacity within one year of starting production. At that time, the company's size will be about 60 people. Subsequent expansions are planned and will be a function of market demand. The chief executive officer of CS2, Steve Lerner, is a former managing director of Amkor Anam Europe and has over 15 years of experience in the semiconductor subcontract assembly industry.

In the heart of Europe

The location of Zaventem is less than 15 miles from either Brussels or Leuven and close to the airport. In fact, the time between airport and factory is only 10 minutes! The central location in Europe renders CS2 in close proximity to major European semiconductor manufacturing plants for its potential customers (such as Alcatel Microelectronics, Philips, Siemens and SGS Thomson) and to IMEC for joint R&D work. In addition, the region of Flanders is known for its high quality of life, the multi-lingual and multi-cultural environment, the strong technical talent readily available and the progressive financial community (such as IT-Partners).

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NEW MURATA PRODUCTS

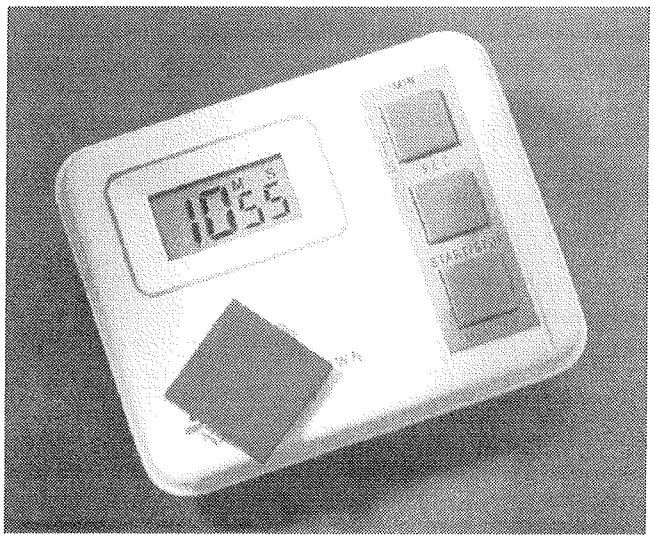
Reflow SMD sounder

This new Murata piezoelectric sounder is fully reflow compatible and can be soldered like the rest of your SMD components. Another component that you can place and forget.

The sound pressure level is 75dB minimum at 10 cm, from a 3V peak-to-peak 4kHz square wave input. Maximum input voltage is 25V p-p and electrostatic capacitance is 14nF at 1 kHz. The sounder is specified for operation over the temperature range -20 to 70°C and perfect for providing on-the-board-sound.

Today, microprocessors are used for microwave ovens, air conditioners, cars, toys, timers and many other warning tasks.

Externally driven sounders are frequently employed in digital watches, electronic calculators, telephones, and office equipment like note book computers and printers. They even appear in automotive equipment.



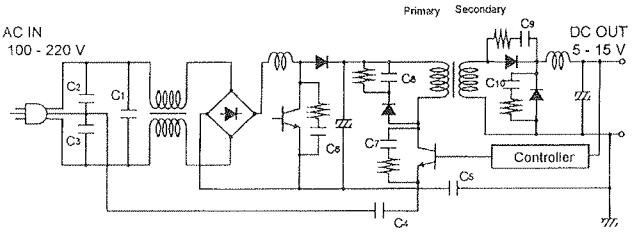
One of many applications

The Murata PKMC 16E4000-TY ideal for these functions, being compact 16 mm square with a 2.7 mm maximum height. Packaging is on trays in boxes 1,200 pieces.

SPS capacitor selection

Switched mode power supply design engineers are perfectly capable of choosing the right capacitor for their circuit; but it takes time. Here we take you straight to the right leaded or chip capacitor and save you the job of having to look them up.

For more details or special applications please contact your usual Murata service point.



	Description	Symbol No.	Series	Rated voltage	Note
Leaded disc capacitors	High voltage capacitor	C6, C7, C8, C9, C10	HR	250V-3.15kVDC	For high frequency pulse circuits
	Safety standard recognised capacitor	C1, C2, C3, C4, C5	KX	250VAC	Class X1, Y1 Test Volt. 4000VAC
			KH	250VAC	Class X1, Y2 Test volt. 2600VAC
			KY	250VAC	Class X1, Y2 Test Volt. 1500VAC
Chip capacitors	High voltage capacitor	C6, C7, C9, C10	GHM1000	630V-3.15kVDC	For high frequency pulse circuit
		C8	GHM1500	250V-630VDC	High capacitance value
	Safety standard recognised capacitor	C1	GHM3000 Type GB	250VAC	Class X2 Test volt. 1075VDC
		C2, C3, C4, C5	GHM3000 Type GC	250VAC	Class X1, Y2 Test volt. 1500VAC

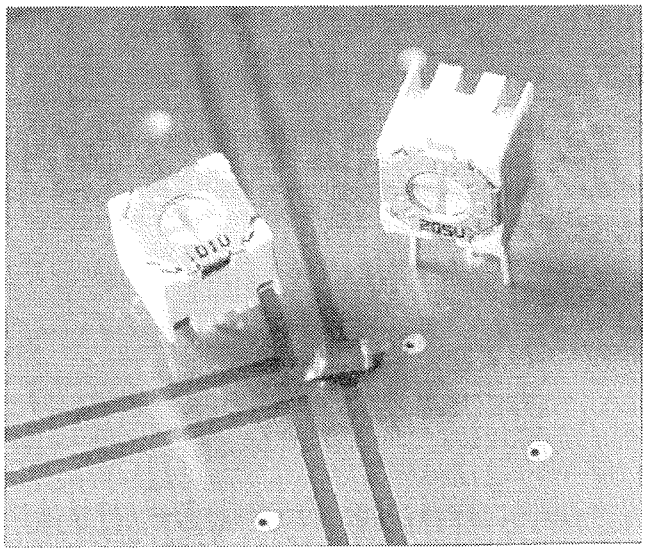
Single turn 6 mm sealed pot

This is a new, low cost family of single turn CERMET potentiometers. It provides superior adjustability with inprocess automatic and zero plus adjustment. Sealed for ultrasonic cleaning after soldering, it offers top and side adjustment with triangular and in-line terminals for bulk packaging or radial taping.

There are seven configurations. Top and side adjustment in both triangular and straight pin arrangements with two orientations of pin layout for each triangular style. Adjustment is aided by a coloured funnel shaped and enlarged rotor with cross slots. The case has an eleven point scale for position visibility.

The standard resistance range is 10 Ohms to 2 MOhms, nominal resistance tolerance is ±20% and power rating is 0.5 W at 70°C, derating to 0. W at 125°C. Maximum working voltage is 300VDC, insulation resistance is 1,000 MOhms minimum and dielectric strength is 600 VAC.

Maximum wiper current is 100 mA, contact resistance variation is 3% or 3 Ohms whichever is the greater. Residual resistance is the greater of 1.0% or 2 Ohms and the effective rotational angle is 240°±5°.

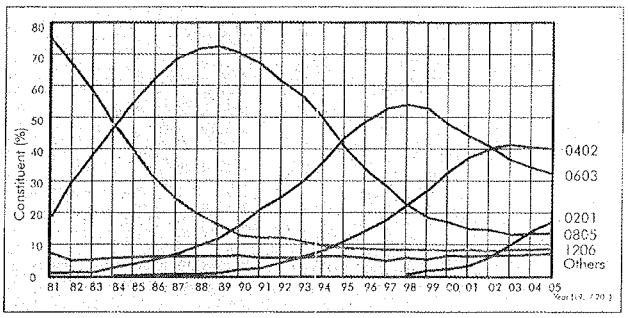


The operating temperature range is -55°C to 125°C and the temperature coefficient of resistance is ±100 ppm/°C.

The POC6ME is a very newly released product and technical literature is still being printed. Samples will be available soon and mass production starts before the end of the year. For full details of the design and range, please quote the reference number below and we will send you the information the moment it arrives from the printers.

Beat your competition

Get the competitive edge now! Multilayer ceramic chip capacitors (MLCCs) continue to get smaller and to perform even better at high frequency. Today's users of larger sizes can reduce space taken by capacitors by up to 93%. Simply by choosing the increasingly popular 0201 size (0.6 x 0.3 x 0.3mm).



The first question people ask when considering the 0201 (Murata GRM33) is "How easily can I handle and solder something that small"? It is true that designs and processes have to be appropriate and require more care than with bigger parts. However world demand for the 0402 is expected to overtake that of the 0805 this year and the 0201 is expected to replace 75% of the 0402 by 2001.

There are at least four equipment manufacturers making pick and place machines capable of placing the

0201 and at least six machines in production. Murata's experience of reflow sgoldering shows that with the right PCB design and process parts placed 50 μm off centre will self-align during reflow soldering. The fastest machines are placing components at some 40,000 pieces on hour. One of the factors making this possible is the reduced mass and thus inertia of the smaller components.

The space to be saved in small products using many capacitors is huge. A typical cellular telephone will contain some 200 to 250 ceramic capacitors. Two hundred and fifty 0402s on a 0.4 mm pitch occupy an area of ~315 mm^2. The same number of 0201s will require only ~160 mm^2 because they can be mounted on a 0.2 mm pitch. A saving of ~155 mm^2. That's a lot of real estate in a cellular telephone.

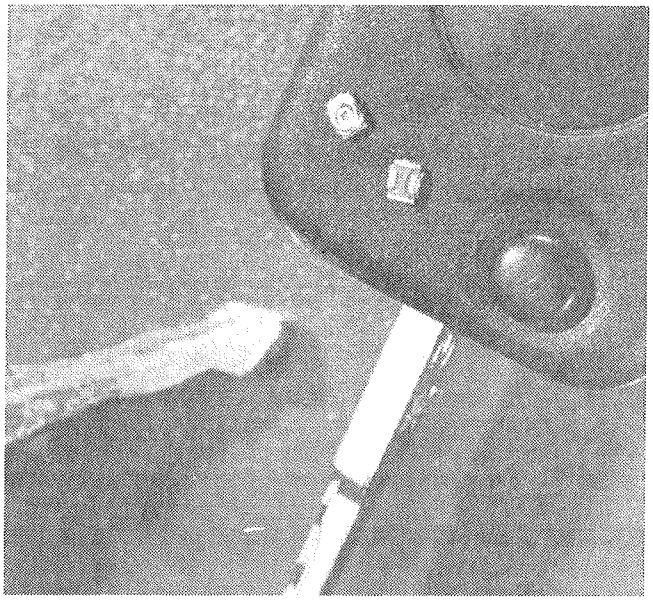
As frequencies rise capacitance values fall. At the same time operating voltages are coming down as I/C speeds increase. The result is a tendency for an increasing share of the total capacitance usage to become available in small sizes.

This trend is compounded by technology increasing the total C/ V per unit volume. Today, the 0201 has capacitance values up to 0.1 μF in three dielectrics with voltage ratings up to 25VDC. Tolerances of 5%,10% 20% and +80/-20% are available depending on the dielectric chosen. An additional benefit is the reduction of high frequency impedance with size. For example the graph shows the superior impedance of the 0201 over the 0603 because of its lower ESL. This in turn results in less signal loss or better filtering at 1.0 GHz or higher.

Don't follow, lead the field. Make use of the performance and space benefits to take a technical and commercial advantage over those competitors who move more slowly. For more information on trends and the utilisation of smaller capacitors please quote the reference number below or contact your Murata service point.

The smallest ever!

That's Murata's claim for the TZS02 family of chip trimmer capacitors at 2.2 x 2.7 x 1.0 mm high maximum.



Being small is not its only asset. The unique construction, using no plastic material provides superioi resistance to soldering heat, resulting in excellent characteristic performance after reflow soldering.

A pierced square tuning aperture allows for high resistance to tuning force and the funnel shaped cover allows for good adjustability with in-process automatic adjustment. Special metal rotors ensure high stability, minimising capacitance drift after setting.

Trimming ranges are 3.0 pF to 6.0 pF, 3.5 to 10.0 pF and 7.0 pF to 20.0 pF.

Full details can be found on www.murata.co.jp/search, on our free CD-ROM catalogue or in catalogue KO1E023.

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Informacije MIDEM
Strokovna revija za mikroelektroniko, elektronske sestavne dele in materiale

NAVODILA AVTORJEM

Informacije MIDEM je znanstveno-strokovno-društvena publikacija Strokovnega društva za mikroelektroniko, elektronske sestavne dele in materiale - MIDEM. Revija objavlja prispevke domačih in tujih avtorjev s področja mikroelektronike, elektronskih sestavnih delov in materialov, ki so lahko:

izvirni znanstveni članki, pregledni znanstveni članki, predhodne objave, strokovni članki ter predavanja in povzetki s strokovnih posvetovanj.

Strokovni prispevki bodo recenzirani.

Revija objavlja tudi aplikacijske članke, poljudne članke, novice iz stroke, vesti iz delovnih organizacij, inštitutov in fakultet, obvestila o akcijah društva MIDEM in njegovih članov ter druge prispevke.

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