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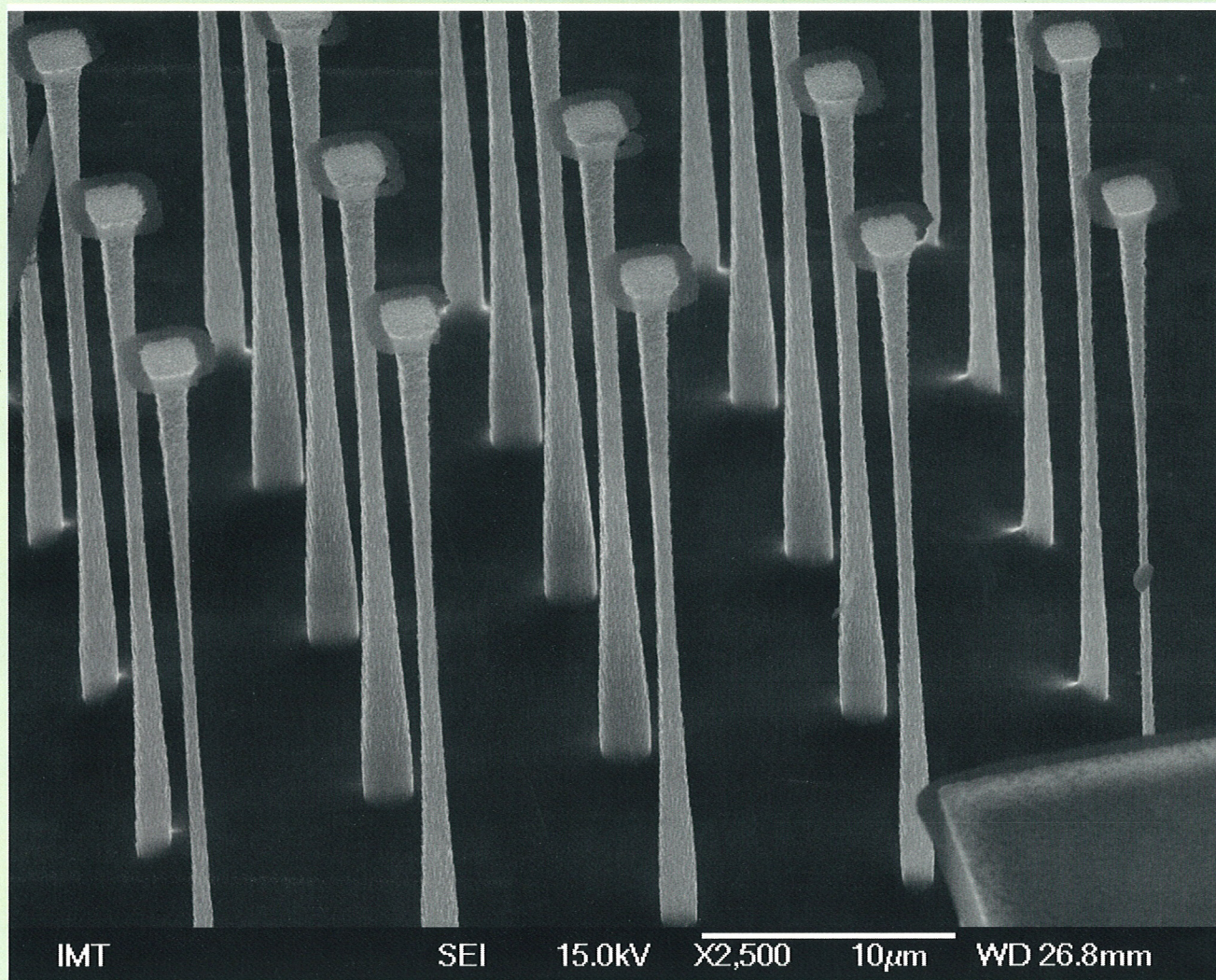
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REALIZING A LOW-COST PFC THAT HAS LOW MCU LOAD REQUIREMENTS

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Key words: Active filter, PFC, PWM modulator, microcontroller

Abstract: This article presents the design of a hybrid system for controlling switching power converters in either continuous conduction mode (CCM) or critical conduction mode. The system is particularly suitable for a Boost converter in Power Factor Correction (PFC) applications. It requires low-cost hardware and a minimum of CPU power. The proposed solution is, therefore, very convenient for use in cost-sensitive applications based on 8-bit MCUs, where the use of special integrated circuits or other complex systems remains unacceptable.

Cenovno ugodna izvedba korektorja močnostnega faktorja z minimalno obremenitvijo pripadajočega mikrokontrolerja

Ključne besede: Aktivni filter, PFC, PWM modulator, mikrokontroler

Izveček: Prispevek predstavlja zasnovano hibridnega elektronskega sklopa za vodenje močnostnih stikalnih pretvornikov v načinu netrganega toka (CCM) ali v načinu mejnega toka. Sklop je zlasti primeren za »navzgor« oz. Boost pretvornike v sistemih za korekcijo močnostnega faktorja (Power Factor Correction, PFC). Izvedba zahteva poceni in enostavno vezje ter minimalno procesorsko moč. Predlagana izvedba je zato primerna za vgradnjo v cenovno občutljive aplikacije, kjer uporaba namenskih integriranih vezij ali drugih kompleksnih rešitev ni smotrna.

1. Introduction

Power Factor Correctors (PFCs) and active filters for harmonic current reduction are becoming a necessity in most power-supply designs. In motor-control applications, for example, the use of PFCs continues to grow. A PFC satisfies the harmonic-current-reduction requirements, and at the same time ensures a sufficiently high DC link voltage to supply a power inverter. However, a PFC adds a considerable cost to an application, and without any benefit to the customer.

The consequence of this is that there is a great deal of research in an attempt to develop a low-cost, functionally optimized solution. On the one hand, there has been considerable growth in special, analog ICs, while on the other hand, many control methods based on digital circuits have been developed; this is because of their improving performance and reducing costs. Analog ICs with the required set of external components are still too expensive, while the use of an extra programmable digital circuit for the control of the PFC in a cost-sensitive application is also not reasonable.

An interesting solution is the use of a microcontroller (MCU) or a digital signal processor (DSP) that is already present in the system and is able to perform the whole, or just a part, of the PFC algorithm as a sideline. Many digital systems and methods have been developed for PFC-converter control, realized by DSP's or MCU's /1-4/, some even use FPGA technology /5/. However, due to their complex-

ity, they all require a lot of computational power and/or sampling rates, while some methods /6-7/ also require zero crossing detection and pre-calculated look-up tables. As such, algorithms are mainly too complex to run in a sideline with main application algorithms, as with induction-motor (IM) control, for example. So, particularly when using low-cost 8-bit MCUs, a different strategy is required.

The main idea is the realization of a part of the PFC algorithm, in particular the fast, inner current control loop, with a simple analog circuit, while the slower voltage control loop is still running on the MCU. A simplified block scheme of a hybrid system is shown in Figure 1.

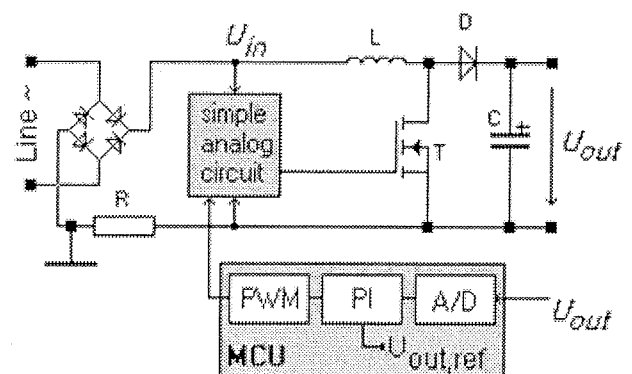


Figure 1: Hybrid Boost-PFC design

A possible solution is the use of the One (Single) Cycle Control (OCC) method, /8/, /9/, which is particularly sim-

ple and inexpensive because the multiplier and the input-voltage measurement is eliminated. A PFC realization example using the OCC control method is shown in Figure 2.

The critical point when using the OCC method in this way is the requirement that the integrator time constant and the clock period must be equal. To achieve this term, more complex circuits are required.

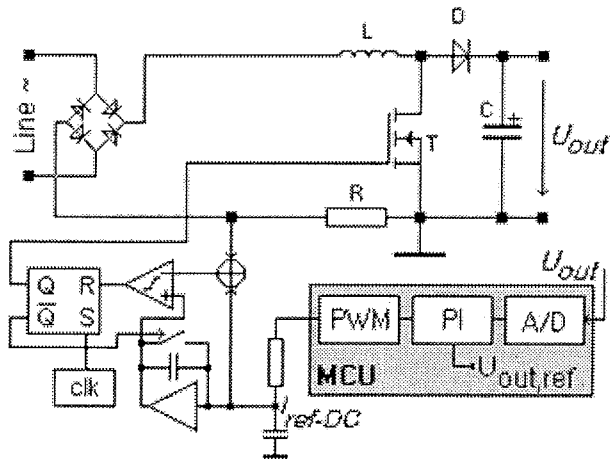


Figure 2: Hybrid Boost-PFC design using the OCC control method

Another, even simpler, solution is described in /10/, with its modification described in /7/. It is a simple and frequently used PFC controller based on a free-running hysteresis current-mode control. The realization block scheme is shown in Figure 3.

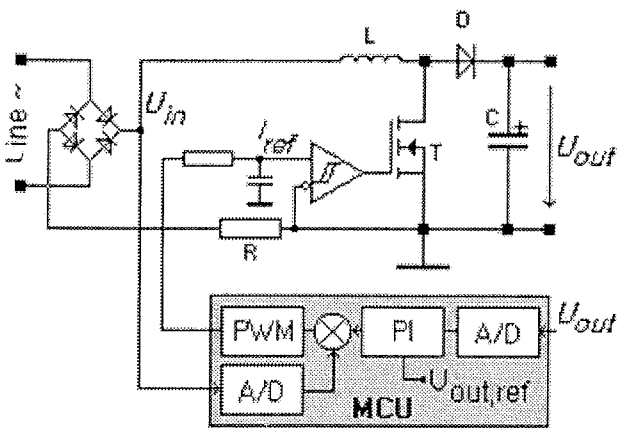


Figure 3: Boost-PFC with hysteresis current-mode control

The realization /10/ requires a lot of computational power and high sampling rates, due to the input-voltage measurement, while the second one, /7/, requires a zero crossing detection circuit and a synchronization algorithm.

This article describes an improved single-phase PFC control strategy based on a hysteresis current-mode control suitable for use with an 8-bit MCU with a minimum of free

resources available. The PFC algorithm occupies a small amount of memory and CPU time, and can therefore be executed in a sideline with the main application tasks, like motor control and lamp ballasts algorithms, while the additional analog circuit is easy to understand and implement.

In this paper only the basic PFC functionality is described, in order that we can clearly present the proposed control-method realization. The final application should include some additional functions to ensure safe and reliable operation. These functions, like soft start, over-current protection, under- and over-voltage protection etc., are not the essence of this document, and are therefore not described in detail.

The paper is organized as follows. The basic principle of operation is described in Section 2, this is followed by a practical realization example in Section 3. In Section 4 the proposed realization is verified with a simulation and experimental results. Finally, there are some conclusions in Section 5.

2. Basic operating principle

The basic idea of the proposed solution is the relocation of the input-voltage measurement circuit and the multiplier into a simple low-cost analog circuit. This is in contrast to the applications in /7/ and /10/, where these two functions are running on the MCU, resulting in considerable CPU load. The proposed realization, where both functions are combined in a single PWM modulator and an analog switch, is given in Figure 4.

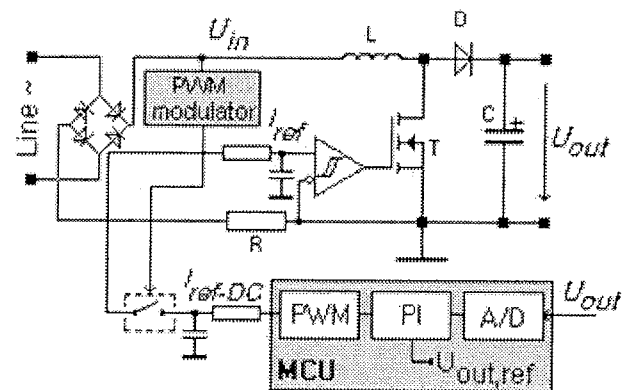


Figure 4: Proposed Boost-PFC control method

As a result, minimal CPU load is achieved as the MCU performs only the output-voltage measurement and a PI controller computation, both with a sample time equal to the line voltage period. In addition, the MCU is occupied with only one analog input, and the PWM output that is used as a D/A converter generating the DC current reference signal I_{ref-DC} . I_{ref-DC} is the voltage-control loop output value.

An analog multiplier is realized with an analog switch being driven by an input-voltage-modulated PWM signal. With this solution, the input current reference I_{ref} has the same si-

nusoidal shape as the input line voltage and an amplitude proportional to the DC current reference I_{ref-DC} .

A trailing-edge modulator (Figure 5) is used as a PWM modulator. Its operating principle is evident from Figure 6.

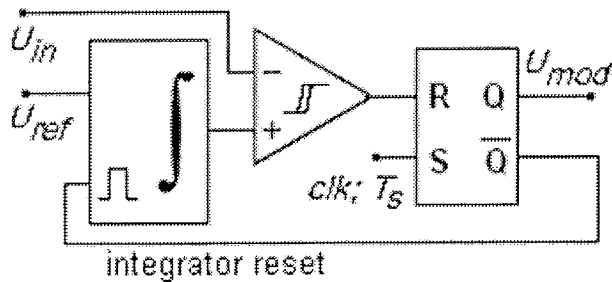


Figure 5: Basic PWM modulator block scheme

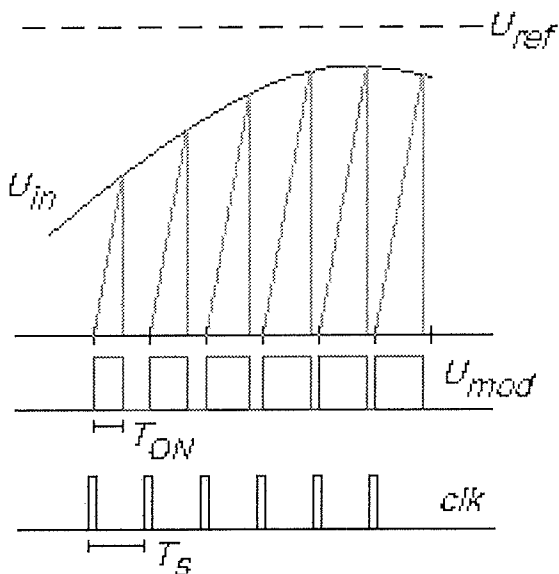


Figure 6: Operating principle of the PWM modulator

In the case that the PWM frequency is much higher than the line frequency and the integrator time constant $T_S' \approx T_S$, the modulator ON-time can be expressed as

$$T_{ON}(t) = \frac{U_{in}(t)}{U_{ref}} \times T_S$$

where $U_{in}(t)$ is the input voltage, U_{ref} is the reference voltage and T_S is the clock signal period. The PWM duty-cycle is then equal to:

$$D(t) = \frac{T_{ON}(t)}{T_S} = \frac{U_{in}(t)}{U_{ref}}$$

The average modulator output voltage is then proportional to the input voltage U_{in} and the PWM amplitude U_{mod} :

$$\overline{u_{mod}}(t) = D(t) \times U_{mod} = \frac{1}{U_{ref}} (U_{in}(t) \times U_{mod}).$$

The reference voltage U_{ref} must satisfy the equation:

$$U_{ref} \geq U_{in,max},$$

where $U_{in,max}$ is the maximum input-voltage amplitude.

By using the analog switch we ensure that the PWM signal amplitude is equal to I_{ref-DC} , representing the output-voltage controller command value. The input-current reference is then equal to:

$$\overline{I_{ref}}(t) = \frac{1}{U_{ref}} (U_{in}(t) \times I_{ref-DC}) = k \times (U_{in}(t) \times I_{ref-DC}).$$

It is obvious that the input-current reference amplitude is proportional to the voltage-controller output value (I_{ref-DC}), while the input-current shape is determined by the input line-voltage shape ($U_{in}(t)$).

The fast current controller is realized in the same way as in /10/, using a hysteresis comparator with a reference signal I_{ref} , as shown in Figure 7.

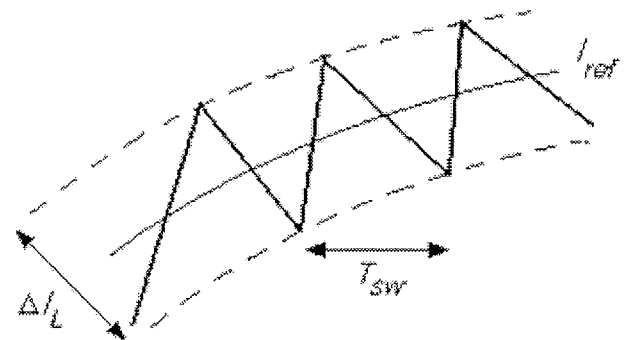


Figure 7: Hysteresis current-mode control principle

The comparator hysteresis ΔI_L directly determines the input-current ripple and the converter switching frequency, which is determined as follows:

$$f_{sw}(t) = \frac{1}{L \times \Delta I_L} \times \frac{U_{in}(t)}{U_{out}} \times (U_{out} - U_{in}(t)).$$

The equation is given assuming that the switching frequency is much higher than the line frequency.

3. Practical realization example

A simple and low-cost PWM modulator is realized employing the well-known 555 timer and an additional integrator circuit. This IC already consists of two voltage comparators, the RS-latch and the discharge transistor. The proposed PWM modulator scheme is shown in Figure 8.

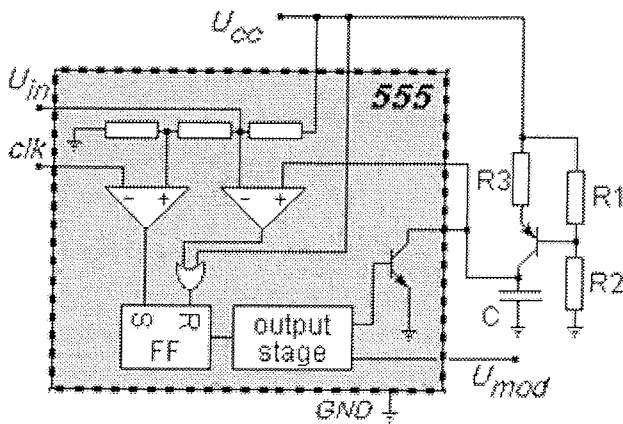


Figure 8: Proposed PWM modulator

The capacitor value is determined as:

$$C = \frac{I_c \times T_s'}{U_{in,max}}$$

where I_c is a charging current, defined as:

$$I_c = \frac{1}{R_3} \left(U_{cc} \frac{R_1}{R_1 + R_2} - U_{EB} \right),$$

where U_{EB} is the emitter-base voltage of the transistor used in an current-source circuit.

The MCU PWM signal was used as a clock signal (*clk*) to trigger the PWM modulator. So this signal carries double the information. The PWM's frequency determines the PWM's modulator frequency, while the PWM's duty cycle determines the input current amplitude. The PWM's frequency must be chosen to be sufficiently high to achieve sufficient resolution and to eliminate a phase shift between the input voltage and the input current. In our case, the PWM's frequency was 50 kHz.

4. Simulation and experimental results

The simulation results were acquired using the Boost converter model and the proposed controller model developed in Matlab-Simulink. A 200-W system with a 380-V output DC voltage and a 230-V input voltage was simulated to prove the proposed realization regularity. The experimental results were acquired using a 200-W PFC prototype board and a Motorola-HC08 evaluation board.

Figure 9 shows the simulation results for stationary (constant-load) operation. The input current directly mirrors the input-voltage shape, which reflects the resistive behavior of the whole system at the line terminals. The experimental measurement results under the same conditions are shown in Figure 10.

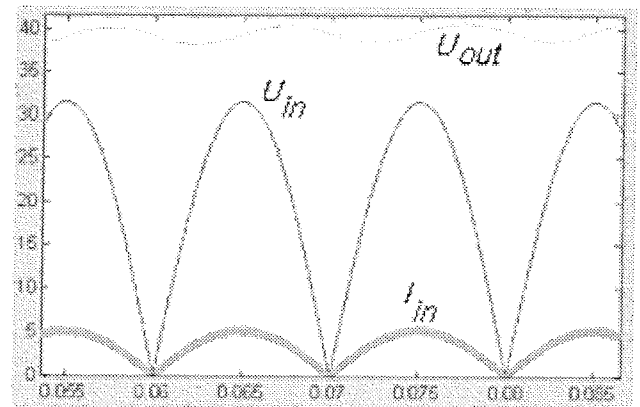


Figure 9: Typical simulation waveforms: DC Bus voltage U_{out} , rectified input voltage U_{in} and rectified input current I_{in}

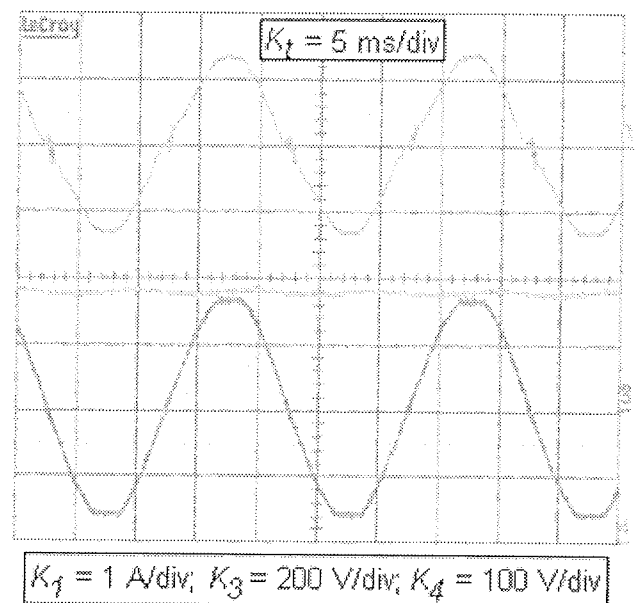


Figure 10: Typical experimental waveforms: DC Bus voltage U_{out} (ch 4), input voltage U_{in} (ch 3) and input current I_{in} (ch 1)

The measured waveforms from Fig 10 directly confirm the simulation results.

Another very important property of the PFC converter is its stable behavior under load variations. Experimental results acquired from a step load change from 140 W to 210 W are shown in Fig 11. It is obvious when comparing with the results in /1/, /5/, /10/ that the proposed PFC controller solution does not adversely affect the dynamic behavior of the closed-loop system.

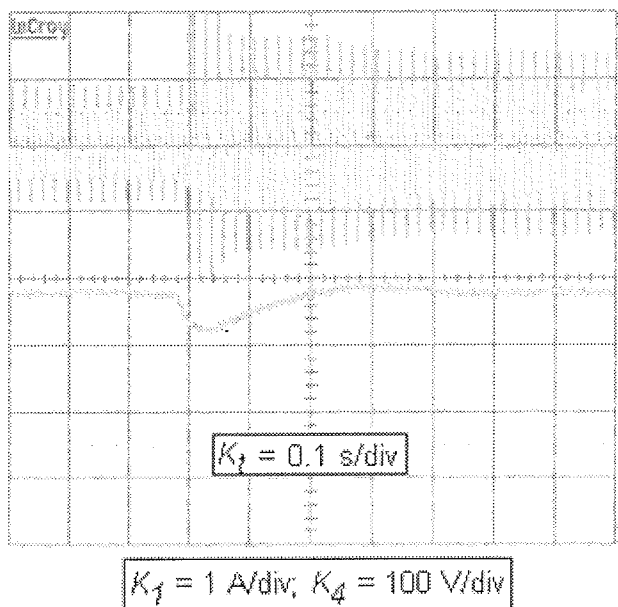


Figure 11: Input-current (ch1) and output-voltage (ch4) waveforms during a step load change from 140 W to 210 W

The switching frequency changes over a line period, as shown in Figure 12. This special course has a very important preference. While the switching frequency decreases in phase with the highest input current, the switching losses are, as a result, considerably reduced. In practice, the switching frequency does not really reduce to zero, as seen in the simulation results. In our case, the minimum switching frequency around the zero crossing point was 50 kHz.

The line-current harmonics measurement results are the same as in /10/, because of the equal current controller realization.

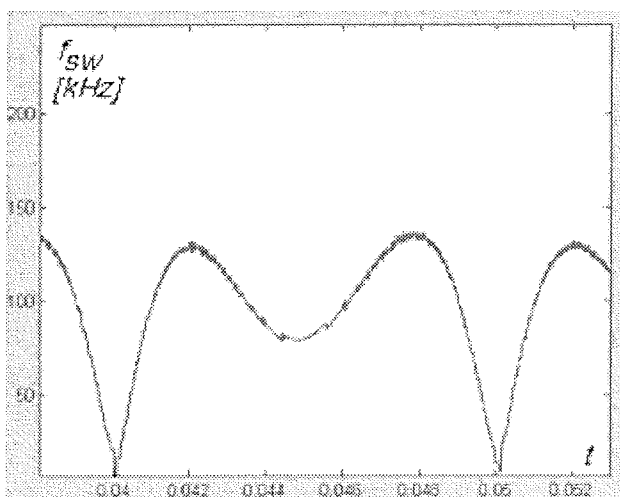


Figure 12: PFC switching frequency over a line half period – simulation results

The real benefit is obvious from the MCU load. The proposed solution requires about 100 A/D samples and mul-

tiplication instructions per second, while in /10/ this rate was 5000 A/D samples and multiplications per second. The PFC functions, written in C-language, occupy 150 program bytes, 10 RAM locations, and are executed in approximately 200 μ s at an 8-MHz MCU bus-frequency, i.e., 1% of the total execution time of the benchmarked MCU.

5. Conclusion

The proposed PFC control method is particularly suitable for the Boost PFC converter design in cost-sensitive applications where the use of special ICs or extra MCUs (DSPs) is not practical. The whole system is designed as a hybrid system, as a combination of a programmable digital circuit and an additional analog circuit. The microcontroller performs only the outer voltage-control loop, while the faster inner current-control loop is realized using a simple and low-cost analog circuit – a PWM modulator, an analog switch and a hysteresis comparator. The PFC algorithm can be executed in a sideline, together with the main application tasks, like motor control and lamp ballasts algorithms.

The proposed realization is suitable for critical conduction mode as well as continuous conduction mode Boost PFC converters.

With this solution, a good compromise between the CPU load and circuit complexity is achieved. The proposed PFC control method can be implemented in low-cost applications based on slower 8-bit MCUs, where previously proposed methods become too complex.

A soft-start function, for example, can easily be implemented by writing an additional program module. This module generates the current reference signal during start-up and switches to the PI-controller when the output voltage reaches its final value. Alternatively, just the PI-controller's output saturation level can be slowly raised to its upper limit during start-up, like in /1/. Over-current protection, which is also very important, can be implemented using an additional voltage comparator and (optionally) an input MCU pin. When using an IC with multiple comparators inside there is no additional hardware cost. Also, the current reference can be software limited. These additional functions result in an MCU program-code extension of up to 50 bytes when it is written in C-language.

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EXPERIMENTAL DETERMINATION OF THE MOSFET TURN-OFF SNUBBER CAPACITOR

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Key words: turn-off snubber, dc-dc converter, power dissipation, approximation functions, differential evolution method, experiment.

Abstract: This paper presents the analysis and design procedures of snubber circuits for low power dc-dc converters, realised using MOS-FETs. The appropriate design of the snubber circuit can considerably increase the power range, or decrease the total power dissipation of the low-power dc-dc converters available as an integrated circuit. The evaluation of a snubber circuit is based on analysis of the measured currents and voltages, approximated by the continuous functions. The differential evolution method is used to determine the approximation functions unknown coefficients. The results of this proposed method enable the reduction of power dissipation on the transistor while the converter's efficiency remains unchanged. The benefits, drawbacks and limits of the proposed approach are analysed in details. Experimental results are also given, obtained by a laboratory prototype of the boost converter.

Eksperimentalno načrtovanje kondenzatorja v izklopnem razbremenilnem vezju MOSFET-a

Ključne besede: izklopno razbremenilno vezje, dc-dc pretvornik, preklopne izgube, aproksimacijska funkcija, diferencialna evolucija, eksperiment.

Izveček: V članku smo predstavili analizo in postopek načrtovanja izklopnega razbremenilnega vezja za dc-dc pretvornike nizkih moči, ki so realizirani z MOS-FET-i. Ustrezno načrtovano razbremenilno vezje lahko pomembno poveča moč ali zmanjša stikalne izgube dc-dc pretvornika nizke moči, ki je na voljo v obliki integriranega vezja. Analiza razbremenilnega vezja temelji na analizi izmerjenih tokov in napetosti, ki smo jih aproksimirali z zveznimi funkcijami. Za določitev neznanih koeficientov izbranih aproksimacijskih funkcij smo uporabili metodo diferencialne evolucije. Iz izraženih analitičnih funkcij smo izračunali potek izklopne energije. Celotna izklopna energija, ki se pretaka med tranzistorjem in razbremenilnim vezjem, je enaka vsoti energije, ki jo absorbira tranzistor in energije, ki jo shrani kondenzator. Potek celotne izklopne energije ima minimum pri izbrani vrednosti kondenzatorja razbremenilnega vezja. Rezultati predlagane metode omogočajo zmanjšanje preklopnih izgub na tranzistorju pri nespremenjenem izkoristku pretvornika. Podrobno smo analizirali prednosti, slabosti in omejitve predlaganega pristopa. Podani so rezultati eksperimenta, ki smo ga izvedli na laboratorijskem prototipu dc-dc pretvornika navzgor.

1. Introduction

Dc-dc converters appear in large numbers of electrical equipment. Most of them are operated in hard switching mode, therefore, they suffer from switching losses. The hard switching operation and reduction of switching losses is discussed in many books and papers relating to these topics (McMurray 1980, Williams 1987, Rashid 1993). Recently basic converter structures such as buck converters, boost converters and buck-boost converters could be realised as chip versions. The switch power losses must be properly evaluated in such cases in order to use the internal chip transistor more efficiently. The snubber circuits are usually placed in the converter structure to adjust the switching-on and switching-off losses. The switching-on snubber circuit is connected in series to limit the di/dt at turn-on. The switching-off snubber circuit limits du/dt at turn-off.

The approach for evaluation of the switching-off dissipation suggested by (Williams 1987) and (Mohan et al. 1989) is efficiently used in the analysis of BJT-s where current and voltage could be replaced by linear functions. It is, however, less appropriate in the case of MOS-FET, where

current and voltage time shapes can not be treated by linear functions.

This paper suggest a modified design approach for a boost converter MOS-FET turn-off snubber circuit based on systematic experimental analysis of losses. The converter's currents and voltages during the switch-off interval are measured for different values of snubber capacitance, and they are approximated by analytical functions to calculate the switching losses. The differential evolution method (Price 1996) is used to determine the approximation functions unknown parameters for currents and voltages. Different energy components in the transistor-snubber system were calculated for different snubber capacitances by analytically given functions for currents and voltages. Analytical functions are also obtained for describing the relationship between calculated energy and snubber capacitance. The obtained analytical relationship enables determination of snubber capacitance according to converter efficiency or transistor dissipation.

2. Description of boost converter and RCD snubber circuit

The boost converter is shown in figure 1. The transistor Tr is equipped with a snubber circuit which consists of capacitor C_{CS} , resistor R_S and diode D_S .

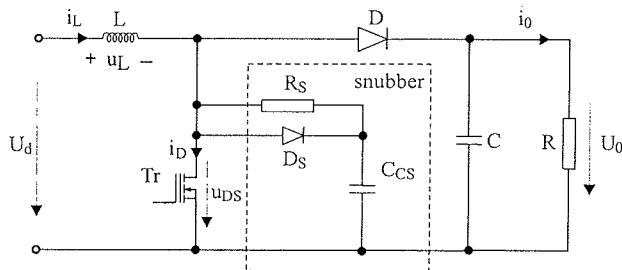


Figure 1. The boost converter with RCD snubber.

The typical waveforms of inductor current i_L , voltage u_L and drain current i_D during the converter operation are shown in figure 2.

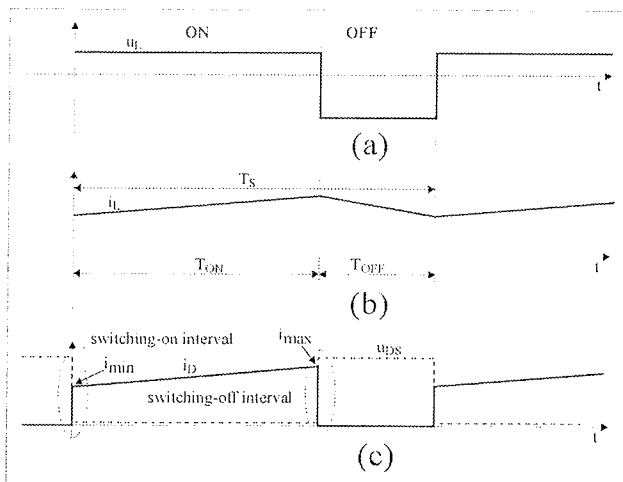


Figure 2. The typical waveforms of the boost converter: (a) the inductor voltage u_L , (b) the inductor current i_L , (c) the transistor current i_D .

A parallel snubber circuit is used to adjust the switching losses during the switching-off interval. The diode D_S connects the capacitor C_{CS} in parallel to the transistor during the switching-off transient. The resistance R_S protects the transistor during switching-on, limiting the discharge capacitor current. On the other hand the R_S must ensure that the capacitor C_{CS} will be completely discharged during the switching-on interval (figure 3b).

The MOS-FET current i_D during the switching-off interval could be considered as constant. At this interval the following can be supposed $i_D = i_{max} = I_D$ (see figure 2). The MOS-FET IRF530, working at the operating point $U_{DS} = 8.55$ V and $I_D = 0.845$ A (figures 1 and 2), was used in the experimental part of the analysis. The MOS-FET itself con-

tains some parasitic elements as capacitances C_{GS} , C_{GD} and C_{DS} . The last one must be taken into consideration in the snubber circuit design, although it is not directly stated by the manufacturer in the data sheet. The value of the unknown capacitor C_{DS} is calculated by the suggested method.

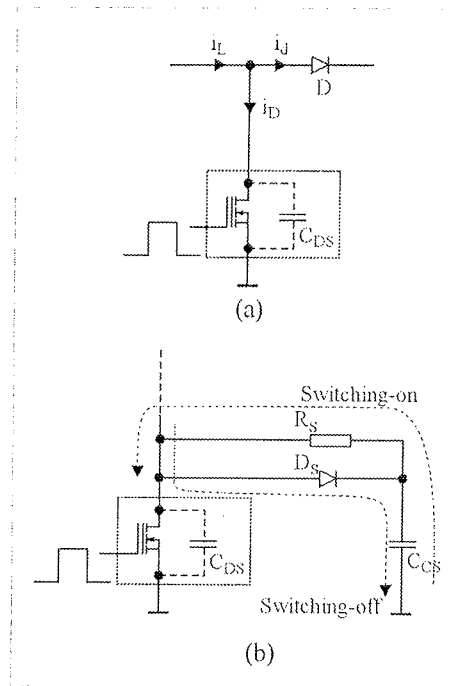


Figure 3. Switching cell of the boost converter: (a) MOS-FET without snubber, (b) the snubber circuit operation.

Measurements were performed by the different values of capacitor C_{CS} (table 1) in the circuit (figure 3b). Current i_D and voltage u_{DS} were measured from the beginning of the switching-off interval at $t = 0$ to the end of the transition interval at $t_x = 1 \cdot 10^{-6}$ s and they are shown in figure 4.

n	C_{CS} [nF]
1	0
2	2.7
3	3.4
4	7.1
5	10

Table 1. Selected values of snubber capacitors.

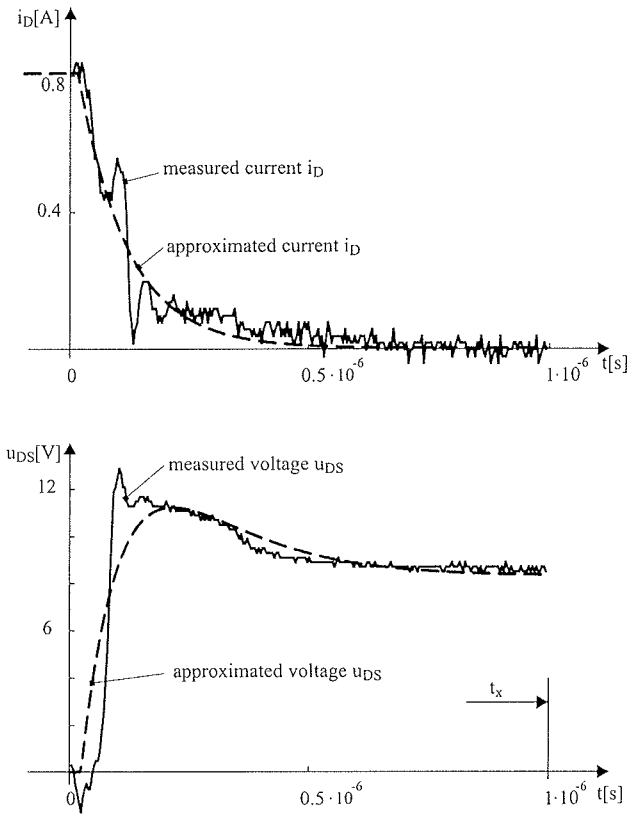


Figure 4. The switching-off transient; measured and approximated currents i_D and voltages u_{DS} .

Analytical formulation of measured current and voltage is needed for further analysis of the snubber circuit. It is obvious that both shapes can not be replaced by a linear function, therefore, nonlinear analytical exponential functions with the prescribed structure (1) and (2) are used to calculate the time-dependent current and voltage.

$$i(t) = a_{11} + a_{12}e^{a_{13}t}, \quad (1)$$

$$u(t) = a_{21} + a_{22}e^{a_{23}t} + a_{24}e^{a_{25}t}. \quad (2)$$

The unknown parameters $a_{(j)}$ are calculated separately for the each measured current and voltage pattern using the approximation procedure described in the next section. They are given in Appendix 1. Current i_D and voltage u_{DS} calculated by equations (1) and (2) are shown in figure 4. The agreement between the measured and calculated current and voltage waveforms seems to be acceptable.

The advantage of the analytical description of the measured current and voltage by (1) and (2) is the possibility of further analytical calculation.

3. Calculation of approximation function parameters

Measured current and voltage patterns were approximated by the analytical functions (1) and (2). The parameters

$a_{(j)}$ appearing in (1) and (2) were determined by an optimisation method based on differential evolution. Differential evolution is a stochastic search method (Price 1996). The optimisation routine, originally developed for the surface approximation (Težak et al. 2002), was implemented in MATLAB™. The routine inputs are the measured current or voltage patterns. The differential evolution minimisation algorithm is applied to the routine searching the unknown

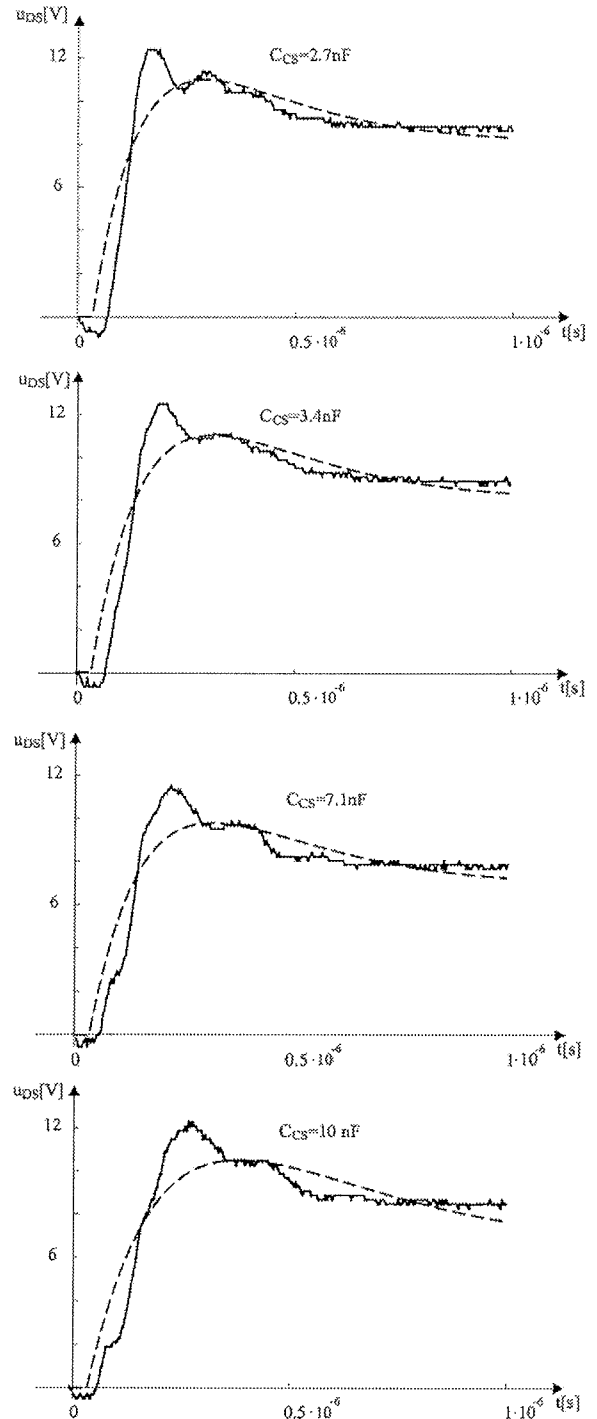


Figure 5. Voltage waveforms for different values of snubber capacitor.

approximation parameters of the selected exponential approximation functions (1) and (2). It is minimising the total error defined as a sum of the squared errors. Error is the difference between the measured and calculated values of current or voltage in the corresponding time sample. The search process is finished when a predefined value of the objective function is reached or when the maximal number of searching steps is achieved. The outputs of the routine are the calculated parameters of equations (1) or (2).

The main advantage of measured results presentation by an analytical function is the possible calculation of function value at any point, and analytical mathematical operations such as multiplication and derivation.

4. Energy consideration

The total switching-off dissipation of the system in figure 3b depends on the value of the parallel capacitance C_s . The capacitance C_s in MOS-FET transistors consists of unknown parasitic capacitance C_{DS} and parallel snubber capacitor C_{CS} , which is given by (3).

$$C_s = C_{CS} + C_{DS} \quad (3)$$

The minimal switching-off dissipation of the whole system can be obtained by the suggested analysis of the total energy absorbed by the MOS-FET and energy stored by the snubber capacitor, which obviously depends on the value of C_{CS} . This energy can be calculated analytically using previously explained approximation functions for the measured currents and voltages, which are measured for the different values of C_{CS} . The first measurement of current and voltage for $C_{CS} = 0$ nF ($n = 1$ in table 1) is shown in figure 4. The next four snubber capacitances were chosen around the value $C_{CS} = 7.1$ nF, which were calculated according to the procedure suggested by (Williams 1987) ($n = 4$ in table 1). The capacitors were selected so that one of them was higher than it (10 nF) and two of them were smaller than it (2.7 nF and 3.4 nF). The performed calculated energy analyses showed, that the calculated capacitance $C_{CS} = 7.1$ nF did not minimise the switching-off losses.

Four additional measurements of currents and voltages for the values of capacitance 2.7, 3.4, 7.1 and 10 nF were done afterwards. The current wave-shapes in all cases remained almost equal to the one in figure 4, as was expected. The measured voltage wave-shapes are given in figure 5 and they depend on the connected capacitance C_{CS} . The energy W_s stored in the capacitance C_s at the end of switching-off interval is calculated by equation (4) in the continuous time domain or by equation (5) in the discrete time domain:

$$W_s = \int_0^{t_x} u_{DS} \cdot i_{C_{DS}} dt \quad (4)$$

$$W_s = \sum_{k=0}^m u_{DS}(k) \cdot i_{C_{DS}}(k) \cdot T_s, T_s = \frac{t_x}{m} \quad (5)$$

where the parasitic capacitance current $i_{C_{DS}}$ was calculated by $i_{C_{DS}} = I_D - i_D - i_d$, as follows from figures 2c and 3a, and T_s is the sampling time. Currents i_D , i_d and voltage u_{DS} are measured instantaneous values of MOS-FET (Tr) drain and diode (D) currents and drain source voltage, respectively. Currents and voltages are measured by Tektronix TDS4000 and are available as data series.

Parasitic capacitance C_{DS} can be determined by equation (6), taking into account that $W_s = W_{DS}$ when $C_{CS} = 0$:

$$C_{DS} = C_s \Big|_{C_{CS}=0} = \frac{2W_s \Big|_{C_{CS}=0}}{U_{DS}^2} \quad (6)$$

where U_{DS} is the steady state value of drain source voltage on the MOS-FET, and C_{CS} is the snubber capacitance.

Further analysis of switching losses is based on the known value of parasitic capacitance C_{DS} , therefore, it has to be determined first. The energy W_s stored in the parasitic capacitance C_{CS} is calculated by (5) which gives $W_s(C_{CS}=0) = 0.04752 \mu\text{J}$; capacitance $C_{DS} = 1.3$ nF is calculated afterwards by (6).

The energy W_{Tr} supplied to the system during the switching-off interval is calculated as energy absorbed by transistor, either by equation (7) in the continuous time domain or by equation (8) in the discrete time domain.

$$W_{Tr} = \int_0^{t_x} u_{DS} \cdot i_D dt \quad (7)$$

$$W_{Tr} = \sum_{k=0}^m u_{DS}(k) \cdot i_D(k) \cdot T_s, T_s = \frac{t_x}{m} \quad (8)$$

The total energy W_{TOT} absorbed in the system during the switching-off process is obtained as a sum of the energy stored in the snubber capacitor W_{CS} , and the energy absorbed by transistor W_{Tr} using equation (9) for five different values of capacitors C_{CS} (see table 1).

$$W_{TOT} = W_s + W_{Tr} \quad (9)$$

The above-mentioned energies were calculated using equations (4) to (9). These results are shown in tables 2 and 3. The energy values in table 2 are calculated directly from the measured current and voltages. The energies in table 3 are calculated by using approximation functions of currents and voltages, which are plotted by the dashed lines in figures 4 and 5. The disturbing influence of the measuring noise on the calculated energy has been eliminated using the described method in which the determined analytical functions are used to calculate the energy. The corresponding values of W_{CS} in table 2 and 3 are the same, because they are calculated from the steady state value of voltage U_{DS} , which is the same in all cases ($U_{DS} = 8.55\text{V}$). The values of W_{Tr} shown in table 2 differ slightly from that ones in table 3, because they were calculated by the measured currents and voltages containing noise. The differ-

ence between results in tables 2 and 3 is indeed negligible, therefore, the results from table 3 will be used further on.

C_S [nF]	W_S [μJ]	W_{Tr} [μJ]	W_{TOT} [μJ]
1.3	0.04752	0.91034	0.9579
4	0.14621	0.77014	0.9164
4.7	0.17179	0.78189	0.9537
8.4	0.30703	0.69078	0.9978
11.3	0.41303	0.69115	1.1042

Table 2. Calculated values of energy (calculated directly by measured data).

C_S [nF]	W_S [μJ]	W_{Tr} [μJ]	W_{TOT} [μJ]
1.3	0.04752	0.91193	0.9595
4	0.14621	0.78064	0.9268
4.7	0.17179	0.78861	0.9604
8.4	0.30703	0.70085	1.0079
11.3	0.41303	0.68446	1.0975

Table 3. Calculated values of energy (calculated by approximation functions).

The values of total energy W_{TOT} and the energy absorbed by transistor W_{Tr} , taken from table 3, are indicated by the cross marks of the graph in figure 6. The marked energies were approximated by analytical functions (10) and (11) in a similar way as was done by the basic functions (1) and (2) for the measured currents and voltages in section 2.

$$W_{TOT}(C_S) = b_{11} + b_{12}e^{b_{13}C_S} + b_{14}e^{b_{15}C_S} \quad (10)$$

$$W_{Tr}(C_S) = b_{21} + b_{22}e^{b_{23}C_S} \quad (11)$$

The values of the calculated coefficients $b_{(i)}$ for $W_{TOT}(C_S)$ and $W_{Tr}(C_S)$ are given in appendix 2. Calculated functions $W_{Tr}(C_S)$ and $W_{TOT}(C_S)$ from the data in table 3 are shown in figure 6 as solid lines. It is necessary to note that it is impossible to obtain the energy value for the capacitance $C_S < C_{DS}$ by the measurement of current and voltage, because parasitic capacitance C_{DS} in case of MOS-FETs is always different to zero. The values of both functions $W_{Tr}(C_S)$ and $W_{TOT}(C_S)$ at point $C_S = 0$ nF can be obtained by the extrapolation of functions (10) and (11) to the hypothetical point where $W_{Tr} = W_{TOT}$. The dashed lines in figure 6 were obtained by the above-mentioned extrapolation.

The value $W_{TOT}(C_S = 0) = 1.001 \mu J$ is used as a base for normalization further on.

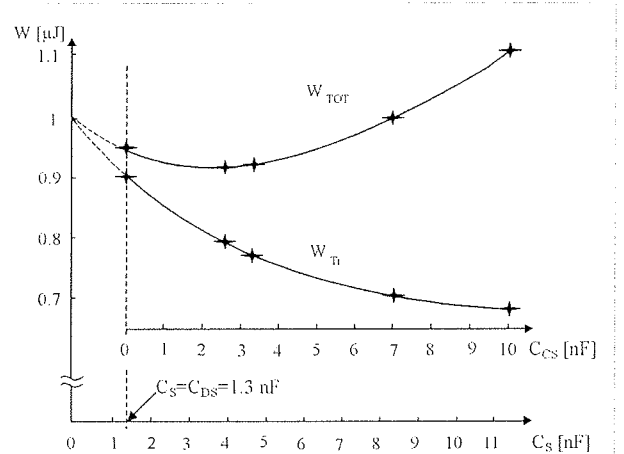


Figure 6. Graph of functions $W_{TOT}(C_S)$ and $W_{Tr}(C_S)$

Per-unit (p.u.) values of energy from table 3 are shown in table 4. The energies are normalised by the energy $W_{TOT}(0) = W_{TOT}(C_S = 0)$ using equation (12).

$$w_{TOT} = \frac{W_{TOT}}{W_{TOT}(0)}, \quad w_{Tr} = \frac{W_{Tr}}{W_{TOT}(0)} \quad (12)$$

C_S [nF]	w_S	w_{Tr}	w_{TOT}
0	0	1	1
1.3	0.04747	0.9112	0.9585
4	0.14606	0.77986	0.9259
4.7	0.17162	0.78782	0.9594
8.4	0.30672	0.70015	1.0069
11.3	0.41262	0.68378	1.0964

Table 4. Calculated values of normalised energy (calculated by approximation functions).

As the total energy functions $w_{TOT}(C_S)$ and $w_{Tr}(C_S)$ are analytical functions of the form (10) and (11) with the known parameters, the minimum of $w_{TOT}(C_S)$ can be calculated analytically by the expression (13).

$$\frac{d w_{TOT}(C_S)}{d C_S} = 0 \quad \Rightarrow \quad C_S = 3.4 \text{ nF} \quad (13)$$

The minimum of the total energy w_{TOT} in point "O" (figure 7) is reached by the capacitance $C_S = 3.4$ nF which gives the snubber capacitor $C_{CS} = 2.1$ nF, due to equation (3).

The dissipation decrease Δw_{TOT} at point "O" in figure 7 is around 6%, while the dissipation decrease Δw_{Tr} on the transistor is around 20%. Moreover, if the snubber capacitance $C_{CS} = 6.5$ nF is used, the efficiency of the converter at point "P" is exactly the same as in the hypothetical case where $C_S = 0$ nF. However, the transistor dissipation w_{TOT} is decreased by almost 30%.

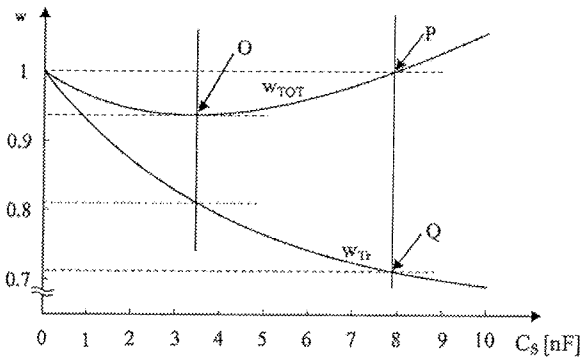


Figure 7. Graphs of normalised functions $w_{TOT}(C_s)$ and $w_{TF}(C_s)$

5. Conclusion

The proper design of a snubber circuit can considerably decrease the total power dissipation on the transistor. The methods for the evaluation of switching-off dissipation suggested in the literature are inappropriate in the case of MOS-FETs, because of the presumption that current and voltage during the switching-off interval can be expressed by a linear function. A new approach to the design of snubber circuits for low power dc-dc converters, based on the experimental analysis of measured currents and voltages is suggested in this paper. Currents and voltages are measured for different values of snubber capacitance and they are approximated by the corresponding analytical functions, in a way that the difference between measured and calculated values becomes minimal in the quadratic sense. The energy values are calculated for the different snubber capacitances by analytically given currents and voltages. The

function describing relationship between the energy and the snubber capacitance is also determined by an approximation. The obtained analytical function enables calculation of proper snubber capacitance regardless of whether the MOS-FET switching-off dissipation or total switching-off dissipation of the snubber circuit is minimised. The only disadvantage of the suggested method is that a certain number of current and voltage measurements are required. The objective of future work will be finding out relationships between the parameters of approximation functions for energy and the MOS-FET data from the data sheet directly, to avoid extensive measuring and calculations.

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Appendix 1

Coefficients $a_{(.)}$ of the equations (1) and (2).

a_{11}	a_{12}	a_{13}
0.028357	0.93109	-9452981.3417

n	C_{Cs} [nF]	$a_{n+1,1}$	$a_{n+1,2}$	$a_{n+1,3}$	$a_{n+1,4}$	$a_{n+1,5}$
1	0	8.3082	-9177.9403	-8142542.4133	9164.3296	-8127151.164
2	2.7	8.176	-12610.1669	-6149625.3087	12596.7656	-6141240.3854
3	3.4	8.052	-12919.3637	-5613668.9851	12906.3012	-5606118.774
4	7.1	7.5534	-10200.2252	-5376230.2305	10188.0022	-5367087.3051
5	10	6.5299	-9817.926	-4035161.8147	9807.0537	-4027274.4877

Appendix 2

Coefficients $b_{(.)}$ of the equations (10) and (11).

b_{11}	b_{12}	b_{13}	b_{14}	b_{15}
$414.489 \cdot 10^{-6}$	$-413.859 \cdot 10^{-6}$	$-9.2579 \cdot 10^{-5}$	$0.36945 \cdot 10^{-6}$	-0.21646

b_{21}	b_{22}	b_{23}
$0.6561 \cdot 10^{-6}$	0.3429310^{-6}	-0.23016

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HIGH-SPEED SINGLE D-FLIP-FLOP PSEUDO-RANDOM BIT SEQUENCE GENERATOR

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Key words: Pseudo-random binary sequence (PRBS) generator, high-speed logic design, bit-error-rate (BER) testing, microwave circuit, emitter-coupled logic (ECL)

Abstract: In this article, a new PRBS generation method using a single D-flip-flop is presented. The new method is suitable for the highest data rates, since it allows operation at clock frequencies equal or higher than a shift-register chain, made of the same type of D-flip-flops. Most of the required delays in the new PRBS generator are generated by microwave transmission lines, enabling a higher clock frequency while simplifying circuit design and lowering the cost. A 2.48832Gbit/s PRBS generator was practically implemented using the new method, producing pseudo-random bit sequences corresponding to two standard polynomials $1+x^6+x^7$ and $1+x^{14}+x^{15}$. This efficient design was practically tested at 2.488Gbit/s while its main application is to provide inexpensive 10Gbit/s and 40Gbit/s pseudo-random data sources.

Gigabitni psevdonaključni podatkovni izvor

Ključne besede:

Izleček: V prispevku je predstavljena nova metoda generiranja psevdonaključnega binarnega zaporedja (PRBS), ki za delovanje potrebuje le en D flip flop. Nova metoda je primerna za generiranje psevdonaključnih zaporedij zelo visokih bitnih hitrosti, saj deluje z enakimi ali večjimi taktnimi frekvencami kot pomikalni register, izveden z verigo enakih D flip floпов. Večina potrebnih zakasnitev pomikalnega registra je izvedena z mikrovalovnimi linijami, kar omogoča višje taktne frekvence ter cenejšo izdelavo. Praktična izvedba PRBS generatorja z bitno hitrostjo 2,48832 Gbit/s uporablja novo metodo in omogoča dva standardna polinoma $1+x^6+x^7$ ter $1+x^{14}+x^{15}$. Ta učinkovita metoda je bila sicer praktično preverjena pri 2,488 Gbit/s, vendar je njena glavna uporaba namenjena enostavnim in poceni PRBS izvorom z bitnimi hitrostmi 10 in 40 Gbit/s.

Introduction:

Pseudo-Random Binary Sequences (PRBS), usually maximum-length sequences, are widely used in communications systems. PRBS are used as spreading sequences in direct-sequence spread-spectrum systems, like mobile terrestrial CDMA systems or GPS navigation signals. Further,

PRBS are used as test data patterns in Bit-Error-Rate test equipment, since they are simple to generate and verify while their mathematical properties resemble random data.

Maximum-length sequences are generated by modulo-2 polynomial division with irreducible polynomials. The latter is practically implemented in the form of linear-feedback

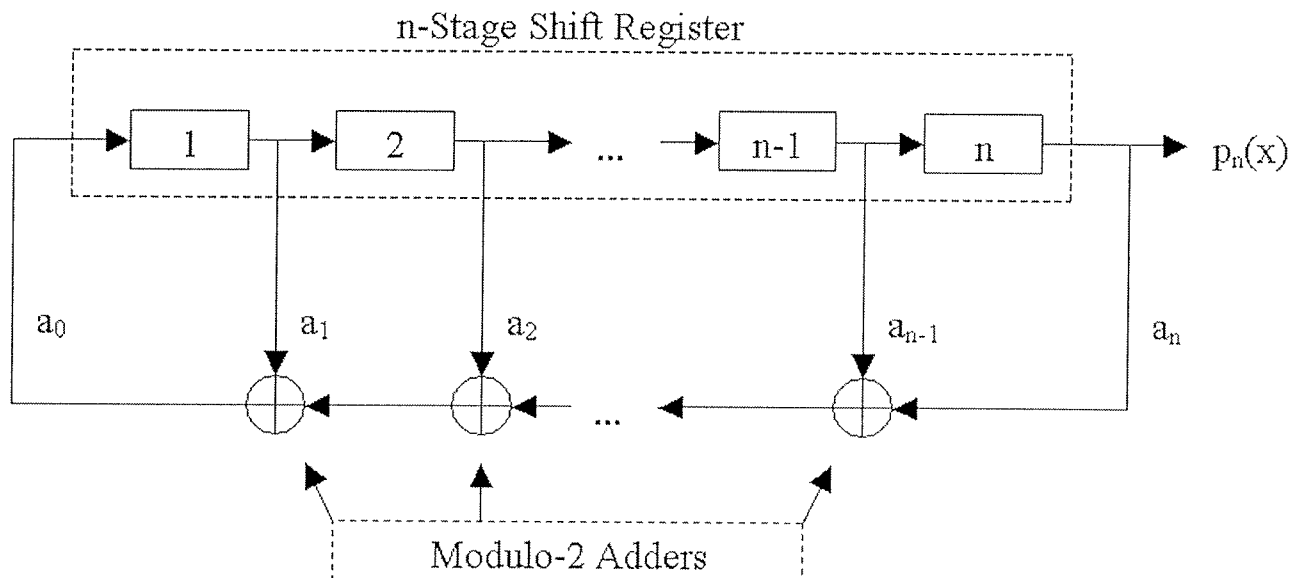


Figure 1: Fibonacci-type n-stage linear-feedback shift register.

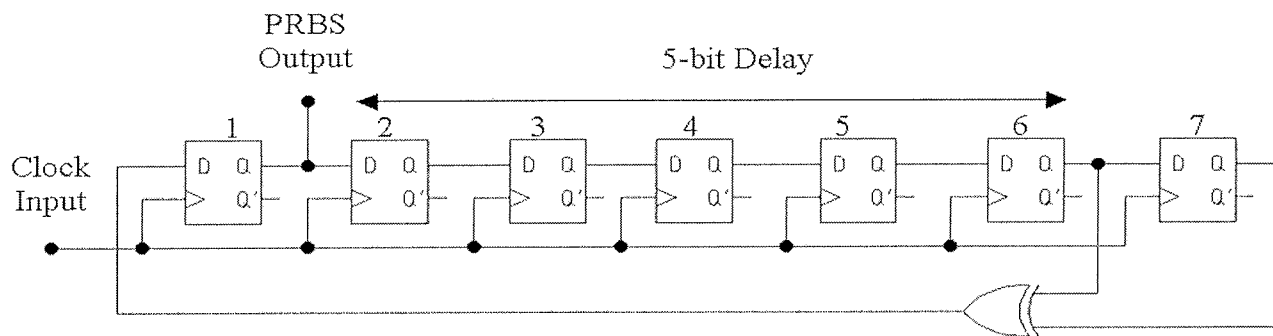


Figure 2: Conventional 7th order PRBS logic circuit generating polynomial $1+x^6+x^7$.

shift registers (LFSR) /1/, where the linearity of the feedback is achieved by modulo-2 addition with EX-OR logic gates as shown on Figure 1. Maximum-length sequences of the length 2^n-1 (where n is the number of shift-register stages) have several interesting mathematical properties, like a precisely-defined pseudo-random distribution of logical ones and zeros, a two-level autocorrelation function and a frequency spectrum including equally-spaced, equal-amplitude spectral lines.

A single D-flip-flop Linear-Feedback Shift Register:

One of the commonly used (modulo-2 irreducible) polynomials in the multi-Gbit/s range communication test equipment is $p(x) = 1 + x^6 + x^7$. Typically such a LFSR comprises seven D-flip-flops and one EX-OR gate as shown on Figure 2.

Ideally, the flip-flops 2 through 6 insert a 5-bit delay ($1\text{-bit delay equals } 1/f_{\text{clock}}$) from the PRBS output tap to the first EX-OR gate tap and the flip-flop 7 inserts a 1-bit delay between the EX-OR gate inputs.

The new method proposed in this article is to replace as many D-flip-flops as possible with transmission lines (microstrip lines, coaxial lines, etc.) to generate delays. However, at least one D-flip-flop is required for signal regeneration (retiming and reshaping) in a PRBS generator. Figure 3 illustrates the new PRBS generator including a single D-flip-flop, an EX-OR gate and additional transmission (delay) lines.

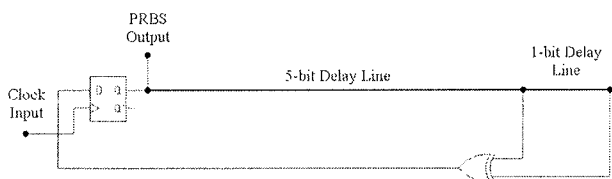


Figure 3: A single-D-flip-flop 7th order PRBS circuit generating polynomial $1+x^6+x^7$.

Note that the circuit from Figure 3 requires an ideal D-flip-flop and an ideal EX-OR gate (without any internal propagation delays) and that the 1-bit delay line is connected

directly between EX-OR gate inputs without any additional PCB traces. Of course, both internal D-flip-flop and EX-OR-gate propagation delays have to be considered in the practical high-speed circuit design, where the sum of both delays is subtracted from the ideal 5-bit delay.

When compared to the conventional LFSR circuit of Figure 2, the new PRBS circuit has many advantages: simplicity, less logic elements (integrated circuits) and a lower cost. A single-D-flip-flop design eliminates complex clock distribution circuits required for several D-flip-flops in conventional high-speed LFSR designs. Finally, the clock frequency can be increased to the upper D-flip-flop toggle limit and the latter is usually much higher than the clock-frequency limit imposed by propagation delays in a chain of D-flip-flops, especially in the case of discrete-packaged devices.

Unfortunately, the single-D-flip-flop PRBS design also has some drawbacks: the PRBS polynomial depends on the delay lines and cannot be changed easily, the PRBS sequence length is limited by the insertion loss and dispersion of the delay lines and the design only works for a selected, single clock frequency as defined by the delay lines.

A 2.48832 Gbit/s PRBS data pattern generator core

The new PRBS generation method, using a single D-flip-flop, has been tested on a working prototype using ON Semiconductor's ECLinPS Lite /2/ integrated circuits, MC100EL31 (D-flip-flop) and MC10EL58 (2:1 multiplexer used as an EX-OR gate) at a clock frequency of 2.48832GHz. Besides the two ECL chips, an 1-bit microstrip delay line and two removable coaxial delay lines were used in the core of the 2.48832Gbit/s PRBS data pattern generator to produce two different pseudo-random sequences corresponding to the polynomials $1+x^6+x^7$ and $1+x^{14}+x^{15}$. Both coaxial delay lines were shortened from the ideal 5-bit (for $1+x^6+x^7$ polynomial) or 13-bit (for $1+x^{14}+x^{15}$ polynomial) propagation delays to compensate for the internal propagation delays of the D-flip-flop, of the 2:1 multiplexer and corresponding PCB transmission lines to the SMA connectors, where the coaxial delay lines are connected.

To reduce the output data jitter and clock crosstalk, two more integrated circuits were added to the PRBS generator prototype as shown on Figure 4. An additional MC100EL31 D-flip-flop is used to decrease the output PRBS data jitter. A differential receiver MC10EL16 is used to remove common-mode signals (primarily 2.48832GHz clock) from the output PRBS data.

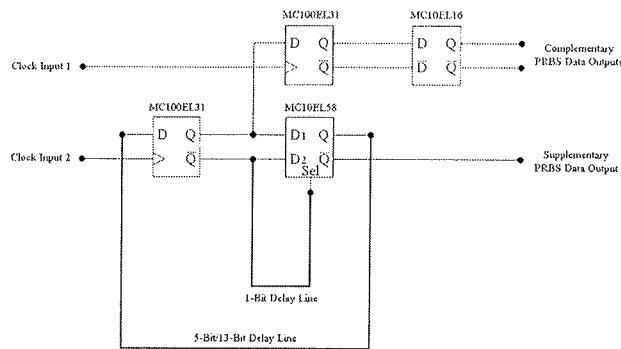


Figure 4: Circuit diagram of the 2.48832Gbit/s PRBS data pattern generator core, with the addition of a second D-flip-flop and a differential receiver.

Bold lines on Figure 4 represent 50Ohm impedance-controlled transmission lines. The circuit has two 2.48832GHz (sinewave) clock inputs driving the clock inputs of the two D-flip-flops. The two complementary ECL PRBS data outputs have to be DC-terminated to Vtt for optimal performance. The supplementary, AC-coupled, PRBS data output is connected to the 7th order polynomial PRBS pattern-sync trigger-generator circuit, to be described later in this article.

The prototype of the 2.48832Gbit/s PRBS generator core, including the second D-flip-flop and differential receiver is built on a 0.8mm-thick, double-sided "Epsilon-10" laminate, with the bottom side acting as the microstrip ground-plane and connected to the Vcc. The top side is used for impedance-controlled microstrip transmission lines. All power supply connections are made using thin wire bridges. The 1-bit microstrip delay line was manually trimmed for the optimum length to compensate for the reactive impedance of the "D2" input of the MC10EL58 multiplexer. A photo of the prototype is shown on Figure 5.

The quality of the output PRBS data was evaluated using a 40GHz-input-bandwidth sampling oscilloscope (HP83480A Digital Communications Analyzer with HP83482A Plug-In). A simple resistive divider circuit was used to terminate the ECL outputs to Vtt, while enabling a DC-coupled connection to the 50Ohm input of the sampling oscilloscope. Since differential test equipment was not available, only single-ended measurements were performed.

The eye pattern of the output PRBS data corresponding to the $1+x^{14}+x^{15}$ polynomial is shown on Figure 6. The clock

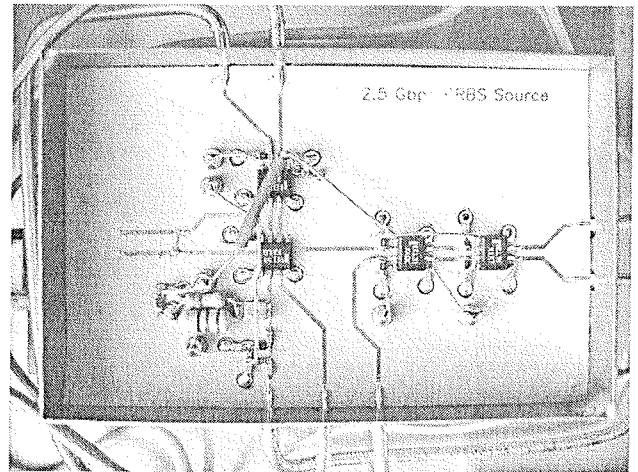


Figure 5: Photo of the 2.48832Gbit/s PRBS generator core circuit prototype.

crosstalk is clearly visible in the PRBS data. The peak-to-peak jitter (of the sampling oscilloscope and the PRBS generator) of approximately 40ps could be further reduced using additional D-flip-flops. The jitter is predominantly deterministic since the measured peak-to-peak value does not grow significantly with time.

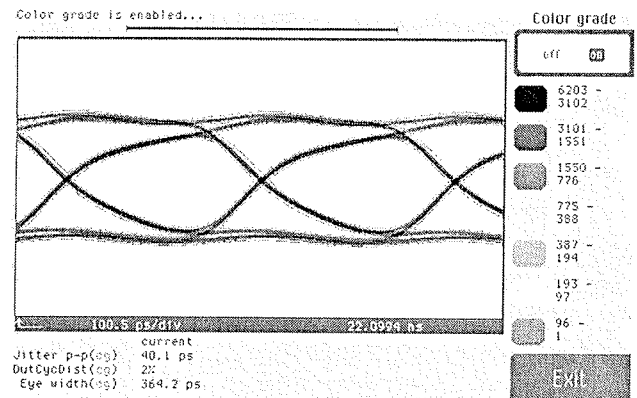


Figure 6: Eye pattern of the $1+x^{14}+x^{15}$ PRBS.

An Agilent 8565EC 50GHz spectrum analyzer was used to measure the frequency spectrum of the output PRBS data corresponding to the $1+x^6+x^7$ polynomial as shown on Figure 7. Again, the 2.48832GHz clock crosstalk is clearly visible in the output PRBS data spectrum. Due to simple NRZ encoding, a $\sin(x)/x$ spectrum envelope is expected and can be fairly well recognized on Figure 7.

A pattern-sync trigger-generator circuit for the $1+x^6+x^7$ polynomial

The eye pattern is one of the most popular measurements of data signal quality since it is implemented easily: the oscilloscope is triggered by a synchronous data clock. No knowledge of the exact data content is needed and no frame nor pattern trigger pulses are required for the meas-

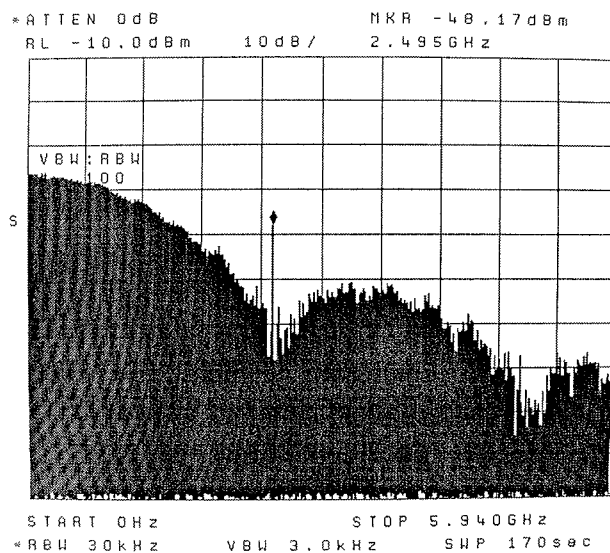


Figure 7: Frequency spectrum of the $1+x^6+x^7$ PRBS.

urement of the eye pattern. However, other measurements like the observation of specific bit distortions may require a frame-sync or pattern-sync trigger pulse. The beginning of a maximum-length LFSR sequence is usually defined with the all-ones state of the shift register. The detection of the all-ones state requires additional high-speed logic circuits and may be very expensive to implement at high clock frequencies. Fortunately, at least for short LFSR sequences there is a simpler, analog way of deriving a pattern-sync trigger pulse.

Since the spectrum of a maximum-length LFSR sequence includes equally-spaced discrete spectral lines, it is sufficient to filter out the lowest-frequency spectral line to obtain a trigger that is synchronous to the whole sequence pattern. In the case of the 2.48832Gbit/s $1+x^6+x^7$ polynomial sequence that has a repetition period 127bits, the lowest discrete spectral component has a frequency of 19.593MHz.

The supplementary, AC-coupled, 2.48832Gbit/s PRBS data is simply fed through a low-pass filter circuit with the cutoff frequency of about 22MHz. The 7th order pattern-sync circuit diagram is shown on Figure 8 and includes an INA-10386 MMIC amplifier and two low-pass filters: a lumped-element 22MHz low-pass and a 400MHz microstrip low-pass to suppress the spurious responses of the lumped-element filter above 1GHz. The prototype photo is shown on Figure 9.

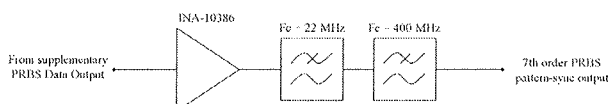


Figure 8: Circuit diagram of the 7th order pattern-sync circuit.

The sinewave output of the analog low-pass pattern-sync circuit is further processed by an additional circuit (descrip-

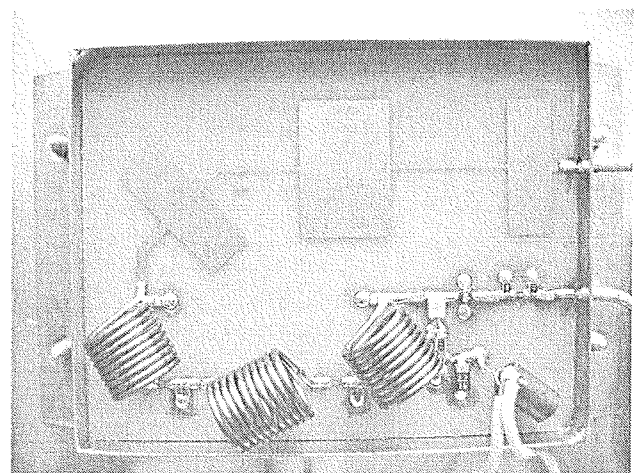


Figure 9: Photo of the 7th order pattern-sync circuit prototype.

tion omitted from this article): MC10H102 gate and yet another MC100EL31 flip-flop. MC10H102 gate converts analog pattern-sync trigger signal to ECL logic levels. Most of the timing jitter of the trigger signal is removed by MC100EL31 D-flip-flop clocked at 2.48832GHz. Such a pattern-sync trigger signal allows a detailed analysis of the PRBS bit pattern. The complete 127-bit PRBS pattern is shown on Figure 10.

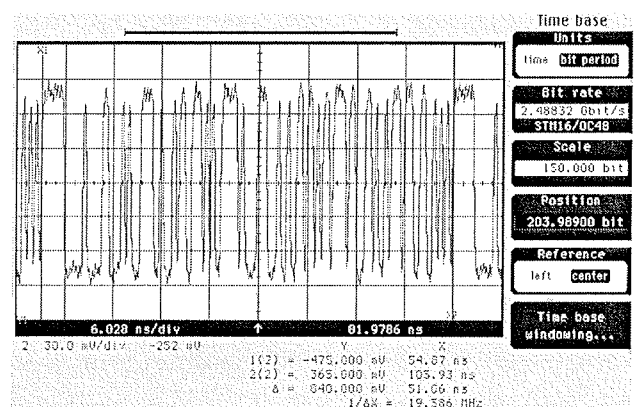


Figure 10: The complete 127-bit PRBS pattern.

An overview of the standalone 2.48832Gbit/s PRBS data pattern generator

The circuits described in this article are parts of the standalone 2.48832Gbit/s PRBS (OC-48/STM-16) data pattern generator. Besides the described PRBS core circuit and PRBS pattern-sync trigger circuit, the generator also includes a 2.48832GHz clock source PLL-locked to an internal crystal reference, a clock-signal distribution circuit (for both D-flip-flops in the PRBS core circuit), a trigger circuit to start the PRBS generator in the case of an all-zero stall and power-supply circuits for the V_{bb} and V_{tt} voltages required by ECL circuits.

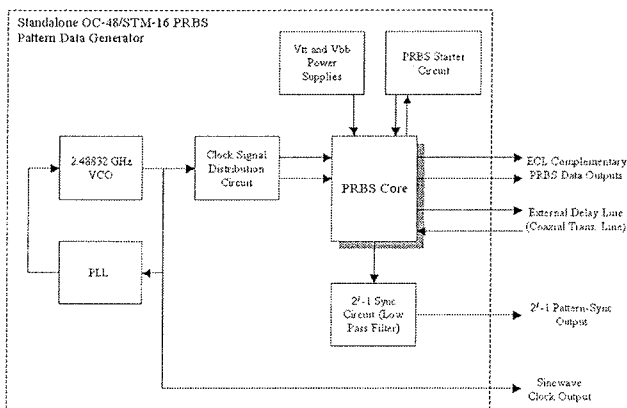


Figure 11: Block diagram of the standalone 2.48832 Gbit/s PRBS generator.

The block diagram of the PRBS generator is shown on Figure 11. The generator has two complementary ECL data outputs (Q and /Q), two connectors for the external delay line, a pattern-sync trigger output for the $1+x^6+x^7$ polynomial and two clock outputs. Descriptions of the additional circuits are beyond the scope of this article, but none of them is not as nearly (relatively) complex as PRBS core circuit. A photo of the standalone 2.48832Gbit/s PRBS data pattern generator prototype is shown on Figure 12.

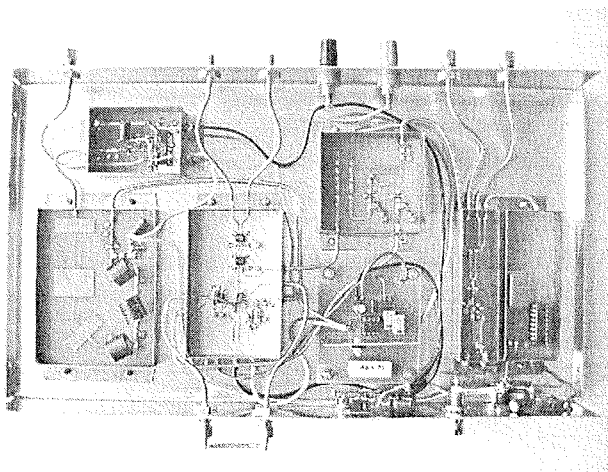


Figure 12: Standalone 2.48832Gbit/s (OC-48/STM-16) PRBS generator.

Conclusion:

The design of a simple and efficient high-speed PRBS data pattern generator was presented in this article. The PRBS generator achieves error-free operation at a clock frequency of 2.48832GHz that is almost twice the limit imposed by device propagation delays for conventional shift-register designs using chains of (discrete) MC100EL31 D-flip-

flops. Furthermore, the clock frequency of the single-D-flip-flop design is limited only by the D-flip-flop maximum toggle frequency. A companion Bit-Error-Rate test receiver could be designed in the same way, implementing a polynomial divider with transmission-line delays in place of D-flip-flops.

Knowing the mathematical properties of LFSR sequences even some other circuits can be simplified, like replacing complex digital pattern-sync circuits with simple analog low-pass filters. Although all of our experiments were made at 2.48832GHz, the principles are fully scalable to higher clock frequencies of 10GHz and even 40GHz. This means that a complete Bit-Error-Rate test setup can be built for 10Gbit/s or even 40Gbit/s for a very small fraction of the cost of similar, commercially available OC-196 and OC-768 test equipment.

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SIMULACIJA OBNAŠANJA SC SIGMA-DELTA MODULATORJEV V ČASOVNI DOMENI Z UPOŠTEVANJEM NEIDEALNOSTI

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Ključne besede: Sigma-Delta modulator, modeliranje, neidealnosti, SC, simulacija, MATLAB, SIMULINK.

Izvleček: V prispevku je predstavljen kompleten nabor modelov v programskem orodju SIMULINK, s katerim je mogoča izčrpna simulacija poljubnega SC¹ Sigma-Delta ($\Sigma\Delta$) modulatorja v časovni domeni. Predlagan nabor modelov zajema večji del neidealnosti $\Sigma\Delta$ modulatorja: podrtavanje vzorčevalnega signala, preklonni termični šum in neidealnosti operacijskega ojačevalnika (beli šum, končno ojačanje, pasovno širino, izhodno odzivnost² in napekost nasičenja³). Naštete neidealnosti so obravnavane ločeno, njihov vpliv je demonstriran na primeru simulacije nizkoprepustnega SC $\Sigma\Delta$ modulatorja 2. reda.

Time-domain Behavioral Simulation of SC Sigma-Delta Modulators Considering Non-idealities

Key words: Sigma-Delta modulator, modeling, non-idealities, switched-capacitor, simulation, MATLAB, SIMULINK.

Abstract: Sigma-Delta ($\Sigma\Delta$) modulators are the most suitable A/D converters for low-frequency, high resolution applications, considering their inherent linearity, reduced anti-aliasing filtering requirements and robust analog implementation. A typical block diagram of an oversampling $\Sigma\Delta$ A/D converter consists of anti-aliasing filter, modulator and decimator (figure 1). Anti-aliasing filter eliminates the spectral components from the input signal above half the sampling frequency. To shape the quantization noise, the input signal is highly oversampled and quantized. Oversampling reduces the noise uniformly while noise shaping additionally pushes the noise out of the band of interest. The decimator then filters all the components out of the signal band and reduces the sampling frequency. The result is a signal coded with a large number of bits at Nyquist rate.

A significant problem in the design of $\Sigma\Delta$ modulators in practice is the estimation of their performance, since they are mixed-signal nonlinear circuits. Typically, large set of parameters have to be optimized, including the performance of the building blocks, in order to achieve the desired SNR or SNDR. Due to the inherent nonlinearity of the $\Sigma\Delta$ modulator loop, the performance optimization has to be carried out with behavioral time-domain simulations /2/. Therefore, a complete set of SIMULINK models will be presented, which allow exhaustive behavioral simulations of an arbitrary $\Sigma\Delta$ modulator, taking most of the non-idealities, such as sampling jitter, switches thermal noise and operational amplifier non-idealities (white noise, finite gain, finite bandwidth, slew-rate and saturation voltages) into account. Each of the models is presented and described. Using the presented building blocks, the simulation of any SC $\Sigma\Delta$ modulator is possible.

The basic concept of the proposed simulation environment is the evaluation of the output samples from their ideal values. The overall performance of the $\Sigma\Delta$ modulator is evaluated in the frequency domain after proper Fast Fourier Transform of the output samples.

Simulations were carried out on a classical II. order SC low-pass $\Sigma\Delta$ modulator architecture. We performed several simulations (figure 3), where only the non-idealities of the first integrator of the modulator were considered, since their effects are not attenuated by the noise shaping /2/. The simulation parameters used are summarized in table 2 and do correspond to audio standards. For audio performance, a minimum SNDR of 96 dB is required. In table 3 the SNDR with the corresponding resolution in bits of the ideal modulator is compared with results of the ideal modulator and the case when only one single non-ideality at a time and all non-idealities are introduced. In figure 11 the PSD of the ideal modulator is presented, while figures 12 and 13 compare the PSD at the output of the ideal modulator when two of the most significant non-idealities were taken into consideration. The output signal spectra show that thermal noise increases the in-band noise floor while the slew-rate produces harmonic distortion.

1 Uvod

$\Sigma\Delta$ modulacije ne moremo uvrstiti med novejšje modulatorske postopke. Predstavlja tehnologijo iz 70-tih let, katere razmah je bil pogojen šele z nedavnimi tehnološkimi inovacijami na področju digitalnega avdia in telekomunikacij.

Nizkoprepustne $\Sigma\Delta$ modulatorje uvrščamo med ustreznejše A/D pretvornike za uporabo na področju visokoločljive digitalizacije analognih signalov, katerih pasovna širina je za več razredov manjša od vzorčevalne frekvence. Ključne prednosti $\Sigma\Delta$ so v linearnosti in robustni analogni implementaciji. Ker njihova arhitektura ni prekompleksna in so relativno neobčutljivi na neidealnosti gradnikov, lahko z uporabo standardnih integriranih tehnologij dosejajo visoke ločljivosti (19-21 bitov in več) /2, 3, 4/. Zaradi omenjenih lastnosti so $\Sigma\Delta$ modulatorji razširjeni v avdio aplikacijah (za pretvorbo nizkopasovnih signalov vse do ločljivosti 20 bitov), v telekomunikacijskih sistemih (za neposredno A/D

¹ angl. switched-capacitor

² angl. slew rate

³ angl. saturation

pretvorbo moduliranih pasovno omejenih medfrekvenčnih signalov (IF^4) ter v senzorskih in merilnih vezjih.

Implementacija $\Sigma\Delta$ modulatorjev temelji na t.i. časovno-zvezni⁵ tehniki ali podatkovnem vzorčenju⁶. Najbolj pogost pristop implementacije temelji na podatkovnem vzorčenju v t.i. SC realizaciji. V nadaljevanju se bomo zato osredotočili na SC $\Sigma\Delta$ modulatorje, ki jih lahko učinkovito realiziramo v standardni CMOS tehnologiji.

Pri načrtovanju visoko zmogljivih SC $\Sigma\Delta$ modulatorjev mora načrtovalec:

- izbrati ustrezno arhitekturo modulatorja, za katero predvideva, da bo zadostila zahtevanim pogojem implementacije in
- predvideti zahteve posameznih blokov znotraj modulatorja za izbrano arhitekturo.

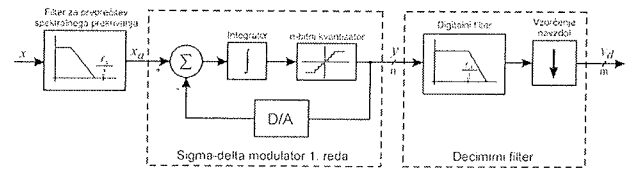
Pri zasnovi $\Sigma\Delta$ modulatorjev v praksi se pojavlja problem določitve njihovih parametrov glede na zmogljivost, saj imamo opravka z nelinearnimi kombiniranimi⁷ vezji. Zaradi nelinearnosti $\Sigma\Delta$ modulatorja mora biti optimizacija zmogljivosti izvedena s simulacijo obnašanja v časovni domeni. V primeru sistema visoke zmogljivosti je simulacija dokaj težavna. Za zadostitev zahtev sistema visokih zmogljivosti je potrebna natančna simulacija številnih neidealnosti. Prav tako je potrebna primerjava zmogljivosti različnih arhitektur za izbiro najboljše rešitve /2/.

Za zasnovo SC $\Sigma\Delta$ modulatorja visoke ločljivosti je potrebno optimizirati niz parametrov vključno z zmogljivostjo posameznih blokov v strukturi za dosego potrebnega razmerja signal-šum (SNR) ali popačitvenega SNR - SNDR⁸. Zato bomo v nadaljevanju predstavili kompleten nabor modelov v ustreznem simulacijskem okolju (SIMULINK), ki omogočajo izčrpno simulacijo obnašanja poljubnega SC $\Sigma\Delta$ modulatorja. SIMULINK je simulacijsko okolje, ki po kriterijih natančnosti, hitrosti in fleksibilnosti najustreznejše za časovne simulacije prehodnih pojavov oz. za t.i. tranzientno analizo /2/. V simulacijo so zajete najpomembnejše neidealnosti: podrtavanje vzorčevalnega signala⁹, termični šum (kT/C) ter neidealnosti operacijskega ojačevalnika (beli šum, končno ojačanje, končna pasovna širina, izhodna odzivnost in napetosti zasičenja).

2 SIGMA-DELTA modulacija

Pretvorniki s prevzorčenjem, ki temeljijo na $\Sigma\Delta$ modulaciji, so zaradi visoke ločljivosti, robustnega delovanja in nizke

občutljivosti na neidealnosti gradnikov zelo primerni za implementacijo visoko zmogljivih A/D vmesnikov v submikronski tehnologiji nizkih napetosti, kjer je načrtovanje preciznih analognih gradnikov, v primerjavi s preprosto realizacijo hitrih digitalnih vezij, težavno.



Slika 1: Blokni diagram A/D pretvornika s $\Sigma\Delta$ modulatorjem

Figure 1: ADC with $\Sigma\Delta$ modulator block diagram

Na sliki 1 je prikazan blokni diagram SD A/D pretvornika, katerega sestavni bloki so:

- a) **Filter za preprečitev spektralnega prekrivanja**, ki iz vhodnega signala odstrani spektralne komponente v frekvenčnem pasu nad polovico vzorčevalne frekvence. Prevzorčenje olajšuje načrtovanje takega filtra, saj ni potrebe po strmi prenosni karakteristiki filtra v zapornem pasu.
- b) **Modulator**. Signal se vzorči in kvantizira. Izhod modulatorja y je kodiran z nizko ločljivostjo (običajno 1 bit) pri nazivni vzorčevalni hitrosti. Modulator preoblikuje spekter šuma tako, da se velik del kvantizacijskega šuma (odvisno od reda modulatorja) nahaja izven frekvenčnega pasu filtriranega signala in ga izločimo s t.i. digitalnim filtriranjem.
- c) **Decimirni filter**. Digitalni filter izloči komponente izven frekvenčnega pasu filtriranega signala vključno z večjim deležem kvantizacijskega šuma. Filtriranju sledi vzorčenje navzdol oz. decimiranje, ki zmanjša vzorčevalno frekvenco vse do Nyquistove. Ločljivost izhodnega signala y_d se zaradi opisanega procesa poveča.

Model $\Sigma\Delta$ modulatorja lahko matematično predstavimo v z-prostoru z naslednjim izrazom:

$$Y(z) = STF(z) \cdot X(z) + NTF(z) \cdot E(z) \quad (1)$$

Funkciji $X(z)$ in $E(z)$ predstavljata z-transformaciji vhodnega signala in kvantizacijskega šuma, $STF(z)$ in $NTF(z)$ pa pripadajoči prenosni funkciji modulatorja, ločeno za vhodni signal in kvantizacijski šum. Prenosni funkciji sta pogojeni z arhitekturo modulatorja. Z vstavitvijo prenosne funkcije časovno diskretnega integratorja dobimo za izhod modulatorja 1. reda:

$$Y(z) = z^{-1} \cdot X(z) + (1 - z^{-1}) \cdot E(z) \quad (2)$$

ki je torej digitalna oblika vsote časovno zakasnjene vhoda in kvantizacijskega šuma pomnoženega s funkcijo preoblikovanja¹⁰. V časovni domeni poteka izračun kvantizacijskega šuma z odštevanjem vsakega vzorca od pred-

⁴ angl. intermediate frequency

⁵ angl. continuous-time

⁶ angl. sampled-data

⁷ angl. mixed-signal

⁸ angl. Signal to Noise Distortion Ratio

⁹ angl. sampling jitter

¹⁰ angl. shaping function

hodnega. Tako je moč kvantizacijskega šuma v nizkofrekvenčnem območju manjša, saj so razlike med sosednjimi vzorci manjše. Modulatorji višje stopnje bolj slabijo kvantizacijski šum znotraj frekvenčnega pasu signala. Za faktor prevzorčenja, ki je večji od 2, je efektivna vrednost šuma n_0 znotraj frekvenčnega območja signala določljiva z izrazom:

$$n_0 = e_{rms} \cdot \frac{\pi^L \cdot M^{L+1/2}}{\sqrt{2L+1}} \quad (3)$$

kjer je L stopnja modulatorja, M faktor prevzorčenja, e_{rms} kvantizacijska napaka A/D pretvornika $e_{rms} = \frac{q}{\sqrt{12}}$, pa kvantizacijski interval $q = \frac{A}{2^{n-1}}$. V idealnem $\Sigma\Delta$ modulatorju je razmerje signal-šum (SNR) med izhodno močjo P_s pri frekvenci vhodnega sinusnega signala in močjo P_N kvantizacijskega šuma znotraj frekvenčnega pasu signala:

$$SNR = 10 \cdot \log \frac{P_s}{P_N} = 10 \cdot \log \left(\frac{A^2/2}{n_0^2} \right) = 10 \cdot \log \left(\frac{2^{2N} \cdot 3 \cdot (2L+1) \cdot M^{2L+1}}{2 \cdot \pi^{2L}} \right) \quad [dB] \quad (4)$$

kjer je A amplituda vhodnega sinusnega signala in N število kvantizacijskih bitov. Poleg kvantizacijskega šuma prispevajo k celotnemu šumu znotraj signalnega pasu še druge neidealnosti, ki jih upoštevamo v naslednjem izrazu:

$$SNDR = 10 \cdot \log \frac{P_s}{P_N + P_D} = 10 \cdot \log \frac{P_s}{P_{N+D}} \quad [dB] \quad (5)$$

3 Neidealnosti $\Sigma\Delta$ modulatorja

V splošni teoretični analizi je edini izvor napake $\Sigma\Delta$ modulatorja zgolj kvantizacijski šum. Vendar pa zmogljivost modulatorja degradirajo še drugi vplivi (t.i. neidealnosti modulatorja), izraženi kot dodaten šum in/ali popačenje v frekvenčnem pasu signala, ki jih povzročajo razne neidealnosti v samem vezju. V praksi, še posebej ko so specifikacije zmogljivosti modulatorja zahtevne, lahko moč šuma zaradi neidealnosti preseže moč kvantizacijskega šuma, kar upravičuje pomembnost modeliranja neidealnosti v sami simulaciji modulatorja. Neidealnosti, ki vplivajo na obnašanje $\Sigma\Delta$ modulatorja lahko razčlenimo v dve skupini /5/:

- a) neidealnosti, ki povzročajo spremembe v prenosni funkciji signala (STF) in šumni prenosni funkciji (NTF). Odvisne so predvsem od arhitekture modulatorja.

Mednje uvrščamo:

- končno enosmerno (DC) ojačanje operacijskega ojačevalnika in
 - odstopanje razmerja kapacitet kondenzatorjev, ki določajo utežitev ojačanja integratorja¹¹.
- b) neidealnosti, ki jih lahko modeliramo kot izvor napake na integratorjevem vhodu in ne vplivajo na lego polov in ničel v prenosnih funkcijah modulatorja. Mednje uvrščamo:
- omejitve integratorjevega dinamičnega odziva (produkt ojačanja in pasovne širine (GBW), izhodna odzivnost, napetost zasičenja ter končno in nelinearno DC ojačanje odprte zanke),
 - termični šum ter
 - ostale neidealnosti, ki so sekundarnega pomena (podrhtavanje urinega signala, nelinearnost kapacitivnosti kondenzatorjev, histereza in zakasnitev komparatorja, nelinearnost večbitnega kvantizatorja).

Tabela 1: Neidealnosti, ki vplivajo na delovanje $\Sigma\Delta$ modulatorja

Table 1: Non-idealities degrading the performance of $\Sigma\Delta$ modulator

Gradnik	Neidealnost	Vpliv neidealnosti
Integrator	DC ojačanje	Povečan kvantizacijski šum, harmonično popačenje
	Izhodna odzivnost	Harmonično popačenje
	GBW	Napaka ustalitve ¹
	Napetost zasičenja	Preobremenitev ²
	Termični šum	Beli šum
Stikala	Upornost R_{DN} večja od 0	Napaka ustalitve, termični šum
Kondenzatorji	Nelinearnost, odstopanje abs. vrednosti	Povečan kvantizacijski šum, harmonično popačenje
Ura	Podrhtavanje	Šum podrhtavanja
Komparatorji	Histereza, zakasnitev	Povečan kvantizacijski šum
Večbitni kvantizatorji	Nelinearnost	Harmonično popačenje

Za SC realizacije $\Sigma\Delta$ modulatorja je značilno, da so vsi bloki oz. gradniki modulatorja ustrezno sinhronizirani. Z modeli, ki jih bomo predstavili, je mogoča simulacija kateregakoli SC $\Sigma\Delta$ modulatorja.

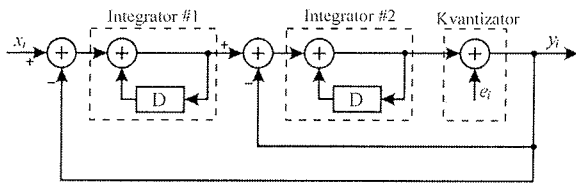
V osnovi poteka simulacija z izračunavanjem izhodnih vzorcev v časovnem prostoru. Predhodno navedene neidealnosti vplivajo na odstopanja vrednosti izhodnih vzorcev od idealnih. Parametre, ki določajo zmogljivost modulatorja, izračunamo v frekvenčni domeni s postopkom hitre Fourierjeve transformacije (FFT).

Za simulacijo neidealnosti smo izbrali klasični 1-bitni $\Sigma\Delta$ modulator II. stopnje, saj so modulatorji z enojno zanko višjih stopenj (3 in več) le pogojno stabilni. Zato se za doseganje visokih ločljivosti pri izbiri arhitekture modulatorja raje odločamo za kaskadiranje $\Sigma\Delta$ modulatorjev II. ali manjše stopnje, kot pa za izbiro arhitekture enojne zanke.

¹¹ angl. integrator weight

¹² angl. settling error

¹³ angl. overload



Slika 2: $\Sigma\Delta$ modulator II. stopnje
Figure 2: II. order $\Sigma\Delta$ modulator

Izračun SNR oz. SNDR $\Sigma\Delta$ modulatorja iz izhodnih podatkov oz. vzorcev se izvede v dveh korakih [2]. V prvem koraku izločimo sinusni signal (S) iz zaporedja N_o izhodnih vzorcev (vrednost O_i je na izhodu v trenutku t_i) z izračunom diskretne Fourierjeve transformacije (DFT) za izhodni signal (O) pri frekvenci f_{in} :

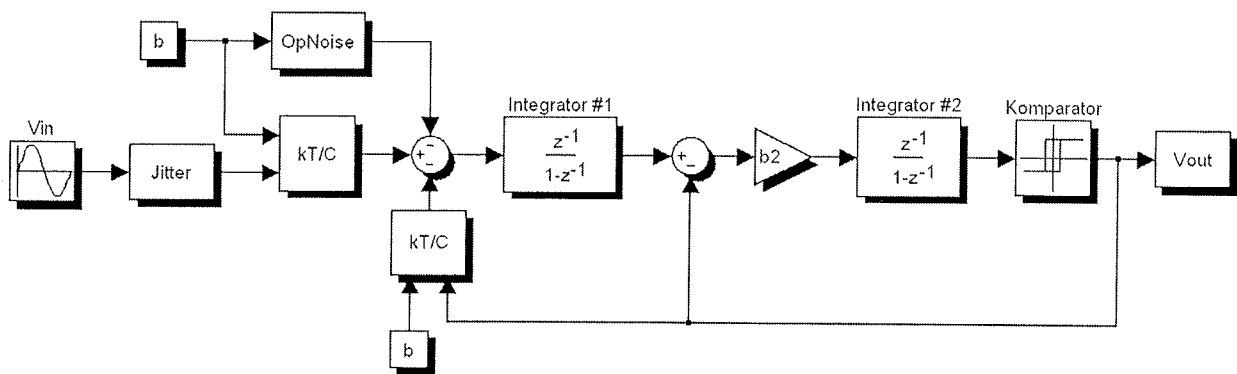
$$S(t_j) = \frac{1}{N_o} \cdot \left[\left(\sum_{i=1}^{N_o} 2O_i W_i \cos(2\pi f_{in} t_i) \right) \cdot \cos(2\pi f_{in} t_j) + \left(\sum_{i=1}^{N_o} 2O_i W_i \sin(2\pi f_{in} t_i) \right) \cdot \sin(2\pi f_{in} t_j) \right] \quad (6)$$

kjer w_i označuje funkcijo oknenja signala (ponavadi Hanningovo okno). Razlika med dobljenim in izhodnim signalom v časovni domeni je šumni signal (N_T), ki vsebuje samo šum in popačenja. V drugem koraku z uporabo FFT izračunamo spekter signala (S_S) in spekter šuma (S_{N+D}), pri čemer uporabimo enako obliko okna kot pri DFT. Končno moč signala (P_S) in šuma (P_{N+D}) dobimo z integriranjem močnega spektra signala in šuma:

$$P_S = \sum_{i=1}^{N_B} S_S^2(i) \quad \text{in} \quad P_{N+D} = \sum_{i=1}^{N_B} S_{N+D}^2(i) \quad (7)$$

kjer $N_B = N_o \cdot BW / f_s$ označuje število otipkov ustrezno zahtevani pasovni širini BW pri vzorčevalni frekvenci f_s .

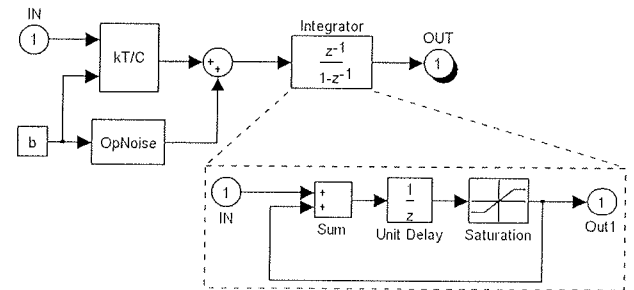
Naslednja podpoglavja podrobno opisujejo vsak posamezen model neidealnosti. Tem sledijo simulacijski rezultati, ki potrjujejo obetavnost predlaganih modelov. Vse simulacije so izvedene v programskem orodju SIMULINK na podlagi klasičnega SC $\Sigma\Delta$ modulatorja II. stopnje (slika 3).



Slika 3: Blokveni diagram SC $\Sigma\Delta$ modulatorja II. stopnje v SIMULINK-u
Figure 3: Block diagram of II. order SC $\Sigma\Delta$ modulator in SIMULINK

3.1 Šum integratorja

Najpomembnejša izvora šuma, ki vplivata na delovanje SC $\Sigma\Delta$ modulatorja sta termični šum, povezan s preklopi pri vzorčenju (preklopni šum) in notranji šum operacijskega ojačevalnika. Skupna moč šuma je vsota teoretične moči kvantizacijskega šuma, moči preklopnega šuma in moči šuma operacijskega ojačevalnika. Zaradi velikega nizkofrekvenčnega ojačanja prvega integratorja je velikost šuma $\Sigma\Delta$ modulatorja določena pretežno s preklopnim šumom in šumom operacijskega ojačevalnika vhodne stopnje.

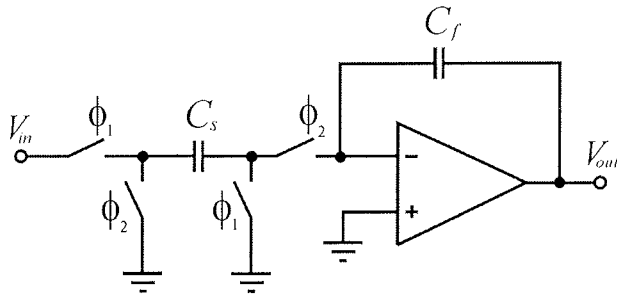


Slika 4: Model šumnega integratorja
Figure 4: Model of a noisy integrator

Te vplive lahko simuliramo s SIMULINK-om z uporabo šumnega integratorja (slika 4). Koeficient b v izrazu za prenosno funkcijo integratorja (9) predstavlja ojačanje integratorja in je glede na shemo SC integratorja na sliki 5 enak razmerju C_s/C_f . Vsak vir šuma bomo podrobneje razložili v naslednjih razdelkih.

3.1.1 Termični šum stikal

Termični šum povzroča naključno valovanje nosilcev zaradi termične energije in je prisoten tudi v stanju ravnovesja transistorja (npr. MOSFET v območju 'ON' in vrednosti toka nič). Termični šum ima t.i. beli spekter (enakovredne vrednosti amplitud spektra vsebovanih frekvenc) in široko pasovno območje, omejeno samo s časovno konstanto preklopnega kondenzatorja ali pasovno širino operacijskega ojačevalnika. Zato je potrebno upoštevati tako stikala kot operacijske ojačevalnike (OpO) v SC vezju. Vzorčevalni kondenzator C_s v SC integratorju je v zaporedni vezavi s



Slika 5: SC integrator
Figure 5: SC integrator

parom stikal (z upornostjo R_{on}), ki periodično vzorči šumno napetost na kondenzatorju. Skupno šumno moč OpO lahko določimo z integralom:

$$e_r^2 = \int_0^{\infty} \frac{4kTR_{on}}{1 + (2\pi f R_{on} C_s)^2} df = \frac{kT}{C_s} \quad (8)$$

kjer je k Boltzmanova konstanta, T absolutna temperatura, upornost pa je modelirana z zaporedno vezavo izvora šuma in izvorom moči, ekvivalentnim Johnsonovemu šumu $4kTR_{on}\Delta f$. Kljub temu, da je generator termičnega šuma upor, je skupna moč šuma odvisna zgolj od kapacitivnosti kondenzatorja C_s .

Prenosna funkcija integratorja $H_I(z)$ ni odvisna od absolutnih vrednosti kapacitivnosti, temveč od razmerja kapacitivnosti, kar je prednost SC vezij (9).

$$H_I(z) = \frac{C_s}{C_f} \cdot \frac{z^{-1}}{1 - z^{-1}} = b \cdot \frac{z^{-1}}{1 - z^{-1}} \quad (9)$$

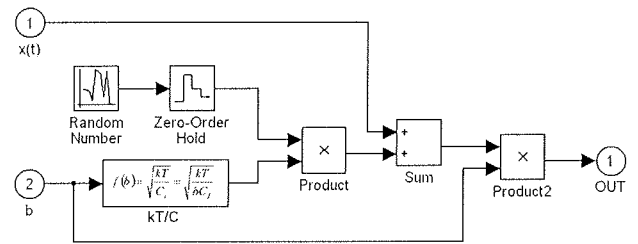
Termična šumna napetost stikala e_r (t.i. kT/C šum) je dodana k vhodni napetosti $x(t)$:

$$y(t) = [x(t) + e_r(t)] \cdot b = \left[x(t) + \sqrt{\frac{kT}{bC_f}} \cdot n(t) \right] \cdot b \quad (10)$$

kjer $n(t)$ označuje Gaussov naključni proces s standardno deviacijo, $b = C_s/C_f$ pa ojačanje integratorja. Izraz (10) je implementiran v modelu na sliki 6:

Če je pol, ki je odvisen od časovne konstante RC , pri frekvenci veliko višji kot je vzorčevalna frekvenca f_s (kar je za SC vezja ponavadi pogoj), potem lahko predpostavimo, da se ves termični šum nahaja v območju 0 do $f_s/2$. Tako je končni spekter bel s spektralno gostoto:

$$S(f) = \frac{2kT}{f_s C_s} \quad (11)$$

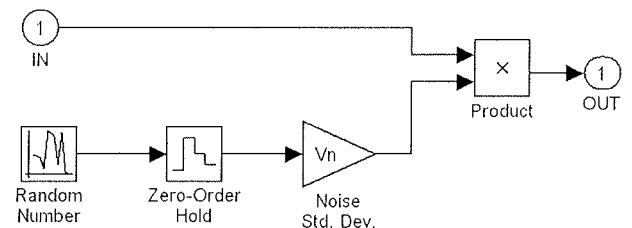


Slika 6: Modeliranje termičnega šuma stikal (blok kT/C)
Figure 6: Modeling switches thermal noise (kT/C block)

Prvi integrator ima ponavadi dva preklopna kondenzatorja na vходу. Preko prvega (C_s) vodimo na vход OpO vhodni signal, preko drugega (C_f) pa v povratni vezavi izход iz modulatorja, kjer vsak od obeh prispeva svoj delež k skupni šumni moči, zato ju modeliramo z ločenima blokoma kT/C .

3.1.2 Šum operacijskega ojačevalnika

Slika 7 prikazuje model, uporabljen za simuliranje vpliva operacijskega ojačevalnika. V_n predstavlja skupno efektivno srednjo vrednost šumne napetosti (RMS), ki se nanaša na vход operacijskega ojačevalnika. K temu prispevajo svoj delež še: šum potresavanja¹⁴ ($1/f$), širokopasovni termični šum in enosmerni odmik napetosti¹⁵. S simulacijo, prikazano na sliki 7, lahko v trenutku urinega cikla v fazi ϕ_2 (C_s na vходу OpO) z upoštevanjem vseh omenjenih šumov operacijskega ojačevalnika in integriranjem rezultirajoče vrednosti vzdolž celotnega frekvenčnega spektra določimo skupno šumno moč OpO V_n^2 .



Slika 7: Šumni model OpO.
Figure 7: Op. amp. noise model

3.2 Neidealnosti operacijskega ojačevalnika

SIMULINK-ov model idealnega integratorja z enotnim ojačanjem¹⁶ je prikazan v črtkanem bloku na sliki 4. Njegova prenosna funkcija je:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (12)$$

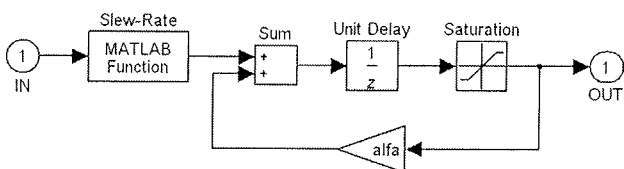
Implementacija integratorja v analognem vezju se od idealnega obnašanja razlikuje v večjih vplivih neidealnosti. Eden izmed pomembnejših vzrokov zmanjšane zmogljivosti v SC $\Sigma\Delta$ modulatorjih nastane zaradi nepopolnega pretoka naboja (energije) v SC integratorjih. Nepopoln izkoristek energije

¹⁴ angl. flicker noise

¹⁵ angl. DC offset

¹⁶ angl. unity gain

ije je posledica neidealnosti operacijskega ojačevalnika, ki ga pogojujejo omejeno ojačanje in pasovna širina, izhodna odzivnost ter napetost zasičenja. Naštete neidealnosti bomo obravnavali posamično v naslednjih razdelkih. Na sliki 8 je prikazan model realnega integratorja z upoštevanjem vseh obravnavanih neidealnosti.



Slika 8: Realni integrator
Figure 8: Real integrator

3.2.1 DC ojačanje

DC ojačanje integratorja, kot ga podaja enačba prenosne funkcije integratorja (12), je neskončno. V realnih razmerah je ojačanje seveda omejeno z določenimi omejitvami samega vezja, predvsem z ojačanjem odprte zanke OpO (A_0), ki je končno. Posledica tega so izgube v povratni zanki. Le del predhodne vrednosti izhoda integratorja (α) se doda k novi vrednosti vzorca na vhodu (slika 8). Omejeno DC ojačanje integratorja tako povečuje šum znotraj (uporabnega) frekvenčnega pasu signala. Prenosno funkcijo realnega integratorja z izgubo¹⁷ lahko zapišemo z naslednjim izrazom:

$$H(z) = \frac{z^{-1}}{1 - \alpha z^{-1}} \quad (13)$$

Enosmerno (DC) ojačanje integratorja H_0 postane:

$$H_0 = H(1) = \frac{1}{1 - \alpha} \quad (14)$$

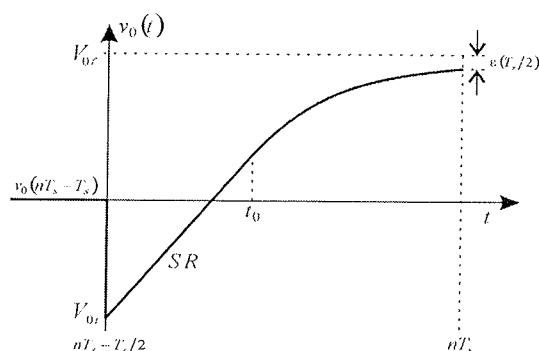
Omejeno ojačanje pri nizkih frekvencah povečuje šum znotraj frekvenčnega področja signala.

3.2.2 Pasovna širina in izhodna odzivnost

Vpliva pasovne širine (BW) in izhodne odzivnosti (SR) OpO sta neposredno povezana in ju lahko interpretiramo kot nelinearno ojačanje. V SC vezjih je njun vpliv v nepopolnem prenosu energije na izhod OpO ob koncu integracijske periode (ϵ). SR vpliva na delovanje OpO v njegovem nelinearnem področju ($t < t_0$), medtem ko je linearno področje delovanja ($t > t_0$) določeno s pasovno širino BW oz. časovno konstanto integratorja $\tau = 1/(2\pi \text{GBW})$. Ti dve področji lahko opišemo ločeno.

Slika 9 podaja izhod SC integratorja $v_0(t)$ v času n-te periode integracije (v fazi ϕ_2 urinega cikla):

$$v_0(t) = v_0(nT_s - T_s) + \alpha V_s \left(1 - e^{-\frac{t}{\tau}} \right), \quad nT_s - \frac{T_s}{2} < t < nT_s \quad (15)$$



Slika 9: Stopnični odziv integratorja
Figure 9: Integrator output step response

kjer je $V_s = V_{in}$ v začetni fazi integracije ($nT_s - T_s/2$). Naklon te krivulje (15) je največji v trenutku $t = 0$.

$$\left. \frac{d}{dt} v_0(t) \right|_{max} = \alpha \frac{V_s}{\tau} \quad (16)$$

Sedaj upoštevamo dve možnosti:

- Vrednost po en. (16) je manjša od SR OpO. V tem primeru SR ne predstavlja omejitve. Izhod integratorja je celo periodo integracije določen z en. (15).
- Vrednost po en. (16) je večja od SR OpO. V tem primeru je naklon izhodne napetosti OpO v trenutku $t < t_0$ linearen in omejen s SR. Ob predpostavki, da je $t_0 < T_s/2$, veljata naslednji enačbi:

$$t \leq t_0 : v_0(t) = v_0(nT_s - T_s) + SR \cdot t \quad (17)$$

$$t > t_0 : v_0(t) = v_0(t_0) + (\alpha \cdot V_s - SR \cdot t_0) \cdot \left(1 - e^{-\frac{t-t_0}{\tau}} \right) \quad (18)$$

Z upoštevanjem zveznosti odvodov en. (17) in (18) v trenutku t_0 dobimo:

$$t_0 = \frac{\alpha V_s}{SR} - \tau \quad (19)$$

Če je $t \geq T_s/2$, velja en. (17) celo periodo integracije. Za izračun vrednosti izhoda $v_0(t)$ v trenutku T_s , ki bo zaradi omejitve ojačanja, BW in SR različen od V_s , zgoraj navedene enačbe v simulaciji implementiramo v bloku *MATLAB function* (slika 8). Končna SR in BW povzročata harmonično popačenje, kar zmanjšuje SNDR $\Sigma\Delta$ modulatorja.

3.2.3 Napetost zasičenja

Dinamika signalov ima v $\Sigma\Delta$ modulatorjih pomembno vlogo. Zato je pomembno upoštevati izhodne nivoje zasičenja simuliranega operacijskega ojačevalnika. To lahko v SIMULINKU enostavno izvedemo z uporabo bloka 'Saturation' znotraj povratne vezave integratorja (slika 8).

Vpliv napetosti zasičenja je zanemarljiv, če izhodno območje integratorja za vsaj 50% presega območje vhodnega analognega signala /6/.

¹⁷ angl. leakage

3.3 Podrhtavanje urinega signala

Na podrhtavanje ure so najbolj občutljivi signali večjih amplitud in visokih frekvenc, saj v tem primeru prihaja do največjega odstopanja pri vzorčenju ob nepravilnih trenutkih vzorčenja. Ker SD modulatorji vzorčijo vhodni signal s frekvenco, veliko večjo od Nyquistove, vpliv podrhtavanja lahko postane v aplikacijah višjih frekvenc dominanten vir napak.

Delovanje SC vezij temelji na pretoku energije glede na urin cikel (fazi $\phi_1 - \phi_2$). Po vzorčenju vhodnega analognega signala variacija ure nima neposrednega vpliva na delovanje SC vezja. Zato je učinek podrhtavanja urinega cikla na SC vezje popolnoma opisan z vplivom na vzorčenje vhodnega signala in ni odvisen od strukture ali stopnje modulatorja /1/.

Vzorčevalni učinek podrhtavanja urinega cikla povzroča neekvidistantne trenutke vzorčenja vhoda ter posledično povečanje napake na izhodu kvantizatorja. Magnituda te napake je funkcija statističnih lastnosti podrhtavanja urinega cikla in vhodnega signala v konverter. Napaka se pojavi, kadar je sinusni signal amplitude A in frekvence f_{in} vzorčen v trenutku, ki ne sovpada z mnogokratnikom vzorčevalne periode T_s :

$$x(nT + \delta) - x(nT) \approx 2\pi f_{in} \delta A \cos(2\pi f_{in} T_s) = \delta \frac{d}{dt} x(t) \quad (20)$$

Učinek, ki ga podaja zgoraj navedeni izraz (20), lahko simuliramo v SIMULINKU z uporabo modela na sliki 10. Domnevamo, da je vzorčevalna nepravilnost δ , Gaussov naključni proces $n(t)$ s standardno deviacijo $\Delta\tau$ (gradnik 'delta' na sliki 10). Ker smo predpostavili, da je spekter učinka podrhtavanja urinega cikla 'bel', ima rezultirajoča napaka konstantno spektralno gostoto moči PSD med 0 in $f_s/2$ s skupno močjo $(2\pi f_{in} \Delta\tau A)^2/2$. V tem primeru je skupna moč napake manjša za faktor prevzorčenja M :

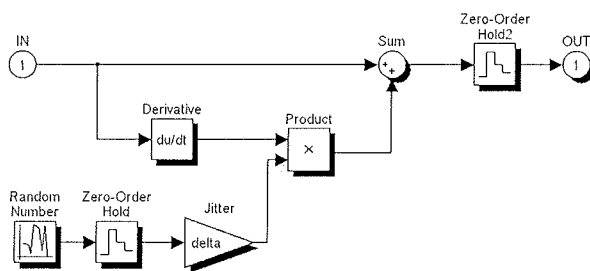
$$P_j = \frac{(2\pi f_{in} \Delta\tau A)^2}{2 \cdot M} \quad (21)$$

Zgornja meja tolerance podrhtavanja urinega cikla bi bila /6/:

$$\Delta\tau \leq \frac{\sqrt{2M/3}}{2\pi B 2^n} \quad (22)$$

4 Rezultati simulacije

Za oceno posameznih vplivov neidealnosti, ki vplivajo na delovanje SC $\Sigma\Delta$ modulatorja, smo izvedli vrsto simulacij s programskim orodjem MATLAB in SIMULINK. Simulacija je izvedena na nizkopasovnem $\Sigma\Delta$ modulatorju II. stopnje (slika 3), kjer smo upoštevali neidealnosti samo prvega integratorja v kaskadi, saj se vplivi integratorja ne zmanjšajo s preoblikovanjem šuma. Simulacijski parametri so zbrani v tabeli 1 in ustrezajo avdio standardom (zato je zahtevano razmerje SNDR določeno z 96dB, kar odgovarja ločljivosti 16 bitov).



Slika 10: Modeliranje podrhtavanja vhodnega signala

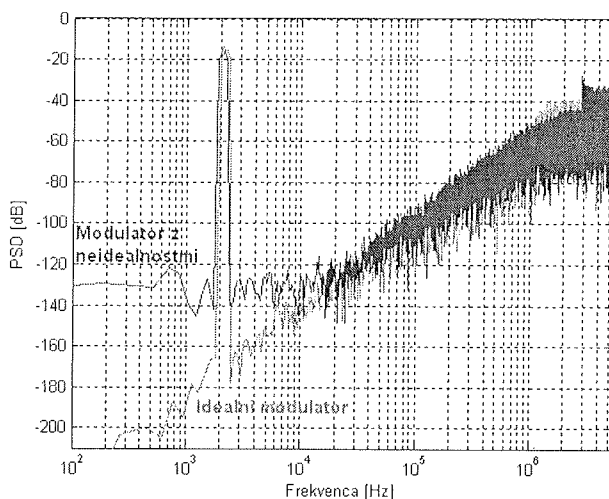
Figure 10: Modeling sampling jitter

Da bi bila simulacija smiselna, smo za navedene vrednosti posameznih neidealnosti v simulaciji načrtno izbrali vrednosti v območju realnih razmer, ki vidno vplivajo na SNDR modulatorja. Npr. za izhodno odzivnost smo izbrali vrednost $15V/\mu s$, saj je njen vpliv nad $1.1\Delta/T_s$ (v našem primeru nad $19V/\mu s$) zanemarljiv /6/.

Tabela 2: Simulacijski parametri

Table 2: Simulation parameters

Parameter	Vrednost
Pasovna širina signala	BW = 22.05 kHz
Faktor prevzorčenja	M = 256
Frekvenca prevzorčenja	$F_s = 11.2896$ MHz
Število vzorcev	N = 65536
Koeficienta integratorjev	$b = b_2 = 0.5$



Slika 11: PSD modulatorja z/brez upoštevanja neidealnosti

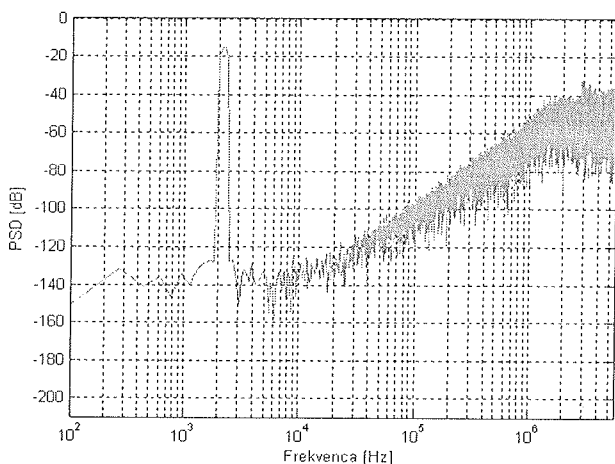
Figure 11: PSD of the modulator with and without the non-idealities

Slika 11 podaja primerjavo spektralne gostote moči (PSD) izhoda modulatorja brez/z upoštevanjem vseh obravnavanih neidealnosti. Pri amplitudi vhodnega signala -3dB je razmerje signal-šum-in-popačenje SNDR 100.7dB (16.43 bit), ob upoštevanju vseh navedenih neidealnosti pa 92.9dB

Parameter neidealnosti	SNDR _{3dB} [dB]	Ločljivost [bit]
Idealni modulator	100.7	16.43
Termični šum ($T = 300K, C_s = 5pF$)	98.2	16.02
Šum OpO ($V_n = 50\mu V$)	97.1	15.84
SR in GBW ($SR = 15V / \mu s$ in $GBW = 3MHz$)	96.1	15.67
DC ojačanje ($H_0 = 1 \cdot 10^3$)	99.9	16.31
Saturacijska napetost ($V_{max} = \pm 1.36V$)	95.9	15.64
Podrhtavanje ure ($\Delta\tau = 8ns$)	98.4	16.06
Simulacija z upoštevanjem vseh neidealnosti	92.9	15.16

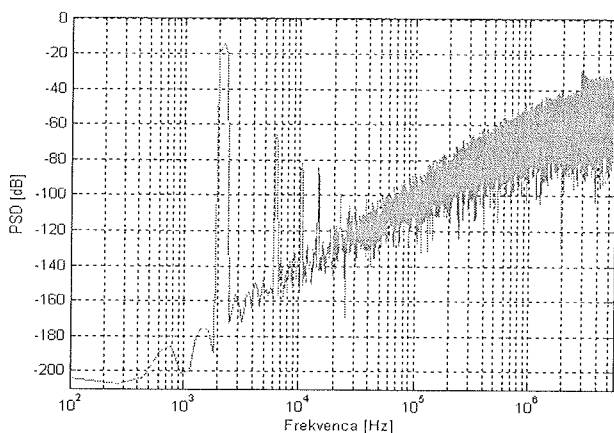
Tabela 3: Rezultati simulacije
Table 3: Simulation results

(15.16 bit). Na slikah 12 in 13 je prikazan potek PSD modulatorja, kjer smo upoštevali samo vpliv termičnega šuma oz. izhodne odzivnosti. Iz rezultatov simulacije je razvidno, da je termični šum bel in temu primerno povečuje šum v samem signalnem pasu, medtem ko povzroča izhodna odzivnost harmonično popačenje.



Slika 12: PSD modulatorja z upoštevanjem termičnega šuma

Figure 12: PSD of the modulator with thermal noise



Slika 13: PSD modulatorja s končnim SR in BW

Figure 13: PSD of the modulator with finite SR and BW

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WEAKLY IONIZED OXYGEN PLASMA

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Key words: Weakly ionised plasma, Radiofrequency plasma, Recombination, FCOP

Abstract: Weakly ionized oxygen plasma is electromagnetically induced plasma of low-pressure oxygen with a negligible density of charged particles and a relatively high degree of dissociation. The high density of atomic oxygen makes it chemically very reactive. This characteristic is used in various surface engineering applications. Neutral atoms recombine into molecules upon contact with solid surfaces. The exothermic characteristic of this reaction is utilised for determining the density of the atom gas.

Šibko ionizirana kisikova plazma

Ključne besede: šibko ionizirana plazma, radiofrekvenčna plazma, rekombinacija, FCOP

Izveček: Šibko ionizirana kisikova plazma je elektromagnetno inducirana plazma kisika pri nizkem tlaku z zanemarljivo gostoto nabitih delcev in razmeroma visoko stopnjo disociacije. Zaradi velike gostote atomarnega kisika je kemično zelo reaktivna. Ta lastnost je izkoriščena pri obdelavi površin. Ob stiku s površino atomi rekombinirajo v molekule. Eksotermen značaj te reakcije je v rabi pri določanju gostote atomarnega kisika.

1. Introduction

Plasma is often referred to as the fourth state of matter. It is also called ionized matter or ionized gas, which is more descriptive. Plasma indeed is a gas of charged particles, which are a product of ionization of the original gas, of course. It is a naturally occurring state and can be found in stars and interstellar space. Such plasma is a thermally equilibric state since the ionization is a product of very high temperature ($10^4 K$ and above). Thermal plasma can also be produced on Earth but because no material can stand the high temperature, it must be contained in magnetic fields (tokamaks). /1/

However, it is possible to create plasma at considerably lower temperatures by delivering the energy for the ionization by means of electromagnetic field. This kind of plasma (electromagnetic plasma) is not in thermal equilibrium with its surroundings, moreover, it isn't even in thermal equilibrium with itself. It is a mixture of at least two different gasses (electrons and positive ions) with different temperatures. Since this isn't a thermally equilibric state, the usual parameters used to describe a state of matter (temperature and pressure) aren't of much use and we have to turn to new ones in order to characterise the plasma. Most commonly used parameters are electron temperature (which is closely linked to the average electron kinetic energy), electron density, ion temperature and ion density.

Another important parameter of a plasma is the degree of ionization. That is the ratio of the number of the gas particles that have been ionized to the total number of the original gas particles. In the weakly ionized plasma, which is the topic of this seminar, that fraction is much smaller than unity which means that the density of charged particles is, if not negligible, at least considerably smaller than the densities of other species.

2. Electromagnetic plasma

EM plasma is created by putting low pressure gas in an electromagnetic field, either DC or AC. The principle of operation of the DC plasma, or DC discharges is that an electron source emits electrons which are accelerated by the stationary electrical field. On their way to the positive electrode, the accelerated electrons collide with other gas particles, producing new electrons.

2.1 Radiofrequency Plasma

The major disadvantage of DC systems is that an electron source is needed. This requirement is omitted by using a high frequency (above 1 MHz) EM field. The field accelerates the few free electrons in the gas which in turn produce new electrons. The intensity of the field is

$$E = E_0 \cos \omega t \quad (2.1)$$

And the force a charged particle feels is

$$m \frac{d^2 x}{dt^2} = eE \cos \omega t \quad (2.2)$$

From this we obtain the expression for its velocity:

$$\frac{dx}{dt} = \frac{eE}{m\omega} \sin \omega t \quad (2.3)$$

And finally the oscillation of the particle:

$$x = -\frac{eE}{m\omega^2} \cos \omega t \quad (2.4)$$

E[V/m]	Oscillatory amplitude [m]	Maximum velocity [m/s]	Maximum kinetic energy [eV]
10	6.110^{-5}	10^4	3.010^{-4}
100	6.110^{-4}	10^5	3.010^{-2}
1000	6.110^{-3}	10^6	3.0
10000	6.110^{-2}	10^7	3.010^2

Table 1 – behaviour of electrons in a 27.12MHz electric field /1/

We can see that even in very strong field ($10^3 V/m$) the maximum oscillatory amplitude of the electrons is relatively small, smaller than the diameter of a typical plasma vessel. Since the actual intensities in use are considerably lower (typically around $10^2 V/m$), we can safely assume that an electron isn't forced by the field to collide with the walls of the vessel.

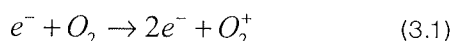
The ions on the other hand, are too massive to follow the oscillations of the electrical field and therefore can't receive any energy from it. That's why in radiofrequency plasma the ions remain at the temperature of the original gas.

2.2 Microwave discharge

With heightening of the frequency, even electrons aren't capable of following the oscillations of the field anymore and thus accumulating enough energy to cause further ionization. The only way for an electron to obtain enough energy is when its direction changes in such way that it follows the changing of the direction of the field. For that reason, the best results are achieved when the electron's oscillatory amplitude is approximately the same as its mean free path. At the frequency of 1 GHz the amplitude is 0.1 mm which corresponds with the mean free path at $10^3 Pa$.

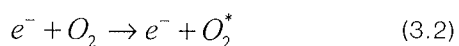
3. Collision processes

As mentioned, the EM field accelerates the electrons which collide with other gas particles. Through these collisions other plasma species are produced. The most important collision process which sustains the glow discharge is ionization. The accelerated electron transfers enough of its energy to the target atom or molecule that the atom or molecule emits another electron.



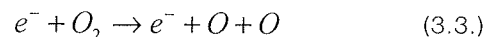
This type of collision process must be frequent enough that the production of new electrons accommodates the loss of electrons through entrapping on the walls of the plasma containing vessel.

When the accelerated electron fails to transfer enough of its energy to ionize the target atom or molecule it can still excite it.



The particle relaxes back to its ground state by emitting a photon if that is allowed by the selection rules. This is why plasma glows.

Another important process, especially for the weakly ionized plasma, is dissociation. This happens in non-noble gases, when a colliding electron brings a molecule enough energy to overcome its binding potential and break it apart.



The dissociated molecules or, plainly put, atoms, are the most important species of weakly ionized plasma. At this point it makes sense to define another plasma parameter – the degree of dissociation. This is the fraction of the original molecules that have been dissociated.

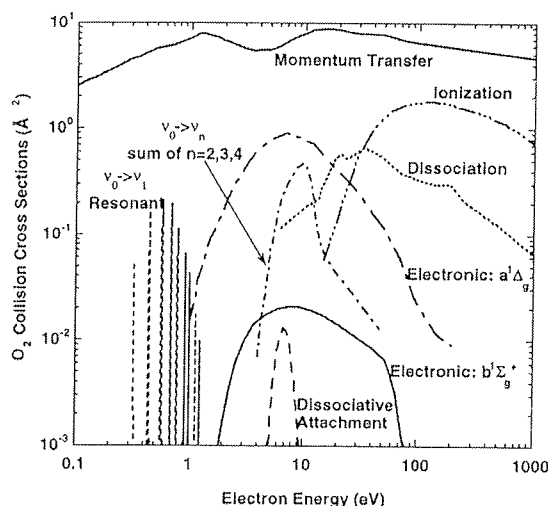


Figure 1: electron collision cross-sections in oxygen. /2/

4. Atom gas

The ionization and dissociation processes happen very roughly at the same rate (depending on the electron energy), so the production of charged particles and neutral atoms is approximately of the same value. However, the density of neutral atoms is in the range of 10% (or higher) of the original molecules while the density of charged particles is several orders of magnitude lower. This is because charged particles 'do not survive' contact with a solid surface, namely the walls of the vessel that contains the plasma. When an electron reaches a solid surface, it binds to it. Ions are more likely to receive than electron (and thus become neutral) than to bind, but in terms of the degree of ionization, the consequences are the same. Effectively speaking, charged particles disappear from the plasma upon contact with solid surfaces.

That is not the case with atoms – they see the wall as a field of potential holes, each deep several electron volts, so that once an atom is caught in such a hole, it can not get out by itself. However, there is only a limited amount of such holes and once they're all occupied (the surface is

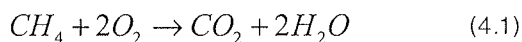
saturated), the next incoming atoms will not be caught in the holes and will bounce off the wall with great probability.

However, upon contact with solid surface atoms do recombine into molecules, but with the right choice of material for the walls, it is possible to reduce this recombination to a negligible level. Recombination inside the vessel is highly improbable because due to the conservation of momentum, this requires a simultaneous collision of at least three particles which is a very rare event in gas of low pressure.

As mentioned, the neutral atoms are the most important species of the weakly ionized plasma. Their most obvious characteristic is that they are not electrically charged and thus the EM field has no effect on them, neither do they interact with other particles over distances larger than their diameter.

From this point of view, the behaviour of the atom gas is very similar to the behaviour of the original, molecular gas. There are two main differences, however.

The first one is that the atom gas is chemically much more active than the original one. The chemical reactions that take place are still the same as those of the original gas, but they happen much more easily since the potential barrier is considerably lower. For example:



For this reaction to take place, certain energy barriers must be overcome. In the case of oxygen, the molecule must be first dissociated before the reaction can happen, which means that we must bring in enough energy to overcome the E_{dis} (5.12 eV for oxygen), the dissociation potential, usually in the form of heightening the temperature. In the atom gas, that potential barrier has already been overcome and such reactions can take place at room temperature.

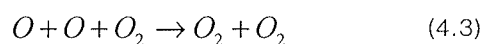
4.1 Recombination

Another important characteristic of the atoms is, as mentioned, that they recombine into molecules upon contact with solid surfaces.

Because of the law of conservation of momentum, in gas the reaction



is not possible. Because the molecule has, by definition, lower potential energy than both the atoms combined, another particle is needed to take on the surplus energy, usually in the form of kinetic energy, for example:



where the second oxygen molecule is the one to take the surplus energy. Such processes are very unlikely at the pressures in use in weakly ionized plasma technologies

(1Pa-10Pa), so the only significant recombination is the recombination that takes place on solid surfaces, namely the walls of the plasma containing vessel. There are three different ways that atoms can recombine on solid surfaces [1]:

1. Two atoms simultaneously strike upon a small area of the surface. They join into a molecule; the atoms of the surface absorb some of the surplus energy. Since there isn't enough time for accommodation, the molecule leaves the surface in a high vibrational state.
2. Atoms are bound to the surface. The atom that hits upon the surface forms a molecule with a bound atom. The bound atom is accommodated on the surface and so the resulting molecule leaves the surface in ground state or a low vibrational state.
3. Two atoms that are bound to the surface form a molecule that leaves the surface. Because both atoms are accommodated, the molecule leaves the surface in ground state or a low vibrational state.

The probability of the first kind of recombination process can be approximated as the probability that two atoms hit the same small area in a limited time range. Let's assume the area to be the size of a basic crystal cell, which is of the order of $10^{-19} m^2$. Furthermore, we can estimate the time range as the time it takes an atom to travel a distance that corresponds with a typical dimension of such a cell. The average velocity of the atoms is

$$\bar{v} = \sqrt{\frac{8kT}{\pi m}} \quad (4.4)$$

which is around 700 m/s at room temperature. That means that the time range, t , is of the order of $10^{-12} s$. The flux of the atoms to the surface is $\phi = \frac{1}{4} n \bar{v}$ and the density of atoms, n , is of the order of $10^{23} / m^3$, so the flux is of the order of $10^{23} / m^2 s$. The average number of atoms that land on that small area in that limited time range is therefore

$$\bar{N} = \Phi S t = 10^{23} / m^2 s * 10^{-19} m^2 * 10^{-12} s = 10^{-8} \quad (4.5)$$

The possibility that at least two atoms hit that part of surface in that time frame equals one minus the possibilities that either one or no atoms do so.

$$P(N \geq 2) = 1 - P(N = 0) - P(N = 1) \quad (4.6)$$

We calculate separate possibilities using the Poisson possibility distribution:

$$P(N) = \frac{\bar{N}^N}{N!} e^{-\bar{N}} \quad (4.7)$$

That gives us

$$P(N \geq 2) = 1 - e^{-10^{-8}} - 10^{-8} e^{-10^{-8}} \quad (4.8)$$

which is very close to zero. We have thus established that the first process is negligible, at least at the pressures in use (1Pa-100Pa) so the recombination must happen through the second two processes. We can sum up their effect in a quantity called the recombination coefficient. It is defined as the probability that an incoming atom recombines upon contact with surface.

Material	Recombination coefficient
Nickel	0.27
Silver	0.015 – 0.24
Stainless steel	0.0099 – 0.17
Aluminium	0.0018 – 0.01
Pyrex	$1.6 \cdot 10^{-6}$ - $2.4 \cdot 10^{-3}$
Quartz	$3.1 \cdot 10^{-5}$ - $3.2 \cdot 10^{-4}$
Teflon	$7.5 \cdot 10^{-5}$

Table 2: recombination coefficients for oxygen

It should be noted that recombination coefficients aren't the same for every gas and that they strongly depend on the roughness of surface. While this dependency has not yet been properly studied, it is believed to be the cause of large discrepancies in reported values of recombination coefficients for certain materials (up to orders of magnitude).

4.2 Lifetime of atoms in a plasma system

Once we agree that the only mechanism of loss of atoms is recombination on the walls of the plasma vessel, we can estimate the half-life of an atom.

The probability that an atom survives a collision with the wall is

$$P_1 = 1 - \gamma \tag{4.9}$$

For N collisions, that probability is

$$P(N) = (1 - \gamma)^N \tag{4.10}$$

To calculate that probability as a function of time, we must first estimate how many times an atom hits upon the wall in unit time. Let us suppose that our plasma vessel is a cylindrical tube with the radius r and the length L . If the density of the atoms is n , then the total number of atoms in the vessel is

$$T = nV \tag{4.11}$$

where the volume of the vessel is $V = \pi r^2 L$. The flux of atoms to the surface is

$$\phi = \frac{1}{4} \bar{v} n \tag{4.12}$$

and the total number of atoms that hit the surface in unit time is

$$F = \phi S = \frac{1}{4} \bar{v} n (2\pi r L) \tag{4.13}$$

The ratio F/T is the average number of times an atom hits a surface in unit time:

$$\frac{dN}{dt} = \frac{F}{T} = \frac{\frac{1}{4} \bar{v} n 2\pi r L}{n\pi r^2 L} = \frac{\bar{v}}{2r} \tag{4.14}$$

Now we can write down the probability that an atom hasn't recombined after the length of time t :

$$P(t) = (1 - \gamma)^{\frac{\bar{v}t}{2r}} \tag{4.15}$$

At room temperature, the average speed for oxygen atoms is around $\bar{v} = 700 \text{ m/s}$. Let us take a look what happens in a glass tube ($\gamma = 10^{-4}$) with the radius $r = 5 \text{ cm}$.

t[s]	P
1	0.993
10	0.932
100	0.497

Table 3: Probabilities of recombination in a glass tube $\gamma = 10^{-4}$

We can see that it is more likely for an atom to be pumped out of the plasma system than to recombine on the walls. However, if we make the vessel of a material that is a good catalyst ($\gamma = 0.1$), then we get drastically different results.

t[s]	P
1	0.000627
0.1	0.478
0.01	0.929

Table 4: Probabilities of recombination in tube of a catalytic material, $\gamma = 0.1$

The chance that an atom hasn't recombined after in a second's time is practically zero. We see that with by choice of material for the plasma containing vessel, we can assure either decent stability of the atom gas, or the completely opposite result.

5 Measuring atom density

As mentioned, various parameters are used to characterize plasma. In weakly ionized plasma the most important parameter is the degree of dissociation or more simply put, density of the atom gas.

There are various methods available for determining atom density in plasma /3/:

- NO titration
- mass spectrometry
- optical emission spectrometry
- optical absorption spectrometry
- catalytic probes

Among the mentioned methods, optical absorption spectrometry is the one that is the most accurate. It is however a very demanding method and as such isn't always available. The catalytic probes aren't as accurate as optical absorption spectrometry, but they are a much more convenient technique. While the rest of the mentioned methods can only be used to determine the order of magnitude of the atom density, the catalytic probes can yield accuracy as good as 30%.

5.1 Catalytic probes

A catalytic probe is basically a small piece of metal submerged in the plasma /4/. It utilizes the exothermic characteristic of the recombination reaction



The metal acts as a catalyst for recombination. The greater the rate of recombination is, the more the probe is heated. Atom density can be determined by observing the temperature of the probe. The choice of metal depends on the type of gas atoms we want to measure. A certain metal can act as an excellent catalyst for one gas but be completely inactive in another. For measuring the density of atoms in oxygen plasma, for example, the most widely used metal is nickel.

As mentioned, the probe is heated by atoms recombining on its surface, which can be expressed as

$$P_{heat} = \frac{1}{4} S n \bar{v} \gamma E_{dis} \quad (5.2)$$

where P_{heat} stands for the heating power, S for the surface of the probe, \bar{v} for the average velocity of the atoms and n for the density of the atoms. The recombination coefficient of the metal is represented by γ , E_{dis} is the dissociation energy that is released with each two atoms that recombine into a molecule. This value is 5.12eV for oxygen, for example.

When the temperature of the probe is constant, it means that the heating power and the cooling power are closely

matched. The probe is cooled by various processes, of which thermal conductivity of the surrounding gas is the predominant. The cooling power is difficult to calculate because it depends of many parameters which aren't always very well known. However, by observing the decline of the temperature immediately after the plasma is switched off, it can be evaluated as:

$$P_{cool} = m c_p \frac{dT}{dt} \quad (5.3)$$

In this expression, m stands for the mass of the metal part of the probe, c_p is the thermal capacity of the metal and $\frac{dT}{dt}$ is the steepest part of the temperature curve after the plasma has been switched off. By switching plasma off we mean that the EM field is switched off and the atom density rapidly falls to zero.

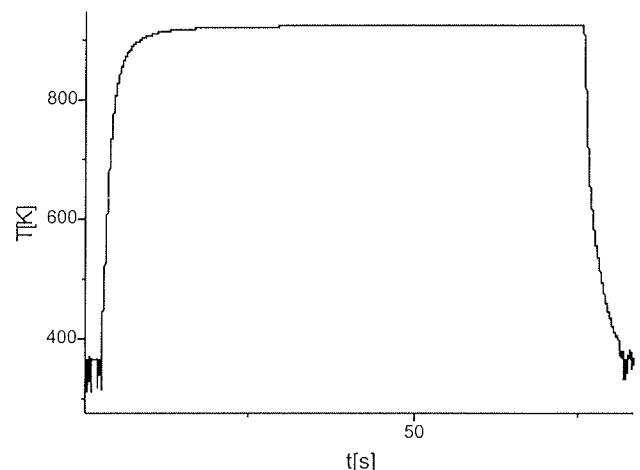


Figure 2: Determining atom density through observation of probe temperature. Temperature plot of a measurement of atom density.

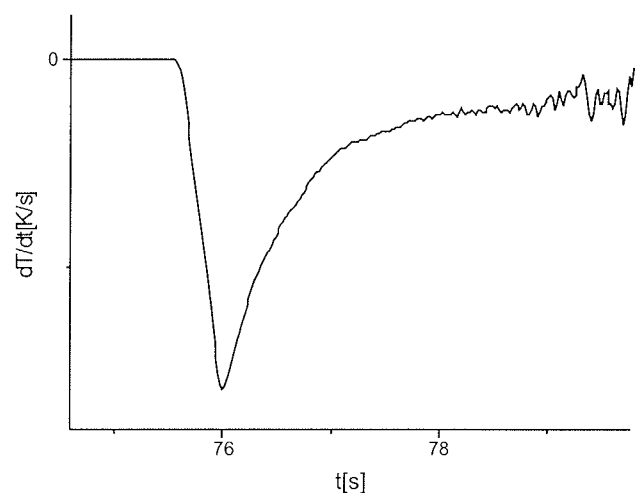


Figure 3: Time derivate of the temperature of the probe, the cooling part of the slope.

The early designs of the catalytic probe included a metal disk attached to thermocouple wires as its essential component. A more advanced design is the Fiber Optic Catalytic Probe. Here the metal disk is substituted by a small piece of metal foil closely wrapped around a small glass sphere (typical diameter is about 0.3 mm) which is attached to an optic fiber. As the foil heats, it emits radiation, which is transmitted through the fiber to an optoelectronic detector, where it is transformed to an electrical one. /5/

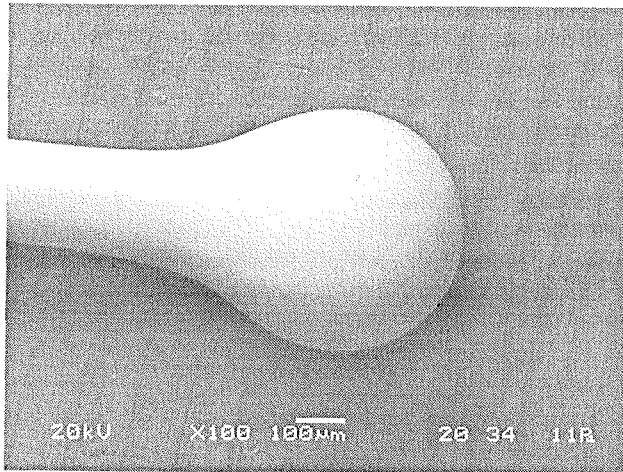


Figure 4: Tip of the FCOP

The advantage of this design to the thermocouple one is that the probe causes less of a disturbance in the surrounding atom gas density because the characteristic dimensions of the metal are much smaller. Furthermore, because the signal is an optical one, it is unaffected by electromagnetic interferences which are quite strong in a radiofrequency system. /6/

However, the catalytic probe has certain limitations, especially the FCOP design. Because the signal to noise ratio worsens considerably at lower temperatures (around 400K), it is impossible to measure very low concentration. On the other hand, at high concentration of the atoms, the temperature is so high that the optical signal exceeds the operational range of the optoelectronic detector (signal overflow). Although this can be improved by replacing the detector for a one with a more suitable range of operation, the limitation still remains because extremely high temperatures (well above 1000K) can destroy the probe.

These limitations could be overcome if the probe was retracted along a dead end tube, which should be closed with a metal part with a very high recombination coefficient. That would mean that the density of atoms at the end of the tube would be zero while the density at the beginning of the tube would be the same as in the main plasma vessel. By knowing the density distribution along the tube, it would be possible to determine the density of atoms in the main vessel by measuring a much lower density inside the dead end tube and thus to expand the working range of the probe.

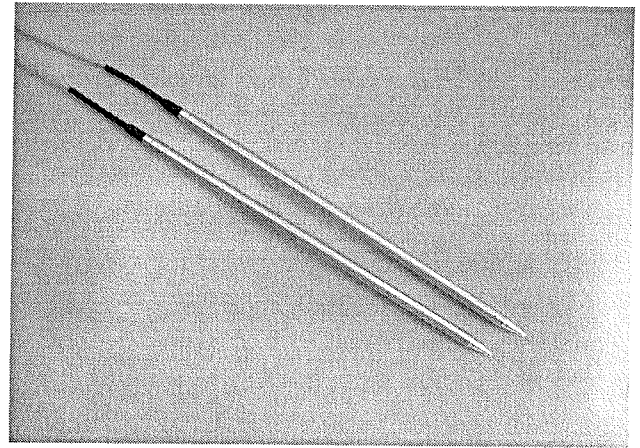


Figure 5: A pair of Fiber Optic Catalytic Probes

6 An example of a simple RF plasma system

This is a simple plasma system located in the plasma lab of the F4 department of IJS. The plasma containing vessel is an around half a meter long glass tube with the diameter of 4 cm. The system is pumped with a two-stage rotary pump which is capable of creating maximum flux of $28m^3/h$. Plasma is produced by means of a 700W radiofrequency generator which is inductively coupled with the plasma. The tube itself is replaceable which allows various variations of system setup. This usually means the choice between a tube that is uniform in diameter or one that has a short (around 5 cm) narrow (diameter of 1 cm) part in the middle. This part separates the 'glow' vessel and the 'post-glow' vessel. The coil of the generator is wound around the glow vessel – here the plasma is created. The narrow part ensures that no charged particles come to the post-glow vessel. That is because the charged particles bind to the walls upon contact and by forcing the plasma to pass through the narrow part, the chance of charged particles reaching the wall of the vessel improves dramatically. The tube also forks out into smaller side tubes through which probes or specimens to be processed are installed.

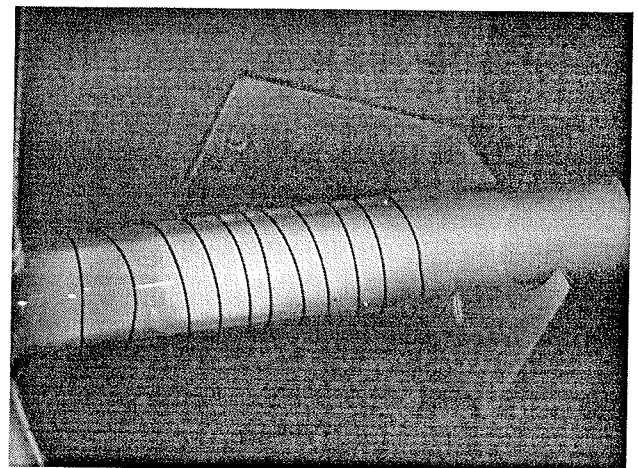


Figure 6: Photograph of a RF glow discharge.

Because this system is relatively small it is primarily intended for research of plasma behaviour rather than mass specimen treatment.

7 Conclusion

We have characterized weakly ionized oxygen plasma as a mixture of molecular and atom oxygen gasses. The relatively high share of atoms in the mixture makes such plasma chemically very reactive and thus suitable for surface engineering. Atoms recombine into molecules upon contact with solid surface. The recombination coefficient is different for each material, which has to be taken into account when constructing the plasma containing vessel. We have also shown a very successful method for measuring the density of the oxygen atoms.

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GNEZDENI GENETSKI ALGORITMI PRI DOLOČANJU PARAMETROV JILES-ATHERTON HISTEREZNEGA MODELA MEHKOMAGNETNIH KOMPOZITNIH MATERIALOV

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Ključne besede: Jiles-Atherton model, mehkomagnetni kompozitni material, genetski algoritmi

Izveček: Delo obravnava izpeljavo, določitev parametrov in uporabo Jiles-Athertonovega modela (J-A model) histerezne zanke mehkomagnetnega kompozitnega (SMC) materiala. Določitev parametrov J-A modela histerezne zanke je osnovana na merjenih histereznih zankah z uporabo genetskih algoritmov. Genetski algoritmi operirajo v določenem obsežnem ampak omejenem področju možnih rešitev. Možnost, da najdejo najboljšo rešitev danega problema v takšnem iskalnem področju je zelo negotova. Nov pristop optimizacije z gnezdjenimi genetskimi algoritmi omogoča zmanjšanje mej obsežnih iskalnih območji. Osnova tega pristopa je, da v genetski algoritem iskanja optimalnih mej iskalnih področji vgradimo genetski algoritem iskanja parametrov J-A modela. Opisan optimizacijski postopek smo poimenovali *GgaA*. Primerjava merjenih rezultatov in rezultatov iz optimiranega J-A modela potrjuje dobro delovanje novega optimizacijskega postopka na podlagi tako imenovanega *GgaA* algoritma.

Nested Genetic Algorithms in Determination of Jiles-atherton Hysteresis Model Parameters for Soft-magnetic Composite Materials

Key words: Jiles and Atherton hysteresis model, soft magnetic composite material, genetic algorithms

Abstract: The paper reports the principle of derivation, parameter determination and use of Jiles and Atherton hysteresis model (J-A model) for soft magnetic composite (SMC) material. The calculation of Jiles and Atherton hysteresis model parameters is based on experimental data and genetic algorithms. Genetic algorithms operate in a given extensive but bounded area of possible solutions. To find the best solution of a problem in this area of possible solutions is uncertain. To overcome this uncertainty a new approach in use of genetic algorithms is proposed. The basis is in genetic algorithms nesting. This means one genetic algorithm built in another genetic algorithm. The procedure is named *GgaA*. Comparison between experimental results and results from optimized J-A hysteresis model confirm a proper functionality of new optimization procedure based on nested genetic algorithms.

1 Uvod

Matematični model histerezne zanke, ki sta ga vpeljala Jiles in Atherton (J-A model) bazira na fizikalnem dogajanju v feromagnetnem materialu in ne izključno na matematičnem ali eksperimentalnem prilagajanju histerezne zanke $/1/$, $/2/$.

2 Model histerezne zanke

V J-A modelu se celotno magnetizacijo M (en. 4) feromagnetnega materiala razdeli na nepovratno M_{irr} (en. 2) in povratno M_{rev} (en.3) komponento magnetizacije.

Deviška magnetilna krivulja M_{an} (histerezna zanka, če izgub ne bi bilo) je opisana z Langevinovo funkcijo:

$$M_{an} = M_s \left[\coth \left(\frac{H + \alpha M}{a} \right) - \frac{a}{H + \alpha M} \right] \quad (1)$$

Nepovratna komponenta magnetizacije M_{irr} je povezana z energijskimi izgubami zidov domen, ki so vpeti v nečistoče materiala:

$$\frac{dM_{irr}}{dH} = \frac{M_{an} - M_{irr}}{k\delta - \alpha(M_{an} - M_{irr})} \quad (2)$$

Povratna komponenta magnetizacije M_{rev} predstavlja delež povratnih procesov premikanja domen in njihovih zidov. V modelu ima naslednjo obliko:

$$M_{rev} = c(M_{an} - M_{irr}) \quad (3)$$

Celotna magnetizacija M je vsota komponent nepovratne M_{irr} in povratne M_{rev} magnetizacije:

$$M = M_{rev} + M_{irr} \quad (4)$$

Enačbo 4 nadalje preoblikujemo na ta način, da M_{rev} nadomestimo z (en. 3) in dobimo:

$$M = (1 - c)M_{irr} + cM_{an} \quad (5)$$

kar nas pripelje do celotne diferencialne susceptibilnosti magnetizacije dM/dH :

$$\frac{dM}{dH} = (1 - c) \frac{M_{an} - M_{irr}}{k\delta - \alpha(M_{an} - M_{irr})} + c \frac{dM_{an}}{dH} \quad (6)$$

Pet osnovno odvisnih parametrov, ki se pojavijo v (en. 1) in (en. 6) so:

- M_s - nasičenost magnetizacije
- a - parameter oblike,
- α - parameter glavnega polja,
- k - konstanta vpetja zidov domen v nečistoče materiala, proporcionalna histereznim izgubam,
- c - konstanta napihovanja domen.

Parameter δ nima fizikalnega pomena in ima vrednost +1 ko je $dH/dt > 0$ in -1 v nasprotnem primeru.

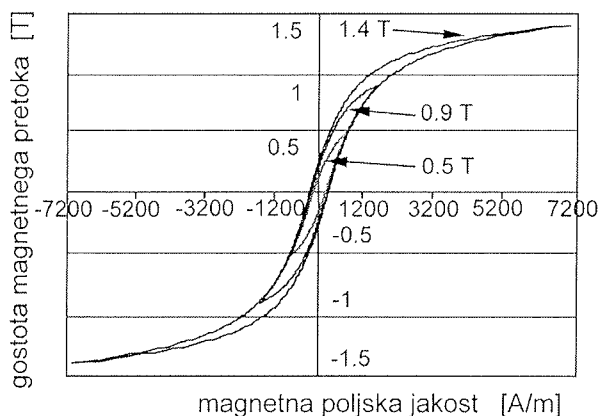
Diferencialno enačbo (en. 6) rešimo z uporabo numerične metode. Rešitve nato uporabimo za izračun gostote magnetnega pretoka B :

$$B = \mu_0(H + M) \quad (7)$$

Za določitev vrednosti petih parametrov J-A histereznega modela uporabimo merilne rezultate histereznih zank in numerične optimizacijske postopke. V našem primeru smo uporabili genetske algoritme, katere bomo v nadaljevanju tudi opisali.

3 Merilni rezultati histereznih zank

Slika 1 prikazuje merjene statične histerezne zanke /3/ za mehkomagnetni kompozitni material.



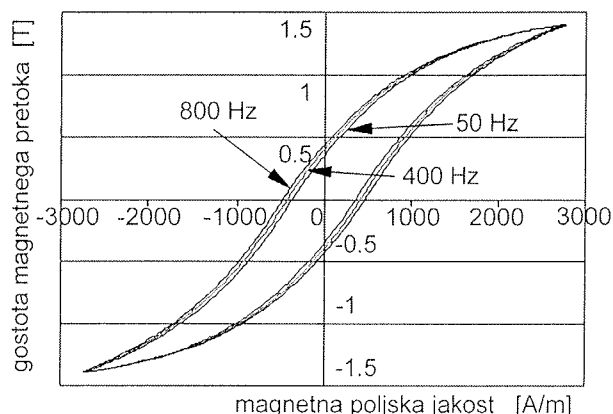
Slika 1. Merjene statične histerezne zanke pri različnih vrednostih gostote magnetnega pretoka.

Merjene statične histerezne zanke (slika 1) ne vsebujejo odziva materiala na izmenično magnetno vzbujanje. S tem pa tudi ne izgub zaradi vrtilčnih tokov in tako imenovanih dodatnih izgub. Merjene vrednosti statičnih histereznih zank pri različnih vrednostih maksimalne gostote magnetnega pretoka bodo uporabljene pri določanju parametrov J-A modela.

Histerezne zanke merjene pri različnih frekvencah vzbujanja in različnih maksimalnih vrednostih magnetizacije /3/ vsebujejo poleg histereznih izgub tudi izgube zaradi vrtilčnih tokov in dodatne izgube.

Na sliki 2 so za mehko magnetni kompozitni material prikazane merjene histerezne zanke pri različnih frekvencah vzbujanja in maksimalni vrednosti gostote magnetnega pretoka 1.4 T.

Razlika v površini med statično histerežno zanko in zankami pri različnih frekvencah kaže na prisotnost izgub zaradi vrtilčnih tokov in dodatnih izgub.



Slika 2. Merjene histerezne zanke pri različnih frekvencah vzbujanja in maksimalni vrednosti gostote magnetnega pretoka 1.4 T.

Na podlagi razlike površin histereznih zank s slike 1 in slike 2 pri isti maksimalni vrednosti gostote magnetnega pretoka lahko zaključimo, da je v mehko magnetnem kompozitnem materialu zelo malo vrtilčnih in dodatnih izgub. To pa seveda izhaja iz same zgradbe materiala /4/.

4 Ovrednotenje parametrov J-A modela z genetskimi algoritmi

Vrednosti parametrov J-A histereznega modela smo določili z uporabo genetskih algoritmov (GA). Genetski algoritem je optimizacijski proces, ki je osnovan na konceptu naravne selekcije in genetike /5/. Algoritem začnemo izvajati s skupkom možnih rešitev - osebkov, ki jih imenujemo začetna populacija (slika 3). Ta populacija ima naključno izbrane vrednosti parametrov.

Rešitve modelov dobljene na podlagi začetne populacije uporabimo za kreiranje nove populacije z upanjem, da bo nova populacija boljša od predhodne. Novo populacijo ustvarimo z uporabo genetskih operatorjev: selekcije, križanja in mutacije. Osebkki trenutne populacije, ki bodo sestavljali novo populacijo so izbrani glede na njihovo oceno kvalitete opisa merjene histerezne zanke s samim J-A modelom. Same lastnosti osebkov trenutne populacije, ki se bodo prenesle v naslednjo generacijo pa so podvržene genetskim operatorjem. To se generacijsko ponavlja toliko časa, dokler ni izpolnjen pogoj za zaustavitev genetskega algoritma (npr. število generacij ali izpolnitev minimalnih zahtevanih pogojev).

Z GA lahko optimiramo zvezne ali diskretno opisane sisteme, poleg tega lahko tudi rokujemo z numerično pridobljenimi podatki, merjenimi podatki ali analitičnimi funkcijami.

Uporabo genetskih algoritmov pri iskanju parametrov J-A modela bomo obravnavali v nadaljevanju.

4.1 Določanje vrednosti parametrov J-A modela

Vrednosti snovno odvisnih parametrov potrebnih za pravilen opis histerezne zanke z J-A modelom (en. 6) smo določili za statične histerezne zanke. Pri tem smo uporabili merjene vrednosti s slike 1.

Sestava populacije z osebki predstavljenimi z nizom parametrov J-A modela uporabljena v optimizacijskem procesu z genetskimi algoritmi je prikazana na sliki 3.

$$pop = \begin{bmatrix} a_1 & \alpha_1 & k_1 & M_{s,1} & c_1 & ocena_1 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ a_n & \alpha_n & k_n & M_{s,n} & c_n & ocena_n \end{bmatrix}$$

n – število možnih osebkov – rešitev.

Slika 3. Zgradba populacije

Posamezna vrstica populacije predstavlja osebek sestavljen iz parametrov J-A modela. Posamezen parameter predstavlja enega od genov osebka. K vsakemu osebku pa se pripiše še njegova ocena. Ocena osebka predstavlja ocenitev posameznika (osebka) glede na izbrano vrednotenje posameznika (npr. vsota kvadratov napake – SSE). V našem primeru smo vrednotenje osebka izbrali kot razliko med merjeno in izračunano gostoto magnetnega pretoka pri istem vzburjanju :

$$ocena = - \left| \sum_{i=1}^n (B_{m,i} - B_{c,i}) \right| \quad (8)$$

B_m – merjena gostota magnetnega pretoka,

B_c – izračunana gostota magnetnega pretoka s pomočjo J-A modela,

n – število meritev.

GA iščejo najboljšo rešitev izmed možnih rešitev (za vsak parameter posebej) z uporabo operatorjev GA (križanje, selekcija in mutacija). Področje možnih rešitev je omejeno z vrednostmi zgornje in spodnje meje (tabela 1). Če globalni optimum obstaja v tem področju ga GA morajo najti.

S pomočjo začetne populacije (slika 3), vrednotenja posameznega osebka in določitev njegove ocene (en. 8) ter izbranega področja iskanja (tabela 1) parametrov smo izvedli optimizacijski postopek določanja parametrov J-A modela. Postopek je bil izveden s 40 osebki v 100-tih generacijah za merjeno histerežno zanko z maksimalno gostoto magnetnega pretoka 1.4 T. Rezultati so podani v tabeli

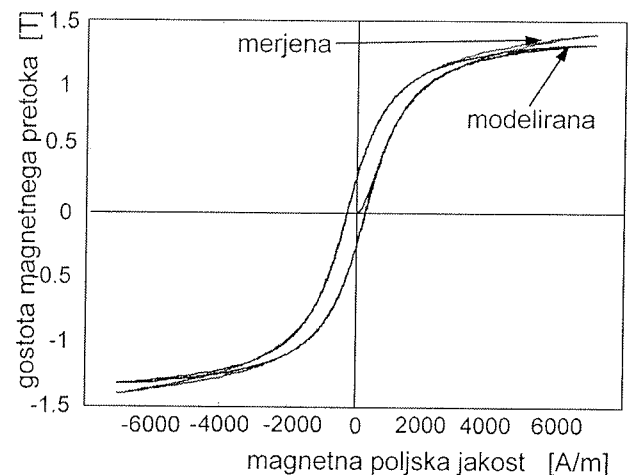
2 ter grafično prikazani v obliki optimirane histerezne zanke J-A modela na sliki 4.

Parametri J-A modela	Zgornja meja iskalnega področja	Spodnja meja iskalnega področja
a	2000	100
α	0.002	0.0001
k	2500	100
M_s	$1.7 \cdot 10^6$	$1 \cdot 10^6$
c	0.3	0.01

Tabela 1. Mejne vrednosti iskalnega področja GA za merjeno statično histerežno zanko $B_m = 1.4 T$

Parametri J-A modela	Optimirane vrednosti
a	694,684
α	0,000614
k	320,873
M_s	1149531,87
c	0,1469

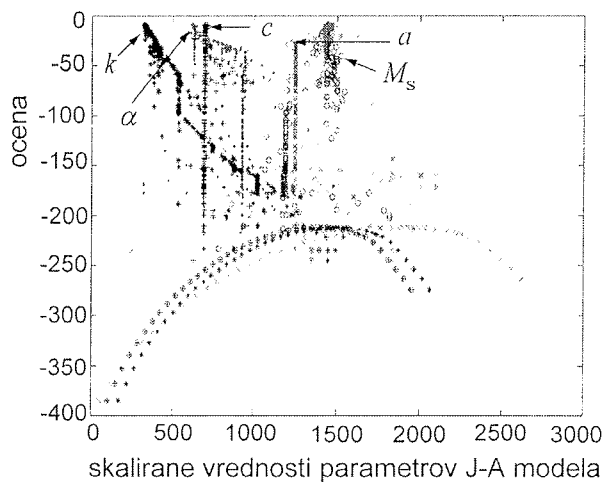
Tabela 2. Optimirane vrednosti parametrov J-A modela za merjeno statično histerežno zanko pri $B_m = 1.4 T$



Slika 4. Optimirana histerezna zanka z GA za merjeno statično histerežno zanko pri $B_m = 1.4 T$.

S slike 4 lahko vidimo, da GA ni našel globalnega optima ampak le neki lokalni optimum. Za ugotavljanje razloga tega problema smo opravili analizo konvergence rešitev posameznih parametrov. Konvergenca parametrov J-A modela glede na doseženo oceno je prikazana na sliki 5.

Iz konvergence parametrov k , M_s in a (slika 5) lahko izluščimo, da je trenutno določeno področje iskanja (tabela 1) za te parametre preozko. To pomeni, da globalni optimum ne obstaja v tem določenem področju iskanja. Drugi možen razlog slabih rezultatov je premajhno število osebkov in generacij glede na operatorje GA (počasna konvergenca).



Slika 5. Konvergenca parametrov J-A modela glede na oceno.

Če področje iskanja razširimo morajo GA operirati z večjim številom osebkov in generacij (podaljša se čas računanja), saj le tako lahko pričakujemo dobre rezultate (GA morajo preiskati celotno področje iskanja). Po drugi strani, če pa zožimo področje iskanja lahko izgubimo globalni optimum. Pri tem pa seveda potrebujemo manj osebkov in manj generacij (hitra konvergenca) za celoten optimizacijski postopek.

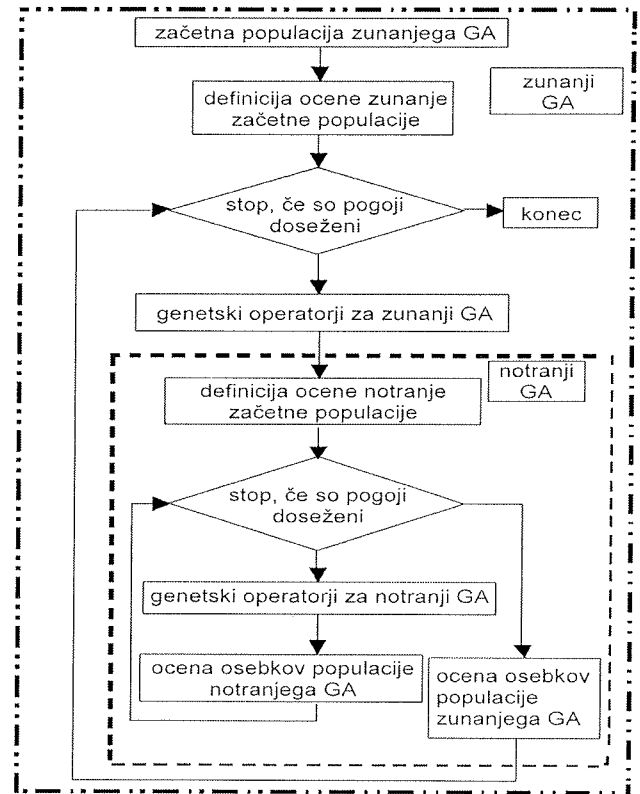
Glede na izpostavljene probleme predlagamo nov način optimizacijskega postopka na podlagi GA. Uprabnost tega načina je predvsem pri določanju globalnega optimuma s širokimi področji možnih vrednosti iskanih parametrov. Glavna ideja je, da uporabimo genetski algoritem, kateri je vgrajen v drugi genetski algoritem. Poimenovali smo ga z *GgaA*. Diagram poteka *GgaA* algoritma je prikazan na sliki 6.

Glavna lastnost *GgaA* je, da zunanji GA poišče optimalno zgornjo in spodnjo mejo področja iskanja, medtem, ko notranji GA zunanemu določa oceno osebka. Dejstvo je, da je na ta način iz širokega iskalnega področja izvečeno področje, ki vsebuje globalni optimum.

Osebek populacije zunanjega GA je sestavljen iz enajstih genov med katerimi prvih deset predstavlja zgornjo in spodnjo mejo iskalnega področja, zadnji pa oceno osebka. Na primer, prvi gen osebka predstavlja zgornjo mejo področja parametra *a*, drugi gen predstavlja spodnjo mejo področja parametra *a* in na enak način še za ostale parametre.

Notranji GA uporablja 40 osebkov in 100 generacij. To število osebkov in generacij je izbrano, zato ker je iskalno področje notranjega GA ozko in se pričakuje, da bo našel optimum za vsa iskalna področja (hitra konvergenca) podana z zunanjim GA. Določitev ocene osebka zunanjemu GA notranji GA poišče najboljše parametre J-A modela za trenutno iskalno področje. Pri tem uporablja merjene statične histerezne zanke in vrednotenje osebka z (en. 8).

Notranji GA je uporabljen tudi ob koncu, kadar so pogoji zaustavitve *GgaA* izpolnjeni (število generacij zunanjega



Slika 6. Diagram poteka *GgaA*.

GA). V tem primeru notranji GA optimira končne vrednosti parametrov J-A modela z optimiranimi zgornjimi in spodnjimi mejami iskalnega področja dobljenimi z zunanjim GA.

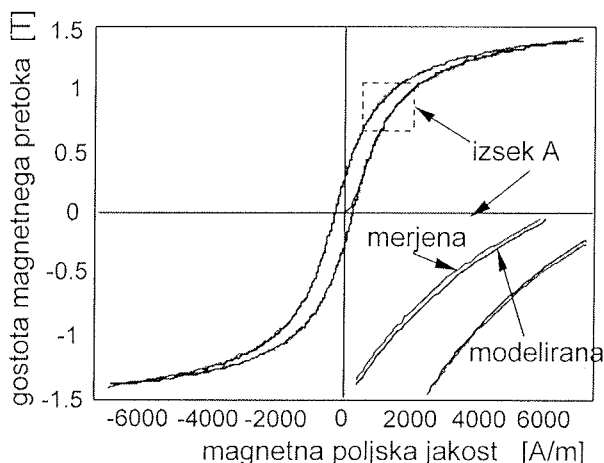
Nov pristop optimizacije z uporabo *GgaA* je bil izveden pri optimizaciji parametrov J-A modela z merjeno statično histereznim zanko z maksimalno gostoto magnetnega pretoka 1.4 T. Rezultati so predstavljeni v tabeli 3 in tabeli 4 ter grafično prikazani na sliki 7 v obliki optimirane statične histerezne zanke z J-A modelom.

Parametri GgaA	Meje iskalnega področja GgaA
<i>a</i> zgornja meja	4000 ÷ 1950
<i>a</i> spodnja meja	1950 ÷ 100
α zgornja meja	0,004 ÷ 0,00195
α spodnja meja	0,00195 ÷ 0,0001
<i>k</i> zgornja meja	4000 ÷ 1950
<i>k</i> spodnja meja	1950 ÷ 100
<i>Ms</i> zgornja meja	$2,4 \cdot 10^6 \div 10^6$
<i>Ms</i> spodnja meja	$10^6 \div 0,4 \cdot 10^6$
<i>c</i> zgornja meja	0,3 ÷ 0,1475
<i>c</i> spodnja meja	0,1475 ÷ 0,005

Tabela 3. Meje iskalnega področja za *GgaA* glede na merjeno statično histereznim zanko pri maksimalnem $B_m = 1.4 T$

parametri J-A modela	Meje iskalnega področja optimirane z GgaA	Optimirane vrednosti z notranjim GA
<i>a</i>	1974.577 ÷ 124.577	1188,541
α	0,00197 ÷ 0,000121	0,001633
<i>k</i>	1974.577 ÷ 137.744	322,618
<i>Ms</i>	$1,6 \cdot 10^6 \div 0,9 \cdot 10^6$	$1,268 \cdot 10^6$
<i>c</i>	0,2479 ÷ 0,04657	0,2220997

Tabela 4. Optimirane vrednosti parametrov J-A modela glede na merjeno statično histerezno zanko pri maksimalnem $B_m = 1.4 T$ z uporabo GgaA.



Slika 7. Rezultati optimizacije GgaA glede na merjeno statično histerezno zanko pri maksimalnem $B_m = 1.4 T$ z uporabo GgaA.

S slike 7 lahko vidimo, da se modelirana histerezna zanka zelo dobro prilega merjeni. S tem je potrjeno dobro delovanje novega optimizacijskega postopka na podlagi tako imenovanega GgaA algoritma.

5 Zaključek

Določitev parametrov J-A modela s pomočjo genetskih algoritmov za SMC material je učinkovita metoda, če že vnaprej poznamo meje iskalnega področja, to pomeni, da poznamo okvirne vrednosti rešitev. Če pa teh okvirnih vrednosti rešitev ne poznamo in operiramo s širokim iskalnim področjem nam uporaba gnezdenih genetskih algoritmov (GgaA) daje dobre rezultate. To je razvidno tudi iz slike 7,

saj primerjava merjenih in modeliranih vrednosti histereznih zank kaže zelo majhna medsebojna odstopanja. Obenem pa so dobljeni rezultati tudi potrditev uporabe J-A modela za mehko magnetne kompozitne materiale. Potrebno pa je poudariti, da se v primeru optimizacije parametrov za dinamične histerezne zanke izgubi fizikalni pomen parametrov J-A modela.

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APLIKACIJSKI ČLANEK APPLICATION ARTICLE

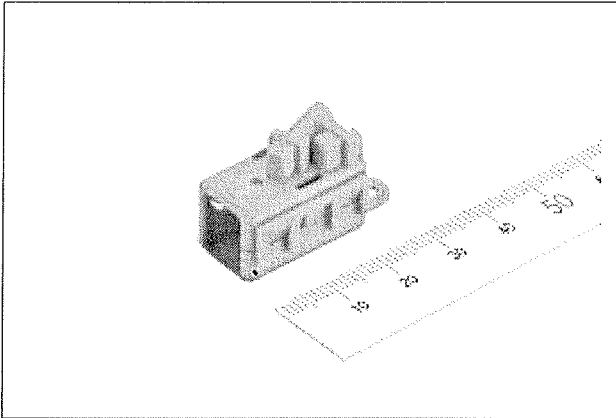
DEVELOPMENT OF LOW VOLTAGE-DRIVEN IONIZER

Murata Manufacturing Co., Ltd. has developed MHM Series low voltage driven ionizer for **negative ion (*1)** generation equipment.

Its original construction of forming a grounding electrode on a ceramic substrate with dia.70µm thick ultra fine wire attached, enables low voltage negative ion generation at -1.8kVdc (approx. 1/2 of the conventional generator) and less than 0.01ppm **ozone (*2)** generation.

It is a small unit at 13.0x23.0x12.0mm, and lead wire can be attached to it with its **self-locking terminal** without soldering.

Amount of negative ion generated at -2.5kVdc was 500,000 ions/cc (wind velocity 3m/sec, 50 cm away from the sample). Amount of ozone generated at -2.5kVdc was less than 0.01ppm (1cm away from the sample).



Background

There are more appliances such as air-cleaner, air-conditioner, humidifier, dehumidifier, etc. with negative ion generation feature produced. With the conventional negative ion generation system, high voltage near -5.0kVdc is applied to a needle shaped terminal. Since the voltage is high there were safety issues. Furthermore ozone tended to be generated as well.

We have applied high power technology and printing technology accumulated through our power durable product line to develop products that can generate ion at a voltage one half of the conventional models. We could also suppress ozone generation by controlling leakage current.

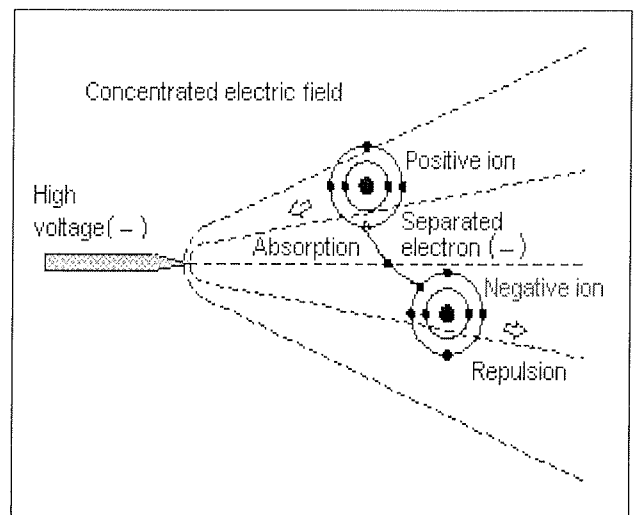
Terminology

*1 Negative ion

Negative ions are negatively charged molecules that are supposed to give refreshing sensations. Generation mechanism is as the following.

- Corona discharge occurs from the concentrated electric field under high voltage.
- Air molecules lose their outer electrons from the discharge energy becoming positive ions.
- Separated electrons are combined with other air molecules to form negative ions.
- Positive ions are absorbed by the electrode leaving only negative ions to be discharged.

Types of negative ions generated are, $O_2(H_2O)_n$ or $CO_3(H_2O)$.



*2 Ozon

Ozone is an allotrope of oxygen and its molecular equation is O_3 . Ozone is generated from electric discharge into air and has peculiar odor. Ozone is used for disinfecting, sanitization and bleaching due to its strong oxidation characteristics. Highly concentrated ozone gives adverse effect to human health after breathing it in for an extended period.

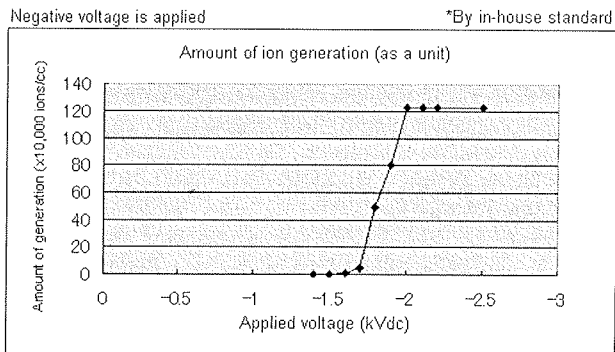
Electric Performance

Part Number	Item	Standard
MHM001	Rated voltage	-2.5kVdc
	Power durability	-5.5kVdc
	Ion generated	500,000 ions/cc or more (*1)
	Ozone generated	0.01ppm or less (*2)

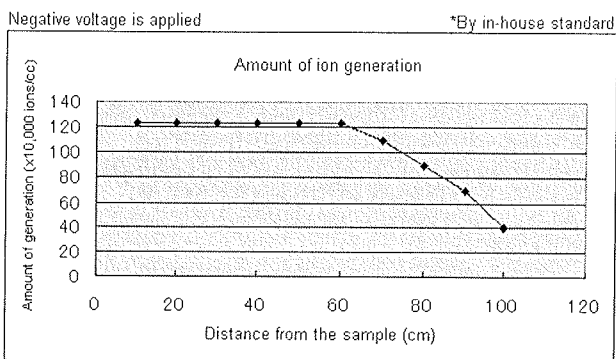
*1 Initial measurement at applied voltage -2.5kVdc, wind velocity 3m/sec, and 50cm away from the sample
Measurement Device: Andes Electric Co., LTD. ITC-201A

*2 Measured at applied voltage -2.5kVdc and 1cm away from the sample
Measurement Device: HIOKI E.E.CORPORATION. 2202

Initial ion generation

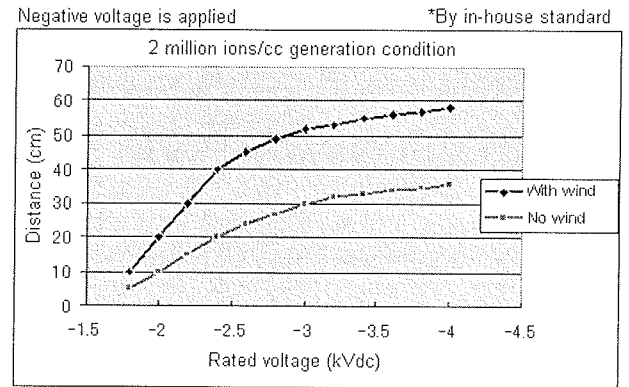


Wind velocity: 3m/sec. 50cm away from the sample. 25°C, At 50%RH (as a unit)
Measurement device: Andes Electric Co., Ltd. ITC-201A
(measurement limit 1.23 million ions/cc)



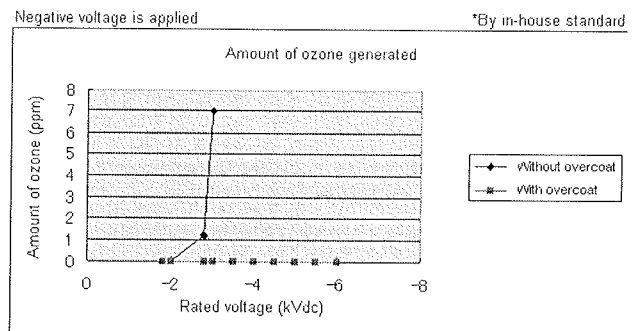
Applied voltage: -2.5kVdc, Wind velocity: 3m/sec. 25°C, At 50%RH (as a unit)
Measurement device: Andes Electric Co., Ltd. ITC-201A
(measurement limit 1.23 million ions/cc)

million ions/cc generation condition



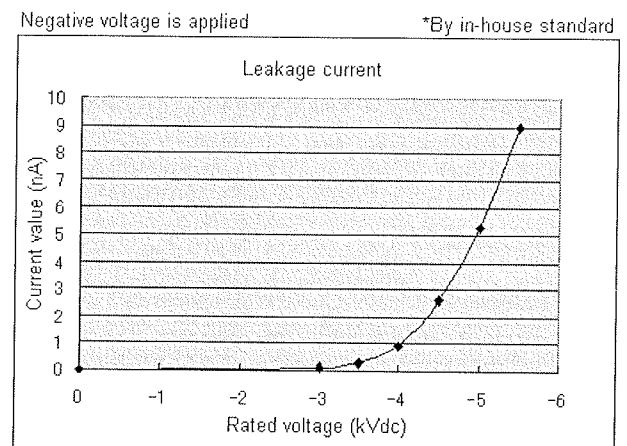
25degree C, 50%RH, Wind velocity: 3m/cc
Measurement device: AIR ION COUNTER/IC-1000

Amount of ozone generated (single element reference data)



5mm away from the sample, 25degree C, 45%RH
Measurement device: HIOKI ozone checker 2202

Amount of leakage current



Measurement device: ADVANTEST R8340

Zapisnik z Občnega zbora strokovnega društva MIDEM z dne 18.04.2005 Minutes of MIDEM Society Assembly on 18.04.2005

Vabilo z dnevnim redom in kandidatno listo je bilo poslano vsem članom po pošti.

Predlagan je bil sledeč **Dnevni red**:

- otvoritev občnega zbora in ugotovitev sklepčnosti (predsednica Marija Kosec)
- sprejem dnevnega reda
- izvolitev delovnega predsedstva
- izvolitev dveh overoviteljev zapisnika
- izvolitev treh članov komisije za sklepe
- izvolitev treh članov volilne komisije
- poročilo predsednice o pripravi kandidacijske liste (Marija Kosec)
- poročilo predsednice o delovanju društva v zadnjem mandatu (Marija Kosec)
- poročilo predsednice o delu izvršilnega odbora in finančnem rezultatu društva (Marija Kosec)
- poročilo nadzornega odbora (Franc Smolek)
- poročilo častnega razsodišča (Radko Osredkar)
- razprava o podanih poročilih in glasovanje o razrešnici dosedanjim organom in predsednici
- glasovanje za nove organe in predsednika
- poročilo volilne komisije o izidu
- nagovor novega predsednika ter predstavitev programa dela za naslednje obdobje
- predlogi članov za nadaljnje delo društva
- sprejem programa dela
- sprememba sedeža društva
- razno
- zaključek občnega zbora

Potek:

Ob 16,30 je občni zbor pričela in pozdravila predsednica društva Marija Kosec.

Predlagani dnevni red je bil soglasno sprejet.

Prisotni člani so za predsedujočega zboru soglasno imenovali Lojzeta Trontlja.

Predsedujoči je ugotovil, da ni prisotna polovica vseh članov. Zato je bilo v skladu s poslovníkom sprejeto, da se vsa glasovanja in izvolitve odložijo za pol ure, med tem pa se obravnavajo poročila. Temu ustrezno so bile premeščene točke dnevnega reda.

1.Poročilo predsednice društva

M.Kosec je izčrpno predstavila delovanje društva v zadnjem mandatu in glavne povdarke.

Posebej je bila predstavljena organizacija rednih letnih konferenc in organizacija delavnic. Naša strokovna revija Informacije MIDEM je v okolju dobro sprejeta in cenjena in si je pridobila ugleden faktor vpliva (Impact Factor). Izvršilni odbor se je po potrebi sestajal. Pregledano in urejeno je bilo članstvo ter pobrana članarina. V društvu bolj ali manj aktivno deluje cca 200 članov. Društvu tudi uspeva pridobiti donacije industrijskih sponzorjev.

Pri pripravi kandidacijske liste je bilo vodilo izvršilnemu odboru vodilo načelo, da so v novem izvršilnem odboru čim enakomerneje zastopani predstavniki vseh strok s področja delovanja društva ter da so zastopane vse večje institucije in industrija. V izvršilnem odboru je tudi nekaj uglednih predstavnikov tujih institucij, ki sodelujejo v društvu.

Predsednica se je zahvalila vsem aktivnim članom za njihovo sodelovanje in pomoč pri dejavnostih društva.

2.V imenu nadzornega odbora je poročal Franc Čuk. Poročal je, da je nadzorni odbor pregledal delo na osnovi prejetih poročil izvršilnega odbora, blagajnika in predsednice. Nadzorni odbor k delu nima pripomb in predlaga občnemu zboru, da dosedanjim organom društva potrdi razrešnico.

3.V imenu častnega razsodišča je poročal Radko Osredkar in prisotne seznanil, da častno razsodišče ni prejelo nobenega problema v razsojanje.

Predsedujoči je ugotovil, da je preteklo pol ure in da lahko prisotni na občnem zboru veljavno glasujejo.

4.Občni zbor je potrdil razrešnico organom društva.

5.Občni zbor je soglasno imenoval:

- dva overovitelja zapisnika: Leopold Knez in Marko Topič
- tri člane komisije za sklepe: Barbara Malič, Janez Holc, Janez Trontelj
- tri člane volilne komisije: Dubrovka Ročak, Uroš Aljančič, Marko Hrovat

6.Volilna komisija je pobrala izpolnjene glasovnice.

7.Ker se je EZS preselila na novo lokacijo (Stegne 7, Ljubljana) in dosedanji naslov društva MIDEM (na lokaciji EZS) ni več veljaven, smo zaprosili EZS, da nam dovolijo spremeniti naš naslov in uporabiti njihovega. Prejeli smo že načelni ustni pristanek.

Občni zbor pooblašča novoizvoljenega predsednika, da izvede spremembo sedeža društva, ko bo prejet tudi pisni pristanek.

8.V točki RAZNO je potekala diskusija, kako še izboljšati delovanje društva.

- Predlagano je bilo, da se vsi člani potrudijo za pridobitev novih članov, zlasti mlajših strokovnjakov s širokega strokovnega področja, ki ga pokriva društvo.
- Apel je bil dan vsem članom, da skušajo pridobiti več finančne podpore društvu.
- Člani so bili pozvani, da še aktivneje objavljajo svoje prispevke v reviji. Kadar je primerno, naj tudi citirajo revijo. Člani naj tudi pošljejo predloge, komu vse še poslati revijo, da bo še bolj poznana in upoštevana.
- Sprejet je bil predlog, da društvo ob prvi priliki najaktivnejšim članom v dosedanjih organih društva (Šorli, Topič, Pompe,...) in dosedanji predsednici svečano podeli zahvalno listino društva (diplomo).

9.Marko Hrovat je občnemu zboru poročal o ugotovitvah volilne komisije. Oddanih je bilo 32 glasovnic in **vsii predlagani kandidati so izvoljeni**:

IZVRŠILNI ODBOR DRUŠTVA:

1. predsednik društva : prof. dr. Slavko Amon, univ. dipl. inž. fiz., Fakulteta za elektrotehniko, Ljubljana
2. podpredsednica : prof. dr. Marija Kosec, univ. dipl. inž. kem., Institut Jožef Stefan
3. podpredsednik: dr. Iztok Šorli, univ. dipl. inž. fiz., Mikroiks d.o.o., Ljubljana
4. tajnik: Igor Pompe, univ. dipl. inž. el., upokojenec
5. blagajnik: prof. dr. Lojze Trontelj, univ. dipl. inž. el., upokojenec
6. član: Darko Belavič, univ. dipl. inž. el., HIPOPT-RR, d.o.o., Šentjernej
7. član: prof. dr. Bruno Cvikel, univ. dipl. inž. fiz., Fakulteta za gradbeništvo, Maribor
8. član: mag. Leopold Knez, univ. dipl. inž. el., Iskra TELA, d.d., Ljubljana
9. član: dr. Miloš Komac, univ. dipl. inž. kem., Ministrstvo za visoko šolstvo, znanost in tehnologijo
10. član: Jožef Perme, univ. dipl. inž. el., IskraEmeco, d.d., Kranj
11. član: prof. dr. Marko Topič, univ. dipl. inž. el.; Fakulteta za elektrotehniko, Ljubljana
12. član: prof. dr. Anton Zalar, univ. dipl. inž. met., Institut Jožef Stefan, Ljubljana
13. član: dr. Werner Reczek, Infineon, Avstrija
14. član: prof. dr. Giorgio Pignatelli, University of Perugia, Italija
15. član: prof. dr. Leszek J. Golonka, Technical University, Wroclaw, Poljska

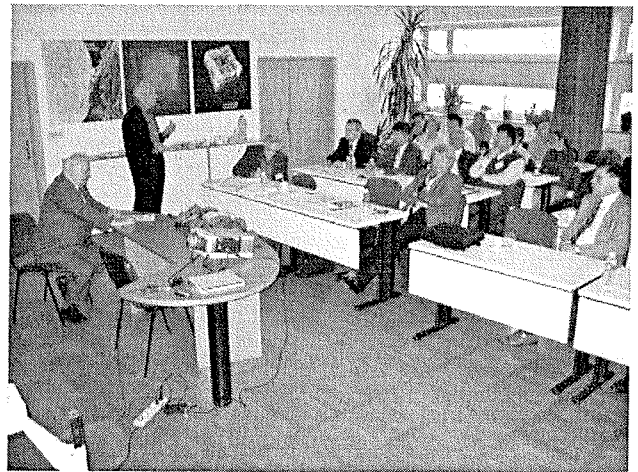
NADZORNI ODBOR DRUŠTVA:

1. prof. dr. Franc Smole, univ.dipl.inž.el., Fakulteta za elektrotehniko, Ljubljana
2. mag. Andrej Pirih, univ. dipl. inž. el., Iskra - Zaščite, d.o.o., Ljubljana
3. dr. Slavko Bernik, univ. dipl. inž. kem., Institut Jožef Stefan

ČASTNO RAZSODIŠČE:

1. Franc Jan, univ. dipl. inž. fiz., upokojenec
2. prof. dr. Radko Osredkar, univ. dipl. inž. el., Fakulteta za elektrotehniko, Ljubljana
3. mag. Milan Slokan, univ. dipl. inž. kem., upokojenec

10.Novoizvoljeni predsednik društva Slavko Amon je občni zbor nagovoril, se v imenu novoimenovanih organov in v svojem imenu zahvalil za izkazano zaupanje in na kratko predstavil program dela za naslednje obdobje.



11.Predsedujoči je ob 18. uri zaključil občni zbor.

Ljubljana, 19.04.2005

Zapisal:

Igor Pompe, tajnik društva MIDEM

Overovitelja zapisnika:

Leopold Knez,
Marko Topič

Poročilo s konference EUROPV2004

Conference report EUROPV2004

Na mednarodni konferenci »Euroconference Photovoltaic Devices: Manufacturing Issues - From Laboratory to Mass Production«, ki jo je od 15. do 20. oktobra 2004 v Kranjski Gori organiziral *Laboratorij za polprevodniške strukture in optoelektroniko* s Fakultete za elektrotehniko Univerze v Ljubljani, je sodelovalo kar 75 uglednih znanstvenikov, raziskovalcev in menedžerjev iz evropskih univerz, raziskovalnih centrov in industrije s področja fotovoltaike. Iz Slovenije je sodelovalo 6 strokovnjakov, sicer pa so prišli udeleženci kar iz 19 držav.

Predavatelji so predstavili razvoj tehnologij sončnih celic in fotonapetostnih modulov in prikazali uspešne primere prenosa znanj in novih tehnologij v serijsko proizvodnjo. Konferenco smo pričeli s pregledom trenutnega stanja in omejitev razvoja in proizvodnje, sledili pa so mu trije tematski sklopi: "napredek razvoja tehnologij", "od laboratorija do proizvodnje" in "proizvodne tehnologije". Razpravljali smo o ekonomskih in ekoloških vidikih serijske proizvodnje pri različnih tipih sončnih celic ter o možnostih izboljšav in razširitve obsega proizvodnje. Konferenca je postregla z vrsto zanimivih predavanj z različnih področij razvoja novih tehnologij in primerov njihove praktične uporabe.

V okviru prvega sklopa so podrobno predstavili predvsem pregled fotonapetostnih tehnologij na raziskovalnem nivoju. Tu je bilo veliko govora o novostih že uveljavljenih kristalnih, polikristalnih in tankoplastnih sončnih celic, pa tudi o novih tehnologijah, kot so na primer organske sončne celice. Te so z vidika proizvodnih stroškov sicer najcene-

jše, vendar pa njihovi izkoristki še ne dosegajo konkurenčnih vrednosti v primerjavi z drugimi tehnologijami.

Na področju prenosa znanj iz laboratorijev v proizvodnjo je bil glavni poudarek na prenosu tehnologij za izdelavo tankoplastnih sončnih celic v proizvodne pilotske linije. Predvsem je bilo na tej konferenci veliko govora o tankoplastnih silicijevih sončnih celicah, ki bistveno zmanjšajo stroške vgradnje silicija v primerjavi s kristalnimi sončnimi celicami. Pri kristalnih sončnih celicah pa so bili predstavljeni novi koncepti tovrstnih tehnologij, ki zmanjšujejo senčenje zaradi kontaktov na gornji površini sončnih celic. Pri tretjem tematskem sklopu so strokovnjaki namenili pozornost proizvodnji kristalnega in polikristalnega silicija kot surovine za izdelavo sončnih celic. Predstavili so tudi proizvodnjo amorfno silicijevih sončnih celic, halkopiridnih sončnih celic itd.

V zaključnem delu mednarodne konference pa so predstavili evropsko regulativo na področju predpisov fotonapetostnih sistemov kot odpadkov in hkrati tudi možnosti recikliranja fotonapetostnih modulov. V trenutnem obsegu proizvodnje reciklaža namreč še ni ekonomsko upravičena. Ko pa bo na primer prišlo do stokrat večje proizvodnje vseh fotonapetostnih modulov, bo dejansko smiselno te fotonapetostne module reciklirati in jih kot odpadke tudi ekološko predelovati.

Mednarodna konferenca v Kranjski Gori je nudila številne možnosti izmenjave in pridobivanja znanja tako na formalnih razpravah po predavanjih ali med predstavitvijo posterjev, kakor tudi na neformalnih medsebojnih srečanjih. Konferen-



Udeleženci EUROPV2004.

ca je bila pomembna tudi z vidika aktivne vpetosti slovenskih raziskovalcev v evropski raziskovalni prostor na področju fotovoltaike. V Laboratoriju za polprevodniške strukture in optoelektroniko se že vrsto let aktivno ukvarjamo z raziskavami in razvojem sončnih celic. Aktivna udeležba v tematskih mrežah in raziskovalnih projektih Evropske skupnosti nam je odprla že marsikatera vrata. Pričakujemo, da bo po Kranjski Gori to še toliko lažje.

Predstavljena tematika je časovno zelo usklajeno sovpadla z aktualnimi razmerami na svetovnem trgu, kjer vlada

veliko povpraševanje po fotonapetostnih modulih, in s številnimi objavami o povečevanju proizvodnih zmogljivosti podjetij v fotonapetostni industrijski panogi, ki se zadnja leta zelo hitro razvija.

Dodatne informacije o konferenci so na voljo na konferenčni spletni strani: <http://www.pv-net.net/europv2004.htm>.

Prof. dr. Marko Topič
Podpredsednik konference EUROPV2004

NOVICE NEWS

Infineon to close 150mm Munich Perlach plant

NUMBER ONE European chip maker Infineon Technologies has announced plans to phase out its chip manufacturing operations in Munich Perlach, Germany by early 2007. Around 800 employees will be affected by the move.

Production currently being undertaken at Munich Perlach will be transferred to the company's facilities at Regensburg and to a lesser extent Villach.

Infineon said in a press release that it had taken the decision because the products currently manufactured at its Munich Perlach plant could be produced more efficiently at the company's newer fabs.

The Munich Perlach plant was founded 20 years ago as a research facility and now manufactures specialist semiconductors, largely high-frequency products. These devices however are increasingly being integrated into CMOS chips, which cannot be manufactured in Perlach. The plant also operates on the older 150mm silicon wafers, making it uneconomical compared to the company's newer 200mm and 300mm fabs.

"As the manufacturing standard for logic products corresponds to 200mm wafer, the cost disadvantage of the 150mm manufacturing vis-a-vis the 200mm manufacturing is considerable and will continue to increase," said a company spokesman.

"With the transfer of the remaining technologies to Regensburg and Villach, the manufacturing will largely be shifted to 200mm."

The company has not said how many - if any - jobs will be lost as a result of the restructuring but promised to "look into the possibility of further employment within the company" for affected workers.

"The restructuring will be done in a manner that is as socially acceptable as possible," said the spokesman. "Supportive personnel measures for the remaining time of production and the phase-out are being discussed with the relevant works council."

Plenty of sleep helps chips work better

EUROPE'S LARGEST chip maker Infineon Technologies has unveiled two new circuit techniques that it claims can reduce current leakage in 120nm and 90nm CMOS technologies.

Presented at the recent Solid State Circuits Conference in San Francisco, the techniques can cut current leakage by up to three orders of magnitude. This is important because current leakage is one of the biggest obstacles in the way of achieving further miniaturisation of transistors.

Reductions in feature sizes cause a huge rise in static power dissipation, which can prevent an integrated circuit from working correctly.

The techniques developed by Infineon in association with the Technical University of Munich and the Christian Albrechts University of Kiel -are based on the so-called sleep transistor concept.

The basic idea is to disconnect circuit blocks that are temporarily not required for data processing from the supply voltage using sleep transistors. The circuit blocks are re-activated by switching on the sleep transistors shortly before new data has to be processed.

IMEC celebrates

In 2004, IMEC commemorated its past and celebrated its future. Twenty years ago, Professor Baron Roger Van Overstraeten and 70 co-workers founded IMEC. Today, thanks to the dedication of its scientists and partners, IMEC has grown to be a world-renowned independent research center in nanoelectronics and nanotechnology. With the inauguration of a 300mm-compatible clean room in May 2004, IMEC can extend its growth into the future with state-of-the-art toolsets and technology. Consistent with the vision of its founders twenty years ago, worldwide collaboration with industry and academia remains the key to success.

IMEC created in its home region of Flanders one more new spin-off company that formerly was in the incubation phase. Gemidis, created in collaboration with Ghent University, provides solutions for the integration of liquid-crystal-on-silicon (LCDS) micro-displays in day-to-day applications. Meanwhile, Photovoltech, a spin-off company established in 2001, plans to increase its production capacity significantly, allowing for the creation of nearly 80 new jobs on top of an existing 90 positions. Also, work with other Flemish companies continues to grow. More than 120 Flemish companies called upon IMEC's services in 2004, 69 of which were small-and medium-sized enterprises (SMEs).

An important focus is collaboration across borders. IMEC actively supports European initiatives targeting innovative technology growth areas. In 2004, Europe launched several initiatives to strengthen collaborative research between

industrial players, research institutes and universities across Europe. ENIAC (European Nanoelectronics Initiative Advisory Council) and ARTEMIS (Advanced Research and Technology for Embedded Intelligence and Systems) are two such initiatives with IMEC experts on the steering committees and participating in working groups. IMEC also initiated discussions to broaden collaboration with both the Netherlands and Germany. The so-called Eindhoven - Leuven - Aachen triangle is a high-technology region that houses strong expertise in silicon- and software-based systems, as well as in healthcare and automotive systems. Open borders enhance open innovation, leading to new developments and opportunities in healthcare, lifestyle and ambient technology.

In 2004, IMEC further strengthened worldwide relationships with key players in its fields of expertise. The most striking example is the consortium of more than 30 tool suppliers, semiconductor manufacturers, material suppliers and mask shops working together on the development of 193nm-immersion lithography. IMEC and its partners can perform research -thanks to its long-term strategic partnership with ASML - on the TWINSCAN™ XT:1250i. This is a pre-production tool, with the highest numerical aperture (NA) available in the world. Agreements were also made with ASML on the delivery of a full-field EUV pre-production tool by 2006.

IMEC was pleased to expand its team of core partners on the sub-45nm silicon research platform to seven participants: Infineon, Intel, Matsushita, Philips, Samsung Electronics, STMicroelectronics, and Texas Instruments. In addition to its core partnership, Philips and IMEC have also performed research and development activities in advanced CMOS technologies for many years. In 2004, Philips renewed its agreement with IMEC for another 5 years.

IMEC's M4 program, developing technologies for the mobile terminal of the future, was further refined in 2004. Although the program is still in its early stages, Samsung has become the first strategic partner and will help drive a broad range of research projects.

New horizons were also explored in 2004. In Asia, IMEC signed a Memorandum of Understanding with the National Science Council of Taiwan to promote cooperation in the fields of technology development, pertaining to basic research, technology strategy R&D management, technical information, and training regarding microelectronics and ICT.

IMEC believes we have entered into an era in which the merging of diverse technologies and disciplines is the key to innovation. To stay at the forefront of new developments in its next 20 years, IMEC will continue to strengthen its multidisciplinary character and extensive collaborations throughout the world, based upon a state-of-the-art research infrastructure and a pool of international talent.

Merck KGaA buys Vecia's polymer electronics business

Merck KGaA has acquired the OLED (organic light-emitting diodes) materials and the polymer electronics businesses of Vecia, a privately-owned speciality chemical company based in Manchester, UK, for 50m in cash. The transaction, subject to regulators approval and approval by E. Merck OHG, is expected to be completed during the first quarter of 2005. The acquisition includes Covion Organic Semiconductors, of Frankfurt, Germany, a leader in the design, development and manufacture of high quality OLED materials, and Vecia's polymer electronics research and development activities, also based in Manchester. The two companies, together with 100 employees, will be integrated into Merck's liquid crystals division. OLEDs are extremely thin semi-conducting organic polymers suitable for a wide variety of applications, including light sources and displays, made by placing a series of organic thin films between two conductors.

"It is apparent that liquid crystal displays will be the dominant flat-panel technology for some years to come," said Merck chairman Bernhard Scheuble. "We see this acquisition as an opportunity to explore alternative technologies for the future." Polymer electronics will increasingly be used in applications such as solar cells, organic TFTs (thin film transistors) and RFID (radio-frequency identification) tags.

Covion is mainly focused on developing, future applications for OLEDs, and had sales of approximately 8m in 2004. Formed in 1999 by Vecia and Aventis Research & Technologies, it was fully acquired by Vecia in 2002.

SEZ Group announces record sales for 2004 Wednesday 6 of April 2005

Austrian wafer processing company SEZ Group has reported its results for the 2004 full year, with record consolidated net sales of 304.8 million Swiss Francs (CHF) - up from CHF 170.1 million in 2003 - and operating profit (EBIT) of CHF 37.8 million (2003: CHF 1.4 million loss).

The company's EBIT margin of 12.4 percent was below expectations, whereas net profit - 32.1 million (2003: CHF 1.8 million) - was better than expected. Order intake improved by 53% to CHF 309.1 million.

In the first quarter of 2005, preliminary net sales of around CHF 77 million exceeded the same period last year (CHF 66.3 million), as well as the previous quarter (CHF 75.7 million). Order intake also improved by 10.6% to CHF 69.0 million compared to the previous quarter.

Commenting on the results, a company spokesman said: "While consolidated net sales advanced favourably, cost of goods sold had a less positive impact on operating profitability due to elevated pricing pressures, advances in the

market and unfavourable changes in the currency exchange.”

In terms of technological changes, SEZ expects the industry to shift from batch to single-wafer wet processing in 2005.

“As the market and technology leader in this industry segment, SEZ will continue to benefit from this trend, especially with its Da Vinci platform,” said the spokesman.

Among SEZ's first-quarter 2005 purchase orders were multiple orders for Da Vinci tools from a Korean memory manufacturer and a large Chinese foundry.

The company has also just announced that Japanese memory manufacturer Elpida Memory has placed an order for multiple 300mm, double-chamber single-wafer cleaning systems.

The company said that it expects its Da Vinci tools to account for about 60% of the group's sales in 2005 – and it is outsourcing production to Eastern Europe to meet the expected demand.

SEZ is also forecasting that the “order momentum” would continue into the second half of this year.

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