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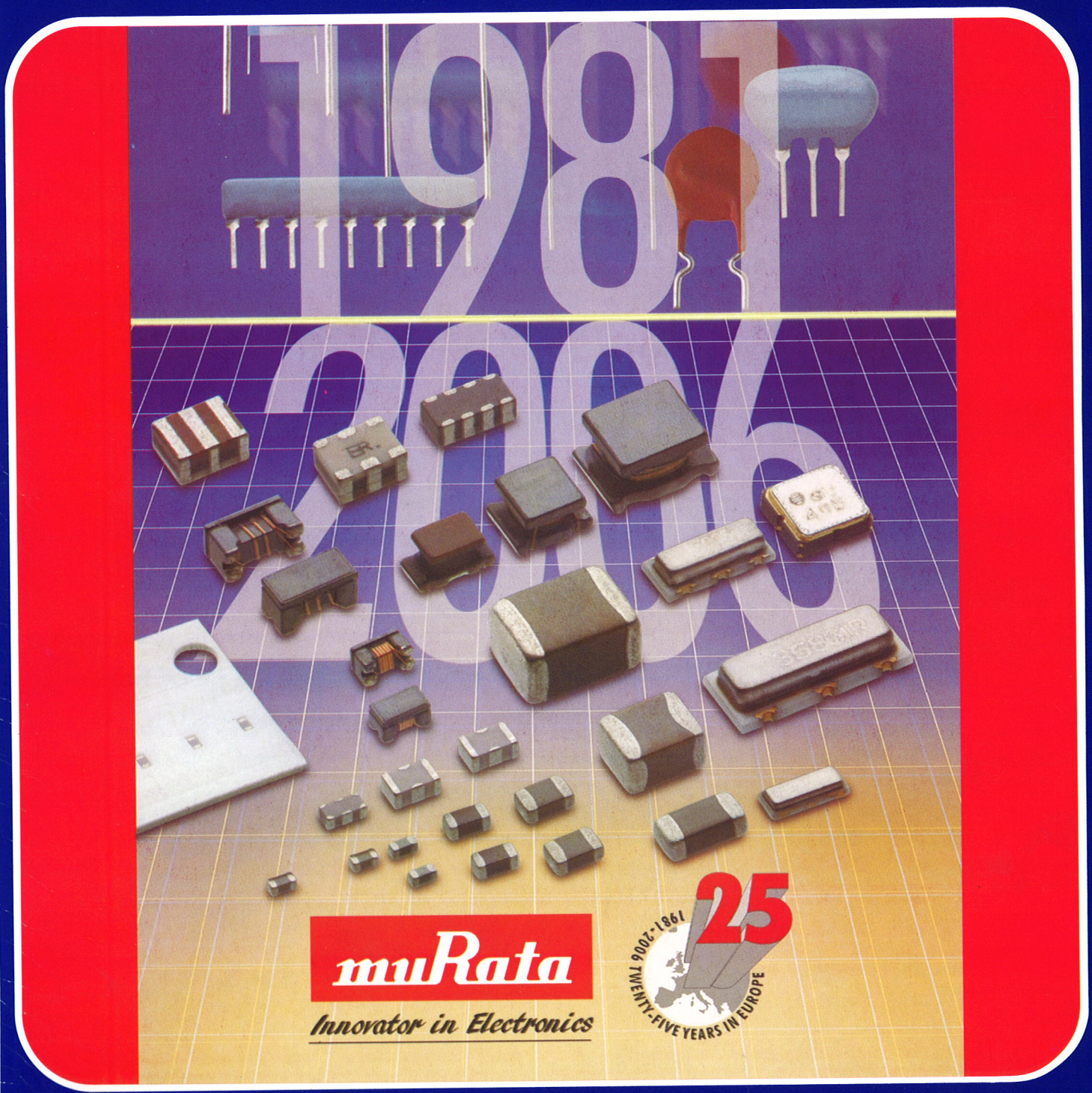
Journal of Microelectronics, Electronic Components and Materials

INFORMACIJE MIDEM, LETNIK 36, ŠT. 3(119), LJUBLJANA, september 2006



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**Naslov uredništva**
**Headquarters**
Uredništvo Informacije MIDEM
MIDEM pri MIKROIKS
Stegne 11, 1521 Ljubljana, Slovenija
tel.: + 386 (0)1 51 33 768
fax: + 386 (0)1 51 33 771
e-mail: Iztok.Sorli@guest.arnes.si
http://www.midem-drustvo.si/

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# D.C. CHARACTERISTICS OF SiC POWER SCHOTTKY DIODES MODELLING IN SPICE

Janusz Zarębski, Jacek Dąbrowski

Gdynia Maritime University, Department of Marine Electronics

**Key words:** Silicon Carbide (SiC), Schottky Barrier Diodes (SBDs), modelling, self-heating, electrothermal macromodel, SPICE

**Abstract:** In this paper the problem of SPICE modelling of the class of silicon-carbide (SiC) Schottky diodes with thermal effects (self-heating) taken into account is considered. Since April 2001 the SiC Schottky diodes made by Infineon Technologies have been commercially attainable. In the paper the SPICE electrothermal (including self-heating) macromodel of Infineon Technologies SiC Schottky diode is presented and in detail investigated. The considered macromodel has been verified experimentally. The silicon-carbide SDP04S60 rectifier has been tested. The nonisothermal characteristics obtained from measurements and SPICE calculations of SDP04S60 diode are compared. Due to the unacceptably large differences between measurements and calculations, some modifications of the macromodel have been proposed.

# DC karakteristike močnostnih SiC Schottky diod – modeliranje s programom SPICE

**Kjučne besede:** Silicijev karbid ( SiC ), Schottky diode, modeliranje, pregrevanje, elektrotermični model, SPICE

**Izvleček:** V prispevku obravnavamo probleme pri modeliranju SiC Schottkyjevih diod s programom SPICE z upoštevanjem termičnih efektov. Od aprila leta 2001 so SiC Schottky diode izdelane pri podjetju Infineon Technologies tudi komercialno dosegljive. Tako v prispevku predstavimo in natančno obravnavamo SPICE elektrotermični model prav teh diod. Predastavljeni model smo preverili tudi eksperimentalno in sicer smo testirali SiC diodo z oznako SDP04S60. Primerjali smo izmerjene in izračunane neizotermične karakteristike. Zaradi velikih razlik med meritvami in napovedmi, predlagamo določene spremembe pri parametrih makromodela.

## 1. Introduction

The silicon carbide (SiC) is a great promising semiconductor material for manufacturing of power devices. It occurs in over 170 polytypes, the most common of which are cubic 3C, hexagonal 4H and 6H structures. A number of most important physical aspects of SiC compared to other semiconductors one can find in the literature, e.g. /1,2,3/. As results from the cited papers, silicon carbide has an order of magnitude higher breakdown electric field and an electron mobility only about 20% lower (for 4H-SiC) than silicon. A high breakdown electric field allows to design the SiC power devices with 10-times thinner and about 100-times higher dopend voltage blocking layers. Smaller dimensions of SiC material result in higher device switching frequency.

Nowadays, a lot of SiC devices, as transistors, diodes, thyristors, LED's, thermistors etc. are manufactured and investigated in laboratories /4,5/. In the case of the power SiC devices a high breakdown voltage is needed. So far, the SiC power diodes, have been the class of semiconductor devices having the greatest values of the breakdown voltage equal to 10 kV for Schottky diodes /6/ and 19 kV for PiN diodes /7/. Since 2001 SiC Schottky diodes made by Infineon Technologies have been available in the market /8/.

A very important feature of all semiconductor devices, including SiC SBDs, is a strong influence of the temperature on their characteristics. Due to the self-heating resulting from the change of the device dissipated power into the heat in the case of nonideal cooling conditions, the junction temperature (often much greater than the ambient one) affects the device characteristics, called the nonisothermal ones. In order to take into account the self-heating, the models of the special kind, called the electrothermal models (ETM) have to be used for the device simulations.

Infineon Technologies, on their web-side /9/, offers the SiC Schottky's electrothermal macromodel for SPICE, indicated as Level 3.

In the paper the Level 3 Infineon's SPICE macromodel is presented, in detail discussed and experimentally verified. The SDP04S60 diode: 4A/600V, has been chosen for investigations, instead of 6A/600V SiC Schottky diode (SDP06S60) considered in /10/. Due to the fact, that obtained results between measurements and calculations differ from each other significantly, therefore some modifications of the macromodel were introduced.

## 2. The Macromodel Form of The SiC Schottky Diode

To derive the electrothermal macromodel of the considered device, the following dependencies have to be used /11/:

- the current-voltage-temperature dependence (isothermal model),

- the dependence of the inside (junction) temperature $T_j$ on the electrical power dissipated in the device, along with the dependence of this electrical power on the device terminal currents and voltages (thermal model).

The structure of such a macromodel is shown in Fig. 1.

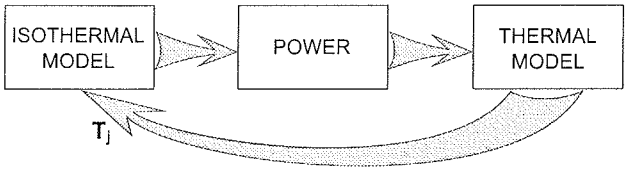


*Fig. 1. The structure of the electrothermal macromodel of the SiC Schottky diode*

Next, the detailed form of the isothermal model and the thermal model, forming the considered electrothermal macromodel are presented and discussed.

The network form of the isothermal model of the SiC Schottky diodes is presented in Fig. 2. /9/.

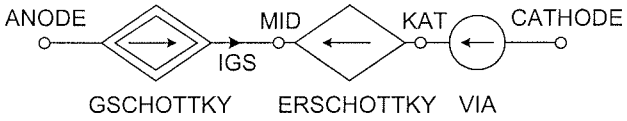


*Fig. 2. The network form of the isothermal model of the SiC Schottky diode*

As seen, the model is composed of three elements: the controlled current GSCHOTTKY source, the controlled voltage ERSCHOTTKY source and the independent source VIA of the efficiency equal to zero. Due to the d.c. dependencies considered here, the wire inductance and junction capacitance are not taken into account in further considerations.

The control current source GSCHOTTKY is of the efficiency

$$I_{GS}(T,V) = I_{bw}\cdot\left[\exp\left(\frac{V\cdot q}{k\cdot(T_0+T)}\right)-1\right] \qquad (1)$$

where $T$ - the analysis temperature ($T \equiv TEMP$) in Celsius degrees, $V$ - voltage between ANODE and MID nodes, $I_{bw}$ - reverse (saturation) current, $q$ - electron charge, $k$ - Boltzmann's constant, $T_0$ - the reference temperature.

The saturation current is expressed by the formula

$$I_{bw} = AREA\cdot A_0\cdot(T_0+T)^2\cdot\exp\left(\frac{-q\cdot\phi_{SiC}}{k\cdot(T_0+T)}\right)\cdot K \qquad (2)$$

where *AREA* - relative device area, $A_0$ - Richardson's constant, $\phi_{SiC}$ - metal-semiconductor barrier height.

In Eq.(2) the factor $K$ models the lowering effect existing in the reverse range of the Schottky diode operation which is given by the following expression

$$K = \exp\left(\frac{q\cdot\sqrt{\beta\cdot EFLD_{(V)}}}{k\cdot(T_0+T)}\right)\cdot \frac{1}{2}\cdot\left(1+\exp\left(AA+AB\cdot(T-127)+AC\cdot(T-127)^2+\frac{\alpha_1\cdot EFLD_{(V)}}{EFLD_{\left(\frac{-VPT}{5}\right)}}\right)\right) \qquad (3)$$

where $b$, $AA$, $AB$, $AC$, $\alpha_1$ and $VPT$ are the model parameters.

The description of the electric field (*EFLD*) dependent on the junction reverse voltage is divided into three ranges according to the value of the anode-cathode voltage, up to the pattern (4), where $V$ denotes the voltage on the diode, $EPT$ denotes the critical electrical field, whereas $x$ and $g$ are the model parameters. *LIMIT* denotes the SPICE standard function.

$$EFLD = \begin{cases} 0 & if \quad V > 0 \\ \sqrt{\xi\cdot \mathrm{LIMIT}(-V,0,VPT)} & if \quad -V < VPT \\ \mathrm{EPT}\text{-}\gamma\cdot\left(\frac{V}{VPT}+1\right) & if \quad -V \geq VPT \end{cases} \qquad (4)$$

In turn, the voltage source ERSCHOTTKY controlled by the current of VIA source models the influence of the diode series resistance on the i(u) characteristics. Thus

$$U_{ERS} = I_{(VIA)}\cdot R_{S(T)} = \frac{I_{(VIA)}\cdot R_{0SQ}}{AREA\cdot V_j^2}\cdot\left(\frac{T_0+T}{T_0}\right)^{\chi} \qquad (5)$$

where $R_{S(T)}$ is the series resistance dependent on the temperature, $R_{0SQ}$ is the specific series resistance at the reference temperature $T_0$, whereas $I_{(VIA)}$ is the zero voltage source current and $\chi$, $V_j$ are the model parameters. The isothermal model parameter values of the diode are collected in Table 1 /9/.

The thermal model of the considered diode has been presented in the network form (Cauer leader) consisting of four resistors (*RTHD*) and capacitances (*CTHD*), representing the junction-to-case thermal impedance of the diode (Fig. 3.) /9/. The values of those elements are given in Table 2. The nodes TJ and TCASE represent the junction and the case temperatures respectively, whereas the potential value of the node TREF representing the ambient temperature, can be fixed by the efficiency of the voltage source VREF. This form of the thermal model is not acceptable by SPICE due to the fact, that the TREF node has not d.c. connection with the other one. Therefore, in the case of the ideal conditions of the case cooling, the nodes TREF and TCASE have to be shorted. Otherwise, between the nodes TCASE and TREF, the *RC* network of the Cauer leader, representing the phenomena of heat removing from the case to the ambient (e.g. by means of a heat-sink), has to be added.

*Table 1 The parameters values of the isothermal model of the SDP04S60 diode*

| Parameter | Value |
|---|---|
| $q$ [C] | $1.602 \cdot 10^{-19}$ |
| $k$ [J/K] | $1.38 \cdot 10^{-23}$ |
| $T_0$ [K] | 273 |
| $A_0$ [A · cm$^{-2}$ · K$^{-2}$] | 110 |
| $\phi_{SiC}$ [eV] | 1.3 |
| *AA, AB, AC* | -1.5, $-12.95 \cdot 10^{-3}$, $91 \cdot 10^{-6}$ |
| $\alpha_1$ | 3.8 |
| $R_{0SQ}$ [mΩ · cm$^2$] | 0.9 |
| *VPT* [V] | 400 |
| *EPT* [V/cm] | $1.05 \cdot 10^{6}$ |
| β | $1.49 \cdot 10^{-8}$ |
| ξ | $2.811 \cdot 10^{9}$ |
| γ | $5.33 \cdot 10^{5}$ |
| χ | 1.5 |
| *AREA* | 0.0116 |
| $V_j$ | 0.75 |

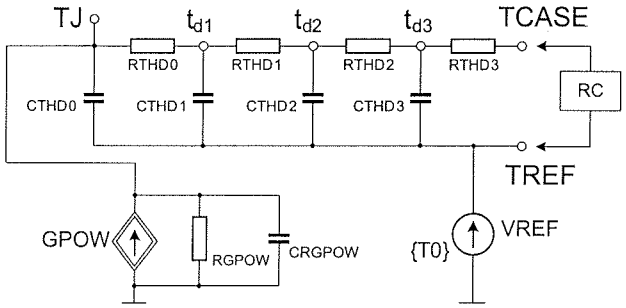


*Fig. 3. The general form of the thermal model of the SiC SDP04S60 Schottky diode*

*Table 2 The parameter values of the thermal model of the SDP04S60 diode*

| Parameter | Unit | Value |
|---|---|---|
| *RTHD0* | [K/W] | 1.756 |
| *RTHD1* | | 1.717 |
| *RTHD2* | | 0.545 |
| *RTHD3* | | 0.094 |
| *CTHD0* | [J/K] | $5.243 \cdot 10^{-4}$ |
| *CTHD1* | | $1.076 \cdot 10^{-3}$ |
| *CTHD2* | | 0.044 |
| *CTHD3* | | 2.025 |
| *RGPOW* | [Ω] | $100 \cdot 10^{6}$ |
| *CRGPOW* | [F] | $10 \cdot 10^{-12}$ |

The controlled current source GPOW represents the real power dissipated in the diode. Its efficiency is described by

$$I_{GPOW} = \begin{cases} ABS\left(I_{(VIA)} \cdot V_{(ANODE,CATHODE)}\right) & if\ t > 25ns \\ 0 & if\ t \le 25ns \end{cases} \quad (6)$$

where $I_{(VIA)}$ is the total current flowing through the diode, $V_{(ANODE,CATHODE)}$ is the voltage on the diode, whereas *ABS* is the standard SPICE function denoting the absolute value of any function.

In the case of the analysis at the steady-state the simplified, shown in Fig. 4, thermal network is used. In this figure the resistance $R_1$ denotes the junction-to-case thermal resistance represented by the sum of $RTHD_i$ (i = 0÷3) and equal to 4.112 K/W, whereas the resistance $R_2$ represents the case-to-ambient resistance of the value depending on the case cooling conditions. Note, that the thermal model can be used in d.c. analysis, if the time limitations in Eq.(6) are eliminated.

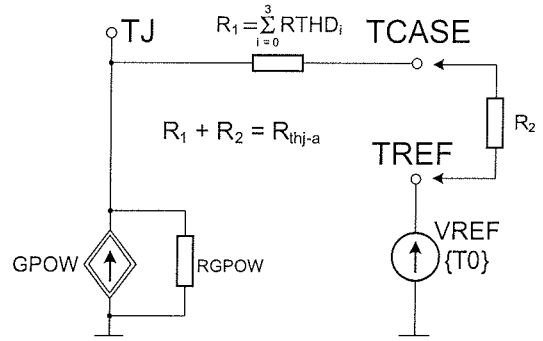


*Fig. 4. The thermal model of the SiC Schottky diode for d.c. analysis*

## 3. The Macromodel Verification

To estimate the correctness of the macromodel described in the early chapter, SPICE simulations of the forward and reverse characteristics of the diode SDP04S60 have been compared to the measurements. The diode has been operated without the heat-sink. The value of the measured thermal resistances $R_{thc\text{-}a}$ is equal to 59.26 K/W.

The results of measurements (points) and SPICE simulations (lines) in the wide temperatures range are shown in Fig. 5 (the forward range) and Fig. 6 (the reverse range), respectively. As seen in Fig. 5, the simulation results based on the original macromodel (the broken lines) differ from the measurements even more than 60 %.

To improve the agreement between simulations and measurements the following modification of the parameter χ (existing in Eq.(5)) has been proposed /10/

$$\chi = 1.58 + \left(35 \cdot 10^{-5} \cdot T^1\right) + \left(32 \cdot 10^{-7} \cdot T^2\right) \quad (7)$$

After these modifications the considered characteristics obtained both from measurements and SPICE calculations fit well and the error of the current estimation at the given voltage is not greater than a few per cent.

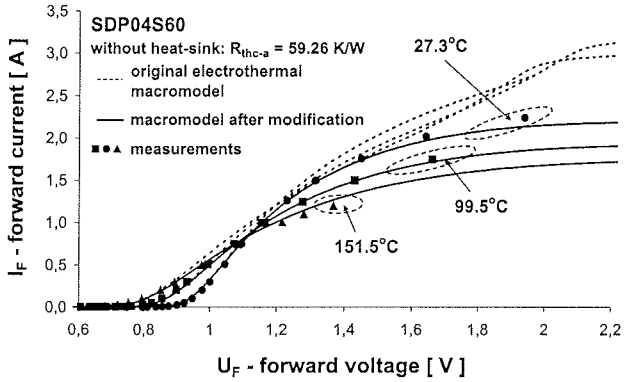


*Fig. 5. The forward characteristics of the SDP04S60 diode without the heat-sink*

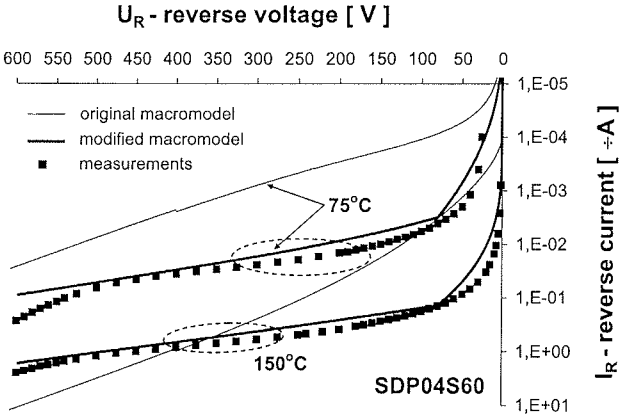


*Fig. 6. The reverse characteristics of the SDP04S60 diode*

The considered macromodel along with the author's additional modifications presented in Table 3, has also been used for modelling the diode characteristics operating in the reverse range /10,12/. Note, that for the considered two ambient temperature values, different values of the selected parameters are required.

As seen, also in this case a very good agreement between the results of measurements (points) and electrothermal calculations has been obtained. One can notice, that in the considered voltage range the dissipated power in the diode can be omitted. Thus, the obtained characteristics can be treated as the isothermal ones.

*Table 3 The macromodel modifications for the SDP04S60 diode operating in the reverse range*

| Parameter | | Value | | |
|---|---|---|---|---|
| | | Original | 75°C | 150°C |
| $\alpha_1$ | | 3.8 | 2 | 1.75 |
| $\beta$ | | $1.49 \cdot 10^{-8}$ | $2.24 \cdot 10^{-7}$ | $1.60 \cdot 10^{-7}$ |
| $\phi_{LS}$ | $V \leq VPT/5$ | $\frac{q \cdot \sqrt{\beta \cdot EFLD_{(V)}}}{k \cdot (T + T_0)}$ | $\frac{q \cdot \sqrt{\beta \cdot EFLD_{(V)}}}{k \cdot (T + T_0)}$ | |
| | $V > VPT/5$ | | $\phi_{LS(VPT/5)} = 10.87$ | $\phi_{LS(VPT/5)} = 7.55$ |

## 4. Conclusions

In the paper the electrothermal macromodel of the SiC Schottky diode has been investigated and verified experimentally. As was proved, the original macromodel is of poor accuracy, whereas after the author's modifications the characteristics obtained from measurements and calculations fit very well. Note, that to perform the simulations the value of the thermal resistance from the case to the sourrounding had to be additionally measured.

## Acknowledgments

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*Prof. Janusz Zarębski; M.Sc. Jacek Dąbrowski*
*Gdynia Maritime University,*
*Department of Marine Electronics*
*Morska 83, 81-225 Gdynia, POLAND,*
*Tel. ++48 58 6901599, ++48 58 6901609,*
*fax ++48 58 6217353*
*E-mail: zarebski@am.gdynia.pl, oakjack@am.gdynia.pl*

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# PRIMERJAVA TONSKIH PREDOJAČEVALNIH STOPENJ S POLPREVODNIŠKIMA TRANZISTORJEMA IN ELEKTRONKO

Rudolf Babič, Davorin Osebik

Univerza v Mariboru, Fakulteta za elektrotehniko računalništvo in informatiko, Maribor, Slovenija

**Kjučne besede:** ojačevalniki, tonski predojačevalniki, frekvenčni spekter, harmonska popačenja, bipolarni tranzistor, tranzistor na poljski učinek, vakuumska elektronka

**Izvleček:** V tem članku bomo skušali pojasniti dileme, ki se pri glasbenikih, predvsem kitaristih, pojavljajo v zvezi z izbiro ojačevalnikov oziroma ojačevalnih elementov za tonske predojačevalne stopnje. Predvsem je zanimiva primerjava med aktualnimi polprevodniškimi tranzistorji, bipolarnimi in tranzistorji na poljski učinek ter še vedno prisotno elektronko. Osvetlili jo bomo s stališča izmerjenih frekvenčnih spektrov in harmonskih popačenj posameznih ojačevalnih stopenj, da bi s tem nekako potrdili slišne razlike med posameznimi skupinami ojačevalnih elementov. Z merilno opremo, ki smo jo aparaturno sestavili na osnovi osebnega računalnika z zvočno kartico, programsko pa nadgradili s programskim paketom MATLAB, smo potrdili, da se razlike v slišnih lastnostih signala na izhodu posameznih ojačevalnih elementov pokažejo predvsem pri prekrmiljenem delovanju ojačevalne stopnje. Od majhnih, vendar že lepo opaznih razlik v obliki izhodnega frekvenčnega spektra, ki smo jih zasledili že pri majhnih vrednostih skupnih harmonskih popačenj, ki so bila glede na uporabljen ojačevalni element različna z vrednostmi od 1 do 5 odstotkov pri istem vhodnem signalu 50 mV, je postala vsebnost višjih harmonskih komponent v izhodnem signalu ojačevalne stopnje pri 20 odstotni vrednosti skupnih harmonskih popačenj pri elektronki bistveno drugačna od tiste pri vezju z bipolarnim oziroma vezju s tranzistorjem na poljski učinek. Vsebina višjih harmonskih komponent pa skupaj z osnovno harmonsko komponento določa sonorne lastnosti signala in s tem tudi slišne razlike. S tem lahko tudi potrdimo, da je prisotna tesna povezava med električnimi popačenji in zvočno barvitostjo.

# The Comparison of Audio Preamplifier Circuits with Solid State Transistors and Vacuum Tube

**Key words:** amplifiers, audio preamplifiers, frequency spectrum, harmonic distortions, bipolar junction transistor, field effect transistor, vacuum tube

**Abstract:** In this article the answer for dilemma which appear, especially between musicians, about the questions what amplifying device is appropriate for audio preamplifier circuits is presented. For this purpose the comparison is made between actual solid state transistors, bipolar junction transistor and field effect transistor versus vacuum tube. The tested preamplifier circuits with component specifications are shown on fig. 4. Although solid state technology overwhelmingly dominates today's world of electronics, vacuum tubes are holding out the small but vibrant area in the creation and reproduction of music. The music is played to be heard by human beings, whose nonlinear ear-brain hearing system are far from fully understood. Since no one knows exactly how to model the human auditory system, no one knows exactly what engineering measurements are appropriate to evaluate the performance of audio equipment. We know that some number of people prefer the sound produced by tube equipments which are found in musical instrument amplifiers (mainly guitar amplifiers), some processing devices used in recording studios and in high-fidelity audio equipments.

Some of the differences in the audio qualities between tubes and transistors have to do with the inherent physical properties of the devices and with the circuit topologies and what components are used with each type of the device. We know already that vacuum tubes have lower total harmonic distortions than bipolar transistor or field effect transistors. The clipping characteristic of tubes are softer, but not too much softer than those of transistors. The feedback is one more thing which tends to make square wave form of the output signal. Thus, the heavy feedback in most solid state designs gives them also worse overload performance.

The differences between transistor sound and vacuum tube sound are highlighted thru the frequency spectrum and total harmonic distortion (THD) measurements. We can confirm that differences exist. We made the personal computer based hardware measurement system with MATLAB package for software support. In fig. 1 the block diagram of proposed measurement system is shown. At the input the first block is source of the corresponding input signal, with white noise data base with 1024 samples for calibration and with harmonic signal data base with frequency of 440 Hz. The second block is PC sound card with D/A conversion. The tested amplifier circuit is connected to the measurement system with input and output attenuation circuit. At the output two blocks with PC sound card with A/D data conversion serve as data acquisition structure. The results of frequency spectrum and their graphs are obtained with MATLAB software tool. With our investigations we can confirm, that there is a close parallel here between electronic distortion and musical tone coloration. The frequency of 440 Hz is chosen, because it is typical guitar signal. We observed that the visible differences between both transistors and the tube are present only at severely overloaded signals. At 50 mV typical guitar transducer output signal total harmonic distortion of 1 % for tube amplifier, 1,8% for field effect transistor amplifier and 4,9 % for bipolar transistor amplifier are obtained. The differences of the output frequency spectrum are small but noticeable, these graphs are shown in fig. 5, 6 nad 7 and the amplitude values of higher harmonic components are summarized in the table 2. When the higher harmonic distortions, for example THD=20% for crunch sound is applied, the content of higher harmonic components and their amplitudes significantly differ for our preamplifiers. These results are shown in the fig. 9, 10, 11 and are summarized in the table 4. We can see, that the tube has at the same THD the least possible amplitude values of higher harmonic components. This means especially for third harmonic component, which gives to semiconductor preamplifiers a metallic quality of sound. With comparison to all high harmonic components, the main emhasis of tube amplifier is on the second harmonic component. This is also one of the main reasons for sonorous sound of vacuum tube.

# 1 Uvod

Razprave o kvaliteti reprodukcije zvoka so že od nekdaj vroča tema inženirjev, uporabnikov ter kritikov /1/. Ocene uporabnikov temeljijo zgolj na osebnih izkušnjah in so subjektivne narave. Razmere na trgu pa dejansko kažejo, da je priljubljenost in prodaja ojačevalnikov na elektronke, posebej za kitare, velika, saj se s tem ukvarja kar nekaj podjetij. Zakaj torej polprevodniška tehnologija, ki sicer prevladuje v svetu elektronike, na tem segmentu ni izpodrinila elektronke in ali je mogoče med subjektivnimi ocenami uporabnikov in tehničnimi lastnostmi najti soglasje, sta vprašanji na kateri smo skušali poiskati odgovor. Ker se glasba ustvarja in predvaja za poslušalce in ker še vedno ne poznamo do potankosti modela človekovega slušnega sistema, tudi ne vemo natančno, katere inženirske meritve bi omogočale določitev lastnosti takšnih naprav. Vemo pa, da določena skupina poslušalcev raje posluša zvok tonskih naprav z elektronkami, naj gre za glasbene ojačevalnike, najpogosteje so to spet ojačevalniki za kitaro, studijske snemalne naprave ali preprosto kvalitetne splošne tonske naprave. Razlogi so subjektivne in objektivne narave. Nekatere razlike v kvaliteti zvoka so prav gotovo v fizikalnih razlikah med polprevodniškimi tranzistorji in elektronko ter topologijo ojačevalnega vezja. V splošnem vemo, da imajo polprevodniški ojačevalni elementi številne prednosti, zaradi katerih so v preteklosti v kratkem času na večini področjih izpodrinili elektronke. Prednosti so nesporno v manjših dimenzijah, nižjih delovnih napetostih, cenenosti, dolgi življenjski dobi, višji zgornji frekvenčni meji, skoraj neomejenih možnostih integracije in izdelavi mikroelektronskih vezij. Ostajajo pa še vedno nekatere prednosti elektronk, ki so prisotne prav na tistih področjih kjer so znane slabosti tranzistorjev: temperaturna stabilnost, toplotna obremenitev, odpornost na preobremenitve, manjše tolerance električnih karakteristik, večje dinamično področje, doseganje večjih moči. preprostejša vezja in manjša popačenja. Kako se nekatere od teh prednosti odražajo na slušnih lastnostih, bomo skušali v nadaljevanju ugotoviti s podrobnejšo analizo harmonskih popačenj pri ojačevalnem vezju z bipolarnim tranzistorjem, s tranzistorjem na poljski učinek in z elektronko.

# 2 Merilni sistem

Za izvajanje meritev harmonskih popačenj in analize frekvenčnih spektrov, s katerimi bi zasledili razlike med posameznimi ojačevalnimi elementi, smo zasnovali in izdelali računalniško podprti merilni sistem /2/, ki smo ga nadgradili s programskim paketom MATLAB. Blokovno shemo aparaturnega dela merilnega sistema prikazuje slika 1.

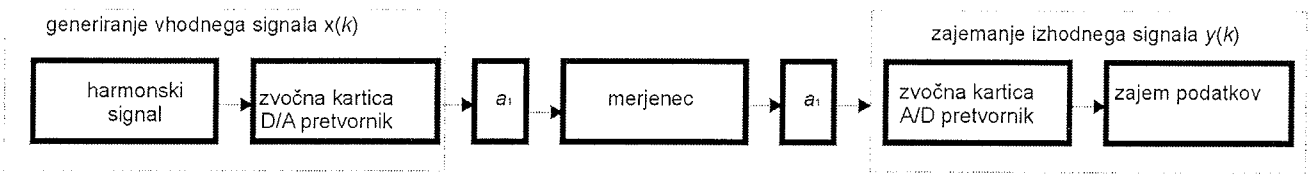
Analogni vhodni signal smo z D/A pretvornikom na zvočni kartici osebnega računalnika generirali na osnovi vnaprej pripravljene datoteke vhodnega signala. Na izhodni strani pa smo z A/D pretvornikom na zvočni kartici poskrbeli za zajemanje signala za končno obdelavo s programskim paketom MATLAB. Uporaba zasnovanega sistema je omogočila enostavno računalniško podprto meritev in izračun frekvenčnih spektrov posameznih ojačevalnih vezij. Dosegli smo tudi visoko stopnjo ponovljivosti in primerljivosti rezultatov, saj so bili generirani vzbujevalni signali enaki pri vseh meritvah. Zaradi merjenja frekvenčnih spektrov ojačevalnih vezij z elektronko, tranzistorjem na poljski učinek in bipolarnim tranzistorjem, ki so med seboj zelo različna, smo v merilno progo vključili še dve slabilni vezji $a_1$ in $a_2$, ki služita za prilagoditev posameznega ojačevalnega vezja in za poenotenje merilnih rezultatov.

Pred izvedbo meritev ojačevalnih vezij smo merilni sistem umerili z neharmoničnim signalom belega šuma /3/. Signal belega šuma smo generirali na osnovi predhodno pripravljenih vzorcev, ki smo jih izračunali s programskim paketom MATLAB. Beli šum ima konstantno gostoto spektra moči $P_X$, ki omogoča enostavno meritev amplitudne in fazne karakteristike vezij s pomočjo hitre Fourierjeve transformacije izhodnega signala. Osnovne statistične podatke belega šuma za 1024 vzorcev v periodi podaja tabela 1.

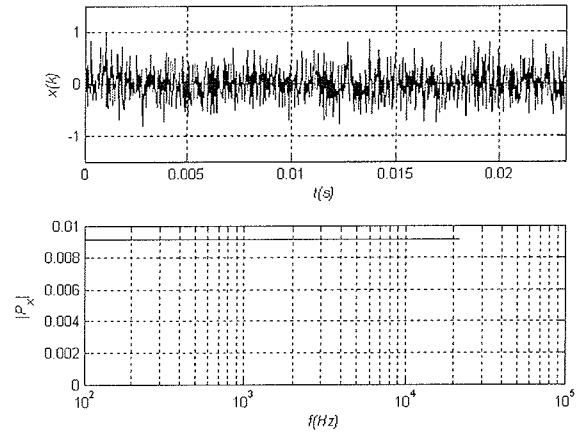
*Tabela 1: Osnovni statistični podatki signala belega šuma s 1024 vzorci*
*Table 1: Basic statistical data for 1024 samples white noise*

| Število vzorcev | 1024 |
|---|---|
| $\bar{x}$ | $6.1096 \cdot 10^{-14}$ |
| $\sigma$ | $2.9127 \cdot 10^{-01}$ |
| $x_{max}$ | 1.0000 |
| $x_{min}$ | $-8.1697 \cdot 10^{-01}$ |
| $P_x$ | $9.099010^{-03}$ |

Srednja vrednost $\bar{x}$ belega šuma gre proti vrednosti nič, amplitudne vrednosti pa so enakomerno razporejene med minimalno $x_{min}$ in maksimalno $x_{max}$ vrednost. Časovni potek $x(k)$ in spekter moči $|P_X(j\omega)|$ prikazuje slika 2.

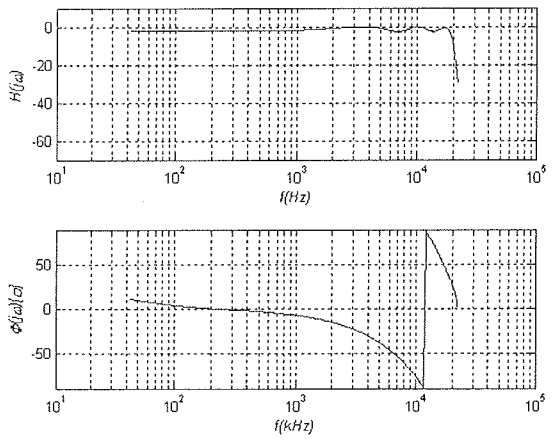



*Slika 1: Blokovna shema merilnega sistema za določitev frekvenčnega spektra*
*Fig. 1: Block diagram of the freqency spectrum measurement system*




*Slika 2: Časovni potek signala belega šuma x(k) in spekter moči $|P_X(j\omega)|$*
*Fig. 2: The time response of white noise signal x(k) and his power spectrum $|P_X(j\omega)|$*

Pri umerjanju smo izhod zvočne kartice osebnega računalnika neposredno povezali z vhodom zvočne kartice in za vhodni signal uporabili vnaprej pripravljeno datoteko 1024 vzorcev belega šuma v eni periodi. Analogno obliko signala belega šuma na vhodu smo najprej generirali z D/A pretvornikom zvočne kartice, potem pa smo ga na izhodu zajemali in vzorčili z A/D pretvornikom iste vzorčne kartice, ga pretvorili v digitalno obliko in ga shranili v izhodno datoteko tipa 'vaw'. V skriptnem jeziku programskega paketa MATLAB smo s pomočjo hitre Fourierjeve transformacije napisali program za izračun frekvenčnega odziva in s tem za analizo ustreznosti odziva merilnega sistema. Rezultate amplitudnega in faznega frekvenčnega odziva merilne sistema na beli šum prikazuje slika 3.

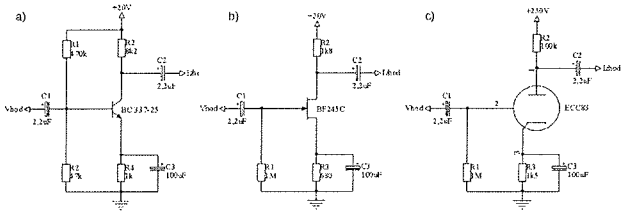



*Slika 3: Amplitudni in fazni frekvenčni odziv merilnega sistema*
*Fig. 3: The amplitude and phase frequency response of measurement system*

Iz prikazanega amplitudnega in faznega frekvenčnega odziva merilne proge vidimo, da je amplitudna frekvenčna odvisnost praktično konstantna v področju od 40Hz do 20kHz, zato pa je fazna frekvenčna odvisnost v tem področju precej nelinearna. Ker pa smo meritve izvajali v frekvenčnem območju od 400 Hz do 3500 Hz, omenjena nelinearnost ni bistveno vplivala na naše merilne rezultate.

## 3 Rezultati

Za analizo popačenj smo izdelali posamezne ojačevalne stopnje, ki so prikazane na sliki 4: predojačevalno vezje z bipolarnim tranzistorjem BC 337 je na sliki 4a, vezje s tranzistorjem na poljski učinek BF 245C na sliki 4b in vezje z elektronko ECC 83 na sliki 4c. Prikazane so tipične konfiguracije vezij z delovanjem ojačevalnega elementa v A razredu, brez negativne povratne vezave in z vrednostmi elementov, ki jih najpogosteje zasledimo pri proizvajalčevih aplikacijah za predojačevalnike. Pri bipolarnem tranzistorju smo uporabili orientacijo s skupnim emitorjem, pri FET tranzistorju orientacijo s skupnim virom in pri predojačevalniku z elektronko orientacijo s skupno katodo. Za gretje triode smo uporabili 12V enosmerno napetost.



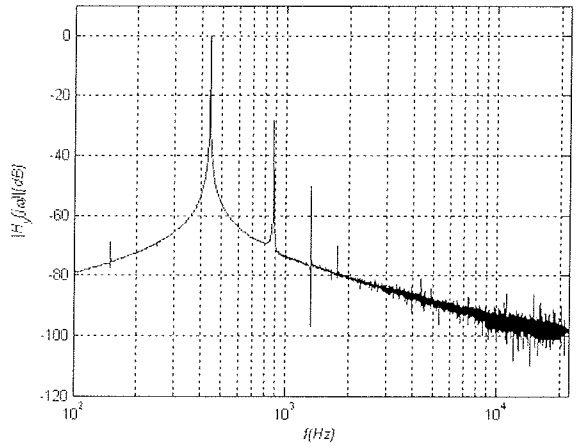

*Slika 4: Vezja predojačevalnikov: z bipolarnim tranzistorjem (a), s tranzistorjem na poljski učinek (b) in z elektronko (c)*
*Fig. 4: Preamplifier circuits with: bipolar junction transistor (a), field effect transistor (b) and vacuum tube (c)*

Ker so ojačenja posameznih ojačevalnih stopenj med seboj različna, smo za lažjo primerjavo frekvenčnih spektrov s prilagodilno stopnjo $a_2$ nastavili izhodni nivo signala na 0dB.

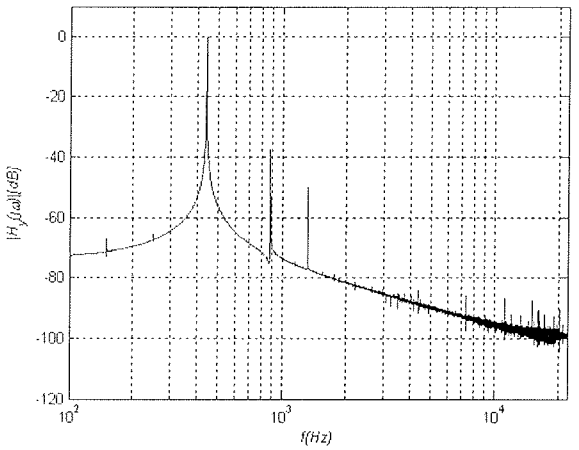
### 3.1 Meritve v linearnem režimu delovanja

Pri meritvi frekvenčnega spektra izhodnega signala smo za testni signal uporabili harmonski signal s frekvenco 440 Hz. Uporabljena frekvenca predstavlja reprezentativen ton električne kitare. Amplituda vhodnega signala je znašala 50mV, kar ustreza običajni vrednosti enojnega tonskega odjemnika pri električni kitari. S takšnim krmilnim signalom smo predpostavili delovanje ojačevalnih stopenj v linearnem režimu delovanja.

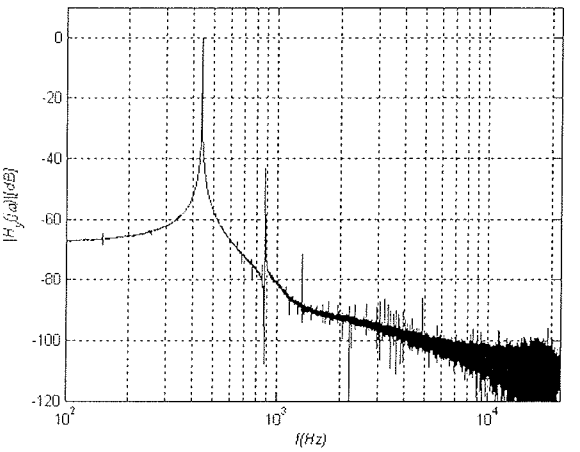
V postopku meritve smo najprej izmerili odzive ojačevalnih stopenj na harmonski vhodni signal in izračunali ter izrisali grafe frekvenčnih spektrov, potem pa še izmerili in izračunali skupna harmonska popačenja. Frekvenčne spektre $|H_y(j\omega)|$ smo iz zajetih merilnih podatkov izhodnega signala izračunali s pomočjo hitre Fourierjeve transformacije v $2^{17}$ vzorcih s programskim paketom MATLAB. Dobljeni frekvenčni spektri so prikazani na slikah 5, 6 in 7.




*Slika 5: Frekvenčni spekter predojačevalnika z bipolarnim tranzistorjem*
*Fig. 5: Frequency spectrum of bipolar transistor preamplifier*




*Slika 6: Frekvenčni spekter predojačevalnika s tranzistorjem na poljski učinek*
*Fig. 6: Frequency spectrum of field effect transistor preamplifier*




*Slika 7: Frekvenčni spekter predojačevalnika z elektronko*
*Fig. 7: Frequency spectrum of vacuum tube preamplifier*

S primerjavo posameznih grafov že zasledimo opazne razlike v vsebnosti višjih harmonskih komponent, v njihovem številu in v njihovih amplitudnih vrednostih. Predvsem zasledimo veliko manjši delež tretje harmonske komponente pri elektronki. Z zmanjševanjem vhodnega signala se skupna harmonska popačenja sicer zmanjšujejo, klub temu pa se ohranjajo značilni vzorci frekvenčnih spektrov. Amplitudne vrednosti posameznih višjih harmonskih komponent nam v primerjavi z osnovno harmonsko komponento, ki je postavljena na 0dB, prikazuje tabela2.

*Tabela 2: Amplitudne vrednosti osnovne in višjih harmonskih komponent pri ojačevalnih stopnjah v linearnem področju delovanja*
*Table 2: The amplitude values for first and higher harmonic components in preamplifiers in linear region*

| | *harmonska komponenta dB* $f_n$(kHz) | | | | |
|---|---|---|---|---|---|
| *ojačevalni element v vezju* | *1.* *0,440* | *2.* *0,881* | *3.* *1,321* | *4.* *1,760* | *5.* *2,200* |
| *BJT* | *0* | *-28* | *-50,* | *-70* | *-79* |
| *FET* | *0* | *-38* | *-50* | *-77* | *-80* |
| *elektronka* | *0* | *-43* | *-72* | - | - |

Skupna harmonska popačenja (THD) smo najprej izmerili s klasičnim merilnikom harmonskih popačenj HM8027 nato pa še izračunali po izvorni definiciji na osnovi izmerjenih višji harmonskih komponent, z izrazom,

$$THD = \frac{\sqrt{\sum_{k=2}^{N} U_{2k}^2}}{U_1} \cdot 100\%$$

V izrazu za THD je *N* število upoštevanih višjih harmonskih komponent v izhodnem signalu $U_{2n}$ in $U_1$ osnovna harmonska komponenta. Izvorna definicija je natančnejša pri večjih popačenjih, pri popačenjih do 10 % pa ni večjih razlik glede na meritev, kot je prikazano v tabeli 3.

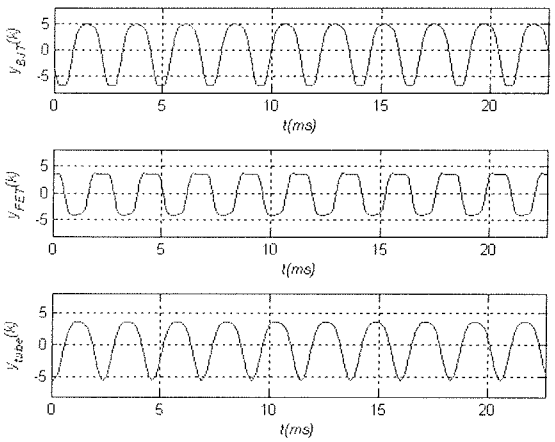
*Tabela 3: Skupna harmonska popačenja posameznih predojačevalnih vezij*
*Table 3: Total harmonic distortion for preamplifier circuits*

| *ojačevalni element v vezju* | *meritev* | *Izračun* |
|---|---|---|
| *BJT* | *4,90%* | *4,99%* |
| *FET* | *1,85%* | *1,78%* |
| *elektronka* | *1%* | *0,90%* |

Zlahka lahko ugotovimo, da so pri bipolarnem tranzistorju prisotna največja skupna harmonska popačenja. Pogojena so z različnimi ojačenji, nelinearnostjo karakteristik, različnim dinamičnim območjem delovanja in posledično z različno vsebnostjo višjih harmonskih komponent.

## 3.2 Meritve v prekrmiljenem režimu delovanja

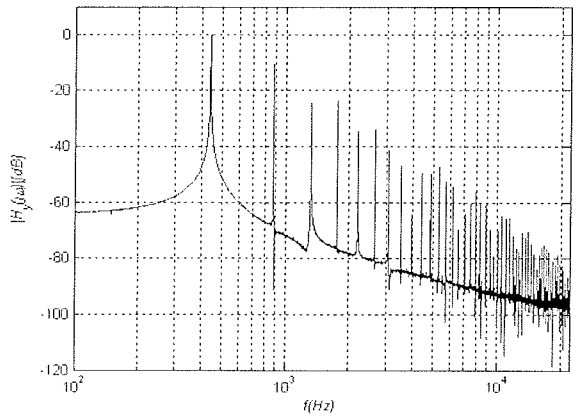
Pri meritvah v prekrmiljenih razmerah smo na vhod posameznih predojačevalnih vezij ponovno pripeljali harmonski signal frekvence 440Hz. S prilagodilno stopnjo $a_1$ smo na vhodu nastavili nivo signala na takšno vrednost, da je znašala izmerjena vrednost skupnih harmonskih popačenj 20%. To je izkustvena vrednost skupnih harmonskih popačenj /2/ za hreščeč zvočni učinek. Spet smo za poenoten prikaz dobljenih grafov frekvenčnih spektrov s pomočjo prilagodilne stopnjo $a_2$ nastavili nivo izhodnega signala tako, da je znašala amplituda prve harmonske komponente 0dB. Slika 8 prikazuje časovne poteke izhodnih signalov vseh treh predojačevalnikov v prekrmiljenem stanju pri istih skupnih harmonskih popačenjih.




*Slika 8: Časovni poteki izhodnih signalov predojačevalnikov z bipolarnim tranzistorjem, $y_{BJT}$, tranzistorjem na poljski učinek, $y_{FET}$ in elektronko, $y_{tube}$*

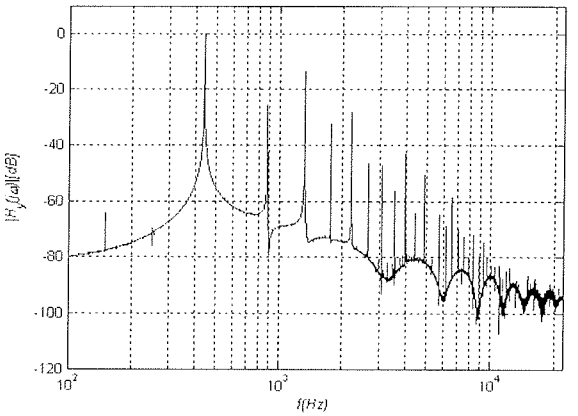
*Fig. 8: The output waveforms for preamplifiers with BJT, $y_{BJT}$,, FET, $y_{FET}$ and tube, $y_{tube}$*

S slike 8 vidimo, da se časovni poteki izhodnih signalov predojačevalnikov pri isti stopnji prekrmiljenja (THD=0,2) med seboj precej razlikujejo. Do razlik pride zaradi različnih vsebnosti višjih harmonskih komponent. To je prikazano na slikah 9, 10 in 11, kjer podajamo frekvenčne spektre vseh treh vezij.



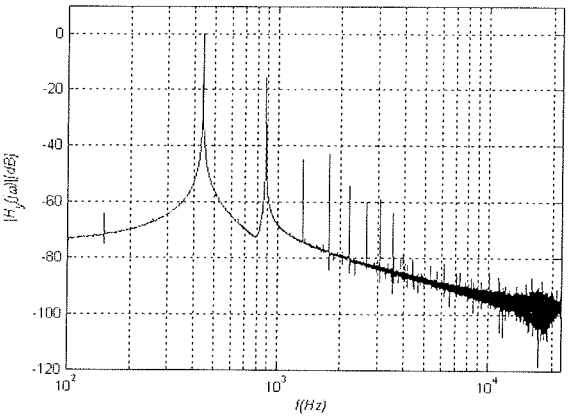

*Slika 9: Frekvenčni spekter predojačevalnika z bipolarnim tranzistorjem pri 20% harmonskih popačenjih*

*Fig. 9: The frequency spectrum of preamplifier with bipolar junction transistor at 20% total harmonic distortion*




*Slika 10: Frekvenčni spekter predojačevalnika s tranzistorjem na poljski učinek pri 20% skupnih harmonskih popačenjih*

*Fig. 10: The frequency spectrum of preamplifier with field effect transistor at 20% total harmonic distortion*




*Slika 11: Frekvenčni spekter predojačevalnika z elektronko pri 20% harmonskih popačenjih*

*Fig. 11: The frequency spectrum of preamplifier with vacuum tube at 20% harmonic distorsions*

Amplitudne vrednosti posameznih višjih harmonskih komponent frekvenčnih spektrov posameznih predojačevalnikov nam v primerjavi z osnovno harmonsko komponento, ki je postavljena na 0dB, prikazuje tabela 4.

*Tabela 4: Amplitudne vrednosti osnovne in višjih harmonskih komponent pri ojačevalnih stopnjah pri 20% skupnih harmonskih popačenjih*
*Table 4: The amplitude values for first and higher harmonic components at preamplifiers at THD= 20%*

| | harmonska komponenta dB $f_n$(kHz) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| ojačevalni element v vezju | 1. 0,440 | 2. 0,881 | 3. 1,321 | 4. 1,760 | 5. 2,200 | 6. 2,640 | 7. 3,080 | 8. 3,520 |
| BJT | 0 | -10 | -24 | -24 | -35 | -34 | -41 | -47 |
| FET | 0 | -26 | -14 | -32 | -28 | -47 | -47 | -43 |
| elektronka | 0 | -16 | -45 | -43 | -54 | -60 | -59 | -64 |

Šele pri prekrmiljenem delovanju posameznih ojačevalnih stopenj pridejo do izraza razlike med bipolarnim tranzistorjem, tranzistorjem na poljski učinek in posebej elektronko. Na zaznavanje zvoka pri človeku v največji meri vpliva uho. Karakteristiko ušesa podaja Fletcher-Munson-ov graf /4/ ki pa kaže le frekvenčno odvisnost ušesa od nivoja glasnosti. Dobljen je na osnovi zaznavanja glasnosti čistih tonov. Povsem drugače je pri signalih, ki so popačeni in polni višjih harmonskih komponent. Med harmonskimi popačenji signala, gledano iz tehničnega vidika in barvitostjo tona, gledano iz glasbenega vidika, lahko po mnenju nekaterih avtorjev potegnemo nekakšne paralele /5/. Osnovna barvna karakteristika tona se skriva v moči višjih harmonskih komponent. Vsaka harmonska komponenta daje svoj karakteristični učinek, če je dominantna. V primeru, da je harmonska komponenta izrazita, spreminja vpliv ostalih komponent. Primer takšnega vpliva je t.i. učinek čebelice, ko zaradi karakteristike ušesa postane neka višja harmonska komponenta zaznavnejša od osnovne in se s tem karakteristični pomen posameznih harmonskih komponent spremeni. S tem se spremeni tudi obarvanost tona.

Višje harmonske komponente lahko razdelimo v dve skupini /5, 6/. Lihe harmonske komponente (tretja in peta), dajeta zamašen in zaprt zvok, medtem ko sode komponente (druga, četrta in šesta) dajejo zborovski in pojoč zvok. Višje harmonske komponente (nad sedmo) dajejo zvoku ostrino. Z glasbenega stališča sode harmonske komponente predstavljajo oktavo, ki jo je težje razločiti od osnovnega tona, vendar pa daje zvoku polnejši karakter. Tretja harmonska komponenta predstavlja kvinto in daje kovinski prizvok, če je njena amplituda dovolj velika. Harmonske komponente, ki dajejo ostrino so z glasbenega vidika nesorodne z osnovnim tonom in kadar so preveč izrazite vnašajo razglašen prizvok.

# 4 Zaključek

Analiza popačenj ojačevalnih vezij z bipolarnim tranzistorjem, tranzistorjem na poljski učinek in vakuumsko elektronko potrjuje nekatere ugotovitve glasbenikov in njihovih somišljenikov, da so pri posameznih ojačevalnih elementih prisotne slišne razlike.

Z meritvami frekvenčnih spektrov in skupnih harmonskih popačenj smo potrdili razlike v vsebnosti višjih harmonskih komponent pri ojačevalnih stopnjah z različnimi ojačevalnimi elementi in s tem tudi sonorne razlike v izhodnem signalu posameznih ojačevalnikov. Zlahka lahko ugotovimo, da so pri bipolarnem tranzistorju prisotna največja skupna harmonska popačenja v primerjavi s tranzistorjem na poljski učinek in posebej v primerjavi z elektronko. Pogojena so z različnimi ojačenji ojačevalnih elementov, nelinearnostjo karakteristik, različnim dinamičnim območjem in posledično z različno vsebnostjo višjih harmonskih komponent, v njihovem številu in v njihovih amplitudnih vrednostih. Predvsem zasledimo veliko manjši delež tretje harmonske komponente pri elektronki.

Razlike med posameznimi ojačevalnimi elementi pridejo do izraza šele pri prekrmiljenem delovanju ojačevalnih stopenj. Pri 20 odstotni vrednosti skupnih harmonskih popačenj je postala vsebnost višjih harmonskih komponent v izhodnem signalu elektronke bistveno drugačna od tiste pri bipolarnem oziroma tiste pri tranzistorju na poljski učinek. Z glasbenega stališča dajejo sode harmonske komponente polni karakter. Tretja harmonska komponenta daje kovinski prizvok, če je njena amplituda dovolj velika. Harmonske komponente, ki dajejo ostrino so z glasbenega vidika nesorodne z osnovnim tonom in v primeru izrazitih amplitud vnašajo prizvok razglašenosti. Glede na vsebnost višjih harmonskih komponent ima elektronka najbolj poudarjeno drugo harmonsko komponento. Ker ima vse ostale, posebej velja to za tretjo harmonsko komponento, tudi do sto krat manjše, ima z glasbenega vidika najprijetnejši zvok.

Predstavljene in opisane meritve in merilni rezultati običajnemu poslušalcu ne povedo veliko, za strokovnjaka s tehniškega področja pa so praktično edina povratna informacija o tem, kaj se dejansko dogaja v ojačevalniku. Klasični merilnik harmonskih popačenj nam daje le oceno prisotnosti popačenj, ne pa nudi vpogleda v strukturo signala. Z relativno preprostim merilnim sistemom pa nam je uspelo dobiti poleg skupnih harmonskih popačenj tudi vpogled v frekvenčni spekter signala, v vsebnost višjih harmonskih komponent in s tem v razširjeno sliko o signalu, iz katere lahko poiščemo sonorne lastnostih signala. Kako dolgo bo elektronka še uspela zadržati svoje mesto na področju ojačevalnikov za kitaro in profesionalne tonske opreme, je vprašanje časa. Hiter napredek vseh vrst signalnih procesorjev, tudi takšnih posebnih za simulacijo zvočnih lastnosti elektronk, jih bo v bližnji prihodnosti zanesljivo nadomestil in izpodrinil.

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*izr. prof. dr. Rudolf Babič, tel.: (02) 220-7230, e-mail: rudolf.babic@uni-mb.si*
*dr. Davorin Osebik, tel (02) 220-7238, e-mail: davorin.osebik@uni-mb.si*
*Univerza v Mariboru*
*Fakulteta za elektrotehniko, računalništvo in informatiko, Smetanova 17, 2000 Maribor*
*Tel.: (02) 220 7000, Fax (02) 220 7272*

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# VARIATIONS OF COLOR CORRELATED TEMPERATURE OF WHITE LED LIGHT

Mitja Prelovšek, Grega Bizjak

Univerza v Ljubljani, Fakulteta za elektrotehniko, Ljubljana, Slovenia

**Key words:** Light-emitting diodes, white LED, correlated color temperature CCT, CCT consistency, color rendering index, illumination, solid state lighting sources

**Abstract:** Correlated color temperature (CCT) variations and low color rendering index (CRI) present many reasons for not using white light-emitting diodes (LEDs) in lighting. In this research color characteristics of light emitted by LEDs were measured on 29 (In)GaN LEDs of 6 different kinds.We found that color characteristics, notably CCT, are significantly dependent on distance from geometrical axis of the LED, of which the ones that do not use light-diffusion layer were more susceptible to CCT variations. Furthermore, variations of color characteristics of LEDs belonging to the same type were significantly higher than the minimum color difference that human eye can notice. The obtained data suggest, that in order to achieve sufficient light quality and color consistency between different white LEDs, diffusion layer use is highly recommended, due to its smoothing effect.

# Razlike v najpodobnejši barvni temperaturi svetlobe belih LED

**Kjučne besede:** svetleče diode, bele LED, najpodobnejša barvna temperatura CCT, konsistentnost CCT, indeks barvnega videza, razsvetljava, polprevodniški svetlobni viri

**Izvleček:** Razlike v najpodobnejši barvni temperaturi in indeksu barvnega videza predstavljajo danes glavno oviro pri uporabi belih svetlečih diod (LED) v razsvetljavi. V opisani raziskavi smo izmerili osnovne značilnosti barve svetlobe pri skupaj 29 (In)GaN belih svetlečih diodah šestih različnih tipov. Ugotovili smo, da je najpodobnejša barvna temperatura (CCT) svetlobe LED zelo odvisna od kota opazovanja glede na geometrično os LED. Pojav je najbolj izražen pri LED, ki nimajo nanesenega difuzijskega sloja za razprševanje svetlobe. Ugotovili smo tudi, da so razlike v najpodobnejši barvni temperaturi svetlobe pri LED istega tipa večje, kot je meja zaznavnosti pri človeku. Pridobljeni podatki kažejo, da je za uporabo v razsvetljavi priporočljiva edino uporaba belih LED z difuzijskim slojem, če želimo doseči ustrezno kakovost barve svetlobe.

## 1 Introduction

Color temperature is a way of describing the hue of white light. The term color temperature originates from the correlation between temperature of planckian black body and its emission spectrum. For example, planckian body heated to 3000 K radiates white light with reddish hue, while at 6000 K the light adopts a bluish hue. The hues and corresponding temperatures are shown on Fig 1, which presents a CIExy color space, while the Table 1 presents the exact CCT values with corresponding x,y coordinates.

The term correlated color temperature (CCT) is used with light sources, that do not function as black body radiators and therefore, the color of the emitted light does not follow the planckian curve plotted on Fig 1. CCT can be obtained by an algorythm, which moves the color of light source on the planckian curve with a minimum visual change in hue. Obviously this procedure can lead to significant mistakes in color representation, especially if there exists a significant offset of the color of the emitted light from the planckian curve.

The CIExy color space, which is shown on Fig 1, is a much more accurate way of specifying color of light. This method of color representation is therefore the prefered one

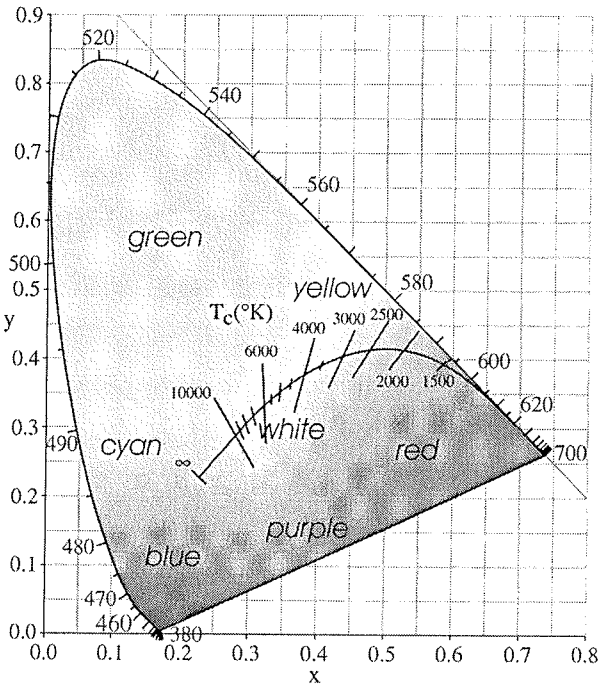


*Fig 1: CIExy diagram with planckian curve*

*Table 1: CCT and CIExy coordinates equivalents*

| T/K | x | y |
|---|---|---|
| 2000 | 0,52669 | 0,41331 |
| 2353 | 0,49059 | 0,41498 |
| 2500 | 0,47701 | 0,41368 |
| 3077 | 0,43156 | 0,40216 |
| 3333 | 0,41502 | 0,39535 |
| 3636 | 0,39792 | 0,3869 |
| 4000 | 0,38045 | 0,37676 |
| 4444 | 0,36276 | 0,36496 |
| 5000 | 0,3451 | 0,35162 |
| 5714 | 0,32775 | 0,3369 |
| 6667 | 0,31101 | 0,32116 |
| 8000 | 0,29518 | 0,30477 |
| 10000 | 0,28063 | 0,28828 |
| 12500 | 0,27011 | 0,27547 |
| 14286 | 0,26526 | 0,2693 |
| 16667 | 0,2607 | 0,26333 |
| 20000 | 0,25645 | 0,25763 |
| 25000 | 0,25251 | 0,25222 |

when measuring LEDs. The biggest advantage of CIExy color space, however, is accurate representation of the perceived color of light containing various distinct peaks in its spectrum. For example, if there are only red and blue components in the spectrum of incident light, then the perceived color of light will be on the line connecting the red point and blue point in CIExy space. Similarly, when there are three or more components in the spectrum, then the perceived color of light is somewhere inside the geometrical shape, which connects all the points in CIExy space.

The CIExy space has 2 coordinates, which allow representation of every color detectable by human eyes. Coordinate x is roughly proportionate to the amount of red color, while y represents the amount of green.

## 2 White LEDs

There are three different technologies of producing white light by using LEDs. First and perhaps the most known way of achieving white light is by mixing light of red, green and blue LEDs with appropriate luminances. This mixture of wavelengths is interpreted as white light by our visual system. The advantage of this principle is, that any color in the triangle in CIExy color space, which connects those three primary colors, can be achieved. However, the costs of the installation are often too high, especially when dynamic color changes are not required.

The second principle is based on luminiscence of red, green and blue phosphor coatings, which are placed over near-UV LED chip. The UV light excites the phosphors, which consequently down-shift UV light into three broad peaks in red, green and blue interval of the spectrum. The n-UV LED chip + RGB phosphors is a technology which is still in its infancy, where the efficiency of such n-UV LED chip and wavelength conversion is too low for illumination applications.

The most widely used white LED technology uses blue LED GaN chips coated with yellow phosphor, which down-shifts part of emitted blue light to yellow wavelengths. The right mixture of yellow and blue spectral components is perceived as white light, which can be seen from Fig 2.

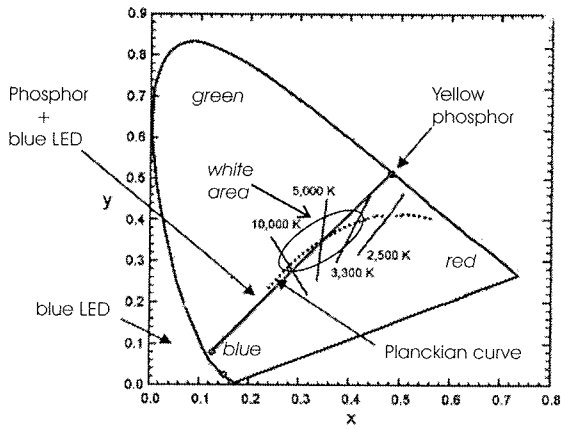


*Fig 2: CIExy diagram with line connecting color coordinates of blue LED and yellow phosphor*

This kind of white LED has only 2 peaks in its spectrum, as shown on Fig 3, and consequently very low color rendering index (CRI).

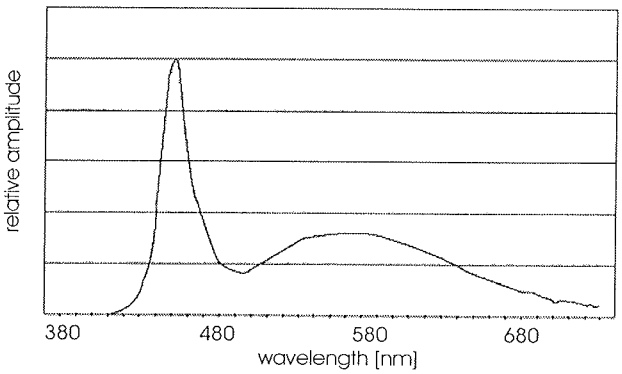


*Fig 3: Spectrum of GaN white LED*

However, low CRI is not the only weakness of this type of white LEDs. The other major disadvantage originates from the fact, that the amount of yellow, which is represented in the spectrum, is directly proportionate to the distance through yellow phosphor, that has to be traversed by the emitted light. Furthermore, since that distance is bigger at larger angles of observation, CCT depends not only on

the thickness of the phosphor coating, but also on the angle of observation as shown on the following figure. Here $d_1$ and $d_2$ label distances through phosphor at an arbitrary angle and on the geometrical axis.

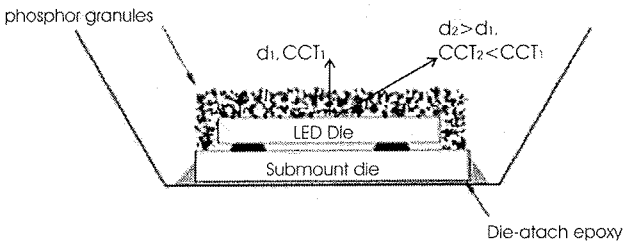


*Fig 4: GaN white LED structure*

CCT variations and dependancies of GaN white LEDs, that are mentioned above, were measured on 3 types of through-hole LEDs, 2 types of high-output LEDs with diffusion layer and 1 type of high-output LED without diffusion layer. The corresponding viewing angles or maximum radiation angles are presented in Table 2, where diodes have been labeled according to their type with TH, HOD or HO, meaning through-hole, high-output diffusion and high-output respectively.

*Table 2: measured LEDs*

| Label | Viewing angle | Number of LEDs |
|---|---|---|
| TH1 | 10° | 5 |
| TH2 | 15° | 5 |
| TH3 | 15° | 5 |
| HOD1 | 110° | 5 |
| HOD2 | 110° | 4 |
| HO | >90° | 5 |

A typical through-hole, high-output diffusion and high-output LED can be seen on Fig 5, Fig 6 and Fig 7 respectively.

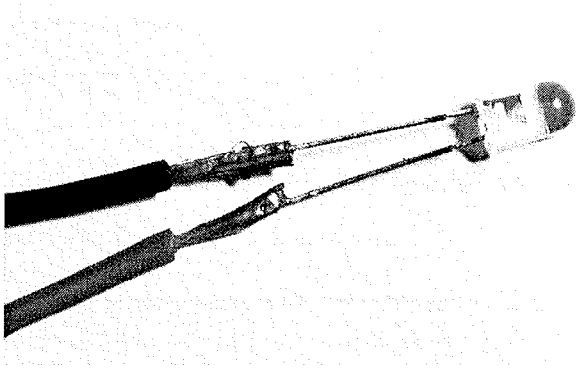

*Fig 5: through hole LED*

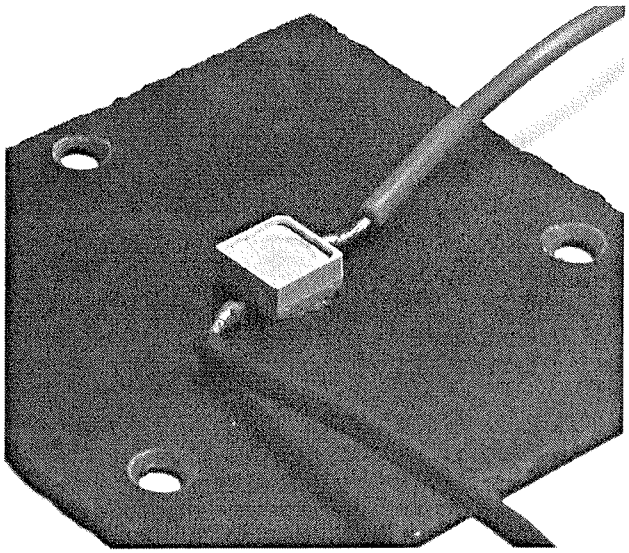

*Fig 6: high output LED with diffusion layer positioned on the measurement holder*

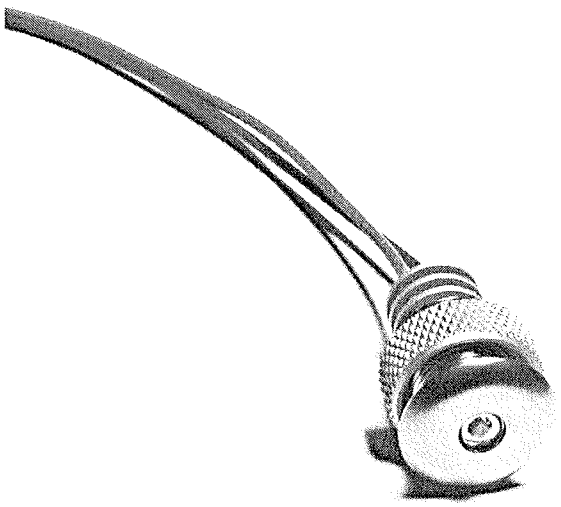

*Fig 7: high output LED*

## 3 Experimental procedures

CCT was measured by rotating the LEDs around their vertical and geometrical axis as shown on Fig 8.

LEDs were rotated on two custom-made holders, while the CCT data were measured by a spectrometer, which was positioned 10cm from the LED. Position of the instruments is shown on the following figure.

The rotation around vertical axis was in our experiment limited to 70 degrees, because 70 degrees present the angle where luminous flux is usually cut off in normal white LED applications. That is achieved either by a reflector of some sort or the LED itself includes lenses that limit the viewing angle, which is a standard practice with indicator LEDs. Therefore, we have set the angle $\varphi$ either to the

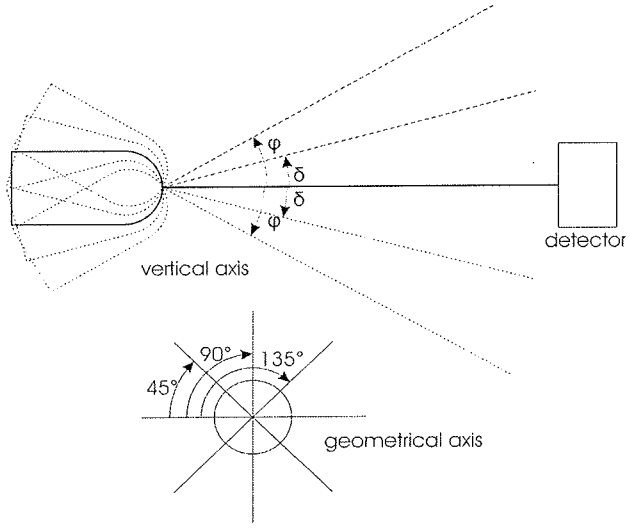


*Fig 8: rotation around geometrical and vertical axes*

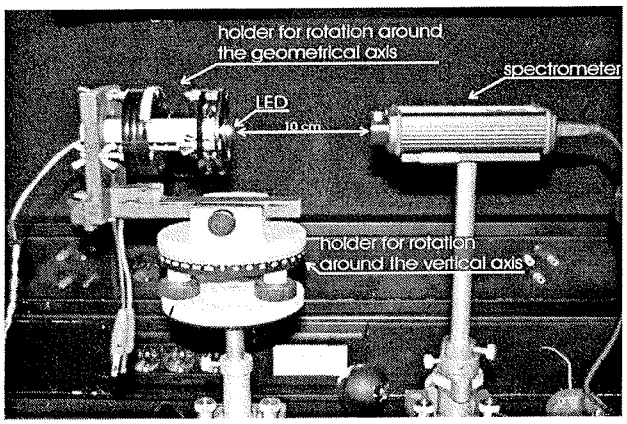


*Fig 9: position of the instruments*

viewing angle of the LED or to 70 degrees, if the viewing angle of the LED exceeded 70 degrees. Measurement angle δ was approximately one half of φ. Measurement angles for corresponding LEDs are shown in Table 3.

*Table 3: Measurement angles*

| Label | δ | φ |
|---|---|---|
| TH1 | 5° | 10° |
| TH2 | 7° | 15° |
| TH3 | 7° | 15° |
| HOD1 | 35° | 70° |
| HOD2 | 35° | 70° |
| HO | 35° | 70° |

With this procedure we obtained 17 different measurement points, which are shown as black dots in the following figure:

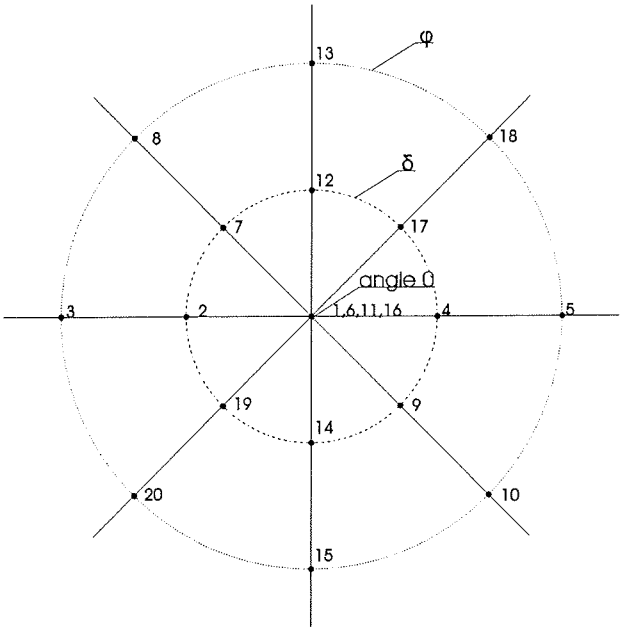


*Fig 10: Measurement points*

Since all of the measured LEDs showed significant CCT dependance on the measurement angle, it was decided, that we will calculate 3 CCT averages for every type of LED - one for every measurement angle (0, δ, φ). Thus we could evaluate the dependance of CCT on the angle of observation.

As for CCT variance calculations, we wanted to be able to evaluate CCT variations, which can be noticed, when an observer looks at a luminaire which employs a cluster of LEDs. The observer is in this very typical LED application able to notice the maximum and minimum CCT variations of separate LEDs compared to an average CCT of the whole cluster at that specific angle of observation. Therefore we calculated the variances separately for every measurement point (Fig 10). The average used for variance calculation was the average of measurements of the same measurement angle, that the measurement point belonged to. For example: to calculate a variance in point 4 (Fig 10), we used 5 CCT measurements of the point 4 (one for every LED in the group) along with the average of 40 CCT measurements (5-times 8, for 5 LEDs in a group and 8 measurement points at the measurement angle δ).

## 4 Results and discussion

As mentioned above, CCT data of all of the measured LEDs have shown significant dependance on the measurement angle, that is whether the measurement point belonged to 0, δ or φ. All of the LEDs without light diffusion layer have shown significant decrease in CCT with increasing measurement angle, while the CCT of LEDs with diffusion layer was slightly higher at angle φ compared to values at angles 0 or δ, as can be seen from Table 4 and Fig 11

*Table 4: dependance of CCT from measurement angle*

| CCT[K] | angle 0 | angle δ | angle φ |
|---|---|---|---|
| TH1 | 7427 | 7174 | 6487 |
| TH2 | 15840 | 11358 | 7137 |
| TH3 | 16100 | 8062 | 7756 |
| HOD1 | 5787 | 5805 | 5850 |
| HOD2 | 6118 | 6132 | 6140 |
| HO | 5509 | 5408 | 5226 |

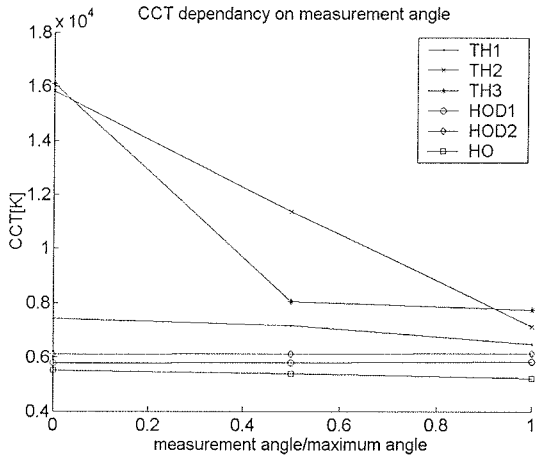


*Fig 11: CCT variation*

These data suggest that unevenly spread diffusion layer on LEDs HOD1 and HOD2 caused the reverse dependance of CCT, which can be seen in Fig 11

To better evaluate the perceived differences in color of light, however, it is more precise to use the distance between two points in CIExy space as a representation. Table 5 and Fig 12 show distances of CCT averages at δ and φ to CCT average on geometrical axis. Minimum difference in color, that human visual system can detect, is approximately 50K to 100K [2] in range of daylight variations, which span from 2000K to 6000K. 100K equals approximately 0.007, which is also shown on Fig 12. For an observer it presents a boundary, when he/she notices the change of color of the emitted light.

*Table 5: Distances from central average in CIExy space*

| Distance in CIExy space | angle δ | angle φ |
|---|---|---|
| TH1 | $4.98 \cdot 10^{-3}$ | $2.3 \cdot 10^{-2}$ |
| TH2 | $2.59 \cdot 10^{-2}$ | $6.38 \cdot 10^{-2}$ |
| TH3 | $6.87 \cdot 10^{-2}$ | $6.5 \cdot 10^{-2}$ |
| HOD1 | $6.13 \cdot 10^{-4}$ | $2.79 \cdot 10^{-3}$ |
| HOD2 | $2.95 \cdot 10^{-4}$ | $4.75 \cdot 10^{-4}$ |
| HO | $5.96 \cdot 10^{-3}$ | $1.68 \cdot 10^{-2}$ |

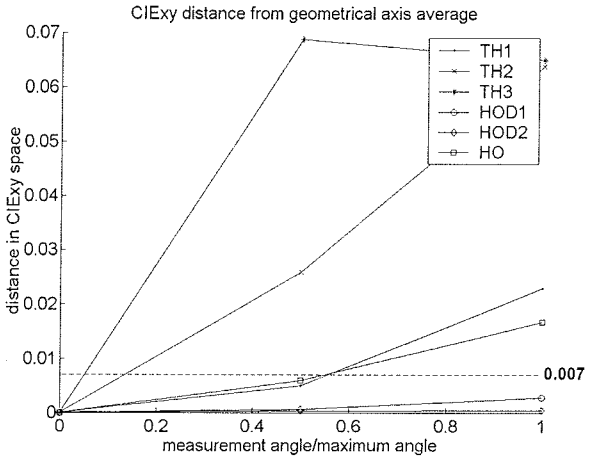


*Fig 12: CCT variation shown as distance in CIExy space*

It can be observed, that LEDs, which use diffusion layer show the best performance in terms of angular stability of CCT. Furthermore, these types of LEDs are the only ones, that remain below the minimum noticeable distance in CIExy space, regardless of the measurement angle. It is thought, that use of diffusion layer with GaN+yellow phosphor white LEDs has positive effect on angular stability of CCT.

There is, however, another obstacle, which must be dealt with, when using white LEDs and these are differences in light color between different LEDs. We calculated 17 variances, one for every measurement point, for each type of LEDs, as explained in chapter 3. The maximum variances at each angle are shown in Table 6 and Fig 13.

*Table 6: Maximum variances at measurement angles*

| Maximum variances | angle 0 | angle δ | angle φ |
|---|---|---|---|
| TH1 | $9.5 \cdot 10^{-3}$ | $1.26 \cdot 10^{-2}$ | $1.99 \cdot 10^{-2}$ |
| TH2 | $2.35 \cdot 10^{-2}$ | $2.7 \cdot 10^{-2}$ | $1 \cdot 10^{-2}$ |
| TH3 | $1.73 \cdot 10$ | $2.8 \cdot 10^{-2}$ | $2.28 \cdot 10^{-2}$ |
| HOD1 | $4.9 \cdot 10^{-3}$ | $5 \cdot 10^{-3}$ | $5.8 \cdot 10^{-3}$ |
| HOD2 | $2.4 \cdot 10^{-3}$ | $2.99 \cdot 10^{-3}$ | $9 \cdot 10^{-3}$ |
| HO | $7.98 \cdot 10^{-3}$ | $7.9 \cdot 10^{-3}$ | $8.18 \cdot 10^{-3}$ |

Again it can be seen, that HOD1 and HOD2 show the best performance, as they are in general always below the noticeable distance in CIExy space. This can be explained with luminance distribution of GaN white LEDs. The point of the highest luminance, which is called the optical axis of the LED, corresponds with the point of the highest CCT. This is because yellow phosphor can down-shift only a limited amount of light. However, optical axis does not, in general, correspond with geometrical axis of the LED and therefore the point of highest CCT is very rarely positioned on the geometrical axis of the LED itself. As the positioning of the LEDs in our experiment did not reflect the direc-

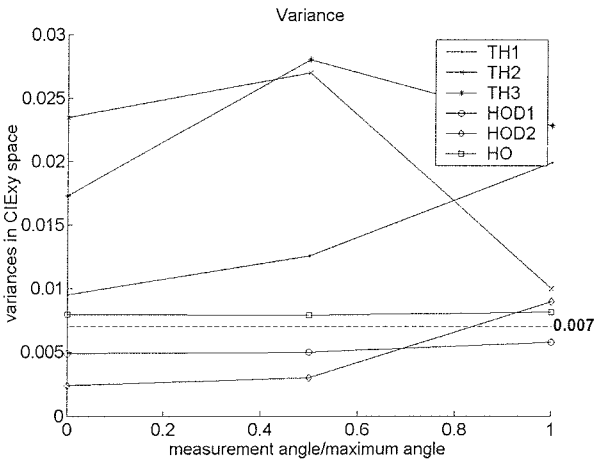


*Fig 13: Maximum variances shown as distance in CIExy space*

tion of the optical axes in any way, it is suggested, that these position variations of the optical axes are the origin of the variances of LEDs without diffusion layer shown in Fig 13. The advantage of using diffusion layers regarding the optical axes problem mentioned above is, that it smooths out the CCT gradient of the LED and consequently makes position variations of the optical axes less noticeable.

## 5 Conclusion

Considering the fact, that LEDs without diffusion layer showed poor performance in terms of CCT variations, it is thought, that the prevailent technology of manufacturing white LEDs today is not capable of enabling a widespread use of white LEDs in illumination. However, use of diffusion layers on LEDs can greatly improve their characteristics, especially in terms of angular stability of CCT.

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*Mitja Prelovšek u.d.i.e.*
*Zarnikova 11, 1000 Ljubljana*
*Tel: 040298550*

*doc dr Grega Bizjak u.d.i.e.*
*Univerza v LjubljaniFakulteta za elektrotehniko*
*Tržaška 25, 1000 Ljubljana*
*Tel: 014768446*
*Email: grega.bizjak@fe.uni-lj.si*

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# APPLICATION OF EXTRAPOLATION ALGORITHMS IN NONLINEAR CIRCUIT SIMULATION AND OPTIMIZATION WITH SPICE OPUS

Borut Wagner, Árpád Bűrmen, Janez Puhan, Sašo Tomažič, Tadej Tuma

University of Ljubljana, Faculty of Electrical Engineering, Ljubljana, Slovenia

**Key words:** extrapolation algorithms, circuit simulation, circuit optimization, integrated circuit design, SPICE.

**Abstract:** In this paper the extrapolation algorithms for vector sequence acceleration are presented. Four extrapolation algorithms are described and their application to circuit simulation is discussed. Steady state evaluation times are compared for the presented extrapolation algorithms and the direct method on real-world test circuits. Results show that the most appropriate extrapolation algorithm for evaluating the steady state of a circuit is the epsilon algorithm. The epsilon algorithm was implemented in SPICE OPUS circuit simulator. The implemented epsilon algorithm was used for optimizing the steady-state response of a test circuit. The accelerated evaluation makes the optimization of steady-state response possible.

# Uporaba ekstrapolacijskih postopkov pri simulaciji in optimizaciji nelinearnih vezij s programskim paketom SPICE OPUS

**Kjučne besede:** ekstrapolacijski postopki, simulacija električnih vezij, optimizacija električnih vezij, načrtovanje integriranih vezij, SPICE.

**Izvleček:** V članku so predstavljeni ekstrapolacijski postopki, ki se uporabljajo za pospeševanje konvergence zaporedij. Opisani so štirje postopki in njihov način uporabe pri simulaciji električnih vezij. Podana je primerjava časov za računanje stacionarnega stanja testnih električnih vezij brez in z uporabo ekstrapolacijskih postopkov. Za implementacijo v programski paket SPICE OPUS je bil izbran epsilon algoritem, ki se je izkazal za najbolj primernega. Postopek je bil uporabljen tudi pri optimizaciji testnega vezja. Zaradi hitrejšega izračuna samega stacionarnega stanja se je pohitril tudi celoten postopek optimizacije stacionarnega stanja in postal primeren za praktično uporabo.

## 1 Introduction

Extrapolation algorithms for vector sequences /1,2,3,4/ are used for accelerating sequences that converge slowly. The limit of a sequence can be calculated efficiently by evaluating only a few terms of the sequence without the explicit knowledge of the sequence generator. Using an extrapolation algorithm and only few terms of the sequence, a new initial term of the sequence can be calculated. With the new initial term, further terms of the sequence are evaluated by the sequence generator. The procedure is iterated until the differences between consequent terms of the sequence are small enough to assume that we are close to the limit of the sequence.

When computing the steady-state response /5/ of a nonlinear circuit all signals in the circuit are assumed to have the same fundamental frequency $f$ and the period $T = 1/f$. The circuit is simulated starting at some initial condition until steady state is reached. Simulation results $\mathbf{x}(t)$, $t \geq 0$ represent node voltages and branch currents of the circuit at time t. The sequence $\left\{\mathbf{x}_0^{(i)} = \mathbf{x}(iT)\right\}$, i = 0,1,2,3 is convergent if the circuit has a steady-state response with period $T$.

To accelerate the computation of steady state, the circuit is simulated for n periods and the extrapolation method is used on vectors $\mathbf{x}_0^{(0)}, \mathbf{x}_0^{(1)}, \mathbf{x}_0^{(2)}, \ldots \mathbf{x}_0^{(n)}$ to compute the new initial vector $\mathbf{x}_1^{(0)}$. Then the circuit is simulated starting with initial conditions $\mathbf{x}_1^{(0)}$ and the new sequence $\left\{\mathbf{x}_1^{(i)} = \mathbf{x}(iT)\right\}$, i = 0,1,2,3 is extracted from the response of the circuit. This is repeated $k$-times until $\left\|\mathbf{x}_k^{(n)} - \mathbf{x}_k^{(0)}\right\|$ is small enough to assume the circuit is in steady state.

The paper is organized as follows. In Section 2 a brief description of four extrapolation algorithms (epsilon algorithm, rho algorithm, theta algorithm and topological epsilon algorithm) is given. In Section 3 the simulation of electrical circuits with SPICE OPUS is presented. Problems that occur when steady-state response of circuits has to be computed are presented. The acceleration of the steady-state response computation by means of extrapolation algorithms is described. In Section 4 simulation times for the test circuits (Greinacher rectifier, narrow-band filter, switching power supply) are compared for the direct approach (transient analysis until all initial transients die off) and for the accelerated steady-state computation by means of extrapolation algorithms. Section 5 describes the implementation details of the selected extrapolation algorithm in SPICE OPUS. In Section 6, the implemented algorithm is used in the optimization of a test circuit. Section 7 concludes the paper.

## 2 Extrapolation algorithms

Vector sequence

$$\left\{\mathbf{x}_0^{(i)}\right\},\ \mathrm{i} = 0,1,2,3... \tag{1}$$

is generated from the initial vector $\mathbf{x}_0^{(0)}$ using the sequence generator $\mathbf{x}_0^{(i+1)} = \mathbf{F}(\mathbf{x}_0^{(i)})$, i = 0,1,2,3... If the sequence $\left\{\mathbf{x}_0^{(i)}\right\}$ is convergent, the limit of the sequence is denoted by $\mathbf{x}$.

An extrapolation algorithm $\mathbf{E}$ generates a new vector sequence $\left\{\mathbf{x}_{k+1}^{(0)}\right\}$, k = 0,1,2,3... with the following two steps

$$\mathbf{x}_{k+1}^{(0)} = \mathbf{E}(\mathbf{x}_k^{(0)}, \mathbf{x}_k^{(1)}, \mathbf{x}_k^{(2)} ... \mathbf{x}_k^{(n_k)}),\ \mathrm{k} = 0,1,2,3... \tag{2}$$

and

$$\mathbf{x}_k^{(i)} = \mathbf{F}(\mathbf{x}_k^{(i-1)}),\ \mathrm{i} = 1,2,3... \text{ for each } \mathrm{k} = 0,1,2,3... \tag{3}$$

The extrapolation algorithm generates the first term $\mathbf{x}_{k+1}^{(0)}$ of a new sequence $\left\{\mathbf{x}_{k+1}^{(i)}\right\}, i = 0,1,2...$ from the $n_k + 1$ terms of sequence $\left\{\mathbf{x}_k^{(i)}\right\}, i = 0,1,2...n_k$.

For each $k$, $n_k + 1 \le d$, $d = \dim(\mathbf{x}_k^{(0)})$ has to be satisfied. If $n_k + 1 > d$ the extrapolation algorithm is overdetermined.

The sequence $\left\{\mathbf{x}_{k+1}^{(0)}\right\}, k = 0,1,2,3...$ generated by (2) and (3) converges faster than sequence (1) to the same limit $\mathbf{x}$.

In the following subsections four extrapolation algorithms are described: epsilon algorithm, rho algorithm, theta algorithm and topological epsilon algorithm. The algorithms differ only in the definition of $\mathbf{E}$.

### 2.1 Epsilon algorithm

For each k in (2) a two-dimension array depicted in Fig. 1 is formed by

$$\boldsymbol{\varepsilon}_{-1}^{(i)} = \mathbf{0},\ \mathrm{i} = 1,2,3... \mathrm{n}_k \tag{4a}$$

$$\boldsymbol{\varepsilon}_0^{i} = \mathbf{x}_k^{(i)},\ \mathrm{i} = 0,1,2... \mathrm{n}_k \tag{4b}$$

$$\boldsymbol{\varepsilon}_{j+1}^{(i)} = \boldsymbol{\varepsilon}_{j-1}^{(i+1)} + (\boldsymbol{\varepsilon}_j^{(i-1)} - \boldsymbol{\varepsilon}_j^{(i)})^{-1},\ \mathrm{i} = 0,1,2... n_k,$$
$$\mathrm{j} = 0,1,2... n_k - 1 \text{ where } \mathrm{i} + \mathrm{j} + 1 \le n_k \tag{4c}$$

The procedure described by (4), is the so-called epsilon algorithm /1/. The inverse of the vector in (4c) is computed as

$$\mathbf{x}^{-1} = \frac{\mathbf{x}}{\|\mathbf{x}\|_2^2}. \tag{5}$$

If $n_k$ is an even number, $\boldsymbol{\varepsilon}_{n_k}^{(0)}$ is the result of the epsilon algorithm, so the extrapolation function (2) is defined as

$$\mathbf{E}(\mathbf{x}_k^{(0)}, \mathbf{x}_k^{(1)}, \mathbf{x}_k^{(2)} ... \mathbf{x}_k^{(n_k)}) = \boldsymbol{\varepsilon}_{n_k}^{(0)}. \tag{6}$$

### 2.2 Rho algorithm

The rho algorithm /1/ is similar to the epsilon algorithm. For each $k$ in (2) $n_k$ has to be even. The result is $\boldsymbol{\rho}_{n_k}^{(0)}$ obtained from

$$\begin{array}{ccccc}
 & & \boldsymbol{\varepsilon}_0^{(0)} & & \\
 & \boldsymbol{\varepsilon}_{-1}^{(1)} & & \boldsymbol{\varepsilon}_1^{(0)} & \\
 & & \boldsymbol{\varepsilon}_0^{(1)} & & \ddots \\
 & \boldsymbol{\varepsilon}_{-1}^{(2)} & & \boldsymbol{\varepsilon}_1^{(1)} & \\
 & & \boldsymbol{\varepsilon}_0^{(2)} & & \cdots \quad \boldsymbol{\varepsilon}_{n_k}^{(0)} \\
 & & & \boldsymbol{\varepsilon}_1^{(2)} & \\
\vdots & & \vdots & & \vdots \\
 & & \boldsymbol{\varepsilon}_0^{(n_k-1)} & & \ddots \\
 & \boldsymbol{\varepsilon}_{-1}^{(n_k)} & & \boldsymbol{\varepsilon}_1^{(n_k-1)} & \\
 & & \boldsymbol{\varepsilon}_0^{(n_k)} & &
\end{array}$$

*Figure 1: Two-dimension array for the epsilon algorithm*

$$\boldsymbol{\rho}_{-1}^{(i)} = \mathbf{0},\ \mathrm{i} = 1,2,3... \mathrm{n}_k \tag{7a}$$

$$\boldsymbol{\rho}_0^{i} = \mathbf{x}_k^{(i)},\ \mathrm{i} = 0,1,2... \mathrm{n}_k \tag{7b}$$

$$\boldsymbol{\rho}_{j+1}^{(i)} = \boldsymbol{\rho}_{j-1}^{(i+1)} + (j+1)\left[\boldsymbol{\rho}_j^{(i-1)} - \boldsymbol{\rho}_j^{(i)}\right]^{-1},\ \mathrm{i} = 0,1,2...$$
$$\mathrm{n}_k,\ \mathrm{j} = 0,1,2... n_k - 1 \text{ where } \mathrm{i} + \mathrm{j} + 1 \le n_k \tag{7c}$$

The inverse of the vector in (7c) is calculated in the same manner as in (5).

### 2.3 Theta algorithm

Extrapolation by theta algorithm /1/ (for an even $n_k$) is computed using the following equations

$$\vartheta_{-1}^{(i)} = \mathbf{0},\ \mathrm{i} = 1,2,3... n_k \tag{8a}$$

$$\vartheta_0^{i} = \mathbf{x}_k^{(i)},\ \mathrm{i} = 0,1,2... n_k \tag{8b}$$

$$\vartheta_{2j+1}^{(i)} = \vartheta_{2j-1}^{(i+1)} + \left[\Delta\vartheta_{2j}^{(i)}\right]^{-1},\ \mathrm{i} = 0,1,2... n_k,$$
$$j = 0,1,2... \frac{n_k}{2} - 1 \text{ where } \mathrm{i} + 2\mathrm{j} + 1 \le n_k, \tag{8c}$$

$$\vartheta_{2j+2}^{(i)} = \vartheta_{2j}^{(i+1)} + \left(\left[\Delta\vartheta_{2j}^{(i+1)}\right], \left[\Delta\vartheta_{2j+1}^{(i+1)}\right]\right) \cdot \left(\Delta^2\vartheta_{2j+1}^{(i+1)}\right)^{-1}, \tag{8d}$$

$$\mathrm{i} = 0,1,2... n_k,\ j = 0,1,2... \frac{n_k}{2} - 1 \text{ where } \mathrm{i} + 2\mathrm{j} + 2 \le n_k,$$

The abbreviations in (8c) and (8d) are

$$\Delta\vartheta_j^{(i)} = \vartheta_j^{(i+1)} - \vartheta_j^{(i)} \tag{8e}$$

$$\Delta^2\vartheta_j^{(i)} = \Delta\vartheta_j^{(i+1)} - \Delta\vartheta_j^{(i)} \tag{8f}$$

and the inverses in (8c) and (8d) are calculated by (5).

For each k and even $n_k$ the theta algorithm extrapolation function **E** is defined as

$$\mathbf{E}(\mathbf{x}_k^{(0)}, \mathbf{x}_k^{(1)}, \mathbf{x}_k^{(2)} \ldots \mathbf{x}_k^{(n_k)}) = \vartheta_{n_k}^{(0)} \quad (9)$$

## 2.4 Topological epsilon algorithm

If the inverse of a vector **x** is defined as

$$\mathbf{x}^{-1} = \frac{\mathbf{y}}{(\mathbf{y}, \mathbf{x})}, \quad (10)$$

the inverse is the so-called inverse of vector **x** with respect to **y**.

In the topological epsilon algorithm the inverses in odd and even terms are computed with respect to different vectors.

For each interation $k$ of the extrapolation algorithm, the topological epsilon algorithm /1/ is defined by

$$\boldsymbol{\varepsilon}_{-1}^{(i)} = \mathbf{0}\ ,\ \mathrm{i} = 1,2,3 \ldots n_k \quad (11a)$$

$$\boldsymbol{\varepsilon}_{0}^{i} = \mathbf{x}_k^{(i)},\ \mathrm{i} = 0,1,2 \ldots n_k \quad (11b)$$

$$\boldsymbol{\varepsilon}_{2j+1}^{(i)} = \boldsymbol{\varepsilon}_{2j-1}^{(i+1)} + \frac{\mathbf{y}}{(\mathbf{y}, \Delta\boldsymbol{\varepsilon}_{2j}^{(i)})},\ \mathrm{i} = 0,1,2 \ldots$$

$$n_k,\ j = 0,1,2 \ldots \frac{n_k}{2} - 1 \text{ where } \mathrm{i} + 2\mathrm{j} + 1 \le n_k \quad (11c)$$

$$\boldsymbol{\varepsilon}_{2j+2}^{(i)} = \boldsymbol{\varepsilon}_{2j}^{(i+1)} + \frac{\Delta\boldsymbol{\varepsilon}_{2j}^{(i)}}{(\Delta\boldsymbol{\varepsilon}_{2j}^{(i)}, \Delta\boldsymbol{\varepsilon}_{2j+1}^{(i)})},\ \mathrm{i} = 0,1,2 \ldots$$

$$n_k\ ,\ j = 0,1,2 \ldots \frac{n_k}{2} - 1 \text{ where } \mathrm{i} + 2\mathrm{j} + 1 \le n_k, \quad (11d)$$

Inverses in the odd terms (11c) are computed with respect to an arbitrary y such that all terms $\boldsymbol{\varepsilon}_{2j+1}^{(i)}$ exist. Inverses in (11d) are computed with respect to $\Delta\boldsymbol{\varepsilon}_{2j}^{(i)}$.

The result of the topological epsilon algorithm is $\boldsymbol{\varepsilon}_{n_k}^{(0)}$, so the extrapolation function **E** is defined as

$$\mathbf{E}(\mathbf{x}_k^{(0)}, \mathbf{x}_k^{(1)}, \mathbf{x}_k^{(2)} \ldots \mathbf{x}_k^{(n_k)}) = \boldsymbol{\varepsilon}_{n_k}^{(0)}.$$

# 3 Simulation of electrical circuits

Nonlinear dynamical electrical circuits can be described by a system of ordinary differential equations

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}(t), \mathrm{t}) \quad (12)$$

where $x(t)$ represents the node voltages and the branch currents of the circuit. In transient analysis, (12) is solved starting from the initial value $x(0)$. The resulting waveforms are represented by vector functions

$$x(t),\ 0 \le t \le t_n. \quad (13)$$

For further reference, $x(t)$ is a column vector with $d$ components:

$$\mathbf{x}(t) = [{}_1x(t),\ {}_2x(t),\ \cdots\ {}_dx(t)]^{\mathrm{T}}. \quad (14)$$

(12) is numerically integrated and solved using the Newton-Raphson iterative metod for times $t = 0 \le t_1 \le t_2 \le \cdots \le t_n$.

Time step $\Delta t_i = t_{i+1} - t_i$ should be small enough to avoid numerical errors. Decreasing the time step increases the computation time as more points have to be evaluated.

## 3.1 SPICE OPUS circuit simulator and optimizer

The simulation of electrical circuits can be done with the SPICE OPUS circuit simulator and optimizer /6/. Circuit simulation is a part of every circuit optimization /7/ where parameters of the circuit are sought, subject to design requirements. During optimization, a circuit is simulated many times, so individual simulations should be as short as possible.

When computing the steady-state response of a circuit, a problem occurs when the period of the steady-state response is much smaller than the largest time constant of the circuit. Such circuits must be simulated for hundreds or even thousands of periods before they reach steady state. To obtain sufficient accuracy, a hundred or more time points must be evaluated per period of the response. Therefore, several million time points have to be evaluated before steady state is reached.

Using the extrapolation algorithms described in Section 2 computing steady-state response of such electrical circuits can be significantly accelerated.

## 3.2 Application of extrapolation algorithms in circuit simulation

To compute the steady-state response of a circuit by means of an extrapolation algorithms, the circuit is simulated (solving (12)) starting from the initial value $x(0) = 0$ for times $0 \le t \le t_n + t_{del}$. Terms of sequence (1) are extracted from the resulting waveforms $x(t)$:

$$\mathbf{x}_0^{(i)} = \mathbf{x}(t_{del} + iT)\ ,\ i = 0,1,2 \ldots n\ ,\ n = \lfloor \mathrm{t_n}/\mathrm{T} \rfloor \quad (15)$$

where T is the period of the steady-state response of the circuit and $t_{del}$ is the time where the first term $\mathbf{x}_0^{(0)}$ is sampled. Then the extrapolation algorithm is used on sequence $\{\mathbf{x}_0^{(i)}\}$ to generate the extrapolated vector $\mathbf{x}_1^{(0)}$ which represents the initial value $x(0)$ for a new simulation.

This iterative process is repeated $k$-times until $\|\mathbf{x}_k^{(n)} - \mathbf{x}_k^{(0)}\|$ in the last ($k$-th) iteration is small enough to assume that the circuit is in steady state.

We can assume that steady state has been reached when the relative and the absolute tolerance criteria

$$\left| {}_lx_k^{(n)} - {}_lx_k^{(0)} \right| \le \delta_a + \max\left\{ \left| {}_lx_k^{(n)} \right|, \left| {}_lx_k^{(0)} \right| \right\} \delta_r \quad (16)$$

for all $l$ = 1,2, ... $d$ are satisfied.

In practice, it is sufficient if $\delta_a$ and $\delta_r$ are less than $10^{-5}$ and $10^{-4}$, respectively and greater than the precision of the data representation (i.e. the relative and absolute precision of *double* is $10^{-14}$ and $10^{-320}$, respectively).

A flow chart of the extrapolation algorithm is depicted in Fig. 2.

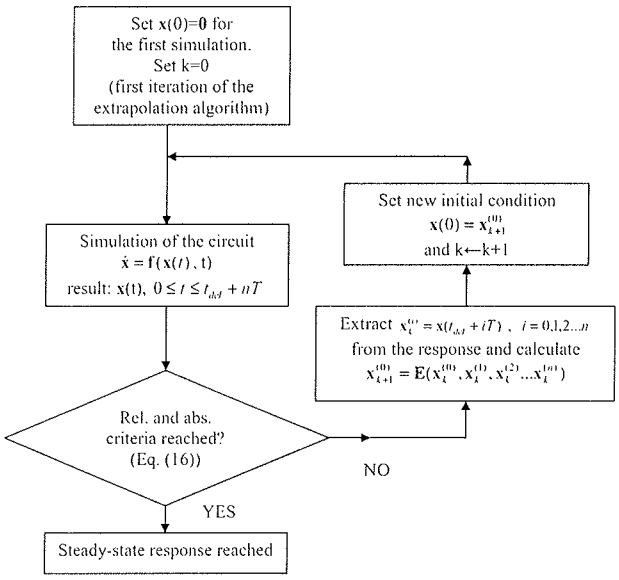


*Figure 2: Flow chart of the extrapolation algorithm for determing steady-state response of a circuit.*

### 3.3 Accelerating the computation of steady state of an electrical circuit

The steady-state response is important in the analysis of power conversion circuits, in the evaluation of nonlinear properties of narrow-band circuits, etc. For such circuits the evaluation of long transients can be accelerated using extrapolation algorithms.

In the following section the above mentioned extrapolation algorithms are tested with the Greinacher rectifier, narrow-band filter and switching rectifier test circuits.

## 4 Comparison

The test circuits were simulated using the direct approach (running a transient analysis until all initial transients died off). It took several thousand periods for the simulator to reach the steady state.

The steady-state responses of the circuits were also computed using the transient analysis accelerated by an extrapolation algorithm (epsilon algorithm, rho algorithm, theta algorithm and topological epsilon algorithm). The total number of periods required for computing the steady state has been greatly reduced.

In the following subsections the test circuits and the detailed results of the steady-state simulation are presented.

### 4.1 Test circuits

The two-stage Greinacher rectifier test circuit is depicted in Fig. 3.

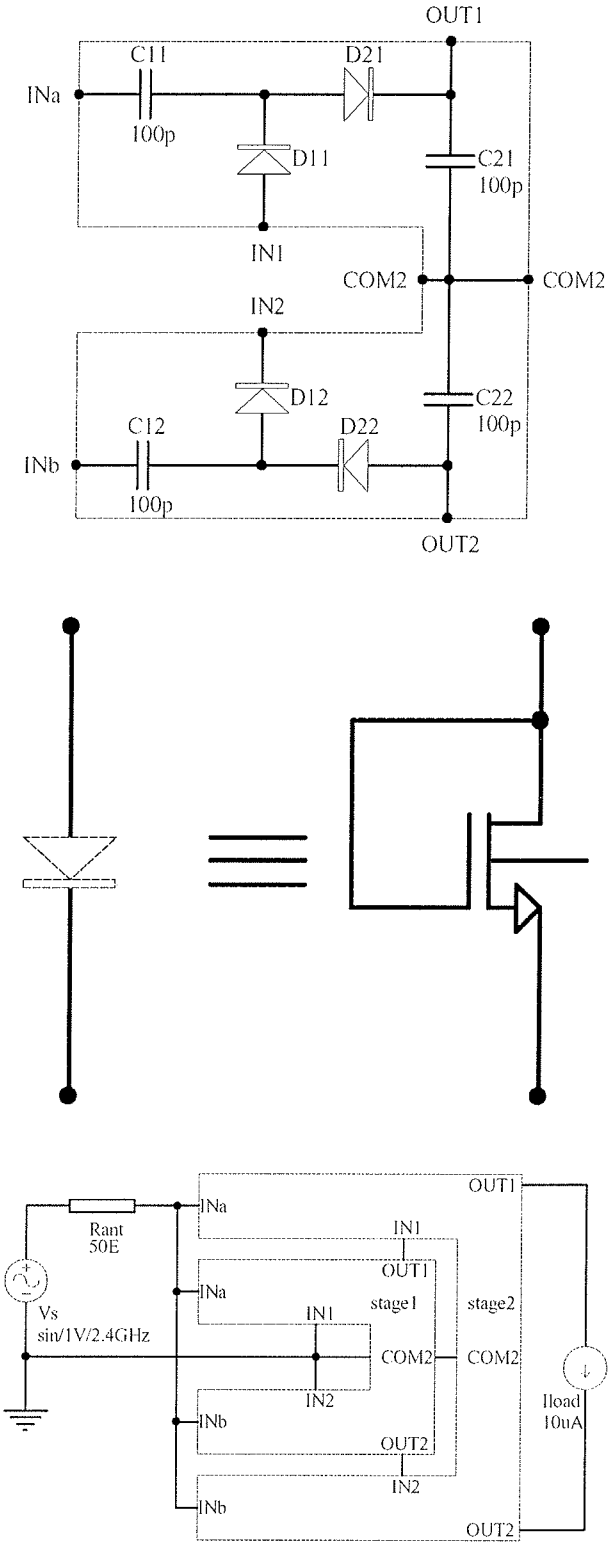


*Figure 3: (a) Single stage of a Greinacher rectifier. (b) Implementation of a diode with an n-channel MOS. (c) Test circuit: two-stage Greinacher rectifier.*

Fig. 3a represents one stage of the Greinacher rectifier. Diodes in Fig. 3a are implemented as n-channel MOS transistors in 0.18μm TSMC technology (Fig. 3b). Two stages are connected together as depicted in Fig. 3c. At the in-

put of the circuit a sinusoidal voltage source $V_s$ with amplitude 1 V and frequency 2.4 GHz is connected in series with resistor $R_{ant} = 50\ \Omega$. The output of the circuit is loaded with $I_{load} = 10\mu A$.

In Fig. 4 a narrow-band filter is depicted. At the input of the circuit (node 1) a sinusoidal voltage source $V_{in}$ with amplitude 1 V and frequency 32767.41 Hz is connected. The output of the circuit is at node 4. The quartz crystal $X_1$ is modelled with resistor $R_s$, inductor $L_s$ and capacitors $C_s$ and $C_p$.

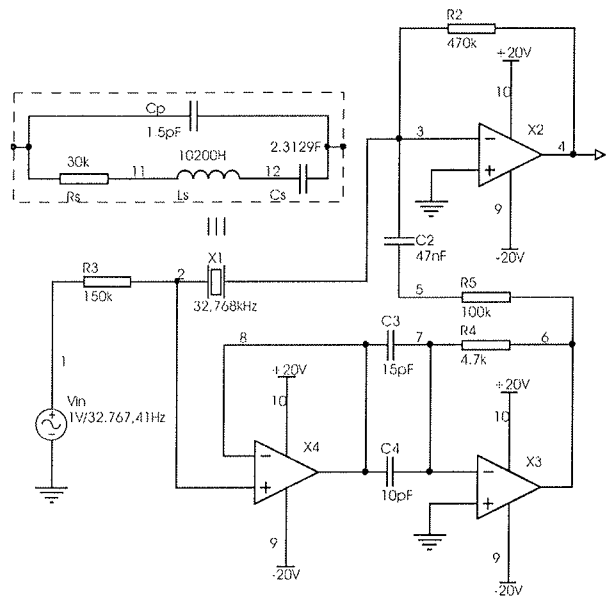


*Figure 4: Narrow-band filter.*

The circuit in Fig. 5 is a switching power supply. The power source (DC voltage 20 V) is connected to node 1. DC voltage of the $V_{pulse}$ is 10 V, amplitude is 20 V, rise and fall times are 10 ns, and the duty-cycle is 9%. At the output (node 4) $r_{load} = 1k\Omega$ is connected.

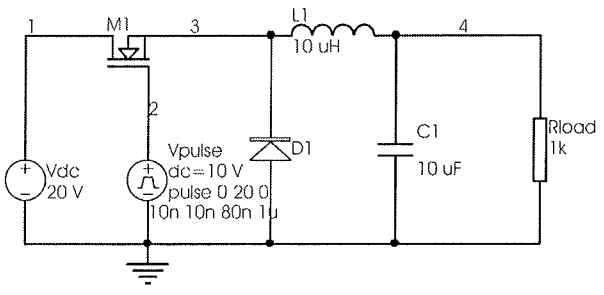


*Figure 5: Switching power supply.*

## 4.2 Results

The steady-state response of the Greinacher rectifier is shown in Fig. 6.

The circuit reaches the steady state in 100ms or in 240000 periods of the signal $V_s$. The steady state of the circuit was also computed with extrapolation algorithm. Parameter $n_k$

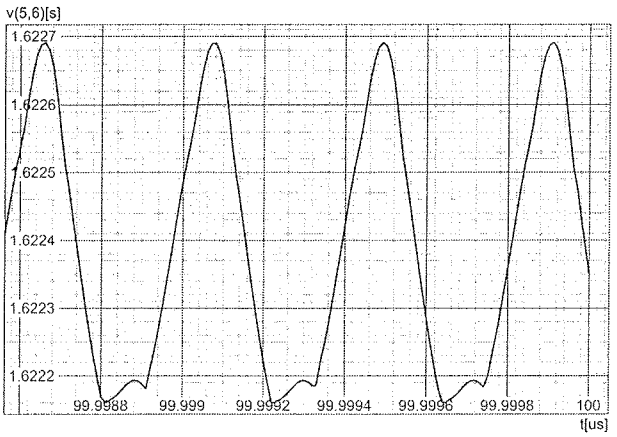


*Figure 6: The steady-state response of the two-stage Greinacher rectifer (loaded with $I_{load}$= 10μA).*

(equations (4), (7), (8) and (11)) was set to 6. The extrapolation algorithm was stopped when the relative and the absolute criteria (16) were satisfied ($\delta_a = 10^{-6}$ and ($\delta_r = 10^{-6}$). The number of iterations of the extrapolation algorithm (k) and the number of periods the circuit was simulated before it reached the steady state ( $\sum_k (n_k + t_{del}/T)$ ) are listed in Table 1.

*Table 1: The number of iterations of the extrapolation algorithm and the number of simulated periods in the computation of the steady-state response.*

| | Greinacher rectifier | | Narrow-band filter | | Switching power supply | |
|---|---|---|---|---|---|---|
| | Iterations | Periods | Iterations | Periods | Iterations | Periods |
| **Epsilon algorithm** | 52 | 330 | 3 | 54 | 4 | 24 |
| **Rho algorithm** | 37 | 222 | 3 | 87 | 5 | 30 |
| **Theta algorithm** | 99 | 594 | 9 | 144 | 12 | 72 |
| **Topological epsilon algorithm** | 274 | 1644 | 3 | 54 | 4 | 24 |
| **Direct transient analysis** | / | 240000 | / | 65535 | / | 100000 |

Using an extrapolation algorithm, the steady-state response of the test circuit was computed more than 140 times faster than with the direct approach (transient analysis until all initial transients die off).

The narrow-band filter took 2 s (65535 periods) of the signal $V_{in}$ before it reached steady state (Fig. 7). Computing the steady state with the epsilon, rho, theta and topological epsilon algorithm took 54, 87, 144 and 54 periods, respectively (Table 1) with $\delta_a = 5.10^{-6}$ and $\delta_r = 5.10^{-6}$.

The steady-state response of the switching power supply is depicted in Fig. 8. Steady state is reached in 100 ms or

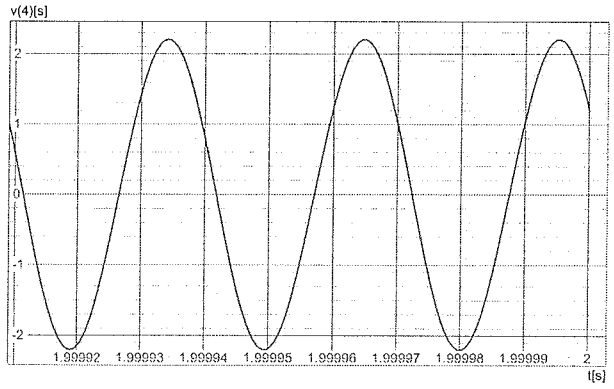


*Figure 7: The steady-state response of the narrow-band filter.*

in 100000 periods of the signal $V_{pulse}$. With the epsilon, rho, theta and topological epsilon algorithm computing steady state took 24, 30, 72 and 24 periods, respectively (Table 1) with $\delta_a = 10^{-6}$ and $\delta_r = 10^{-7}$.

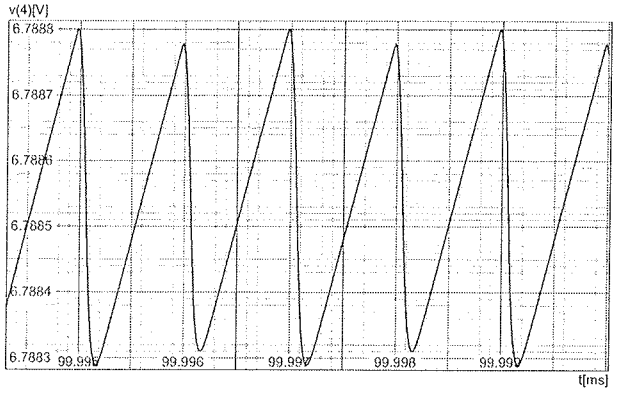


*Figure 8: The steady-state response of the switching power supply.*

# 5 Implementation of an extrapolation algorithm in SPICE OPUS

## 5.1 Choice of the extrapolation algorithm

The results listed in Table 1 show that for the selected test circuits the best of the extrapolation algorithms is the epsilon algorithm. Therefore we chose it for the implementation in SPICE OPUS.

The epsilon algorithm was also chosen due to it's simplicity and good results obtained with other circuits the extrapolation algorithm was tested on /8,9/.

## 5.2 SSSE analysis

The new *SSSE* (Steady-State Shooting with Extrapolation) analysis was implemented in the SPICE OPUS circuit simulator /6/. The syntax of the *ssse* analysis is as follows:

ssse <freq> [step [skip [periods]]] [history]

< > ... required parameter

[ ] ... optional parameter

*freq* represents the fundamental frequency (f) of the steady-state response, *step* represents the basis for the variable time step (same as the first argument for the transient analysis, default value: 10/ *freq*), *skip* represents the time skipped ($t_{del}$ in (15)) before the response is sampled (default value: 0) and *periods* gives the number of periods ($n_k$) that are taken into account for sampling (default value: 2).

The iteration limit of the epsilon extrapolation algorithm is given by the *itl2* option. Convergence (see (16)) is defined with the absolute and the relative tolerances given by products of *sssetol*vntol*, *sssetol*abstol*, and *sssetol*reltol* options. Steady state is reached when the difference (16) is within tolerances.

By default only the last transient run results (steady-state response) are saved in a plot as final results of the ssse analysis. If the *history* flag is set then all transient iterations performed during the steady-state analysis are saved in plots.

The steady-state response of the Greinacher rectifier in Fig. 6 was obtained with the following SPICE OPUS commands.

```
.options itl2=1000
.options sssetol=1e-2
.options abstol=1e-4
.options reltol=1e-4
.control
set xmumult=1
ssse 2.4g 2p 0 6 history
.endc
```

The *xmumult* option is set to 1 to turn off numerical oscillation detection, which can interfere with the extrapolation algorithm.

# 6 Optimization of electrical circuits

Circuit simulation is a part of every circuit optimization /7/ where parameters of the circuit are sought subject to design requirements. During optimization, a circuit is simulated many times, so individual simulations should be as short as possible.

If the circuit is being optimized and the steady-state response is computed in every iteration of the optimization, fast computation of the steady-state response is a prerequisite for realistic optimization times.

## 6.1 Optimization of the Greinacher rectifier test circuit

To demonstrate the application of the *ssse* command, an optimization proccess was run on the test circuit in Fig. 3. Table 2 lists the optimization parameters.

*Table 2: The optimization parameters.*

| | |
|---|---|
| **Parameter 0** | *Width of transistors modelling diodes D11 and D12 (Stage 1)* |
| **Parameter 1** | *Width of transistors modelling diodes D21 and D22 (Stage 1)* |
| **Parameter 2** | *Width of transistors modelling diodes D11 and D12 (Stage 2)* |
| **Parameter 3** | *Width of transistors modelling diodes D21 and D22 (Stage 2)* |
| **Parameter 4** | *Capacitance of all capacitors of Stage 1 and Stage 2* |

The optimization was started at *Initial value* of the parameters in Table 3. The explicit constrains are defined by the columns *Minimum value* and *Maximum value*. The parameters were allowed to change by the value of the *Increment* column in Table 3.

*Table 3: Initial, minimum, maximum values, and increment of optimization parameters.*

| | Initial value | Minimum value | Maximum value | Increment |
|---|---|---|---|---|
| **Parameter 0** | *10 μm* | *0.22 μm* | *100 μm* | *0.18 μm* |
| **Parameter 1** | *10 μm* | *0.22 μm* | *100 μm* | *0.18 μm* |
| **Parameter 2** | *8 μm* | *0.22 μm* | *100 μm* | *0.18 μm* |
| **Parameter 3** | *8 μm* | *0.22 μm* | *100 μm* | *0.18 μm* |
| **Parameter 4** | *100 pF* | *10 pF* | *300 pF* | *10 pF* |

The circuit behavior was described with the cost function which consists of penalty functions of measurement values multiplied by weights /10/.

Table 4 shows the measurements, measurements goals, norms and weights.

If a *measurement value* violates a *measurement goal* by *norm*, the contribution to the cost function equals *measurement weight*.

*Table 4: Measurements performed on the test circuit.*

| | | goal | weight | norm |
|---|---|---|---|---|
| **Measurement 1** | $V_{DC\_load}$ | *> 2 V* | *3* | *1 V* |
| **Measurement 2** | $V_{ripple\_load}$ | *< 250 μV* | *1* | *100 μV* |
| **Measurement 3** | $V_{DC\_noload}$ | *> 3 V* | *1* | *1 V* |
| **Measurement 4** | $V_{ripple\_noload}$ | *< 140 μV* | *1* | *100 μV* |

Measurements are defined by

$$V_{DC\_load} = \left\{ \frac{1}{T} \int_{(n_k-1)T}^{n_k T} (v_{OUT2}(t) - v_{OUT1}(t)) dt \right\} \Bigg|_{I_{load}=10\mu A} \quad (17a)$$

$$V_{ripple\_load} = \left\{ \max_{t\in[(n_k-1)T, n_k T]} (v_{OUT2}(t) - v_{OUT1}(t)) - \min_{t\in[(n_k-1)T, n_k T]} (v_{OUT2}(t) - v_{OUT1}(t)) \right\} \Bigg|_{I_{load}=10\mu A} \quad (17b)$$

$$V_{DC\_noload} = \left\{ \frac{1}{T} \int_{(n_k-1)T}^{n_k T} (v_{OUT2}(t) - v_{OUT1}(t)) dt \right\} \Bigg|_{I_{load}=0} \quad (17c)$$

$$V_{ripple\_noload} = \left\{ \max_{t\in[(n_k-1)T, n_k T]} (v_{OUT2}(t) - v_{OUT1}(t)) - \min_{t\in[(n_k-1)T, n_k T]} (v_{OUT2}(t) - v_{OUT1}(t)) \right\} \Bigg|_{I_{load}=0} . \quad (17d)$$

Measurements 1 and 2 were made with $I_{load} = 10\mu A$ (Fig. 3c). Measurements 3 and 4 were made with no load ($I_{load} = 0$).

The optimization took 2964 iterations. Every iteration of the optimization included two SSSE analyses.

On an AMD Athlon XP 2500+ (1.83 GHz clock) computer with 512 MB of RAM, the optimization took 3 hours and 10 minutes. Optimum parameters are shown in Table 5 and the final measurement values in Table 6.

*Table 5: Optimum parameter values after the optimization.*

| | Value |
|---|---|
| **Parameter 0** | *16.60 μm* |
| **Parameter 1** | *21.10 μm* |
| **Parameter 2** | *27.76 μm* |
| **Parameter 3** | *26.68 μm* |
| **Parameter 4** | *300 pF* |

For measurements 2 and 4 the goals were achieved, while Measurements 1 and 3 violated the goals. The final cost function value was 0.6792.

Table 6 also lists the measurement values before optimization (at initial values of the parameters in Table 3). Average improvement of the measurements is 16 %.

In Sections 4.2 and 5.1 we have demonstrated that the acceleration ratio for the Greinacher rectifier test circuit (in case of the epsilon algorithm) is 727 (240000/330 ≅ 727, see Table 1). If ordinary transient analysis was used, the optimization would take more than 95 days. This clearly

*Table 6: Measurement values before and after the optimization.*

| | Before optimization | After optimization | Improvement |
|---|---|---|---|
| **Measurement 1** | *1.624 V* | *1.794 V* | *10.5 %* |
| **Measurement 2** | *326.0 μV* | *249.9 μV* | *23.3 %* |
| **Measurement 3** | *2.670 V* | *2.911 V* | *9.0 %* |
| **Measurement 4** | *176.5 μV* | *138.9 μV* | *21.3 %* |

demonstrates that if the steady-state response of a circuit has to be computed in an optimization loop, an efficient extrapolation algorithm is necessary.

## 7 Conclusions

Four extrapolation algorithms (epsilon, rho, theta and topological epsilon algorithm) were described in this paper. Using these algorithms the steady-state computation has been accelerated several hundred times.

The extrapolation algorithms were tested on three test circuits (Greinacher rectifier, narrow-band filter and switching power supply). The epsilon algorithm was shown to be the most appropriate for the implementation in the SPICE OPUS circuit simulator. The steady-state responses of the test circuits were computed several hundred times faster than with the direct approach (transient analysis until all initial transients die off). A new SPICE OPUS analysis utilizing the epsilon algorithm was implemented.

The Greinacher rectifier test circuit was optimized using the SSSE analysis. The purpose of the optimization was to show that the optimization of the steady-state response can be accelerated significantly by using extrapolation methods. Optimization with the SSSE analysis (accelerated transient analysis) lasted 3 hours and 10 minutes. It has been estimated that the optimization with the direct approach (direct transient analysis) would take more than 95 days.

## 8 Acknowledgment

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*univ. dipl. ing. el. Borut Wagner*
*University of Ljubljana*
*Faculty of Electrical Engineering*
*Tržaška cesta 25, SI-1000 Ljubljana, Slovenia*
*E-mail: borut.wagner@fe.uni-lj.si*
*Tel: +386 1 4768724, Fax: +386 1 4264630*

*doc. dr. Árpád Bűrmen*
*University of Ljubljana*
*Faculty of Electrical Engineering*
*Tržaška cesta 25, SI-1000 Ljubljana, Slovenia*
*E-mail: arpadb@fides.fe.uni-lj.si*
*Tel: +386 1 4768322, Fax: +386 1 4264630*

*doc. dr. Janez Puhan*
*University of Ljubljana*
*Faculty of Electrical Engineering*
*Tržaška cesta 25, SI-1000 Ljubljana, Slovenia*
*E-mail: janez.puhan@fe.uni-lj.si*
*Tel: +386 1 4768322, Fax: +386 1 4264630*

*prof. dr. Sašo Tomažič*
*University of Ljubljana*
*Faculty of Electrical Engineering*
*Tržaška cesta 25, SI-1000 Ljubljana, Slovenia*
*E-mail: saso.tomazic@fe.uni-lj.si*
*Tel: +386 1 4768432, Fax: +386 1 4264630*

*prof. dr. Tadej Tuma*
*University of Ljubljana*
*Faculty of Electrical Engineering*
*Tržaška cesta 25, SI-1000 Ljubljana, Slovenia*
*E-mail: tadej.tuma@fe.uni-lj.si*
*Tel: +386 1 4768329, Fax: +386 1 4264630*

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# NEW INTERPOLATION TECHNIQUE FOR HIGHLY LINEAR CMOS ADC

Shazia Seemi, Mohd Shahiman Sulaiman, Arshad Suhail Farooqui, M.B.I. Reaz

Faculty of Engineering, Multimedia University, Cyberjaya, Malaysia

**Key words:** CMOS ADC, flash, interpolation, high-speed ADC, data converter

**Abstract:** A new interpolation technique for high speed ADCs is described. Simple summing differential amplifiers operating in continuous time are used as the interpolator. Incorporated in a 1.3Gsample/s 6-bit CMOS Flash with Interpolation Analog-to-Digital Converter and prototyped on CMOS 0.18-um process, measured results indicated a significant improvement in converter linearity compared to other interpolation techniques.

# Nova interpolacijska tehnika za zelo linearne CMOS ADC pretvornike

**Kjučne besede:** CMOS ADC, flash, interpolacija, hitri ADC, podatkovni pretvornik

**Izvleček:** V prispevku opišemo novo interpolacijsko tehniko za zelo hitre ADC pretvornike. Kot interpolator uporabimo enostavne diferencijalne operacijske ojačevalnike v realnem času. Vgrajen v 6-bitni CMOS Flash z 1.3Gvzorcev/s in skupaj z ADC pretvornikom izdelan v 0.18um CMOS tehnologiji; meritve pretvornika kažejo bistvene izboljšave v njegovi linearnosti v primerjavi z drugimi interpolacisjkimi tehnikami.

## 1 Introduction

High speed requirements for ADCs (Analog to Digital Converters) in the fields of data storage and digital communication has led to finding new ways to accomplish high speed without sacrifying dynamic and static performance /1/-/2/. Although Flash Architecture is a good choice for high speed ADCs, it has a large number of input amplifiers. This results in a large input capacitance and high power consumption /3/-/5/. An alternative approach is to use Interpolating architecture that has fewer amplifiers at the input stage /3/. Interpolation can be of two types, current mode or voltage mode. Current mode interpolation is based on the summation of currents reflected through current mirrors with different ratios. It is fast but power hungry and is not very precise due to non-idealities in current mirrors /6/-/7/. Voltage interpolation requires less number of amplifiers, hence, consumes less power. One of the major drawbacks of voltage interpolation is the skew related to the delay from amplifier output to each comparator, i.e. delay from amplifier output to each comparator may not be the same. This delay is primarily due to the series resistance and input capacitance of the comparator. It can be reduced by adding series resistance at the input of the comparator but there could be phase errors when a sinusoidal input is applied. The phase errors degrade comparator's dynamic performance /8/. The interpolation circuit presented in this paper solved the issues faced by voltage-mode interpolation by significantly reducing the delay mismatches and the phase errors and consuming power less than that of a current-mode interpolation circuit. When implemented in a data converter, the circuit demonstrates that the new active/voltage-mode interpolation circuit is capable of working at the frequency before this only achievable by current-mode interpolator and with better linearity performance, compared to the work by /6/,/9/,/11/ and /13/. This circuit would allow more active interpolator to be used in the future to achieve low power consumption and high linearity.

## 2. Interpolator Cell Architecture

Active interpolation circuit is performed by summing the output currents of two differential pairs into resistive loads.

Figure 1 depicts the circuit diagram of the basic interpolator cell. The two identical differential pairs (M1, M2, M5 and M3, M4, M6) share the same resistive loads $R_{L1}$ and $R_{L2}$. The small signal current through $R_{L1}$ is equal to the sum of currents flowing through M1 and M3, and the current through $R_{L2}$ is equal to the sum of currents flowing through M2 and M4. The differential output $(Voutp - Voutn)$ is proportional to the sum of differential input voltages

$$(Voutp - Voutn) \propto (Vinp1 - Vinn1) + (Vinp2 - Vinn2)$$

Hence, it is proportional to the average of the input voltages. From small-signal analysis, the interpolator output is given as

$$Voutp - Voutn = \frac{g_m r_o R_l [(Vinp1 - Vinn1) + (Vinp2 - Vinn2)]}{2R_l + r_o + sC_l R_l r_o} \quad (1)$$

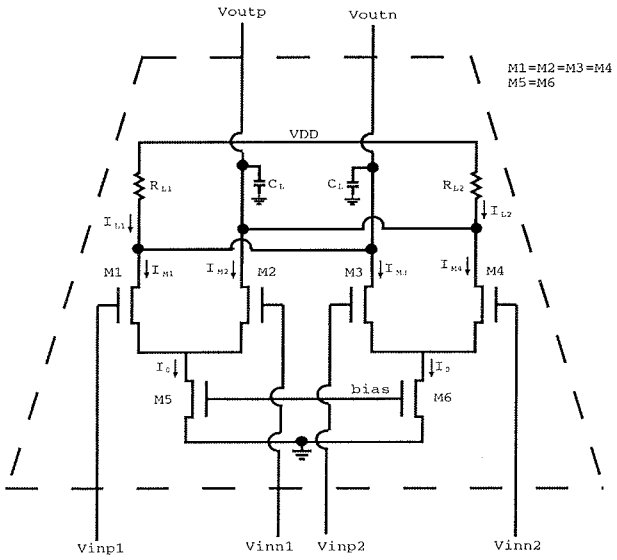


*Figure 1: Interpolator Cell*

The new interpolation technique is performed by arranging the interpolator cells as illustrated in Figure 2. The signals to be interpolated ($IN_{n-1}$, $IN_n$ and $IN_{n+1}$) are fed into the differential inputs of $IAMP_{n-2}$ through $IAMP_{n+2}$. Interpolated outputs are received as $OUT_{n-2}$ through $OUT_{n+2}$. The input pairs of $IAMP_{n-2}$, $IAMP_n$ and $IAMP_{n+2}$ are connected together. This is done in order to maintain the same common mode at all interpolator cell outputs and to equalize the path delays of interpolated and non-interpolated signals. Averaging resistors (Ravg) are used to reduce the effects of device mismatches, as demonstrated by /9/. Besides that, advanced circuit layout techniques such as gate-aligned and common-centroid are used to ensure device symmetry. The combination of active interpolation based on the new interpolator cell, resistive averaging and symmetrical layout techniques results in uniform path delays and fairly low nonlinearities, hence solving problems commonly faced by voltage interpolator.

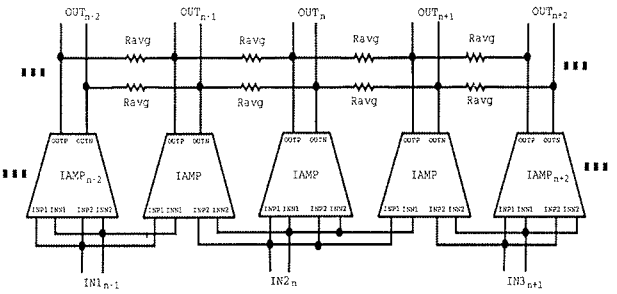


*Figure 2: Delay equalization using interpolator cell*

## 3. A 6-bit Interpolating ADC

The proposed interpolation scheme is verified by designing a 1.3Gsample/s 6-bit Interpolation with Flash ADC and prototyped on a CMOS 0.18-um CMOS process. Interpolation is performed by a two-stage 16-to-64 interpolator with resistive terminated averaging. Figure **3** depicts the top segment of the interpolator. Figure 5 shows the ADC block diagram. The averaging and termination resistor values are calculated based on the following formulas

$$R_{avg} = \frac{8}{7} R_L$$

$$R_{trm} = R_{avg} - R_L$$

where

$R_L$ is the load resistor of interpolator cell.

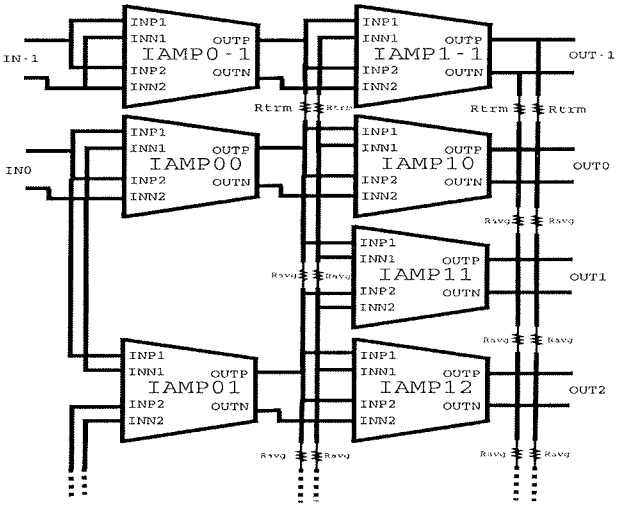


*Figure 3: 16-to-64 Interpolator*

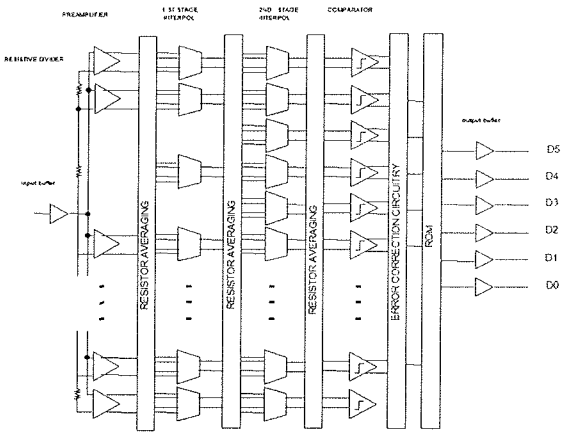


*Figure 5: ADC Block Diagram*

## 4. Results and Discussion

The whole ADC was prototyped on CMOS 0.18-um 6-metal 1-poly process, mounted on a 40-pin ceramic package.

The proposed interpolation technique achieves a phase difference of only 0.05° between the interpolated and non-interpolated outputs. This phase difference is significantly lower than 0.45° obtained using resistive interpolation /8/ and other voltage-mode interpolation techniques. The value of INL is ±0.35 LSB at 1.3GSps, which is lower than

other interpolation based designs /6/,/11/. Figure 6 shows a plot of the measured DNL, which varies from +0.15LSB to -0.15LSB. This is the lowest DNL achieved in a CMOS-based high speed ADC (/9/,/12/,/13/) and is certainly the best DNL figure for voltage-mode interpolator. Table 1 compares various types of interpolation with the new technique proposed in this paper. It can be seen that the new technique offers an enormous decrease in pertinent phase delay problem of voltage interpolation. It can also be seen from the table that, the new technique has a better static performance as compared to current interpolation technique.

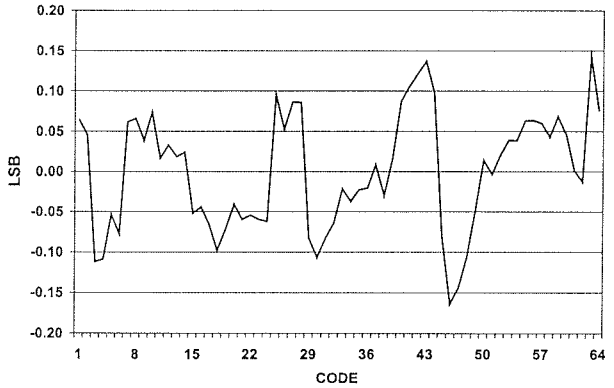


*Figure 6: Measured DNL for ADC based on the new Active Interpolation Technique*

*Table 1 : Comparisons with other Interpolating ADCs*

| | Voltage | Current | This work |
|---|---|---|---|
| **Phase** | >=0.45° | <=0.05° | <=0.05° |
| **Delay** | >±0.5 LSB | >=±0.4 LSB | ±0.15 LSB |
| **DNL** | >=±0.5 LSB | >=±1 LSB | ±0.35 LSB |
| **INL** | Low | High | Low |

The whole interpolator for the ADC has a bandwidth of 750 MHz, occupies an active area of 0.13mm$^2$ and consumes 122-mA current from a 1.8-V power supply. A parametric comparison between this design (ADC using Active Interpolation) and other works is summarized in Table 2.

*Table 2 : Performance Comparison of ADCs based on various interpolator circuit*

| | DNL (LSB) | INL (LSB) | Power (mW) | Process (µm) | Voltage Supply (V) |
|---|---|---|---|---|---|
| ADC1300 (This work) 6-bit, 1.3Gsample/s | 0.15 | 0.35 | 612 | 0.18 | 1.8 |
| 6-bit 1.3Gsamples/s (Uyttenhove, Steyaert, 2003) | 0.42 | 0.8 | 600 | 0.25 | 1.8 V(A) / 2.5 V(D) |
| 6-bit 1.6Gsamples/s (Scholtens, Vertregt, 2002) | Approx. 0.25 | 0.42 | 340 | 0.18 | 1.95(A) / 2.35(D) |
| 10-bit, 300Mhz (Kimura, Matsuzawa, 1993) | 0.4 | 1 | 400 | 1,bipolar | 5.2 |

## 5. Conclusion

The new interpolation technique offers extremely low phase delay between the interpolated and the non-interpolated signal, which improves its dynamic performance. At the same time, combination with resistive-averaging network when implemented in an ADC improves the static performance. The ADC's ability to achieve high sampling rate of 1.3Gsample/s while maintaining very low static and dynamic errors makes this interpolation technique suitable for implementation in high speed ADCs.

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*Shazia Seemi, Mohd Shahiman Sulaiman,*
*Arshad Suhail Farooqui, M.B.I. Reaz*
*Faculty of Engineering, Multimedia University,*
*63100 Cyberjaya, Malaysia*

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# A FRAMEWORK FOR HIGH-LEVEL SYSTEM DESIGN EXPLORATION

Jože Dedič, Matjaž Finc, Andrej Trost

University of Ljubljana, Faculty of Electrical Engineering, Laboratory for Integrated Circuits Design, Ljubljana, Slovenia

**Key words:** abstraction, design-space exploration, modeling, high-level design, TLM.

**Abstract:** The complexity of modern embedded systems requires a revised and systematic approach to efficient and concurrent management of hardware (HW) and software (SW) parts in a codesign process. In order to optimally meet the ever increasing design requirements and at the same time leverage design productivity, higher-level aspects need to be addressed before worrying about the HW/SW boundary. This way high-level design decisions evaluation is enabled and premature ad-hoc decisions are avoided. This paper deals with high-level aspects of system-level modeling and provides modeling extension, from which contemporary related methodologies could greatly benefit. High-level aspects, their influence on the entire design flow and systematic integration into the codesign environment are presented. A design flow and realization of supporting library are detailed, both offering support for high-level exploration. Applicability of the proposed high-level codesign concepts is illustrated with a case study.

# Programsko ogrodje za visokonivojsko raziskovanje na sistemskem nivoju

**Ključne besede:** abstrakcija, modeliranje, raziskovanje načrtovalskega prostora, TLM, visokonivojsko načrtovanje.

**Izvleček:** Visoka kompleksnost modernih vgrajenih sistemov zahteva posodobljen in sistematičen način pristopa k sočasnemu načrtovanju strojne in programske opreme (SNSPO). Nenehno povečevanje načrtovalskih zahtev je ob hkratni zahtevi po povečevanju načrtovalske produktivnosti mogoče samo v primeru, da se pred obravnavo meje med strojno in programsko opremo osredotočimo na visokonivojske lastnosti sistema. To nudi osnovo za ovrednotenje visokonivojskih sistemskih odločitev, na podlagi katerih se je mogoče izogniti prezgodnjim in neutemeljenim načrtovalskim odločitvam. V članku bomo predstavili visokonivojske pristope modeliranja na sistemskem nivoju in predlagali razširjen pristop uporabe abstrakcije. Uporaba predlaganih mehanizmov je sodobnim metodologijam, ki se ukvarjajo s sorodnim raziskovanjem, lahko v veliko pomoč. Predstavljeni so visokonivojski pristopi, njihov vpliv na celoten načrtovalski potek in sistematična integracija v okolje s podporo za SNSPO. Podrobno sta prikazana načrtovalski potek razširjenega koncepta abstrakcije in izvedba podpornih knjižnic, ki omogočata visokonivojsko raziskovanje. Uporaba predlaganega visokonivojskega pristopa je prikazana na praktičnem primeru.

## 1 Introduction

The design complexity of the state-of-the-art systems steeply increases due to the rapidly increasing scale of integration and tightening performance demands. The major driving force behind research activities that are addressing system design is to decrease the constantly growing gap between designer productivity and increase in complexity from the underlying technology, described for example with the Moore's Law. Addressing this gap, the majority of research studies concentrate their work on various abstraction levels of HW/SW codesign /1/-/5/ and they seamlessly deal with different aspects tightly integrated. Although the designer using this approach must be fully aware of different abstraction levels (from purely abstract to implementable) and different aspects (architecture and functionality description, design space exploration, etc.), it is the role of the methodology to define the entire design flow, define all the intermediate steps of it and provide effective means for automating this extremely complex process. As a result, research efforts in HW/SW codesign are focused on seamless integration of efficient methods that the system designer would benefit from.

In this paper we will especially focus on raising the level of abstraction, which is one of the generally recognized approaches /6/-/9/. The concept of abstraction is used to effectively handle complexity at different levels of system realization, starting at system specification and ending at its implementation. Providing adequate evaluation support at system-level specification, premature system-level decisions can be avoided and the design effort can be directed towards detailed exploration of potentially feasible solutions. To enable this, support for abstraction must be leveraged and design stages must be approached systematically, while consistently following system-level optimization efforts.

Unambiguously defined abstraction levels and clearly defined transitions among them directly contribute to automation of lowering the level of abstraction /8/, /11/. Lowering the level of abstraction is based on making design decisions about the system and if the decisions to be taken are within manageable complexity and of a rigidly defined abstraction level, they could be automated. E.g. lowering the level of abstraction from C to the assembler and later to an executable binary code is supported automatically. Automation is enabled by the use of a compiler and design decisions are made by the use of switches. Yet another important reason for heightening the level of abstraction is narrowing the gap between the initial informal description of the system and formal system description

which could possibly be executed and evaluated. Currently there exists a huge gap in this area and system-level approaches that for example use UML /12/ try to cover it.

Based on the above, we propose a system-level design methodology that systematically extends the currently used levels of abstraction. For the methodology a framework implementation is explained. Section 2 classifies the types of abstraction and based on that introduces the contemporary related work. In Section 3 we will focus on transaction level modeling, which is a widely used modeling approach supporting refinements throughout different levels of abstraction. An explanation of the framework supporting extended concept of abstraction will follow in Section 4. Applicability of the extended abstraction level modeling will be demonstrated in Section 5 by means of a case study of a JPEG encoder. With conclusions and plans for future work we will end this paper.

## 2 Related work

Numerous research studies dealing with different aspects of the design methodology have been published /1/-/4/. While the heterogeneity issue of HW/SW codesign is still being under the examination, the research interest is slowly drifting away from the concern about HW/SW boundaries towards higher levels of abstraction. This contributes to leveraging the design productivity and enables more efficient design space exploration.

The today's widely used system-design approach dealing with an abstraction is transaction level modeling (TLM) presented by Gajski et al. in /7/. TLM abstraction is based on an approach where the design description is started by describing only the most important system-level features (specification model). Features unimportant or yet unknown for the current model of the system are simply left out (undescribed). Throughout successive refinement steps (from specification to implementation model) as the designer's knowledge of the system progresses, being the result of the model evaluation feedback, additional features are added to further detail the description of the system. This also corresponds to lowering the level of abstraction. The process of successive model refinement is finished once the model of the system is described at the abstraction level low enough for system implementation by means of automation tools. At every level of abstraction an evaluatable model (EM) is obtained. The model at the lowest level of abstraction encapsulates all the information the designer captures throughout model refinement and consists of all the necessary implementation details. Being an implementation model (IM), it provides grounds for system implementation.

Besides TLM, other types of abstraction can be identified. Jerraya et al. ground their work on the approach introducing layers of intermediate adapters /4/, /10/, /14/. The SPACE methodology applies the concept of layers of services to implement the support for the OS-like-features within SystemC /3/. This type of abstraction is based on the concept of layers of services. Interfaces provide mechanisms for connecting neighboring layers and offer efficient means of access to functionality while hiding realizations implemented within particular layers. For example, SW engineers apply programming techniques using this type of abstraction to successfully cope with complexity. Unlike the aforementioned type of abstraction, here to obtain EM and IM, all layers of abstraction must be fully implemented, as they depend on each other.

The third type of abstraction is based on the concept of platforms, presenting layers of abstraction. At each layer the designer's task is to best map the requirements with abstraction of potential implementations. Choosing a potential implementation at the current level of abstraction introduces specification of requirements for the succeeding lower level of abstraction. Similarly to the first mentioned type of abstraction, here the description of the system also starts with system-level features, but differentiates in that here individual layers of abstraction are not refined, but rather supplement each other with different levels of implementation details. Compared with abstraction based on the concept of layers of services, this type of abstraction provides EMs at all abstraction levels and does not have so rigidly defined layer's stacking. An example of the design methodology applying this concept of abstraction is Metropolis /1/, /16/ based on recursive paradigm of platform-based design /9/, /15/.

Observation of arrangements of abstraction-based approaches led us to the conclusion that these approaches belong to a set of vertical concepts for addressing complexity. They should however be thought of distinctively from a set of horizontal concepts, i.e. component-based approach /10/ and functionality-architecture separation. Horizontal concepts can coexist on all layers of abstraction. For example, the component-based approach is included as its integral part within TLM. Inspection of methodologies reveals that all the above mentioned concepts can be freely combined to leverage the design productivity. For example, Metropolis uses platform-based design (vertical concept), component-based design and application-architecture separation (horizontal concepts). They model heterogeneous systems at higher levels of abstraction by using the Metropolis metamodel specification where system functionality is presented by a set of objects that concurrently perform actions while communicating with each other. Jerraya et al. /2/, /4/, /17/ combine in /14/ the first two types of abstraction with the component-based design. An example of methodology implementation onto a SystemC simulation backbone with the support for OS scheduling is also given in /14/. SPACE methodology /3/ combines first two types of abstractions and component-based design.

C-extension languages, which deal with system-level modeling and HW/SW codesign, like SystemC /6/, /18/ or SpecC /19/, have support for TLM built in. Built around

the SpecC system-level design language /20/, Gajski et al. /7/, /13/ developed an SoC exploration methodology, which covers the entire path necessary for system development. Methodologies that base some of their work on these language extensions also favor variations of TLM, primarily computation-communication separation. The AAA /21/-/23/ methodology relies on the graph theory and focuses on automatic mapping of application to architecture. For manageability they use hierarchy, but to our knowledge, this methodology is weak in abstraction.

In order to enable early system-level exploration (where lower-level details are not captured yet) only the first and the third type of abstraction can be used. The second type does not support this because it requires all layers to be available if model evaluation is to be done. Taking into account popularity of TLM based abstraction approach (throughout the usage of SystemC or SpecC) we concentrated our research work on TLM based abstraction. Nevertheless, we believe the approach we propose can be successfully combined with other two types of abstraction.

## 3 Levels of abstraction within TLM exploration

The starting point in TLM is a functionally complete SW description of the algorithm that needs to be implemented in the system. This forms an un-timed model, called the specification model (presented with circled A in Fig. 1), usually described with a programming language (e.g. C). At this abstraction level, the model yields confirmation of functional correctness of the algorithm description. The functional correctness is later refined to include architectural timing details and component communication is specified in the way that is architecturally implementable. In the final step, a fully functional and fully timed RTL model of the system is obtained (circled F). A detailed explanation of TLM can be found in /6/ or /7/.

The purpose of following the steps of successive refinements is guiding the designer from the starting specification model (also called the system architecture model (SAM) /6/) through the well defined intermediate steps (i.e. levels of abstraction) to the final implementation model (referred to also as the RTL model). By making design decisions and detailing the system description, the designer is able to replace more abstract models with less abstract down to the point where the system description can be used for the system realization by the use of automation tools.

To study the concept of successive refinements supported within TLM, we focused on aspects this approach features. In Fig. 1 it can be observed that the TLM approach favors the description approach where the designer can independently focus on the *computation* and *communication* part of system modeling.

For the purpose of a clearer separation onto problem domains we examined the TLM from the perspective of the Rugby metamodel (RM) /8/, /11/. It has been developed especially for the study of modeling and handles abstraction in essentially more fundamental way. The RM introduces four domains; *computation*, *communication*, *data* and *time*. Terms *computation* and *communication* from the TLM model should not be regarded equal to terms having the same name in the RM. As it will be explained later, these TLM terms are a superset of terms in the RM.

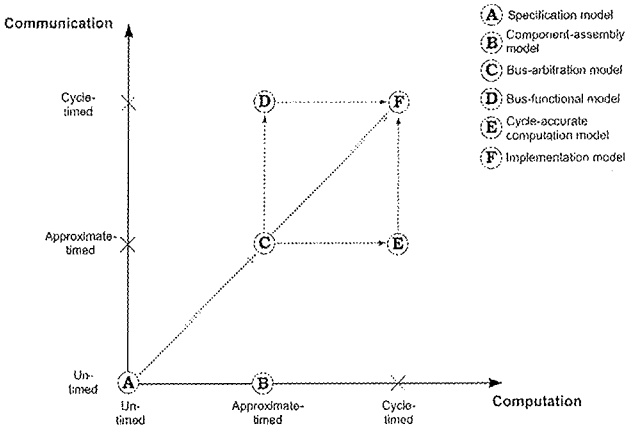


*Fig. 1. The basic concept behind the TLM approach is successive refinement of system description*

*Table 1. Abstraction level exploration in the TLM model*

| TLM aspect | abstraction exploration of... | | | |
|---|---|---|---|---|
| | *computation domain* | *communication domain* | *data domain* | *time domain* |
| *computation* | partial | x | partial | full |
| *communication* | x | full | partial | full |

### 3.1 TLM computation domain

We argue that methodologies offering a formal support from the TLM's specification model onward offer full utilization of abstraction in the time domain (RM) only. The TLM starting system description contains no information about computation durations, which implies a fully abstract time domain (RM). Throughout the TLM refinement steps, timings get gradually defined to a completely time-accurate model, thus lowering the level of abstraction.

On the contrary, we find the data (RM) and the computation (RM) abstraction of quite a low-abstraction level, as the starting model (TLM) is functionally complete and correct. The possible abstraction levels are therefore in these two domains not fully explored. Data to be processed and their processing algorithm (i.e. computation) are in TLM starting point already in their final form. Input test vectors for functional verification can be fully applied and all further refinements deal with timing and communication issues instead. If computation is to be remapped to the HW domain, this becomes the issue of transformation between

the same levels of abstraction, but across the heterogeneity boundary.

Computation row of Table 1 summarizes the above.

### 3.2 TLM communication domain

Here the communication (RM) and time (RM) domains are fully explored throughout the available levels of abstraction. If we take a closer look at the TLM's specification model communication principles, we can see that communication is simply implemented with a mechanism of a shared variable, additionally extended with events /6/, /7/. This kind of communication is obviously of a high abstraction level. Throughout the successive refinements, shared variables are gradually replaced with channels down to the point where every data and every handshake bit level signal of the wire on the communication bus are known. Simultaneously care is also taken for lowering the level of abstraction in the time domain (RM). When communication is abstracted with shared variables, communication takes no time, but throughout the successive refinements an accurate RTL implementation model is gradually obtained.

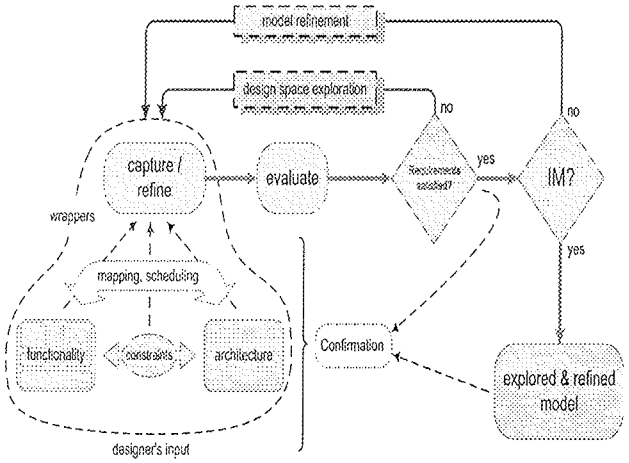


*Fig. 2. The design flow*

Minding the fact that the TLM system model communicates data produced in the computation part of the model, the abstraction level exploration of both data (RM) domains are equal (i.e. only partial).

The bottom row of Table 1 summarizes the above.

### 3.3 Downsides of the TLM approach

In the initial step of the TLM, a model has to be captured in the functionally complete manner in order to allow for the evaluation of high-level design decisions and profiling it for further refinements and design decisions. It is already an established practice to describe the model functionality in a programming language (e.g. C or C++). The major drawback of this approach is the starting point for the description of the algorithm which is, seen from the system perspective, insufficiently abstract. This puts a burden on system-level design alternatives exploration, because a low-level description needs to be included in the model of the system in order to obtain evaluation feedback. In the codesign process, binding ad-hoc decisions at early stages should be avoided as they unjustifiably narrow the available design space and eliminate potentially better design solutions.

Furthermore, the TLM SAM execution model is SW oriented and thus inherently sequential and memory based, while HW is fundamentally concurrent. Sequential algorithms that are proved as effective in SW are seldom the best choice in HW. As it has already been pointed out in literature (e.g. /25/), algorithms targeting HW mostly significantly differ from algorithms targeting SW due to the exploitation of different types of implementation resources. Making further design decisions based on profiling of the SW description (e.g. /13/, /26/) can not provide substantial information for optimal HW/SW codesign.

Even if the issue of inherently suboptimal solution is left aside, raising the level of abstraction addresses the large conceptual gap between the high-level system description and the programming language functional description. We propose a modeling solution at higher levels of abstraction that resembles formal methods of description of UML class diagrams /12/, which is further leveraged with a domain-specific semantics and syntax, promoting it to the form of a formal system specification. A formal high-level specification benefits from an executable specification throughout all layers of abstraction - not only functionally complete.

## 4 The design flow supporting higher levels of abstraction

The approach we propose enables a systematically and intuitively developed model of the system beginning with a description at higher levels of abstraction. This narrows the gap between the informal system specification and the initial formal model description. We provide techniques that enable creation of an executable and evaluatable model of high-level system description starting with pure abstract computation operations, operating on abstract data transmitted through abstract communication channels and taking no or evaluated amount of time. Sequences of transformations between abstraction levels feature smaller gaps, thereby extending a solid ground for future research in the field of automatic transition between successive stages. Important high-level design decisions are in this way fragmented into several smaller decisions, offering improved system level design guidance.

Following our methodology (Fig. 2), designing a system starts by capturing the system-level specifications about the system to be developed. The designer first identifies the system-level functionality, high-level proposition of an architecture and system restrictions and demands (constraints). Wrappers provide support for capturing function-

ality, constraints and architecture. From that an executable specification can be built at all levels of abstraction serving as a basis for analysis of the model. Even at a high abstraction level an executable model of the system is built. Its purpose is evaluation of system level aspects. Throughout lowering the level of abstraction the feedback information about design decisions is becoming more detailed.

After comparing evaluation feedback results with constraints, the designer gets confirmation if the system description is viable or not. If the evaluation results do not meet the specified constraints, changes need to be made in the system description until requirements are met. The process of finding a viable solution at the specific abstraction level is called design-space exploration, shown by an inner loop arrow in Fig. 2. Once the designer's input is found viable (i.e. system constraints are met), the design space is narrowed and the model description needs to be further detailed. Detailing is done by means of model refinement (outer loop arrow in Fig. 2) by means of abstraction principles given in previous text. The process of model refinement has to be done until the level of abstraction is low enough (i.e. the IM is reached), where automated tools can take over.

## 4.1 Wrappers

In order to enable transparent, concise and domain-separated capturing of the specification about a system to be developed, we provide a library of wrappers that promotes application of vertical and horizontal complexity-addressing concepts presented in Section 2. As a vertical complexity-addressing concept we provide techniques that allow capturing and evaluating the system-level information above the levels of abstraction fundamentally supported in TLM. Horizontal complexity-addressing concepts that our methodology supports are functionality-architecture and computation-communication separation. By applying domain separation, the designer can independently focus on each problem domain.

Besides domains separation and capturing and evaluation of the system information, the role of wrappers is also providing basis for fast and easy construction of executable and evaluatable model. Our methodology provides support for firmly based design decisions grounded on the model evaluation feedback results, as for example execution time, resource activity, idle time and utilization share. To relieve the designer of the burden of repeatedly implementing support for these commonly required aspects, we implemented support for logging relevant information as an integral part of wrappers. During model execution, wrapper's logging functionality is responsible for automatic collecting of information by means of simulation traces that can be later reviewed and from them important design decisions can be drawn.

System functionality is intuitively described as a network of tasks that communicate through ports, thus providing grounds for computation-communication separation. For the simulation and evaluation purposes we provide a modeling scheme where all instantiated functionality wrappers (representing tasks) are capable of operating in parallel. From the functionality point of view, the task execution is limited only by their data dependency. The maximum level of parallel operations that specific algorithm permits is first examined and this is later decreased by applying restrictions of execution units. Each task is assigned an execution unit responsible for characterizing the cost of executing services (e.g. time, energy, and size by means of logical block or transistor count) and providing limitations on executions (e.g. resource un/availability). When more than one task specifies the same execution unit, it is up to the execution unit scheduling policy to determine the outcome of such a request. This provides the basis for automatic mapping and scheduling algorithms in the way the design requirements are met.

## 4.2 Backbone for simulation and evaluation

To provide support for describing and evaluating an executable model of the system, we utilize mechanisms provided by the SystemC modeling language. We furthermore leverage them with the proposed concept of the heightened level of abstraction presented in previous sections. As shown in Fig. 3, we provide libraries of wrappers on top of SystemC library /6/, /18/. By instantiating and extending the wrappers with algorithm-specific features, the designer can rapidly capture and evaluate the system description at different levels of abstraction. The description of the system is compiled and executed and simulation traces are obtained. They are used as a basis for system analysis of the applied design decisions.

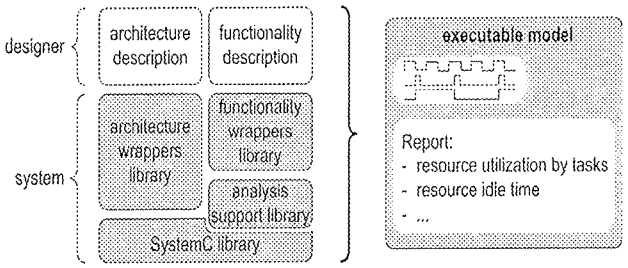


*Fig. 3. Libraries utilization for evaluation*

As depicted in Fig. 3, we built support for functionality wrappers tightly integrated with analysis support and underlying SystemC libraries. Actual implementation of computation is realized within functionality wrappers library. The role of architecture wrappers is to enable a rapid description of architectural resources responsible for services characterization and defining constraints on services required by the algorithm. Services offered by a given architecture are for example characterized by means of execution time, energy, area, etc. Complementary, constraints provide support for issues like for example resource contention and communication not being timeless, etc.

Support for analysis is automatically appended to every instantiated task and collects information relevant for evaluating the system description. After executing a model of the system, collected simulation traces and numerical data are available for analysis. The information collected is based on architecture services utilization, coupled with their constraints and characterization. Various system implementations can be easily built (exploring design space) and feedback results of their evaluations can be used for finding a path towards a solution that best meets system constraints. As it will be shown in the case study section, the information relevant for further design decisions (e.g. resource utilization or task being idle because of resource contention) is obtained automatically.

## 5 Case study – system-level JPEG model exploration

To put the concepts of the proposed heightened level of abstraction into practice, we present a system-level case study of a JPEG encoding system. A more detailed information about the JPEG standard can be found in /27/ and the complete C reference code in /28/. Presenting the entire design flow from the initial idea, over various high-level exploration aspects, down to the final implementation would be much out of the scope of this paper and would even blur the entire idea of the system-level modeling we propose. To our knowledge, the idea of the heightened level of abstraction as presented here has not been presented and studied elsewhere and so we are not able to make side by side comparison conclusions. However, the results we obtain can be proved correct if compared with full implementations, as for example /27/. Differentiation of our proposal essentially originates from the fact that concepts we propose help the designer at abstraction levels that are higher than the level of abstraction used in initial capturing model of the system of the state-of-the-art methodologies.

Fig. 4 depicts an implementation model of a JPEG encoding system targeting a single processor (*processor p1*) and one memory bus (*busUnit b*). The JPEG encoding process consists of four consecutive stages: color-space conversion (*rgb2yuv*), forward discrete cosine transform (*frwrdDCT*), coefficient quantization (*quantization*) and entropy coding (*entrCod*). Other pre and post processing stages (e.g. down-sampling) are omitted here for clarity. It is straightforward to model the JPEG encoding process in this way since it reflects an intuitive flow of data processing stages. According to the aforementioned processing stages we instantiated tasks with data dependency as indicated in Fig. 4, thus forming a formal description and a frame for further detailing. In contrast, Fig. 5 shows a slightly different implementation, offering more architectural resources, with three processors (*p1*, *p2* and *p3*) all connected to a shared memory bus (*busUnit b*).

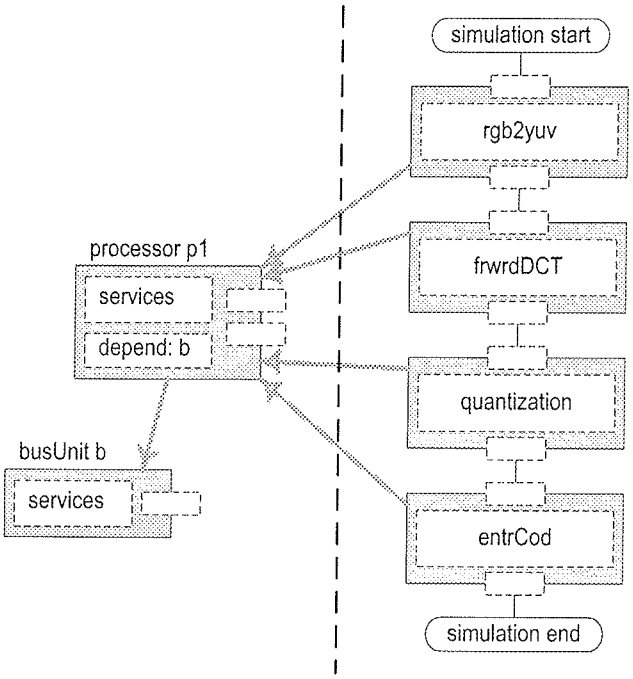


*Fig. 4. JPEG encoding model of the system targeting single processor*

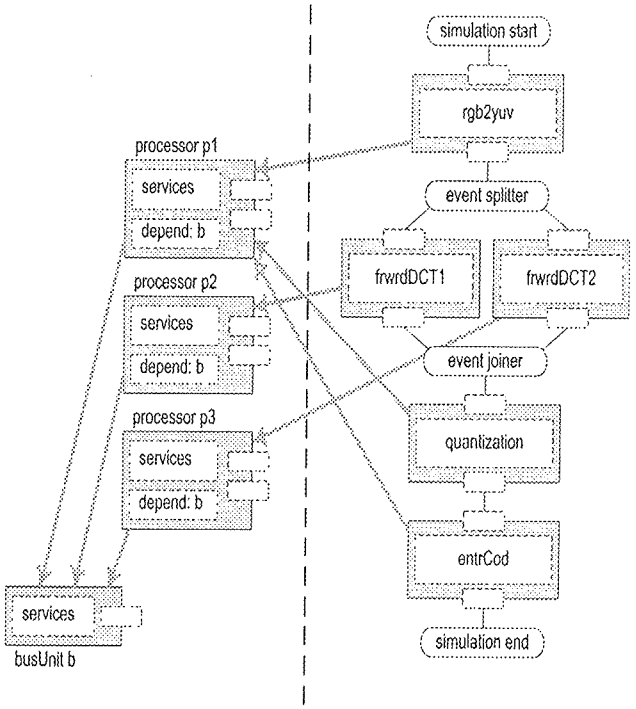


*Fig. 5. JPEG encoding model of the system targeting three processors*

To study the possibility of speedup at the system level, the designer needs to determine high-level properties of the algorithm; the minimum amount of data that can be processed between successive stages is an 8x8 pixel block and a complete color picture is composed of three color planes. To exploit these algorithm properties, we experimented with pipelining where individual color planes are

sequentially fed into the encoder, i.e. immediately after a stage processes one color plane, the data is forwarded to the next stage (firing job request). If based only on data dependency (i.e. without consideration of architectural limitations), the successive stage can start with processing immediately after the first chunk of data is processed in previous stages.

To allow distribution of the processing load in the case where more than one execution unit is available for execution, a simple event splitter is used. It is based on a round-robin scheduler, where jobs are alternatively assigned to *frwrdDCT1* (executed on *p2*) or *frwrdDCT2* (executed on *p3*). Similarly, the event joiner merges job requests from both tasks to execute *quantization* (executed on *p1*).

Fig. 6 lists a high-level algorithm description for the forward DCT encoding stage. When studying a specific DCT realization (e.g. /28/), it can be concluded that 11 multiplications and 20 additions are needed to apply the 1-D DCT transform. These operations represent abstract functions. The purpose of the triple nested *for* loops of Fig. 6 listing, explained from the inside out, is as follows. The 2-D DCT transform (of an 8x8 pixel block) is obtained by applying the 1-D DCT transform to rows first (loop 3) and columns second (loop 2). The pixels to be transformed must be grouped in segments of 8x8 pixels (*structured block* in data domain) (loop 1).

```
void frwrdDCT::MainThread()
{  // divide requested size (m_bytes) into blocks of 8x8 bytes and
   // do 2 pass   1D DCT - horiz.pass: 8B read, processing, 8B write
   // vert.pass: 64B read, processing, 64B write

   int blocks = ROUND_UP( m_bytes, 64 );

   if( m_bytes % 64 )
      cout  << sc_time_stamp()
            << " input size to frwrdDCT is not 8x8 aligned\n";

   for( int i = 0; i < blocks; i++ ) // loop 1
   {
      // pass 0 - horizontal, pass 1 - vertical
      for( int pass = 0; pass < 2; pass++ ) // loop 2
      {
         for( int line = 0; line < 8; line++ ) // loop 3
         {
            m_pExecUnit->GetData(this, (pass==0)?8:32, false);

            // 11MUL, 20ADD
            m_pExecUnit->Mult( 11 );
            m_pExecUnit->Add( 20 );

            m_pExecUnit->WriteData(this, (pass==0)?8:32, false);
} } } }
```

*Fig. 6. High-level description of DCT. Although functionally incomplete, algorithm features are captured.*

To further detail the forward DCT model, the accessing scheme for data storage can be applied. For this purpose, it must be defined how the pixels are stored in memory. Our choice was to store rows of pixels of one color plane into successive memory addresses. This implies that when reading rows (first pass), 8 subsequently read bytes are exactly what we need, but when reading columns (second pass), pixels are scattered in memory, and therefore more consumable memory accesses must be made. As the listing reveals, all requests are performed through execution unit interface (*m_pExecUnit*) attached to every functionality wrapper (functionality-architecture separation).

The models of the other JPEG encoding stages are constituted in a similar manner and won't be further detailed hereafter.

Fig. 7 shows a detailed explanation of a functionality wrapper whose responsibility is to provide common functionality for instantiating user-defined tasks, i.e. in this case study a user-defined encoding stages of Fig. 4 and Fig. 5. The functionality wrapper is provided within our high-level simulation library and it only needs to be extended with algorithm-specific features. It is responsible for accumulating input job requests (via *ExecuteThread event*), executing the user's algorithm (function call *MainThread()*) and signaling job completion (via *ThreadDone event*). Two execution modes are provided. In the first mode (*TriggerThread_in event* is unspecified) all accumulated job requests are executed sequentially without freeing the execution unit (architecture wrapper) between successive runs. In the second mode, a queued job is run only when *TriggerThread_in event* happens. This scheme offers a possibility for different scheduling types. In this case study we applied the first execution mode. The designer's sole responsibility is to implement the encoding stages via method implementation (*MainThread()*) that is executed through a functionality wrapper call.

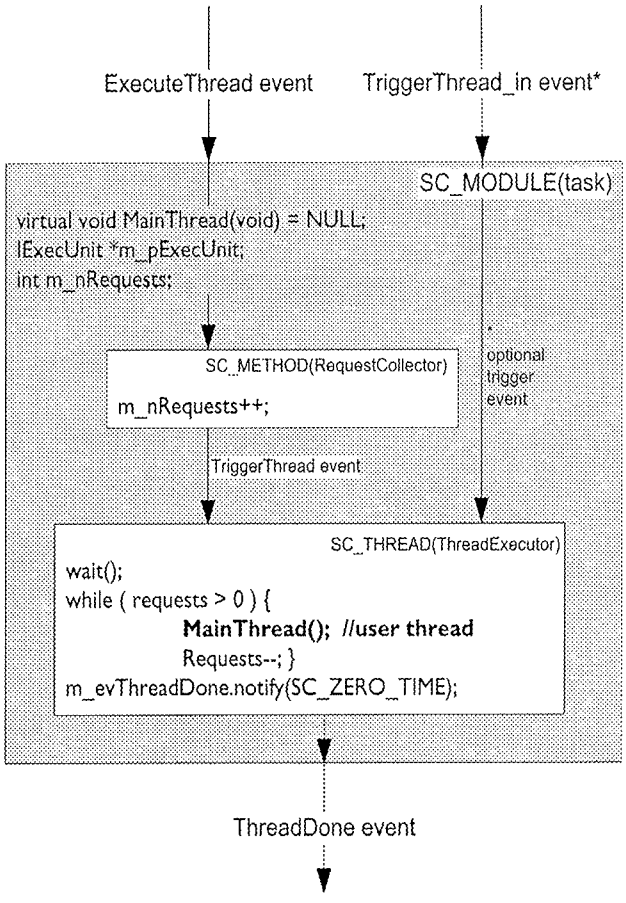


*Fig. 7. Functionality wrapper*

UML static class diagram notation of Fig. 8 illustrates how the model framework is applied to the JPEG encoding sys-

tem. As it can be seen, it is seamlessly connected with system-level modeling libraries we built. The bottom part of the diagram shows classes directly responsible for functionality implementation (*rgb2yuv*, *frwrdDCT*, *quantization*, *entrCod*) and architecture description (*processor*, *busUnit*). The system designer is responsible for the implementation of functionality methods. The top part of the diagram represents the system libraries built on top of SystemC. Decomposition into functionality and architecture can be clearly observed. Every task (implementing functionality as part of the algorithm) that needs to be described must be derived from the system functionality wrapper and must address all computational requests through the execution unit interface (*IExecUnit*). Computational requests are provided with the interface *IExecUnit* and must be implemented by the designer within the architectural description. For example, *processor* is derived from *IExecUnit* and the designer must specify all methods required by the interface. Following this rule, tasks can be simply mapped to their executors at the instantiation time and various mappings schemes can be explored. Following the same rules, the communication unit (*busUnit*) is created. Analysis support, built into the system libraries, provides automatic report generation. The class *unitStats* is responsible for collecting information about each architectural element (active or idle time, which task has occupied it, etc.).

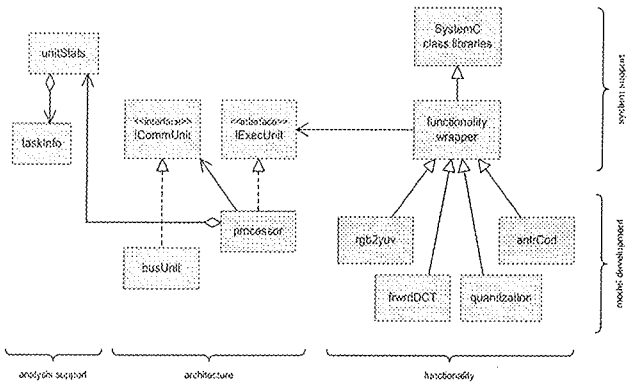


*Fig. 8. Class diagram representation of the JPEG encoder model*

## 5.1 Results

By following the rules and concepts established by our methodology, we built two different system specifications generating two executable models of the system. Results, generated automatically, exemplify the level of information obtained on the basis of a high-level system description. They represent a high-level design decision feedback that our methodology provides. Analysis of these results sets a solid basis for further design decisions. The most important results (automatically generated by *unitStats*) are presented in Table 2 and Table 3, presenting one- and three-processor variants. It should be noted that the task percentage of processor utilization in a single processor variant matches results stated in literature on the basis of a full functional implementation /27/. We obtained these results with the amount of around 100 lines of the source code for the system description (not taking into account our methodology system libraries built on top of the SystemC).

*Table 2. Two processors*

| Architecture | p1 | | bus | |
|---|---|---|---|---|
| RET[ns] | 430 680 | | 93 240 | |
| Functionality | exec. active | task wait | exec. active | task wait |
| rgb2yuv [% RET] | 35.9 | 0 | 12.7 | 0 |
| frwrdDCT [% RET] | 46.8 | 23.9 | 61.8 | 0 |
| quant [% RET] | 13.5 | 31.2 | 18.5 | 0 |
| entrCod [% RET] | 3.8 | 9.0 | 7.0 | 0 |
| total [ns] | 430 680 | | | |

Each table is split into two parts: architectural part (upper) and functionality part (lower). The architectural part shows the resource execution time (RET), i.e. summation of the time the services were required from a specific resource. Complementary, the functionality part presents tasks' active and wait timings (in % of RET). The numbers stated in the *exec. active* column represent the percentage of the time a specific task was being actively executed on a specific resource. Similarly, the numbers stated in the *task wait* column represent the time a specific task had to wait a specific resource to become available – this is the time

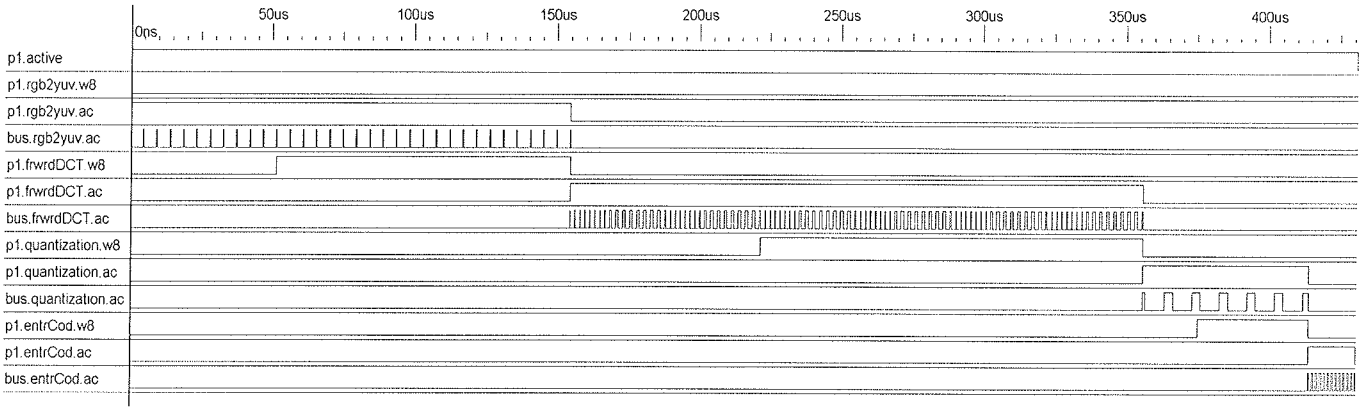


*Fig. 9. JPEG encoding stage timing diagram (single processor)*

*Table 3. Three processors*

| Architecture | p1 | | p2 | | p3 | | bus | |
|---|---|---|---|---|---|---|---|---|
| RET[ns] | 233 460 | | 148 880 | | 75 100 | | 93 240 | |
| Functionality | exec. active | task wait | exec. active | task wait | exec. active | task wait | exec. active | task wait |
| rgb2yuv [% RET] | 66.7 | 0 | - | - | - | - | 12.7 | 1.4 |
| frwrdDCT [% RET] | - | - | 100 | 0 | 100 | 0 | 41.2 / 20.6[a] | 15.5 / 8.5[a] |
| quant [% RET] | 24.9 | 17.7 | - | - | - | - | 18.5 | 0 |
| entrCod [% RET] | 8.4 | 0 | - | - | - | - | 7.0 | 3.32 |
| total [ns] | 261 660 | | | | | | | |

[a] % RET originating from p2 and p3

interval during which a task may be executed regarding data dependency, but its execution is not started because of the unavailability of HW resources.

The second set of results is presented in Fig. 9 and Fig. 10, where the system activity is presented as a function of time. Fig. 9 clearly shows the execution of sequential stages and wait times (abbreviated as w8), consequently induced by pipelined data processing. Fig. 10 reveals that high-level descriptions with even very low complexity can quickly become difficult to analyze manually if parallel execution has to be considered. It can be seen that bus contentions arise, making the task execution time even less predictable. For example, this unpredictability is the reason why *p2* RET is not two times *p3* RET, despite that *p2* processes two color planes and *p3* just one.

In the above we presented design flow steps that enable capturing of high-level information about the system serving as a basis for building an executable and evaluatable model of the system. The model, once compiled and executed, provides an important feedback for further design decisions. After the satisfying high-level model of the system is obtained, the description of the system can be further detailed. Assured that important high-level decisions are formally verified, confidential migration towards an appropriate modeling level within TLM can be approached. The related research work can be used to take over from this point on.

## 6 Conclusion and future work

Our paper opens with an overview of contemporary research methodologies in order to present the reader the role of abstraction these methodologies apply. The use of abstraction is studied, because mastering transformations through abstraction layers is to our opinion the key to leveraging the design productivity. We propose an approach that primarily focuses on the levels of abstraction that are essentially higher than the widely used TLM. The concept of refinements for changing the level of abstraction is explained on the basis of the RM. By doing that, we come to the conclusion that there is still room for specifying levels of abstraction that are higher than in other current state-of-the-art modeling approaches.

In order to provide a framework for exploration at higher levels of abstraction we provide a set of libraries, built on top of the simulation kernel of SystemC, that enables rapid, transparent and formal capturing of high-level information about the system. Based on that, an executable code is obtained that simulates high-level aspects of the system under development. We also introduce an analysis support to provide automatic collection of the feedback data that serves as a basis for model evaluation and further design decisions. Our case study exemplifies the use of the methodology and shows how to quickly capture and transform the information at the proposed levels of abstraction into an executable and evaluatable model.

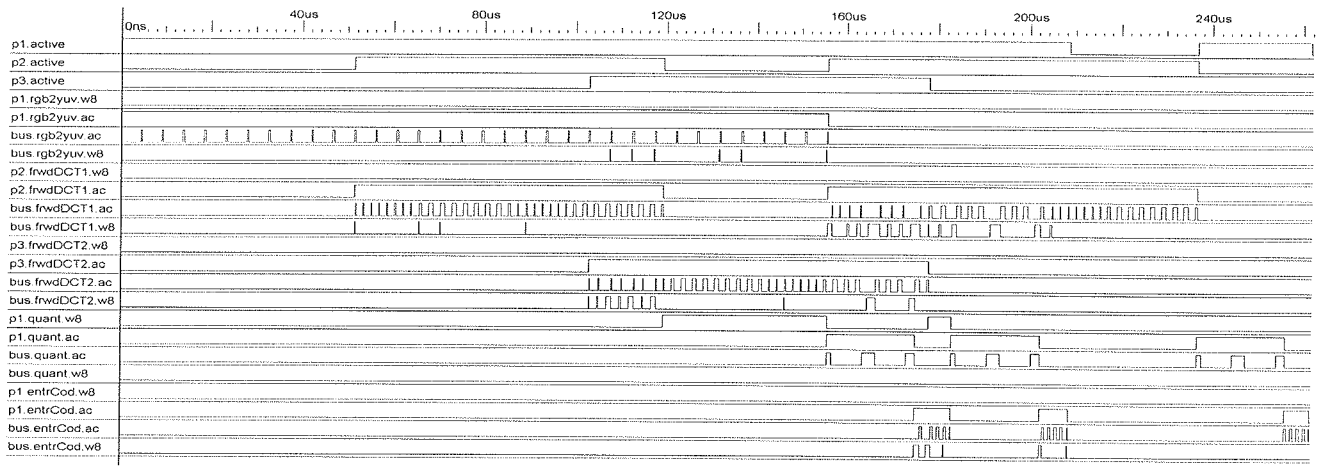


*Fig. 10. JPEG encoding stage timing diagram (three processors)*

Because of the regularities discovered in the process of building the high-level model of the system, in both the algorithm and architecture domain, we are currently engaged in graphical design capturing system together with the infrastructure for automatic code generation that we currently have to obtain by hand. Our long term plans involve implementing the design flow within the graphical modeling environment. Because of its rich extensibility, the GME modeling platform is considered as a modeling framework /29/, /30/.

## 7 Acknowledgment

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*Jože Dedič, B.Sc.,*
*joze.dedic@fe.uni-lj.si,*
*Matjaž Finc, M.Sc.,*
*matjaz.finc@fe.uni-lj.si,*
*Assistant Prof., Dr. Andrej Trost,*
*andrej.trost@fe-uni-lj.si*

*University of Ljubljana*
*Faculty of Electrical Engineering,*
*Tržaška 25, 1000 Ljubljana, Slovenia*
*Tel: +386 1 4768 351*

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# CALIBRATION SYSTEM FOR SMART PRESSURE SENSORS

Matej Možek, Danilo Vrtačnik, Drago Resnik, Uros Aljančič, Samo Penič, Slavko Amon

University of Ljubljana, Faculty of Electrical Engineering, Laboratory of Microsensor Structures and Electronics, Ljubljana, Slovenia

**Key words:** smart sensor, digital temperature compensation, calibration, pressure sensor

**Abstract:** *A modular design of high throughput calibration system for smart pressure sensors is presented. Based on obtained results, the capacity of calibration system is 250.000 sensors per year. In addition, a novel digital thermal compensation technique is introduced, using system self-learning capability for optimization of calibration parameters. Calibration results on a run of 16568 sensors show reduction of temperature error over entire temperature range from initial 0.15%FSO/°C to 0.05%FSO/°C.*

# Sistem za umerjanje tlačnih senzorjev

**Kjučne besede:** inteligentni senzor, digitalna temperaturna kompenzacija, umerjanje, tlačni senzor.

**Izvleček:** V prispevku je predstavljena modularna zasnova sistema za umerjanje tlačnih senzorjev. Na osnovi prvih testov je kapaciteta sistema 250.000 senzorjev letno. Predstavljena je izboljšana metoda digitalne temperaturne kompenzacije senzorjev preko optimizacije parametrov umerjanja na osnovi zmožnosti samostojnega učenja sistema. Rezultati umerjanja na 16568 senzorjih kažejo na zmanjšanje temperaturne napake preko celotnega uporabnega temperaturnega področja s prvotnih 0.15%FSO/°C na 0.05%FSO/°C.

## 1. Introduction

Smart sensors represent an attractive approach in sensor applications for industry automation due to their adaptability, achieved by means of digital signal processing. Smart sensors are generally integrated with signal conditioning circuits. Signal conditioning circuits are necessary to adjust the offset voltage and span, compensation of temperature effects on both offset voltage and span, as well as to provide an amplified signal. Several piezoresistive pressure sensors with integrated signal conditioning have been presented over the past few years /1/. Temperature compensating methods for these sensors are based either on analog, digital or mixed approaches. Analog approach usually comprises an amplifier with laser trimmable thin film resistors /2,3/ or off-chip trimmable potentiometers /4,5/, to calibrate the sensor span and offset voltage and to compensate the sensor temperature drift. Analog compensation techniques are relatively slow, inflexible and cost-ineffective. In digital approach, sampling for raw digital pressure and temperature values is first performed, followed by evaluation of the output digital values via transfer polynomials, and converting the computed pressure value to according analog voltages. Mixed approach retains strictly analog signal conversion path, while presetting the offset and span of operational amplifiers by digital means /6/.

Low cost advanced differential sensor signal conditioners /6,8/ can accommodate nearly all bridge sensor types with signal spans from 1 mV/V up to 275mV/V. Sensor's temperature dependence can be compensated by temperature sensing element, which can be either on-chip (usually an additional bridge resistor) or off-chip (thermistor, internal diode or external diode). The output can be adapted either to analog voltage output (0...5V) or current output (4...20mA) as well as digital outputs: PWM, $I^2C$, SPI or OWI (one-wire interface). Sensor signal conditioner can also be transformed into a simple controller by means of digital outputs which can trigger an actuator. Output resolution can be selected from 10 bits to 15 bits, with the highest sampling rate up to 3.9kHz.

The excitation of sensor comprises ratiometric voltage (externally regulated), constant voltage (on-chip) or constant current (on-chip). Sensor connection fault is detected instantaneously by comparison of the range of sensor input voltage. Variations on the common mode voltage of the sensor are monitored permanently - this enables monitoring of sensor aging. Extended temperature operation enables a wider application range in automotive industry.

However, these sensor signal conditioner features cannot be turned into an advantage without a dedicated calibration process.

Design of the actual calibration system itself is smart since the system represents a digitally-controlled closed loop, capable of self-learning. Closed loop design enables the optimization of calibration procedure parameters as well as of mentioned smart sensor properties. On the sensor level, calibration system contains orthogonalization of input quantities and full-scale output (FSO) optimization. The latter is the basis of the pre-calibration, which is performed upon entire lot of calibrated sensors. Furthermore, the system contains dedicated statistics software, which gives a detailed insight into smart sensor acquired data and calibration coefficients. The obtained statistical data provide closed loop feedback parameters, while at the same time represent the input data for failure analysis.

## 2. Calibration setup

Figure 1 shows a general setup of smart sensor calibration system. The setup consists of sensor calibration station, central database server and post-calibration sensor test systems. Calibration station performs the calibration procedures upon DUC (devices under calibration). Central database server gathers data from distributed databases which reside locally in every calibration station. The server performs analyses upon gathered dataset and provides the "intelligence" of the system. Finally, post-calibration sensor test subsystems provide means for evaluation of sensor properties during final testing such as thermal cycling and sensor packaging.

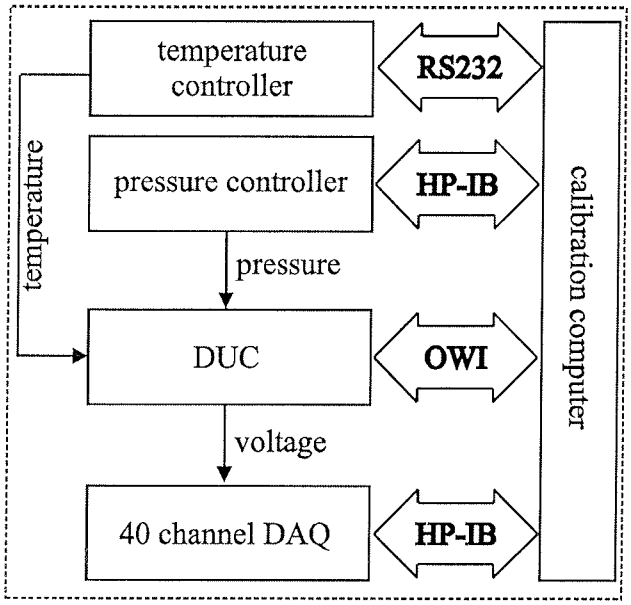


*Fig. 1: Smart pressure sensor calibration system block diagram*

### 2.1. Data acquisition

Calibration procedure starts with the acquisition of calibration points. The calibration points can be ordered into an *arbitrary* calibration scenario. Number of calibration points is chosen between 5 and 8, depending on the degree of evaluation polynomial . Chosen degree is a tradeoff between desired calibration accuracy and duration of entire acquisition. The acquisition stage of calibration procedure follows the numbered order of calibration points starting at least pressure and temperature, as shown in Figure 2.

Based on tests performed, among all 7-point calibration scenarios, the one presented in Figure 2 yields most accurate results if the middle temperature point is set at room temperature.

Calibration accuracy is depending primarily on the number of calibration points at a given temperature, while the acquisition time is primarily dependent on the temperature stabilization at a given calibration point. Calibration time

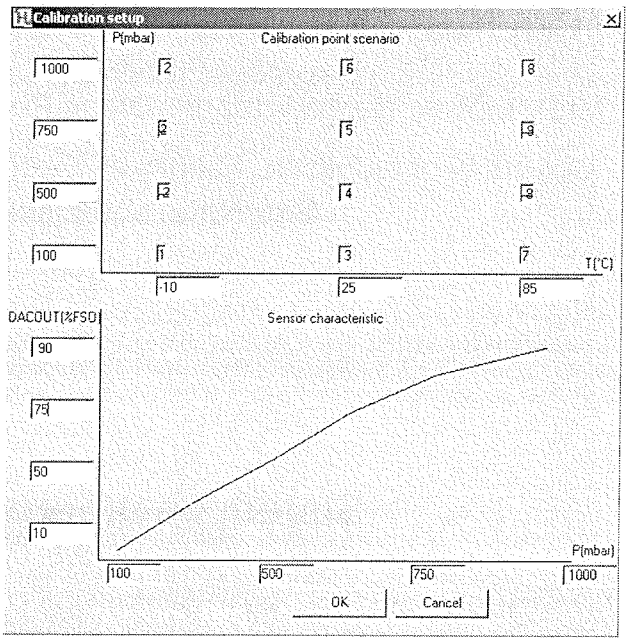


*Fig. 2: Calibration scenario*

can be shortened by means of zone calibration i.e. measuring entire sensor production lot at a constant temperature at all pressure points. This principle can be further enhanced by introduction of Peltier element temperature controller that was reported elsewhere /7/.

Each of calibration points consists of pressure controller set point ($p$), raw pressure sensor output ($Z_P$) and raw temperature sensor output ($Z_{T1}$) and a D/A converter output from signal conditioner (*DACOUT*).

#### 2.1.1. Sensitivity compensation algorithm

The system is able to match sensor sensitivity to the desired measurement range. The system initially presets the lowest sensitivity on all sensors and applies full-scale pressure. Sensor response is read. If the read raw pressure conversion result is within ASIC D/A converter limit interval, the sensitivity is increased by selecting higher setting of programmable gain amplifier in sensor ASIC and the output is measured again. When the gain setting is too high, the output reads maximum D/A converter output value ($FFFF_{16}$). The highest gain setting is selected, that yields the maximal output.

By measuring uncompensated pressure sensor offset and its full-scale output, the measurement range of the signal conditioner ADC is adapted resulting in its maximum bit yield. Typically 99% ADC bit yields are achieved. This reduces the importance of uncompensated pressure sensor sensitivity and offset. Low sensitivity can be improved by setting the programmable gain amplifier (*PGA*) in the signal conditioner, while shifting the entire ADC measurement range compensates high offset voltages. This enables the use of sensors whose offset can be greater than its signal, as is the case with very low-pressure sensors.

### 2.1.2. D/A converter thermal response adjustment

Signal conditioner's 11-bit D/A converter response features large chip-to-chip differences when used in the temperature range (typ. ±50 levels at 85°C) as can be seen from rightmost histogram bar width in Figure 3. Figure 3 shows the D/A converter readout histogram at calibration point 7 (85°C). Number of calibrated smart pressure sensors was 16568. Histogram bars on the left represent the number of sensors, which can be considered faulty due to their inadequate D/A converter response at calibration temperature.

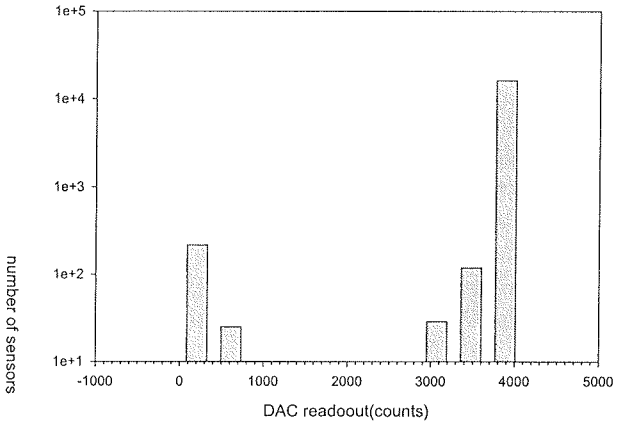


*Fig. 3: Signal conditioner D/A readout at calibration point 7 (pressure=1000mbar, T=85°C)*

Deviations of D/A converter's response over temperature range, shown in Figure 3, are compensated by a dedicated D/A calibration mechanism, which provides means for minimization of sensor specific errors (e.g. calibration point to calibration point errors) as well as system specific errors (e.g. signal conditioner chip to chip errors). The D/A calibration mechanism is based on the successive approximation method, where every sensor's D/A output is connected to 40-channel DAQ (data acquisition) system as indicated in Figure 1.

This arrangement of instruments forms a closed regulation loop, which tests all 11 bits in the sensor's D/A output according to successive approximation algorithm. After the desired voltage output is achieved, the result is normalized to DAC resolution and stored for further computation of calibration coefficients. This is performed in such a manner that the desired transfer characteristic is obtained at every temperature calibration setpoint.

The speed of closed regulation loop was improved with implementation of a dedicated 40 channel SAR (successive approximation register) and a precision comparator.

## 2.2. Orthogonalization of calibration points

Next step in calibration is the orthogonalization of acquired calibration points. Calibration points are orthogonalized along the temperature axis only, since pressure controller provides satisfactory pressure setpoint precision. Orthogonalization is included in the process of calibration points acquisition and is achieved at each setpoint by means of digital filtering, where a simple averaging filter is used to stabilize temperature within desired temperature gradient limits. The main advantage of this approach lies in the location of temperature measurement, which is located in the device under calibration (i.e. on the sensor ASIC or on the pressure sensor membrane). Since temperature controller shown in Figure 1 is left out of temperature stabilization process, this method detects faulty sensors by means of device under calibration temperature stabilization timeout, which is currently set at 20s.

## 2.3. Calculation of calibration coefficients

Pressure sensor's signal conditioner uses two-dimensional rational polynomial for pressure calculation /8/, which enables correction of nonlinearities up to the third order.

$$Y=\frac{Z_P+c_0+2^{-(R-1)}c_4Z_{T1}+2^{-2(R-1)}c_5Z_{T1}^{\ 2}}{c_1+2^{-(R-1)}c_6Z_{T1}+2^{-2(R-1)}c_7Z_{T1}^{\ 2}}$$
$$p=Y(1-2^{-15}c_2-2^{-15}c_3)+2^{-15}c_2Y^2+2^{-15}c_3Y^3 \qquad (2.1)$$

Where $c_0$ through $c_7$ are calibration coefficients of pressure sensor, $p$ is the normalized DAC output resulting from successive approximation algorithm, described in section 2.1. The value of p is in interval [0..1). $Z_P$ is an offset corrected raw A/D readout from pressure sensor and $Z_{T1}$ is a chip-offset corrected raw A/D readout from temperature sensor. Note that the actual temperature and pressure set points have only indirect significance to further calibration process, since the calculation polynomial not dependent on them. More important is the temperature and pressure stability at the desired calibration setpoint.

The resulting pressure output of the sensor can be adapted to various orders of calibration, ranging from linear to third-order nonlinearity calibration. Hence, a wide variety of algorithms are implemented into calibration coefficients calculation.

If $c_2$ and $c_3$ coefficient ($2^{nd}$ and $3^{rd}$ order nonlinearity) are set to zero, the remaining coefficients can be determined by solving a system of linear equations. However, this system is resolved by computing a Vandermonde matrix, which is generally ill conditioned. This can lead to large deviations from sensor characteristic. Generally, a sensor characteristic using the equation is evaluated by full set of coefficients or at least with $c_3$ set to zero. In this case a set of nonlinear equations must be resolved. This can be achieved by implementing several iterative methods such as Newton-Raphson, Wegstein and Broyden /9/. Special attention has been devoted to use of Broyden method, since it does not include calculation of Jacobian matrix at each iteration. The latter can be singular, which can fail the progress of iterations.

Both approaches have been combined into automatic algorithm for determination of a complete set of coefficients. Initial guess, prerequisite for later iterations, can be evaluated by setting $c_2$ and $c_3$ to zero. This yields an exact first-order solution, which serves as initial guess input into Broyden algorithm. The higher order nonlinearities ($c_2$ and $c_3$) have generally small values (or high for bad sensor). If a Broyden algorithm yields $c_2$ and $c_3$ coefficients zero, an exact solution is used. Calculation is evaluated versus all calibration points and a combined standard uncertainty is calculated according to RSS (square root of the sum-of-the-squares) method. In order to avoid large deviations from sensor characteristic, the Vandermonde system is solved and resulting coefficients are validated against preset sensor type limits, which are stored in the database.

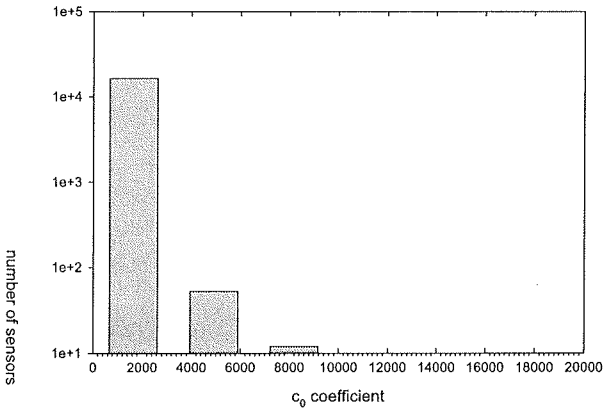


*Fig. 4: Coefficient $c_0$ limit distribution*

## 2.4. Validation of calibration coefficients

A test lot of sensors is calibrated repeatedly, until sufficient amount of data is gathered. Each of coefficients $c_0$ through $c_7$ are then plotted into corresponding histogram. Figure 4 shows the distribution of $c_0$ coefficient value for 16568 sensors. Coefficient validity interval in Figure 4 is initially set at 16-bit integer range, so the entire dataset is plotted. After calibration of test-lot, the interval is subsequently narrowed to [0..3000] as shown in Figure 4. The validity interval could be narrowed more, but as validity criteria for all coefficients ($c_0..c_7$) are superimposed, this is more than sufficient. This iterative evaluation of coefficients was implemented into an algorithm for automatic setting of calibration limits, which represents the basis of system self-learning. Human intervention is required only until a sufficient amount of sensors are calibrated. During that initial phase system is learning what criteria denote a good sensor. After that, the system autonomously makes more and more sharp distinctions between good and bad sensors.

## 2.5 Storage into database

Smart sensor's database record consists of 39 fields, which can be divided into several groups. Calibration setup related information, describing record number, timestamp of calibration and ISO63 date code for a lot as well as sensor position in calibration system and calibration identification number. Smart sensor calibration settings are ASIC configuration word, calibration validity interval and calibration coefficients $c_0..c_7$. Calibration point related settings such as values of raw pressure and temperature sensor response and results of D/A converter calibration. The contents of records enable complete traceability of calibrated sensors and statistical processing of calibration effectiveness.

## 3. Measurements and results

The calibration procedure has been implemented upon a series of 16568 automotive sensors. Temperature selectivity with typical lower and upper sensor error bands are presented in Figures 5, 6 and 7, each corresponding to selected temperatures -10°C, 25°C and 85°C, respectively. Results are plot within minimum and maximum admissible temperature error bands according to /9/. Temperature error is calculated as a normalized difference between ideal MAP sensor response and the calibrated response. Typical temperature selectivity of raw pressure sensor 0.15%FSO/°C has been reduced to 0.05%FSO/°C with the use of digital temperature compensation. Raw, uncompensated sensors without signal conditioner and digital temperature compensation have temperature selectivity typically 2.5%FSO/°C, around -10°C.

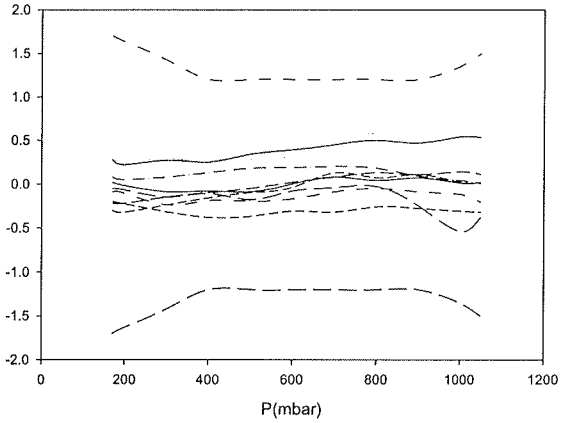


*Fig. 5: Temperature selectivity at -10°C*

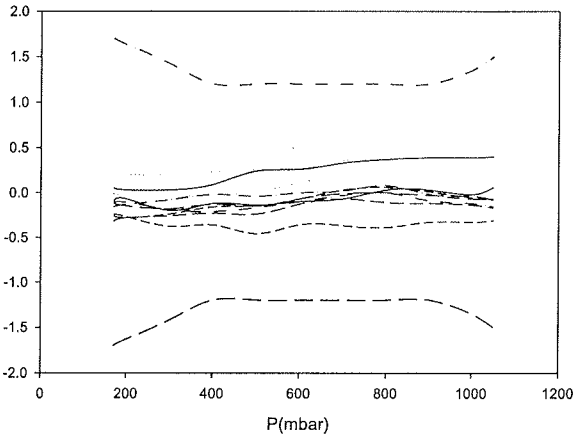


*Fig. 6: Temperature selectivity at 25°C*

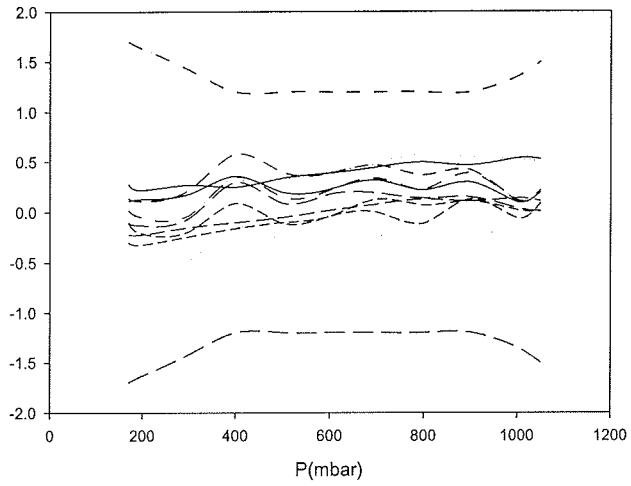


*Fig.7: Temperature selectivity at 85°C*

## 4. Conclusion

Smart pressure sensor calibration system has been designed, fabricated and tested. Sensor calibration setup and calibration software have been tested on a production lot consisting of 16568 Manifold Absolute Pressure sensors. Calibration results show significant improvements in sensor temperature response, achieved by means of digital temperature compensation approach presented in this paper.

Acknowledgments: **This work was supported by Ministry of Higher Education, Science and technology of Republic of Slovenia within program R-252 and HYB d.o.o. Trubarjeva 7, 8310 Šentjernej.**

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*mag. Matej Možek*
*doc.dr. Danilo Vrtačnik*
*doc.dr. Drago Resnik*
*mag. Uroš Aljančič*
*Samo Penič, univ. dipl. inž. el.*
*prof.dr. Slavko Amon*

*University of Ljubljana, Faculty of Electrical Engineering,*
*Laboratory of Microsensor Structures and Electronics*
*Trzaska 25, Ljubljana 1000, SLOVENIA*
*e-mail: matej.mozek@fe.uni-lj.si*
*Telefon: 01 4768 380, Telefax: 01 4264 630*

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# 1. Slovenska fotovoltaična konferenca SLO-PV 2006
# 1st Slovene Photovoltaic Conference

## Poročilo s 1. Slovenske fotovoltaične konference (Ljubljana, 21. september 2006)

Zaradi vedno večjega zanimanja v Sloveniji za izkoriščanje sončne energije preko fotovoltaike smo na Fakulteti za elektrotehniko Univerze v Ljubljani v sodelovanju s slovensko Tehnološko platformo za fotovoltaiko organizirali prvo slovensko fotovoltaično konferenco (SLO-PV 2006), ki je potekala v četrtek, 21. septembra 2006 na Fakulteti za elektrotehniko v Ljubljani pod generalnim sponzorstvom podjetja HSE d.o.o. in Bisol d.o.o. Konference se je udeležilo preko 180 udeležencev iz vrst raziskovalcev, inženirjev, gospodarstvenikov, srednješolskih učiteljev in zasebnih investitorjev.

Program konference je bil sestavljen iz štirih tematskih sklopov: predstavitev svetovnih in slovenskih tehnologij v fotovoltaiki, predstavitev evropske in slovenske fotovoltaične tehnološke platforme, izmenjava izkušenj slovenskih načrtovalcev fotonapetostnih sistemov in predstavitev sončnih elektrarn v Sloveniji. Detajlne vidike konference s programom in posameznimi prredavanji si lahko ogledate na SLO-PV 2006 spletnih straneh http://slo-pv.fe.uni-lj.si.

Konferenco je svečano otvoril častni predsednik dr. Jože Zagožen, generalni direktor Holdinga Slovenske elektrarne d.o.o., ki je poudaril pomembnost raziskav novih tehnologij in vlaganj v vse vire električne energije in da bo fotovoltaika igrala v prihodnje vedno bolj vidno vlogo. Na konferenci se je slovenski javnosti prvič predstavilo podjetje Bisol d.o.o. s sedežem v Velenju, ki je prvo slovensko podjetje na področju proizvodnje fotonapetostnih modulov. Po dveh letih razvoja je julija letos uspešno zagnalo proizvodnjo multikristalnih silicijevih modulov z načrtovano letno proizvodnjo 15MW, kar predstavlja skoraj 1% trenutne letne svetovne proizvodnje fotonapetostnih modulov. Največji slovenski proizvajalci električne energije iz sončnih elektrarn

so predstavili zasnovo in obratovanje svojih elektrarn. Ekonomsko atraktivna odkupna cena električne energije iz sončnih elektrarn kvalificiranih proizvajalcev 89,67 SIT/kWh je bila v letu 2004 ponujena samo majhnim sončnim elektrarnam (do 36 kW), zato so se v Sloveniji v zadnjih dveh letih gradile samo majhne sončne elektrarne. Trenutno znaša skupna moč okoli 250 kWp. Z novo uredbo julija letos (Ur.l. RS

75/2006) pa je odkupna cena 89,67 SIT/kWh ponujena tudi kvalificiranim proizvajalcem srednjih in velikih sončnih elektrarn in v kratkem lahko pričakujemo še hitrejšo rast investicij v sončne elektrarne.

*Dr. Marko Topič*

*Predsednik konference*

*SLO-PV 2006*

# Enaindvajseta Evropska fotovoltaična konferenca in razstava – Slovenski raziskovalci nagrajeni za najboljši poster v sekciji

# 21st European Photovoltaic Solar Energy Conference and Exhibition – Slovene Researchers Were Awarded the Best Session Poster Award

Twenty-first European Photovoltaic Solar Energy Conference and Exhibition

Dreseden, 4th - 8th September 2006

Na nedavno končani enaindvajseti evropski konferenci o fotovoltaiki je raziskovalna skupina Laboratorija za polprevodniške strukture in optoelektroniko, Fakultete za elektrotehniko Univerze v Ljubljani prejela nagrado za najboljši poster v sekciji 5 "PV Modules and Components of PV Systems", kjer je bilo prijavljenih 130 prispevkov. Prispevku :

"Effective Efficiency and Performance Ratio as Energy Rating System for PV Modules"

Marko Topič (1), Kristijan Brecl (1), J. Kurnik (1), J. Sites (2)

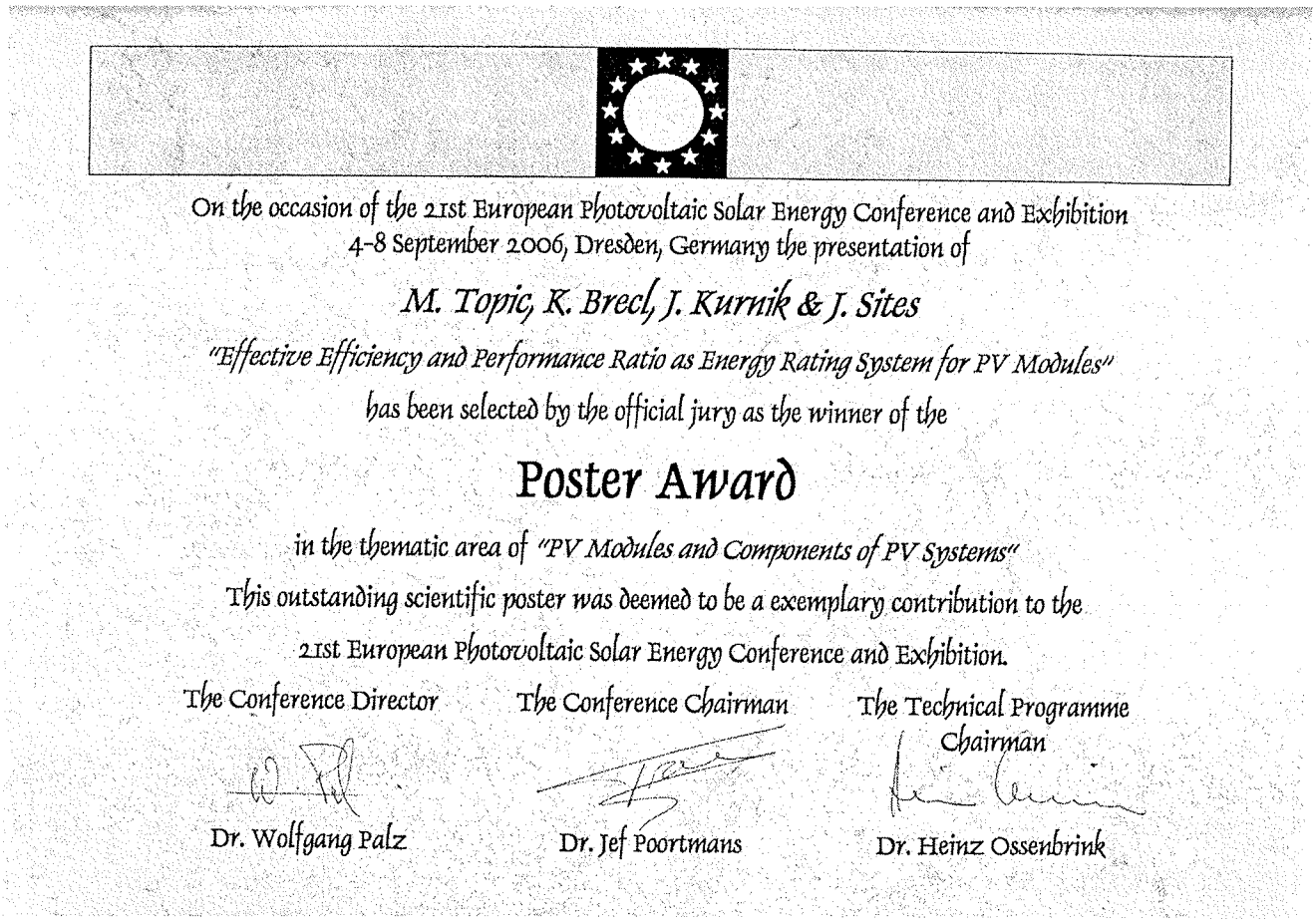
(1) Faculty of Electrical Engineering, Slovenia

(2) Colorado State University, Fort Collins, USA

**je bil podeljen POSTER AWARD**

Na konferenci so podelili 8 takšnih nagrad, za vsako sekcijo posebej:

1 Fundamentals, Novel Devices and New Materials
2 Crystalline Silicon Solar Cells and Materials Technology
3 Amorphous and Microcrystalline Silicon
4 CIS, CdTe and other (II-VI) Ternary Thin Film Cells
5 PV Modules and Components of PV Systems
6 PV Systems in Grid-Connected Applications
7 Global Aspects of PV Solar Electricity



On the occasion of the 21st European Photovoltaic Solar Energy Conference and Exhibition
4-8 September 2006, Dresden, Germany the presentation of

*M. Topic, K. Brecl, J. Kurnik & J. Sites*

*"Effective Efficiency and Performance Ratio as Energy Rating System for PV Modules"*

has been selected by the official jury as the winner of the

**Poster Award**

in the thematic area of *"PV Modules and Components of PV Systems"*

This outstanding scientific poster was deemed to be a exemplary contribution to the 21st European Photovoltaic Solar Energy Conference and Exhibition.

The Conference Director — Dr. Wolfgang Palz

The Conference Chairman — Dr. Jef Poortmans

The Technical Programme Chairman — Dr. Heinz Ossenbrink

8 Specific issues of PV-Industry, Commerce and Finance

Vseh prispevkov na konferenci je bilo okoli 1100. Konferenco je obiskalo 2.700 znanstvenikov, predstavnikov industrije in politikov iz 95 držav. Spremljajočo komercialno razstavo z enako tematiko pa je obiskalo 3.600 obiskovalcev.

Samo »industry day« je obiskalo 1.300 udeležencev.

O razsežnosti dogodka priča »PRESS RELEASE«, ki je bil objavljen po konferenci in razstavi.

## *European PV Solar Energy Conference establishes itself as world's leading event*

*6,300 scientists, industry representatives and politicians from 95countries met in Dresden.*

*Dresden / Munich, 14.09.2006 - The 21st European Photovoltaic Solar Energy Conference (EU PVSEC) closed last Friday with arecord-breaking number of visitors. 2,700 scientists, industry representatives and politicians from 95 countries and around 3,600 visitors to the parallel trade exhibition informed themselves on the latest developments in solar energy generation. The EU PVSEC has positioned itself as a platform for exchange between research and industrial application. The figure of around 6,300 participants and specialist visitors fromall over the world shows how far this transfer has expanded.The European Photovoltaic Solar Energy Conference is supported by various bodies including UNESCO, the European Commission and the Federal Ministry for the Environment.*

*Dr. Jef Poortmans, Program Director Photovoltaics at the Interuniversity Microelectronics Center (IMEC) in Leuven, Belgium, described the positioning of the conference and exhibition from the scientist's perspective: "The EU PVSEC is the world's most important event for the exchange of scientific, technical, strategic and economic information in the area of photovoltaics," he explained during his opening speech as Conference Chairman.*

*"Business-to-Business-to-Science", was the brief formula used by Dr. Winfried Hoffmann, General Manager of SCHOTT Solar and President of the European Photovoltaic Industry Association, EPIA in his opening speech to describe the conference and exhibition's positioning and significance. He said that at no other conference and exhibition is there such a lively exchange of research, industry and politics. The entire spectrum of solar energy generation from the basics in the area of silicon to the global aspects of photovoltaics in the context of energy supply was explored in over 900 speeches and presentations.*

*In his welcome speech, Michael Müller, the parliamentary secretary of state at the Federal Ministry for the Environment, Nature Conservation and Nuclear Safety described energy and raw materials as the key issue of the 21st century. Müller sees the EU PVSEC as a symbol of the change which is currently taking place. Germany represents about 60% of the world photovoltaics market and there are around 3,500 companies operating in this branch of industry, many of whom are world market leaders.*

*Setsuo Luchi, the head of department at the Japanese Ministry for Economics, Trade and Industry (METI) described Japan's solar energy strategy. He said that the production of solar-generated electricity has been promoted by the state in Japan since 1974. Since 1997, the promotion of renewable energy sources has been anchored by legislation. According to Luchi, this has been a dramatic success: thanks to effects of scale, the costs of solar generated electricity dropped in Japan by over 80% between 1993 and 2002. The METI believes that a further cost reduction of 85% by 2030 is realistic. There are plans to quadruple the 2004 production level of 1.13 gigawatts to 4.82 gigawatts by 2010.*

*Michael Eckhart, President of the American Council on Renewable Energy, gave an impressive description of the change in thinking, which is currently taking place in the US. He said that it is not just the cost of petrol, which has recently doubled for US consumers, that has given rise to this paradigm shift. Broad sections of the public are also becoming aware of the dangers of climate change. Politicians have recognised the risk of increasing reliance on oil imports. In the USA, the promotion of renewable energy sources is under the authority of the Federal States. One major breakthrough in this regard is the Million Solar Roofs programme, initiated by Arnold Schwarzenegger, the Governor of California, under which solar power plants with a capacity of around 3 gigawatts are to be built over the next few years with an investment of $3.2 billion. The USA was represented at the EU PVSEC with 18 speeches in the fields of research and industrial application.*

*A highlight of the EU PVSEC was the presentation of the Becquerel Prize, first awarded by the European Commission in 1989 to mark the 150th anniversary of the discovery of the photovoltaic effect by the Frenchman Alexandre-Edmond Becquerel. This year the prize went to the American, Dr. Richard Swanson. Dr. Swanson, who founded the company SunPower in 1991, after spending twenty years in research, was distinguished for his groundbreaking work in the development of high-efficiency silicon solar cells. Using SunPower solar cells, NASA's solar-powered research aircraft, Helios, reached an altitude of just under 30,000 metres in 1999 - an altitude which had never before been reached by a non rocketpowered aircraft.*

*With a total of 6,300 participants and specialist visitors, the EU PVSEC broke visitor records. Of the total, around 2,700 were registered as participants at the conference. Around 3,600 specialist visitors attended the parallel industry exhibition. According to Peter Helm, Managing Director of the Munich project developer, WIP Renewable Energies, "the participant and visitor structure reflects EU PVSEC's function as an interface for research and industry. At the same time, it impressively underlines how conference and exhibition complement each other". WIP-Renewable Energies has been the organiser of the EU PVSEC since 1986.*

*The EU PVSEC 2006 is supported by the European Commission, the Federal Ministry for the Environment, Nature Conservation and Nuclear Safety, UNESCO, the World Council for Renewable Energy (WCRE), the European Photovoltaic Industry Association (EPIA), the German Solar Industry Association (BSW e.V.) and the City of Dresden.*

# 1981-2006 TWENTY FIVE YEARS IN EUROPE

Murata is celebrating 25 years in Europe and is justly proud of it's role in the technology revolution over this period both in Europe and worldwide in developing advanced ceramic based products for the modern and future electronics market. Survival in a dynamic and dramatically changing market remains a serious challenge which Murata is well placed to meet with a focus on business **Agility, Flexibility and Innovation** embedded in the company philosophy, policies and product development. Murata has successfully introduced exciting products to many markets including the all important Automotive market here in Europe and worldwide.

*Back in the days: D. Oram and T.Churcher*

*Fleet, UK Locations*

*Enjoying japanese food*

The Company was inaugurated in Europe in 1981 and in 1988 formally established the Murata European Headquarters in Nuremburg, Germany. 1989 was very productive with establishment of the factory in Plymouth UK and a network of satellite locally facing sales offices established across Europe including Amsterdam which is now the European Headquarters.

Like many electronics companies following strong growth through the 1990's, Murata is now facing the shift of production to the Far East but remains both globally and in Europe, a financially strong and independent company.
Murata has extended partnerships with customers and concentrated on developing products based on their needs and projects.

muRata
*Innovator in Electronics*

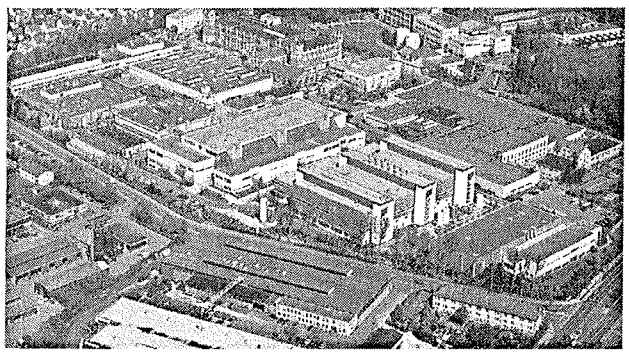
*25th Anniversary Image*

# NOVICE
# NEWS

## Bosch to build new semiconductor fab in Reutlingen

The Bosch Group is investing some 550 million euros in the construction of a new manufacturing facility for 200 millimetre (eight-inch) semiconductors at its site in Reutlingen, near Stuttgart. Construction of the facility is to begin in the autumn of 2007. Rollout of production is planned for mid-2009. The plant will have a total capacity of up to 1,000 silicon wafers per day, equivalent to a daily production volume of up to one million microchips. "In investing heavily in state-of-the-art manufacturing technology, we are securing the long-term future of our international automotive electronics business," said Franz Fehrenbach, chairman of the Bosch Board of Management. Bosch has been manufacturing 150-millimeter (six-inch) semiconductors in Reutlingen for ten years now. The location can therefore draw on a wealth of expertise and has a good infrastructure.

Semiconductor and micromachined chips from Reutlingen are used above all in the automobile industry. As components in electronic control units, they form the "central nervous system" of many functions in the vehicle, including electronic safety systems such as ABS, ESP, or airbags, fuel-efficient and clean engines with electronic engine management, or modern driver assistance systems. On average, between 100 and 200 application-specific microchips are installed in a middle or luxury-class car. "We anticipate that the semiconductor market for automotive applications will grow by an average of ten percent per year in the medium term," said Dr. Bernd Bohr, member of the Bosch Board of Management and Chairman of the Automotive Group. In addition, the company is opening up additional marketing channels, especially in consumer electronics, via its recently founded subsidiary Bosch Sensortec. In total, some 800 jobs will be created in the new 200-millimeter semiconductor manufacturing facility by 2012. The company will be able to cover most of its requirements for qualified personnel internally - drawing especially on associates from a nearby facility.



The new 200-millimeter wafer fab in Reutlingen will mainly be geared to the "smart power process." In this technology, integrated circuits combine on one chip highly sensitive signal processing and high-voltage circuits for the control of high-performance actuators. These chips have to work reliably even under the especially tough thermal and mechanical loads experienced during automobile operation. The technology applied here uses ultra-fine structures, which are deposited on the chips. In the initial stages, these structures will be 0.35 micrometers wide - far less than one hundredth of the diameter of a human hair. At a later stage, Bosch plans to halve structure width to 0.18 micrometers. Precision such as this makes extremely high demands of manufacturing technology. In addition, MEMS technologies are also to be rolled out in the 200-millimeter wafer fab, manufacturing micromechanical sensors that are used above all in the automobile, but also in cell phones, handhelds, or games consoles. With this move, Bosch is ensuring that it will be able to draw on the most advanced manufacturing technology in this growth market.

## Central China's first 12-inch fab

Semiconductor Manufacturing International Corporation ("SMIC"), announced that the first 12-inch (or 300mm) fab in Central China began construction in the Wuhan East Lake New Technology Development Zone, Hubei Province, China. The groundbreaking ceremony was attended by Yu Zheng Sheng, Politburo member of Central Committee and Secretary of Hubei provincial party, Luo Qing Quan, Governor of Hubei Province, Chen Yu Jie, Director of the Overseas Chinese Affairs Office of the State Council, Li Hai Feng, Deputy Director of the Overseas Chinese Affairs Office of the State Council and Richard Chang, President and CEO of SMIC.

The facility will be financed by an investment company associated with the Hubei provincial government, Wuhan City government and Wuhan East Lake New Technology Development Zone. The company, the Wuhan Xinxin Semiconductor Manufacturing Corp, will own the facility and has engaged SMIC to manage the facility. The fab is scheduled to be completed by the end of 2007. and commercial production is scheduled to start in the first half of 2008.

The monthly 12-inch wafer capacity is estimated to be 12,500 initially and increase progressively up to 20,000-25,000 in 2009.

"We recognise the important contribution that SMIC has made to China's semiconductor industry. The Hubei Province will provide the necessary infrastructure support in order to help build up a world-class semiconductor industry in the region." said Miao Wei, Secretary of the Wuhan Municipal Committee.

"We are grateful that the Hubei provincial government and the Wuhan City government have provided such invaluable support to the semiconductor industry in the region," said Richard Chang, President and CEO of SMIC. "We have every confidence in the future prospects of the Wuhan fab."

## Intel quietly opens Irish 65nm fab

IDA Ireland, the government development agency, was forced to withdraw an offer of EU R170 million in state funding for the new wafer fabrication facility last year after the EU signalled it would not allow further local funding. Intel proceeded with its plans to open the facility, but warned that it would reconsider potential investments in the Irish region.

Speaking at the opening of the factory, Bertie Ahern said that he welcomed Intel's decision to locate its new facility in Leixlip. "Today's event is a continuation of the success story for Intel Ireland which is the largest Intel operation outside the US, employing almost 5,000 people," said Ahern.

Intel is expected to release its new microarchitecture shortly and the presentations at the opening and subsequent press releases reveals part of the marketing strategy is designed to announce the company's intention of claiming back market share from rival AMD. Despite clearly being the largest manufacturer and investor of microprocessors, the company has seen AMD move ahead in the high end server market as well as a few niche areas. There was much effort in describing Europe's first full 65nm facility and products shipped ahead of the crowd. The enthusiasm in this message unfortunately only highlighted that the company has been worried by AMD's advances.

"Intel is establishing a clear technology lead with our next generation of dual-core processors based on the Intel Core microarchitecture," said Intel President and CEO Paul Otellini. "Our manufacturing capability is key to fueling Intel's success."

Intel has achieved an important manufacturing milestone with its three 65nm factories. Known as manufacturing "cross-over," it means that Intel is currently producing more than half its PC and server microprocessors using this process technology. During a ceremony to officially open the Ireland factory, Otellini said that the 300mm wafers that began running through the new facility three months ago helped the company reach this milestone.

"Intel's ability to ramp advanced 65nm silicon technology into high-volume production in three factories clearly sets us apart," said Otellini. "The combination of 65nm technology and Intel's new Core microarchitecture changes the game in terms of the benefits we can provide our customers."

During the summer Intel will introduce Intel Core2 Duo processors for desktop and notebooks the Dual-Core Intel Xeon processor 5100 series. Intel also claimed it is on track to begin production using 45nm process technology by the end of 2007.

## SEZ gains momentum in Asia Pacific

The SEZ Group announced it has received multiple-system orders for more than a dozen Da Vinci tools from industry-leading chipmakers based in Taiwan and Singapore. Placed by top foundries-both new and existing customers-the orders extend SEZ's momentum in Asia Pacific, following other recent purchases from customers in China and Korea.

Moreover, as several of these customers are focused on memory-device manufacturing, the orders underscore that the Da Vinci platform is serving as a catalyst for the escalating shift to single-wafer wet processing within the memory sector. While logic chip manufacturers have led this transition, memory makers and foundries are increasingly seeking the cost and performance advantages of single-wafer applications for their advanced manufacturing operations.