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A New Quantum-Based Building Block for Designing a Nano-Circuit with Lower Complexity

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Abstract: Next-generation nano-scale computational systems are being hampered by two significant obstacles: shrinking transistor size and power dissipation. Moore's law does not hold when transistor size reaches the atomic level. So, it becomes necessary to investigate alternative technologies that surpass traditional Complementary Metal Oxide Semiconductor (CMOS) technology's physical constraints. Quantum Dot Cellular Automata (QCA), a transistor-free computational paradigm, is thought to be the best alternative to CMOS technology for designing nano-scale logic circuits. However, not many designs cut energy usage and offer straightforward access to inputs and outputs. Moreover, adders, the primary component in logic circuits and digital arithmetic, are crucial in developing several efficient QCA designs. In this context, the 4-bit Ripple Carry Adder (RCA) is a straightforward type of adder that can help produce circuits with minimal necessary space and power consumption because of its exceptional qualities. The synthesis of high-level logic further demonstrates the design's effectiveness. The outcomes of QCADesigner demonstrated that the proposed circuits are less complicated and use less power than earlier designs compared to conventional design approaches.

Keywords: Nanotechnology; Quantum-dot cellular automata; XOR gate; Majority voter gate; Full adder; Ripple Carry Adder

Nov gradnik na kvantni osnovi za načrtovanje nano vezja z manjšo kompleksnostjo

Izvleček: Računalniške sisteme naslednje generacije v nano merilu ovirata dve pomembni oviri: zmanjševanje velikosti tranzistorjev in razprševanje energije. Moorov zakon ne velja, ko velikost tranzistorja doseže atomsko raven. Zato je treba raziskati alternativne tehnologije, ki presegajo fizikalne omejitve tradicionalne tehnologije kovinsko oksidnih polprevodnikov (CMOS). Quantum Dot Cellular Automata (QCA), računska paradigma brez tranzistorjev, naj bi bila najboljša alternativa tehnologiji CMOS za načrtovanje logičnih vezij nano velikosti. Vendar pa ni veliko zasnov, ki bi zmanjšale porabo energije in omogočile neposreden dostop do vhodov in izhodov. Poleg tega so seštevalniki, glavna komponenta v logičnih vezjih in digitalni aritmetiki, ključni pri razvoju več učinkovitih zasnov QCA. V tem kontekstu je 4-bitni Ripple Carry Adder (RCA) enostavna vrsta seštevalnika, ki lahko zaradi svojih izjemnih lastnosti pomaga pri izdelavi vezij z minimalno potrebnim prostorom in porabo energije. Sinteza logike visoke ravni dodatno dokazuje učinkovitost zasnove. Rezultati programa QCADesigner so pokazali, da so predlagana vezja manj zapletena in porabijo manj energije kot prejšnje zasnove v primerjavi z običajnimi pristopi načrtovanja.

Ključne besede: nanotehnologija; kvantni točkovni celični avtomati; vrata xor; vrata večinskega volivca; popolni seštevalnik; ripple carry adder

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1 Introduction

High leakage power and sub-node scaling of 22 nm technology are issues that transistor-based technologies must deal with [1]. These problems motivate designers of Very Large-Scale Integration (VLSI) to create a different technology for the next Integrated Circuits (ICs) and diode-based technologies [2-4]. To address the issues with CMOS technology [5], VLSI designers are looking into a number of other technologies, including Quantum-dot Cellular Automata (QCA), single

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electron transistors, and tunnel field effect transistors. Compared to competing technologies, QCA technology provides a number of advantages, including a smaller footprint need, quick switching times, and reduced power dissipation [6].

QCA is a very intriguing and well-liked technology for creating nano-scale logic circuits. There are no transistors in the QCA technology. The QCA cell, which comprises 4 quantum dots, is the fundamental unit of QCA [7]. This method is energy-efficient since there is no actual charge movement between QCA cells. Logical values are determined based on the electrons' location in quantum dots. Due to Coulombic contact, electrons in a QCA cell are situated at the opposing corners. There are two logics 1 or 0 values in each cell. On the other hand, these advantages led researchers to develop a number of projects that explain how to construct QCA circuits [8]. Adders, SRAM [9], ALUs, switching, encoder-decoders [10], reversible logic, and memories are just a few of the recently invented circuits. Full adders play a very prominent part in digital circuits since they are employed in the creation of logical and mathematical processes [11]. Therefore, building a QCA-based adder with reduced space, shorter delays, straightforward access to inputs and outputs, and lower complexity will be more crucial than ever [11]. This paper uses a novel, low-complexity, and low-power three-layer full adder circuit to suggest a new QCA-based ripple carry adder (RCA) design for improving the previous designs. With simple access to inputs and outputs, XOR and majority gates were used to create an RCA circuit, and the results were compared to earlier designs. All protected Nano-communication networks [12] are designed using adders and RCA designs. QCADesigner-E as a usually used tool for power analysis, will be utilized in this paper for simulation and assessment.

The structure of this essay is as follows. The background of QCA is presented in Section 2, with a focus on its distinctive cells. The 4-bit RCA's detailed architecture is shown in Section 3. Section 4 displays the simulation's findings. Finally, the paper is concluded in the last section.

2 QCA background and related works

This section discusses the important and basic parts of this technology and the best previous works related to the subject.

1.1 QCA Cells and Wires

A QCA cell is a square nanostructure with four quantum dots (micro), roughly as shown in Figure 1(a). In the context of QCA, "micro" refers to the individual components or elements of the system, namely the quantum dots. These quantum dots are the building blocks of QCA and serve as the basic units of information processing [13]. In the cell, a tunnel junction connecting two pairs of quantum dots allows for the passage of two electrons between them. The two electrons are positioned in the cell at opposite ends because of Coulombic repulsion [14, 15]. In the context of QCA (Quantum-dot Cellular Automata), nonlinear and linear refer to different types of behavior exhibited by the system. Linear QCA refers to a system where quantum dots' behavior can be described using linear operations, similar to classical digital logic gates, while nonlinear QCA involves more complex interactions between quantum dots, resulting in nonlinearity due to quantum effects like Coulomb interactions and electron tunneling [16]. There is no cell-to-cell tunneling; tunneling only takes place within the cell. Bisectional behavior results from the interaction of the discrete electronic charge, Coulombic repulsion, and quantum confinement. Binary "0" and "1" with polarisations of "1" and "+1", respectively, can be represented by the two charge configurations. A QCA "wire" is a chain of cells contiguous to one another, as opposed to a physical wire, as depicted in Figure 1 (b). As there are no electron tunnels between cells, QCA offers a method of information transfer without current flow [17].

1.2 QCA Logic Gates

The fundamental gates of QCA are inverters and three-input majority gates. A majority gate comprises 4 cells that achieve the function of M (a, b, and c) = ab+bc+ac, as shown in Figure 2 (a) [18]. Cells are placed diagonally from one another to achieve the inversion functionality, as shown in Figure 2 (b). Inverters and majority gates make up a universal set that can be employed to implement any logic operation. By setting one of the

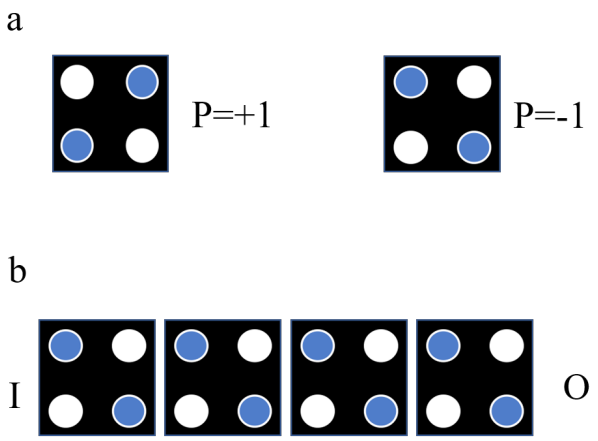

Figure 1: Structure of basic QCA: (a) QCA cells, and (b) QCA wire.

majority gate inputs to "0," for instance, AND (a, b) = M (a, b, 0) = ab, a two-input AND gate is realized. In the same manner, an OR gate is implemented by setting one input to "1," i.e., OR (a,b) =M (a,b,1) = ab + b 1 + a 1 = a + b [19].

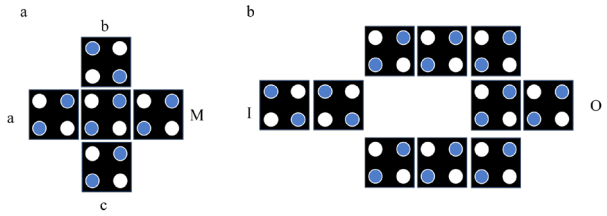

Figure 2: Structure of basic QCA: (a) Three-input majority gate, and (b) Inverter gate.

1.3 QCA Clocking

To drastically reduce metastability issues and enable long pipelines, adiabatic switching is used for QCA clocking. One-half of the wire is used for signal transmission during each clock cycle, and the other half is left unpolarized [20]. The cells in the active clock zone that is still present cause the newly activated cells to become polarized during the subsequent clock cycle, which deactivates half of the previously active clock zone [21]. As a result, signals continue from one clock zone to the next. Four-phase clock signals are used to control four different circuit areas. Each zone of the clock signal has four states: high, low, low to high, and high. When the status changes from high to low, the cell starts to calculate and keeps the value while the state is low. The cell is released when the clock is in the low-to-high state and not operating [22].

1.4 Related work

This section reviews numerous significant and useful recommendations for the design of sophisticated and straightforward QCA RCA circuit designs. Abedi, et al. [23]. propose a cross-level QCA architecture in a full adder QCA design. Additionally, supplied proposed a RCA that is based on this design. Using *QCADesigner*, these designs have been accuracy-tested and assessed. Compared to earlier methods, conventional evaluation methodology and particular cost function QCA were applied for superior performance. The suggested RCA has a delay period of 1.75 clock cycles and uses 262 cells in a 0.208 μm^2 area. Also, Balali and Rezai [14] proposed a QCA structure for the full adder to create a high-speed, efficient, and reliable four-bit RCA using the QCA technology. Their modeling results have demonstrated that there are significant increases in circuit speed and latency. To verify the accuracy of these designs, QCADesigner was employed. The four-bit RCA that is suggested in the QCA technology is designed with minimum complexity and high speed. It has a delay of 1.25 clock cycles and 209 cells in a 0.3 μm^2 area. Also, the fundamental QCA and QCA-based digital design concepts have been put out by Chan, et al. [24]. The creation of straightforward digital logic utilizing certain QCA approaches has been discussed in this article. The four-bit ripple adder has been provided using a combinational notion from the traditional RCA and the CLA. These circuits were implemented utilizing the 5-input majority gate, which theoretically can lower the latency of the traditional QCA-based RCA. The recommended adder has a latency of 3.25 clock cycles, an area of 2.5 μm^2, and 1246 cells. The designed structures have been verified using the QCADesigner. Finally, Hashemi and Navi [25] suggest a reliable QCA and an RCA full adder circuit based on a successful five-input majority gate. These circuits have employed a robust crossover design in comparison to similar designs. Owing to the full adder circuit's efficient architecture, it has been employed for RCA design in a variety of scales. The coherent and bistable simulation engines of the QCADesigner have used to simulate the suggested designs. The proposed RCA uses 442 cells with an area of 1 μm2 and a delay of 2 clock cycles.

2 Proposed design

This part presents and simulates new designs and effective architectures for a one-bit QCA full adder and four-bit QCA RCA. One-bit QCA full adder block diagram is illustrated in Figure 3, and the exploited full adder's QCA-based layout with a three-input majority gate and three-input XOR gate is shown in Figure 4. This complete adder comprises 15 cells and uses 0.5 clock cycles to generate outputs with a 0.01 μm2 area and simple input and output connectivity. This three-layer implementation of a QCA full adder uses ordinary QCA cells. Input cells are A, B, and C, and output cells are COUT and SUM. In this design, the first layer acts as an XOR gate and is used to generate the SUM, while the second layer is utilised to transmit values to the third layer, where all of the circuit's inputs are applied and the COUT output is generated.

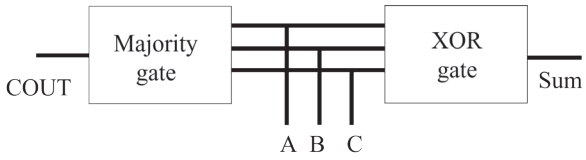

Figure 3: QCA-based full adder diagram

The proposed adder can easily implement the higher adder designs. Higher adders, such as 4-bit RCA, have been designed using this Complete adder with fewer QCA cells, which is entirely distinct from earlier ver-

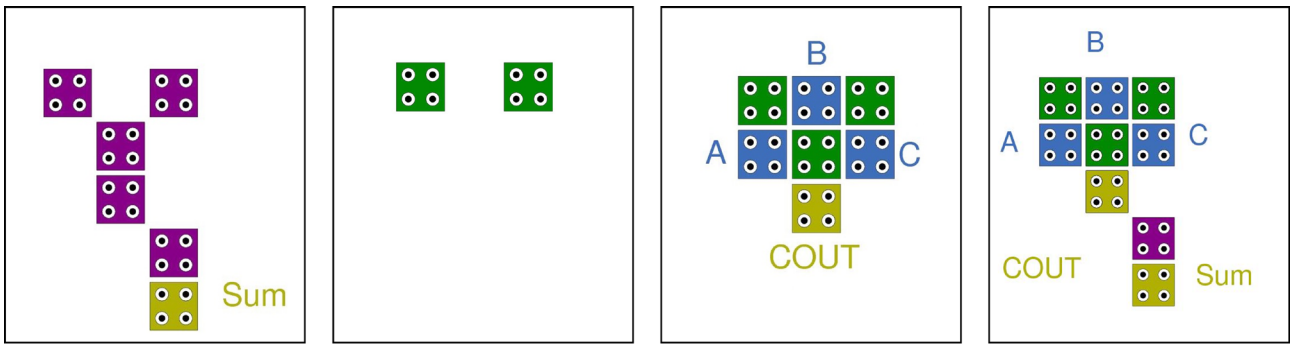

Figure 4: QCA-based full adder layouts and layers

sions. The proposed four-bit RCA design is illustrated in Figure 5 with its structure. Also, a four-bit QCA-based RCA that uses four one-bit full adder QCA-based circuits as its structural unit is also depicted in Figure 6. The 72 cells in the suggested four-bit QCA-based RCA have an area of 0.11 μm^2 and a delay of 1.75 clock cycles. All of the inputs and outputs on this three-layer circuit are accessible. There are five outputs (S0-S3, COUT) and 9 inputs (A0-A3, B0-B3, C). The outputs in this design are easily accessible because they are not encircled by other cells. To transfer signal output, this structure does not need a wire in other words. Thus, it is simple to feed the outputs to another QCA input.

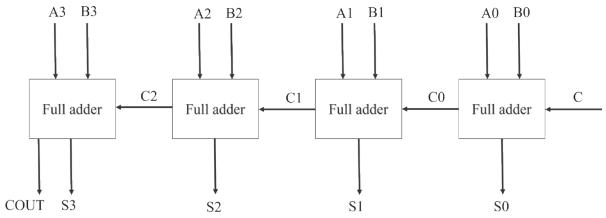

Figure 5: The proposed schematic for 4-bit RCA

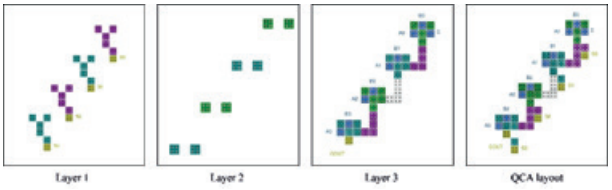

Figure 6: Three layers of the proposed QCA-based 4-bit RCA

3 Simulation tool and results

The software QCADesigner-E is used in this paper to simulate the suggested design [26]. Fast design, layout, and simulation of QCA circuits are made possible by QCADesigner software. Table 1 contains all of the simulation parameters for the simulated objects. The default parameters for all simulation measures and conditions are used in this tool [27].

Table 1: Simulation parameters

Parameter	Bistable approximation engine Value	Coherence Vector engine Value
Cell size	18 *18 nm^2	18 *18 nm^2
Radius of effect	65 nm	80 nm
Relative permittivity	12.9000000	12.9000000
Clock high	9.8e−22J	9.8e−22J
Clock low	3.8e−23J	3.8e−23J
Clock amplitude factor	2.000000	2.000000
Clock shift	0.000000e+000	0.000000e+000
Layer separation	11.5000 nm	11.5000 nm
Maximum iterations per sample	100	-
Number of samples	12800	-
Convergence tolerance	0.001000	-

The constructed full adder circuit simulation results are shown in Figure 7. All possible states have been applied to the circuit's inputs, and the outputs have created the desired outcomes, as shown in the correct table. Both outputs are formed concurrently after two clock cycles. The third layer of this full adder, designed in three layers, receives the three inputs and processes them to produce the COUT output from the third layer and the SUM output from the first layer. The accuracy of the suggested designs was demonstrated by these simulations, which were run using the default settings. Tables 2 and 3 compare the supplied full adder and RCA circuit cell, latency, and space usage to the best previous designs.

Table 2: Comparisons among the designs

Designs	Area (μm^2)	Cells	Delay (Clock cycle)
Proposed design	0.01	15	0.5
Ahmadpour, et al. [28]	0.01	20	0.5
Seyedi and Navimipour [6]	0.01	22	0.75
Sarmadi, et al. [29]	0.04	30	1.0
Sayedsalehi, et al. [30]	0.02	33	0.75

Figure 8 displays the simulation results for the QCA-based RCA circuit. The circuit generates the proper output when subjected to every possible condition. Actually, Figure 8 displays the outcomes of the simulation for the variables A0, A1, A2, A3, B0, B1, B2, B3, and C. As depicted in the figure, the circuit receives input from all potential states and generates the desired output. Also, simulation results show strong polarization of the output cells for this circuit.

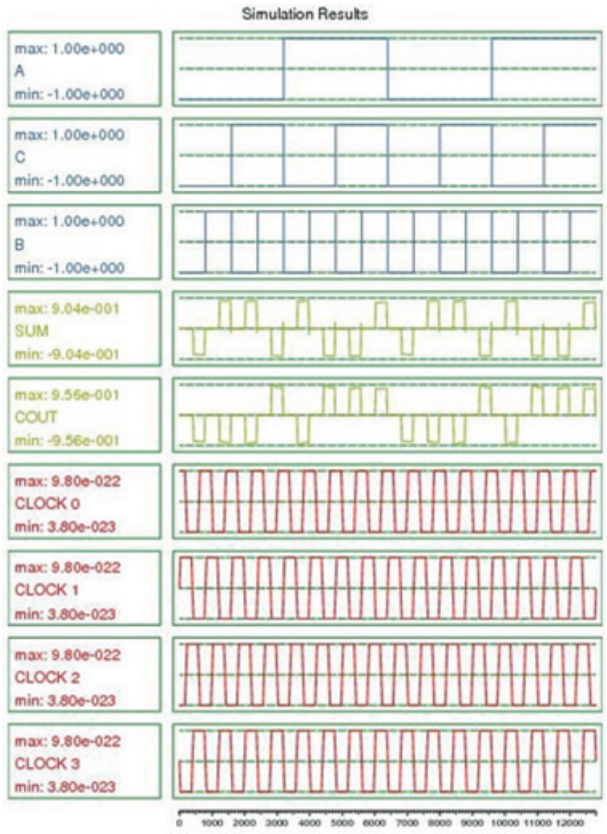

Figure 7: Simulation outcomes of the proposed design

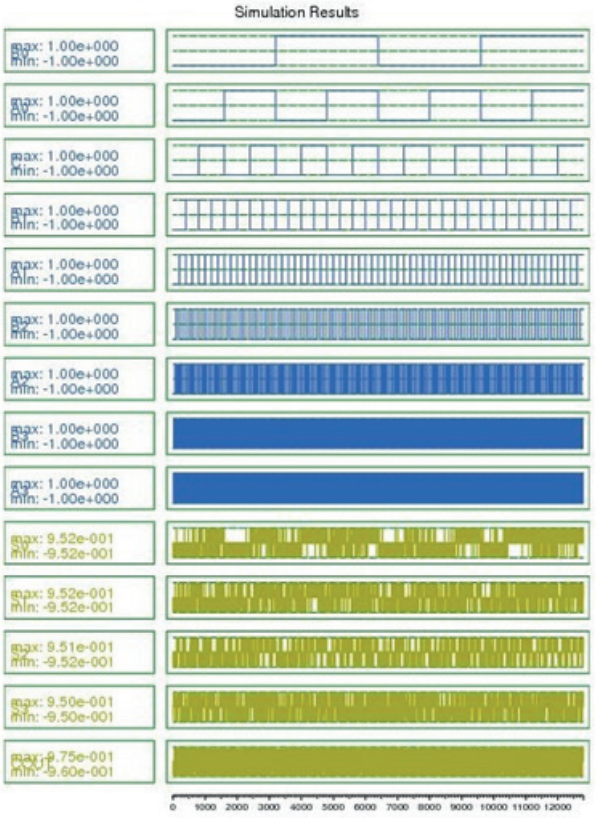

Figure 8: Simulation result of the proposed RCA

Table 3: Comparisons among the RCA designs

Designs	Area (μm^2)	Cells	Delay (Clock cycle)
Proposed design	0.11	72	1.75
Balali and Rezai [31]	0.3	209	1.25
Sonare [32]	0.51	366	2/5
Rashidi and Rezai [33]	0.14	175	1
Abedi, et al. [23]	0.208	262	1.75
Mohammadi, et al. [34]	0.24	237	1.5
Labrado and Thapliyal [35]	0.3	295	1.5

Table 4: Comparison of total and average energy dissipation

Designs	Power and energy analysis	
	Total energy dissipation (eV)	Average energy dissipation (eV)
Proposed full adder design	1.458	1.057
Ahmadpour, et al. [28]	1.25	1.15
Seyedi and Navimipour [6]	1.55	1.56
Sarmadi, et al. [29]	1.80	1.87
Sayedsalehi, et al. [30]	1.69	1.55
Proposed RCA design	2.80	2.63
Balali and Rezai [31]	2.48	2.59
Sonare [32]	2.74	2.70
Rashidi and Rezai [33]	3.02	2.98
Abedi, et al. [23]	3.56	3.15
Mohammadi, et al. [34]	2.89	3.12
Labrado and Thapliyal [35]	2.485	2.84

Additionally, we compared the suggested designs in Table 4 to the best current designs in terms of Total energy dissipation (eV) and Average energy dissipation in order to better comprehend and compare circuits (eV). It is obvious that the current design is the most energy-efficient one.

4 Conclusion and future works

A new and emerging technology that plays a significant role in nanotechnology and has been researched for years is QCA technology. Considering the advantages of QCA, such as fast switching time, low power requirement, and high device density, it can be a good alternative. According to the cases mentioned in this article, this technology has been used to implement adder circuits. In fact, it creates an innovative architecture for a 1-bit QCA full adder. Then, applying this innovative full adder layout, a high-speed adder is developed as a 4-bit RCA. Our study effort is shown to provide fewer cells and smaller areas with realistic simulation results compared to the newly published collector architecture. The presented multi-layer architecture is significantly more durable than the conventional full adder.

The suggested full adder consists of 15 cells and achieves output generation in 0.5 clock cycles. It occupies an area of 0.01 μm^2 and features straightforward input and output connectivity. Additionally, the suggested four-bit QCA-based RCA incorporates 72 cells, covering an area of 0.11 μm^2. The RCA exhibits a delay of 1.75 clock cycles. In this study, QCADesigner-E assessed the total power dissipation of the QCA structure. These circuits have one of the best power consumption rates and are easily accessible to the inputs and outputs. In the future, high-speed adders can be designed that play an essential role in multi-layer designs and further improve computational performance. High-performance QCA circuits and an n-bit ripple carry adder can be created at the nanoscale using the given effective architectures. The suggested concept may therefore have a fundamental impact on the development of high-speed circuits as well as other forms of adders, such as complete subtractors and borrow ripple subtractors.

5 Conflict of Interest

The authors declare that they have no conflicts of interest.

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High-Gain Super Class-AB Bulk-driven Sub-threshold Low-Power CMOS Transconductance Amplifier for Biomedical Applications

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Abstract: This article describes a high-gain sub-threshold region-operated bulk-driven (BD) super class-AB power-efficient single-stage operational transconductance amplifier (OTA) with enhanced unity gain frequency (UGF). The proposed amplifier has a BD adaptively biased flipped voltage follower (FVF) differential input pair functioning in class-AB mode to raise the dynamic current and subsequently raise the UGF, and slew rate. Additionally, the core circuit of the proposed OTA employs partial positive feedback (PPF) to magnify the circuit's effective input transconductance and gain. Moreover, the circuit's overall gain is moved up by using three additional low-power current mirror loads, two of which are FVF current mirrors and one of which is a self-cascode current mirror, placed at the output. The proposed OTA circuit and its traditional counterpart are developed and simulated on the Cadence Spectre tool by exploiting UMC 0.18µm CMOS process technology, both circuits are biased with a minimal supply of 0.5V. The simulation results exhibit that the proposed circuit delivers 72.35dB open loop DC gain, 61.33º phase margin, and 18.706 kHz UGF with a consumption of only 62.82nW power. The performance outcomes ensured the suitability of the proposed OTA circuit for biomedical applications.

Keywords: Adaptive biasing, Bulk-driven OTA, FVF, Partial Positive Feedback, Self-cascode

Ojačevalnik prevodnosti CMOS z nizko močjo in velikim ojačenjem Super Class-AB za biomedicinske aplikacije

Izvleček: V članku je opisan enostopenjski operacijski transkonduktančni ojačevalnik (OTA) z visokim ojačenjem, ki deluje v podpražnem območju in je voden preko substrata (BD), ki je energetsko učinkovit in ima povečano frekvenco enotnega ojačenja (UGF). Predlagani ojačevalnik ima BD adaptivno pristranski diferencialni vhodni par z obrnjenim napetostnim sledilnikom (FVF), ki deluje v načinu razreda AB za povečanje dinamičnega toka in posledično povečanje UGF in hitrosti premikanja. Poleg tega jedro vezja predlaganega ojačevalnika OTA uporablja delno pozitivno povratno zvezo (PPF) za povečanje učinkovite vhodne transkonduktivnosti in ojačitve vezja. Poleg tega se celotno ojačenje vezja poveča z uporabo treh dodatnih tokovnih zrcal z nizko porabo, od katerih sta dve tokovni zrcali FVF, eno pa je tokovno zrcalo s samokaskodo, ki je nameščeno na izhodu. Predlagano vezje OTA in njegovo tradicionalno analogno vezje sta razvita in simulirana v orodju Cadence Spectre z uporabo 0,18µm CMOS procesne tehnologije UMC, obe vezji sta obremenjeni z minimalnim napajanjem 0,5 V. Rezultati simulacije kažejo, da predlagano vezje zagotavlja 72,35 dB DC ojačitve v odprti zanki, 61,33º fazno razliko in 18,706 kHz UGF s porabo samo 62,82 nW energije. Rezultati delovanja so zagotovili primernost predlaganega vezja OTA za biomedicinske aplikacije.

Ključne besede: prilagodljiva pred napetost, množično voden OTA, FVF, delna pozitivna povratna zanka, samo-kaskoda

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1 Introduction

Over the last few years, due to the advancement of CMOS technology, there is a continuous requirement for portable handset electronic devices like laptops, notepads, wireless sensor networks, mobile phones, biomedical implantable devices, etc in our everyday lives. The medical field is also drastically changing towards portability to continuously monitor patient health [1-5], this makes the attraction in the evaluation of ultra-low-voltage, low-power circuit designs for portable applications. Analog circuit designers are still rigorously working in this field and illustrating different design techniques for low voltage in the literature [6-8].

As the most fundamental block in an analog circuit, the OTA plays a pivotal role in analog front-end circuits used in biomedical data acquisition systems. Electromyograms (EMG), Electroencephalograms (EECG), Electrocardiograms (ECG), and other bio-potential signals are low voltage (amplitude in mV), and low-frequency signals with only a few kHz range. Rail-to-rail input/output swing, high DC gain, low noise, high linearity, and minimal power consumption are the basic requirements of the OTA used in biomedical applications [3]. Achieving these characteristics using a low power supply in deep submicron technologies is really a challenge. The conventional gate-driven technique is unsuitable for application under a 1V environment because of the threshold voltage constraint; OTA's restricted linear range and high power consumption are two of its biggest flaws. The weak-inversion design technique is well-suited to reduce power consumption, as the necessary drain-to-source voltage (V_{DS}) for strong inversion is 250 mV, which is decreased to about 78 mV [5, 9-11]. An alternate approach for operating rail-to-rail is to use the bulk-driven (BD) technique, which can prevail over the aforementioned linearity and threshold voltage restrictions. The bulk-driven technique in combination with the sub-threshold technique is preferable for biomedical applications, as the combined effect of both techniques increases linearity and reduces power consumption. Although the bulk-driven technique increases input common-mode range (ICMR), it reduces open-loop DC gain, and UGF and raises input-referred noise, since the gate transconductance (g_m) is (2.5–5) times higher than the bulk transconductance (g_{mb}) [12-16]. A number of bulk-driven OTA designs are described to improve the above-mentioned disadvantages of reduced bulk-transconductance under sub-1V environments in the literature [10-19], and also discussed in the references [20-22] in extremely low voltage conditions with very little power loss. Despite being the most power-efficient, single-stage amplifiers cannot deliver enough gain, in order to provide high gain, cascode techniques are used earlier. This approach is no longer used since it lowers output voltage swings. A self-cascode (SC), as described in references [5, 11, 14, 16], is an excellent approach to carry a strong DC gain and great output swing. It consists of two transistors but is handled as a single composite transistor. When SC loads are used, the output impedance roughly increases by a factor of 10, which is comparable to a gain improvement of about 20 dB. The composite SC loads don't require any extra bias sources to drive the cascode transistors and hence maximize the voltage gain. Some authors utilize partial positive feedback (PPF) techniques mentioned in [5, 12, 16, 17, 23-29] to improve the input core bulk- transconductance and hence improve the small-signal performances of bulk-driven OTAs, but the enhancement of the large-signal performances is not mentioned in these techniques.

This paper presents an improved bulk-driven low-power single-stage super class-AB OTA [12, 26, 30-32], operated in a sub-threshold region, which has been termed as super class-AB bulk-driven sub-threshold (SBDST) OTA in the whole paper. The proposed amplifier utilizes an adaptive bias technique in the input differential pair based on a BD-FVF [26, 31] functioning in the class-AB mode to improve the dynamic current and unity gain frequency. The partial positive feedback (PPF) technique has been exploited in the core circuit to improve the overall effective input transconductance and hence gain of the circuit. In addition to the improvement of input transconductance, output impedance also increases by using low power and high performance three current mirrors at the output, hence, the overall gain of the circuit further raises. The proposed SBDST OTA offers significant open loop DC gain, UGF, and slew-rate while exploiting minimal power, by utilizing the aforementioned techniques.

This paper is structured as follows: The study of conventional OTA is covered in Section 2, along with a thorough circuit description of both the proposed and conventional OTA. Section 3 discusses the proposed OTA's intricate circuit analysis. In Section 4, the simulation outcomes of conventional and proposed OTA including Monte Carlo, process corner analysis, and layout are covered. Section 5 compares the proposed OTA's performance to those of the other previously reported designs, and Section 6 finally brings to a conclusion of the paper.

2 Circuit Descriptions

2.1 Conventional Bulk-driven Sub-threshold (BDST) OTA

The conventional BDST OTA, in which the input core circuit is designed using bulk-input PMOS transistors PI_{1a}-

PI_{1b}, is depicted in Fig. 1. The differential input transistor pair working in the sub-threshold region is biased by using transistor P_B; the drain current (I_{DS}) of a transistor operating in sub-threshold is expressed as [11]:

$$I_{DS} = I_s \left(\frac{W}{L}\right) e^{\left(q\frac{V_{GS}-V_{Tn}}{nKT}\right)} \left[1 - e^{\left(q\frac{-V_{DS}}{KT}\right)}\right] \quad (1)$$

where I_S and K are the characteristic current of the sub-threshold and Boltzmann constant, n is the slope of the curve in the sub-threshold region, T is the absolute temperature and q is the charge of electron respectively.

The transistors are in saturation in the sub-threshold region if $V_{DS} \geq 3V_T$, where ($V_T = KT/q$) is the thermal equivalent voltage and its value at 27° is 26 mV.

Applying the condition $V_{DS} \geq 3V_T$ in (1), then the term $e^{\left(q\frac{-V_{DS}}{KT}\right)} \ll 1$, hence the equation (1) simplifies to

$$I_{DS} = I_s \left(\frac{W}{L}\right) e^{\left(q\frac{V_{GS}-V_{Tn}}{nKT}\right)} \quad (2)$$

The output of differential input pair consists of NMOS transistor pair ($N_{1a\text{-}3a} - N_{1b\text{-}3b}$), form the non-linear current mirrors with a current transfer ratio $K_1 = 2$. These current mirrors known as the adaptive loads [26], are loads of the input transistor pair. The output of the adaptive loads is routed to the summing stage, which is at the circuit's output, to raise the output impedance. The summing stage of the conventional OTA uses PMOS transistors ($P_{2a\text{-}2b} - P_{3a\text{-}3b}$) as a current mirror to boost the largely dc gain of the circuit. The conventional BDST OTA's effective transconductance is provided by:

$$G_{m,BDST} = K_1 . g_{mb1,a/b} \quad (3)$$

where g_{mb1} represents the bulk-transconductance of input transistors.

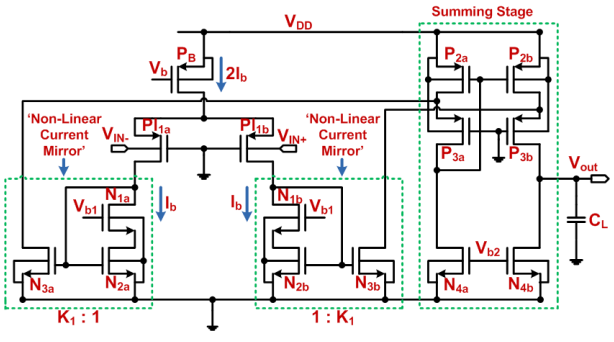

Figure 1: Conventional Bulk-driven sub-threshold (BDST) OTA

The output impedance R_{out} of the BDST OTA is provided as:

$$R_{out} = [r_{o4,bN} || (r_{o3,bP} + (r_{o3,bN} || r_{o2,bP}))] \quad (4)$$

since, $r_{o3,bP} >> (r_{o3,bN} || r_{o2,bP})$

therefore, equation (4) is simplified as:

$$R_{out} = (r_{o4,bN} || r_{o3,bP}) \quad (5)$$

Effective transconductance and the circuit's output impedance combine to provide the open loop dc gain (A_v), which is expressed as:

$$A_{V,BDST} = G_{m,BDST} . R_{out}$$
$$A_{V,BDST} = K_1 . g_{mb1,a/b} . (r_{o4,bN} || r_{o3,bP}) \quad (6)$$

The main problem of conventional BDST OTA is a very low open-loop gain, it is only about 32 dB. A non-linear current mirror is employed here to increase the amplifier's slew rate and unity gain frequency (UGF), which can be evaluated with capacitive load C_L by the following equations:

$$UGF_{BDST} = \frac{K_1 . g_{mb1,a/b}}{2\pi C_L} \quad (7)$$

$$SR_{BDST} = \frac{2.K_1 . I_B}{C_L} \quad (8)$$

The values of UGF and slew rate of the conventional amplifier are 1.637 kHz, and 0.92V/ms respectively, which are quite low. Therefore, some structural change is required in the amplifier to get better the whole performance of the conventional BDST OTA concerning open-loop gain, slew rate, UGF, etc.

2.2 Proposed SBDST OTA

We proposed the super class-AB bulk-driven sub-threshold (SBDST) OTA, which is depicted in Fig. 2, to enhance the performance of conventional BDST OTA. Its input core makes use of two identical adaptively biased BD-FVF pair, eliminating the bias current source of the conventional circuit, which is supplied by P_B in Fig. 1.

The best possible dimensions of transistors are selected to function the proposed SBDST in a sub-threshold region so that the circuit can obtain low power operation i,e., below 100nW. To extend the input common-mode range (0 to V_{DD}) of the circuit bulk-driven differential pair is used in the input stage, however, gate transconductance (g_m) is (2.5–5) times more than the bulk transconductance (g_{mb}) [12]. Consequently, the

circuit's effective transconductance decreases, and hence, the gain and UGF of the circuit are also considerably low. To overcome these limitations an adaptive biased super class-AB [26, 31, 32] is incorporated into the input core. The BD-FVF pair at the input consists of bulk-driven transistors PI_{1a}-PI_{1b}, diode-connected transistors PI_{3a}-PI_{3b} connected in negative feedback [31, 32], and the current source made by transistors NI_{5a}-NI_{5b}. The input core of the SBDST is made up of adaptively biased input differential pair PI_{2a}-PI_{2b} and adaptive loads. Non-linear current mirrors ($N_{1a\text{-}3a}$ - $N_{1b\text{-}3b}$) with a current ratio of $1{:}K_1$ are called adaptive loads. The source terminal of FVF pair is the output node that has very low impedance, given by $\frac{1}{g_{m3a}\, g_{m1a} r_{o1a}}$. The FVF is capable to source a significant amount of current even greater than the bias current I_b on the variation of differential input voltage because of the low impedance at the output node. Hence, the FVF pair in combination with the adaptive biased differential pair makes the proposed OTA function in class-AB. This combination eliminates the limitations of traditional BDST OTA.

Differential input signals V_{in-} and V_{in+} are applied across the bulk terminal of transistors PI_{1a}-PI_{1b} as well as to the bulk terminal of adaptive biased differential pair PI_{2a}-PI_{2b}. Due to the voltage follower action of FVF, the transistor PI_{1a} source terminal is also V_{in-}. This terminal is named C as shown in Fig.2 and is also connected to the source terminal of the transistor PI_{2a}, hence, the total signal voltage that appears across the transistor PI_{2a} is $V_{BS} = [V_{in+} - V_{in-}] = [V_{in+} - (-V_{in+})] = 2\,V_{in+}$. Similarly, the V_{BS} of the transistor PI_{2b} is $2V_{in-}$. Therefore, the proposed SBDST OTA's effective transconductance is twice as much as that of the traditional OTA and is equal to $2g_{mb1,a/b}$.

Since the transconductance of the SBDST increases, so the gain and UGF are also increase. To further enhance the transconductance, and gain, the PPF technique has been introduced using transistors N_{4a} and N_{4b} at adaptive load ends of the input core, shown in Fig. 2 inside the box colored green. The PPF loop increases the overall input transconductance but with a little loss of phase margin (PM), as it generates a non-dominate pole at node *E* of the SBDST OTA. Therefore, a small compensation capacitor C_C is used between the drain of NI_{5b} and the output node.

In addition to the improvement of transconductance, output impedance is also enhanced using three current mirrors at the output of the circuit. Among these mirrors, two are highly-effective FVF current mirrors [5] with a current gain factor of 1.25, and one is a self-cascode current mirror. In composite SC structure, the aspect ratio of the cascode transistor and the transistor connected to the supply is set to 20, to operate in saturation in the sub-threshold region [11, 16]. Hence, by raising the input stage's transconductance and the output stage's output impedance, the proposed SBDST OTA's overall performance is enhanced.

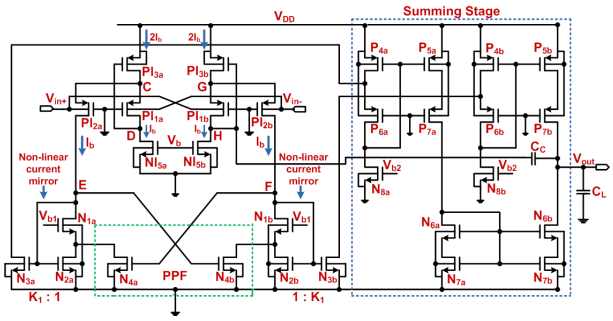

Figure 2: Proposed SBDST OTA

3 Explanation of the proposed SBDST OTA

This section describes the SBDST OTA's overall transconductance, voltage gain, UGF, and stability.

3.1 Effective transconductance and UGF

The half sub-circuit of the input core of SBDST and its small signal AC equivalent circuit are depicted in Fig. 3a and b.

The input signals V_{in-} and V_{in+} are applied to the bulk terminal of the transistors PI_{1a} and PI_{2a} respectively, assuming the voltage at their source terminals is V_C, and

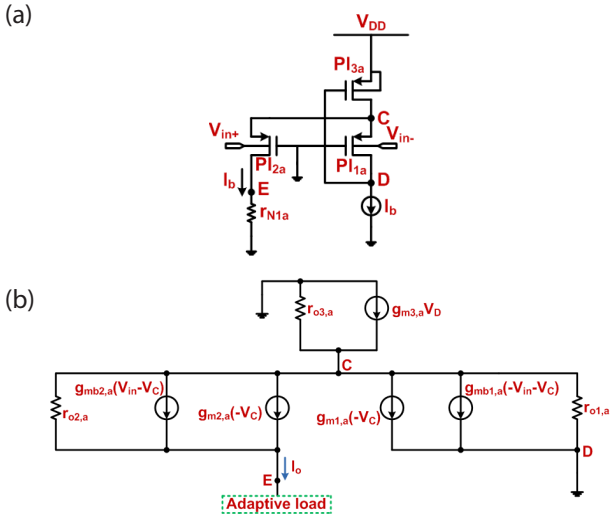

Figure 3: (a) Input core's half circuit of SBDST OTA, (b) half circuit small signal equivalent model

the transistor PI_{3a} gate voltage is V_D. The drain terminal of PI_{1a} is also connected to point D, so its drain voltage is also V_D. A constant DC source I_b made by transistors NI_{5a}-NI_{5b} biases the transistor PI_{1a}. As a result, zero AC small signal current passes through the input transistor PI_{1a} [31].

And all the AC signal current of PI_{3a} is the output AC small signal current I_o which flows through the transistor PI_{2a} [12, 26,31,32]. The effective overall transconductance of the proposed OTA is calculated from the following equations,

The small signal current through transistor PI_{1a} at node *D* is given by:

$$g_{m1,a}\left(-V_C\right)+g_{mb1,a}\left(-V_{in}-V_C\right)+\frac{\left(V_C-V_D\right)}{r_{o1,a}}=0 \quad (9)$$

and the output current I_o contributed by PI_{2a} is expressed as:

$$I_o=g_{m2,a}\left(-V_C\right)+g_{mb2,a}\left(V_{in}-V_C\right)+\frac{\left(V_C-V_E\right)}{r_{o2,a}} \quad (10)$$

Neglecting the output resistance term from both equations since its value is very high.

So, Eq. (9) can be approximated as:

$$g_{m1,a}\left(V_C\right)+g_{mb1,a}\left(V_{in}+V_C\right)=0 \quad (11)$$

$$\Rightarrow \left(g_{m1,a}+g_{mb1,a}\right)V_C=-g_{mb1,a}V_{in} \quad (12)$$

$$\Rightarrow \quad V_C=\frac{-g_{mb1,a}V_{in}}{\left(g_{m1,a}+g_{mb1,a}\right)} \quad (13)$$

Eq. (10) can be written as:

$$I_o=g_{mb2,a}V_{in}-V_C\left(g_{m2,a}+g_{mb2,a}\right) \quad (14)$$

Putting the value of V_C from Eq. (13) to Eq. (14) and solving it in terms of V_{in}, then the equation becomes:

$$I_o=g_{mb2,a}V_{in}+\frac{g_{mb1,a}V_{in}}{\left(g_{m1,a}+g_{mb1,a}\right)}\left(g_{m2,a}+g_{mb2,a}\right) \quad (15)$$

Since the transistors PI_{1a} and PI_{2a} are identical, therefore

$$g_{m1,a}=g_{m2,a} \text{ and } g_{mb1,a}=g_{mb2,a} \quad (16)$$

Putting the above relations into Eq. (15), then the value of I_o can be simplified as:

$$I_o=2g_{mb1,a}V_{in} \quad (17)$$

As the circuit is symmetry, therefore the input core transconductance is given as:

$$\mathrm{G_{m,\,input\ core}}=\frac{\mathrm{I_o}}{\mathrm{V_{in}}}=2\mathrm{g_{mb1}} \quad (18)$$

Considering the current gain $K_1 = 2$ of the non-linear current mirror together with the partial positive feedback technique employing the transistors N_{4a}, and N_{4b} in the input core, the effective overall transconductance of the proposed SBDST OTA is provided by:

$$\mathrm{G_{m,\,effective}}\big|_{\mathrm{SBDST}}=\mathrm{K_1}\frac{2\mathrm{g_{mb1}}}{(1-\alpha)} \quad (19)$$

where K1 and α are the aspect ratios of the transistors given by $\mathrm{K_1}=\frac{\mathrm{g_{m3,\,N}}}{\mathrm{g_{m2,\,N}}}$ and $\alpha=\frac{\mathrm{g_{m4,\,N}}}{\mathrm{g_{m2,\,N}}}$.

The UGF of the SBDST OTA is given by:

$$\mathrm{UGF}=\frac{\mathrm{G_{m,\,effective}}\big|_{\mathrm{SBDST}}}{2\pi\mathrm{C_L}}=\frac{\mathrm{K_1}}{(1-\alpha)}\frac{2\mathrm{g_{mb1}}}{2\pi\mathrm{C_L}} \quad (20)$$

Due to its enhanced effective transconductance value, the proposed OTA provides a significantly higher UGF than the traditional BDST OTA, as shown by expression (20).

3.2 Voltage gain

The SBDST OTA's open loop voltage gain is obtained by multiplying the circuit's output impedance and effective transconductance. The entire circuit's output impedance at the output node is provided by:

$$R_{out}=(g_{m7,bP}r_{o7,bP}r_{o5,bP})\|(g_{m6,bN}r_{o6,bN}r_{o7,bN}) \quad (21)$$

Hence, the proposed SBDST OTA's overall voltage gain is given by:

$$A_V\big|_{SBDST}=G_{m,effective}\big|_{SBDST}R_{out}$$

$$\Rightarrow A_V\big|_{SBDST}=\mathrm{K_1}\frac{2\mathrm{g_{mb1}}}{(1-\alpha)}[(g_{m7,bP}r_{o7,bP}r_{o5,bP})\|(g_{m6,bN}r_{o6,bN}r_{o7,bN})] \quad (22)$$

3.3 Stability analysis

The proposed SBDST OTA introduces a dominant pole (p_1) at the output node owing to its capacitive load and output impedance hence, its frequency is not influenced by the PPF loop and is given as:

$$\mathrm{p_1}=\frac{1}{\mathrm{R_{out}}\left(\mathrm{C_C}+\mathrm{C_L}\right)} \quad (23)$$

where C_C is the small compensation capacitor and C_L is the load capacitance.

The PPF technique employed in the input core causes the non-dominant pole (P_2) at the drain terminal of $N_{2,a/b}$ to shifts towards a lower value, and its value given in [12], is expressed as:

$$p_2 = \frac{\left(g_{m2,N} - g_{m4,N}\right)}{C_P} \quad (24)$$

where C_p indicates the parasitic capacitance at the above-mentioned drain terminal node. This node has a higher impedance due to PPF action. The lower secondary pole value in (24) limits the maximum possible UGF. To ensure a stable phase margin a small compensation capacitor C_C is placed between the drain of NI_{5b} and the high-impedance output node.

4 Simulation results

Using 180nm CMOS process technology, the traditional BDST and proposed SBDST OTAs are driven by only 0.5V supply for a load capacitor of 15pF and are simulated in the Cadence Virtuoso simulator. The bias current I_b of the BD-FVF pair in SBDST OTA is fixed to 10nA and the total stand-by-current under the sub-threshold region of operation is 124nA while that of conventional OTA is 100nA, and the reference temperature for both is 27°C. The bias current used for biasing the high-performance FVF current mirror is 1.2nA. In the design, all the MOSFETs have an optimum value of aspect ratio to lower the influence of channel length modulation and input referred noise of the circuit. Additionally, the bias voltage V_{b1} has been chosen properly to bias the transistor $N_{2,a/b}$ in the triode region, so that the combination of transistors ($N_{1a\text{-}3a} - N_{1b\text{-}3b}$) works as a non-linear mirror.

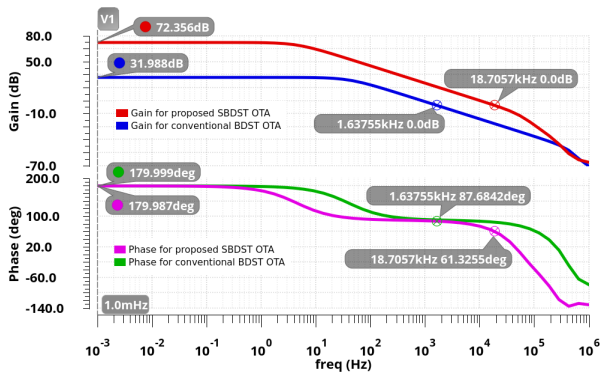

Figure 4: Simulated AC plot of BDST OTA and SBDST OTA

Figure 4 shows the AC responses of conventional BDST OTA and proposed SBDST OTA, the simulation outcomes demonstrate that the open loop DC gain, UGF, and phase margin of the proposed SBDST OTA are 72.356 dB, 18.7057 kHz, and 61.3255° respectively. This result of the proposed OTA exposes that the improvement in DC gain is 2.26 times and in UGF is 11.42 times than the conventional circuit, with a little loss of phase margin. A compensation capacitor of value, C_C = 0.4pF is used in the SBDST OTA, to increase its phase margin above 60°.

The overall effective input core transconductance is exposed in Fig. 5, the proposed SBDST OTA accomplishes a significantly greater effective input core transconductance of 1.76μS compared to 158.5nS of conventional bulk-driven OTA.

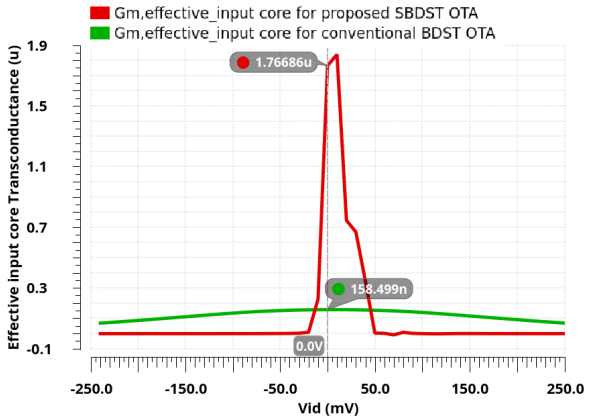

Figure 5: Effective input core transconductance of BDST OTA and SBDST OTA

One of the most crucial factors of an OTA is noise, it is an undesired signal that frequently combines with the desired signal as a result of fluctuations in the power supply or component mismatches, producing unwanted output. In addition to this, the thermal, as well as flicker noise of MOS transistors itself, adds to the overall noise density. Since the range of biosignals is 10mHz ≤ f_{bio} ≤ 1kHz, hence the flicker noise predominates more in bi-

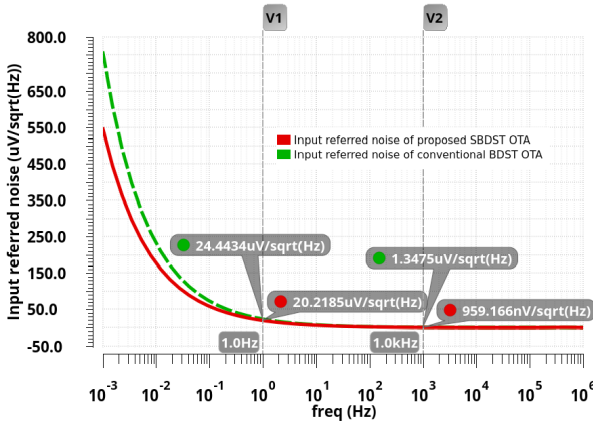

Figure 6: Plot of input referred noise voltage of BDST OTA and SBDST OTA

omedical applications. So, the design of the OTA circuit must assure minimum input-referred output noise for biomedical applications. Figure 6 highlights the input-referred noise produced at the input pair terminals of the proposed and conventional OTA, the SBDST OTA and BDST OTA are found to have input-referred noise (IRN) values of 0.959 μV/√Hz and 1.347 μV/√Hz, respectively, at 1 kHz. Its value is less in the proposed SBDST OTA due to the enhancement in the overall effective transconductance of the input pair.

The PSRR ± and CMRR values must be very large to reject unwanted signals which are generated by variations in the power supply, these unwanted signals are common to both inputs. Figure 7 shows the result of CMRR and PSRR ± of the SBDST OTA, it is found that the proposed SBDST OTA at 1 mHz provides a high CMRR, PSRR+, and PSRR– of values 161.48 dB, 86.17 dB, and 69.22 dB respectively.

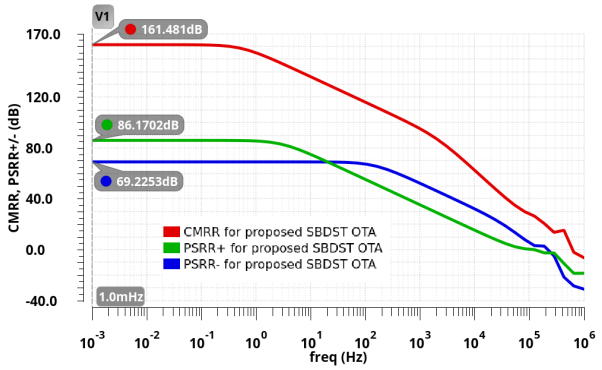

Figure 7: CMRR, PSRR (+/–) of proposed SBDST OTA

Figure 8 shows a unity gain closed loop structure of the suggested SBDST OTAs by shorting its inverting input to output to achieve the transient response of large-signals. The output response is highlighted in Fig. 9 for a 15pF capacitive load when a step input signal of 0.5V peak-to-peak voltage (V_{pp}) at 250Hz frequency is applied at the non-inverting input of OTA. It is found that the value of an average slew rate of the SBDST OTA is 2.07 V/ms.

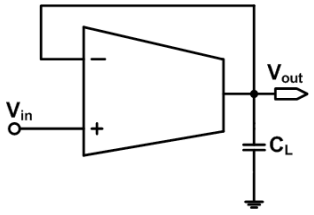

Figure 8: Unity gain configuration of the SBDST OTA

Sinusoidal transient response is evaluated by applying two sinusoidal input signals of $0.5V_{pp}$ and $0.4V_{pp}$ with common-mode voltages (V_{cm}) of 0.25V and 0.2V, respectively on the non-inverting input terminal in Fig. 8 at 250 Hz frequency. The simulation's outputs are revealed in Fig. 10(a) and (b), the result displays that the proposed OTA provides (12.55 mV–491.3 mV) and (12.56 mV–399.37 mV) of output signal swing respectively. The output voltage swing in response to a sinusoidal transient is nearly rail-to-rail.

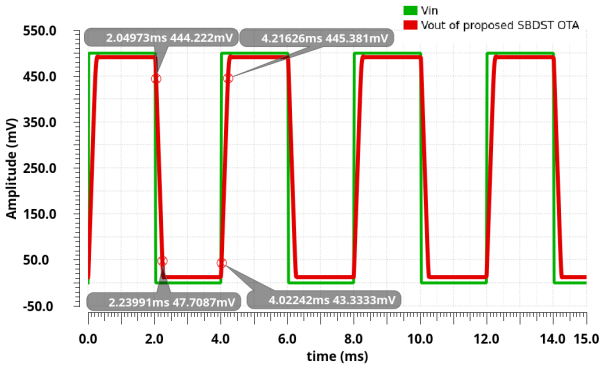

Figure 9: Large-signal pulse response to 0.5Vpp at 250 Hz square wave for proposed SBDST OTA

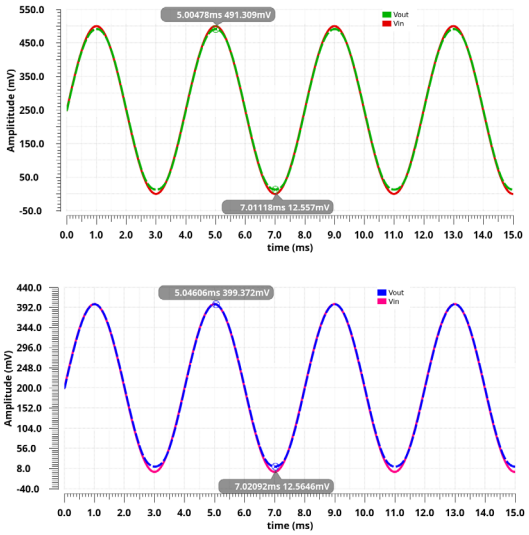

Figure 10: Sinusoidal transient response of the proposed SBDST OTA for (a) $V_{in,pp}$ = 0.5V with V_{cm} = 0.25V, (b) $V_{in,pp}$ = 0.4V with V_{cm} = 0.2V

The proposed OTA's input common-mode range (ICMR) is evaluated by performing its DC sweep analysis in a non-inverting voltage buffer configuration with a 15pF capacitive load, and the simulation's output is exposed in Fig. 11(a), and the variation of error voltage (V_{out}–V_{in}) over the whole input (0 to V_{DD}) voltage range is displayed in Fig. 11(b). It has been found that the error voltage generated at 0V input is 12.63 mV, while at 0.5V input is 8.8 mV only. Thus, it is ensured from the DC sweep results revealed in Fig. 11(a) and (b), that the proposed SBDST OTA is linear over a wide range of ICMR.

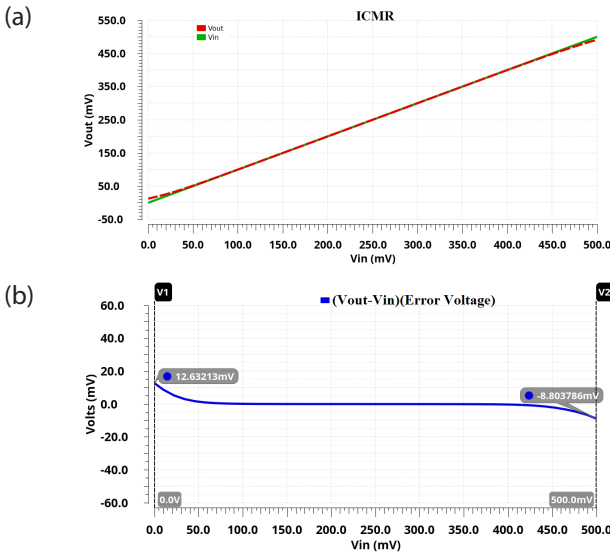

Figure 11: (a) DC sweep for ICMR of the SBDST OTA, (b) Error voltage (V_{out} - V_{in}) in DC sweep

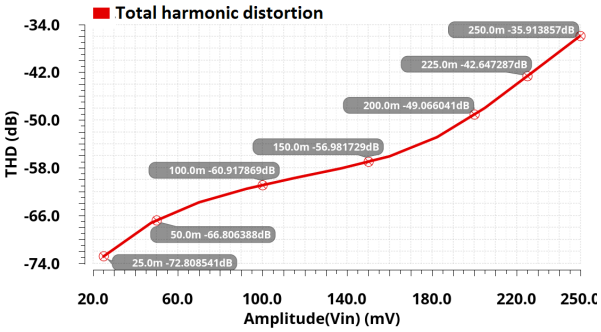

Figure 12: Plot of THD against amplitude for SBDST OTA

A 250 Hz sine wave input signal with varying peak-to-peak amplitudes from 50mV to 500mV has been used to assess the nonlinearity of the SBDST OTA in a unit gain configuration. The simulation result is highlighted in figure 12. At 200 mV (pp), the total harmonic distortion is -60.91dB, and up to 466 mV(pp) amplitude of the input sine wave, the SBDST OTA ensures that the THD value is less than -40dB.

The robustness of the OTA is determined by the deviation of its performance parameters from process and mismatch. For 300 samples, Monte Carlo simulations are utilized to assess the proposed SBDST OTA's robustness. The statistical data of such analysis is shown in Fig. 13 in the form of a histogram.

In addition to this, Monte Carlo simulations of the whole parameters of the SBDST OTA have been tabularized in Table 1. Table 1's outcomes demonstrate that the proposed OTA delivers low standard deviation (SD) for all the performance parameters and hence is insensitive to process variations.

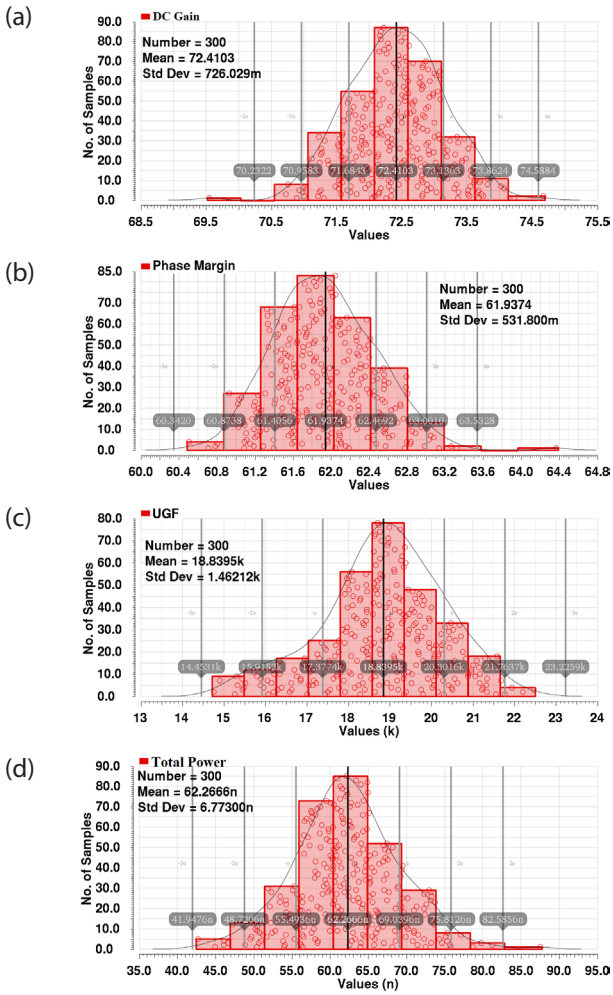

Figure 13: Simulation results of Monte Carlo iteration of (a) DC gain, (b) PM, (c) UGF, (d) total power consumption for 300 samples

Table 1: Performance result of proposed SBDST OTA under Monte Carlo simulation using 300 samples

Parameters	Mean (μ)	SD (σ)
Open loop DC gain (dB)	72.41	726m
Phase margin (degree)	61.94	531.8m
UGF (kHz)	18.84	1.462k
CMRR (dB) @ 1mHz	151.7	10.66
PSRR+ (dB) @ 1mHz	86.31	1.399
PSRR– (dB) @ 1mHz	69.28	883.6m
SR(av) (V/ms)	2.078	140.1m
IRN (μV/Hz$^{0.5}$) at 1kHz	0.96	6.999n
Total current (nA)	124.5	13.55n
Total Power (nW)	62.27	6.773n

Integrated circuits (ICs) must be so designed by manufacturers that after fabrication, PVT (process, voltage, and temperature) fluctuations have no effect on ICs. Deviations in manufacturing conditions like dopant concentrations, temperature, pressure, and variations in the semiconductor fabrication process cause "process

variation". The other key factors for process variation are variations in metal thickness, oxide thickness, UV light wavelength, faults in the manufacturing process, and variations in transistors characteristics [12]. There may be a chance of voltage fluctuation also in some circumstances, so the proposed OTA's simulation results should also be verified by varying the supply voltage.

Figure 14 shows the five process corners (TT, FF, SS, FNSP, and SNFP) effects at 27 ºC on the gain and phase margin of the proposed SBDST circuit. The SS corner has the largest DC gain, measuring 76 dB, and the FNSP corner has the lowest DC gain, measuring 65.59 dB. To check the sensitivity of the proposed OTA against the variations of PVT, corner analysis for five different corners at temperatures (–14 ºC, 27 ºC, and 60 ºC) has been done, and the performance of OTA has been also verified by varying ±10% supply voltage. The simulation results of all the performance parameters against fluctuations of PVT are tabulated in Table 2 and Table 3.

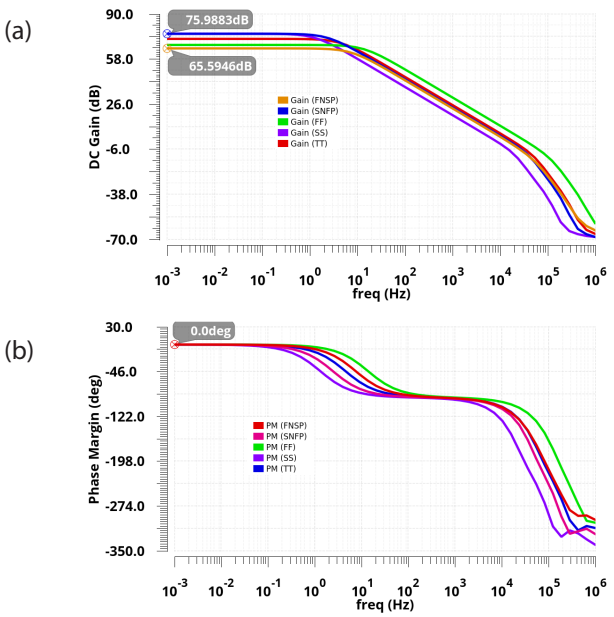

Figure 14: Process corners effect on DC gain and phase margin at room temperature

Table 2: Simulation results on the variation of supply voltage

Parameters	VDD – 10%	VDD + 10%
Open loop DC gain (dB)	63.33	77.64
Phase margin (degree)	68.43	56.83
UGF (kHz)	7.4	27.46
CMRR (dB) @ 1mHz	126.88	115.1
PSRR+ (dB) @ 1mHz	71.13	94.4
PSRR– (dB) @ 1mHz	61.66	73.28
IRN (μV/Hz$^{0.5}$) at 1kHz	0.96	0.94
Total current (nA)	102.9	144
Total Power (nW)	46.3	79.2

Figure 15 depicts the layout of the single-stage SBDST OTA. The proposed OTA takes up (76 x 81) μm2 area, including the area of the compensation capacitor, and the post-layout outcome of the AC response of the SBDST OTA is exposed in Fig. 16. The simulation outcomes of post-layout express that the open loop DC gain, UGF, and phase margin are 72.281 dB, 18.329 kHz, and 61.635º respectively. The results of pre-layout and post-layout AC responses expose that there is a high degree of proximity. This proximity supports the usability and design of this SBDST OTA.

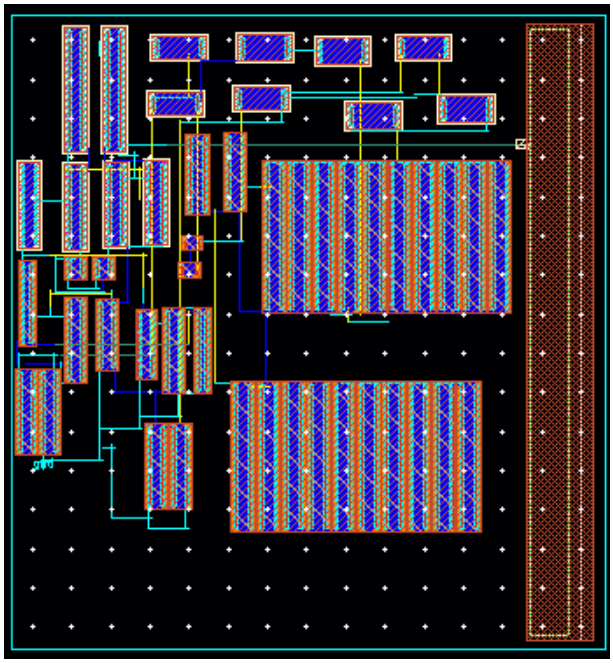

Figure 15: Proposed SBDST OTA's layout

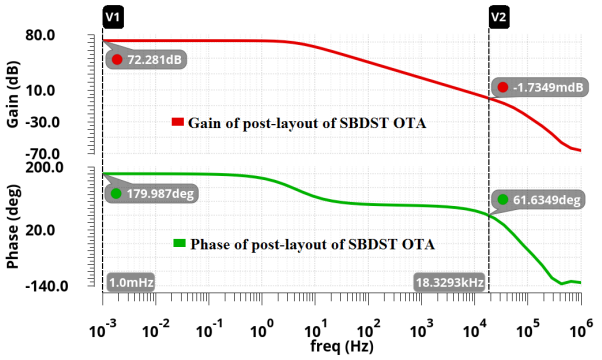

Figure 16: Post-layout AC plot of BDST OTA

Table 3: Simulation results of the performance of SBDST OTA on variations of process and temperature

Parameters	Different corners at temperature –14 °C				
	TT	FF	SS	SNFP	FNSP
Open loop DC gain (dB)	79.41	76.17	80.68	79.08	73.63
Phase margin (degree)	53.37	54.04	53.29	58.79	54.1
UGF (kHz)	9.08	23.57	2.68	5.21	10.16
CMRR (dB) @ 1mHz	135.18	131.26	149.96	109.27	133.98
PSRR+ (dB) @ 1mHz	98.44	91.51	102.45	91.49	85.1
PSRR– (dB) @ 1mHz	73.09	70.34	74.68	72.24	68.85
SR(av) (V/ms)	1.22	2.5	0.58	1.58	0.84
IRN (μV/Hz$^{0.5}$) at 1kHz	0.93	0.81	1.31	1.03	0.88
Total Power (nW)	18.14	58.99	4.83	10.85	29.58
Parameters	Different corners at temperature 27 °C				
	TT	FF	SS	SNFP	FNSP
Open loop DC gain (dB)	72.36	68.06	76	75.99	65.59
Phase margin (degree)	61.96	65.42	59.69	61.28	68.07
UGF (kHz)	19.11	34.77	8.47	15.41	14.39
CMRR (dB) @ 1mHz	161.49	142.19	131.91	107.02	136.82
PSRR+ (dB) @ 1mHz	86.17	79.86	93.27	89.12	74.44
PSRR– (dB) @ 1mHz	69.21	65.56	72.41	71.72	63.69
SR(av) (V/ms)	2.06	3.66	1.12	2.91	1.41
IRN (μV/Hz$^{0.5}$) at 1kHz	0.95	0.92	1.08	0.94	0.96
Total Power (nW)	62.81	162.98	21.79	42.62	88.66
Parameters	Different corners at temperature 60 °C				
	TT	FF	SS	SNFP	FNSP
Open loop DC gain (dB)	65.35	60.48	69.72	70.18	14.08
Phase margin (degree)	69.83	73.96	65.86	65.74	102.17
UGF (kHz)	23.15	33.87	13.87	25.77	0.093
CMRR (dB) @ 1mHz	133.58	139.19	124.83	102.66	137.38
PSRR+ (dB) @ 1mHz	76.11	70.17	82.49	81.76	19.35
PSRR– (dB) @ 1mHz	63.69	59.27	67.59	67.47	14.08
SR(av) (V/ms)	2.74	4.32	1.66	3.9	1.8
IRN (μV/Hz$^{0.5}$) at 1kHz	1.03	1	1.09	0.96	1.21
Total Power (nW)	137.94	316.13	55.62	102.48	175.65

5 Performance comparison and discussions

Table 4 lists the performance parameters of proposed OTAs. To verify the overall performance of OTA in terms of the responses to small- and large-signals, two popular figures of Merit (FOM_{Sm}, FOM_{La}) are specified in [22, 27, 28], and are given in equations (25) and (26) respectively.

$$FOM_{Sm} = \frac{UGF\left(MHz\right)\times C_L\left(pF\right)}{I_T\left(\mu A\right)} \tag{25}$$

$$FOM_{La} = \frac{SR_{av}\left(V/\mu s\right)\times C_L\left(pF\right)}{I_T\left(\mu A\right)} \tag{26}$$

The proposed SBDST OTA performance parameters are compared with some of the other recent BD OTAs and reported in Table 5. According to Table 5, the proposed SBDST OTA has offered the largest DC gain, PSRR+/– among others and also has maximum CMRR except that of [19] only. The proposed SBDST OTA's large-signal response (FOM_{La}) is comparable to only [14] in comparison to the other remaining OTAs given in Table 5, but it has provided the highest small-signal response (FOM_{Sm}) as compared to other reported OTAs, with the exception of [20].

Table 4: Proposed SBDST OTA performance parameters

Parameters	SBDST OTA
Power supply (V)	0.5
Load capacitance (pF)	15
Technology	0.18µm
DC gain	72.35
Phase margin (°)	61.33
UGF (kHz)	18.7
CMRR (dB) @ 1mHz	161.48
PSRR+ (dB) @ 1mHz	86.17
PSRR– (dB) @ 1mHz	69.22
IRN @ 1kHz(µV/Hz$^{0.5}$)	0.95
SR average (V/ms)	2.07
Total current (nA)	125.64
Total power (nW)	62.82
FOM_{Sm}	2.23
FOM_{La}	0.247

6 Conclusions

This article's work presents an enhanced bulk-driven single-stage architecture of an OTA functioning in the weak-inversion region, powered by 0.5V of power supply. The proposed architecture of the amplifier employs a BD-FVF that is based on an adaptively biased differential input pair operating in the class-AB mode to improve dynamic current and unity gain frequency. Additionally, it employs a partial positive feedback technique in the differential pair's core to increase the gain of the circuit. Further, the gain of the circuit is increased by using a low-power, high-performance current mirror load based on FVF at the amplifier's output. The suggested OTA's simulation results show that the amplifier uses just 62.82nW of power and has a DC gain of 72.35 dB, a phase margin of 61.32°, and a UGF of 18.7 kHz. For a 250 Hz input sine wave of 200 mV (pp), the SBDST OTA in its unity gain configuration offers -60.91 dB total harmonic distortion. The obtained outcomes of the amplifier ensured that the proposed SBDST OTA is appropriate for biomedical signal processing, audio signal processing, and low-frequency sensors.

7 Conflict of Interest

The authors declare that they have no conflicts of interest.

Table 5: Proposed SBDST OTA and previously reported BD OTAs performance differences at 0.18µm technology

Parameters	[14] 2015	[11] 2017	[15] 2017	[16] OTA_1 2018	[16] OTA_2 2018	[17] 2018	[19] 2019	[29] 2021	[20] 2022	This-Work 2023
C_L(pF)	15	15	12	15	15	50	15	50	30	15
Power supply (V)	0.5	0.5	0.6	0.6	0.6	0.8	0.6	0.7	0.4	0.5
Phase margin (°)	68.9	54	62.45	93	78.41	87	74	89.07	60	61.33
(DC gain)[a] (dB)	67.8	70.4	61.5	61.9	60.76	44.3	71@ 0.1Hz	71.35	60	72.35
UGF (MHz)	0.003	0.009	0.03015	0.0024	0.00773	1.45	0.0182	0.00107	0.007	0.0187
CMRR[a] (dB)	–	106 @ 1Hz	–	122 @ 1Hz	119@ 1Hz	–	201.8@ 10Hz	138.5	85	161.48
PSRR[a]+ (dB)	–	70@ 1Hz	67.9	62.8@ 1Hz	61.8 @ 1Hz	–	77.4@ 10Hz	77.08	76	86.17
PSRR[a]– (dB)	–	–	–	–	–	–	–	60.23	–	69.22
IRN[b] @ (µV/HZ0.5)	0.56	2.53	6.25 @ 0.1Hz	2.454	2.97	–	0.25@ 0.1Hz	0.779	–	0.95
SR average (V/µs)	0.84/ 0.59[c]	0.967	0.0553	1.15	1.404	3.5	0.0066	0.00157	0.079	0.00207
Total current (nA)	52	125.5	275	50.63	115	62,000	240	200	60	125.64
Total power(nW)	26	64	165	30.38	69	49,600	144	140	24	62.82
FOM_{Sm}	0.94	1.11	1.31	0.711	1.008	1.17	1.13	0.27	3.5	2.23
FOM_{La}	0.24	116	3.01	340.7	183.13	2.82	0.412	0.39	39.5	0.247
Area (µm^2)	52000	–	–	6620	7406	–	16,000	–	7900	6,156

a: at 1mHz, b: at 1kHz, c: V/ms

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An Energy-efficient and Accuracy-adjustable bfloat16 Multiplier

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Abstract: The approximate multipliers have been extensively used in neural network inference, but due to the relatively large error, they have yet to be successfully deployed in neural network learning. Recently, the bfloat16 format has emerged as a viable number representation for neural networks. This paper proposes a novel approximate bfloat16 multiplier with on-the-fly adjustable accuracy for energy-efficient learning in deep neural networks. The size of the proposed multiplier is only 62% of the size of the exact bfloat16 multiplier. Furthermore, its energy footprint is up to five times smaller than the footprint of the exact bfloat16 multiplier. We demonstrate the advantages of the proposed multiplier in deep neural network learning, where we successfully train the ResNet-20 network on the CIFAR-10 dataset from scratch.

Keywords: approximate computing; deep neural networks; energy-efficient processing; bfloat16 multiplier

Energijsko učinkovit približni množilnik v zapisu bfloat16 z nastavljivo natančnostjo

Izvleček: Približni množilniki so se izkazali za zelo primerne pri sklepanju z nevronskimi mrežami, vendar zaradi relativno velike napake še niso bili uspešno uporabljeni pri učenju globokih nevronskih mrež. Pred kratkim se je za predstavitev realnih števil v nevronskih mrežah začel uveljavljati zapis bfloat16. V članku predlagamo nov približni množilnik v zapisu bfloat16 s sprotno nastavljivo natančnostjo za energetsko učinkovito učenje v globokih nevronskih mrežah. Velikost predlaganega množilnika je samo 62 % velikosti natančnega množilnika v zapisu bfloat16. Poleg tega je njegov energijski odtis do petkrat manjši od odtisa natančnega množilnika bfloat16. Uporabnost predlaganega množilnika predstavimo na primeru učenja globokih nevronskih mrež, kjer uspešno naučimo mrežo ResNet-20 na naboru podatkov CIFAR-10.

Ključne besede: približno računanje; globoke nevronske mreže; energijsko učinkovito računanje; množilnik v zapisu bfloat16

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1 Introduction

Neural network capability of learning from data and generalising the gained knowledge makes them a very popular modelling tool in various application fields. The popularity growth in the last years can be attributed to the deep models, which pose considerable requirements to the processing hardware. Thus, new hardware solutions are being developed continuously to keep the processing hardware on par with the computing demands.

Approximate computing has emerged as a popular strategy for area- and energy-efficient circuit design, where the challenge is to achieve the best trade-off between design efficiency and accuracy. Efficient designs come at the cost of accuracy reduction and vice versa. Nevertheless, approximate computing perfectly fits neural networks, which, to a certain extent, tolerate or even adapt to an error caused by noisy input data or erroneous computation. Widely used approaches in approximate computing are precision scaling and approximate arithmetic.

In precision scaling [1], we use fewer bits to represent numeric values rather than executing all the required mathematical operations with the full representation. Several standards for the floating-point presentation recently appeared: IEEE 754-2019 for half-precision

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[2], posit format with dynamic range and mantissa [3] and Google's bfloat16, targeting the machine-learning workloads [4]. Storing the numeric values with fewer bits reduces the size of arithmetic circuits and their complexity. Besides, it saves on-chip memory and reduces the amount of data that must be transferred, improving speed.

Multiplication represents a ubiquitous arithmetic operation in neural network processing. Moreover, multipliers are complex circuits that importantly affect a processing hardware's area and energy footprint. Hence, the applications can benefit in terms of power and area consumption by replacing the exact multiplier with an approximate one. The approximate multiplier design can originate in the logarithmic approximation of numerical values [5-8] or non-logarithmic approaches, like discarding some stages in Booth multipliers [9-11]. Although most approximate multipliers are designed for fixed-point arithmetic, many floating-point designs, capable of presenting numerical values in a wider range, have appeared lately.

There have been several attempts to use approximate integer multipliers in neural network learning [12-14]. The authors of these studies report that the learning was successful, but they mainly worked with tiny neural networks. To the best of our knowledge, there has yet to be a successful attempt to train large-scale neural networks using approximate multipliers. In neural network learning, we need higher precision arithmetic, so until now, neural networks have mainly been trained using the exact floating-point multipliers [3], [15].

Common to most of the existing designs is that their accuracy can be adjusted at the design time. As such, they can perfectly fit the targeting application but fail for many others. However, many applications need adjustable accuracy during run time. In neural network processing, for example, we can use lower accuracy during the inference phase but need much higher accuracy during the learning phase. Moreover, some parts of an application may still require exact multiplication. For such an application, it would be beneficial to design a multiplier capable of handling all accuracy requirements, thus avoiding putting a plethora of multipliers on a chip and not exploiting them simultaneously.

Several precision-tuning 32-bit floating-point multipliers for deep neural network processing have recently been proposed. The work [16] proposes the 32-bit floating-point approximate PAM multiplier with run-time customisation, which can successfully replace a single-precision floating-point multiplier in some deep neural networks and image-processing applications. In [17], the authors proposed a 32-bit iterative approximate floating-point multiplier based on two-dimensional pseudo-Booth encoding. The accuracy of the proposed multiplier is tuned by three parameters: iteration, encoder's radix, and word length after truncation. To our knowledge, the only state-of-the-art approximate 16-bit bfloat multiplier is proposed in [15]. This variable-precision approximate multiplier uses the bfloat16 format for operand representation and the intermediate conversion of product exponent to the posit encoding to control the mantissa multiplication accuracy. All these multipliers were used only in the inference phase in deep learning models and in image-processing applications, where neglectable degradation in accuracy was observed.

A design that would suit most applications should be able to multiply with the required accuracy, not excluding exact computation, and accept a wide range of numeric values. In this paper, we propose an efficient and accuracy-adjustable approximate 16-bit multiplier for operands presented in the bfloat16 format, which does not require any hardware reconfiguration to adapt accuracy and demonstrates its applicability in the neural network inference and learning phases.

In the remainder of the paper, we first detail the proposed BFILM multiplier design. Section 3 shows the hardware characteristics of the design and demonstrates the BFILM multiplier usability in neural network inference and learning. Lastly, we conclude the paper with the main findings.

2 The design of BFILM multiplier

The proposed brain float iterative logarithmic multiplier (BFILM) operates on numerical values in the bfloat16 format. The advantage of representing the numerical value 0 in the bfloat16 format is, that it keeps one sign bit $s(0)$ and the 8-bit exponent $e(0)$ equal to the IEEE 754 single-precision floating-point format but shortens the mantissa $m(0)$ to 7 bits. Thus, it enables using tiny numerical values, important in the neural network learning phase [18] for example. While the multiplier determines the sign and the exponent exactly, it follows the idea of the approximate iterative logarithmic multiplier to compute the mantissa. The number of steps, which determine the accuracy of the multiplier, can be changed on the fly.

Fig. 1 shows the structure of the BFILM multiplier, which takes operands 0_1 and 0_2 to compute the approximate product P_{approx}. The multiplier consists of a straightforward circuit for determining the sign of the product

and two loosely connected circuits for determining the product's exponent and mantissa.

2.1 The exponent circuitry

The exponent circuity in Fig. 1 incorporates two adders. We must add both operands' exponents to get the product's exponent. However, the bfloat16 format uses the offset-binary representation of the exponent, with the zero offset being 127. To correctly code the product's exponent, we need an additional adder to subtract the offset. The logic connected to the carry input c_{in} of the first adder covers the situations when the product's exponent must be normalised due to the large approximate product P_a obtained from the mantissa multiplier.

2.2 The mantissa circuitry

The mantissa circuitry in Fig. 1 comprises the mantissa multiplier and the mantissa normalizer. The mantissa stores only the fractional bits, to which we must prepend the leading one to get an 8-bit fixed point unsigned number at the input to the mantissa multiplier. The multiplication results is a product, given in 16-bit unsigned fixed-point format with two integer bits and 14 fractional bits, of which we take only the nine most significant bits to the output P_a of the mantissa multiplier. We form the product's mantissa m(P_{approx}) regarding the integer part of the output P_a. When it is greater than one with P_a [8] set, we normalise the result by shifting the radix point one place to the left. To do so, we increment the product's exponent and take the middle seven bits P_a [7:1]. In all other cases, normalisation is unnecessary, and the product's mantissa equals the seven least significant bits P_a [6:0].

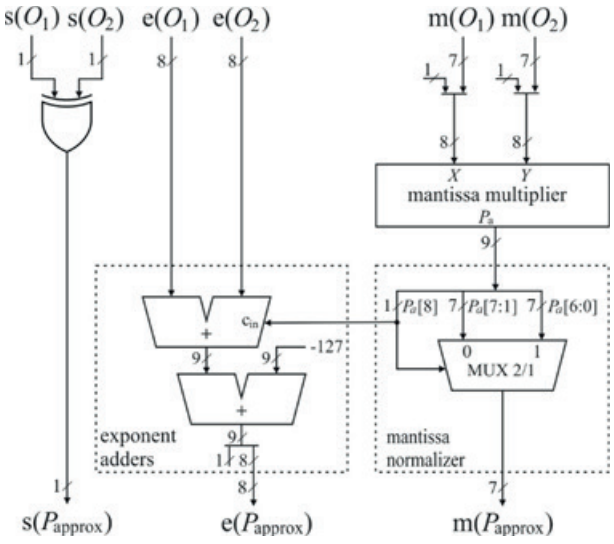

Figure 1: The circuitry of the 16-bit bfloat multiplier.

An important component of the BFILM multiplier is the approximate mantissa multiplier that relies on the iterative logarithmic multiplier (ILM) [7]. Suppose we have two non-negative 8-bit operands *x* and *y*, expressed as the sum of the leading bit and the residuum, $x = 2^{k_x} + r_x$ and $y = 2^{k_y} + r_y$, which multiply to the product

$$\begin{aligned} p = xy = x\left(2^{k_y} + r_y\right) &= x2^{k_y} + xr_y \\ &= x2^{k_y} + 2^{k_x} r_y + r_x r_y \ . \end{aligned} \tag{1}$$

By summing up the first-order Taylor expansions of

$$\begin{aligned} \log_2 x &= k_x + \log_2\left(1 + r_x 2^{-k_x}\right) \\ &= k_x + \ln\left(1 + r_x 2^{-k_x}\right)\log_2 \mathrm{e} \\ &\approx k_x + r_x 2^{-k_x} \log_2 \mathrm{e} \end{aligned} \tag{2}$$

and $\log_2 y \approx k_y + r_y 2^{-k_y} \log_2 \mathrm{e}$, we get the approximation

$$\begin{aligned} \log_2 p &\approx \left(k_x + k_y\right) + 2^{-\left(k_x + k_y\right)}\left(r_x 2^{k_y} + r_y 2^{k_x}\right)\log_2 \mathrm{e} \\ &\approx \left(k_x + k_y\right) + \log_2\left[1 + 2^{-\left(k_x + k_y\right)}\left(r_x 2^{k_y} + r_y 2^{k_x}\right)\right] \end{aligned} \tag{3}$$

By taking the antilogarithm of $\log_2 p$ approximation, we obtain an approximate product

$$\begin{aligned} p_a &= 2^{\left(k_x + k_y\right)}\left[1 + 2^{-\left(k_x + k_y\right)}\left(r_x 2^{k_y} + r_y 2^{k_x}\right)\right] \\ &= 2^{\left(k_x + k_y\right)} + r_x 2^{k_y} + r_y 2^{k_x} \\ &= \left(2^{k_x} + r_x\right)2^{k_y} + r_y 2^{k_x} \\ &= x2^{k_y} + r_y 2^{k_x} \end{aligned} \tag{4}$$

which equals equation (1) with the last term omitted. Thus, computing the product approximation p_a requires only two shifts and an addition, completely avoiding multiplication of the term $r_x r_y$.

The ILM core circuitry in Fig. 2 computes the approximate product and both residua. The leading one detectors extract the leading one bits 2^{k_x} and 2^{k_y} and their characteristic numbers k_x and k_y from operands *x* and *y*. We need both leading one bit to compute the residua and the characteristic numbers to do the required shifts of the operand *x* and the residuum r_y. The truncated barrel shifters output only the nine most significant bits required in further processing, thus importantly reducing their size and the size of the adder.

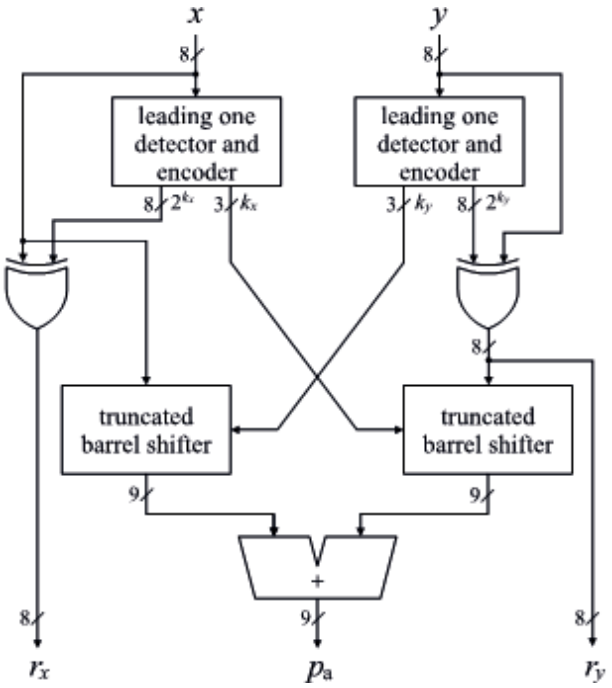

Figure 2: The circuitry of the ILM core.

The relative error of the product $(p - p_a)/p = r_x r_y /p$ can be as high as 25 %. To reduce it, we can iteratively repeat the above procedure by multiplying residua r_x and r_y and adding the result to the current approximation. The procedure can be repeated until at least one residuum becomes zero, thus achieving an error as small as necessary.

The mantissa multiplier shown in Fig. 3 comprises the ILM core, two multiplexers, and an accumulator to iteratively refine the approximate mantissa product P_a. In the initial ILM step ($I = 1$), the multiplexers pass the operands X and Y to the ILM core, while in the next ILM steps ($I>1$), the multiplexers feed the ILM core with residua r_x and r_y from the previous ILM step. The accumulator keeps the approximation of the mantissa product, which is in each ILM step increased by the value p_a. To comply with the circuitry presented in Fig. 1, the accumulator needs to keep only the nine most significant bits.

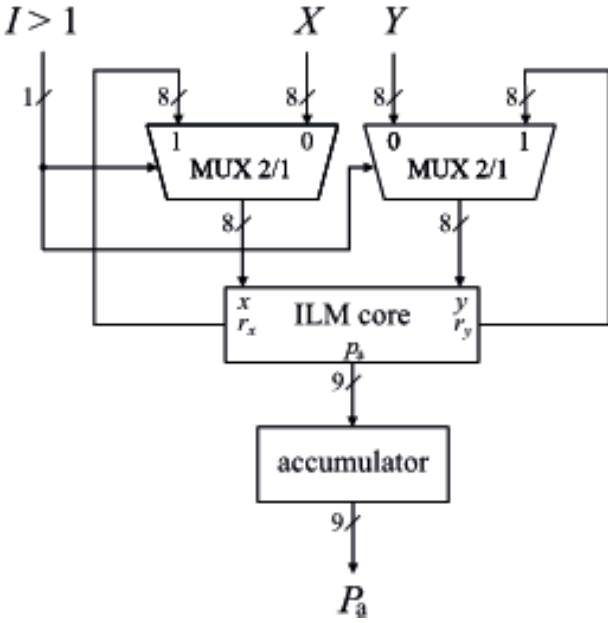

Figure 3: The circuitry of the approximate mantissa multiplier.

At this point, we would like to emphasize that the proposed multiplier does not require any hardware reconfiguration if we want to perform more than one ILM step. For example, when more ILM steps are required, we only need to feed the residua r_x and r_y (Fig. 2) back to the input of the ILM core as presented in Fig. 3. In this case, the multiplexers choose what goes to the ILM core: the new operands, X and Y, or the residua from the previous iteration, r_x and r_y. In the actual implementation, of course, we must add registers at the input of multiplexers, but these are not shown for simplicity.

3 Results

3.1 Hardware performance

We implement the multipliers in Verilog and synthesise them to the SkyWater PDK 130 cell library using OpenLane [19-21]. The library consists of a 130 nm technology with an operating voltage of 1.8 V, and five metal layers [22-23]. The timing constraints, used for all evaluated designs, specify clock-related parameters, which affect synthesis and timing analysis. We set a clock signal with a period of 10 ns, hence not violating a critical path. To evaluate the power, we use timing with a 100 MHz virtual clock (by definition, a virtual clock is a clock that has no real source in the design and is commonly used to specify delay constraints during static timing analysis), load capacitance equal to 33.442 fF (PDK default) and supply voltage equal to 1.8 V.

We analysed the hardware performance of the BFILM multiplier in terms of power, area, delay, and power-delay-product (PDP) and compare it with the exact bfloat16 multiplier. Table 1 shows that the BFILM multiplier outperforms the exact multiplier in all hardware metrics; its energy consumption estimated through PDP is even more than five times smaller.

Table 1: The synthesis results for the examined multipliers.

Multiplier	Delay [ns]	Power [uW]	Area [um^2]	PDP [fJ]
exact bfloat16	2.89	869	6120	2590
BFILM	**1.67**	**298**	**3796**	**498**

Table 2 compares hardware characteristics of the state-of-the-art variable-accuracy bfloat16 multipliers. The results are given as relative values to the standard reference implementations of the exact bfloat16 multiplier. The BFILM multiplier, with its very slim design, outperforms the recently proposed BFLP16-prop multiplier [15] in all aspects.

Table 2: Comparison of the bfloat16 multipliers regarding hardware gains relative to the exact bfloat16 multiplier.

Multiplier	Delay [%]	Power [%]	Area [%]	PDP [%]
exact bfloat16	100	100	100	100
BFLP16-prop [15]	104	58	81	59
BFILM	**58**	**33**	**62**	**19**

Since the BFILM multiplier does not require reconfiguration or additional hardware for more accurate processing, the multiplier's size (area) and power are preserved for an arbitrary number of the ILM steps. Of course, with the additional ILM steps, it is necessary to observe that residua r_x and r_y must be multiplied once or twice and added to the final product. Therefore, in this case, the processing time required to calculate the product increases linearly with the number of the ILM steps and thus does also the energy consumption. We assess different configurations of the BFILM multiplier in terms of delay, energy consumption (PDP) and the mean relative error distance (MRED), and present them in Table 3. For easier comparison, the delay and energy consumption are given relative to the values of the exact bfloat16 multiplier.

The proposed multiplier with two or three ILM steps has a lower energy consumption than the exact bfloat16 multiplier and the BFLP16-prop multiplier [15]. Moreover, the BFILM multiplier with two ILM steps is not much slower than the state-of-the-art BFLP16-prop multiplier [15]. However, the BFILM multiplier with only one ILM step has a rather large error, which with two ILM steps comes close to the BFLP16-prop multiplier's MRED, and then drops by order of magnitude with each additional ILM step.

Table 3: Comparison of delay, PDP, and the MRED error for the different number of ILM steps in the BFILM multiplier.

Multiplier	Delay [%]	PDP [%]	MRED [10^{-3}]
exact bfloat16	100	100	0
BFLP16-prop [15]	104	59	3.50
BFILM, 1 ILM step	**58**	**19**	**91.21**
BFILM, 2 ILM steps	**115**	**38**	**9.08**
BFILM, 3 ILM steps	**173**	**58**	**0.86**

These results suggest that the BFILM multiplier should fit well with error-resilient applications where low-energy consumption is an important goal and where most of the time the BFILM multiplier with a small number of ILM steps could be used. An important feature of the BFILM multiplier is that we can control the product accuracy by adjusting the number of ILM steps without hardware modification, ultimately leading even to removing the exact multiplier from the circuitry.

3.2 Impact on neural network learning

Convolutional neural networks achieve remarkable performance in visual recognition tasks [24]. However, the learning and inference of convolutional neural networks are computationally demanding tasks that involve many multiplications. Nevertheless, convolutional neural networks are error-tolerant models, making them perfect candidates for employing approximate multipliers. Therefore, we assess the influence of the proposed multiplier on the performance of the inference and learning phases.

To evaluate the BFILM multiplier, we select the ResNet-20 convolutional neural network [25-26] and the CIFAR-10 dataset [27]. We change the number representation in the ResNet-20 convolutional neural network from the single-precision floating-point format to the bfloat16 format. In the experiments, we use the Caffe framework [28], where we replace the calls to the cuBLAS multiplication routines with the calls to our own GPU kernels, which emulate the proposed BFILM multiplier.

The neural network learns using the predetermined split of the dataset to train and test sets [27]. Before learning, we preprocess the images by subtracting their mean value. Besides, we quantify the ResNet-20 single-precision floating-point weights to the bfloat16 format representation by simply discarding the last 16 bits of the floating-point mantissa. In the learning phase, we optimize the multinomial logistic loss function [29] with the Nesterov momentum algorithm [30]. The learning starts with randomly initialised weights. In all experiments, we train the network for 64000 epochs.

In the first experiment, we evaluate the influence of the proposed multiplier on the ResNet-20 classification accuracy. As the BFILM multiplier is configurable in terms of the number of steps affecting the multiplication error, we test several BFILM configurations. In the tested configurations, BFILM-1-1, BFILM-1-2, BFILM-2-2 and BFILM-2-3, the first number denotes the number of ILM steps in the inference phase, while the second number denotes the number of ILM steps used in the learning phase.

Table 4 shows the classification accuracy of the CIFAR-10 dataset. For each configuration, we list the average value and standard deviation over five runs. Significant multiplication error of BFILM-1-1 leads to low classification accuracy. Increasing the number of the ILM steps in the inference and learning phase improves classification accuracy. For example, with BFILM-2-2 and BFILM-2-3, the classification accuracy is almost the same as with the exact bfloat16 multiplier.

Table 4: Performance of the ResNet-20 convolutional neural network on the CIFAR-10 dataset using bfloat16 multipliers.

Multiplier	Test set classification accuracy [%]
exact bfloat16	91.50 ± 0.10
BFILM-1-1	86.32 ± 1.26
BFILM-1-2	90.98 ± 0.15
BFILM-2-2	91.30 ± 0.30
BFILM-2-3	91.40 ± 0.20

Also, we can see from the results for BFILM-1-1 and BFILM-1-2 that increasing the number of the ILM steps in the learning phase positively affects classification performance. On the other hand, a further increase in the number of steps in the inference phase from BFILM-1-2 to BFILM-2-2 has much less impact. Moreover, according to Table 3, BFILM-1-2 has a very small energy footprint and thus could be sufficient for neural network inference and learning.

The second experiment highlights the advantage of the on-the-fly accuracy adaptation of the BFILM multiplier, which can help in faster and more energy-efficient neural network learning. The idea is to start with one ILM step in the inference and learning phase to save energy and later, when model performance improves, increase the number of the ILM steps to further refine the result.

Fig. 4 shows the outcome of the learning process on the training and testing set for five separate runs, each with randomly initialised neural network weights. For the loss (red) and the accuracy (green), we show the span of obtained values and the curve averaged over all runs. We see that with the BFILM-1-1 configuration, the model improves rapidly and reaches a classification accuracy of more than 60 % in only 10000 epochs. At this point, we use an additional ILM step in the learning phase (BFILM-1-2) to improve the model's convergence and achieve more than 99.4 % of the accuracy of the exact bfloat16 multiplier. However, if the accuracy still needs to be increased for some applications, we can enhance the model by training it with additional ILM steps.

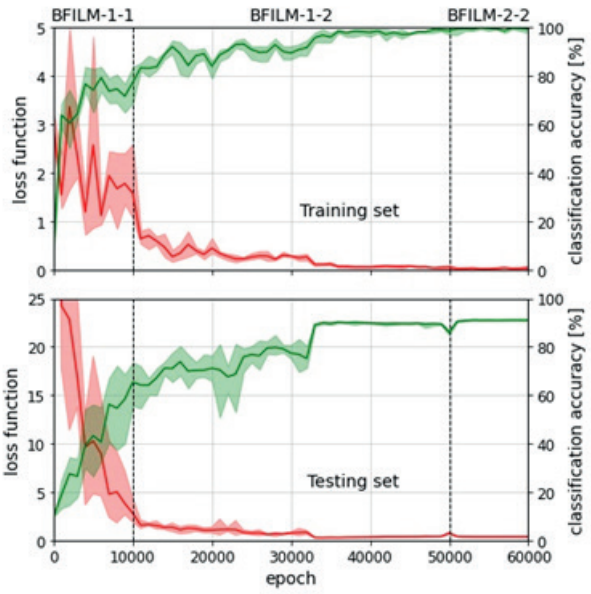

Figure 4: Varying configuration of BFILM during the learning phase.

4 Conclusion

In this paper, we proposed a novel approximate bfloat16 multiplier with adjustable accuracy, which can be achieved without any hardware reconfiguration. Instead, the proposed BFILM multiplier iteratively uses an approximate logarithmic multiplier core to reduce the error. This way, we avoid using additional error refinement circuits, keeping the design small and energy efficient. The primary purpose of the proposed design is to use it in deep neural network processing in the inference and learning phases. We apply the BFILM multiplier in the ResNet-20 convolutional neural network to classify the CIFAR-10 dataset. We demonstrate the impact of various BFILM configurations on the neural network learning process and classification accuracy. The results show that we can easily adjust the multiplier's accuracy according to the application's requirements. The main advantage of the on-the-fly adaptation of the BFILM multiplier comes to expression during the learning phase. The results prove that we can start with one ILM step in the inference and learning phase to save energy and later, when model performance improves, increase the number of the ILM steps to refine the result further. In future work, we aim to develop an algorithm that could optimize the learning process in terms of speed and efficiency by automatically adapting the ILM steps to the BFILM multiplier when needed.

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6 Conflict of Interest

The authors declare no conflict of interest.

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A New Design Optimization Methodology of Fully Differential Dynamic Comparator

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Abstract: The need to reduce the time to market for high-performance integrated circuits has become a primary concern in modern electronics design. Many efforts are currently being made to streamline the design process for increasing complexity circuits while providing optimal performances, especially for nanoscale technologies. This paper presents a new and effective methodology for the design of fully differential comparators to achieve a high-performance operation using dynamic topology and nanoscale technology. The proposed methodology is not process dependent and can be applied to similar conventional comparator structures to optimize the operation speed while ensuring good offset cancellation, efficient noise immunity, and reduced design time and complexity. The design steps include theoretical analysis and simulation-based optimization of the comparator speed, as well as offset and noise reduction within a minimal design time. All the analog and digital building blocks are designed using dynamic topologies, including the clock generator, to ensure high speed and synchronized operation. The resulting circuit is a new two-stage dual clock fully differential comparator. Compared with its equivalent counterparts, it provides improved operation speed, and reduced offset voltage and kickback noise. This comparator is designed in the TSMC 65 nm CMOS process. Its performance shows that it achieves a 1.25 GHz operation speed, presents less than 9 mV offset error, and generates a kickback noise of less than 40 mV with a 10 kΩ input resistance during the reset phase only. It consumes 213 µW from a 1.2 V power supply at 1.25 GHz.

Keywords: fully differential dynamic comparator; kickback noise; offset self-calibration; clock generator; finite state machine.

Nova metodologija optimizacije zasnove polnega diferencialnega dinamičnega komparatorja

Izvleček: Potreba po skrajšanju časa za trženje visoko zmogljivih integriranih vezij je postala glavna skrb pri sodobnem načrtovanju elektronike. Trenutno potekajo številna prizadevanja za racionalizacijo postopka načrtovanja vedno bolj zapletenih vezij ob zagotavljanju optimalnih zmogljivosti, zlasti za tehnologije v nanometrski razsežnosti. V tem članku je predstavljena nova in učinkovita metodologija za načrtovanje polnih diferencialnih komparatorjev za doseganje visoko zmogljivega delovanja z uporabo dinamične topologije. Predlagana metodologija ni odvisna od procesa in jo je mogoče uporabiti za podobne konvencionalne strukture komparatorjev, hkrati pa zagotovi dobro izničevanje odmikov, učinkovito odpornost proti šumom ter skrajša čas in zapletenost načrtovanja. Koraki načrtovanja vključujejo teoretično analizo in na simulaciji temelječo optimizacijo hitrosti delovanja komparatorja ter odpravo kompenzacije in šuma v minimalnem času načrtovanja. Vsi analogni in digitalni gradniki so zasnovani z uporabo dinamičnih topologij, vključno z generatorjem ure, da se zagotovi visoka hitrost in sinhronizirano delovanje. Tako nastalo vezje je nov dvostopenjski dvotaktni polni diferencialni komparator. V primerjavi z enakovrednimi primerki zagotavlja večjo hitrost delovanja ter manjšo kompenzacijsko napetost in šum povratnega udarca. Ta komparator je zasnovan v 65 nm postopku CMOS podjetja TSMC. Njegovo delovanje kaže, da dosega hitrost delovanja 1,25 GHz, ima manj kot 9 mV napako odmika in ustvarja šum odboja manj kot 40 mV z vhodno upornostjo 10 kΩ. Pri 1,25 GHz porabi 213 µW iz 1,2-voltnega napajanja.

Ključne besede: fully differential dynamic comparator; kickback noise; offset self-calibration; clock generator; finite state machine.

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1 Introduction

The scaling of silicon technologies has been one of the primary factors that have allowed for outpacing the exponential increase of performance demand over the past few decades. Transistor scaling increases the integration density and operation speed. At the same time, the resulting circuits are more sensitive to random and systematic errors, such as offset and noise. Additional circuitry for error compensation and noise suppression is then needed, leading to a drastic increase in design time and effort. Therefore, in modern circuit design, optimization methodologies to improve performances have become mandatory not only to answer to the increasing design constraints, but also to compensate for increased errors and noises while optimizing the time to market. Recently, optimization methodologies have become a major research field in MOS circuit design [1]–[3].

Dynamic comparators are largely used in advanced mixed signal systems, such as analog to digital converters (ADCs). The design constraints of these systems are usually stringent, depending closely on those of the comparator. To improve the immunity of ADCs to sensed common noise, a specific variant of the dynamic comparator is usually used [4]– [7]; it is a six-terminal circuit that compares an input voltage difference to a reference voltage difference [8] and is commonly called a differential pair comparator or fully differential dynamic comparator (FDDC). However, it is slower than the common four-terminal-like circuit and is more sensitive to kickback noise, as well as process and mismatch variations [9]. Achieving high performance and good noise immunity with a six-terminal dynamic comparator requires more design effort and time than with the common four-terminal one. Therefore, design methodologies could help designers significantly reduce design time and efforts.

An FDDC was employed in [4] for its low kickback noise, good power efficiency, and simple dynamic structure. To reduce mismatch effects on loop stability, the authors kept the comparator gain at low values, leading to a considerable decrease in the operation speed. As for immunity to comparator noise, the authors applied a noise-shaping successive approximation register quantizer to all stages in a pipelined ADC. Although the proposed technique has advantages other than the noise immunity of the comparator, it remains complex and specific to the designed ADC. In [5], a charge distribution FDDC was used to implement a level-crossing ADC. It was constructed with two separate comparators to compare the differential input voltage to a differential reference voltage. The two separate comparators were more sensitive than an all-in-one FDDC when it came to the process and mismatch variations and noise unbalance. The suppression of the sensed common noise was less efficient. In addition, the comparison was performed over two clock cycles, which affected the operation speed. Moreover, a static second stage was added to the comparator to increase the gain, making the comparators even slower. Another FDDC was used in [7] to implement a SAR-assisted noise-shaping pipeline ADC. The proposed structure included self-calibrated current sources to compensate for mismatches and operated with two synchronized clocks. The circuit design achieved good performance. However, the proposed comparator was specific to the designed ADC and the operation speed was very low.

As for offset compensation, mismatches are usually calibrated off-chip to reduce the design complexity [4], [5]. In [7], a background calibration for interstage offset was proposed to compensate for comparator mismatches. Even if the operation speed was not altered, there were "dead zones" in the calibration scheme that reduced its efficiency. Moreover, the proposed scheme mainly relies on the overall system architecture and can hardly be reproduced with a different circuit design.

The comparator gain is also an important feature to implement high-resolution ADCs. It is usually increased by using preamplification stages or multistage comparators. In [5], a three-stage comparator was used, but only the first one was dynamic. Thus, the comparator gain was high, whereas the operation speed was low. Likewise, a two-stage dynamic comparator, in which only the first stage is dynamic, was also presented in [10]. In [11], a three-stage, fully dynamic comparator was proposed. However, the presented structure was not fully differential, and the three stages operated over the same clock period.

The current paper presents a new two-stage fully dynamic fully differential comparator. The decision is made over the entire clock period. Also, additional circuitry is added to generate synchronized clocks, to reduce kickback noise, and to compensate for mismatches. The whole system is fully dynamic without a considerable increase in design complexity. It achieves a fully differential comparison, optimal operation speed, good immunity to kickback noise, and self-calibrated offset voltage. The proposed design is process independent and can be used in different applications.

Section 2 presents the proposed system architecture of the FDDC, including clock generation, kickback noise immunity, and offset calibration. The new two-stage FDDC is presented and discussed in section 3. Its operation is also detailed and compared with the one-stage-like circuit. Section 4 describes the proposed

circuit and how it ensures immunity to kickback noise while also detailing the clock generator design. Section 5 presents the proposed design technique for a digital offset self-calibration scheme using full custom dynamic circuits. Section 6 presents the simulation results and circuit characterization. A comparison to state-of-the-art performances is also addressed.

2 Proposed system architecture

The comparator is typically a one-bit ADC. When the difference between the compared voltages is about a few hundred millivolts or more, the decision process is usually accurate and fast. However, as the input voltage decreases to a few millivolts and less, the decision process becomes much slower and more sensitive to the input signal quality, as well as to circuit nonidealities such as offset and switching noises. Indeed, analog signals usually present noise. Noise is random and common to comparator inputs. On the other hand, a dynamic comparator is usually designed with small

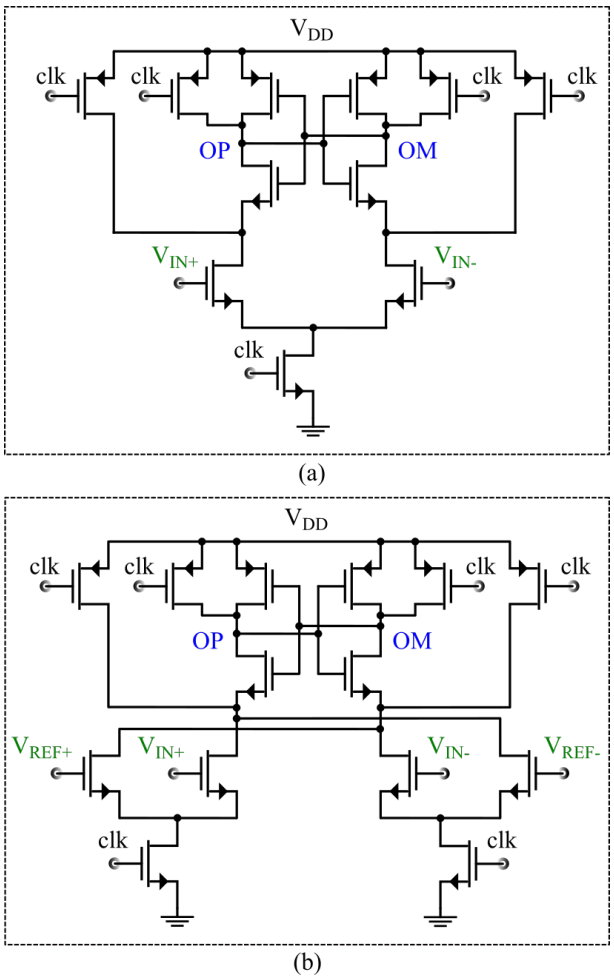


Figure 1: Strong-arm latch comparator (a) dynamic comparator (b) fully differential dynamic comparator.

MOS devices, which makes the circuit more sensitive to process and mismatch variations, especially when designed in nanometer-scale technologies. Moreover, because of the dynamic operation of the comparator, there are large voltage variations in the internal nodes between devices. These variations are coupled through parasitic capacitors to the comparator inputs as a voltage signal creating a disturbance that is usually called kickback noise. This switching noise is added to the analog input signal and affects the comparison results. Kickback noise cannot be removed, but there are a few techniques to reduce its effects on the decision process [12], [13].

Fig. 1(a) shows a four-terminal comparator, which is known as the strong-arm latch comparator and has been largely used in ADC design [14]. It presents two inputs and two outputs. One input is generated from an external voltage source, while the other comes from a resistive ladder. This affects the two inputs with different noise levels, making the comparison process only effective when the sensed voltage is greater than the difference between the two input noise signals. In contrast, a six-terminal comparator is shown in Fig. 1(b); this is called the differential pair comparator [8], [15] or FDDC [16], [17], and has been largely used in pipeline and SAR ADCs [18]. This comparator presents four inputs and two outputs.

The inputs are a differential analog input signal and differential reference voltage. The two outputs are complemented: a positive output *OP* and negative output *OM*. The positive output *OP* goes high when the differential analog input voltage V_{IN+} - V_{IN-} is greater than the reference voltage difference V_{REF+} - V_{REF-}:

$$\begin{aligned} &if\ \left(V_{IN+}-V_{IN-}\right)-\left(V_{REF+}-V_{REF-}\right)\geq 0 \\ &\quad then\ OP='1'\ and\ OM='0' \\ &\quad else\ \ OP='0'\ and\ OM='1' \end{aligned} \tag{1}$$

Thus, the common noise in each differential input is cancelled separately, which considerably improves the comparator precision. This section describes the top-level architecture of the proposed FDDC, including immunity to kickback noise and self-calibration of the offset voltage.

Fig. 2 describes the proposed system. The symbol shown in Fig. 2(a) presents the input and output terminals of the system. Fig. 2(b) illustrates the clock diagram of the external and internal clock signals, while Fig. 2(c) depicts the top-level architecture.

The proposed comparator is a new two-stage FDDC. The clock generator produces two synchronized clock

signals *clk* and clk_s to ensure the operation of the first and second stages, respectively. To reduce the input noise, an RC circuit can be added at the comparator inputs as a first-order filter, but at the price of a reduced operation speed. In the proposed solution, the resistance of a CMOS switch and parasitic capacitor *Cp* at the comparator inputs together form an RC filter. These two components are too small to affect the comparator speed but also too small to ensure the cancellation of the kickback noise. Therefore, in the proposed scheme, the switches, together with the input parasitic capacitors, are used as track-and-hold circuit blocks, which are controlled to reduce the effect of noise on the decision process. Two clock signals clk_n and clk_n' are used to control the switches to operate only during the comparator reset time (when *clk* = `0') before beginning a new cycle. Thus, kickback noise appears at the comparator inputs for a limited period, during which the decision process cannot be affected.

The clock generator provides four synchronized clock signals: *clk*, clk_s, clk_n, and clk_n'. These clock signals ensure a three-phase operation comparator: track-and-hold, decision, and reset. The circuit is designed so that the track-and-hold, as well as a part of the decision process, are performed during the reset time, which improves the comparator speed compared with the state-of-the-art method. The comparator is described in detail in section 3, while noise suppression and clock generation are presented in section 4.

To compensate for the comparator offset errors, a three-phase operation system is proposed. First, the initial reset phase is controlled using the external signal *reset*. When this signal is high, the two *N*-bit outputs *d+* and *d-* of the two counters are initialized to zero. Thus, the initial reset phase allows for initializing the capacitor banks to equal initial charges. This represents the initial state S_0 of the two FSMs used in the self-calibration process. At that time, the eight input switches are configured to connect the four comparator inputs *IN+*, *IN-*, *REF+*, and *REF-* to the differential inputs V_{IN+}, V_{IN-}, V_{REF+}, and V_{REF-}, respectively. Second, a calibration phase is controlled by two complementary external signals *calib* and *calib'*. This phase occurs only once after the initial reset phase. When *calib* and *calib'* are set to '1' and '0', respectively, eight switches (in blue in Fig. 2(c)) that are placed at the system inputs disconnect the comparator inputs *IN+*, *IN-*, *REF+*, and *REF-* from the differential inputs V_{IN+}, V_{IN-}, V_{REF+}, and V_{REF-}, and connect them to the common mode reference voltages V_{CM}, which ensures equal charges at the input parasitic capacitors. V_{CM} is the mean value of the input range. During the calibration phase, the comparator outputs *Q+* and *Q-* are applied to the offset regulator. At each clock cycle, according to *Q+* and *Q-* levels, the clock generator increments one of the two *N*-bit control signals *d+* and *d-* by 1 to compensate for the mismatches in the comparator as well as in the switches at the comparator inputs. This process continues as long as *Q+*, *Q-*, *calib* and *calib'* remain unchanged. The offset regulator design is detailed in section 5.

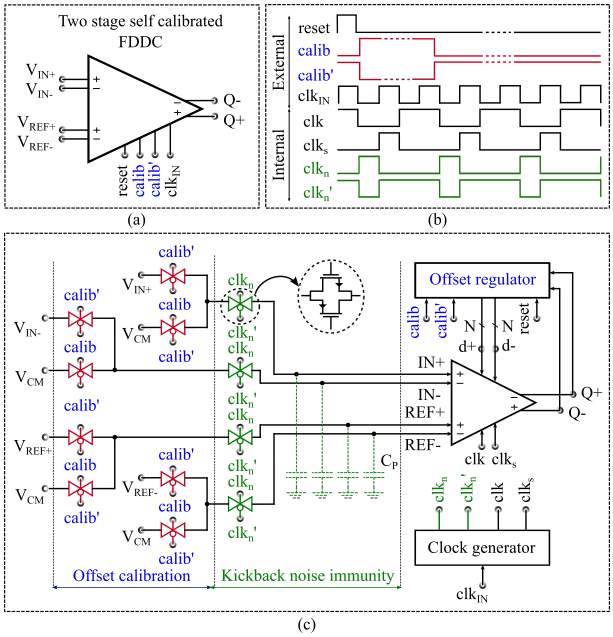


Figure 2: Proposed system (a) symbol view (b) clock diagram (c) architecture.

3 New two-stage fully differential comparator

The operation speed is a primary constraint in the comparator design. The comparison speed can be defined as the time required to provide a valid output decision. A dynamic comparator operates under a clock signal *clk* alternating decision and reset phases in each clock cycle. The two phases of decision and reset usually correspond to the two clock levels '1' (on) and '0' (off). Thus, denoting the decision and reset times by t_{on} and t_{off}, respectively, the total comparison time t_{clk} is equal to:

$$t_{clk} = t_{on} + t_{off} \tag{2}$$

A track-and-latch circuit, basically a Set Reset (SR) latch, is usually added to the comparator outputs to retrieve static output signals. Thus, the decision time t_{on} is typically the sum of two times: the comparison time t_c needed by the dynamic comparator to produce a valid output, and the SR latch time t_{SR} required by the SR latch to change state according to the comparator outputs. The decision time t_{on} is then equal to:

$$t_{on} = t_c + t_{SR} \tag{3}$$

Once the SR latch state has changed, the comparator outputs can be reset to the initial value without affecting the SR latch state until the next decision process begins. Inserting (3) into (2), the total comparison time t_{clk} is then defined in terms of the comparison time t_c, the SR latch response time t_{SR} and the reset time t_{off}:

$$t_{clk} = t_c + t_{SR} + t_{off} \tag{4}$$

The comparison time t_c depends on the internal capacitor sizes, internal feedback loops, and the value of the resolved input voltage. For a few hundred millivolts of the input voltage, t_c can be small and reach nano and picoseconds according to the comparator structure. However, when resolving near 0 V input values, the comparator output evolution becomes slow and t_c tends to infinity. Therefore, to sense micro and nanovolt input values in a reduced time, it is necessary to minimize the comparator internal capacitors by using small devices, and to improve the comparator structure by creating positive feedback loops, immunity to switching noises, and compensation for process and mismatch variations.

A double tail and three-stage triple-latch comparators are designed with a 28 nm MOS process [11]. The first one is a two-stage double tail comparator that includes only one positive feedback loop, while the second one includes three positive feedback loops. The first one achieves a comparison time t_c equal to 50 ps against 27 ps for the second comparator when resolving the 5 mV input value. Nevertheless, in the two comparators, the stages operate during the same clock period, which makes t_c the sum of the response times of all stages put in a series. Moreover, there is no improvement for t_{SR} and t_{off} in the total comparison time t_{clk} in (4). In [3], a two-stage dual-clock latch comparator is proposed. The comparator includes one feedback loop. However, the second stage is controlled by a second clock, reducing the on-time t_{on} in (2) to t_c only. Thus, the total comparison time t_{clk} defined in (4) becomes:

$$t_{clk} = t_c + t_{off} \tag{5}$$

Moreover, the second stage is built with a stack of two elements only, which reduces the total capacitor seen at the outputs of the first stage, leading to a minimal comparison time t_c. The comparator is designed with a 180 nm MOS process and achieves a comparison time of 900 ps when resolving a 25 µV input value. However, the second stage operates when only one of the first-stage outputs decreases to a threshold value. If both outputs reach this value, the second-stage outputs will not be complementary, and the comparison decision will not be valid. This happens when resolving small input values and when the PMOS threshold voltage $|V_{THP}|$ is larger than $V_{DD}/2$, which is usually the case in scaled technologies like 65 nm and below.

In the present work, a new two-stage FDDC where the comparison speed is optimized with no restriction on technology use is proposed. Indeed, as shown in Fig. 3, each stage includes a positive feedback loop, which reduces the comparison time t_c compared with [3]. In addition, the positive feedback loop in the second stage provides complementary outputs, regardless of the technology parameters used. Moreover, the two stages operate under two different clock signals as in [3], which reduces the total comparison time t_{clk} to the sum of the decision time t_c and the reset time t_{off} as defined in (5).

The circuit operates as follows: in the first stage, a differential analog input voltage $\Delta V_{IN} = (V_{IN+} - V_{IN-})$ and differential reference voltage $\Delta V_{REF} = (V_{REF+} - V_{REF-})$ are applied to the four input pair transistors ($M_{1\text{-}4}$). The voltages V_{IN+} and V_{REF-} are applied to transistors ($M_{1,4}$), which have a common drain. These transistors generate two currents and feed node *X*- with a current, which is the image of the sum of the two applied voltages ($V_{IN+} + V_{REF-}$). Likewise, considering the circuit symmetry, transistors ($M_{2,3}$) feed node *X*+ with a current, which is the image of the sum of the two applied voltages ($V_{IN-} + V_{REF+}$). When the clock signal *clk* is low, the tail transistors ($M_{5,6}$) turn off, while the reset transistors ($M_{11\text{-}14}$) turn on. This allows for initializing the latch nodes *X*+, *X*-, *O*+ and *O*- to V_{DD}. Conversely, when *clk* goes high, the tail transistors ($M_{5,6}$) close while the reset transistors ($M_{11\text{-}14}$) open. At this time, the four input pair transistors feed the latch nodes *X*+ and *X*- with a differential current $\Delta I_X = I_{X+} - I_{X-}$, which is the image of the voltage difference between the sums of the applied voltages. This voltage difference is denoted as ΔV_{INPUT} and is equal to:

$$\begin{aligned} \Delta V_{INPUT} &= \left(V_{IN+} + V_{REF-}\right) - \left(V_{IN-} + V_{REF+}\right) \\ &= \left(V_{IN+} - V_{IN-}\right) - \left(V_{REF+} - V_{REF-}\right) \end{aligned} \tag{6}$$

The resulting ΔI_X activates the latch transistors ($M_{7\text{-}10}$) which operate as a strong positive feedback loop to regenerate the outputs *O*+ and *O*- to complementary logic levels. The generated outputs are then applied to the input transistors ($M_{s1,s2}$) of the second stage. Transistors ($M_{di+(i=1..N)}$) and ($M_{di-(i=1..N)}$) are two capacitor banks, each one including *N* binary-weighted charges. These capacitor banks are controlled by two *N*-bit inputs, *d*+ = ($d_{i+(i=1..N)}$) and *d*- = ($d_{i-(i=1..N)}$), and are used to compensate for process and mismatch variations. This specific

structure of the charges also reduces the switching noise and improves the operation speed [3].

Considering the second stage, when clk_s is high, outputs O_s+ and O_s- are initialized to '0' turning off transistors ($M_{s3,s4}$). As clk_s becomes low, reset transistors ($M_{s5,s6}$) open. As shown in Fig. 3(b), this happens at the end of the reset phase of the first stage, where both outputs *O*+ and *O*- are initialized to V_{DD}. Thus, transistors ($M_{s1,s2}$) turn off like the other four ones. When one of the first stage outputs *O*+ and *O*- begins decreasing, transistor (M_{s1}) or (M_{s2}), respectively, begins operating to charge one of the output voltage O_s+ and O_s-, respectively, to V_{DD}. When the applied input voltage difference is too small, both *O*+ and *O*- can decrease before regenerating to logic levels. Then, transistors ($M_{s3,s4}$) will operate as positive feedback to maintain one of the outputs to '0' while the other one charges to V_{DD}. Without these transistors, this may result in both outputs O_s+ and O_s- at V_{DD}. In this case, when these signals are applied to the SR latch, they create an undefined state, resulting in a wrong output *Q*+ and *Q*- decision.

The last stage is a NOR gate SR latch. It maintains its state when the applied signals O_s+ and O_s- are initialized to '0' and keeps or changes the state when the outputs are complemented, resulting in static outputs *Q*+ and *Q*-.

4 Clock generator and kickback noise suppression

The generation of synchronized clock signals is achieved by sequential circuits using data flip flops (DFFs). The true single-Phase clock (TSPC) DFF presented in [19] is considered to design the clock generator in the proposed system in Fig. 2(c). It is a nine-transistor, three-stage DFF operating with one single clock signal and including no more than three stacked devices per stage. This circuit is shown in Fig. 4, where a reset command and inverter are added to the output.

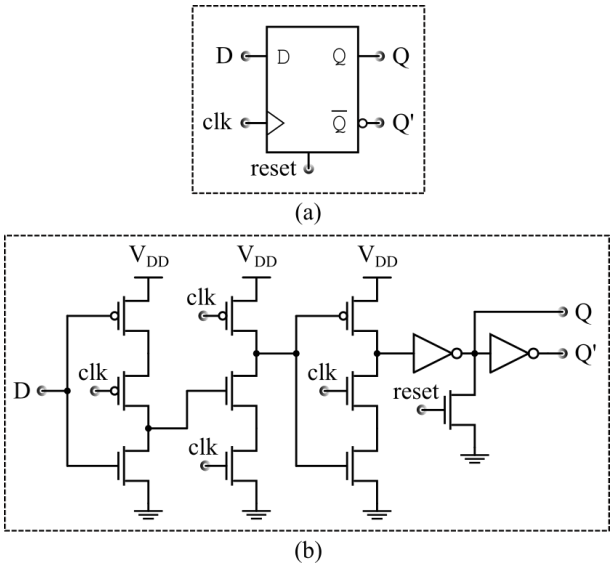


Figure 4: True Single-Phase Clock DFF (a) symbol (b) circuit-level Design.

This structure is convenient and should provide an operational speed greater than the comparator. A detailed description of the circuit can be found in [19].

Fig. 5 shows the design details of the proposed clock generator. The circuit generates four signal outputs *clk*, clk_s, clk_n and clk_n'. Because the last two are complemen-

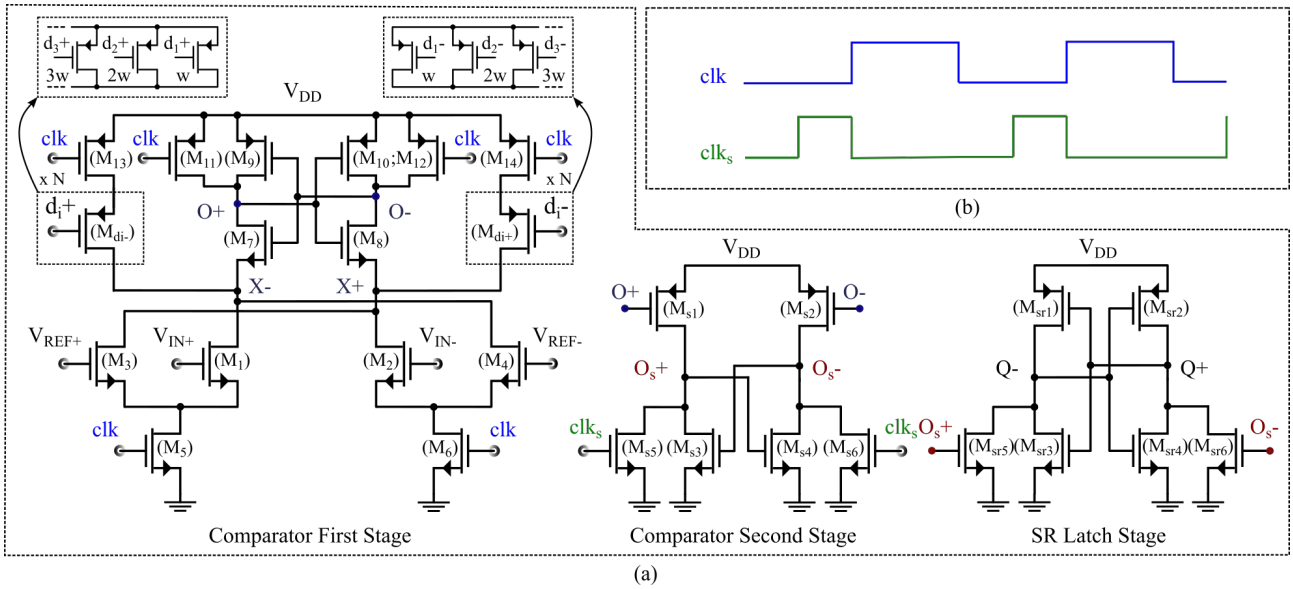


Figure 3: Proposed FDDC (a) circuit (b) clock diagram.

tary, the circuit states can only be defined according to the three outputs *clk*, clk_s, and clk_n. These three outputs are denoted by vector $c = (clk\ clk_s\ clk_n) = (x\ x\ x)$, where x is equal to '1' or '0'. As described in Fig. 5(a) and (b), the circuit goes through four states S_0, S_1, S_2, and S_3. First, the clock generator is initialized to state S_0 with an external reset = '1'. This state corresponds to the sample-and-hold phase by connecting external signals to the comparator inputs (Fig. 1(c)). This also corresponds to the reset of the comparator first stage. Vector *c* is then equal to (0 0 1). Second, state S_1 corresponds to the reset of the two comparator stages, for which *c* is equal to (0 1 0). Third, state S_2 is the state where the comparator first-stage operation begins, which corresponds to *c* equal to (1 0 0). Fourth, state S_3 is the continuation of state S_2 with *c* still equal to (1 0 0). This last state is required because the first-stage operation is slower than the second one. Therefore, high and low levels of *clk* must last longer than those of clk_s and clk_n.

The finite state machine (FSM) is depicted in Fig. 5(b). It has no inputs and generates the three outputs: *clk*, clk_s, and clk_n. The gate-level and circuit-level synthesis are given in Fig. 5(c) and (d), respectively. An inverter is added to generate the complement of clk_n. State S_0 is the sample-and-hold state, while state S_2 is the decision phase. Inserting states S_1 and S_3 in between S_0 and S_2 allows for reduction of kickback noise effects on the decision process. Indeed, as discussed in [13], isolating the decision process from the sample-and-hold phase can significantly reduce the effect of kickback noise on the decision process. However, the clock generation in [13] used delay circuits, and outputs were not synchronized. Hence, the design was specific to the chosen clock timing, as well as to the technology used. In contrast, the proposed design generates synchronized outputs and can be reproduced without considering the technology used or transistor size.

5 Proposed offset self-calibration technique

In Fig. 2(c), the proposed offset regulator receives the comparator static outputs *Q*+ and *Q*- and generates two N-bit outputs *d*+ and *d*-. These outputs are then used to control the 2*N* binary-weighted transistors (M_{di+}) and (M_{di-}) shown in Fig. 3(a). The least significant bit (LSB) transistor is set to minimal dimensions, while, for the other weighted transistors, the channel width is doubled until reaching the most significant bit (MSB) transistor. The main idea is to create a progressive charge imbalance to compensate the comparator offset as in [3], [20]. However, in [3], a high-level design methodology for the self-calibration scheme is proposed. As a result, the circuit is slow and large because of the large number of chained gates. Whereas in [20], the offset regulation is off chip and too complex for a circuit-level design. In the present work, the proposed

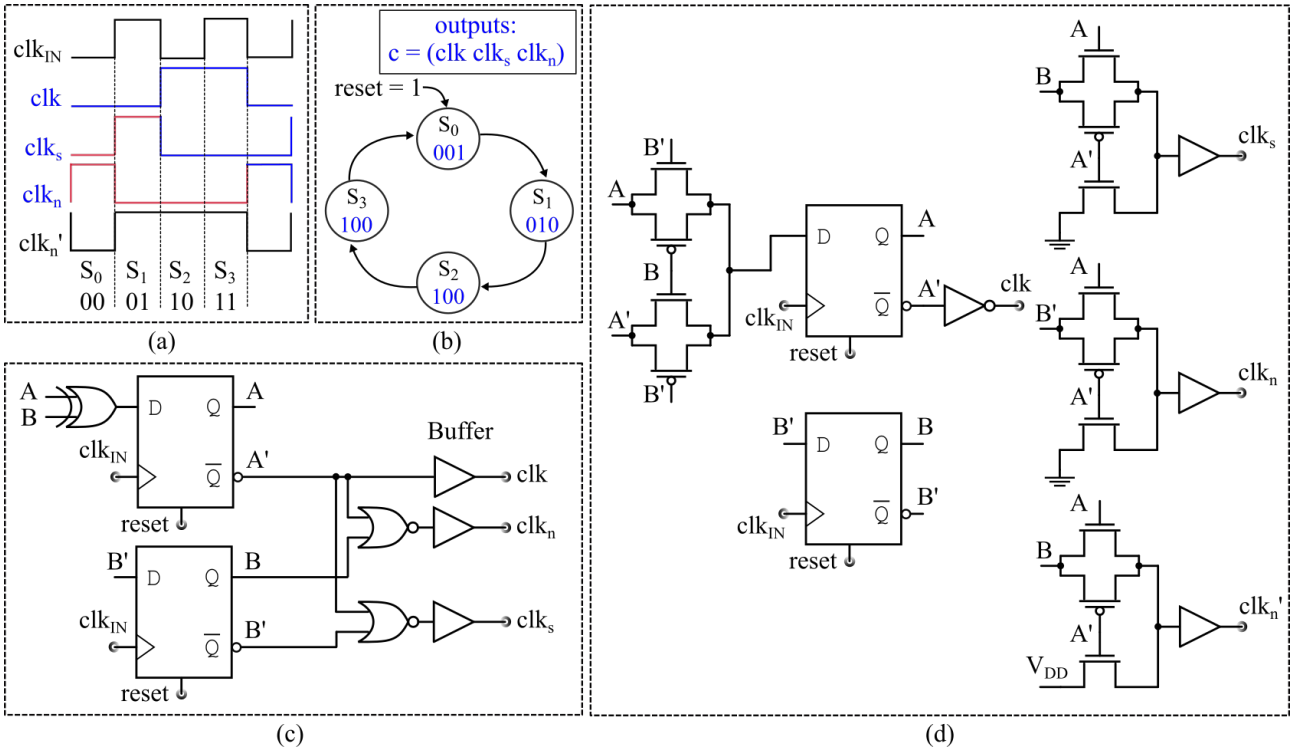


Figure 5: Proposed clock generator design (a) clock diagram (b) Moore finite state machine (c) gate-level design (d) circuit-level design.

offset regulator is minimalist and could be easily designed at the circuit level.

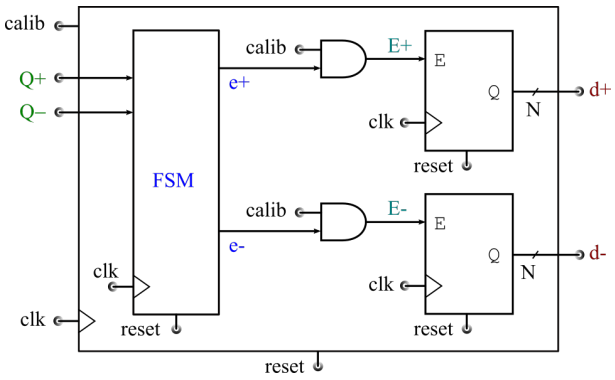


Figure 6: Block diagram of the proposed offset regulator.

The proposed offset regulator block diagram is presented in Fig. 6. The circuit input stage is an FSM, which receives the comparator static outputs *Q*+ and *Q*- and generates two control digits *e*+ and *e*-. These two digits are combined into the calibration control signal calib using an AND gate to generate two digital signals: *E*+ and *E*-. These signals are then used as two enable input signals of two *N*-bit counters. The counters generate two *N*-bit control words to calibrate the two capacitor banks in the comparator shown in Fig. 3(a). In these capacitor banks, two cases will not be used to avoid a significant variation in the capacitive compensation load: "all transistors are on" and "all transistors are off", which correspond to *d*+ and *d*- equal to 0 and 2^N-1, respectively. Therefore, the two *N*-bit control signals *d*+ and *d*- should be initialized to 1, for which all the binary-weighted transistors are on, except for the LSB transistor. Then, according to *Q*+ and *Q*- levels, *d*+ and *d*- incrementation will either be stopped by setting *E*+ and *E*- to '0' or pursued by setting *E*+ and *E*- to '1'. The incrementation should stop before reaching 2^N-1, for which all transistors are blocked. The case *d*+ and *d*- equal to 2^N-2 turns off all the calibrating transistors, except the LSB one. The parasitic capacitors of the blocked transistors can be neglected compared with those of the on transistors.

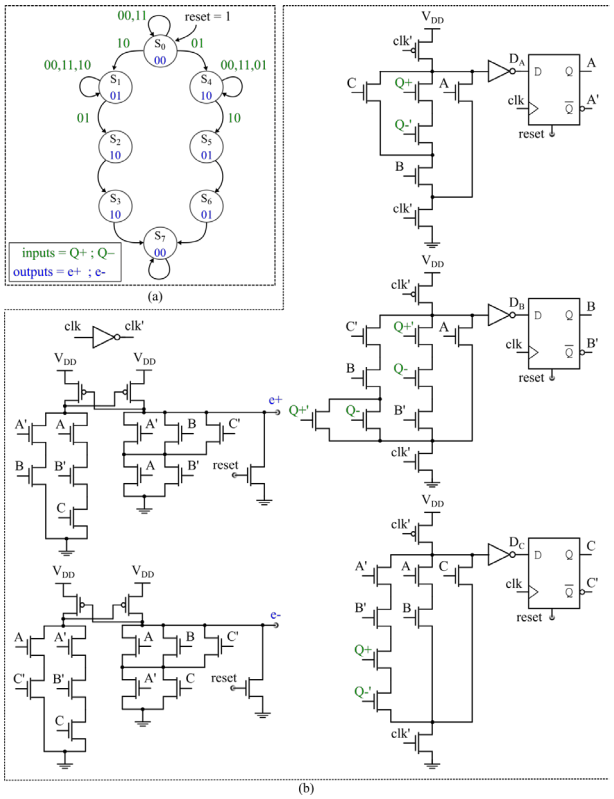


Figure 7: Proposed FSM design to control the two counters, (a) Moore FSM, (b) proposed circuit-level design.

Each conducting transistor is then equivalent to a capacitor. As a result, when *d*+ and *d*- are equal to '1', the *N*-1 largest capacitors are in parallel. This sets the calibrating capacitive load at the maximum value on both sides of the comparator. When applying a 0 V-input voltage, the comparator output *Q*+ is either high or low. When *Q*+ is high, the comparator is considered as exhibiting a positive offset voltage. To compensate for this offset, *d*- is incremented by 1 ($d\text{-} = d\text{-}_{(initial)} + 1 = 2$). This corresponds to a first step decrease of the capacitive load on the right side of the comparator with

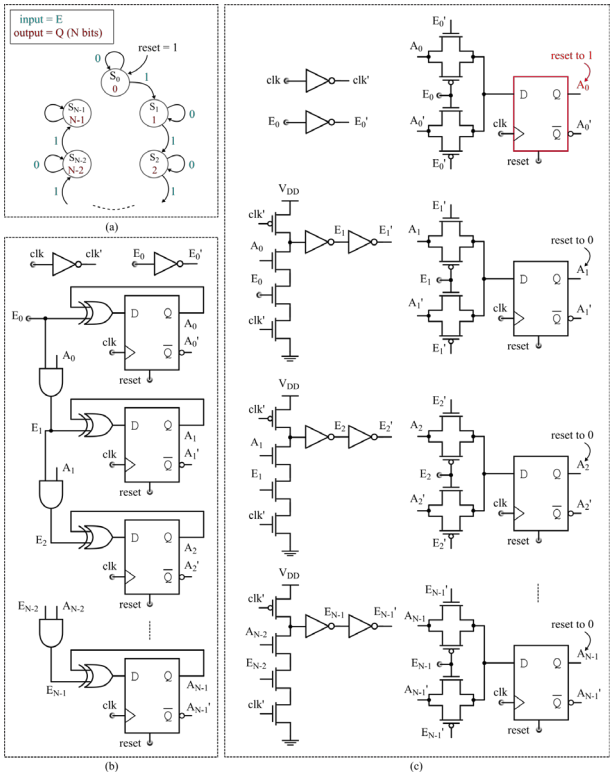


Figure 8: Proposed *N*-bit counter design (a) Moore FSM (b) module-level design (c) proposed circuit-level design to start the counter from 1.

respect to the left side. Hence, in the next comparison cycle, the positive offset voltage either decreases toward 0 V or becomes negative. If the offset voltage is still positive in the next cycle, that is *Q*+ is still high, *d*- is incremented again. This continues until the offset voltage becomes negative, that is *Q*+ becomes low, or until *d*- reaches 2^N-2. The generation of *e*+ and *e*- according to *Q*+ and *Q*- levels is described by the FSM shown in Fig. 7(a). A reset command sets the system to state S_0 where both digital outputs *e*+ and *e*- are set to '0'. When *Q*+ and *Q*- are equal to '1' and '0', respectively, the system enters state S_1 where the outputs *e*+ and *e*- are set to '0' and '1', respectively. The system remains in that state until *Q*+ and *Q*- change to opposite logic levels. When this happens, the system enters state S_2 where outputs *e*+ and *e*- are set to '1' and '0', respectively. This state allows for rebalancing the system once the offset voltage changes signs. Simulations have shown better results when the system is rebalanced twice by adding state S_3.

Then, the system enters a final state S_7 where both outputs *e*+ and *e*- are set back to '0' again. Because the circuit is symmetrical, considering *Q*+ and *Q*- equal to '0' and '1', respectively, leads to states S_4, S_5 and S_6 which are symmetrical to states S_1, S_2 and S_3, respectively. Fig. 7(b) shows the proposed FSM circuit synthesis. It uses dynamic circuits and the DFF shown in Fig. 4. To generate static outputs *e*+ and *e*- with maximal operation speed, switched circuits with positive feedback are used.

The generated outputs are used to control two *N*-bit counters. Fig. 8(a) shows the FSM of an *N*-bit counter. The module-level design of the counter is shown in Fig. 8(b), while the proposed circuit-level design is shown in Fig. 8(c). In the proposed circuit-level design, the first DFF is reset to '1' instead of '0' to initialize the *N*-bit counter to 1 instead of 0. Fig. 9 shows the modified DFF. However, to avoid the counter reaching 2^N-1, the on time of the external signal *calib* is set to exactly 2^N-2 cycles.

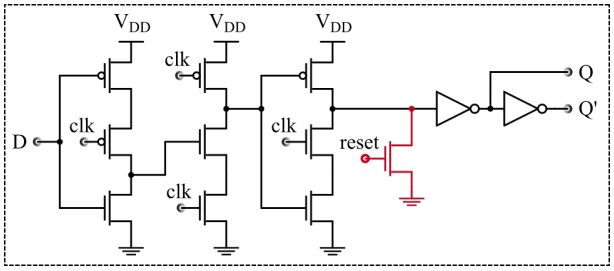
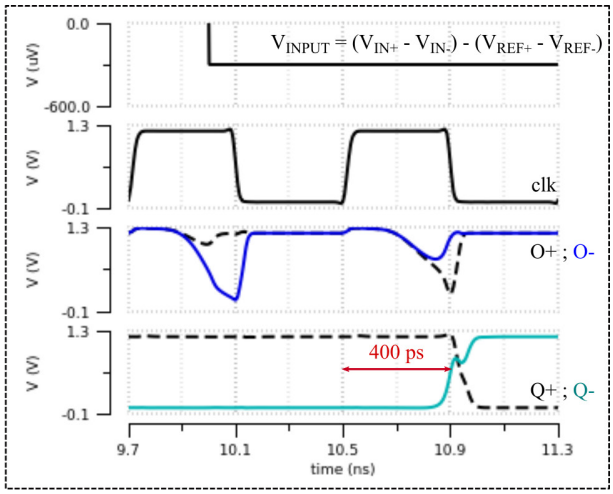


Figure 9: First DFF of the *N*-bit counter (a) symbol (b) circuit-level design.

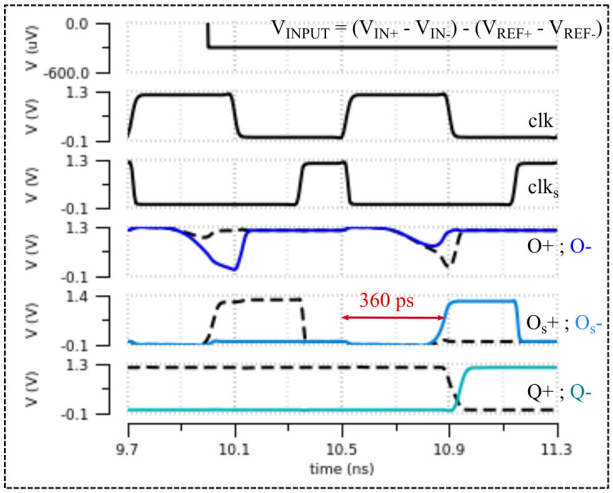
6 Simulation and comparison

To validate the proposed design methodology and evaluate the proposed circuit performances, the proposed two-stage FDDC shown in Fig. 3 has been designed in the TSMC 65 nm CMOS process using standard-threshold MOS devices. The offset calibrating capacitor banks are set to six bits. The basic comparator shown in Fig. 1(b), followed by a NAND-based SR latch is also designed using the same standard-threshold devices and will be used on a comparison basis to show the advantages of the proposed structure.

In the first simulation set, both FDDCs are simulated at room temperature under nominal operating conditions. They are powered by 1.2 V supply voltage and operate at a 1.25 GHz clock frequency. A first DC voltage source is set to -300 µV and connected to the differential input voltage, while a second DC voltage source is set to V_{CM}



(a)



(b)

Figure 10: Transient analysis of the fully differential dynamic comparator (a) basic comparator (b) proposed two-stage comparator.

= 950 mV and is connected to both reference inputs to set V_{REF} = (V_{REF+} - V_{REF-}) to 0 V. Fig. 10 shows the transient analysis results for both comparators. This figure is used to determine the decision time t_{on} for both structures. In Fig. 10(a), the decision time t_{on} of the basic comparator, as defined in (3), is equal to the difference between when *clk* goes high and when the negative output *Q*- of the SR latch crosses the mid supply voltage value (V_{DD}/2 = 600 mV). In this first case, the output *Q*+ and *Q*- transition must happen during the *clk* on-time. Otherwise, the decision could not be made, and the comparator output would be invalid. In Fig. 10(a), *Q*+ transition happens slightly before *clk* transition.

In the proposed circuit, the decision time t_{on} is equal to the comparison time t_c, as discussed in section 3. The comparison time t_c in Fig. 10(b), corresponds to the difference between when *clk* goes high and when the negative output O_s- of the second stage crosses 600 mV. In this second case, O_s- transition must happen during the *clk* on-time. However, since O_s- logic level is maintained during the reset, *Q*+ and *Q*- transition could happen at any time of the clock cycle, even after *clk* transition.

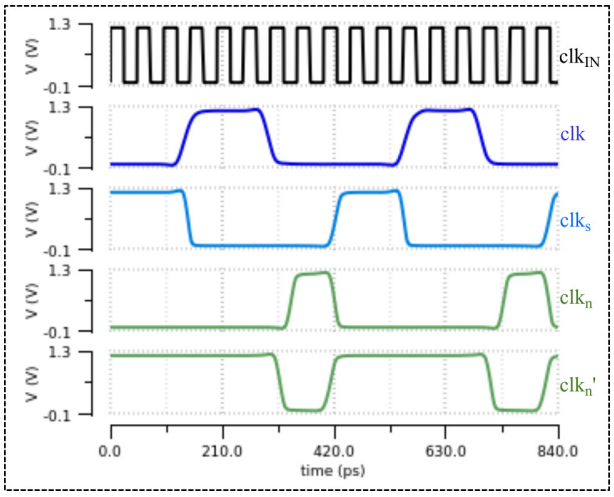
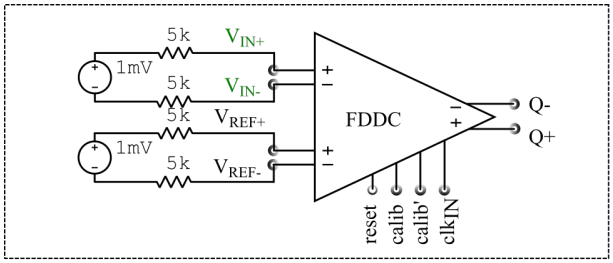


Figure 11: Transient evolution of the generated clocks.

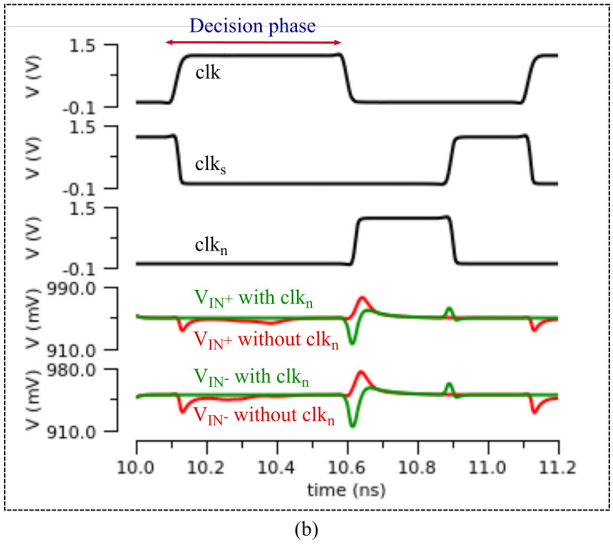
Thus, the decision time t_{on} is equal to 400 ps and 360 ps in the basic and proposed comparators, respectively. The speed improvement of 40 ps in the proposed comparator is then about 10%, as in [3]. However, in [3], the two-stage comparator could not operate properly when powered by voltages equal to 1.2 V and below. The proposed design operation is independent of the technology used, as discussed in section 3.

In the second simulation set, the clock generator shown in Fig. 5(d) is simulated under 1.2 V with a 20 GHz input clock signal clk_{IN}. The results are shown in Fig. 11. In this figure, four synchronized outputs *clk*, clk_s, clk_n, and clk_n' are generated in accordance with the clock diagram of Fig. 5(a). The simulations show that the signal frequency can exceed 2.5 GHz.

In the third simulation set, immunity to kickback noise is simulated using the circuit of Fig. 12(a). In that circuit, the stage preceding the comparator represents the Thevenin equivalent, with a Thevenin resistor R_{TH} equal to 2 x 5 k. The comparator is the proposed FDDC, including switches and the clock generator, as detailed in Fig. 3. To assess the proposed design, simulations are performed with and without noise reduction. The transient evolution of the comparator input signals with and without noise reduction is shown in Fig. 12(b). In both cases, the kickback noise is about a few tens of millivolts. However, compared with the input signals without noise reduction (in red in Fig. 12(b)), input signals with noise reduction (in green) exhibit noise during the reset time only, whereas without noise reduction, noise is present during the entire decision cycle. Although the noise maximum level is not reduced, the circuit remains immune to kickback noise during the decision phase, which is essential to ensure high accuracy.



(a)



(b)

Figure 12: Kickback noise simulation (a) simulation circuit (b) kickback noise at the comparator inputs.

In the fourth simulation set, the offset correction is simulated using the circuit shown in Fig. 13(a). The differential analog input is connected to a triangular voltage source V_{INPUT} = V_{IN+} - V_{IN-} with a slope equal to 1mV/10 ns. The differential reference inputs V_{REF+} and V_{REF-} are connected to a common mode voltage source V_{CM} = V_{REF+} = V_{REF-} = 950 mV.

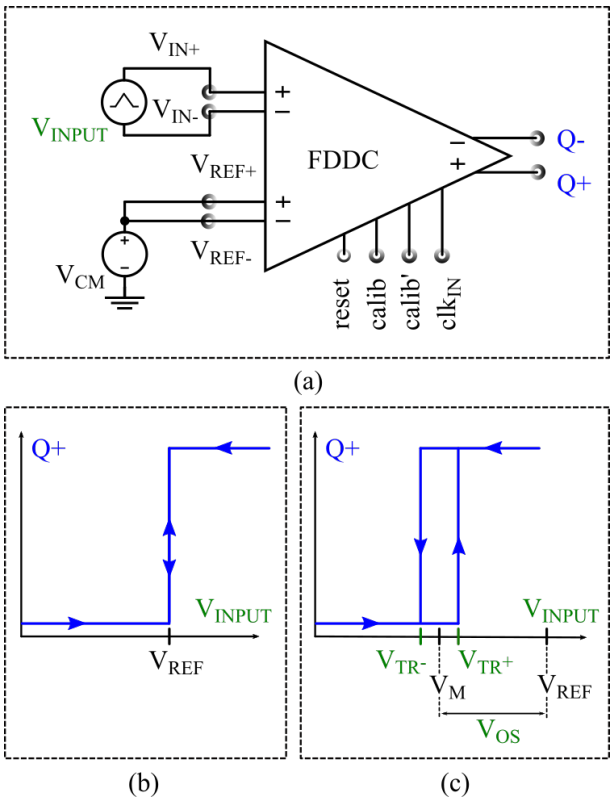


Figure 13: Offset self-calibration simulation (a) simulation circuit (b) ideal transfer characteristic (c) real transfer characteristic.

The differential input voltage $V_{REF} = V_{REF+} - V_{REF-}$ is then equal to 0 V. Thus, considering the two voltage differences, V_{INPUT} and V_{REF}, the ideal transfer characteristic of the dynamic comparator would be similar to the one presented in Fig. 13(b). Here, both hysteresis and offset are null. However, in real conditions, the comparator always exhibits hysteresis and offset [21]. Fig. 13(c) shows the realistic transfer characteristic. The hysteresis window is centered on V_M and delimited by trip points V_{TR+} and V_{TR-}. The offset voltage V_{OS} is defined as the difference between V_M and V_{REF}:

$$V_{os} = V_M - V_{REF} \tag{7}$$

This offset definition is used to evaluate offset voltage compensation using the comparator capacitor banks. Considering the circuit symmetry, simulations can be performed by holding *d+* or *d-* at 1 while incrementing the other from 1 to *N* - 2. In Fig. 14, the offset voltage is determined by holding *d-* at 1 while incrementing *d+* from 1 to *N* - 2 for *N* - 2 clock cycles.

In the fifth simulation set, the operation of the offset regulator FSM shown in Fig. 7(a) is evaluated using the circuit shown in Fig. 15. In this circuit, an offset voltage equal to 50 mV is added in series with a positive comparator input.

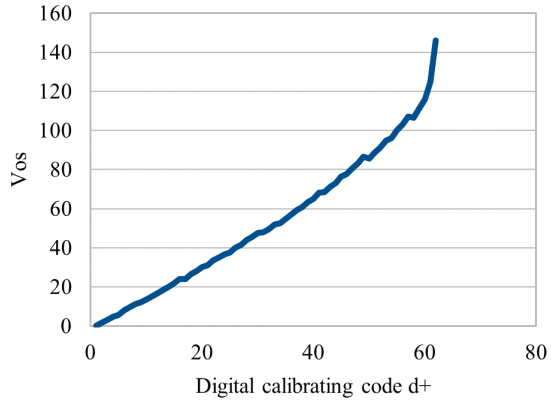


Figure 14: Offset voltage compensation by capacitor banks.

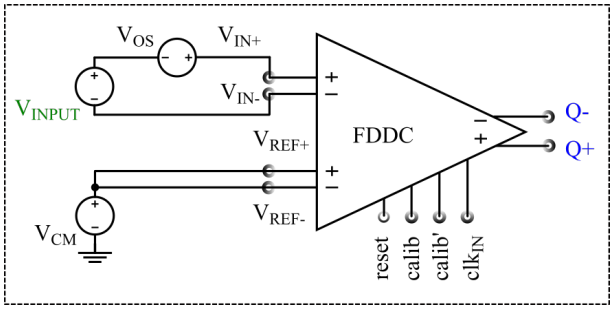


Figure 15: Simulation circuit of the FDDC, including an offset voltage V_{OS}.

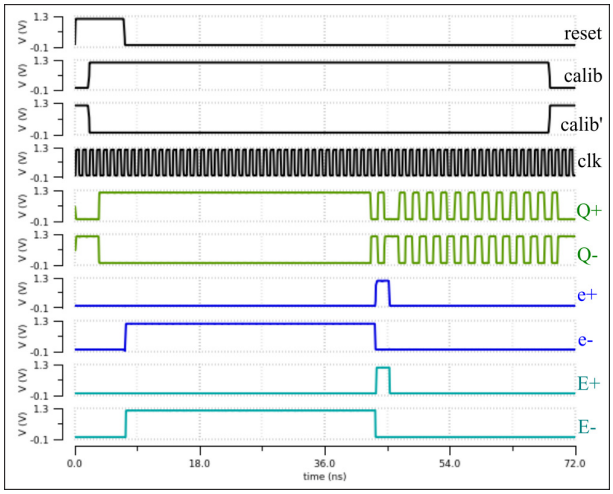


Figure 16: FSM input output signals of the offset regulator when V_{OS} = 50 mV.

Fig. 16 shows the applied input signals *reset*, *calib,* and *calib'*. The reset action initializes both FSM outputs *e+* and *e-* to '0', which corresponds to state S_0 of the FSM shown in Fig. 7(a). Then, with *Q+* and *Q-* equal to '1' and '0', respectively, the FSM outputs *e+* and *e-* become '0' and '1', respectively, which corresponds to state S_1. After 35 clock cycles, *Q+* and *Q-* change to the opposite logic levels, leading *e+* and *e-* to change to '1' and '0', respectively. This change lasts two clock cycles, which corresponds to state S_2 followed by state S_3 in the FSM. After

these two cycles, the outputs *e*+ and *e*- are set back to '0' which corresponds to the FSM last state S_7.

Two signals *E*+ and *E*-, which are identical to *e*+ and *e*-, are also generated. Indeed, because *calib* = 1, an AND logic operation between *calib* and *e*+ and *e*-, as shown in Fig. 6, results in the two signals *E*+ and *E*-. These signals are applied to the enable inputs of two 6-bit counters, leading to two offset calibration control signals *d*+ and *d*-, respectively. Fig. 17 shows the generated control signals, where *d*+ and *d*- are equal to 3 and 37, respectively.

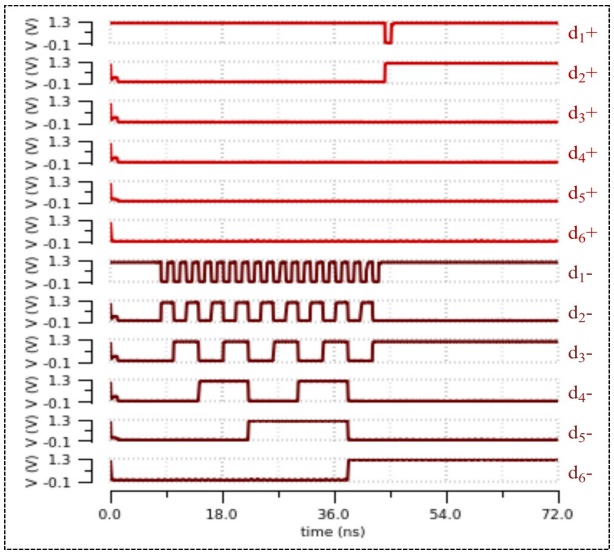


Figure 17: Six-bit offset control signals *d*+ and *d*- when V_{OS} = 50 mV.

In Fig. 18, the trip points V_{TR+} and V_{TR-} are determined as 741 µV and -77 µV, respectively. The offset voltage V_{OS} is determined using (7) and is equal to 332 µV. Thus, the proposed self-calibration method has effectively reduced the offset voltage from 50 mV to a few hundred microvolts.

In the sixth simulation set, the circuit in Fig. 15 is used again with an offset voltage equal to 150 mV to evaluate the maximum offset correction that the designed

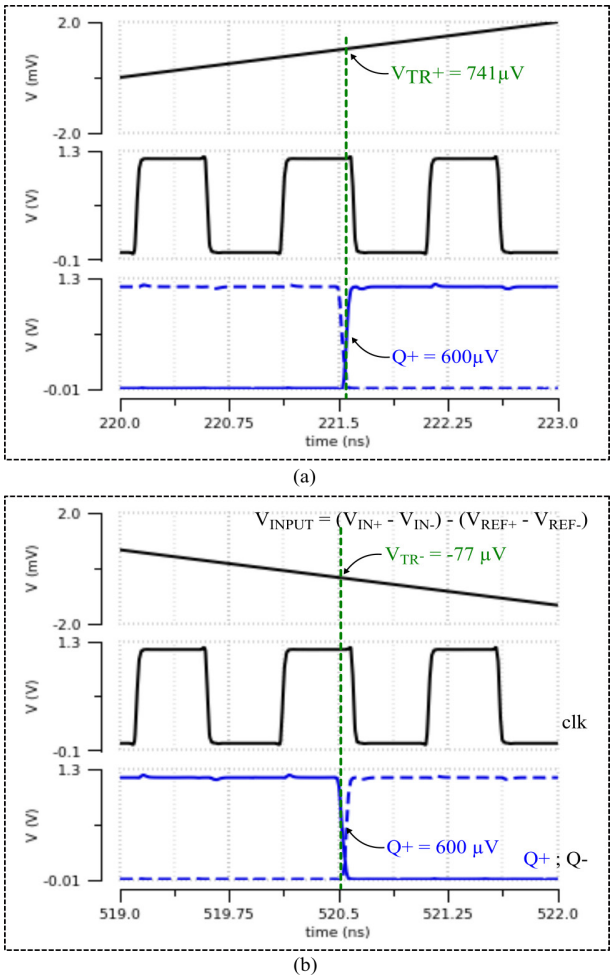


Figure 18: Offset evaluation with V_{OS} = 50 mV (a) trip point V_{TR+} (b) trip point V_{TR-}.

system could achieve. Fig. 19 shows the resulting offset regulator FSM outputs. The system goes through states S_0, S_1, S_2, and S_3. However, the control signal *calib* is set to '0' before the FSM reaches state S_2, that is, before *Q*+ and *Q*- change to the opposite logic levels. Indeed, the control signal *calib* is used to disable the counter incrementation when it reaches 2^N-2, as discussed in section

Table 1: Summary and comparison of the characteristics of fully differential dynamic comparators.

Parameter	2002' [8]	2014' [23]	2016' [22]	2017' [24]	2018' [25]	This work
Process	CMOS 350 nm	CMOS 90 nm	CMOS 40 nm	CMOS 180 nm	CMOS 180 nm	CMOS 65 nm
Topology	Diff. pair	4-inputs	Diff. pair	Diff. pair	Diff. pair	Diff. pair
Meas/Sim	Measured	Simulated	Measured	Simulated	Simulated	Simulated
Offset regulation	No	No	No	Analog	No	Digital
V_{OS} range/max (mV)	80	33	-	±1	±5	±9
Kickback noise during decision (mV)	-	1	-	0.45	-	≈0
Comparison rate (GHz)	0.1	1	3.33	0.5	1.3	1.25
Power (µW)	580	51	2100	373	265	213
Energy/Comp. (fJ/comp)	5800	51	630.63	746	203.85	170.4

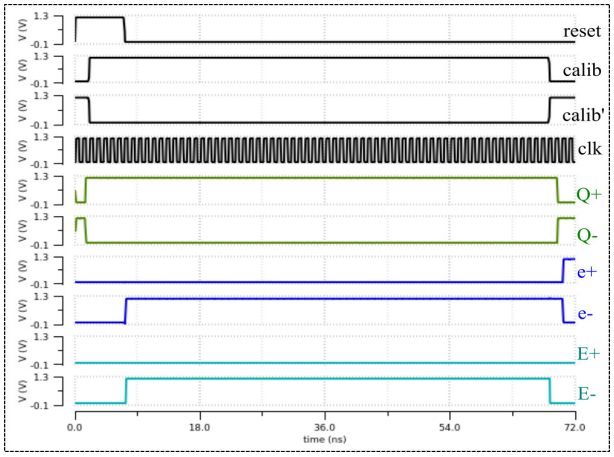


Figure 19: FSM input output signals of the offset regulator when V_{OS} = 150 mV.

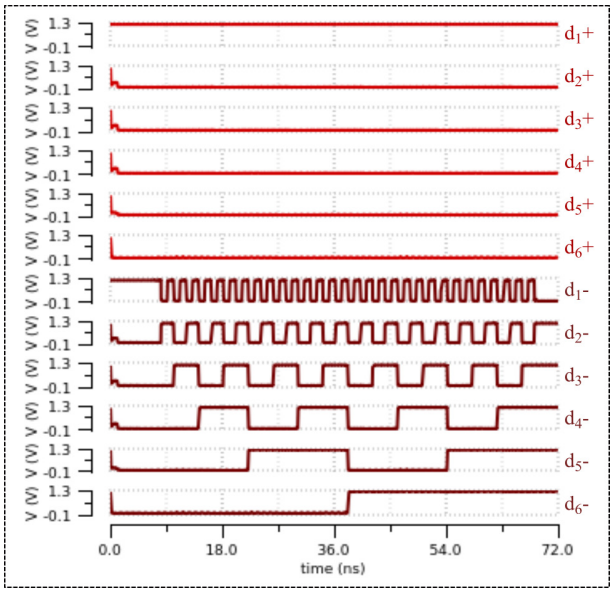


Figure 20: offset control signals *d+* and *d-* when V_{OS} = 150 mV.

5. Therefore, the enable signal *E-* is no longer identical to *e-*. Fig. 20 shows the resulting counters outputs *d+* and *d-*, which are equal to 1 and 62, respectively.

Fig. 21 is used to determine the maximal offset correction. The obtained offset voltage after correction is 4.33 mV. Thus, the system can achieve a maximal offset correction of 145.67 mV.

In the seventh simulation set, the offset voltage is determined while considering the process and mismatch variations. Fig. 22 shows the offset variation of the designed FDDC under mismatch variation with and without offset calibration with a 100-run Monte Carlo simulation. Without offset calibration, the offset voltage V_{OS} has a maximum variation of ±160 mV. This offset is reduced to ±9 mV after calibration.

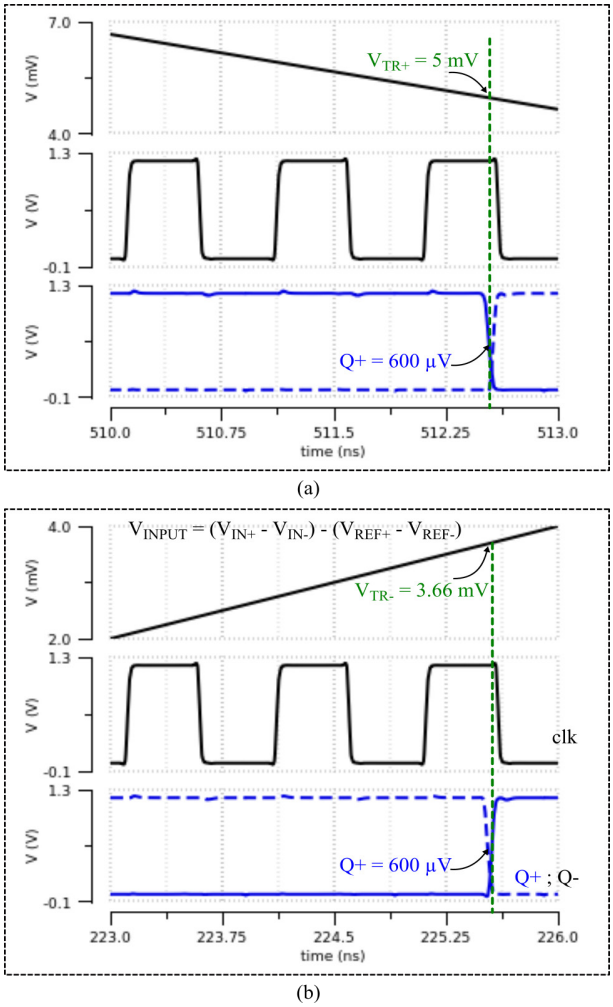


Figure 21: Offset evaluation with V_{OS} = 150 mV (a) trip point V_{TR+} (b) trip point V_{TR-}.times.

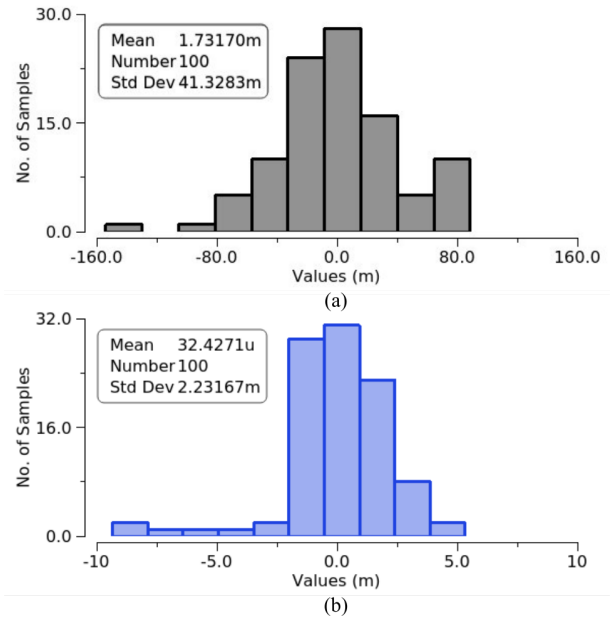


Figure 22: Monte Carlo simulation of the offset voltage (a) without calibration (b) with calibration.

The proposed design achieves an effective self-calibration of the offset voltage. The standard deviation is reduced from 41.3 mV to 2.23 mV after calibration, resulting in a decrease of more than 18 times. The offset correction can be improved by increasing the channel length of the calibration transistors, as discussed in [3], or by increasing the number of charges in the capacitor banks.

The proposed design performance is summarized in Table. 1. This table also presents the performance achieved in current related works on FDDCs. The proposed design is the only one that includes offset calibration and noise cancellation in FDDCs. It achieves the second-best energy efficiency after a 40 nm CMOS design [22]. However, in [22], no offset regulation is proposed, which would increase the consumed power and decrease the operation speed.

7 Conclusions

The current paper presented a new and effective methodology design for FDDCs, including kickback noise immunity and offset self-calibration. In the proposed design, the kickback noise is almost null during the decision phase and less than 40 mV during the reset phase. Moreover, the proposed FDDC achieves an effective digital offset self-calibration, in which the offset voltage is reduced more than 18 times. The proposed circuit is designed with minimalist building blocks and consumes no more than 213 µW at a 1.25 GHz comparison rate. It achieves high performance compared with the current state-of-the-art achievements in terms of offset calibration, noise cancellation, operation speed, power consumption, and design simplicity. Moreover, the proposed design methodology is generic and independent of the technology used.

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Towards Smaller Single-point Failure-resilient Analog Circuits by Use of a Genetic Algorithm

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Abstract: Failure-resilient analog circuits are difficult to design, but artificial intelligence can help crawl the topology solution space. Using evolutionary computation-based topology synthesis we evolve analog arcus tangent computational circuits, resilient to any rectifying diode or resistor high-impedance single failure or removal. We encode analog circuit topologies as individuals with an upper-triangular incident matrix. Circuits are evolved using a combined technique utilizing parts of NSGA-II and PSADE, based on a special three-dimensional robustness function. We show that topology size for a failure-resilient circuit can be classes smaller than hand-made component-redundancy-based solutions. Our best failure-resilient topology comprises six diodes, three resistors, and a voltage offset source.

Keywords: analog circuits, analog circuit synthesis, circuit optimization, failure-resilience, circuit robustness

Manjšanje analognih vezij odpornih na odpoved poljubne komponente z uporabo genetskega algoritma

Izvleček: Analogna vezja, ki so odporna na napake, je težko načrtovati. Pri prečesavanju prostora možnih topologij lahko pomaga umetna inteligenca. Z sintezo topologij, temelječi na evolucijskem algoritmu, smo razvili analogno računsko vezje za inverzni tangens, ki je odporno na visokoimpedančno okvaro posamezne komponente (diode ali upora) ali njene odstranitve. Topologija analognega vezja je v algoritmu zapisana v obliki zgornje-trikotne vpadne matrike. Vezja razvijemo z uporabo kombinirane metode z uporabo večkriterijskega optimizacijskega algoritma NSGA-II in PSADE, kjer je za usmerjanje sinteze razvita posebna tri-kriterijska funkcija robustnosti. V članku prikazujemo kako zmanjšati velikost topologije, odporne na odpoved komponente, na razrede manjšo velikost od ročno izdelanih robustnih topologij, ki temeljijo na redundanci posameznih komponent. Naš najboljši rezultat je analogno računsko vezje za inverzni tangens, ki je sestavljeno iz šestih diod, treh uporov in odmičnega napetostnega vira.

Ključne besede: analogna vezja, sinteza analognih vezij, optimizacija vezij, odpornost na napake, robustnost vezij

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1 Introduction

Design of an analog circuit is a challenging task, especially when the product has to meet high standards and fulfill tough requirements.

Designers often use various simulation tools to predict temperature, humidity, and electromagnetic behavior during circuit operation. Furthermore, to predict the blueprint manufacturability and maximize the production yield, they also use statistical methods, such as Monte Carlo analysis [1].

However, customer requirements might get even harder. When a device is targeted for use in harsh conditions (i. e., space exploration, aeronautical missions, automotive, robotics), we expect the product to be robust against extreme temperature swings, high ionizing and electromagnetic radiation levels, high working currents, and more. That kind of stress can lead to component faults and premature device failure. Furthermore, failed components in remote and unmanned missions could not be replaced easily.

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Researchers have already focused on hardening electronic devices against failures per se [2]. The classical ways of doing that include component redundancy, overdesign, shielding and insulation, thermal management, and so on. Most of the time such solutions significantly increase the size, weight, and finally, the cost of the device. The upper methods usually aim to protect every circuit component as if it was the main breaking point of the system.

Researchers have already proposed systems resilient to failures that occur in vivo. Meaning, the circuit has the ability to persist functional when one or more components fails during the circuit operation [3]–[6]. Such systems usually utilize duplicated circuit modules to form redundant sub-systems which are controlled by various voting mechanisms [3], [7]. However, the demultiplexer then becomes the weak part of the system.

This paper shows an alternative method of evolving failure-resilient analog circuits. Using an intensive evolutionary search, we can find novel analog circuit topologies that exhibit robustness to *any* electronic component (semiconductor diode or resistor) high-impedance failure or removal, without a dedicated active demultiplexing system.

We show in this work, that by using an evolutionary topology synthesis tool, we can greatly reduce the size and the number of needed components to achieve failure-resilience of an analog circuit, compared to canonical hand-made design.

To the best of our knowledge, this is one of the few published works on the automated synthesis of a priori robust, failure-resilient nonlinear computational analog circuits [3], [4], [8]–[15], and also one of the first attempts of redundancy reduction by using evolutionary search.

The paper is organized as follows. We summarize previous work on robust topology synthesis in Section 1.1 and describe our motivation in 1.2. We describe the applied topology synthesis technique in Section 2. Results are given in Section 3, summarized in 3.8 and concluded in Section 4.

1.1 Previous work

The discovery of novel circuit topologies has been done by hand for over a century. This is changing with the availability of novel tools, relying on artificial intelligence [16]. Since the beginning of this research area [17]–[19], computer-aided circuit synthesis has become human-competitive and trustworthy for fabrication [16], [20]. We believe, rather than replacing a human expert in the industry, AI might help in the rapid exploring of undiscovered topology space, thereby helping and speeding up the design process.

Reviews of existing analog circuit synthesis techniques can be found in existing literature [21], [22]. However, we give a brief overview of existing topology synthesis efforts for extremely robust and failure-resilient analog circuits below.

1.1.1 Synthesis method

Analog topology synthesis is an extremely non-linear and complex task, which is why most existing approaches in this field search topology with a method, based on the Darwinian selection of the fittest, i.e. evolutionary or genetic algorithm.

Somehow special are the works of Zebulum and Keymeulen, et. Al., who presented an evolutionary algorithm that is being run on the controlling unit of the circuit under failure, in vivo [4], [12].

Evolutionary methods demonstrate a capacity to tackle unconventional challenges. One compelling reason that supports the continued relevance of evolutionary computation, even when compared to neural networks like GNNs, is that they do not always require prior training to align with the defined cost function.

However, emerging tools rooted in GNNs, like CktGNN, showcase impressive capabilities in generating robust circuit topologies [23].

1.1.2 Synthesis goals and degrees of robustness

Passive filters are usually the entry point for showing the performance of analog circuit synthesis tools. Most of the works on failure-resilience also experimented with the synthesis of robust passive analog filter circuits, dealing with various degrees of component faults. Resistor/capacitor/inductor removal was considered in [9], [15], while in addition [3], [7] also studied the complexity of partial and full short-circuit and high-impedance faults. Studies [24]–[27] only considered R/L/C parameter perturbation without full component failure.

Other authors reported syntheses of

- compensator circuit [8] and
- inverter, amplifier, and oscillator [13] resilient to bipolar transistor removal,
- PID controller with R/L/C removal resilience [10],
- transistor-fault resilient amplifier [11],
- half-wave rectifier, NOR gate, and voltage-controlled oscillator for extreme temperature swings (in situ evolution) [12]

- XNOR gate, analog multiplier, and inverter resilient to arbitrary faults in the controlling unit FPTA (Field Programmable Transistor Array) [4]
- the natural logarithm and square-root analog computational circuits resilient to semiconductor diode short-circuit or high-impedance malfunction [28]

1.2 Motivation

1.2.1 Failure-resilience

For this work, let us define failure-resilience as an analog circuit topology property, where any of the basic components (diode or resistor) can be removed or replaced with high-impedance failure, with the circuit showing minimal-to-zero deformation of nominal signal processing abilities. The voltage source and the 10 k Ω input-pullup resistor are excluded from the definition.

The methodology incorporates various failure scenarios using specialized "failure-defining" Spice models, as demonstrated in our prior work [28], where we successfully synthesized analog circuits resilient to both high-impedance and short-impedance failures in semiconductor diodes. In this paper, we primarily concentrate on minimizing topologies that are fully resilient to high-impedance failures. However, due to high computational costs, we do not address short-circuit failures for all component types in this paper; this topic is left for future research.

1.2.2 Size of failure-resilient circuits

Failure-robustness comes with a cost. It is generally paid by (often significantly) higher total number of needed components for the same nominal task as a non-robust circuit would perform. For a system to survive such rigorous change, as one or any component removal/failure, redundant elements and connections must be available in the system.

Let us consider an example of a non-linear, computational analog circuit from Figure 1. The circuit outputs an inverse tangent of input voltage signal between 0 and 10 V. It is a hand-designed linear voltage divider, with diodes used to switch between five linear segments, which closely interpolate the mathematical function [29]. Due to its simplicity, the topology is often used instead of the amplifier-chain summing circuit. If any of the components in the dotted square (except for the voltage source) fails (or is removed), the circuit's transfer function severely changes as seen in Figure 2 with absolute error range plot and Figure 3 with relative error plots.

The most common and straightforward approach to achieving failure-resilience property is to introduce redundancy on a single-component level. In the case of an arctan circuit, every diode has to be paired in parallel and every resistor has to be (at least) tripled in parallel. Two diodes in parallel give a sub-circuit where, theoretically, any of the two diodes might enter high-impedance failure without transfer function transformation. Single resistor with resistance R_n has to be replaced with three parallel resistances 3 R_n to maintain 33% relative error of sub-circuit in case of one resistor entering high-impedance failure.

Figure 4 shows a hand-designed topology that fulfills the failure-resilience criteria. Fair nominal response and narrow error range in failure cases are presented in Figure 5 and Figure 6. Evidently, the circuit topology hence the number of needed components goes off-scale. While the nominal non-robust topology includes 10 resistors and 5 diodes (excluding the input resistor, see 1.2.1), the hand-made robust version comprises 30 resistors and 10 diodes. In CMOS technology, for example, resistors occupy large chip areas [30]. In addition, those resistances are multipliers of the nominal values, which further multiplies the needed area for fabrication. The circuit total cost would be above comparison to the nominal non-robust version.

However, novel studies of analog topology synthesis imply, that number of needed components for failure-resilience might somehow be lower than expected in hand-made designs [3], [7]. The possible reason for that phenomenon is that open-ended topology synthesis allows component-level redundancy to be replaced with system-level redundancy.

1.2.3 Topology size as a synthesis constraint

In this study, we explored the lower limits of topology size for a failure-resilient computational analog circuit. We show, that for the arcus-tangent circuit, the topology could be reduced from 40 critical components in hand-made design down to 8 components by evolutionary-based synthesis. This also has fewer components than used hand-made non-robust design (15).

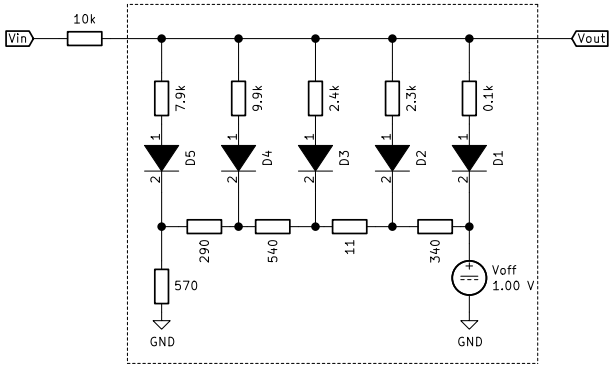

Figure 1: Canonical hand-designed piece-wise linear arctan computational circuit topology.

Our study provides step-by-step size-reducing results for further investigation and a better understanding of underlying mechanisms.

Primary contribution of this paper lies in the demonstration of a novel application of evolutionary methods, resulting in the attainment of system robustness that has not been observed in any existing systems or circuits within the literature.

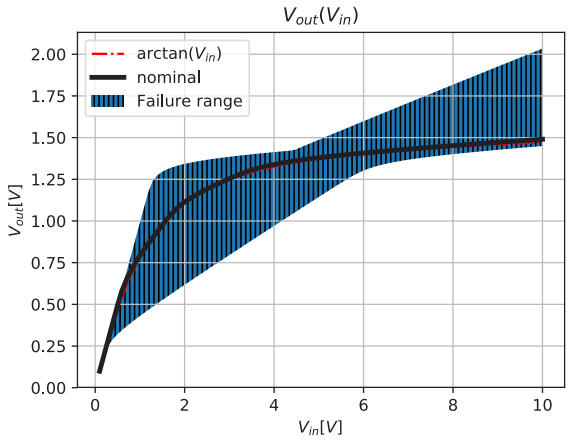

Figure 2: Hand-designed non-robust arctan circuit: nominal response (black) completely covers the arctan function. The range of various failure responses is given in blue.

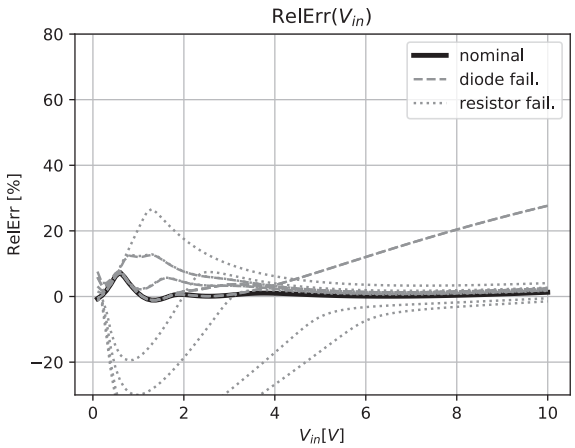

Figure 3: Relative error curves of nominal (solid) and component failures (dotted and dashed).

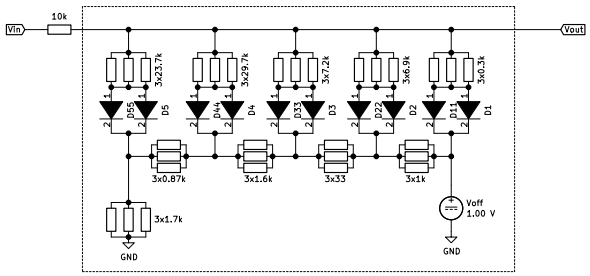

Figure 4: Hand-designed piece-wise linear arctan computational circuit, robust to any single component high-impedance failure or removal.

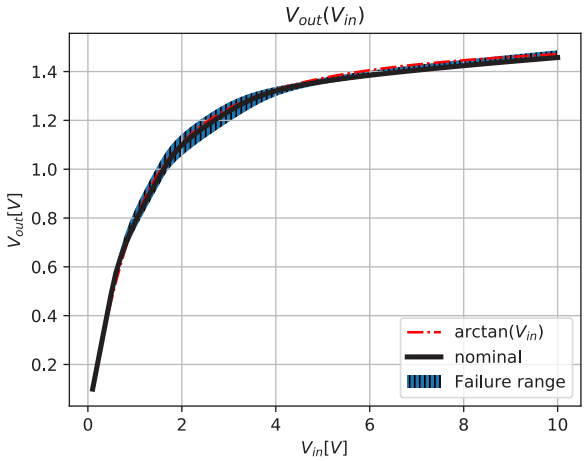

Figure 5: Hand-designed failure-resilient arctan circuit: nominal response (black) covers the arctan function. The range of various failure responses is given in blue.

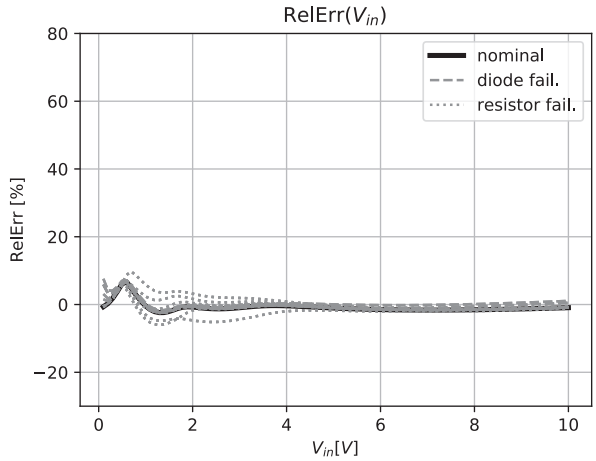

Figure 6: Hand-designed failure-resilient arctan circuit: relative error curves of nominal (solid) and component failures (dotted and dashed).

2 Methods

In this section, we provide details of the methods used in this circuit synthesis. The applied approach is mostly based on [28].

2.1 Analog Circuit Representation

Upper-triangular incident matrix is a well-proven method of encoding an analog circuit topology [22], [28], [31]. It is based on a fixed set of available component terminals. Each building block can comprise one or more input/output terminals (see Figure 7). Usually, the building-block terminals are located on the left side of the fixed set, and outer connections are located on the right-side of the set. The set is then mirrored in two dimensions, forming a connection matrix, where the logical one represents an existing zero-impedance

connection between the terminals on both axes. The matrix is filled with logical ones on a diagonal so that by definition, every terminal is connected to itself. Only the upper matrix triangle is used to exclude half of the redundant mirror connections from the bottom triangle, to reduce the effective matrix size, without sacrificing any topology search space [31], [32]. Additionally, in the inner-connections sector of the matrix, we allow every possible connection, while in the outer-connection section only one positive logical value is allowed per line, filtering-out any connections between outer terminals.

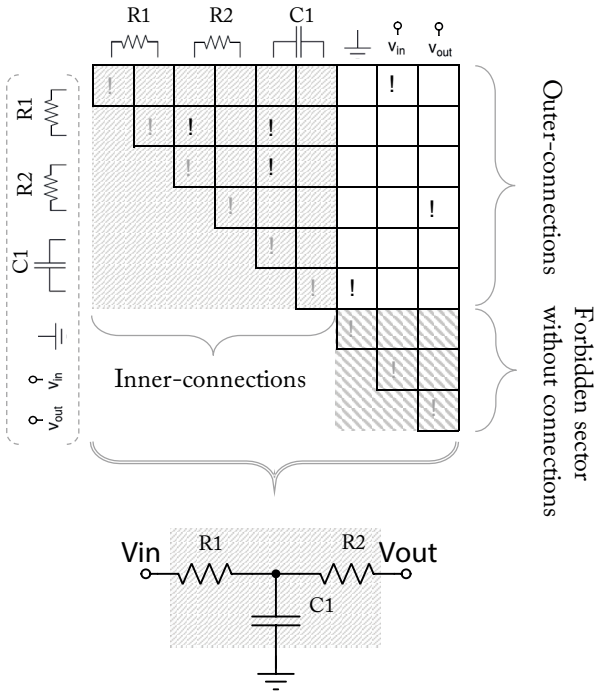

Figure 7: An example of an upper-triangular matrix, representing a simple T-shaped analog circuit topology [31].

Components with adjustable parameters (i.e., resistances, capacitances, transistor widths and lengths, etc.) have their values organized in a separate array, called value vector. While the topology matrix is purely binary, the value vector is a numeric entity.

2.2 Genetic Reproduction and Sizing

For evolutionary computation and mimicking natural genetic reproduction, we use the topology-matrix crossover technique, described in [31]. Every terminal is connected to other terminals via the logical values that reside on a column and a row, intersecting the diagonal element, that represents the connection to itself. By exchanging the two lines of the matrix with another topology matrix, the information of the terminal connecting with the rest of the circuit is transferred. Figure 8 shows two examples of newly-created offspring with one terminal (N=1) and three terminal (N=3) information being exchanged. Note that in the applied algorithm, the number of exchanged terminal connections N is a randomly-chosen number from the set {1,2,3}.

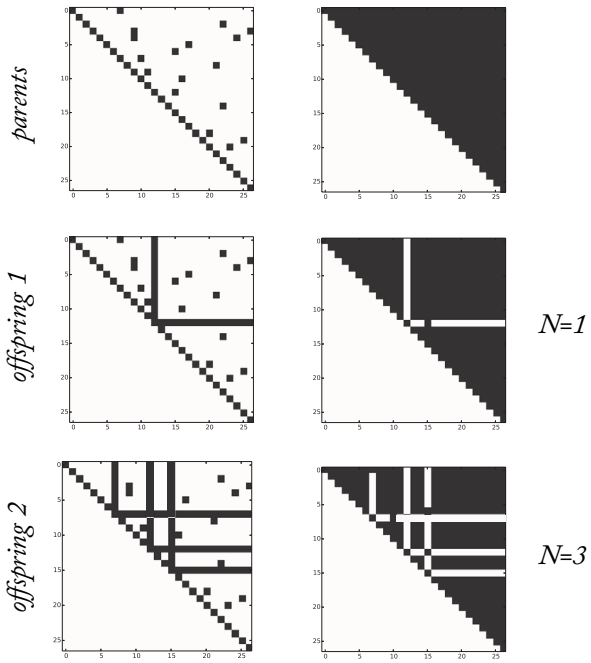

Figure 8: Topology crossover examples. For better illustration, parent no. 2 is a full upper-triangular matrix [31].

The value vector is being optimized using two different methods. The first one is a reproduction mechanism, inspired by a well-known intermediate crossover [33]. The choice between topology-matrix or value-vector crossover is initiated by the evolutionary algorithm. In one case offspring will inherit a modified topology and in another a modified parameter.

Another parameter tuning technique in this work is an established PSADE (Parallel Simulated Annealing and Differential Evolution) [34]. Due to its computational expensiveness (yet effectiveness), it is triggered only every 10th generation on one to three best individuals.

2.3 Fitness function

The fitness function should encompass the desired properties of the circuit. Additionally, it should filter out individuals with unwanted properties and help to guide the searching algorithm through the valley of local minima. We will briefly review the applied fitness function below, but the full justification of chosen criteria is given in [28].

In the case of open-ended topology synthesis, the fitness function definition is rather complex and com-

prises several stages. The first is an evaluation of the circuit's transfer function, i.e. signal processing quality, using a DC analysis in Spice simulator. In the case of arctan circuit design (let us denote the mathematical function as *g*) we calculate the root mean square error (RMSE) between V_{out} (V_{in}) and $g(V_{in})$. We call the result *fitness* and denote it as *f*.

Calculation of failure-resilient circuit fitness needs to be carried out for every predicted failure scenario. In our work, failure-resilience is defined as the high impedance failure of any resistor or semiconductor diode (see 1.2.1). In the case of 30 resistors and 10 diodes, the total number of RMSE calculations must be 41 – that is one for nominal (no failure) scenario f_{nom}, and 40 for every critical device failed, multiplied by the number of failure types considered (only one failure type in this case). Vector ***f*** comprises all RMSE results:

$$\boldsymbol{f} = \left[f_{nom}, f_{1,1}, \ldots, f_{1,F}, \ldots, f_{N,F} \right] \tag{1}$$

where N is the total number of critical components and F is the total number of failure types [28].

Failure-resilient circuit evaluation is carried out in multiple dimensions, and forms a three-dimension robustness vector ***r***:

$$\boldsymbol{r} = \begin{bmatrix} f_{nom} \\ f_{\max} \\ \sigma_f \end{bmatrix} \tag{2}$$

where f_{nom} is RMSE result of no-failure, nominal circuit topology, f_{max} is the maximum of vector ***f*** and α_f is the standard deviation of the same vector [28]. Vector ***r*** gives insight into a single failure-resilient candidate

- nominal performance
- performance in case of worse single-point failure and
- statistical failure scattering.

This separation gives a chance to the NSGA-II algorithm to non-dominantly sort the individuals into Pareto-fronts and by that maintain the genetic diversity, thus avoiding premature convergence.

In the specific case of a failure resilient circuit synthesis, a practitioner might encounter a *false-robustness* phenomenon, which we explain below.

Let us consider an example of a simple diode half-wave rectifier (Figure 9, left). If D0 fails or is removed, the rectifier is no longer working, and statistically, one critical component (diode) makes a 100% chance of circuit failure. Imagine a topology modification, that would harden the circuit against the D0 removal or high-impedance failure. Let us have four additional diodes to fulfill that requirement (one would be enough, but we assume the search algorithm does not know that). The search algorithm can encounter a topology with four diodes with no effect on the nominal transfer function (example in Figure 9 (right)). Still, if D0 fails, the circuit does, too. However, if any of D1-4 fails, the circuit still delivers the transfer function. It appears as only 20% of critical components (diodes) cause a fatal scenario for the circuit. The latter circuit might get promoted because of its better "robustness" value. Obviously, this is not the case, because D1-4 are not electrically connected and do not play any role in signal processing. That kind of circuit has to be ranked out since it does not contribute to real circuit robustness.

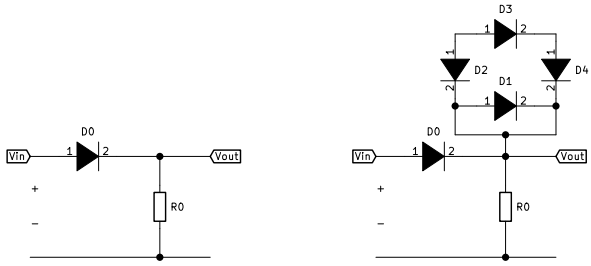

Figure 9: False-robustness problem [28].

Inclusiveness [28] successfully unfolds the false-robustness problem. Using modified diode models and SPICE simulator commands we determine which of the components are electrically connected (*included*) and have an effect on signal processing. Inclusiveness (denoted by *I*) is calculated as a ratio between the number of all critical and included components. Having an updated robustness definition:

$$\boldsymbol{r} = \begin{bmatrix} f_{nom} \\ f_{\max} \\ \sigma_f \end{bmatrix} I \tag{3}$$

circuits with greater inclusiveness are promoted over the circuits with floating or flawed connected components. However, this can lead the synthesis to build larger circuits with excessive redundancy, so component number limits must be set elsewhere in the algorithm. In our case, the top number of available devices is set in the pre-defined component set, which also defines the topology-matrix size. Note that only the inclusiveness of diodes was considered in our work.

2.4 Synthesis algorithm

The search and sorting algorithm utilize major ideas from NSGA-II [35].

The evolutionary algorithm is initiated by a randomly generated population. Then every individual is evaluated according to the fitness/robustness from Section 0. Sorting is performed in three steps, following NSGA-II. In the first step, individuals that do not dominate each other (are not beaten in any combination of objectives) are assigned to a front (i.e. Pareto front). The remaining individuals are put in a second, third, etc., front, with the same non-dominance criteria. A new generation assembly is the second step. We aggregate the new generation starting with individuals from the 1st front, and continue with available individuals from further fronts. Because a union of parents and offspring is usually larger than available space in the new generation, there is a front of individuals, that does not fit as a whole to the new generation. A selection between non-dominated individuals needs to be undertaken. This is done in the third step, the crowding distance calculation. The crowding distance is the distance between two neighboring points (i.e. individuals) along each of the objective axes. Ranking individuals with higher crowding distance helps to a more even distribution in a front of individuals.

After the assembly of the new generation, a parent selection process takes place. With the tournament, some randomly selected individuals are chosen from the generation. The selected individuals compete based on their front number (lower is better) and crowding distance (higher is better). Two tournaments take place to choose two future parents.

Having selected two parents, their genetic material gets reproduced. This can be done by mating their genetic material as in 0 or by mutating it. Control over mating/mutation is a statistical probability, set at the beginning of the algorithm. Similarly, a probability parameter controls whether the topological or parametric part of the gene will be mated/mutated.

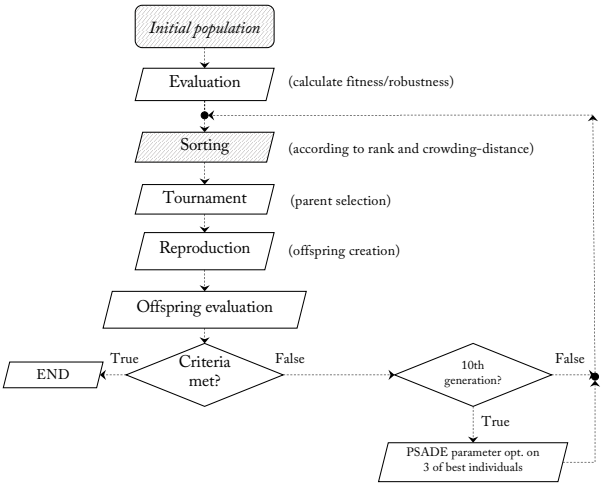

Figure 10: The applied evolutionary algorithm flowchart [31].

We repeat the synthesis algorithm until at least one of the stopping criteria (i.e., design requirements, max. number of generations, timeout.) is met. When ten generations have passed, we run a PSADE [34] parameter optimization on three of the best circuits from the population and thus fine-tune the ambitious individuals.

Figure 10 summarizes the main synthesis algorithm steps.

2.5 Finding minimal topology

Our objective was to evolve circuits with consistent performance even if devices are removed. Initially, we aimed to incorporate as many "redundant" components as possible. However, circuit size doesn't always reflect actual functional contributions, leading to "dummy" or electrically connected but non-functional components.

To address this, we introduced "Inclusiveness" to prevent circuits dominated by dangling sub-circuits, enhancing evolutionary outcomes. Individuals with greater inclusiveness measure propagate more effectively. Our experimentation revealed a paradox when maximizing redundancy while minimizing circuit size simultaneously. Hence, we perform separate stages for minimizing and maximizing circuit schematics. We are listing two more reasons, why the size of circuit schematics is not another objective of NSGA-II search.

Our topology representation method using an upper-triangular incident matrix limits arbitrary extensions during evolution runs. Varying matrix sizes in the evolutionary pool cause inconsistent crossovers and mating patterns.

The third concern relates to the computational complexity of NSGA-II and evaluating circuits under different failure scenarios. A variable maximum component number during evolution would increase computational effort, impacting NSGA-II's performance and circuit robustness evaluation. As a result, we chose not to experiment with variable component numbers to minimize computational burden.

3 Results

Our experiment comprised eight independent topology searches. For each synthesis we predefined the set of available components, that is N_d diodes and N_r resistors that are subject to possible high-impedance failure. V_{off} and a R_{in} input resistor (the latter was non-optional) were also available with each synthesis but were excluded from failure consideration.

The main part of the experiment was discovering the possibilities of finding topologies with fewer components than in hand-designed examples (e.g., from Figure 4), that perform arcus tangent analog calculation and exhibit the failure-resilience property (1.2.1).

The genetic algorithm parameters were fixed through the experiment and are summarized in Table 1.

Table 1: Genetic algorithm properties.

Parameter	Value
Population	1000
Tournament	3
Mating prob.	0.6
Topology reproduction prob.	0.8

Resistance values were limited to the range between 10 and 100 kΩ, and voltage source with DC range of 0 to 6 V. Every synthesis was conducted on an i9 HP desktop, utilizing 16 computational threads on 8 processor cores.

3.1 Synthesis with a max of 12 diodes, 12 resistors

With the ambition to cut the number of needed components for the circuit, we gave the first upper limit of Nd_{max} = 12 and Nr_{max}=12. This is already a significant cut of the total number of components (Nd + Nr) in comparison to hand designed example from Figure 4 which comprises 40 components. The algorithm can, however, synthesize a topology with fewer elements.

Starting with a random population, without any prior knowledge available in the population itself, we let the combined NSGA-II algorithm run for 306 generations

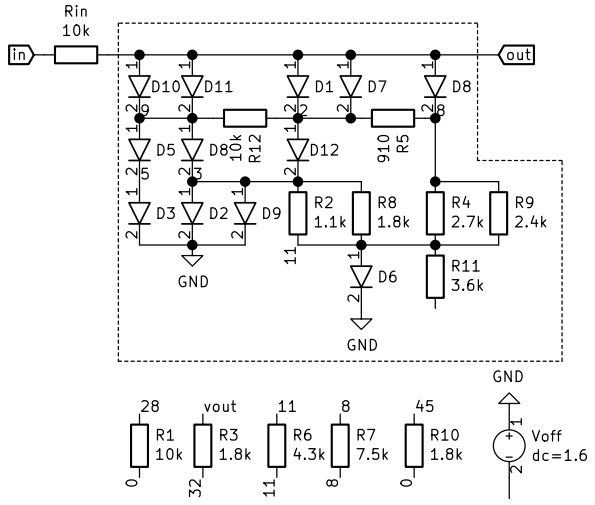

Figure 11: Synthesized arctan computational circuit (Nd_{max} = 12, Nr_{max} = 12), robust to any single component high-impedance failure or removal.

(roughly 15 hours). The outcome is presented in Figure 11. The final topology comprises all 12 available diodes. Some resistors were excluded from the final topology since they do not have any signal-processing effect (such as short-connected resistors, or resistors connected to simulator-helper nodes). The voltage source was also not included in the final design. We excluded some of the components already from topology schematics in Figure 11.

We summarize the circuit performance in three parameters: nominal topology RMSE is 0.312, the worst failure RMSE is 0.370 and the standard distribution of all cases (nominal and failures) is 0.026. One can visualize those results in Figure 12 and Figure 13.

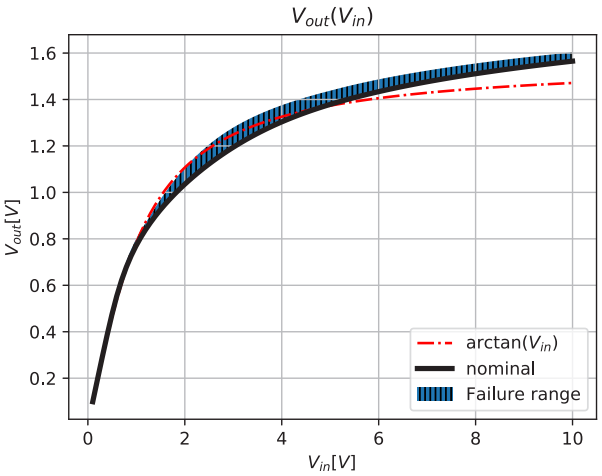

Figure 12: Synthesized arctan computational circuit (Nd_{max} = 12, Nr_{max} = 12): nominal response (black), arctan function (red, dashed-dotted). The range of various failure responses is given in blue.

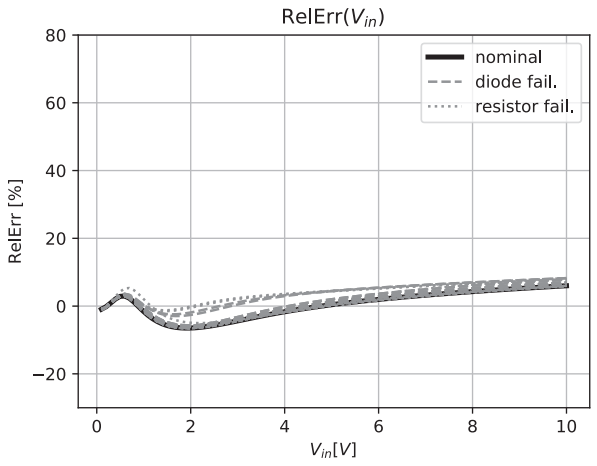

Figure 13: Synthesized arctan computational circuit (Nd_{max} = 12, Nr_{max} = 12): relative error curves of nominal (solid) and component failures (dotted and dashed).

Together with a voltage source, six available resistors were not used in the final circuit. That is why we con-

ducted our experiment with tighter device component limits.

3.2 Synthesis with a max of 10 diodes, 10 resistors

The next synthesis was limited to Nd_{max} = 10 and Nr_{max}=10. We stopped the algorithm after 822 generations (that was after 33h).

The outcome is presented in Figure 14. The final topology comprises all 10 available diodes. Two resistors were not included in the final topology.

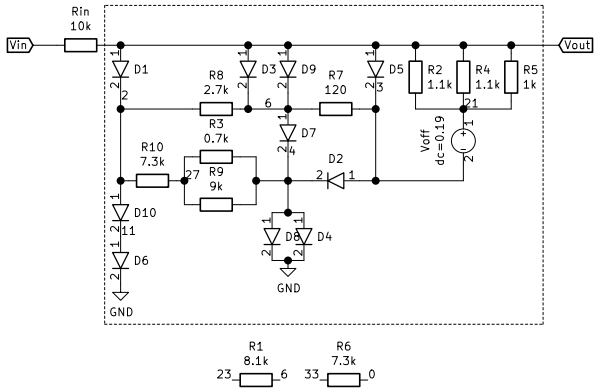

Figure 14: Synthesized arctan computational circuit (Nd_{max} = 10, Nr_{max} = 10), robust to any single component high-impedance failure or removal.

Circuit performance: nominal topology RMSE is 0.158, the worst failure RMSE is 0.270 and the standard distribution of all cases (nominal and failures) is 0.032. One can visualize failure ranges in Figure 15 and Figure 16. This circuit performs better than the one from the previous synthesis, according to the three observables. It also comprises 2 diodes less and four resistors more.

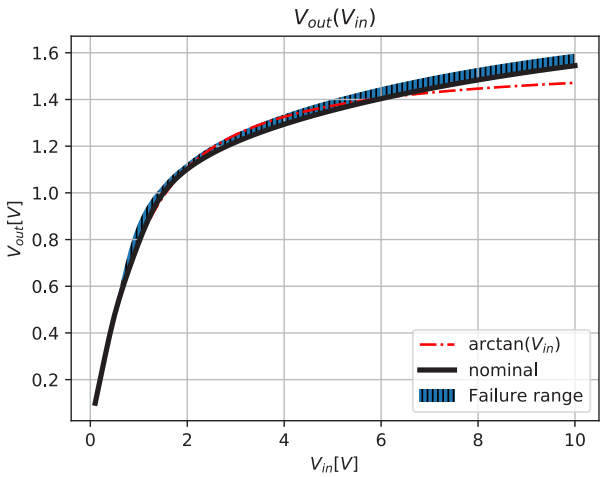

Figure 15: Synthesized arctan computational circuit (Nd_{max} = 10, Nr_{max} = 10): nominal response (black), arctan function (red, dashed-dotted). The range of various failure responses is given in blue.

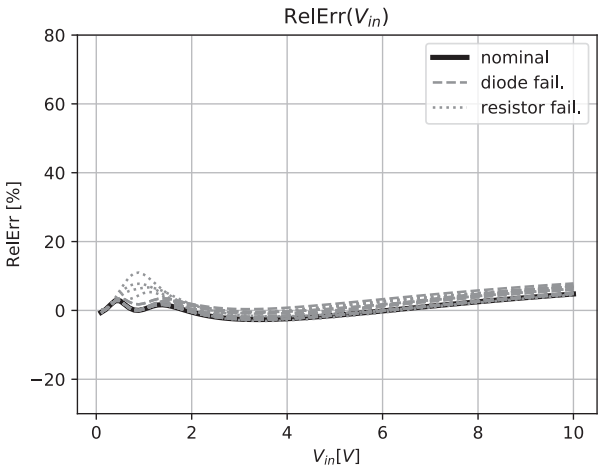

Figure 16: Synthesized arctan computational circuit (Nd_{max} = 10, Nr_{max} = 10): relative error curves of nominal (solid) and component failures (dotted and dashed).

3.3 Synthesis with a max of 8 diodes, 8 resistors

We proceed with Nd_{max} = 8 and Nr_{max} = 8. We stopped the algorithm after 432 generations (11h).

The outcome is presented in Figure 17. The final topology comprises 6 diodes and 6 resistors that can fail during the circuit operation. Two resistors and two diodes were not included in the final topology.

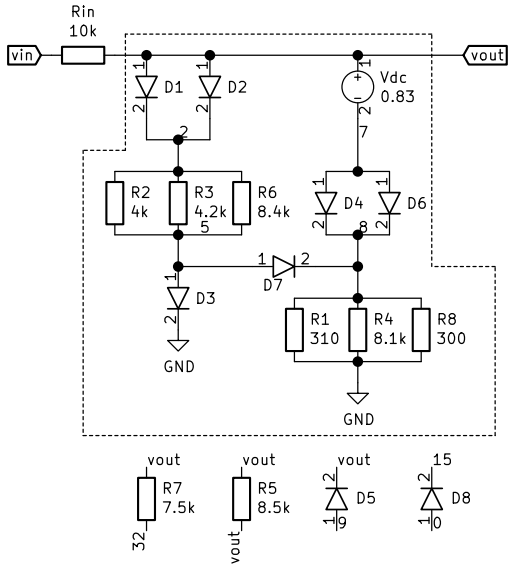

Figure 17: Synthesized arctan computational circuit (Nd_{max} = 8, Nr_{max} = 8), robust to any single component high-impedance failure or removal.

Circuit performance: nominal topology RMSE is 0.149, the worst failure RMSE is 0.152 and the standard distribution of all cases (nominal and failures) is 0.017. One can visualize failure ranges in Figure 18 and Figure 19.

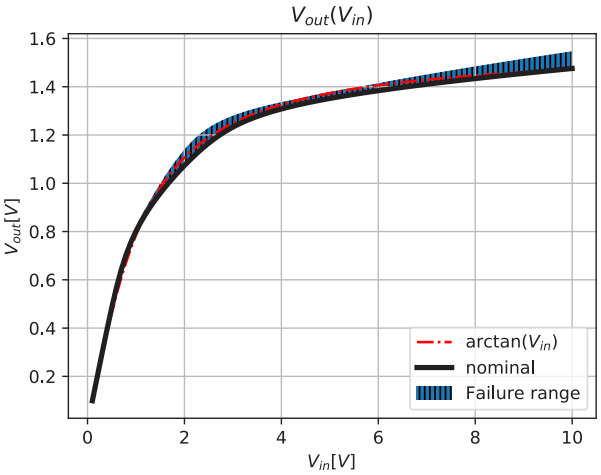

Figure 18: Synthesized arctan computational circuit (Nd_{max} = 8, Nr_{max} = 8): nominal response (black), arctan function (red, dashed-dotted). The range of various failure responses is given in blue.

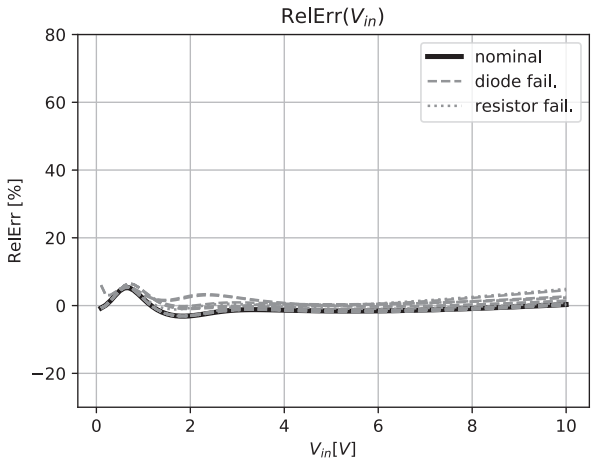

Figure 19: Synthesized arctan computational circuit (Nd_{max} = 8, Nr_{max} = 8): relative error curves of nominal (solid) and component failures (dotted and dashed).

Because the algorithm kept solving the problem using less than the maximum of available components, we proceed and further tighten the Nd_{max} and Nr_{max} criteria.

3.4 Synthesis with a max of 6 diodes, 6 resistors

We stopped the Nd_{max} = 6 and Nr_{max}= 6 synthesis after 2340 generations (48 h).

Figure 20 shows the outcome. The final topology uses all available diodes and three out of six available resistors.

Circuit performance: nominal topology RMSE is 0.106, the worst failure RMSE is 0.110 and the standard distribution of all cases (nominal and failures) is 0.008. One can visualize failure ranges in Figure 21 and Figure 22.

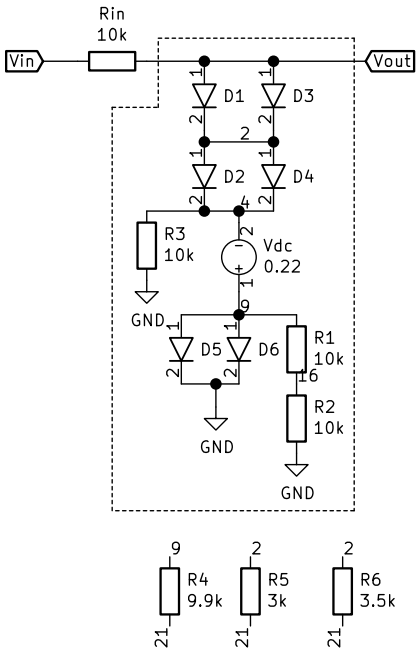

Figure 20: Synthesized arctan computational circuit (Nd_{max} = 6, Nr_{max} = 6), robust to any single component high-impedance failure or removal.

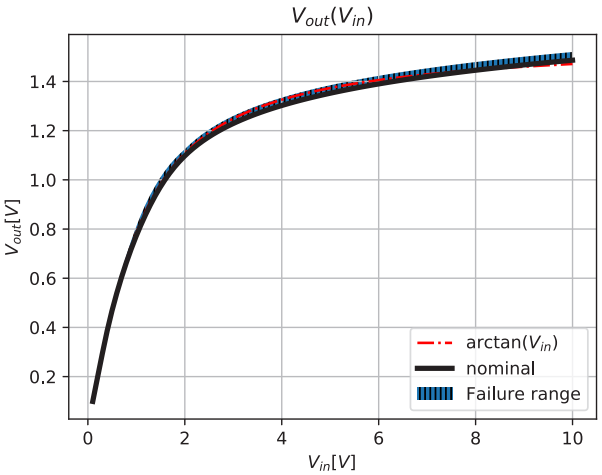

Figure 21: Synthesized arctan computational circuit (Nd_{max} = 6, Nr_{max} = 6): nominal response (black), arctan function (red, dashed-dotted). The range of various failure responses is given in blue.

3.5 Synthesis with a max of 5 diodes, 5 resistors

The Nd_{max} = 5 and Nr_{max}= 5 synthesis was stopped after 2582 generations (36 h).

As shown in Figure 23, the final topology comprises all available components.

Although the synthesis comprises only ten critical components (plus voltage source and input resistor), the performance was not yet diminished. The nominal

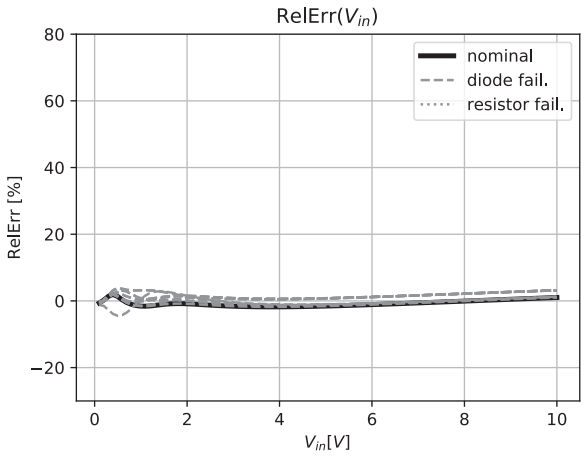

Figure 22: Synthesized arctan computational circuit (Nd_{max} = 6, Nr_{max} = 6): relative error curves of nominal (solid) and component failures (dotted and dashed).

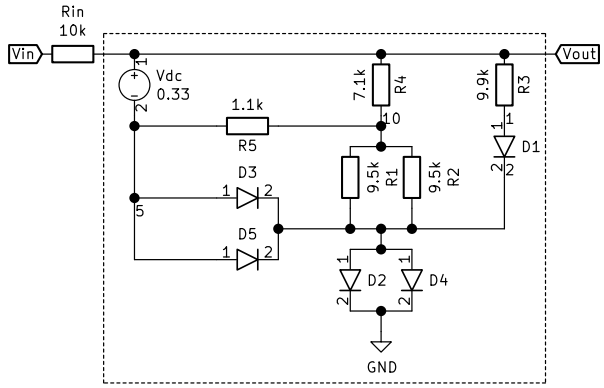

Figure 23: Synthesized arctan computational circuit (Nd_{max} = 5, Nr_{max} = 5), robust to any single component high-impedance failure or removal.

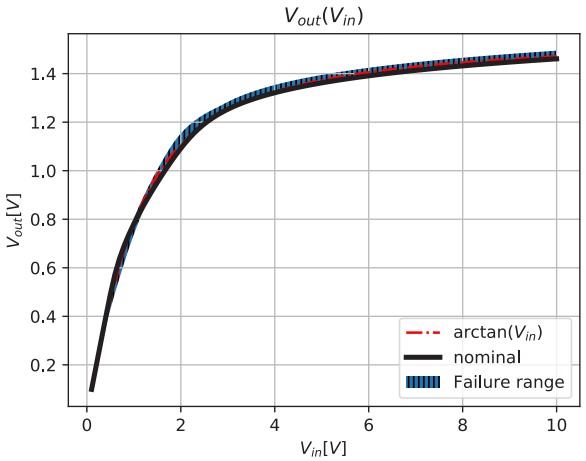

Figure 24: Synthesized arctan computational circuit (Nd_{max} = 5, Nr_{max} = 5): nominal response (black), arctan function (red, dashed-dotted). The range of various failure responses is given in blue.

topology RMSE is 0.108, the worst failure RMSE is 0.165 and the standard distribution of all cases is 0.022. See failure ranges in Figure 24 and Figure 25.

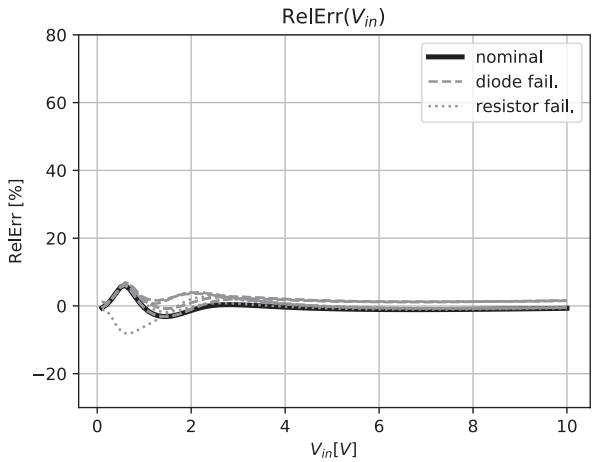

Figure 25: Synthesized arctan computational circuit (Nd_{max} = 5, Nr_{max} = 5): relative error curves of nominal (solid) and component failures (dotted and dashed).

3.6 Synthesis with a max of 4 diodes, 4 resistors

Searching for the bottom limit, we conducted the Nd_{max} = 4 and Nr_{max} = 4 synthesis. We finished it after 1077 generations and 12h.

The final topology comprised 4 resistors and 4 diodes (Figure 26).

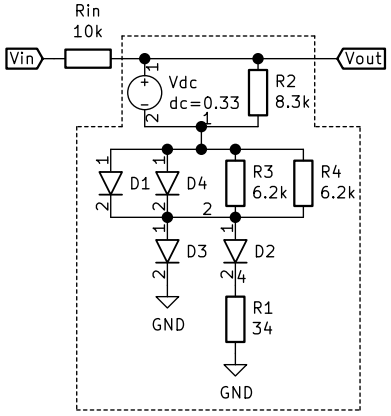

Figure 26: Synthesized arctan computational circuit (Nd_{max} = 4, Nr_{max} = 4), robust to any single component high-impedance failure or removal.

The nominal topology RMSE is 0.173, the worst failure RMSE is 0.217 and the standard distribution of all cases is 0.028. See failure ranges in Figure 27 and Figure 28.

We have discovered, that this synthesis is a probable bottom limit in our experiment. To illustrate, how a smaller design poorly fits the requirement, we show one more synthesis.

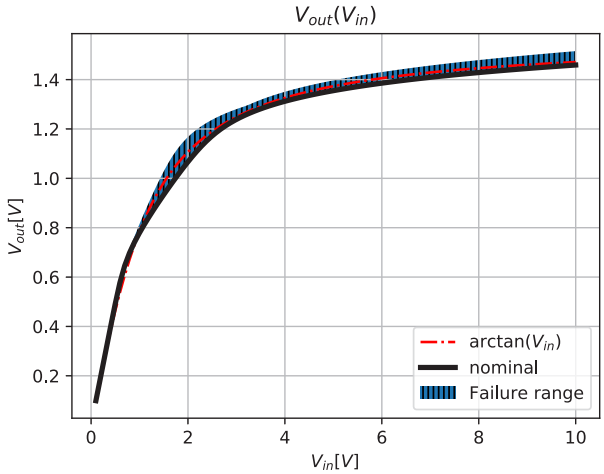

Figure 27: Synthesized arctan computational circuit (Nd_{max} = 4, Nr_{max} = 4): nominal response (black), arctan function (red, dashed-dotted). The range of various failure responses is given in blue.

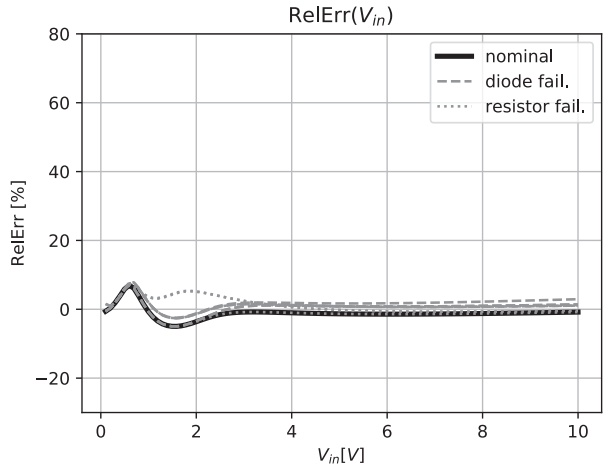

Figure 28: Synthesized arctan computational circuit (Nd_{max} = 4, Nr_{max} = 4): relative error curves of nominal (solid) and component failures (dotted and dashed).

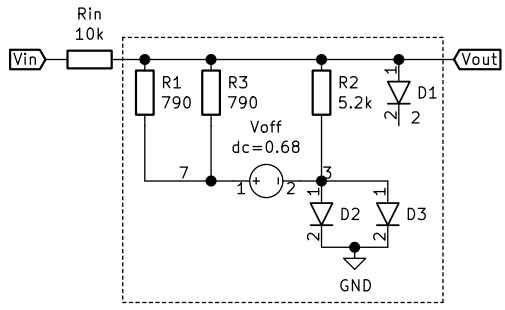

Figure 29: Synthesized arctan computational circuit (Nd_{max} = 3, Nr_{max} = 3), robust to any single component high-impedance failure or removal.

3.7 Synthesis with a max of 3 diodes, 3 resistors

Using limits Nd_{max} = 3 and Nr_{max}= 3 synthesis, we finished the search after 3188 generations (11h).

See Figure 29 for the topology. The nominal topology RMSE is 0.497, the worst failure RMSE is 0.507 and the standard distribution is 0.010. Failure ranges are shown in Figure 30 and Figure 31. We can observe a two-piece approximation of the arctan function, which yields high RMSE.

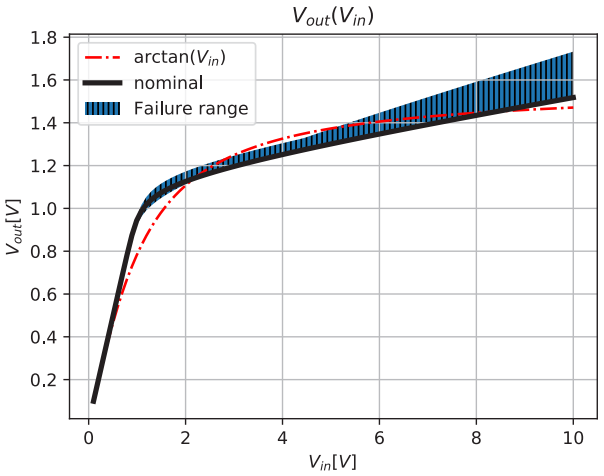

Figure 30: Synthesized arctan computational circuit (Nd_{max} = 3, Nr_{max} = 3): nominal response (black), arctan function (red, dashed-dotted). The range of various failure responses is given in blue.

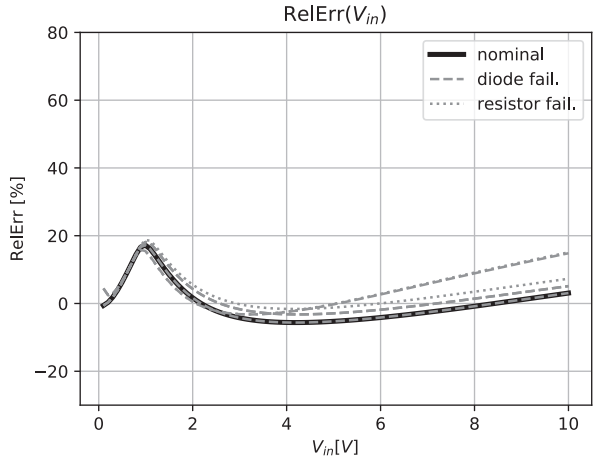

Figure 31: Synthesized arctan computational circuit (Nd_{max} = 3, Nr_{max} = 3): relative error curves of nominal (solid) and component failures (dotted and dashed).

3.8 Result Summary

Table 1 summarizes the experiment results. Surprisingly, tightening the number of available diodes and resistors has led to improved circuit performance in

both nominal functionality and robustness, with its best at Nd=6, Nr=3. Although initial syntheses involved searches over $Nd_{max} > 6$, $Nr_{max} > 3$ topology space, the Nd = 6, Nr = 3 best solution was not discovered in these.

Table 2: Results of a conducted experiment. Every row is an independent topology synthesis with different num. of component limits. The first row is the hand-made robust design.

Nd_{max}	Nr_{max}	Nd	Nr	f_{nom}	f_{max}	σ_f
N/A	N/A	10	30	0.116	0.262	0.047
12	12	12	6	0.312	0.370	0.026
10	10	10	8	0.158	0.270	0.032
8	8	6	6	0.149	0.152	0.017
6	6	6	3	**0.106**	**0.110**	**0.008**
5	5	5	5	0.108	0.165	0.022
4	4	4	4	0.173	0.217	0.028
3	3	2	3	0.497	0.507	0.010

There might be several reasons for that phenomenon. The first, most obvious one, is an enormous search space for topology search. Within one synthesis run, we cannot sample every possible circuit, but rather crawl the space using the evolutionary search. This is why two evolutionary syntheses with the same goal but different initial settings might not produce the same outcome.

The second reason is more related specifically to the robustness definition in our experiment. As noted, our problem definition does not reward circuits with fewer components, but rather the opposite. Inclusiveness (see 2.3) rewards circuits that electrically include all available components to push means of redundancy into the circuit and avoid false robustness. During the synthesis, while the objectives might already be met with requirements, the inclusiveness criteria might draw the search toward more included components, which makes the search too wide and lasting long. We conclude, that with such-defined search problem, the hard limits on the topology size and the number of available components are key to an efficient small-size failure-resilient topology search.

4 Conclusions

Using the topology synthesis tools, we can find topologies, that exhibit novel properties, such as failure tolerance. We showed that failure-resilience in analog circuits can be achieved with smaller-than-expected topologies, by introducing system-level redundancy instead of much more expensive component-level redundancy. Using an evolutionary-based topology synthesis tool, we introduced novel topologies of analog arcus tangent circuit. The most compact one comprises six diodes, three resistors, a voltage source, and an input resistor. Each of the diodes and the three resistors can fail or be removed, with almost no computational error.

Based on this research, we can conclude that the integration of system redundancy for single-point failures was achieved by imposing a strict limitation on the maximum size of available components. We showed, that to achieve such resilience, surprisingly low number of electrical components is needed.

In the realm of CMOS design, reducing the number of components doesn't necessarily translate to cost savings on its own. However, we conducted a brief analysis of the total resistance for both robust circuits, encompassing both hand-crafted and synthesized designs. Total resistance can provide a rough estimate of circuit area in certain CMOS processes. For instance, the total resistance of a hand-designed circuit (as shown in Fig. 4) amounts to approximately 219 kΩ, whereas the resistance of the best synthesized circuit totals around 20 kΩ (a difference of a decade).

Furthermore, reducing the number of components can have a direct impact on cost savings in the realm of discrete electronics, such as PCBs. In the domain of discrete resistors, the resistance value itself does not significantly affect the cost of the device, assuming factors like manufacturer, package, power rating, and tolerance remain the same. With this in mind, the minimization of robust topologies emerges as a pivotal factor in achieving cost-effective and highly reliable circuits.

In comparison to previous experiments, this study considers not only diodes, but also resistors to be a possible point of failure. We experimented with evolutionary search for circuits that are robust to both, short-circuit and open-circuit failures in all possible failure points (components), including some experiments including transistors. However, we acknowledge that further investigation and modified approaches are required to address this specific problem effectively.

We believe our work will inspire further practitioners in the field of analog circuit topology synthesis.

5 Supplementary material

The source code of the synthesis tool is available online at https://github.com/zigarojec/MatrixCircEvolutions.

6 Acknowledgments

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7 Conflict of Interest

We can declare no conflict of interest in this work.

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