ULTRA LOW NOISE PAGC AMPLIFIER FOR MICROSYSTEM SENSOR SIGNAL PROCESSING

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Abstract: One of the key properties of the microsystems is the quality of the front-end sensor signal processing. Typically a fully differential input and output stages are required for most of the analog signal processing to maintain the best possible rejection of the unwanted signals.

The design of such amplifier is discussed in this article. Special attention is paid to the offset voltage minimization, 1/f noise and thermal noise minimization. Temperature dependent Programmable Automatic Gain Control (PAGC) is incorporated to allow for sensor temperature coefficient compensation. Amplifier parameters are measured and characterized on the realized ASIC.

Ekstremno malošumni PAGC ojačevalnik za procesiranje senzorskega signala v mikrosistemih

Ključne besede: malošumni ojačevalnik, avtomatska regulacija temperaturnega koeficienta (PAGC), mikrosistemi

Izvleček: Ključna lastnost v mikrosistemih je kvaliteta procesiranja vhodnega senzorskega signala. Običajno zahtevamo vhodno stopnjo z diferencialnim vhodom in izhodom. Na ta način zagotovimo najboljše slabljenje neželjenih signalov. V članku je prikazana izvedba takšnega ojačevalnika, kjer sta minimizirana šuma 1/f in termični šum. Temperaturno odvisna avtomatska regulacija ojačenja z možnostjo nastavitve PAGC omogoča kompenzacijo temperaturnega koeficienta senzorja.

Rezultati simulacij in meritev na izdelanem ojačevalniku so podani v članku.

1. Introduction

The target was the amplifier with minimal input noise, differential input stage and single-ended output. The output signal has to be around the reference level V_{ref}.

The most commonly used answer to a problem is combination of either four input amplifier or combination of two unity gain input amplifier and the output stage. In both cases the input noise contribution is the sum of four input transistors together with resistor noise. A solution where the noise contribution is only the noise of two input transistors and the resistor noise is minimised to a negligible level is presented. The front-end block diagram is shown in figure 1.

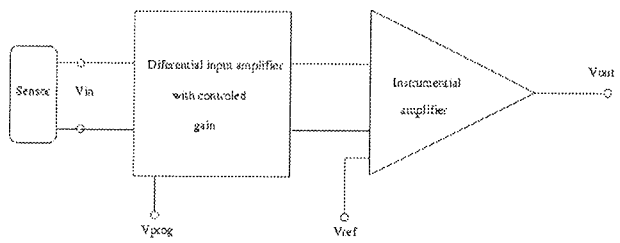


Fig.1: Front-end block diagram

2. Differential input amplifier

Selected topology of the differential amplifier with controlled gain is shown in the figure 2.

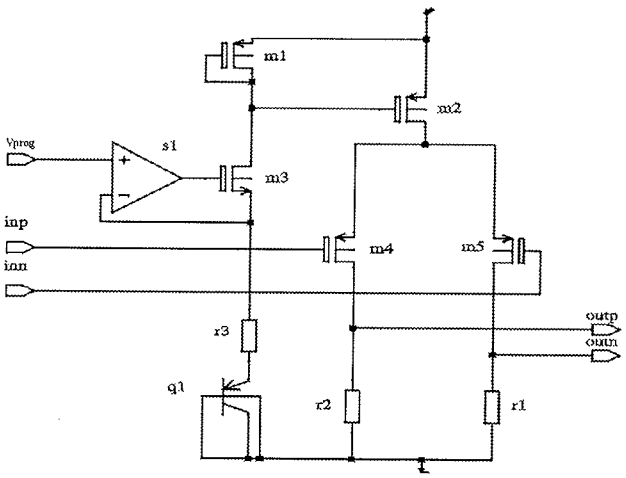


Fig. 2: Differential amplifier

It consists of the differential input transistor pair m4 and m5 and load resistors r1 and r2. The bias generator is made of bipolar transistor q1, resistor r3, MOS transistors m1 and m3 and sub circuit s1 for driving the transistor m3.

The bias generator, its influence and main proprieties is described in section 3. The dimensions of differential pair and bias current are calculated to obtain 26dB gain i.e. 20dB at each output.

The target 1/f noise density of differential amplifier at 1 kHz is less than 7nV/√Hz; the target thermal noise density level at 100 kHz is less than 5nV/√Hz and the gain-bandwidth product over 100MHz.

2.1 Noise characteristic

Several simulations were made to analyze the influence of the input stage transistor type on noise performance. The amplifier was intended to be used in a magnetic microsystem where the equivalent noise resistance of the sensor was 1kΩ. In all simulations and measurements this equivalent noise resistor was included.

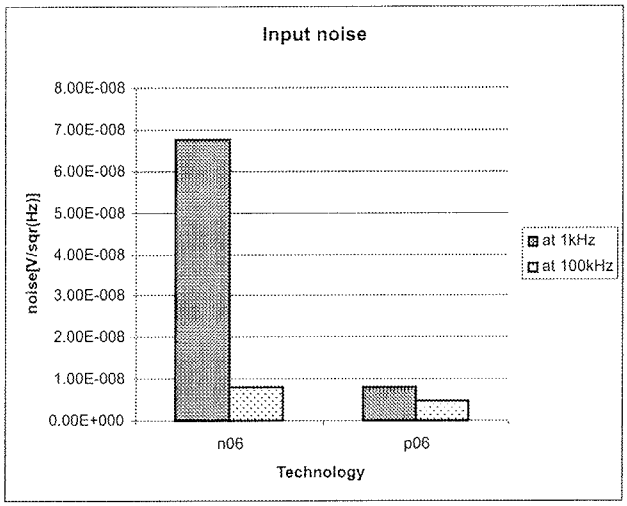


Fig. 3: Noise density for n-type input transistor stage (n06) for p-type input transistor stage (p06)

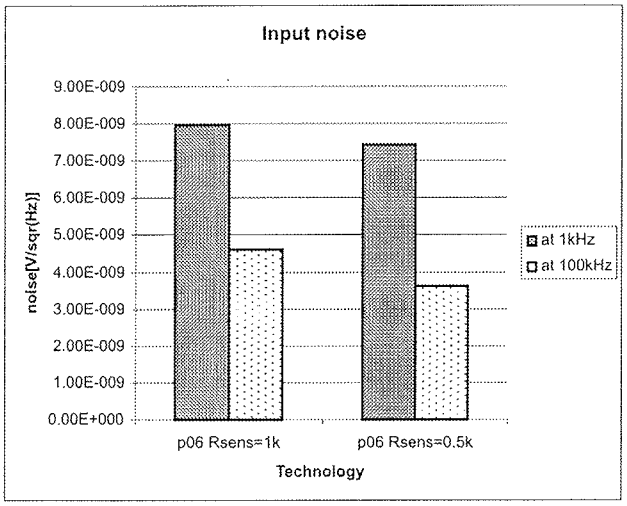


Fig. 4: The influence of equivalent noise resistance of the microsensor

The analyses were made for 0.6μm technology. It was found out, that p-type transistor input stage, using the same transistor sizes, has lower noise than the n-type. Figure 3 presents simulation results for p and n-type input stage. As shown, the noise level for n-type input differential stage is around 68nV/√Hz, and for p-type stage 7,9nV/√Hz at 1kHz (1/f noise mainly). At 100kHz (thermal noise) the noise density levels are 8.1nV/√Hz for n-type and 4.6nV/√Hz for p-type. Even with lowest noise level around 24nV/√Hz at 1kHz for n-type input stage could be achieved.

Figure 4 shows the noise density level at different sensor equivalent noise resistances. As expected, the sensor resistance value has major influence on thermal noise (100kHz). The thermal noise level of the system for 1kΩ sensor equivalent noise resistance is 4,62nV/√Hz and 3,62nV/√Hz for 0.5kΩ sensor equivalent noise resistance.

2.2 Comparing technologies

The basic proprieties of the input differential stage for different technologies have been analysed. Figure 5 shows the noise density level of input differential amplifier in 0,35um, 0,6um and 0,8um CMOS technology. The comparison is done for p-type input stage transistors due to better performance. As expected 1/f noise (at 1kHz) level is lower with smaller technology; meanwhile the thermal noise (at 100kHz) doesn't change a lot. The noise level varies from 5,27nV/√Hz for 0.35um technology, up to 8,95nV/√Hz for 0.8um technology. The thermal noise is around 4.65nV/√Hz, for all technologies.

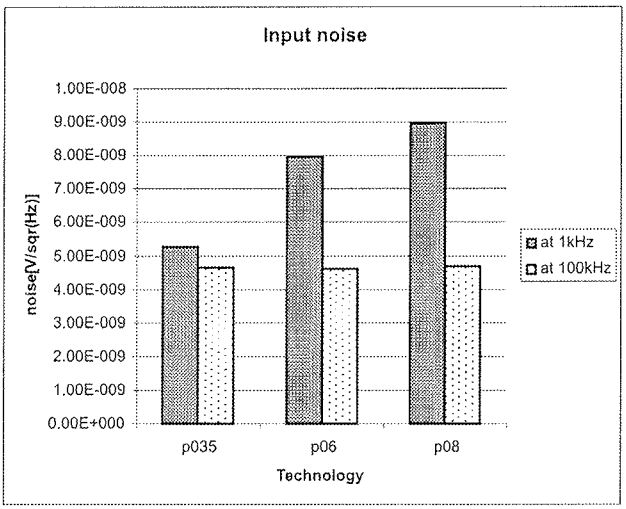


Fig. 5: Noise at different technologies

The influence of different technologies on gain has been analysed. For these simulations the dimensions of input differential transistor pair were modified to achieve the same input capacitances, to compensate the gate oxide thickness change with the technology. For example, the thickness of gate oxide for 0,8um technology is 18nm, for 0,6um technology 12nm and for 0,35um around 15nm. In 0,35um technology, the thickness is larger due to the use of tran-

sistor with mid-gate oxide, operating at 5V. Figure 6 shows the gain for different technologies with p-type input transistors and for comparison the 0,6um n-type input transistor stage is added. As seen, the gain doesn't vary a lot with technologies. As expected n-type input stage has a higher gain factor.

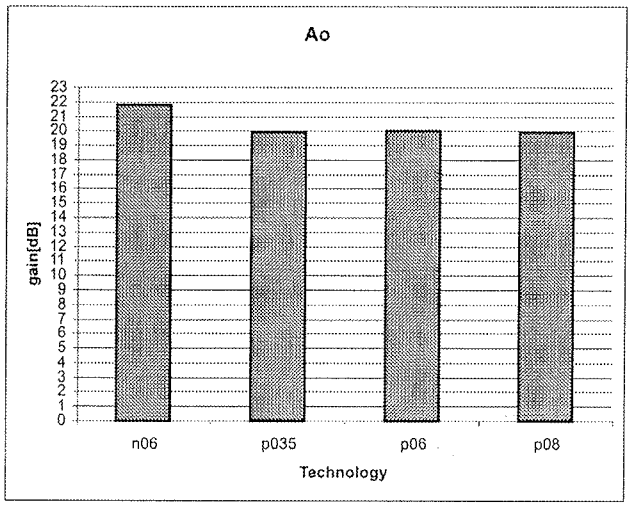
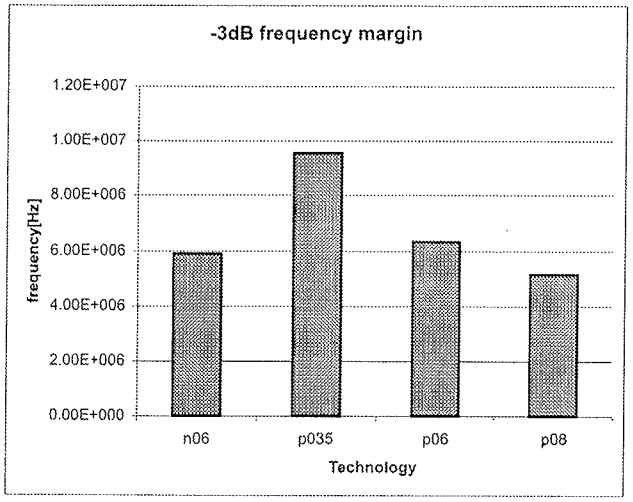


Fig. 6: Gain at different technologies



Fig, 7: -3dB frequency margin

Variation of -3dB frequency margin is shown in figure 7. As shown, n-type of input stage doesn't have the best performance. The best technology is 0,35um where gain-bandwidth product over 190MHz has been achieved.

2.3 Performance of the selected differential input stage

Due to the best performance the p-type input differential stage in 0,35um technology was chosen for our system. Several analyses with different corners (worst cases of technology parameters) have been performed in the temperature range between -20°C and 100°C.

In figure 8, the results for temperature sweep are presented. The gain variation for technology corners *wp* (worst power), *ws* (worst speed), *wz* (worst n-type transistors) and *wo* (worst p-type transistors) can be observed.

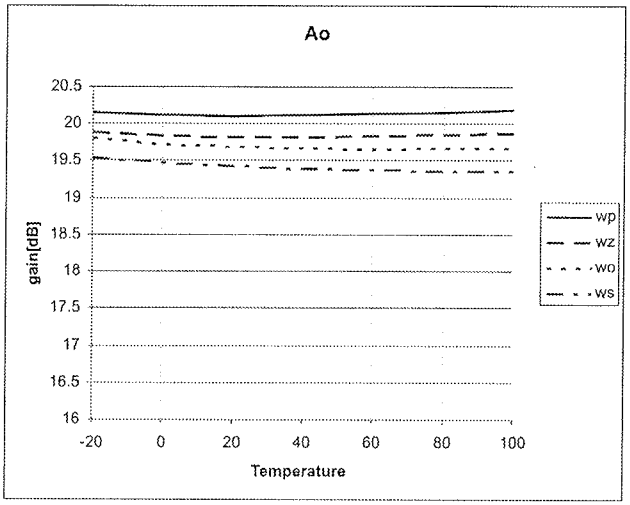


Fig. 8: Gain variations with temperature and process corners

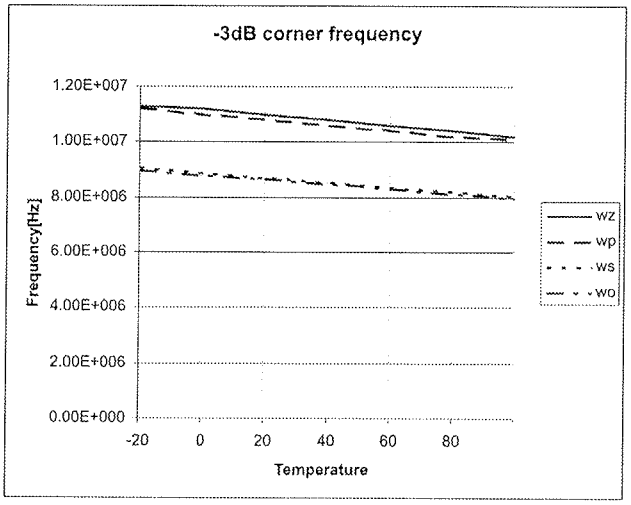


Fig. 9: -3dB corner frequency as a function of temperature and process corners

As shown, in the worst case the gain of the input stage drops to the lowest value around 19,4dB at worse speed parameters and at the highest temperature.

The lowest -3dB corner frequency is 8MHz at worst p-type transistors condition at high temperature. This corresponds to the worst case gain-bandwidth product of 156MHz. The level of input noise density at 1kHz (1/f noise) is shown in figure 10.

When changing the corners there are no noticeable influence to the noise density level. However noise density at 1kHz changes with the temperature from 4,75nV/√Hz to 6,12nV/√Hz, and from 4.25nV/√Hz to 5,25nV/√Hz at

100kHz as seen at figures 10 and 11, in the temperature range of 120 °C.

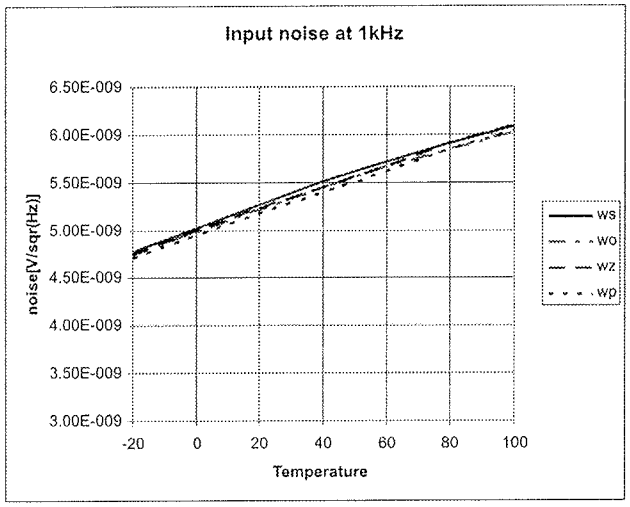


Fig. 10: Input 1/f noise

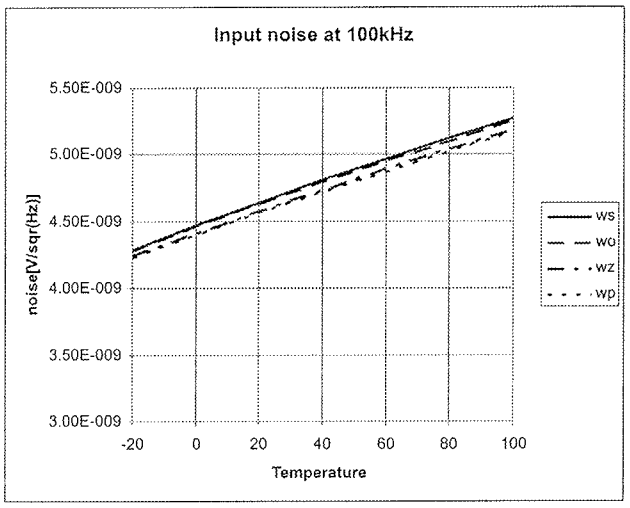


Fig. 11: Input thermal noise

3. Programmable automatic gain control

The programmable bias generator is used to control the gain of the amplifier and to compensate the temperature dependence of the proposed amplifier and of the microsensor.

Special attention was paid to the design of relevant components of the bias generator to minimize its influence to the overall noise. The topology of the bias generator is shown in figure 12.

Minimization of the noise influence is taken care by appropriate sizes of the transistors m1 and m2. The temperature coefficient of the bias current is set by the appropriate selection of the reference voltage and the value of resistor r3.

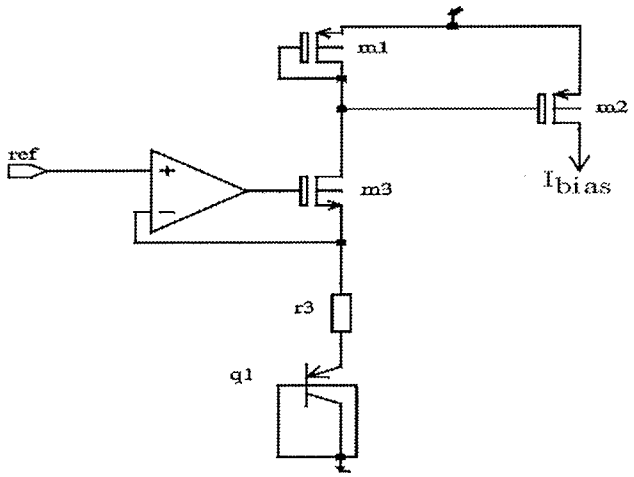


Fig. 12: Bias generator

Figure 13 shows the temperature behavior of the bias current for all corners.

When selecting such temperature dependence of the bias current we obtain minimal gain variation of the amplifier as seen in the figure 8. The sensor temperature coefficient can be programmed by the control voltage on the Prog input. The temperature dependence of the bias current is given by the expression:

$$I_b(temp) = \frac{V_{prog} - V_{be}(temp)}{r_3(temp)}$$

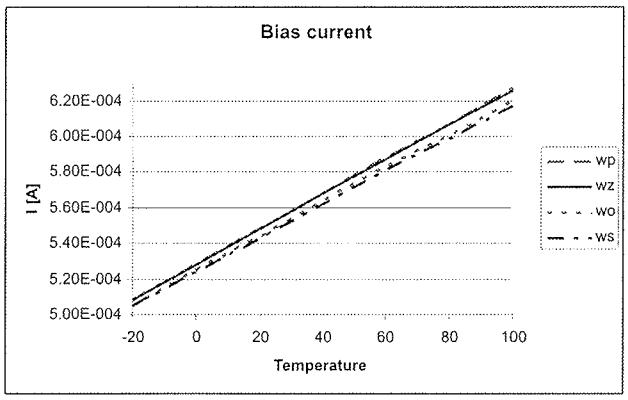


Fig. 13: Bias current

As both the temperature dependance of the V_{be} and r_3 are known for a given technology the wide range of bias current temeprature dependance can be achieved by changing the programming voltage V_{prog}.

The measured results for noise density are shown in figure 14 compared to simulation results. A perfect matching with simulated results has been observed also in other amplifier characteristics.

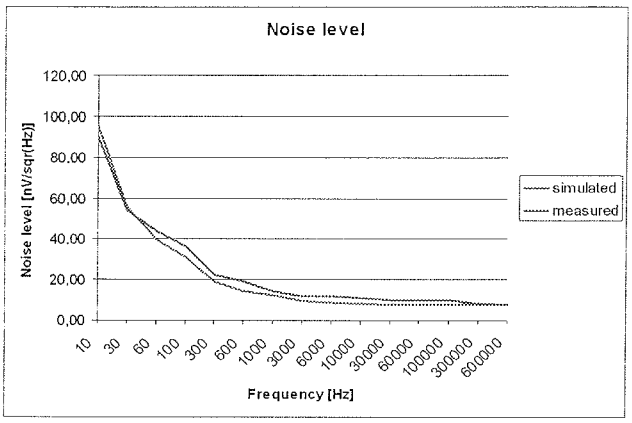


Fig. 14: Measurement results compared to simulation results

4. Conclusion

A minimal noise and offset input amplifier with automatic temperature controlled gain has been introduced. It has been shown, that n-type transistors have larger noise than p-type transistors. When using smaller technology, 1/f noise is decreasing for the same silicon area. Very low 1/f noise density level of 5,27nV/√Hz at 1kHz typical and 4,65nV/√Hz thermal noise density typical with dominant contribution of the sensor equivalent noise resistance has been achieved. The microsystem sensitivity is temperature stabilized by the use of special programmable bias current generator. Typical sensitivity variation of the system with temperature is 70ppm/°C. Typical gain-bandwidth product is 190MHz.

5. References

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