REDUCTION OF SWITCHING NOISE AND POWER SUPPLY CURRENTS IN DIGITAL CIRCUITS WITH DIRECTED DATA FLOW

Dušan Raič

Faculty of Electrical Engineering, University of Ljubljana, Ljubljana, Slovenia

Key words: mixed design, switching noise, clock distribution.

Abstract: Substrate noise is a serious limiting factor in the design of analogue-digital systems. Distributed clock systems can be used as an efficient method to solve the simultaneous switching noise problems associated with the data processing and clock distribution. We present a short overview of known methods for switching noise reduction and propose a general clock distribution technique for circuits with directed data flows. The clock distribution network is implemented by a clock pipeline. The associated synchronisation problems are solved by reverse clocking scheme and signal latching in feedback loops. The processing of N-bit long data by the proposed system shows that power supply spikes can be reduced by a factor ~1.2N and the associated substrate noise by a factor of ~0.75N comparing to the standard central-clock solutions. This makes this method particularly well suited for measuring systems as noise reduction increments proportionally to precision.

Koncept digitalnega vezja z usmerjenim pretokom podatkov za omejevanje šuma in napajalnih tokov v integriranih vezjih

Ključne besede: načrtovanje analogno-digitalnih vezij, preklopni šum, signal ure.

Izvleček: Eden od pomembnih faktorjev ki omejujejo načrtovanje analogno-digitalnih integriranih vezij je šum, ki nastane zaradi injiciranja nosilcev v substrat vezja. Uporaba porazdeljenega signala ure v digitalnem delu vezja lahko ta problem v veliki meri zmanjša. V tem delu najprej podajamo kratek pregled znanih metod za zmanjševanje preklopnega šuma in nato predlagamo splošno rešitev za sisteme z usmerjenim pretokom podatkov. Krmiljenje signala ure je zasnovano na zakasnilni liniji. Zaradi tega nastane problem sinhronizacije, ki ga rešimo z uporabo obratnega pretoka podatkov in signala ure ter z ustreznimi zakasnitvami v povratnih zankah. V primerjavi s klasičnim sistemom predlagana metoda pri podatkovnih strukturah z dolžino N bitov omogoča zmanjšanje konic napajalnega toka za faktor ~1.2N in zmanjšanje šuma v substratu za faktor ~0.75N. Ker sta obe izboljšavi proporcionalni s preciznostjo obdelave podatkov je opisana metoda zlasti uporabna v merilnih sistemih.

1. Introduction

It is well known that digital circuits generate considerable electrical noise as a result of logic gate transitions from one state to the other. In logic systems the switching noise can cause transient faults while in mixed analog-digital circuits it can seriously limit the performance or even prevent proper operation of analog blocks that share the common substrate. In addition to substrate noise the power supply current spikes cause voltage drops and bouncing that can lead to functional failures and undesirable stressing of materials used to supply power to circuit elements.

With the evolution of VLSI circuits toward smaller feature sizes and higher operating speeds this problem is becoming more and more important. Supply currents in future digital chips are expected to rise dramatically /13/.The gap between transistor and interconnect performances is causing intolerable delays in old fashioned clock distribution networks /7/. At the same time the smaller sizes of basic elements give opportunity to integrate large systems containing analog blocks so that the demand for mixed circuits is increasing as well. As a consequence, the noise, clock and power distribution are becoming of utmost importance for future generations of integrated circuits.

There are many known techniques for reducing effects of the switching noise and switching currents. Examples of known solutions show that that they can be divided roughly into 5 categories:

1. *Isolation techniques* separate sources of noise from areas where they would do most harm.
2. *Additional circuits or devices* cancel effects of the switching noise.
3. *Special circuit techniques and logic topologies* are tailored to generate low switching noise and/or limit switching currents.
4. *Architectural measures* divide the circuit into blocks that are coordinated in such a way that we minimize the influence of noise-generating to noise-susceptible blocks.
5. *Additional data processing* can be used in order to remove noise components from output data.

However, none of the approaches can solve all possible problems. An early paper /1/ and a recent one /2/ present typical isolation techniques. Noise attenuation is possible only to a certain degree, so the methods described are useful when all other means have been exhausted and the level of noise is still expected to be too high. The general drawback of these methods is limited success and the in-

crease of chip area and design time which both reflect on the production cost.

Switching noise reduction devices can be used as additional logic elements driving load replica with the inverted logic function so that the quantity of switching current which flows in an inductance is reduced. Additional circuits can be used also to isolate the noise source logically. Methods of this kind are very specific and can be economically applied only to selected nodes of particular interest or nature that must be identified in each system individually.

Special circuits and logic topologies are most powerful design tools to reduce switching currents and switching noise. Circuit techniques have been invented to limit switching currents in stages that draw significant amounts of current, such as output signal driving stages. Another class of inventions covers the structure of logic operators. On the first place we have to mention various current mode techniques where switching currents are kept constant by means of current generators /16/. The problem with current mode logic families is that supply current is drawn regardless of circuit operating frequency, essentially preventing the power-down mode or power-saving operations in the system. Circuits from this family can be also more complex than known standard CMOS logic, resulting in increased chip area and design time.

Data processing measures are very specific and can be applied only when data processing is possible or already present in the system. In such a case the noise reduction technique is based upon shaping the noise from the digital circuit and concentrating it in a single, or a small number of parts in the frequency spectrum that can be filtered out /15/.

A well known example of architectural measures is the so called 'quiet period sampling' technique. It typically relies on two or more clocks that are separated in time to synchronize analog and digital blocks so that analog data are sampled in intervals when digital blocks do not produce noise. An example of this method comprising two clock signals is described in /14/. By delaying the digital clock signal, noise induced upon the substrate embodying the analog circuitry is shifted by an amount of time necessary to allow the noise to settle before the analog clock samples new data. A similar solution is described in /18/ where the clock system is divided into four clock subsystems, generating two pairs of clock signals so that one pair of signals is delayed with respect to the other pair in order to reduce the switching noise on power bus.

2. The distributed clock approach

The common drawback of known architectural methods is the lack of generality, so our goal is to find a systematic solution that can be used automatically in a broad range of circuits without going into the specifics of individual system timing and architecture. The method is based on directed data and clock flow control as presented on Figure 1. This structure is very general so that it can represent a large number of known building blocks such as counters, shift registers and data pipelines (Figure 2).

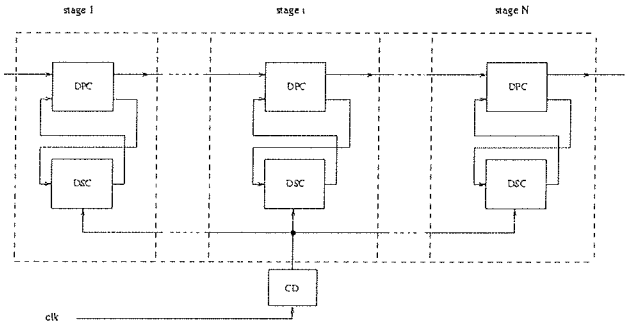
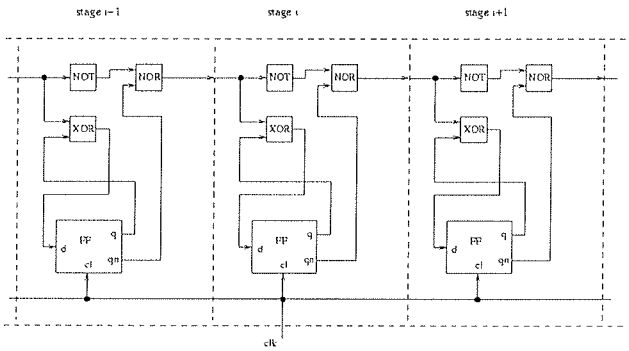
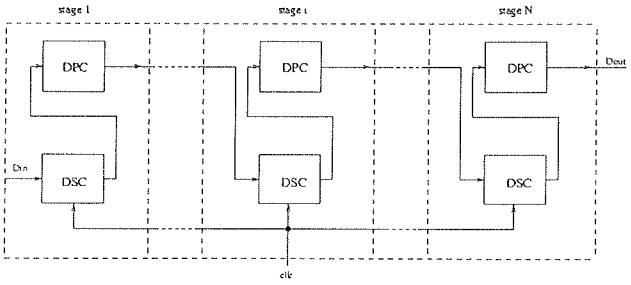


Figure 1. Structure of a synchronous digital system with directed data flow.



(a) Synchronous counter. DPC elements implement binary counting and DSC elements contain single flip-flops.



(b) Data pipeline. DPC inputs are connected to DSC outputs from the same stage while inputs to DSC elements come from DPC outputs from previous stage. The number of flip-flops in DSC elements may vary according to pipeline implementation.

Figure 2. Examples of typical building blocks, presented in the form of the structure from Figure 1.

In classic synchronous systems there is only one central clock driver (CD) while the data can be processed in several stages. The data flow is defined by connections be-

tween the data processing (DPC) and data storing circuits (DSC). Synchronized by the clock, transients occur in all stages simultaneously, causing large current spikes at clock edges. However if we treat the clock also as a data-flow process, the switching currents of most important noise sources (clock driver, flip-flops and logic gates) become controllable by the clock network. They can be distributed in time so that significant peak value reductions become possible. For the same reason, only a fraction of circuit nodes is active at a given time, leading to similar reduction of crosstalk /6/ and parasitic currents in the substrate /4/.

To control the clock flow we propose to replace the central clock driver by the clock pipeline, acting as a delay line. Signals from all stages are used so that we replace the central clock signal by a large number of local clock signals, applied in small circuit clusters. The simplest implementation of such clock delay line is the inverter chain (Figure 3). More complex solutions with delay lock loops can be used if clock delay is to be adapted to some system parameters.

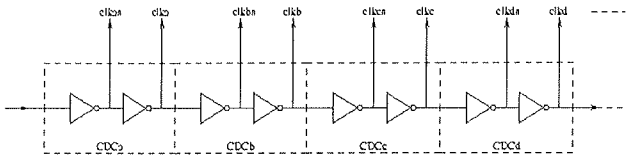


Figure 3. Clock pipeline implemented as a simple inverter chain.

Clock pipelines have been proposed in previous work on high speed clocking as a means for clock skew control in large processing arrays. In /2/,/8/ they were primarily studied as a substitute for the wire interconnect, taking only the signal from the last stage as the clock for a given module. One important property of clock pipelines is that clock skew depends more on transistor properties than on wires. Because of that, reasonable delay modeling is possible by timing or even logic simulation tools.

3. The synchronisation problem

The replacement of clock signal by a large number of delayed signals violates the basic principle of synchronous logic which relies on one single clock, distributed without significant delays to all parts of the system. However safe system operation is possible also under the distributed clock conditions if the data processing flow and the clock signal flow are properly coordinated in the time.

One possible solution is the application of reverse-clocking principle /22/.This technique has been reported mainly to prevent pipeline malfunctions at high speeds when clock lines start to exhibit RC line effects /3/. The idea is to propagate data and clock signals through a pipeline in opposite directions so that false strobing is not possible. In the case of distributed clocking, the clock delays are introduced by purpose so that they play a vital role also at low clock speeds.

The proposed structure is presented on Figure 4. Comparing to Fig. 1, the central clock driver is replaced by N delay line elements (CDC). If feedback data loops are presented in the system they are additionally delayed by the FDSC circuit which is synchronized from the last stage of the clock delay line.

In systems with the central clocking scheme the data to be processed remains stable after the active clock edge so that outputs of DPC circuits stabilize during the clock period. When the next active clock edge arrives, outputs are stored in DSC circuits so that next processing cycle begins. In the system with directed data flow and reverse clock distribution as presented on Figure 4, the same functionality is assured by the fact that active clock edge travels in time along the clock delay line and synchronizes individual data storage circuits sequentially. Stages that are hit first change their outputs. Because of the opposite direction of the data and clock signals these changes cannot influence inputs to stages that have not been hit yet. Processing inputs and the result of a given stage at the time when it is hit by the active clock edge depend exclusively on results from the previous clock cycle, stored in DSC circuits of the stages that have not been hit yet by the same active clock edge.

The reverse clock distribution as described above assures proper synchronization as long as stage inputs are not connected to outputs from the same stage. If such a connection is required by the system, the feedback data does not follow the rule of uniform data direction between stages. In such case additional data storage circuit (FDSC) is required in the feedback loop. The proposed structure with data feedback to stage 1 is presented on Figure 4. Feedback data from stage N (or any other stages) are delayed in the FDSC by the clock signal from the last clock delay line stage. This signal actually characterizes the end of current clock cycle and assures that feedback data will remain stable until the end of next processing cycle. Because of that, delayed feedback data from FDSC can be used as input to any DPC stage.

Another important limitation of the reverse clocking technique is the reduction of the effective clock cycle time. From the description given above it is evident that input to stage 1 must not change while the active clock edge travels along the clock delay line. If t_d is the clock delay in one stage then the effective clock cycle period is reduced for $N \cdot t_d$.

In order to automate the process of clock distribution the clock pipeline can be integrated into the data storage circuits. Each pipeline stage in this case contains the data processing, data storing and clock delay element. The central clock driver is completely removed and replaced by a distributed clock network. A typical example of this concept is presented on Figure 5. Depending on the type of

the logic circuit, various solutions for specific flip-flop and latching circuits are possible in order to provide the necessary delays and clock phases. With appropriate circuit design, transistor dimensions can be optimized to minimize the switching currents and the associated noise /23/.

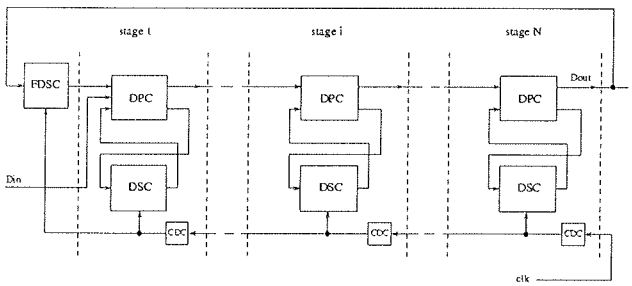


Figure 4. A general solution for switching noise reduction, based on distributed clocks from clock pipeline.

Although the delay and overlapping of the clock signals influence the noise and current spike reduction they are not essential for the spirit of this technique nor they can cause malfunction. The designer can decide upon these parameters on the basis of system speed and noise parameters, leaving the basic architecture unchanged.

4. Circuit solutions and results

Figure 5 illustrates the proposed technique on the shift register example. On Figure 7 we can see the power supply current simulation for N = 24, compared to equivalent register with the central clock. The reduction factor R = 11.2 has been measured for minimum-sized C^2MOS flip-flops operating at Vdd = 3V in a 0.6 um technology. The clock delay line has been integrated inside flip-flops. The register outputs in this example were loaded with 20 fF and the data shifted was 666666h -> CCCCCCh.

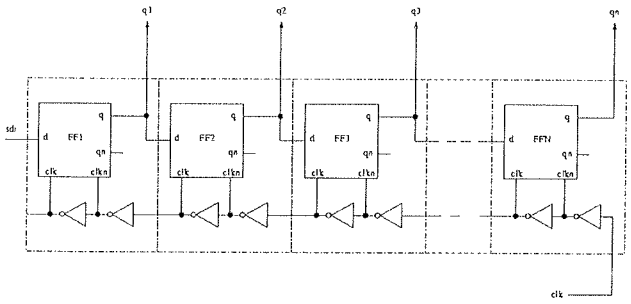


Figure 5. Example of a shift register, implemented according to Figure 4.

The simplicity of reverse clock principle requires also a price to be paid. The clock delay line may consume more power than an equivalent central clock driver may. Another important consideration is the limitation of clock period by the total delay in the clock delay line. This limitation

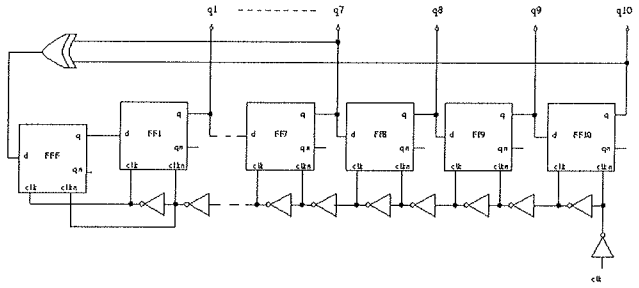


Figure 6. Example of proper feedback handling in the pseudo-random sequence generator, implemented according to Figure 4.

means in a way that circuit speed has been traded for supply current and noise reduction. Best results of the method described can be therefore expected in systems of moderate size and speed.

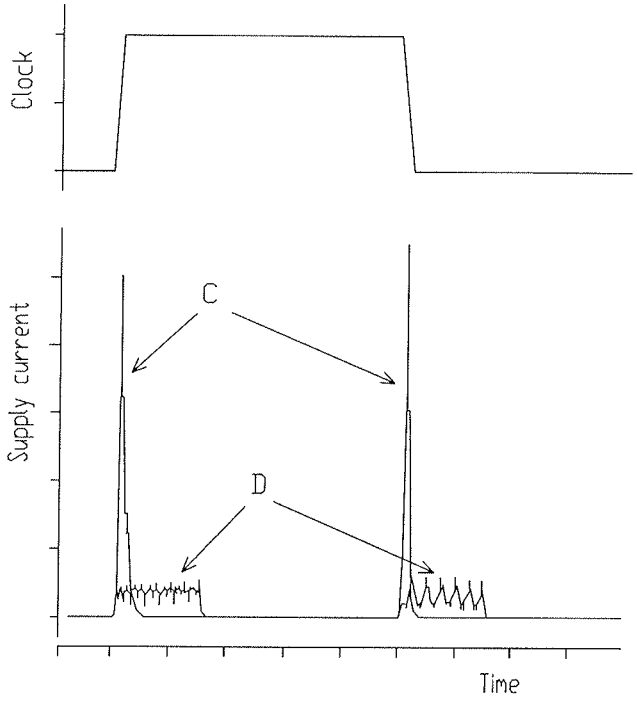


Figure 7. Simulation of power-supply current in the shift register from Figure 5 (waveform D), compared to equivalent circuit with central clock (waveform C).

5. Conclusion

The presented method is a mixture of circuit and architectural measures to reduce noise and switching currents in integrated circuits. It can be applied to digital systems with directed data flow processed in a number of stages. The reduction does not take place in individual logic gates, it comes into effect in larger blocks or the integrated circuit as a whole. Another important feature of the method is the fact that it can be used as an additional measure, together with other known methods for noise reduction and switch-

ing current limitation. It also does not imply any operating frequency limitations other then those given by the logic circuitry, including the power-down mode. The last but not least, the reduction of switching currents and noise does not apply only to logic gates and flip-flops, but also to the clock distribution system. The later is known to be an important source of noise because of large signal buffers and long metal lines. According to /3/, an estimation of power consumption in various chips shows 20-45% of power to be used for clock system. Half of this power can be roughly assigned to flip-flops and the other half to clock buffers. Switching currents and noise can be assumed to follow the same distribution.

If the logic block is composed of N stages, the switching current and switching noise can be reduced proportionally to N. Exact numbers depend on timing relations between clock signal delay, switching characteristics of the logic and data being processed. In simple cases with minimum processing logic, like the one presented on Figure 5, high reduction factors around N/2 can be achieved easily.

A number of well known building blocks, such as counters, shift registers and data pipelines can be built according to the presented method. The supply current spike and substrate noise reductions are proportional to the number of stages if compared to the conventional central clock systems.

References

/1/ J. R. Burns, "Switching Response of Complementary-Symmetry MOS Transistor Logic Circuits", *RCA Review*, vol. 25, pp. 627-661, December 1964.

/2/ A. L. Fisher, H.T. Kung, "Synchronizing Large VLSI Processor Arrays", *IEEE Trans. Comput.*, C-34, pp. 734-740, August 1985.

/3/ J. Yuan, C. Svensson, "High-speed CMOS Circuit Technique", *IEEE J. Solid-State Circuits*, Vol. 24, pp.62-70, February 1989.

/4/ D. K. Su, M. J. Loinaz, S. Masui, B. A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits", *IEEE J. Solid-State Circuits*, Vol. 28, pp.420-429, April 1993.

/5/ D. Allstot, S Chee, S. Kiaei, M. Shrivastawa, "Folded Source-Coupled Logic vs. CMOS Static Logic for Low-Noise Mixed-Signal Ics", *IEEE Trans. Circuits and Systems-1: Fundamental Theory and Applications*, Vol. 40, pp.553-563, September 1993.

/6/ P. Larsson, C. Svensson, "Noise in Digital Dynamic CMOS Circuits", *IEEE J. Solid-State Circuits*, Vol. 29, pp. 655-662, June 1994.

/7/ D. Matzke, "Will Physical Scalability Sabotage Performance Gains ?", *IEEE Computer*, Vol. 30, pp. 37-39, September 1997.

/8/ M. Nekili, G. Bois, Y. Savaria, "Pipelined H-Trees for High-Speed Clocking of Large Integrated Systems in Presence of Process Variations", *IEEE Trans. VLSI Syst.*, Vol. 5, pp.161-174, June 1997.

/9/ C.F. Webb et al., "A 400-Mhz S/390 Microprocessor", *IEEE J. Solid-State Circuits*, Vol. 32, pp.1665-1672, November 1997.

/10/ M. Ingels, M. S. Steyaert, "Design Strategies and Decoupling Techniques for Reducing the Effects of Electrical Interference in Mixed-Mode IC's", *IEEE J. Solid-State Circuits*, Vol. 32, pp.1136-1141, 1997

/11/ D.W. Bailey, B.J. Benschneider, "Clocking Design and Analysis for a 600-MHz Alpha Microprocessor", *IEEE J. Solid-State Circuits*, Vol. 33, pp. 1627-1633, November 1998.

/12/ H. Kawaguchi, T. Sakurai, "A Reduced Clock-Swing Flip-Flop for 63 \% Power Reduction", *IEEE J. Solid-State Circuits*, Vol. 33, pp. 807-811, May 1998.

/13/ B. Chapell, "The fine art of IC design", *IEEE Spectrum*, Vol. 36, pp. 30-34, July 1999.

/14/ E. Swanson, N. Sooch, D. Knapp, "Method for reducing effects of electrical noise in an analog-to-digital converter", *US Pat. 4746899*, 1988

/15/ A. Corry, G. Mostyn, J.Y. Michel, "Noise reduction in integrated circuits and circuit assemblies", *US Pat. 5649160*, 1997

/16/ P. Werking, "Source-coupled logic with reference controlled inputs", *US Pat. 5798658*, 1998

/17/ J. A. Olmstead, "Noise Problems in Mixed Analog-Digital Integrated Circuits", *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 659-662, Portland, OR, 1987

/18/ W. Haberecht, E. DeMan, M. Schulz, "A Programmable 32 Tap Digital Interpolation Filter in 1.5 um CMOS with 80 Mhz Output Data Rate", *Proc. IEEE Custom Integrated Circuits Conf.*, pp.13.1.1-13.1.4, Boston, MA, 1990

/19/ M. Shoji, "CMOS Digital Circuit Technology, *Prentice-Hall*, Englewood Cliffs NJ, 1988.

/20/ N. M. Rabaey, "Digital Integrated Circuits: a design perspective", *Prentice-Hall* , Englewood Cliffs NJ, 1996

/21/ A. Yasuo, M. Ikeno, "A Time Digitizer CMOS Gate-Array with a 250 ps Time Resolution," *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 2, pp. 212-220, 1996

/22/ D.Raič, "Method for switching noise reduction", *Electronics Letters*, vol. 35, pp. 1794-1795, October 1999.

/23/ D.Raič, "Switching noise in distributed clock systems", *Informacije MIDEM*, vol. 31, pp. 264-268, December 2001.

Dr. Dušan Raič
Faculty of Electrical Engineering
Tržaška 25, Ljubljana, Slovenia
E-mail: dusan.raic@fe.uni-lj.si

Prispelo (Arrived): 06.06.2002 *Sprejeto (Accepted): 20.11.2002*