UDK621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 36(2006)1, Ljubljana

LIMIT CYCLES IN HIGH ORDER ΣΔ MODULATORS

D.Strle

University of Ljubljana, Faculty for Electrical Engineering, Ljubljana, Slovenia

Key words: ΣΔ modulators, limit ajcles, dithoring

Abstract: Limit-cycles generated in ΣΔ modulators are analysed and discussed in this paper. Simulation results of two high order modulators are presented together with techniques to reduce limit cycles. The procedure is limited to general single loop ΣΔ modulators. Simulations are based on a general state-space description, which is applicable to general single loop architecture with one or multi bit internal ADC and/or DAC. Simulation results prove that high order modulators are as susceptible to limit-cycles as low order modulators are, which is in contrast to what is generally believed. To reduce the probability of the appereance of limit cycles a method called dithering is used to reach ultimate performance. Simulation results of 2nd and 5th order modulators are presented, and the method's efficiency is discussed.

Limitni cikli pri ΣΔ modulatorjih visokega reda

Kjučne besede: ΣΔ modulatorji, limitni cikli, tresenje

Izvleček: V prispevku analiziramo in prikažemo limitne cikle, ki se generirajo v ΣΔ modulatorjih višjega reda. Predstavljeni so simulacijski rezultati modulatorja 2. in 5. reda skupaj z metodo eliminacije limitnih cilkov. Metoda analize je primerna za splošne modulatorje prvega reda z enim filtorm v zanki. Simulacije bazirajo na splošnem opisu v prostoru stanj, ki ga lahko uporabimo za poljuben modulator višjega reda z eno ali več bitnim notranjim kvantizatorjem in D/A pretvornikom. Simulacijski rezultati kažejo, da tudi modulatorji visokega reda niso imuni na tvorbo limitnih cilklov, kar je v nasprotju s splošnim prepričanjem. Da bi zmanjšali verjetnost pojava limitnih ciklov pri ekstremnih zahtevah uporabimo metodo tresenja (dither). Simulacijski rezultati dokazujejo uporabnost metode za modulatorje višjega reda.

1. Introduction

Over-sampling and noise shaping are efficient techniques for increasing the resolution of a quantizer by trading the quantizer's accuracy for circuit speed, possibly resulting in a high resolution A/D or D/A converter using only a 1-bit quantizer /1/. The resulting circuitry is simple, robust and has very good distortion properties, so it is very suitable for numerous integrated applications mainly because of modest matching requirements. This principle has been known for a long time but the modulator models' theoretical concepts are restricted. Usually linearization of a quantizer is used to understand basic principles and behaviour. Unfortunately, such simplification blurs some important aspects of the behaviour, so it is supplemented by long term time domain simulations of a nonlinear model and an FFT, which uncover some aspects of the behaviour but do not give a general overview of the problem. Because of the system's nonlinearity and complexity, an analytic solution exists only for a 1st order modulator /2/ and partly for a 2nd order /3/, while for higher order modulators only approximate analytical models exist. None of them gives a complete qualitative and quantitative understanding of the behaviour. In reality the modulator is not an ideal A/D converter because of non-ideal circuit effects and because of the appearance of limit cycles, which lead to undesirable tonal behaviour of a bit-stream and state variables. This article will analyse the appearance of limit cycles using long term time domain simulations of a nonlinear model of a modulator and an FFT.

It is well known that a 1st order modulator has tonal quantization noise spectra /2/. It was believed that for high order modulators (N≥2) the in-band tones inside the quantization noise are reduced by the loop filter's high-pass noise transfer function (NTF). However, limit-cycles are formed because of the quantizer's nonlinearity. They have very high amplitudes close to $f_s/2$ and a still unacceptable level in the base-band. In addition they may live only for a short time due to some special conditions that may exist due to different circuit conditions (offset voltage, input DC voltage, AC voltage of high or small amplitudes, etc.). Empirical observations of a 2nd order modulator show that tones with frequencies dependent on DC input voltage are generated with frequencies f_T and amplitudes attenuated with NTF of a loop-filter /1/:

$$f_T(n)=\frac{n\, f_s |A_{DC}|}{2\Delta} \qquad n=\{0,1,2,\ldots\} \qquad (1.1)$$

Tones at low and high frequencies are dangerous because they may reduce the S/N ratio. Those in the base-band are attenuated by NTF. Their rms values may be higher than noise in a base-band and thus directly reduce the S/N ratio. The tones close to $f_s/2$ usually have very high amplitudes and may be eventually translated to the base-band by some nonlinear process, sampling or cross-talk; especially dangerous to the references is cross-talk. It is therefore necessary to understand the behaviour as well as possible to be able to predict the tones and to use an appropriate technique for minimizing the probability of tone formation and existence. For ultimate performance modulators limit-cycles must be broken by adding an appropriately shaped dither signal. If an A/D converter is to be used for any "acoustic device" or for very narrow-band signal conversion, than the smallest number of tones that are even smaller than the level of total noise in the base-band could reduce the S/N ratio considerably /4/. Generally the in-band tones with rms values below the rms noise level in the whole band are not dangerous. Unfortunately, out-of-band spectral components coupled with the reference voltage through substrate connection or supply voltage are very dangerous because they are not attenuated and have very large amplitudes; they can be easily transferred to the base-band by some nonlinear process or cross-talk.

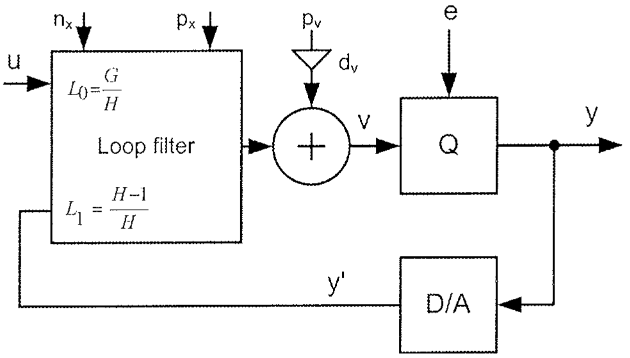


Figure 1: *State-space model of a modulator*

The paper is organised as follows. Section 2 presents a state-space model of a general single loop modulator. It includes circuit noise sources and dithering inputs. Section 3 presents some simulation results for 2^{nd} and 5^{th} order modulators showing tonal behaviour in the base-band and at high frequencies close to $f_s/2$ as a function of different conditions. Section 4 summarises the results and concludes the paper.

2. State-space model of a modulator

A discrete-time modulator can be efficiently represented by its state-space model shown in Figure 1 and described by equation using integrator outputs x(n) as state-variables, v(n) as the loop filter's output, y(n) as a quantizer's output (bit-stream of a one bit modulator) and u(n) as the input signal. The topology is defined by state transition matrix **A**, vector of input signal connections **b** and vector of reference connections **r**, while vector **c** defines the linear combination of state-variables forming the loop filter's output v(n). Different dither signals can be added to the model: p_V is a pseudo-random signal with an appropriate PDF connected to a quantizer's input through weight d_v and $\mathbf{p}_x$ is a vector of different dither signals possibly connected to the state variables through diagonal matrix $\mathbf{Id}_x$. For S-C implementation the kT/C noise sources are added through noise vector $\mathbf{n}_x$ and connected to state-variables through matrix $\mathbf{N}_X$ /5/.

$$\begin{aligned} v(n) &= \mathbf{c}^T\mathbf{x}(n)+d_v p_v(n) \\ \mathbf{x}(n+1) &= \mathbf{A}\mathbf{x}(n)+\mathbf{b}u(n)+\mathbf{r}y(n)+ \\ &\quad +\mathbf{Id}_x\mathbf{p}_x(n)+\mathbf{N}_x\mathbf{n}_x(n) \qquad (2.1) \\ y(n) &= Q\{v(n)\} \end{aligned}$$

No other constraints limit the modulator's topology in Figure 1 except that the D/A converter is for now assumed ideal and therefore $y' = y$. An analytical solution, which would give general and qualitative results of this nonlinear system does not exist at the moment and is beyond the scope of this paper. The formulation above is used only for efficient simulations of a general, high order, single loop modulator with a one bit quantizer. The next section presents simulation results and tonal behaviour of 2^{nd} and 5^{th} order modulators using a state-space description defined in equation (2.1).

3. Simulation results

3.1. LP 2^{nd} order modulator:

Let us start with a known 1-bit 2^{nd} order modulator with f_{OVS} = 4MHz. We are interested in the spectral components and the S/N ratio as functions of input DC voltage, the state variables' initial conditions, dither signal, presence and level of circuit noise and level of AC input signal voltage amplitude. Simulation of a standard 2^{nd} order modulator implemented with the S-C technique is performed here. An AC signal with amplitude of a_{in} = 58μV and frequency f_{in} = 3.7 kHz is connected to the input to have a reference, while DC input voltage is swept from approx. -4.5mV to +4.5mV in 51 steps. The PSD of y(n) is calculated using the FFT of 2^{18} (262,144) samples. Noise sources (dither and kT/C) are switched on or off to generate two different groups of results. The dither signal used is a binary, pseudo-random signal with weight 0.5 and length L = 2^{16}. It is connected to a quantizer's input. The results in Figure 2 present a 3D plot of a PSD of bit-stream y(n) in the base-band when dither and kT/C noise sources are switched off. The frequency is plotted on the x-axis, DC input voltage on the y-axis and PSD relative to 1Vrms on the z-axis. As expected we observed many tones whose amplitudes and frequencies depended on the DC input voltage. These tones have sufficient energy in the base-band to be able to corrupt the S/N ratio.

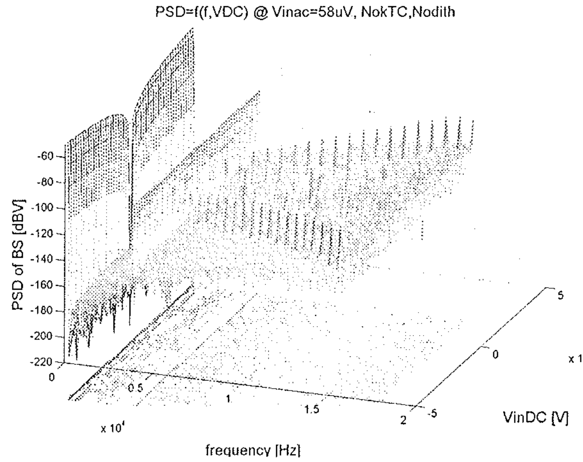


Figure 2: *PSD of a Mod2 bit-stream: no dither and no kT/C*

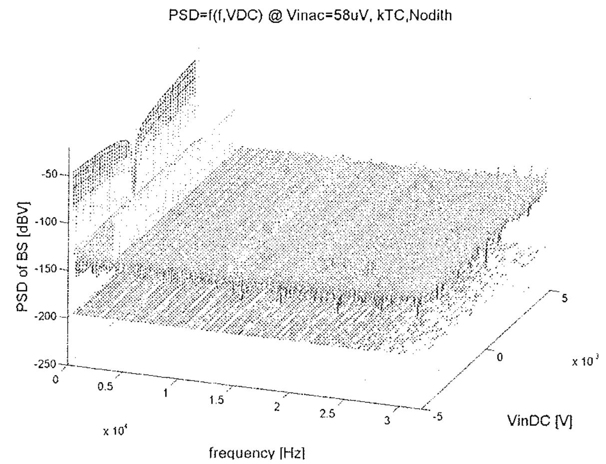


Figure 3: *PSD of a Mod2 bit-stream: no dither, kT/C noise included*

Figure 3 shows the same modulator when the dither signal is switched off but circuit noise and kT/C noise sources corresponding to the S-C implementation are switched on. We could immediately see that the low frequency portion of the spectrum was covered with "thermal" noise, but tones in higher frequencies in the base-band are not affected; they are approximately the same in frequency and power as before. The message from that experiment is that only kT/C noise cannot decorrelate low frequency (and also high frequency) tones. It would be possible to "cover" the base-band tones by increasing the kT/C noise level but this would decrease the S/N ratio in the base-band, so this approach is of little benefit. In addition, high frequency tones remain unchanged as will be shown in the next subsection. Adding the dither signal efficiently decorrelates limit-cycles in the base-band as shown in Figure 4.

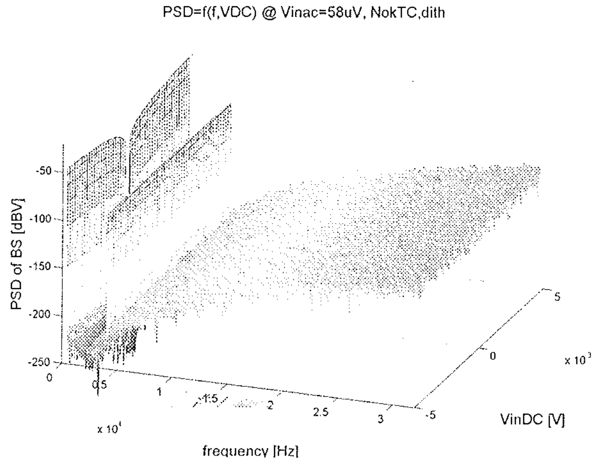


Figure 4: *PSD of a Mod2 bit-stream: dither included, no kT/C noise*

A dither signal has a flat spectrum and is connected to a quantizer's input or it could be HP shaped and connected to a second integrator's input. We can see that the tones' peak amplitudes are reduced for more than 10dB at high frequencies and even more at low frequencies, but at the same time the base-band noise floor has increased slightly. Additionally, the modulator's S/N ratio is reduced by approximately 3dB because part of the second integrator's voltage range has been consumed by dither "noise." Decorrelation of tones at high frequencies close to fs/2 is even more dramatic, as will be shown later.

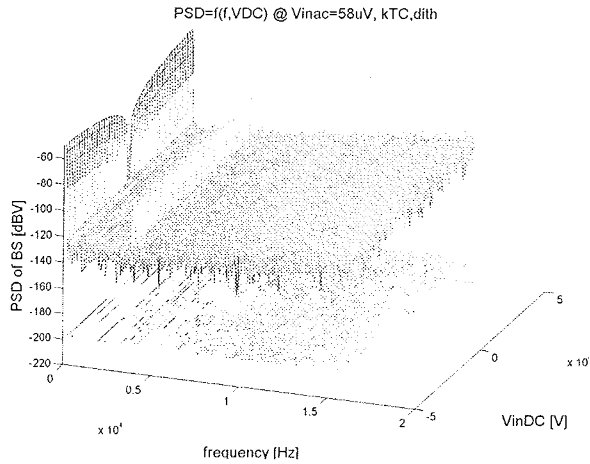
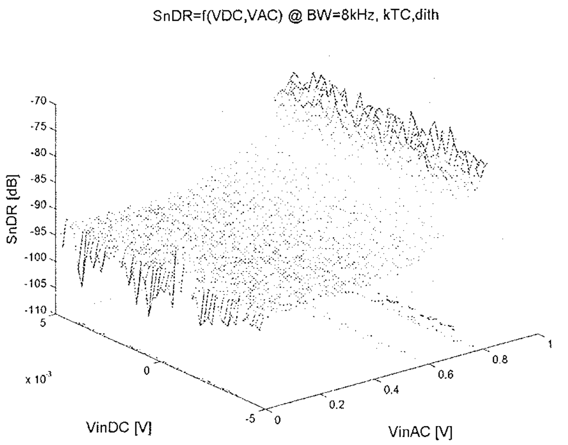


Figure 5: *PSD of a Mod2 bit-stream: dither included, kT/C noise included*

Figure 5 shows a bit-stream's real spectrum when a dither signal is applied and all circuit noise sources are switched on. The noise floor in that case is approximately flat in the base-band and tones are almost completely eliminated in the base-band and also at high frequencies close to $f_s/2$, so the chance of cross-talk is greatly reduced.

The conclusion from this experiment is that kT/C noise alone is not sufficient to eliminate tones in the base-band and at high frequencies for a 2nd order modulator. A suitable dither signal must be used to achieve that goal. The improvement is much more dramatic for a smaller bandwidth where the tone power's relative contribution might be much bigger than the noise floor's power. Because integrators are analogue modules with unpredictable offsets that change with stress, temperature, supply voltage, etc., "tones" can move around the base-band as a function of external conditions and may corrupt the A/D conversion process. It is therefore important to eliminate or at least reduce the potentially harmful tonal behaviour of any ΣΔ modulator using appropriate techniques.

To further investigate a mod2's behaviour with regard to its tonal behaviour under different conditions, a mod2 was simulated using different DC and AC input voltages. The maximum possible Signal to Noise and Distortion ratio (SNDR) has been calculated and plotted on a 3D plot shown in Figure 6. Dither and kT/C noise have been switched on. Noise level in the base-band is measured for each pair of AC and DC input voltages and is compared to the maximum possible input signal's rms voltage before overload starts to reduce the SNDR. For input signals around signal ground with amplitudes from 0 up to ~$0.58V_{ref}$, the SNDR is more



SnDR=f(VDC,VAC) @ BW=8kHz, kTC,dith

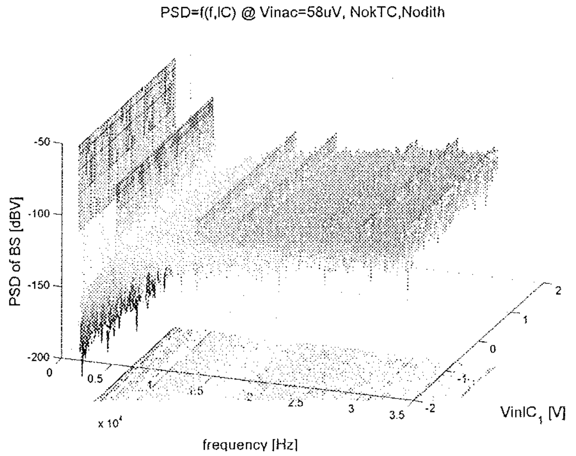
Figure 6: *PSD=f (DC, AC); dither and kT/C included*

than 90dB in the 8 kHz bandwidth. Tones in the base-band have been eliminated or at least reduced below the noise floor. In addition, the noise level is approximately constant for all amplitudes up to 0.7V, while the noise level starts to increase at higher input voltages, which suggests the biggest useful input voltage taking into consideration the integrator model that includes the limitation of the state variable voltages due to real circuit behaviour.

The major limitations to reaching better performance are quantization noise and kT/C noise. Both can be improved; the first one by increasing the over-sampling ratio and the second by increasing the capacitances of input switched capacitors.

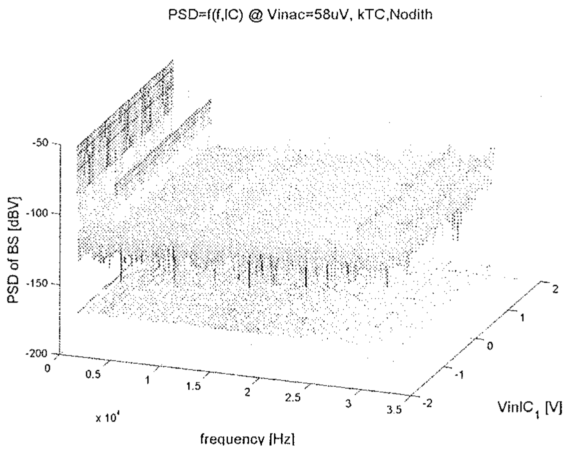
In the literature /1/ we saw many statements that the limit-cycles depend also on the state variables' initial conditions. To test that we performed simulations and analysis of a 2nd order modulator at a fixed DC input voltage ($V_{ref}/1024$), fixed AC input voltage of $a_{in} = 58\mu V$ and different conditions regarding kT/C noise and dither, changing the initial conditions. The same experiment was performed first with a 2nd order modulator and then also with a 5th order modulator. The same initial conditions for all state-variables were used, which varied from $-3.3V_{ref}$ to $+3.3V_{ref}$. A bit-stream's PSD is observed and plotted on a 3D plot with frequency on the x-axis, initial condition voltage on the y-axis and PSD on the z axis for different combinations of dither and circuit noise. The results are presented in Figure 7 through 10.

The analysis of simulation results shows that at least for the stated conditions (60uV AC input signal and fixed DC input voltage $V_{ref}/1024$) the tones' frequencies and amplitudes do not depend on the initial conditions. As before, we can see that by using appropriate dither and circuit noise the tones can be almost completely eliminated as shown on Figure 10. The remaining tones seem independent of the initial conditions. Unfortunately these experiments do not prove that limit cycles are independent of initial conditions because we could not test all possible combinations of different conditions.



PSD=f(f,IC) @ Vinac=58uV, NokTC,Nodith

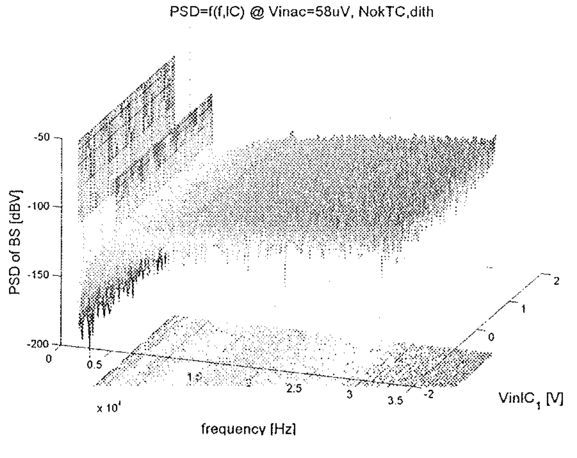
Figure 7: *Tones as a function of initial conditions (IC); no dither, no kT/C*



PSD=f(f,IC) @ Vinac=58uV, kTC,Nodith

Figure 8: *Tones as a function of initial conditions (IC); no dither, kT/C*

As we mentioned previously, very dangerous tones are generated at high frequencies close to $(f_s/2)$. These types of limit cycles are formed for any kind of input signal even in the presence of a high amplitude AC input signal. They are not



PSD=f(f,IC) @ Vinac=58uV, NokTC,dith

Figure 9: *Tones as a function of initial conditions (IC); dither, no kT/C*

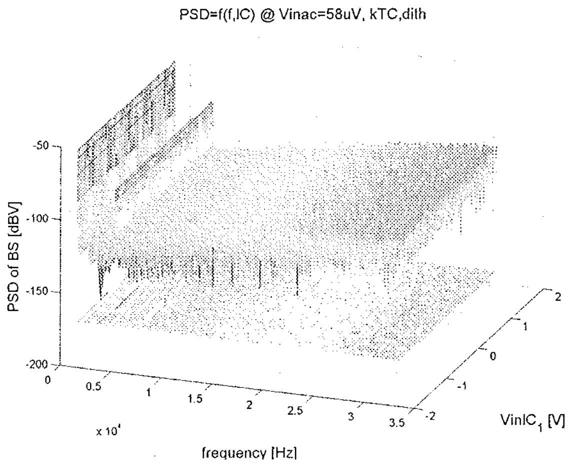


Figure 10: *Tones as a function of initial conditions (IC); dither, kT/C*

dangerous by themselves because they are out of the band and are attenuated by the decimation filter. Unfortunately, they may be transferred back to the base-band by some nonlinear process or by cross-talk to the input or, for example, through the references. Simulations of a standard 2nd order modulator were performed with sine-wave signals having amplitudes from 1uV to maximum input voltage of $V_{ref} / \sqrt{2}$.

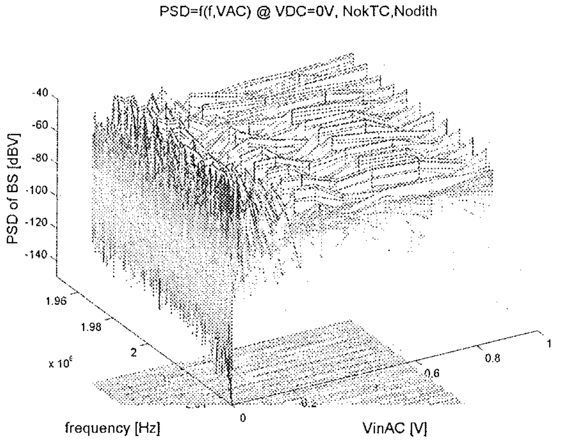


Figure 11: *PSD of y (n) at high frequencies; no dither, no kT/C*

A bit-stream's PSD is observed in a band between $(f_s/2)$ - 80kHz and $(f_s/2)$ as a function of frequency and input signal amplitude at a fixed DC input voltage of $(V_{ref}/1024)$.

The results are presented on four 3D plots shown in Figure 11 through Figure 14. In all cases the x-axis is the frequency, the y-axis represents the amplitude of a sine wave and the z-axis shows the bit-stream's PSD.

It is obvious that when dither is switched off many tones at high frequency are present (Figure 11). Their amplitudes are higher than the level of quantization noise, and the frequencies and amplitudes depend on the input AC signal's amplitude.

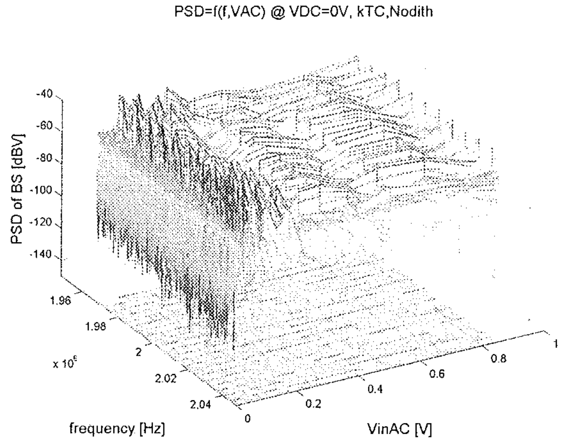


Figure 12: *PSD of y (n) at high frequencies; no dither, kT/C*

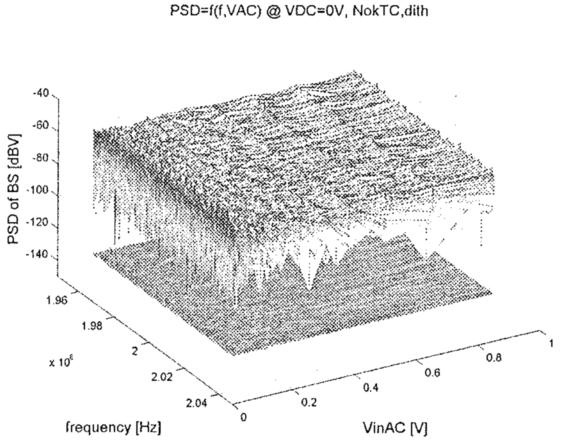


Figure 13: *PSD of y (n) at high frequencies; dither, no kT/C*

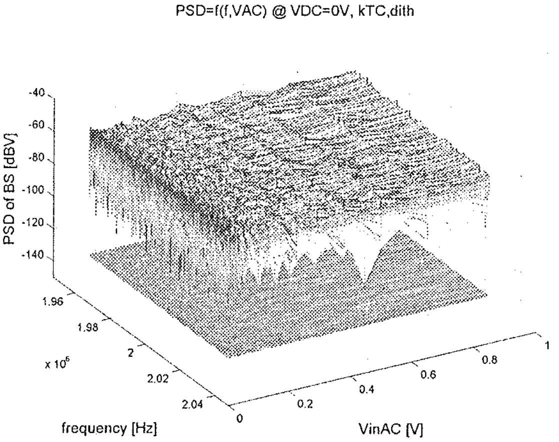


Figure 14: *PSD of y (n) at high frequencies; dither, kT/C*

The addition of kT/C and thermal noise to the structure, which corresponds to S-C stages, does not break the HF limit cycles or improve the tonal behaviour as demonstrated in Figure 12. The HF tonal behaviour is greatly improved if a dither signal is applied to a quantizer's input, independent of kT/C noise as shown in Figure 13 and Figure 14.

From these simulations and analyses we can conclude that applying an appropriate dither signal and an appropriate level of circuit noise almost completely removes tones in the base-band as well as at high frequencies. The price paid is a small reduction in the maximum achievable SNR ratio because part of the last integrator's voltage range is occupied by the dither signal; this loss is in the range of 2 to 3dB.

3.2 LP 5th order modulator:

The same technique used for the 2^{nd} order modulator is used for the 5^{th} order modulator with a 1 bit quantizer. Again, simulations of an ideal modulator demonstrate tones in the base-band dependent on DC input voltage as shown in Figure 15. Adding kT/C noise just covers low frequency tones. Higher frequency base-band tones remain unchanged as can be observed in Figure 16. Therefore, without using a dither signal it does not make sense to decrease the input switched capacitors' kT/C noise too much because sooner or later the tones in the base-band will limit the (S/N) ratio.

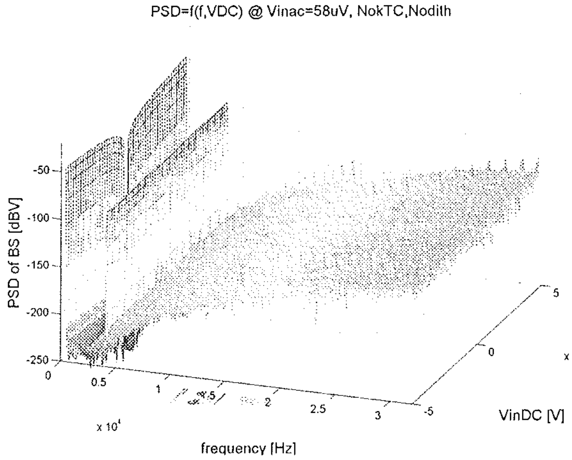


Figure 15: PSD of a mod5; no dither, no kT/C

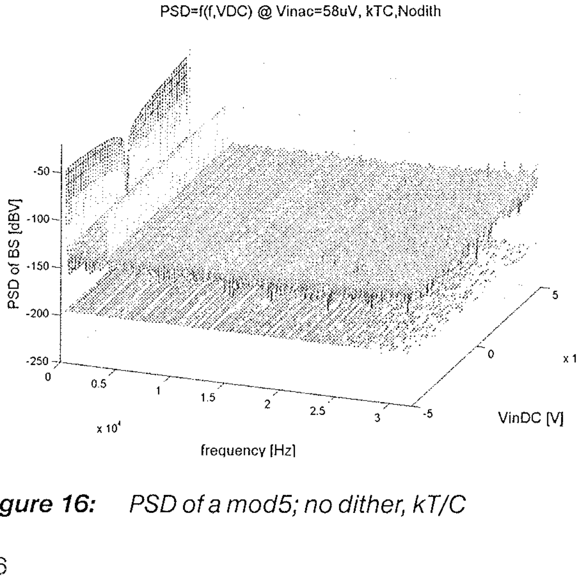


Figure 16: PSD of a mod5; no dither, kT/C

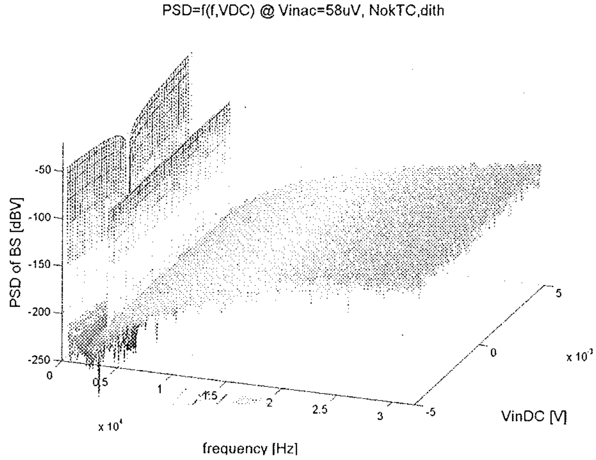


Figure 17: PSD of a mod5; dither, no kT/C

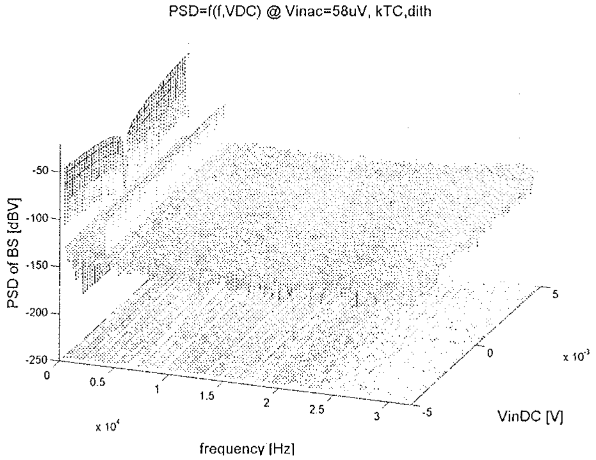


Figure 18: PSD of a mod5; dither, kT/C

Adding a dither signal to a quantizer's input efficiently decorrelates limit-cycles in the base-band as shown in Figure 17. A real situation including dither and kT/C noise is depicted in Figure 18, which looks similar to Figure 16 with the important difference that in this case tones at higher frequencies of a base-band are eliminated.

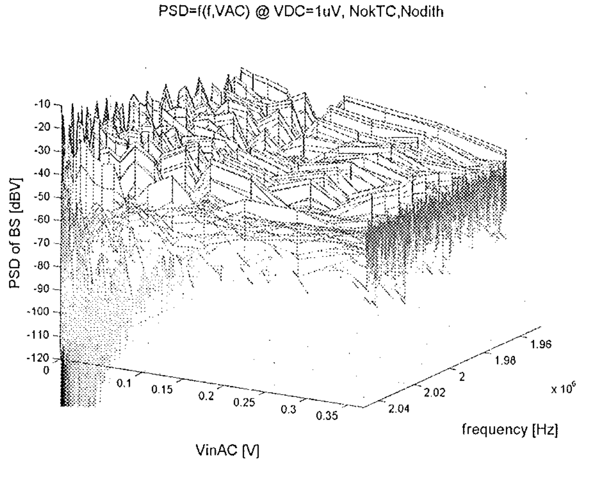


Figure 19: PSD of a mod5 at HF; no dither, no kT/C

In-band tones of a 5th order modulator have less power in general than a 2nd order modulator because the NTF has greater attenuation of quantization noise in the base-band; unfortunately the demands for the S/N ratio are bigger. Again, tones can be eliminated using dither and kT/C noise. As before, not only base-band tones are dangerous but also high frequency tones because they could be translated to the base-band by some nonlinear process or, for example, a cross-talk mechanism.

The high frequency behaviour of an ideal 5th order modulator is presented in Figure 19 through Figure 22. The PSD of a quantization noise in a band 80 kHz away from $f_S/2$ is presented as a function of AC input voltage. All 3D plots have input signal amplitudes on the x-axis, frequency on the y-axis and the bit-stream's PSD on the z-axis.

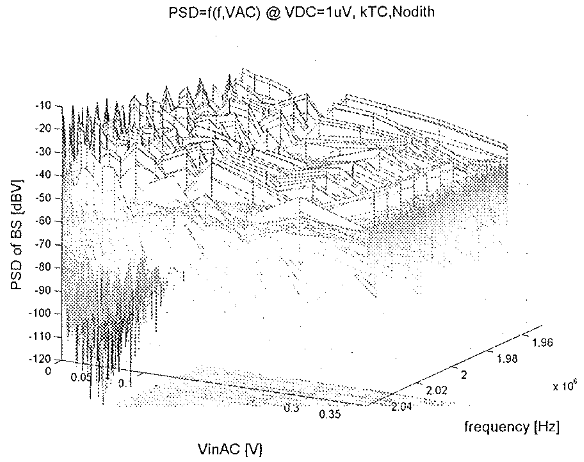


Figure 20: *PSD of a mod5 at HF; no dither, kT/C*

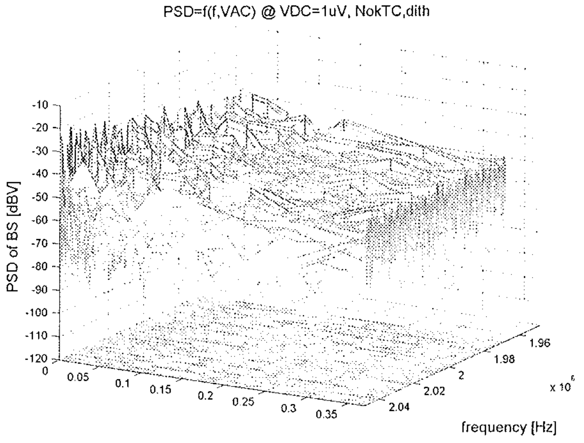


Figure 21: *PSD of a mod5 at HF; dither, no kT/C*

As before, the kT/C noise alone does not change HF limit-cycles as we can see from Figure 19 and Figure 20. Their frequencies and amplitudes depend on the applied amplitude of the AC signal. The most dangerous tones are those with frequency close to $f_S/2$ because they can be aliased to the base-band; their amplitudes are very big compared to the level of the signal, so even the smallest cross-talk, which has, for example, 100dB of attenuation, will degrade the performance.

Applying a dither signal to a quantizer's input reduces the amplitudes of tones at HF by more than 10db. This is a significant improvement, while the penalty in SnR is only ~3dB. Further reduction of HF tones is possible by applying a frequency shaped dither signal to the modulator.

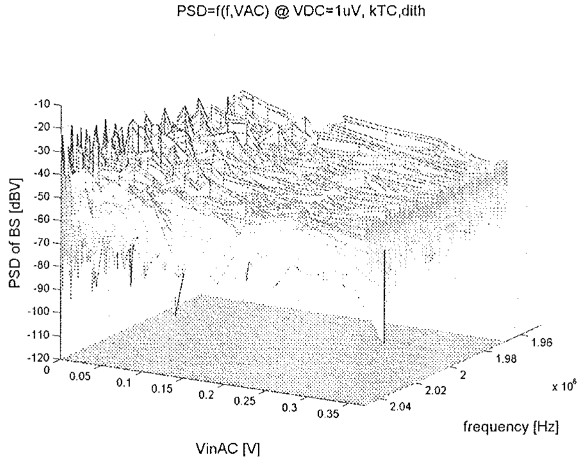


Figure 22: *PSD of a mod5 at HF; dither, kT/C*

4. Conclusion

A new state-space model of a general single loop ΣΔ modulator including kT/C noise sources and dither inputs and sources has been developed and used. Thanks to modern computers' high computing power it is fairly easy to simulate the tonal behaviour of any single loop modulator in a short time. For a 2nd order modulator it is proven that the quantization noise spectrum consists of tones whose frequencies depend on DC input voltage. They can be greatly reduced by applying appropriate dither to the modulators' state variables. Thermal and kT/C noise alone cannot decorrelate the modulators' tonal behaviour, so an appropriate dither signal is needed. Describtion of dither signal is beyond this paper's scope. A dither signal's effect is even greater on the quantization noise's HF part, which reduces the chance of HF tones appearing in the base-band due to some cross-talk mechanism. Further research will focus on an analytical solution and the study of tonal behaviour as a function of different parameters, signals and dither signals connected to the modulators' loop filter's state-variables.

5. References

/1/ R. Schreier, G.C. Temes, "Understanding Delta-Sigma Data Converters," Wiley Interscience, 2005

/2/ R.M.Gray, "Quantization Noise Spectra," IEEE Trans. Inform. Theory, Nov. 1990.

/3/ S.Mann, D.Taylor, "Limit Cycle behaviour in the double loop band-pass Sigma-Delta A/D converter," IEEE Trans CAS.II, Analogue and digital Signal Processing, vol .46, Aug.1999.

/4/ C. Dunner and M. Sandler, "A comparison of Dithered and Chaotic Sigma-Delta Modulators," J. Audio Eng. Soc., VOl. 44, No. 4, pp.227-244, Apr. 1996.

/5/ D.Strle, "Capacitor-area and power-consumption optimization of high order Ó-Ä modulators," Inf. MIDEM, 2001.

D.Strle,
University of Ljubljana, Faculty for Electrical Engineering, Tržaška 25, Ljubljana, Slovenia

Prispelo (Arrived): 03. 01. 2006; Sprejeto (Accepted): 30. 01. 2006