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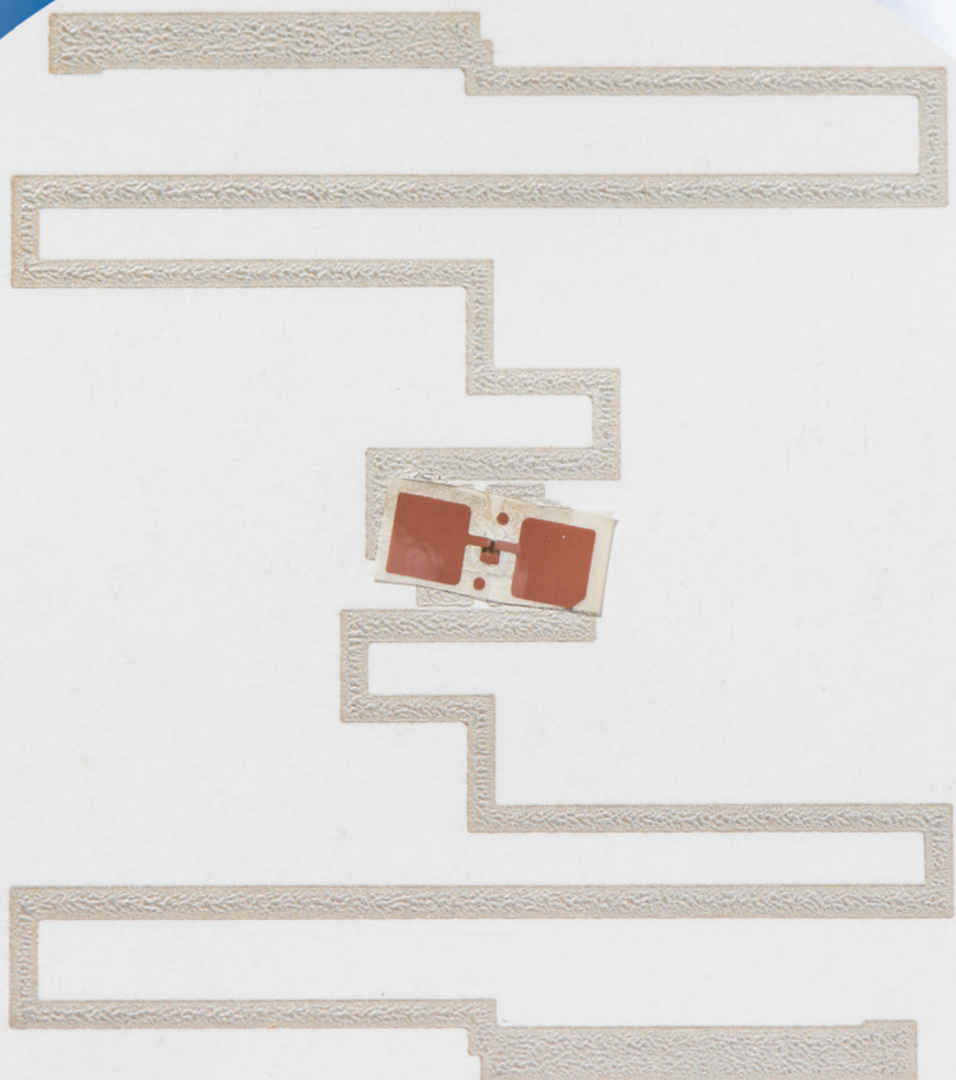

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Printed antenna with integrated chip (M. Đokić et al.)
(*photo by Jure Ahtik*)

Naslovnica:
Tiskana antena z integriranim vezjem (M. Đokić et al.)
(*foto: Jure Ahtik*)

Editorial | Uvodnik

Dear Reader,

This issue brings seven original scientific papers and four professional articles. The later are the last of this kind, since Editorial Board decided on December meeting that professional articles will not be considered for publication any more. Editorial Board agreed that peer-reviewed contributions published in the Journal are:

- review scientific papers (only upon invitation)
- original scientific papers.

Institutional support for our journal has been decreasing in the last two years. To cover publishing costs and to secure continuation of quality growth we introduced page charges for papers published in the journal. Nevertheless, we will continue to provide a free electronic access to all papers published in *Informacije MIDEM* –Journal of Microelectronics, Electronics Components and Materials (since 1986).

We sincerely hope you will receive all changes with understanding and look forward to receiving your next manuscript(s) in our inbox (editor@midem-drustvo.si).

Prof. Marko Topič
Editor-in-Chief

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Original scientific paper

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Comparison between the characteristics of screen and flexographic printing for RFID applications

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Abstract: In this paper, we investigated and compared the characteristics of novel smart card RFID antennas which were printed using two different fabrication technologies: industrial screen printing and industrial flexographic printing. After the printing process, the drying processes were optimized separately for each of the printing techniques in order to achieve optimal performances for the proposed antennas. The characteristics of the antenna were analysed by measuring several parameters such as resistance, backscattered power, antenna impedance and return loss. The effect of the lamination process on the readability and operability of the final cards were analysed in detail. The possibility of using the printing processes in the realization of RFID antennas was investigated in terms of fabrication speed, and repeatability of the printing. We have proved that industrial screen printing and flexographic printing techniques can be used equally well for producing RFID smart cards. Flexographic printing has proved to be a faster solution, but screen printing has shown higher repeatability.

Keywords: smart cards; printed antenna; RFID; screen printing; flexographic printing

Primerjanje lastnosti sito in fleksotiska za aplikacije RFID

Izvleček: V članku smo raziskovali in primerjali lastnosti novega dizajna anten RFID za pametne kartice. Antene so bile natisnjene z različnima tehnologijama: z industrijskim sitotiskom in fleksotiskom. Po tiskanju se je optimiziral postopek sušenja za vsako tehnologijo tiska posebej, da bi dosegli najboljše delovanje anten. Lastnosti antene smo analizirali z merjenjem velikega števila parametrov, kot so upornost, moč povratnega signala, impedanca antene in izguba povratnega signala. Podrobno smo analizirali tudi vpliv laminacije na končno berljivost in delovanje kartic. Možnost izdelave anten RFID z različnimi tehnologijami tiska smo proučili glede na hitrost izdelave in ponovljivost tiska. Dokazali smo, da se lahko industrijski sitotisk in fleksotisk uporabljata za izdelavo pametnih kartic RFID. Fleksotisk se je izkazal kot hitrejša rešitev, sitotisk pa omogoča boljšo ponovljivost.

Ključne besede: pametne kartice; tiskana antena; RFID, sitotisk; fleksotisk

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1 Introduction

The demand for RF and wireless systems that require low cost and high performance has been growing rapidly over the last decade. Radio frequency identification (RFID), one of the key technologies in the fast-growing printed electronics industry, uses an electromagnetic field to transfer data.

An RFID system consists of a tag that contains an integrated circuit (IC) chip and an antenna, and has the ability to respond to radio waves transmitted from an RFID reader. The main advantages of an RFID system are the non-contact and non-line-of-sight characteristics of the technology used. Because of those characteristics, RFID is suitable for operation in a variety of working conditions where there is, for example, dust, snow, ice, dirt, stress, humidity, etc. [1]. RFID is currently used in many applications such as medical products, pharmaceutical logistics, vehicle security, transportation, contactless payment, etc. [2].

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Printed electronics, such as RFID, may be printed using different technologies. Conventional printing processes are much faster and better suited to printing large areas than is the case with digital printing processes [3]. For example, inkjet printing [3-5], as a representative of the digital printing process, is very accurate but relatively slow. On the other hand, some conventional technologies, like flexographic-printing [6-8] or screen-printing [9-12], are suitable for large area printing and mass production. These technologies are characterized by high production speed, high resolution and the possibility of printing a number of different functional (conductive) inks [13]. Screen printing is a special type of stencil printing, which means that, in the printing process, the ink passes through the screen and onto the substrate. Flexographic printing, unlike screen printing, uses soft, flexible printing plates which were formerly made solely from rubber but are now usually made from photopolymers. Low pressure applied between the plate cylinder and substrate is sufficient to transfer the ink from the plate cylinder to the substrate [14].

Ink selection is one of the essential steps in the printing process. Besides conventional process printing inks, there are many types of functional printing ink available on the market today such as conductive, dielectric, electrochromic, thermochromic, etc. Conductive inks are far more expensive than conventional inks, and it is therefore necessary to find the best price and keep consumption to a minimum. [15] The factor of price is of great significance in mass production, since the final price of a single tag is a major barrier to greater popularization and application [16, 17].

In this paper, we studied and compared the characteristics of screen- and flexographic-printed UHF antennas. The proposed UHF folded dipole antenna was designed using the CST Microwave Studio, an EM simulator. After printing, the drying processes were optimized to achieve optimal performances for the proposed antennas and then chips were integrated with. At the end lamination process was used. The characteristic parameters of the antenna such as resistance, backscattered power, antenna impedance and return loss were measured as well as the operability of the laminated smart card. The possibility of using these printing processes for making of RFID antennas was investigated in terms of fabrication speed and the repeatability of the printing process.

2 Experiments

2.1 Antenna design

The UHF RFID antenna was designed and simulated using the CST Microwave Studio, an EM simulator. The laminated antenna is designed to operate according to the UHF standard with a central operating frequency of 868 MHz. The proposed antenna is folded to fit the size of a standard credit card, with a small or negligible reduction in antenna efficiency. It was designed on polycarbonate film (thickness: 120 µm; grammage: 120 g/m^2; surface roughness, ISO 4288: 2.3 µm) with a relative permittivity of $\varepsilon_r = 3.2$ and a dissipation factor of 0.0019. In simulations, 16 µm of silver were used for conductive material, and conductor losses were modelled using bulk conductivity for silver. The configuration of the proposed folded dipole antenna is shown in Figure 1.

Initially antenna dimensions were determined for the laminated case since the number and thickness of dielectric layers during lamination affects the characteristics of the antenna. Nine dielectric layers were used in the simulation, with the antenna placed between the fourth and fifth layers. Figure 2 shows the simulated return losses and the total efficiencies of the proposed non-laminated and laminated dipole antennas. It can be seen that the fundamental resonance occurs at 868 MHz with reflection better than −10 dB in the case of the laminated antenna. Lamination process significantly influences the resonant frequency of the antenna and its return loss, due to changes in the effective dielectric constant of the substrate and antenna impedance. Non-laminated antenna operates at 930 MHz with reflection better than −7.5 dB. Total efficiency of the proposed laminated antenna obtained using CST Microwave Studio is better than 90% at the resonance. Radiation efficiency of the proposed laminated antenna was also calculated, and it was found to be higher than 95% at the resonance. The efficiency of non-laminated antenna is significantly lower due to the impedance mismatch. Furthermore, it can be mention that the proposed laminated antennas has omnidirectional radiation pattern with the gain of 1.9 dBi.

2.2 Antenna fabrication

The proposed antenna is printed using screen and flexographic printing technologies. Two silver conductive printing inks were used in the printing processes: SunChemical CRSN2442 SunTronic 280 Thermal Drying Silver Conductive Ink for the screen printing and Acheson Electrodag PD-054 for the flexographic printing. SunChemical CRSN2442 is a thermal curing ink, whereas Electrodag PD-054 is a UV curing ink, but successive heat curing is recommended for better results. The

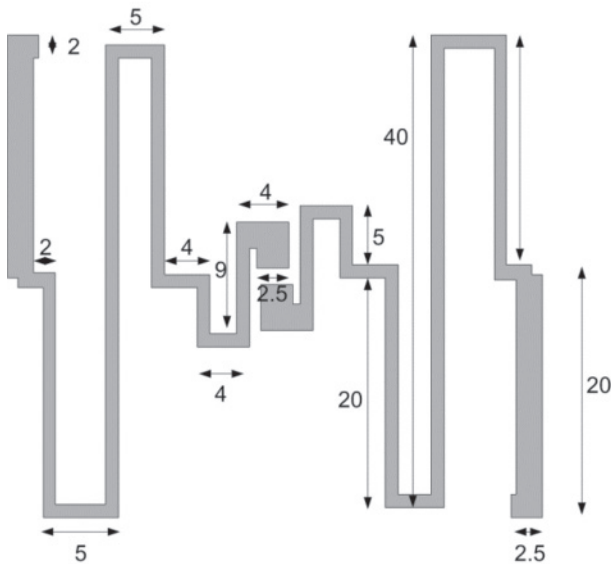


Figure 1: Design of a dipole antenna

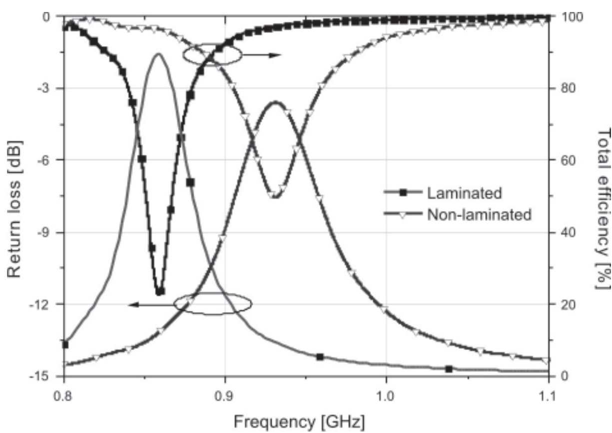


Figure 2: Simulated return loss and total efficiency of the proposed laminated and non-laminated antennas.

characteristics of both inks, with their recommended specifications, are presented in Table 1.

A block diagram of the fabrication process for the antenna is shown in Figure 3. In the screen printing process, antenna samples were printed using the Siasprint Novaprint-P screen printer with a monofilament polyester plain weave mesh of 120 l/cm and a theoretical ink volume of 16.3cm^3/m^2. After printing, the optimal drying process for the ink was determined. Optimal drying was determined to be the point where the sheet resistance of the printed samples became constant irrespective of longer drying time, higher temperature or higher or longer UV exposure. In accordance with the thermal ink specification, the drying was performed in a hot zone tunnel. The tunnel has the ability to heat up to 72 °C (maximal value). Therefore, in order to achieve optimal drying conditions, the maximal temperature was used with a different number of passages through the tunnel until the lowest sheet resistance was obtained. The best results, i.e. the lowest sheet resistances, were obtained when the samples passed through the tunnel seven times (at 72 °C for 30 s).

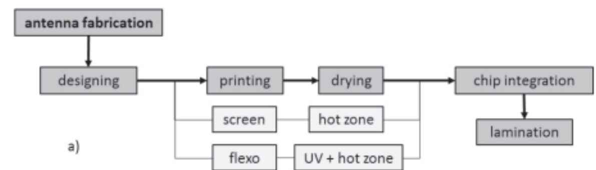


Figure 3: Schemes of smart card fabrication process

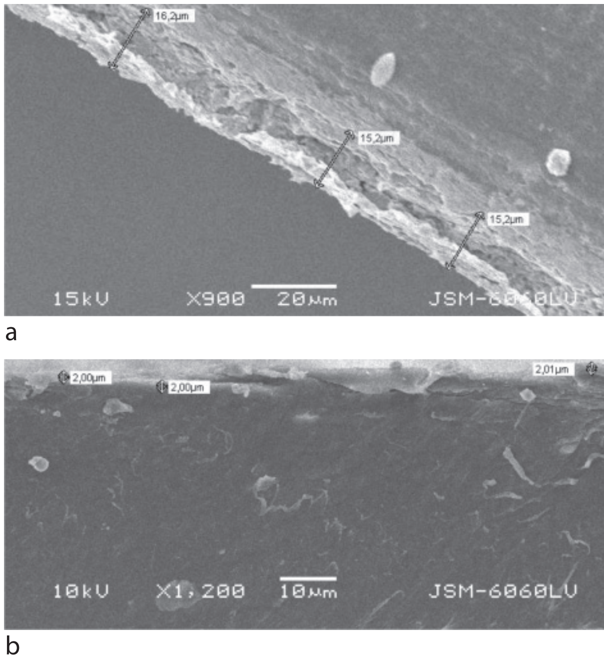
Flexographic antenna samples were printed using an in-line OMET XF 340 flexographic printing machine with eight printing units. All the printing units were equipped with a UV drying unit. The printing machine was also able to dry substrate using hot zone (heat curing/hot air drying), as was the case here. An anilox roller able to deposit large amounts of ink was used for this purpose (screen frequency of 60 cell/cm, cell volume: 30 cm^3/cm^2, cell geometry: hexagonal). The optimal results, with the lowest sheet resistance, were obtained when the substrate was dried seven times under the UV units, and at the maximum temperature in the hot zone at the end. The power of the UV lamps was 160 W/cm and the final printing speed was set to 25 m/min.

On the printed test elements, the thickness of the ink layer was measured using a JEOL JSM-6060LV scanning electron microscope. The measurements were performed on the 10-sample cross section. Figure 4 shows

Table 1: Characteristic properties of the printing inks used.

Printing ink	Solids	Drying condition	Sheet resistance (25 µm layer thickness)
SunChemical CRSN2442 SunTronic 280 (thermal ink)	69–71%	Heat curing / hot zone: 30–90 s at 100–130 °C	10–32 mΩ
Acheson Electrodag PD-054 (UV ink)	100%	UV curing: Fusion "D"; Light intensity 1.4 J/cm2, Power of UV lamp: 160 W/cm Heat curing / hot zone: 60 s at 100 °C	<75 mΩ

the variation in the ink thickness between the screen (Figure 4a) and flexographic (Figure 4b) printed samples.



a

b

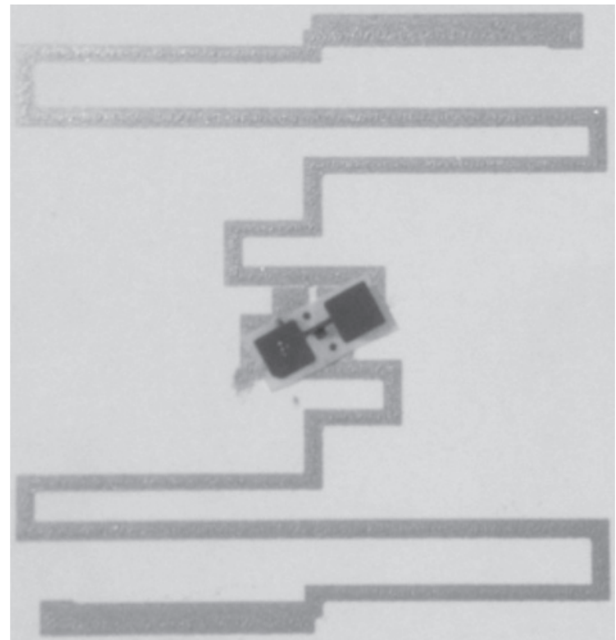
Figure 4: The cross-cuts for the screen- (a) and flexographic printed (b) samples.

The ink layer thickness for the screen prints ranges from 12.2 µm to 16.2 µm with a standard deviation of 2.13, and from 1.26 µm to 6.76 µm with a standard deviation of 1.91 for the flexographic prints. Non-uniformity is much higher in the flexographic prints.

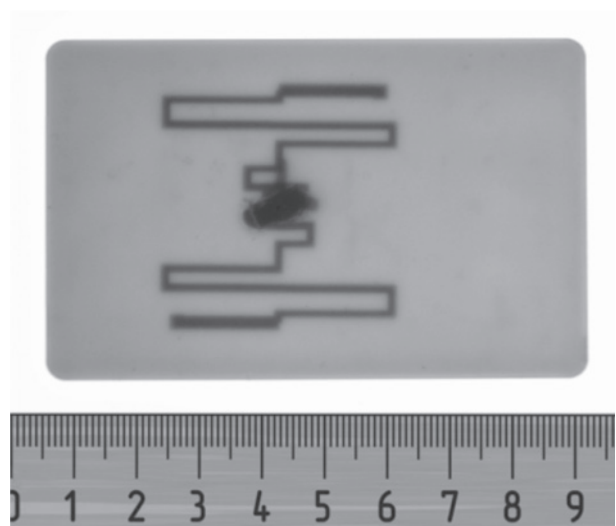
2.3 Chip integration and card lamination

After drying NXP SL3ICS1002/1202 strap chips operating in a frequency range of 840–960 MHz with a characteristic impedance of Z = 22-j195 Ω and a Q-factor of 9 were integrated on the printed antennas. Figure 5a shows a photograph of the printed antenna with the mounted chip. The chips were assembled manually with isotropic conductive glue based on silver particles (Bison ELECTRO glue) and then dried in a thermal oven for 30 minutes at 120 °C.

After chip integration, a lamination process was performed to produce the final smart cards. To begin, in the heat phase, nine foil layers were assembled for 19 minutes at a high temperature of 199 °C and a pressure of 300 N/cm^2. The assembled foils were then exposed in the cold phase for 18 minutes at 25 °C and a pressure of 500 N/cm^2. Lastly, the standard cards were cut into the final standard format (ISO/IEC 7810), as shown in Figure 5b.



a



b

Figure 5: Printed antenna with integrated chip (a), final laminated smart card prototype (b).

3 Measurements and results

A card evaluation is presented in the part of the paper that follows. A block diagram of the evaluation process is shown in Figure 6. To begin, on the non-laminated cards, the sheet resistance and ink layer thickness of the conductive printed lines were measured. Then, using a network analyser, the antenna impedance and return loss of the proposed antenna were evaluated. To conclude, the backscattered power of the non-laminated and laminated smart cards was assessed in a real

environment in order to determine the operability of the final card.

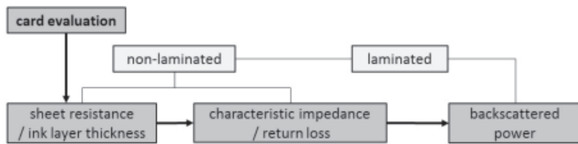


Figure 6: Testing and measurement process

3.1 Resistance measurements

The resistance was determined after drying the screen and flexographic printed samples. Figure 7 shows the printing form for flexographic printing. The printed antennas were positioned in the first three columns, and the test elements were positioned in the last column (vertically to print the length) on the polycarbonate foil in order to determine the resistance and uniformity of the printed conductive lines. The resistance was measured after 24 hours of conditioning with a 50% relative humidity at 23 °C using the Fluke 289 True-rms Industrial Logging Multimeter.

All the resistance measurements were performed on the test elements with a nominal length of 22 mm and a line width of 3 mm. The measurements were performed (along the print length) on each meter for the on-screen prints, while the measurements were performed on each three to five meters of the printed substrate for the flexographic-prints. Each measurement was performed three times on three successive elements.

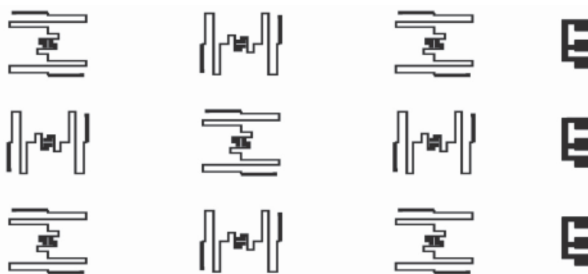


Figure 7: The printing form for flexographic printing: antennas (the three left-most columns), test elements for sheet resistance measurements (the last column on the right).

The results of the resistance measurements for the test elements printed using screen and flexographic printing machines are presented in Figure 8 and Figure 9, respectively.

Note that the average resistance of the screen-printed layer is much lower (1.20 ± 0.12 Ω) than that for the flexographic prints (31.90 ± 9.73 Ω).

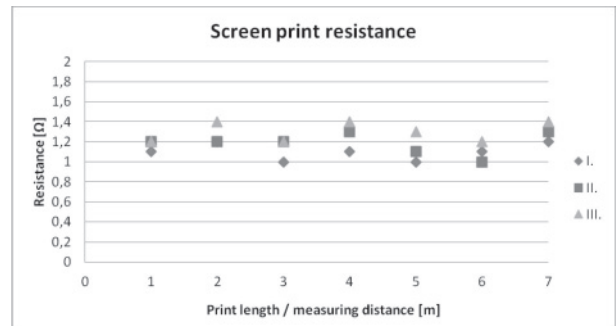


Figure 8: Screen print resistance measured three times on three successive elements (I., II., III.)

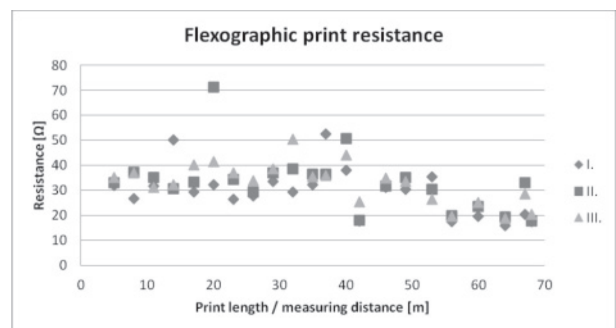


Figure 9: Flexographic print resistance measured three times on three successive elements (I., II., III.)

In terms of print length, the resistance is non-uniform. This is evident especially on flexographic prints, where the standard deviation reaches almost 10 Ω (9.73 Ω). The high ink layer thicknesses on screen printed samples consequently show lower resistance. On the other hand it is clearly evident that the low layer thicknesses for the flexographic printed samples yield resistance values which are almost 30 times higher. The reason for this lies in Ohm law, which states that resistance values are lower when the thickness of the printed conductive layer is higher. The thickness of the conductive layers printed using screen printing ranges from 12.2 μm to 16.2 μm, whereas the thickness for flexographic prints spans from 1.26 μm to 6.76 μm. Another reason is the mixture of conductive ink, where a specification given by the manufacturer shows different specific resistances for each ink. The results achieved demonstrate a high correlation with ink layer thickness.

3.2 Antenna impedance and return loss

The characteristics of the antenna were measured using an Agilent E5071C ENA Network Analyser. An ENA network analyser is used for measuring antenna impedance and return loss. The impedance of the proposed antenna was measured for the non-laminated cards in the anechoic chamber using a simple broadband network analyzer technique for measuring balanced antennas, without a balun described in [18]. The

measured characteristics parameters were summarized in Table 2, where f_r denotes the resonant frequency, s_{11} denotes the return loss at the resonant frequency and *Real (Z)* are real parts of the impedance of the antennas. The real part of the impedance was shown at frequencies where the imaginary part was equal to zero.

The results of some of the characteristic parameters measured were summarized in Table 2 and Figure 10. Figure 10 shows the return loss measured and Smith charts for antennas printed on a flexographic machine (F2) and another for a screen-printed antenna (S4).

Table 2: Measured characteristic parameters of the proposed antennas.

Technology	No. of antenna sample	fr [MHz]	S11 [dB]	Real (Z)/f [Ω/MHz]
Screen				
	S1	913,50	-8,450	22,04/908,44
	S2	929,42	-7,550	20,12/919,54
	S3	925,56	-7,290	19,02/917,36
	S4*	929,91	-7,791	20,21/920,50
Flexographic				
	F1	914,23	-12,018	86,08/924,60
	F2*	937,39	-16,755	67,51/943,40
	F3	923,39	-13,407	78,70/932,80
	F4	924,60	-32,710	52,50/924,60

**Smith charts for the denoted antennas samples are provided below.*

The resonant frequencies of the measured antennas are similar for all antennas printed using both technologies. However, the return losses and the characteristic impedances are much smaller for an antenna fabricated using screen printing technology.

Due to the fact that the thickness of the conductive ink in the case of screen printing was much higher, the inductance of the screen printed antennas was slightly smaller and resistance significantly decreased. It can be seen that the antennas implemented using screen printing show the value of the real part of the impedance to be around 20 Ω, while the imaginary part has an inductive character. On the other hand the antennas fabricated using flexographic printing show a higher value for the impedances – over 50 Ω, but their imaginary part was capacitive at the resonance (Figure 10). The output characteristic impedance of the SL3ICS1002/1202 chip was 22 – j195 Ω at 915 MHz. After mounting the chip on antennas, screen printed antennas show a better level of matching with the real part of the chip impedance. However, despite the higher resistance value for flexographic printing, it shows a better level of matching with its imaginary part.

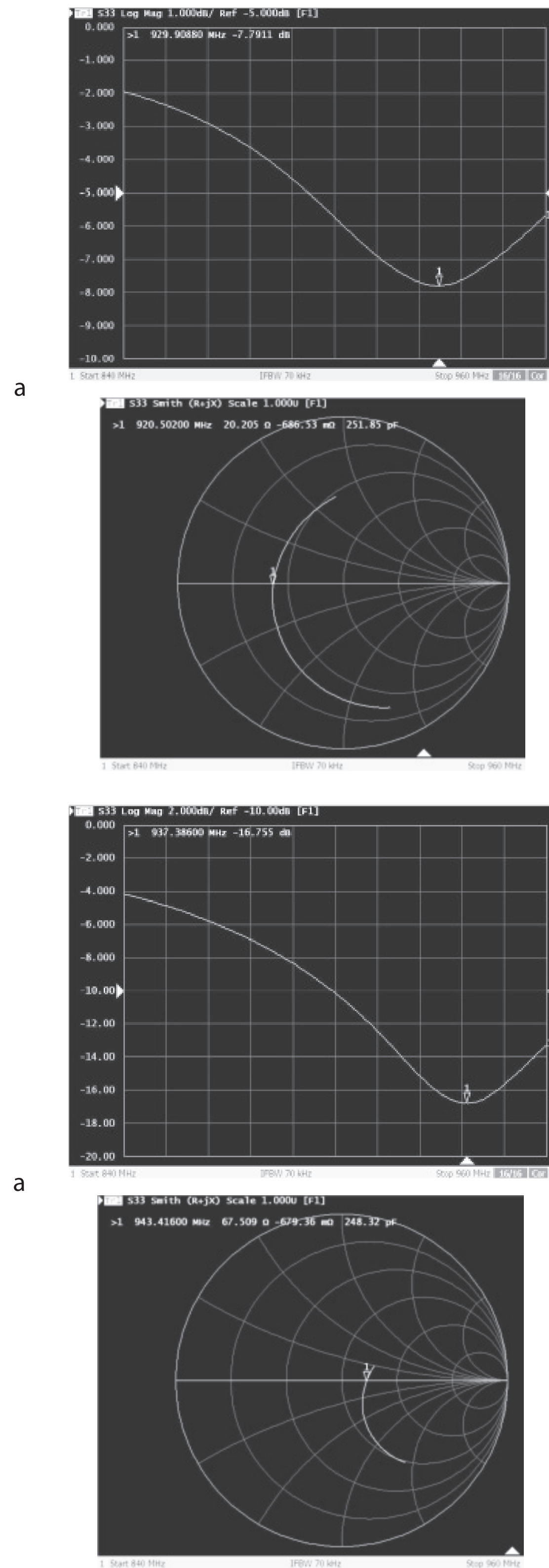


Figure 10: Measured return loss (left) and a Smith chart (right) for: (a) screen printed antenna (antenna, S4*), and (b) a flexographic printed antenna (antenna, F2*).

3.3 Backscattered power measurements

Non-laminated and laminated cards were evaluated by measuring the backscattered power. The backscattered power was measured using an IDS-R902 reader (Figure 11). It comprises the reader electronics and an A0025 circularly polarized patch antenna (Poynting GmbH, Dortmund, Germany) with gain of 6.5 dBi emitting UHF EM radiation at a frequency of f = 868 MHz. The reader electronics measures the intensity of the modulated backscattered signal. The backscattered power was measured on non-laminated and laminated cards by moving each card separately in a straight line perpendicular to the reader in 2 cm increments. The measurements were taken separately on 10 fabricated cards with screen-printed antennas and 10 fabricated cards with flexographic-printed antennas.

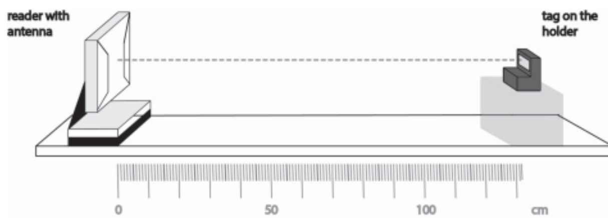


Figure 11: Schematic illustration of measuring the backscattered power

The results presented on Figure 12 show the median values of all the samples measured for the defined distances. The final median values of the reading distances and backscattered power achieved for screen- and flexographic antennas printed on non-laminated cards, with their related standard deviations, are shown in Table 3 below.

Table 3: Median values for reading distances and backscattered power achieved for non-laminated cards

	Screen printing		Flexography	
	Distance [cm]	Power [dBm]	Distance [cm]	Power [dBm]
Average	39,40	-57,67	34,73	-59,87
Standard deviation	±1,14	±1,11	±12,69	±2,03

It can be observed that card readability depends on the conductivity of the printing ink used to print the antenna. Antennas printed with screen-printing thermal ink with a resistance of 1.22 Ω (sheet resistance: 118.12 mΩ/sq), had 30-times higher conductivity than those printed with flexographic UV inks with a resistance of 35.94 Ω (sheet resistance: 3489 mΩ/sq). As a consequence, cards printed with thermal ink had slightly better readability and higher backscattered power (dBm) for the return signal than cards printed

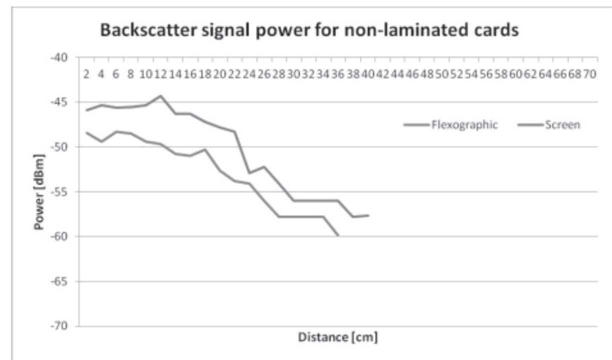


Figure 12: The effect of reading distance on the backscattered power achieved for non-laminated cards made using screen and flexographic-printing.

with UV inks. The maximum reading (working) distance showed differences between the inks applied. UV inks have a shorter reading range. The standard deviation values are very high for flexographic-printed antennas. The reason for such results can be found in the weak uniformity of ink layer thickness and the resultant high variability in sheet resistance.

Backscattered power measurements were also performed for the laminated cards (Figure 13). The median values for the reading distances and backscattered power achieved for screen- and flexographic antennas printed on laminated cards, with their related standard deviations, are presented in Table 4 below.

Table 4: Median values for the reading distances and backscattered power achieved for laminated cards

	Screen printing		Flexography	
	Distance [cm]	Power [dBm]	Distance [cm]	Power [dBm]
Average	62,84	-59,38	58,00	-65,27
Standard deviation	±5,79	±1,41	±3,46	±1,44

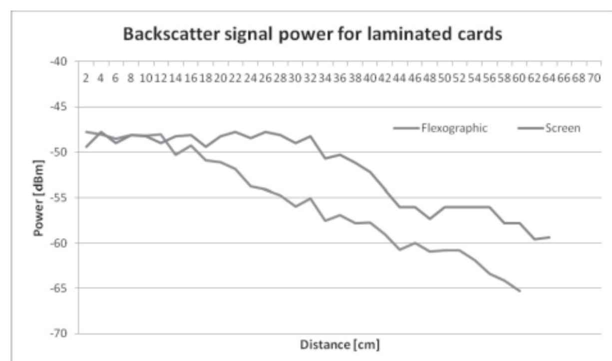


Figure 13: The effect of reading distance on the backscattered power of laminated cards made using screen and flexographic-printing.

The comparison of the maximum reading distances for non-laminated and laminated cards revealed some clear differences. Since the antenna is designed for laminated cards, the lamination process for screen-printing increases the reading distance from 39.4 cm to 62.84 cm.

As is the case with screen-printed antennas, the card lamination process also increases the reading distance also for laminated cards in which the antennas were printed using flexography (this time from 34.73 cm to 58.0 cm). This increase is similar to that for screen-printed antennas, but there are obvious differences in backscattered power, which is higher for laminated cards with screen-printed antennas. The main reason for this again lies in the higher resistance of flexographic - UV conductive ink.

4 Conclusions

In this paper, the possibility of utilising screen and flexographic printing processes in the fabrication of UHF RFID antennas has been investigated in terms of fabrication speed and the repeatability of the printing process. Through optimizing the antenna design and printing processes, it may be possible to streamline printing for low-cost mass production. In order to prove the aforementioned statement, industrial flat-bed screen printing and a roll to roll flexographic printing machine were used in to produce the proposed folded dipole antenna. The characteristics of the antennas were evaluated by measuring the resistance, antenna impedance and return loss. After the drying process and lamination had been completed, the operability of the smart card was ascertained by measuring the backscatter power.

It was demonstrated that the higher ink conductivity achieved using screen printing increases backscattered power. Furthermore, screen printing gives us a more stable response because of greater uniformity in the ink layer thickness and the lower resistivity (a median value of approx. 1.2 Ω), which is in contrast to flexographic printing which has a level of resistance that is approximately 26 times higher (approx. 31.9 Ω). The resistance of the antenna directly affects the reading distance and backscatter power. Screen printed card shows 8% better reading range with a stronger backscatter power. The main effect on the operability of the final tag is the quality of the conductive ink itself, and the repeatability and stability of the printing process. The research has proved that screen- and flexographic printing technology can be used equally well for printing of smart cards UHF antennas, but screen printing results in better card operability. Flexographic printing, on the other hand, has proved to be a faster and more cost-effective solution.

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A Parallel Architecture with Novel Filtering and Data Accessing Order for Deblocking Filter in H.264/Svc Using Reconfigurable Architecture

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Abstract: In this paper we present a parallel filtering architecture with novel filtering and data accessing order for deblocking filter in H.264/SVC. The deblocking filter is the complex part in H.264/SVC which consumes more computation time and it has to adapt for normal filtering (PAFF), MBAFF filtering and inter-layer prediction. The filtering order of MBAFF coded frames has to support all combinations of field/frame mode for current and adjacent MB to filter a macroblock which increases the complexity of deblocking filter. The proposed filtering architecture adapts efficiently for the MBAFF coded frames by reducing the complexity, results in faster filtering of a macroblock. Implementing the filter architecture in reconfigurable platform helps in faster adaptability to normal filtering operation and MBAFF filtering. The proposed deblocking filter architecture is implemented in Cyclone V (5CEFA9F31C8N) and the results are analyzed. The proposed architecture achieves 19% increase in processing speed and 21% reduction in area.

Keywords: H.264/SVC; Deblocking Filter; PAFF/MBAFF; Reconfigurable Architecture

Paralelna preoblikovalna struktura za deblokirni filter v H.264/Svc z novim filtriranjem in vrstnim redom dostopa do podatkov

Izvleček: V članku predstavljamo novo paralelno filtrno strukturo v H.264/Svc z novim filtriranjem in vrstnim redom dostopa do podatkov. Deblokirni filter je kompleksen del H.264/SVC, ki potrebuje več računskega časa in se mora prilagoditi navadnemu filtru (PAFF), MBAFF filtru in medslojnimi napovedmi. Vrstni red filtriranja MBAFF kodnih okvirjev mora podpirati vse kombinacije trenutnih in sosednih MB načinov polje/okvir za filtriranje makro bloka, kar zaplete deblokirni filter. Predlagana filtrna struktura se prilagodi MBAFF kodiranim okvirjem z zmanjšanjem obsežnosti, kar omogoča hitro filtriranje makro blokov. Predlagana struktura je implementirana v Cyclone V (5CEFA9F31C8N) in dosega 19 % višjo hitrost procesiranja in 21 % zmanjšanje površine.

Ključne besede: H.264/SVC; deblokirni filter; PAFF/MBAFF; preoblikovalna struktura

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1 Introduction

H264/SVC is the recent international standard used for video coding [1]. It is a scalable video coding (SVC) extension of H.264/AVC standardized by the joint team of ITU-T VCEG and ISO/IEC MPEG. Due to these latest advancements in video coding standards it has been applied to various multimedia applications such as video telephony, video conferencing over mobile TV, Blu-ray Disc and HD DVD optical storage media [2-4], [15]. Nowadays RTP/IP is mostly used in modern video transmission and storage systems and it is characterized by variety of connection qualities and receiving devices [1]. The RTP/IP [16] access network is the standardized packet format for delivering audio and video over IP networks. The receiving devices are varied from cell phones to high-end PC's where variation is terms of both resolution and processing power of devices. H.264/SVC addresses these issues by providing scalable video sequence.

In H264/SVC [14], [10], [20] the scalability is in terms of spatial (resolution), temporal (frames) and quality (PSNR) by removing part of the video bit stream depending upon the need of the users. The scalability in

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H.264/SVC is achieved by layered structures as base layer with several additional enhancement layers. The video performance is increased from base layer; with base layer is having lowest video content information. The deblocking filter employed in H264/SVC is of high complexity and consumes over 30% of total execution in H264/SVC. In H264/AVC [5], [6], [17] the in-loop deblocking filter is employed after motion compensation to remove the blocking artifacts. The block artifacts are resulted from both quantization of transform coefficient and block based nature of motion compensation. The H264/SVC employ the in-loop deblocking filter after the motion compensation for frames coded either in PAFF or MBAFF type and in the inter prediction layer of spatial resolution to remove blocking artifacts. In each case an adaptive deblocking filter [6], [11], [12] is applied on each 4x4 block edge considering the boundary strength (Bs) values of the pixel across the boundary based upon the block type whether it is intra or inter coded. The deblocking filter is implemented using various architectures [7-9], [18], [22]. In [9], a new filtering order which modifies the basic filtering order by adopting the data reusability between successive filtering. The filtering architecture in [8], achieves higher data reusability by combining both horizontal and vertical filtering of a 4x4 macroblock. Hybrid scheduling method in [7] uses less number of processing cycles to filter a macroblock. The same Hybrid scheduling method which uses both in/post-loop filters is effectively adopted for multiple standards H.264/MPEG 4 with reduced gate counts compared to other filtering architecture which supports multiple standards. In [21], scalable deblocking filter architecture provides parallelism at macroblock level in wave front order for filtering the frame. It is implemented in Virtex 5 and the level of parallelism is limited by the resource availability. In this paper, a novel filtering and data accessing order with parallel processing using reconfigurable architecture is adopted for the deblocking filter to support normal and MBAFF coded frames. By adopting a reconfigurable architecture using Cyclone V for these deblocking filter results in increase of computational speed and efficiency. Section 2 provides concept of deblocking filter. Section 3 gives clear explanation regarding the proposed deblocking filter architecture and its adaptability for PAFF and MBAFF coded frames with filter processing order. Sections 4 discuss the results obtained by implementing it in Cyclone V and compare it with various filtering architecture.

2 Deblocking Filter

In our architecture, an adaptive deblocking filter [2] is employed. The deblocking filter is used to remove the blocking artifacts resulted from both quantization process and motion compensation due to its block based nature. Each macroblock consist of one 16x16 luminance block and two 8x8 chrominance blocks. The deblocking filter is applied to each 4x4 block in the macroblock.

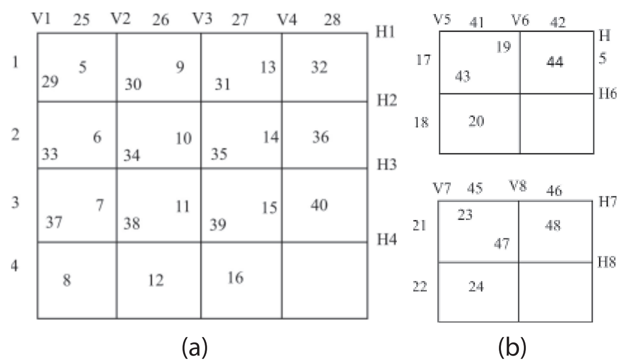


Figure 1: (a) luma block, (b) chroma block

The filtering is applied in the order of vertical edge first then on the horizontal edges as shown in Figure 1. The same filtering order is followed in chrominance block also. The deblocking filter is adaptive based on three levels they are slice level, edge level and sample level.

2. 1 Adaptability of Filter

2.1.1 Slice Level

In the Slice level, the $Offset_A$ and $Offset_B$ is transmitted along the slice header syntax which is used to adjust the values of α and β, which is a quantization dependent parameters. By varying the values of a and b from positive to negative, the filtering is varied from strong to weak compared to zero offset values. A zero offset value will give no change in filtering. A negative offset value will helps to maintain the edge sharpness in high resolution video.

Table 1: Bs value for each coded MB

Block nodes and conditions	Bs
One of the block is intra and its macro block edge	4
One of block is intra	3
One of the block has coded residuals	2
Different motion vector, Different Reference frame, Different no of reference frame	1
Otherwise	0

2.1.2 Edge level

The filtering applied for each 4x4 block depends upon boundary strength (Bs) value. The Bs value is varied from 4 to 0 based upon the block mode and the cod-

ing type of the two adjacent blocks with order of decreasing filter strength. The Bs value of 1 to 3 mentions standard filtering, value of 4 means strong filtering and value of 0 means no filtering. The varying filtering level reflects on the number of samples that has to be modified. In case of MBAFF, consideration has to be taken in applying a strong vertical filtering at the field level. The following Table 1 shows the boundary strength value for each coded block and filters that have been used.

2.1.3 Sample level

By using sample level adaptability in the deblocking filter, the original edges in the picture is preserved. The sample level adaptability is achieved by analyzing the values across the boundaries. Let P_0, P_1, P_2, P_3 and q_0, q_1, q_2, q_3 be the samples across boundaries of adjacent coded blocks. p_0 and q_0 be the sample at the boundaries. Figure2. shows the condition where filtering is applied. For Boundary strength (Bs) value other than zero, the following consideration has been taken in to account before applying filtering. The filtering for the line-of-pixels (LOP) will only takes place after satisfying the below equations (1), (2), (3)

$$|p_o - q_o| \langle \alpha(Index_A) \tag{1}$$

$$|p_1 - p_o| \langle \beta(Index_B) \tag{2}$$

$$|q_1 - q_o| \langle \beta(Index_B) \tag{3}$$

The thresholds α and β are dependent on both Quantization Parameter (QP) and encoder selected offset values. The table index values $Index_A$, $Index_B$ are given by the following equations,

$$Index_A = Min(Max(0, QP + Offset_A), 51) \tag{4}$$

$$Index_B = Min(Max(0, QP + Offset_B), 51) \tag{5}$$

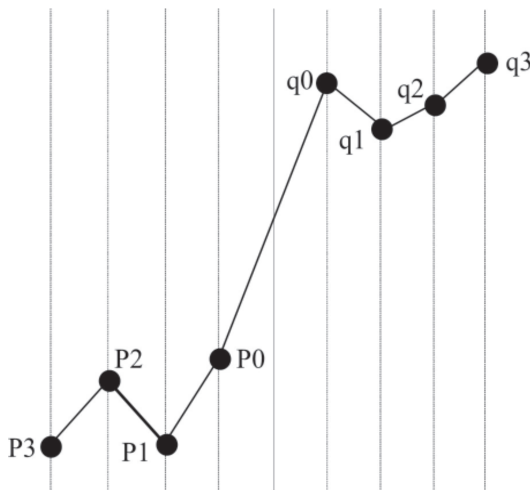


Figure 2: Condition where filtering is turned on

For luminance samples, the following additional spatial activities are checked to determine the extent of filtering,

$$|p_2 - p_o| \langle \beta(Index_{6B}) \tag{6}$$

$$|q_2 - q_o| \langle \beta(Index_B) \tag{7}$$

2.2 Filter operations

2.2.1 Filtering operations for Boundary strength value for Bs = 1 to 3

For boundary strength from 1 to 3, the value of p_0 and q_0 are modified as below

$$p_o^{'} = p_o + \Delta_o \ and \tag{8}$$

$$q_o^{'} = q_o - \Delta_o \tag{9}$$

The Δ_o value is calculated in two step process, first Δ_{oi} is calculated and the clipping is applied to this Δ_{oi} value

$$\Delta_{0i} = (4(q_0 - p_0) + (p_1 - q_1) + 4)\rangle\rangle 3 \tag{10}$$

The values of p_1 and p_2 are modified, if the corresponding equations (6) and (7) are satisfied. The values are modified by the below equations

$$p_1^{'} = p_1 + \Delta_{p1} \tag{11}$$

$$q_1^{'} = q_1 + \Delta_{q1} \tag{12}$$

The Δ_{p1}, Δ_{q1} is calculated in two step process, first Δ_{p1i} is calculated and the clipping is applied to these Δ_{p1i} value

$$\Delta_{\perp} p1i = (p_{\perp}2 + ((p_{\perp}0 + q_{\perp}0 + 1)\rangle\rangle 1) - 2p_{\perp}1)\rangle\rangle 1) \tag{13}$$

The clipping process that has been applied to the Δ_{oi}, Δ_{p1i}, Δ_{q1i} are discussed below.

2.2.1.1 Clipping process

Clipping process is used to reduce the blurring resulted from too much low pass filtering. In clipping, a significant part of the intermediate values Δ_{oi}, Δ_{p1i}, Δ_{q1i} is limited in the range –c1 to c1. The c1 value is get from the 2-dimensional table that is indexed by $Index_A$ and Bs. For an increase in $Index_A$ and Bs value, the c1 value will keep increases providing a strong filtering

$$\Delta_{p1} = Min(Max(-c_1, \Delta_{p1_1}), c_1) \tag{14}$$

$$\Delta_{q1} = Min(Max(-c_1, \Delta_{q1_1}), c_1) \tag{15}$$

For clipping the delta value, the c0 is set to c1 first and for each true conditions of (6), (7) the c1 is incremented by 1.

$$\Delta_0 = Min(Max(-c_0, \Delta_{0i}), c_0) \tag{16}$$

In case of chrominance samples, the filtering is only applied to p0 and q0 values. For clipping the c0 value is initially set to c1 plus 1.

2.2.2 Filter operations for Boundary strength (Bs = 4)

In case of luminance filtering, for boundary strength equal to 4 a strong 4-tap and 5-tap filter or a weak 3-tap filter is applied based upon the sample value. The strong filter modifies up to three samples including edge sample on each side. The weak filter modifies only the edge sample. For applying the strong filter, the conditions in (17) has to be satisfied

$$\left|p_0 - q_0\right| \langle (\infty \rangle\rangle 2) + 2 \quad (17)$$

If both the conditions (6) and (17) are satisfied, the filtering is applied by the below equations

$$p_0^{'} = (p_2 + 2p_1 + 2p_0 + 2q_0 + q_1 + 4)\rangle\rangle 4 \quad (18)$$

$$p_1^{'} = (p_2 + p_1 + p_0 + q_0 + 2)\rangle\rangle 2 \quad (19)$$

$$p_2^{'} = (2p_3 + 3p_2 + p_1 + p_0 + q_0 + 4)\rangle\rangle 3 \quad (20)$$

In case of chrominance filtering, if either of the conditions (6) or (17) is satisfied then only p_0 is changed according to the following equations and p_1, p_2 are left unchanged

$$p_0^{'} = (2p_1 + p_0 + q_1 + 2)\rangle\rangle 2 \quad (23)$$

For modifying the q values, conditions (6) is replaced by (7) and the same filtering process is repeated by replacing p sample positions by q sample positions.

2.3. Deblocking filter in H264/SVC

The deblocking filter is used to remove the blocking artifacts produced due to motion compensation and quantization process. In H264/AVC the deblocking filter is applied for the reconstructed frame to remove the blocking artifacts results from motion compensation and quantization process. The H264/SVC consists of several layers from base layer to enhancement layer providing increased scalability in terms of spatial resolution, temporal resolution and quality. For H264/SVC the deblocking filter is applied in the same manner as H264/AVC, additionally the deblocking filter is applied in the interlayer prediction and a special consideration has to be done for MBAFF coded frames since it is widely supported in H.264/SVC. The deblocking filter operation is same for normal case and interlayer prediction, for the later, some additional condition has to be included in applying the deblocking filter. In the inter-layer prediction process of H264/SVC the enhancement layer data is predicted from previously reconstructed data of base layer. In case of inter-layer prediction, the deblocking filter is applied only for the I_BL type macroblock to the corresponding 4x4 co-located blocks. In I_BL type macroblock, all luma blocks of enhancement macroblock corresponds to lower resolution layer blocks of intra-picture coded. Since the deblocking filter consumes 30% of total computation time, an effective filtering in terms of faster computation is necessary to improve the efficiency of H264/SVC.

The interlaced type frames consist of top and fields which are captured at different time instants, the top field consist of odd number of rows and bottom field consist of even number of rows from the frame's initial position [19]. The frames are coded either using PAFF or MBAFF coding in H.264/SVC encoder. In PAFF, the two fields can either combined as single coded frame (frame mode) or coded as two separate fields (field mode) for a single frame. While in MBAFF coding, each vertical macroblock pair is coded either in field or frame mode. In frame mode, the macroblock pair contains the frame lines. In case of field mode, for each macroblock pair the top macro block contains top field lines and the bottom macroblock contains bottom field lines, doubling the spatial extent of the field coded macroblock. In H264/SVC, the MBAFF coding for interlaced frames is widely used. In deblocking filter operation, the filtering on the MB edges includes pixel from neighboring MB, creating dependency due to the coding type of neighboring macroblock. Since for normal PAFF coded frames an entire frame is either coded in field or frame, the above mentioned dependency is avoided for filtering operation. In MBAFF coding, the adaptability of field or frame mode is for each vertical macroblock pair, so a higher dependency is created on filtering the MB edge increasing the complexity of deblocking filter. Efficient deblocking filter architecture is needed to reduce the complexity and faster filtering for MBAFF coded frames.

3. Proposed Method

In this paper, a normal filtering architecture is designed for PAFF coded frames and parallel filtering architecture for MBAFF (frame/field mode for each macroblock pair) coded frames. The normal filtering architecture uses filtering unit pair which performs both horizontal and vertical filtering simultaneously. Since for filtering a 4x4 macroblock, the macroblock has to be filtered four times this requires repeated memory access. The proposed filtering architecture helps in reducing the number of memory access providing faster filtering operation. The filtering unit is capable of performing the above mentioned filtering operation. For PAFF coding, the choice between frame or field mode is applicable for entire frame. Normal filtering process consisting of single filtering unit pair is assigned

to current MB providing faster filtering. For MBAFF coded frames, a parallel filtering architecture with two filtering unit pair is assigned to the macroblock pair for faster and efficient filtering. The control unit in both Input and Output Buffer Controller Unit perform additional functionalities to store and retrieve the vertical macroblock pair data in proper order. The proposed method adapts for both normal filtering process and MBAFF filtering. In case of normal filtering process, the additional modules that are used in MBAFF coding are disabled by the method of clock gating. In case of inter-layer prediction, the filtering is only applied for I_BL type macroblock which is of intra-coded [13]. The filtering order is same for deblocking filter in inter-layer prediction process, but the Filtering Unit is designed to check whether the macroblock is of intra-coded I_BL type otherwise filtering is disabled for that particular macroblock.

3.1 Normal filtering operation

In case of normal filtering operation, a single filtering unit pair is assigned to a macroblock. The proposed architecture for deblocking filter in normal filtering process is given in Figure 3. The filtering pair consists of horizontal and vertical filters. The filtering operation is done subsequently for all edges in the row and column using corresponding horizontal and vertical filters. The vertical filtering for the horizontal edges takes place simultaneously except for first filtering operation which starts after two MB cycle. The filtering architecture consists of Input Buffer Controller, Filtering Module and Output Buffer Controller. The Filtering Module contains a Filtering Unit accompanied with Input Control, Output Control and a Transpose Unit. This organized filtering architecture helps in effective and faster filtering of each MB. Each Unit in the filtering architecture is given in detail below.

3.1.1 Input Buffer Controller

The input buffer controller unit consists of a control unit, two separate buffer unit each of it store a 4 x 4 data block of size (4x32) bit. In the two buffer unit, one is used to get data from reference memory (previous reconstructed MB) and other buffer unit is used to hold current MB data that has to be filtered. The reference memory and current MB data is loaded to both horizontal and vertical filtering unit. The buffer unit consists of a register array to store the macroblock for simpler data accessing. The control unit provides proper data accessing method from the buffer unit to each filtering unit. For horizontal filtering the data is accessed in the row order from the buffer unit, while for vertical filtering the data is accessed in the column order from the buffer unit. For MBAFF coded frames, proper macroblock from each vertical macroblock pair has to be accessed for parallel filtering process.

3.1.2 Filtering module

Filtering Module consist of Filtering Unit accompanied with sub units of Input Control, Output Control and a Transpose Unit. The sub units help in effective data movement to and from the Filtering Unit providing faster filter operation.

3.1.2.1 Filtering Unit

The Filtering unit is capable of performing the above mentioned adaptive filtering operation based upon the slice level, edge level and sample level. Since QP and offset values are same for 4x4 blocks. Each Filtering Unit computes the boundary strength and threshold values only once for the 4x4macroblock. The Filtering Unit is configured to perform both horizontal and vertical filtering.

3.1.2.2 Input Control

The Input Control helps in choosing the data given to the Filtering Unit. The Input Control consists of two buffers (FIFO). In those two buffers, one of it is used to store the data for current MB is of size (4x32) bit and the other is used to store the reference macroblock from Reference memory or Output Control Unit is of size (4x32) bit. This buffer helps in simultaneous data loading and filtering. In horizontal filtering, it chooses the data from reference memory (previous reconstructed data), Current MB data and transpose of previous filtered data. For vertical filtering, the Input Control additionally receives semi-filtered pixel from output buffer (FIFO buffer) which is stored temporarily in it.

3.1.2.3 Output Control with Transpose Unit

The Output Control with Transpose Unit consists of two temporary buffers (FIFO) and an additional buffer (FIFO) of size (4x32) bits each. It is employed in both Filtering Module to get filtered output ‘p’ and ‘c’ from the Filtering Unit and forwards it to the corresponding next stage. In horizontal filtering, the output control forwards it’s either to the vertical filtering unit for filtered pixel ‘r’ or Input Control of same filtering unit for filtered pixel ‘c’ except for the last edge in the row in which both ‘r’, ‘c’ is forwarded to vertical filtering unit. For vertical filtering the output data is either forwarded to same Vertical Filtering Unit for filtered pixel ‘c’ or to the Output Buffer Unit (for future vertical filtering) for filtered pixel. The additional buffer stores the filtered pixel ‘p’ in case of last edge in the row. The Transpose Unit used in our filtering architecture is different from normal Transpose Unit used in [8]. Since the horizontally filtered pixel data is given to the Vertical Filtering Unit, the pixel data is transposed to convert the pixel

accessing order from row wise to column wise. After final vertical filtering of macroblock, the transpose unit converts the macroblock in to normal mode (i.e. for column wise to row wise), which is stored in Immediate Reference Memory for the next MB filtering, Reference Memory for subsequent next row filtering.

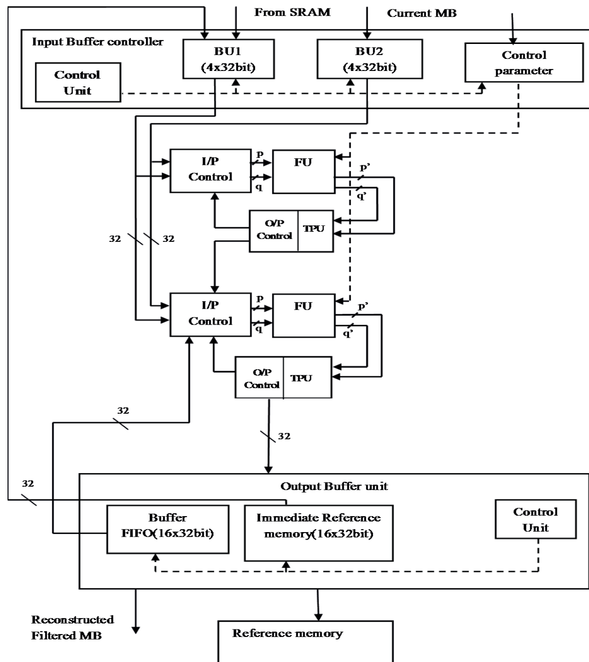


Figure 3: Normal filtering architecture

In the normal transpose module, the transposing operation for the pixel data is performed at the output, while in our filtering architecture the transposing operation is done at the input itself by the control unit. In case of normal transpose architecture, the transpose operation is applied after getting the 4x4 block of data, results in complexity in storing the future filtered output. Since in our proposed architecture, the transposing operation applied at input level helps in reducing the complexity in storing the future filtered pixel and accessing the transposed output. Figure 4. shows the data storing order in the buffer for subsequent horizontal and vertical filtering.

3.1.3 Output Buffer Controller Unit

The Output Buffer Controller Unit consists of several storage units such as Temporary Buffer (FIFO), Immediate Reference Memory and a Control Circuit to support the filtering operation. The Output Buffer Controller Unit receives the filtered data from the vertical filtering unit and by using control circuit the filtered pixel output is moved to the appropriate storage unit. The temporary buffer holds the semi-filtered data which has been later used for subsequent vertical filtering of the current MB. The Immediate Reference Memory (size

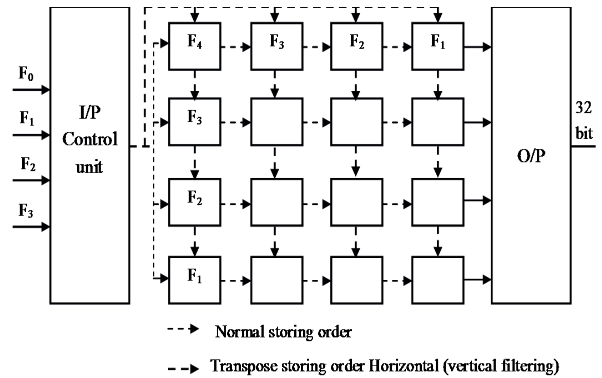


Figure 4: Normal filtering architecture

16x32bit) holds the last column of the final filtered MB as reference pixel data for filtering first vertical edge of the next MB. The control circuit bypasses the filtered pixel data to Reference memory for subsequent row filtering in the current Frame.

3.1.4 Memories

The Immediate Reference Memory holds the last column of filtered MB which consists of four 4x4 macroblock for subsequent macroblock filtering in the frame. The Buffer FIFO is also used to hold the four 4x4 semi-filtered macroblock for future filtering operations of same macroblock. The memory consumed by Immediate Reference memory and Buffer FIFO is of 1K, in which each occupies 512 bits. Since most FPGA has multiple SRAM slots and the dual port SRAM is used as Immediate Reference Memory and Buffer FIFO in our architecture.

3.1.5 Filter processing order

In normal filtering process, a filtering unit pair is used for simultaneous horizontal and vertical filtering. Initially vertical filtering starts after two horizontal filtering cycles based on the filtering order. Figure 5 shows the filtering order for the given macroblock. For filtering a 4x4 macroblock, 31 clock cycles is required. To filter a 16x16 luma MB, 121 clock cycles is needed and for two 4x4 chroma macroblock, 80 clock cycles is needed.

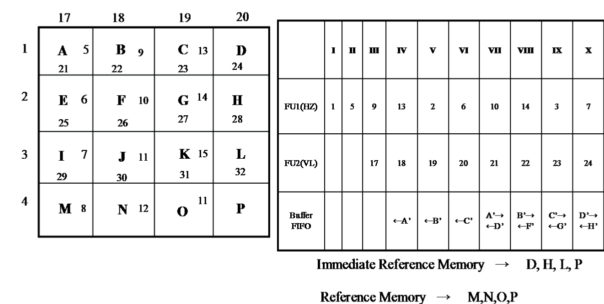


Figure 5: Filter processing order

So totally 201 clock cycles is required to filter a macroblock. To filter a HD frame of resolution 1920x1080, the number of clock cycles required to filter all the luma block is (8100 x 121) clock cycles and for all the chroma blocks is (8100 x 80) clock cycles. The edge filtered in each Filtering Unit and the semi-filtered data that are moved in and out from Buffer FIFO as given in Figure 5. After filtering a current MB, the filtered macroblock stored in Immediate Reference Memory are D, H, L, P and in Reference Memory are M, N, O, P.

3.2 MBAFF filtering operation

For MBAFF coded frames, the current and adjacent MB (reference MB) is coded either in frame or field mode. Thus, for filtering current MB edges combinations of frame/field, field/field, frame/frame and field/frame modes have to be considered. The proposed system provides a novel parallel filtering and data accessing order to reduce this complexity for efficient and faster filtering. In our proposed method, the filtering always takes place for both bottom and top field lines of the frame which requires novel macroblock accessing order from the current MB pair for both field/frame modes.

Meanwhile the macroblock of adjacent MB are always stored as field mode in reference memories for future reference, thus complexity in filtering due to the above mentioned dependency is greatly reduced. Based on the current MB mode, the adjacent macroblock are accessed in proper 4x4 blocks for filtering (i.e. directly for field mode or frame mode). In filtering vertical macroblock pair, each edge is represented by an 8x8 blocks, filtering have to takes place for these blocks. In the 8 x 8 blocks, the filtering for each 4 x 4 block is independent of each other, so an effective parallel filtering architecture provides a faster filtering of these 8x8 blocks. Two filtering unit pair is used for these parallel filtering of each edge. Figure.6 shows the filtering architecture for MBAFF coded frames. Each pair of filtering unit is assigned to the macroblock in the pair. Each filtering unit simultaneously filters the 4x4 block of the corresponding macroblock pair in horizontally and vertically. Initially in each Filtering Unit pair vertical filtering takes place after two horizontal filtering. Since the filtering unit consists of combinational circuit and in MBAFF coding the filtering for each edge takes place for 8x8 blocks, a large memory is needed to store the semi-filtered data and the reference data. These two filtering unit pairs help in achieving faster filtering of the macroblock pair. The Input Buffer Controller Unit consists of two Buffer Unit for storing the reference macroblock and current vertical macroblock pair. The Buffer Unit used to store the reference macroblock data is of size 2(4 x32) bit.

The Buffer Unit used to store the vertical macroblock pair is of size 2(4x32) bit. The control unit in the Input Buffer Controller accesses the proper 4x4 macroblock from current MB and adjacent MB Buffer Unit to the two filtering unit pair according to the proposed filtering architecture. The Output Buffer Controller Unit consists of two Temporary Buffer (FIFO) of size (16x32) bit, such that each Temporary Buffer (FIFO) is used to store the corresponding semi-filtered data of the macroblock in the pair for later use. Comparing to the normal filtering

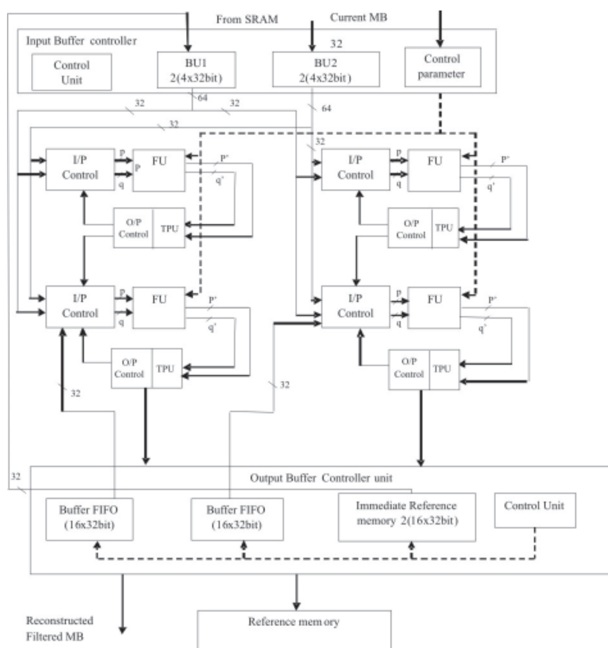


Figure 6: MBAFF filtering order

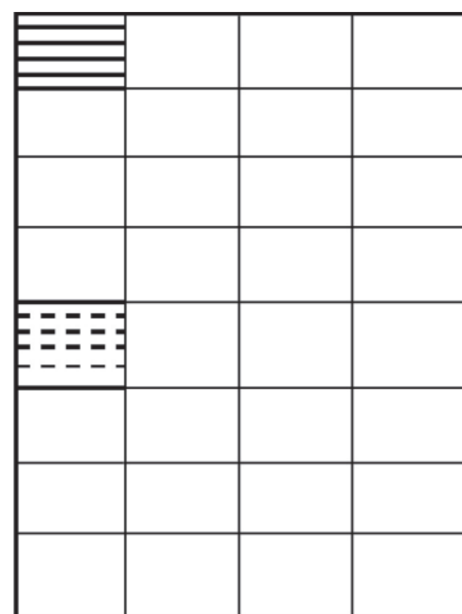
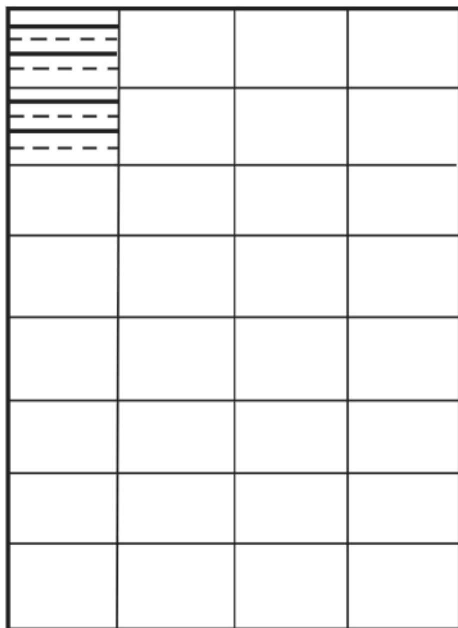


Figure 7: 4x4 macroblock accessing in Field mode



Frame Mode

Figure 8: 4x4 macroblock accessing in Frame mode

process, the immediate reference memory size is also doubled to store the last column of the previous filtered macroblock pair. The Reference Memory size also consumes two times the memory used in normal filtering process. The filtered data is stored in unique manner in the reference memory to support the filtering architecture by means of faster accessing. Compared to normal filtering process, the filter architecture for MBAFF coding consumes twice its area but the speed has been improved.

3.2.1 Filtering method for macroblock

In our proposed method, each current 8 x 8 macroblock constitutes the field lines of both macroblock in the pair and the filtering will take place for both 4 x 4 top fields and 4 x 4 bottom fields.

Since each current MB may be either of field or frame mode, a proper accessing of field lines in the macroblock pair is required. In case of both first vertical and horizontal edge filtering, the current 8 x 8 macroblock is filtered with the previous filtered macroblock which is of field or frame mode. Thus proper filtering order and a reference data accessing order is required for efficient filtering. In case of current macroblock of field mode, parallel filtering is applied for the macroblock 1, 2 in the vertical macroblock pair as given in the Figure 7. The same filtering order is adopted for the whole vertical macroblock pair. For current macroblock of frame mode, the successive macroblock 1, 2 in the vertical MB pair is accessed for parallel filtering as given in Figure 8.

This filtering order is applied for whole MB pair in frame mode.

3.2.2 Data Storing in Reference memories

The proposed filtering architecture overrides the dependency between the current MB and reference macroblock due to different coding modes adopted in both macroblock (i.e. field or frame mode).To support this filtering architecture, the final filtered MB is stored in a field format in the Immediate Reference Memory and in the Reference Memory. The control unit in the Output Buffer Unit stores the previous filtered MB always in field mode, such that the reference macroblock can be accessed according to the current macroblock mode (i.e. either directly for field mode or frame mode). This helps in reducing the complexity in data accessing of reference macroblock due to the mode dependency. The order in which the filtered MB stored in reference Memories for frame and field mode is given in Figure 9.

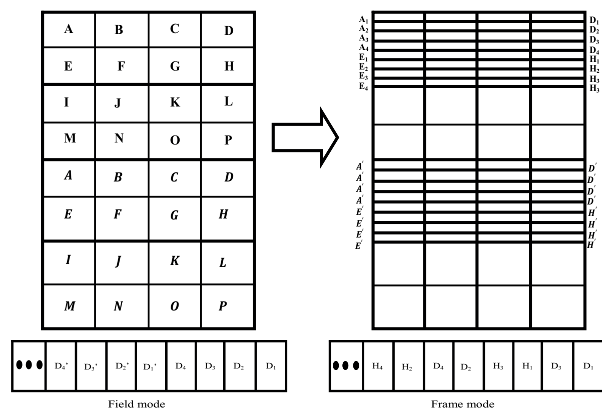
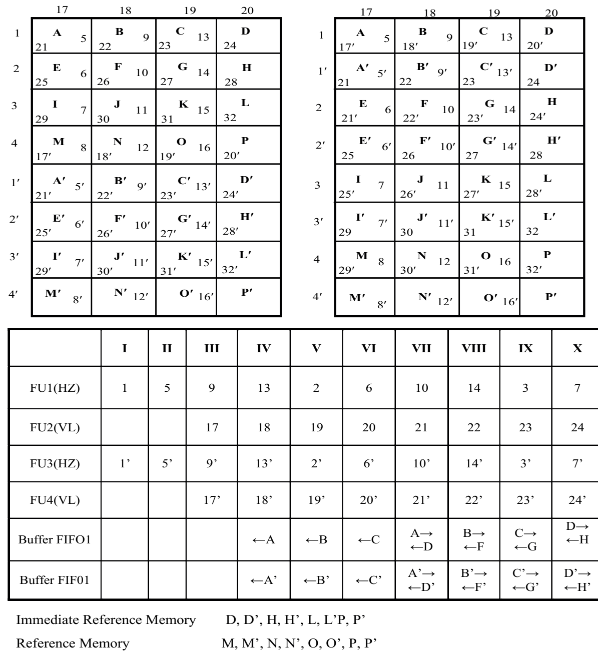


Figure 9: Data Storing order in the Immediate Reference Memory and Reference Memory

3.2.3 Filter processing order

Two filtering unit pair with individual Buffer FIFO is used for parallel filtering of macroblock pair. Each Filtering Unit pair works as the normal filtering operation processing the corresponding macroblock in the pair. Since in MBAFF filtering of macroblock pair works as two normal filtering processes, the number of clock cycles required to filter the vertical macroblock pair is same as the normal filtering process. Since for filtering a 4x4 macroblock 31 clock cycles is required. In filtering the vertical macroblock pair, for 16x16 luma MB 121 clock cycles is needed and for two 4x4 chroma macroblock 80 clock cycles is needed. Additionally some 20 cycles are required for MBAFF filtering. The total number of clock cycles required to filter a vertical macroblock pair is 221 clock cycles. To filter a HD frame of interlaced type, the number of clock cycles required to filter all the macroblock is (8100 x 221) clock cycles.



	I	II	III	IV	V	VI	VII	VIII	IX	X
FU1(HZ)	1	5	9	13	2	6	10	14	3	7
FU2(VL)			17	18	19	20	21	22	23	24
FU3(HZ)	1'	5'	9'	13'	2'	6'	10'	14'	3'	7'
FU4(VL)			17'	18'	19'	20'	21'	22'	23'	24'
Buffer FIFO1				←A	←B	←C	A→ ←D	B→ ←F	C→ ←G	D→ ←H
Buffer FIF01				←A'	←B'	←C'	A'→ ←D'	B'→ ←F'	C'→ ←G'	D'→ ←H'

Figure 10: Filtering Order for MBAFF frames

The Figure 10 shows the filtering order of the macroblock pair in each Filtering Unit (FU) and the semi-filtered data which is moved in and out from Buffer FIFO. The filtered macroblock stored in Immediate Reference Memory is given by D,D',H,H',L,L',P,P' and in Reference Memory is given by M,M',N,N',O,O',P,P'.

4 Results

The proposed deblocking filter for H264/SVC is implemented in Cyclone V (5CEFA9F31C8N) and the results are analyzed.

Table 2: Comparison of proposed filtering architecture with other filtering architecture

	Gate count	Processing Cycles per MB	Frequency (MHz)	Memory
[7]	19.64k	250	100	864+8N
[8]	24k	446	100	1000
[9]	20.66k	614	100	640
Proposed Normal	18.1k	202	200	3768
MBAFF	29k	242	200	7536

Compared to other filtering architecture, our proposed architecture achieves 19 % increase in processing speed. Since temporary buffer is used to store the semi-filtered pixel information, it helps in saving a significant number of clock cycles in accessing the semi-filtered pixel for further filtering process. In addition, the vertical macroblock pair is filtered in parallel and the adjacent MB is stored in field mode in the reference memories to avoid the dependency between the current and adjacent MB, which in turn reduces the complexity of deblocking filter. In transpose module, for the filtered output the proposed method applies transposing operation at the input level, helps in reducing the complexity in storing the future filtered pixel and accessing the transposed output. As a result, the proposed system achieves 30 % complexity reduction in the deblocking filter. Table 2 shows the comparison of deblocking filter with various architectures. Some additional clock cycles has been spent on proper accessing of proper macroblock in the pair which has been compensated by the reduction in complexity. Since the H264/SVC supports various level of layers with scalable resolution in terms of spatial, temporal and quality. This deblocking filter can be effectively implemented in various layers of different resolution by adopting the in-built SRAM slot for memories. The number of memory references for filtering a macroblock is also reduced. The proposed deblocking filter will filter the whole MB in 201 clock cycles for both luma and chroma blocks. In case of MBAFF filtering, the processing will takes place in 221 clock cycles. The proposed filter architecture occupies 8 % less area compared to other filtering architecture.

5 Conclusion

The deblocking filter operation for H264/SVC has more complexity compared to other operation. The filter has to be adaptable for PAFF/MBAFF coded frames and inter-layer prediction. A novel filtering order with parallel processing and efficient data accessing method is applied to the deblocking filter in H264/SVC for faster filtering. The proposed architecture has reduced memory references compared to other filtering architecture. The architecture is implemented in Cyclone V (5CEFA9F31C8N) and performance improvement in terms of processing speed (i.e. number of clock cycles for filtering) of 19 % and area reduction by 8 % is achieved.

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Variable Gain Amplifier for mobile WiMAX receiver

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Abstract: In this paper a Variable Gain Amplifier (VGA) applied to mobile WiMAX standard is presented. The VGA plays an indispensable role in radio frequency receiver. It keeps the signal power falling to the ADC constant while the input one varies substantially. The proposed VGA cell is composed of two transimpedance amplifiers and a transconductance amplifier. Flexibility was ensured to VGA control using a novel method based on active resistor implemented with current conveyer structure. The VGA circuit is optimized for high gain, low noise and low power consumption. In order to attempt mobile WiMAX standard specifications, three VGA cells are cascaded. The studied circuit is designed in CMOS 0.35 µm AMS process technology. It can provide a maximum gain of 74 dB and a minimum gain of 20 dB. The simulated structure provides less than 21 dB of noise figure, a CMRR of 82 dB and a margin phase of 97 °. It achieves an ICP1 of -15.5 dBm. The power consumption is approximately equal to 15 mW under ±0,75 V supply voltage.

Keywords: Variable Gain Amplifier; mobile WiMAX; high gain; low noise

Ojačevalnik s spremenljivim ojačenjem za mobilni WiMAX sprejemnik

Izvleček: Predstavljamo za mobilni WiMAX prilagojen ojačevalnik s spremenljivim ojačenjem (VGA). VGA igra neizogibno vlogo v sprejemniku radijske frekvence. Drži signalno moč na ADC konstanti, pri spremenljivem vhodnem signalu. Predlagana VGA celica je sestavljena iz dveh transimpedančnih in enega transkonduktančnega ojačevalnika. Fleksibilnost kontroliranja VGA je zagotovljena z aktivnim uporom, ki je realiziran s tokovno prenosno strukturo. VGA vezje je optimizirano za visoka ojačenja, nizki šum in nizko porabo energije. Za zagotavljanje standardov mobilnega WiMAX je uporabljena kaskada treh VGA celic. Vezje je izdelano v CMOS 0.35 µm AMS tehnologiji. Največje ojačenje je 74 dB, najmanjše 20 dB. Šum simulirane strukture je pod 21 dB. CMRR je 82 dB in robna faza 97 °. Dosega ICP1 -15.5 dBm. Pri napajalni napetosti ±0.75 V je poraba okoli 15 mW.

Ključne besede: Ojačevalnik s spremenljivim ojačenjem; mobilni WiMAX; visoko ojačenje; nizek šum

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1 Introduction

The IEEE 802.16 task group has been founded in 1999 to develop wireless broadband standards. This family of standards is authored by the Institute of Electrical and Electronics Engineers (IEEE). It belongs to the Wireless Metropolitan Area Networks (WMAN). It has been commercialized under the label WiMAX (Worldwide Interoperability for Microwave Access) by the WiMAX forum industry [1]. The forum is an organization that certifies and promotes the interoperability and compatibility of broadband wireless products based upon IEEE 802.16 standards. Different projects were proposed by the working group. The mainly approved standards areWiMAX for fixed and mobile applications [2]. IEEE 802.16a is addressed to fixed application. The frequency band is between 10-66 GHz for LOS (Line Of Sight) environments and 2-11GHz for NLOS (Non LOS) environments. IEEE 802.16e adds mobility and allows communication from base station to mobile phone and laptop. Mobile WiMAX operates in the frequency band of 2-6 GHz. It promotes a data rate up to 70 Mbit/s and a distance up to 50 km theoretically [3].

This work will be restricted to the mobile WiMAX standard. Mobile WiMAX specifications are given in [2] in the physical layer section. Only OFDMA (Orthogonal Frequency Division Multiple Access) modulation scheme is used. A mobile WiMAX receiver shall be able of detecting and decoding a maximum input signal of -30 dBm and a minimum input signal of -91 dBm. NF (Noise Figure) shall be less than 8 dB in addition to a maximum of 5 dB from implementation losses [2]. In our research we are inter-

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ested in the profile operating in the 3.4-3.6 GHz frequency band. Thus the channel bandwidth is set to 10 MHz and the receiver uses TDD (Time Division Duplexing) for duplexing mode and 1024 for the FFT size [4].

In mobile WiMAX standard, it is required to design the receiver frontend with low cost and low power consumption to ensure integrability and mobility.VGA (Variable Gain Amplifier) constitutes one of the key components of the receiver. It has to maintain the signal power falling to the ADC (Analog to Digital Converter) constant while the input one varies substantially [5-9]. These variations are more important for mobile WiMAX since the receiver moves. A lot of trade-offs have to be considered when designing the VGA. Firstly, VGA has to meet high linearity since it constitutes the last component of the receiver. In the other hand, a high gain range is required in order to adjust low input signal. It is also important that VGA ensures low noise and low power consumption [10]. These constraints and requirements make VGA design task delicate and a real challenge for designers especially when it is applied for mobile WiMAX standard.

This paper is structured as follows. In section 1, VGA specifications for mobile WiMAX standard and VGA topology are detailed. VGA optimization approach is proposed in section 2. Simulation results are reported in section 3. Section 4 presents concluding notes.

2 VGA Circuit

2.1 VGA specifications

The distribution of WiMAX specifications through the different components of the receiver was completed. System level simulations were applied to a homodyne receiver. Each block characteristics, such as gain, ICP1 (Input-1 dB-Compression Point), NF (Noise Figure) and IIP3 (Third Order Intercept Point measured at the Input) are obtained. Table I lists the VGA specifications for the mobile WiMAX receiver. When the input signal is strong with large power, it doesn't require an important amplification.In this case, VGA provides low gain (21 dB). If the input signal is weak with low power, VGA should provide high amplification to reach ADC full scale.

Table 1: VGA specifications

Parameters	specifications	
	weak signal	Strong signal
Gain (dB)	72	21
NF (dB)	20	17
ICP1 (dBm)	8	5
IIP3 (dBm)	18	15

2.2 VGA electrical design and voltage gain formulation

In this work, the adopted VGA circuit is proposed in [10]. It is composed by three cascaded blocks: two transimpedance amplifiers and a transconductance amplifier. The transconductance amplifier is based on differential pair with source degeneration topology. The chosen VGA architecture is shown in figure 1.

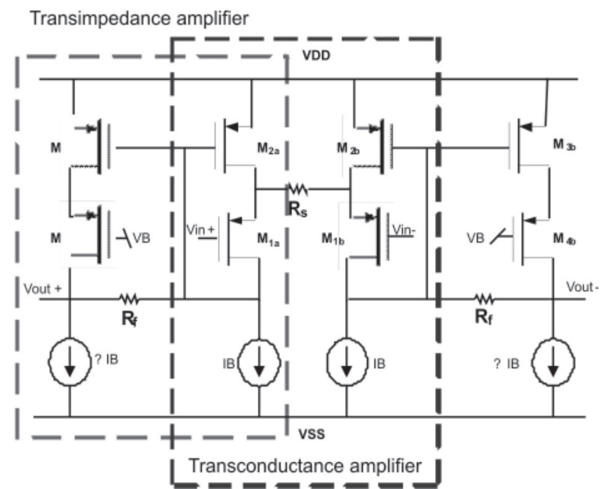

Figure 1: VGA architecture

VGA operation can be explained briefly as follows: a differential input voltage is applied to the transconductance amplifier ($M_{1a,1b}$ PMOS transistor). It is reproduced across the source degeneration resistor R_s, causing the appearance of current signal into $M_{2a,2b}$. Current amplification is then ensured by mean of the two transimpedance amplifiers. Amplified current is converted to an output voltage signal via the feedback resistor R_f. Gain range is ensured through R_s and R_f resistors variation.

Expression (1) describes the voltage gain of the VGA circuit [10] where G_m is the transcondcutance gain and R_m is the transresistance gain which is detailed in (2).

$$A_v = G_m R_m \quad (1)$$

$$R_m = -\frac{(R_f A_i - R_{in})}{(1 + A_i)} \quad (2)$$

Where R_{in} is the input resistance and A_i is the current gain of the current amplifier.

Formula (3) describes the DC differential transconductance gain. It can be approximated to $1/R_s$ if $R_s >> g_{01}/g_{m1}g_{m2}$.

$$G_{md} \approx 1 \Big/ \left(\frac{g_{01}}{g_{m1} g_{m2}} + R_s \right) \quad (3)$$

Expression (4) gives the DC transimpedance gain. If we consider that $R_f >> 1/g_{m3}$, formula (4) can be approximated to expression (5).

$$R_m = \frac{v_{out}}{i_{in}} = \frac{\frac{1}{g_{m3}} - R_f}{1 + 1/\alpha} \quad (4)$$

$$R_m \approx -\frac{R_f}{1 + 1/\alpha} \quad (5)$$

Small signal analysis is performed to the half VGA circuit. The differential voltage gain is described by expression (6) assuming that $g_m >> g_0$, $C_{gs} >> C_{gd}$ and $C_{gs2} + C_{gs3} = C_{gs2}(1+\alpha)$. The DC voltage gain is given by expression (7) where r_{0c} is the output resistance of the current mirror (expression (8)).Considering that $R_f >> 1/g_{m3}$, $R_s > r_{o2}$ and $\alpha >> 1$, the DC voltage gain will be reduced to R_f/R_s. The differential voltage gain formula is a transfer function presenting one zero and three poles (expressions 9-12).

$$A_v \approx A_{V0} \frac{1 - \frac{s}{\omega_z}}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})(1 + \frac{s}{\omega_{p3}})} \quad (6)$$

$$A_{V0} = \frac{-(\frac{1}{g_{m3}} + R_f)(\frac{\alpha}{\alpha+1})}{(R_s // r_{02})(1 + \frac{R_f}{(1+\alpha) r_{0c}})} \approx \frac{R_f}{R_s(\frac{\alpha}{\alpha+1})} \quad (7)$$

$$r_{0c} = g_{m4} r_{04} r_{03} \quad (8)$$

$$\omega_Z \approx + \frac{g_{m1}}{C_{gs1}} (\frac{r_{01}}{r_{02} // R_s}) \quad (9)$$

$$\omega_{p1} \approx -\frac{g_{m1} r_{01} g_{m3} r_{0C}}{C_{gs1}(r_{01} g_{m3} r_{0C} + R_f)} (1 + \frac{1}{\alpha} + \frac{R_f}{\alpha r_{0C}}) \approx -\frac{g_{m1}}{C_{gs1}} (1 + \frac{1}{\alpha}) \quad (10)$$

$$\omega_{p2} \approx -\frac{g_{m3}}{C_{gs2} + C_{gs3}} \frac{r_{0C}}{(r_{0C} + R_f)} (1 + \frac{1}{\alpha} + \frac{R_f}{\alpha r_{0C}}) \approx - \approx -\frac{g_{m3}}{C_{gs3}(1+\alpha)} (1 + \frac{1}{\alpha}) = -\frac{1}{\alpha} \frac{g_{m3}}{C_{gs3}} \quad (11)$$

$$\omega_{p3} \approx -\frac{g_{m3}}{C_L} \frac{r_{0C}}{1 + g_{m2} R_f} (1 + \frac{1}{\alpha} + \frac{R_f}{\alpha r_{0C}}) \approx - \approx -\frac{\alpha}{R_f C_L} (1 + \frac{1}{\alpha}) = -\frac{1+\alpha}{R_f C_L} \quad (12)$$

2.3 Noise study

The input-referred mean-square noise of the VGA is given by this expression,

$$\overline{v_{ni}^2} \approx -\frac{1}{g_{m1}^2} (\overline{i_{n1}^2} + \overline{i_{n2}^2}) + \overline{v_{n,Rs}^2} + \overline{v_{n,Rf}^2} \left| \frac{1}{A_{V0}} \right|^2 + + \overline{i_{n3}^2} \left| \frac{1 + g_{m1} R_s (1 + g_{m2} R_f)}{g_{m1}(-1 + g_{m3} R_f)} \right| \quad (13)$$

Where:

$$\overline{i_{ni}^2} \approx 4kT g_{mi} \Delta f$$

$$\overline{v_{n,Ri}^2} \approx 4kT R_i \Delta f$$

If we consider that $g_{m2} R_f >> 1$ and $g_{m3} = g_{m2}$, (13) can be estimated to (14),

$$\overline{v_{ni}^2} \approx -\frac{1}{g_{m1}^2} (\overline{i_{n1}^2} + \overline{i_{n2}^2}) + \overline{v_{n,Rs}^2} + \overline{v_{n,Rf}^2} \left| \frac{1}{A_{V0}} \right|^2 + + \overline{i_{n3}^2} \left| R_s \right|^2 \quad (14)$$

2.4 Common Mode Rejection Ratio(CMRR)

The common mode rejection ratio CMRR is by definition the ratio of the common-mode gain to differential-mode gain. It describes the ability of an amplifier to reject the common mode signal while amplifying the differential signal [11-12]. It is usually expressed in dB andcan be described as:

$$CMRR = 20 Log \left| \frac{A_{dm}}{A_{cm}} \right| \quad (15)$$

Where A_{dm} is the differential mode gain and A_{cm} is the common mode gain which are defined by the following expressions respectively:

$$A_{dm} = (A_{11} - A_{12} - A_{21} + A_{22})/2 \quad (16)$$

$$A_{cm} = (A_{11} + A_{12} + A_{21} + A_{22})/2 \quad (17)$$

Where A_{ij} are the small signal voltage gains given below:

$$A_{11} = \frac{v_{out}^+}{v_{in}^+} \Big| v_{in=0}^- \quad (18)$$

$$A_{12} = \frac{v_{out}^+}{v_{in}^-} \Big| v_{in=0}^+ \quad (19)$$

$$A_{21} = \frac{v_{out}^-}{v_{in}^+} \Big| v_{in=0}^- \quad (20)$$

$$A_{22} = \frac{v_{out}^-}{v_{in}^-}\bigg|v_{in=0}^+ \quad (21)$$

2.5 Phase Margin

The phase margin given for an operational amplifier is the difference between the operational amplifier phase shift and -180 deg at the unity-gain frequency.

Phase margin of the VGA cell is described by formula (22),

$$\phi_M = 180° - \cot an(\frac{GBW}{f_{P_1}}) - \cot an(\frac{GBW}{f_{P_2}}) + \cot an(\frac{GBW}{f_Z}) \quad (22)$$

Where : f_{pi} is the frequency of the i-th pole, f_z is the zero fequency.

2.6 R_s and R_f implementation

2.6.1 R_s implementation

In this work, the source degeneration resistor$R_s$is implemented using the current conveyer techniques. The studied structure is used in [13,14,15] (figure 2), it is based on high linearity second generation topology, operating at low voltage low power environment. Currents mirrors (M_5, M_6) and (M_7, M_8) ensure current following between X and Z paths. Differentiel part of the curent conveyer structure ensures voltage following betwen Y and X nodes. C_1 and C_2 are used in order to improve frequency response and circuit stability. R_x and R_z impedances depend on bias current, supply voltage and transistors sizes, and can be described by formula (23) and (24).

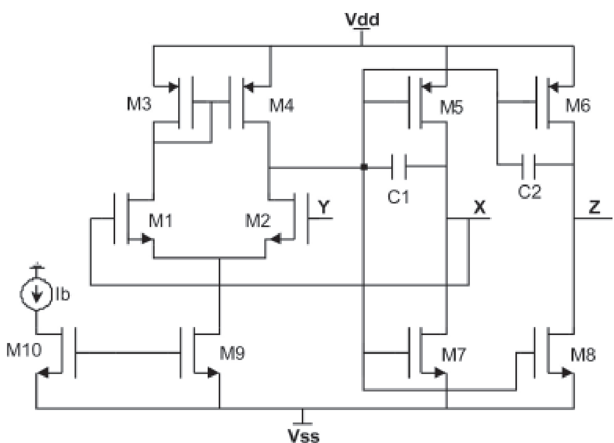

Figure 2: Low-voltage low-power current conveyors

$$R_x = \frac{1}{\frac{r_{05}+r_{07}}{r_{05}r_{07}} + g_{m1}\frac{r_{01}}{2}(g_{m7}+g_{m5})} \approx \approx \frac{2}{g_{m1}\frac{r_{01}}{2}(g_{m7}+g_{m5})} \quad (23)$$

$$R_Z = \frac{1}{g_{ds8}+g_{ds6}} \quad (24)$$

Expression 24 shows that $R_x$resistor variation depend on bias current I_b. Thus the circuit is a current conveyer CCII.R_x is considered a floating positive resistor controlled by the current and it is composed by two current conveyer CCII (figure 3).

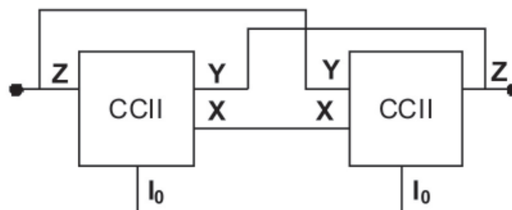

Figure 3: $R_s$architecture

2.6.2 $R_f$implementation

The feedback resistor $R_f$is implemented using two polycilicon resistor R_{f1} and R_{f2} [10]. It is demonstrated in [10] that R_f is used to determine the bandwidth of the VGA circuit. Figure 4 shows the used architecture for R_f implementation.

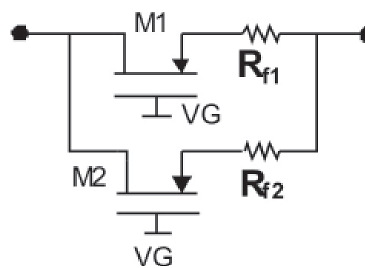

Figure 4: R_fArchitecture

3 VGA Circuit Optimization

In electronics fields, optimization helps designers to achieve best results. Optimization can be performed to transistors sizes, bias current, voltage and passive components.

3.1 Problem formulation

Solving an optimization problem consists to find a solution that minimizes or maximizes a particular criterion. In most cases, the optimum found is not unique. Thus there exist a set of solutions minimizing or maximizing the considered criterion. An optimization problem can be described as follows [16]:

Minimize $f(\vec{x})$: function to optimize

Subject to $\vec{g}(\vec{x}) \leq 0$: constraints to satisfy

Where $\vec{x} \in R^n$, $\vec{g}(\vec{x}) \in R^q$: *n* parameters

In this work, we are looking for optimizing the transistors sizes and the bias current of the VGA circuit. The optimization program is written in C++ language while considering steps listed below.

3.2 Optimization approach

The adopted optimization methodology is based on the following steps:

Constants initialization: μ_n, C_{ox}, V_{tn}, V_{tp}, Vdd, f_0, R_f and R_s.
Parameters to optimize: transistors length: [0.35 µm, 0.45 µm], transistors width [1 µm, 800 µm] and bias current: [4 µA, 300 µA]

Model determination: VGA modelization is described in the previous section. Gain, noise figure, phase margin, linearity conditions and CMRR expressions are listed. These parameters represent the constrains of the algorithm where: Gain>20 dB, NF<25 dB, PM>45° and CMRR>100 dB.

Test vector generation (including bias current and transistos sizes).

Constraints verifications: if these constrains are verified the vector test represents a valid solution which can be used, if not another test vector will be generated.

Table 2: Ttransistors sizing after optimization

Transistors	W/L
M1a,b	4/0.35
M2a,b	30/0.35
M3a,b	10/0.35
M4a,b	90/0.35

The optimized value of the bias current is 5 µA.

3.3 Optimization results

After several iterations, many valid vectors test were obtained. The chosen solution is listed in table 2.

4 Simulation Results

The VGA cell is simulated using the Advanced Design System ADS tool with AMS 0.35 µm CMOS process parameters under ±0.75 V power supply. Current sources are implemented using cascode current mirrors. The bias current is set to 5 µA. The R_f and R_s resistors are implemented using architectures mentioned in section 2. Preliminary simulations of the VGA circuit shows that specifications needed for WiMAX standard are not satisfied especially in term of gain (simulated value of the gain = 25 dB << 72 dB = desired value). This problem can be solved by cascading several VGA cells. To attempt a gain of 72 dB, three VGA cells cascaded are required (figure 5).

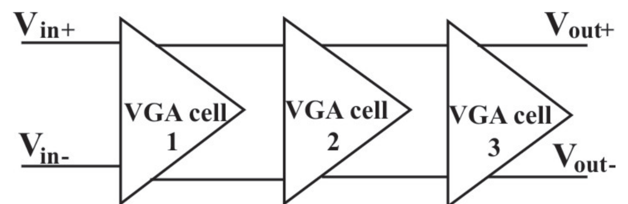

Figure 5: Overall VGA architecture

Simulations results for gain and noise figure are depicted in figures 6, 7, 8 and 9. High gain is obtained by maximizing R_f and minimizing R_s. Figure 6 shows that the maximum gain obtained by cascading three VGA cells is above 80 dB. R_f and R_s control allows to provide the gain necessary for mobile WiMAX application. The corresponding noise figure curve is shown in figure 7. Noise shown in figure 7 is equal to 19.83 dB which

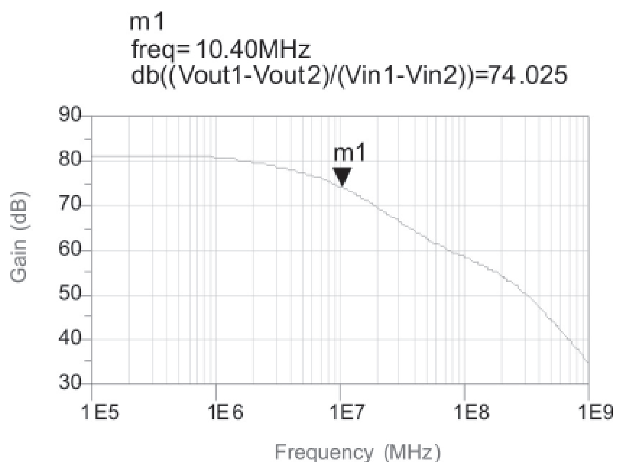

Figure 6: Max gain determination

comply with our application requirements. By adjusting R_f and R_s values, Graph 8 is obtained showing the minimum gain of three VGA cells which is around 25 dB. The corresponding noise is illustrated in figure 9 (21 dB). Bandwidth is maintained at 10 MHz for both max and min gain.

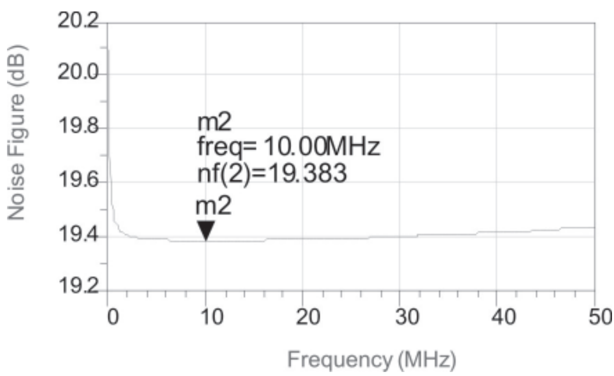

Figure 7: Noise figure determination for max gain

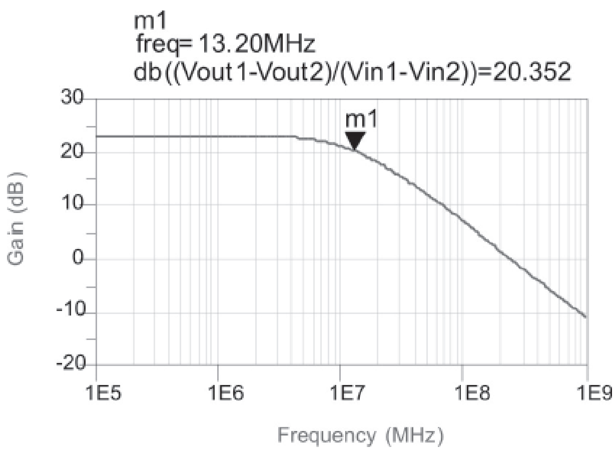

Figure 8: Min gain determination

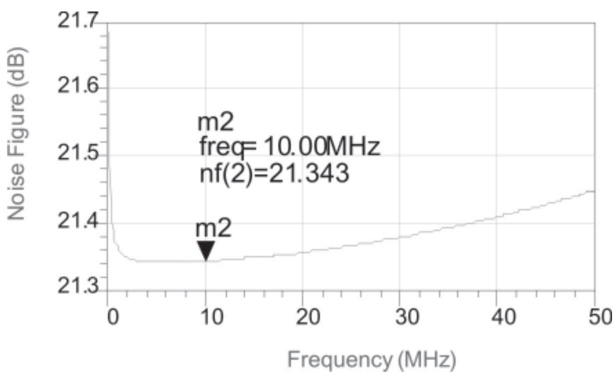

Figure 9: Noise figure determination for min gain

The simulated values of the PM and CMRR are presented in figures10 and 11. Figure 10 shows a CMRR equal to 81 dB at 10M Hz. A PM of 97.32 dB is obtained.

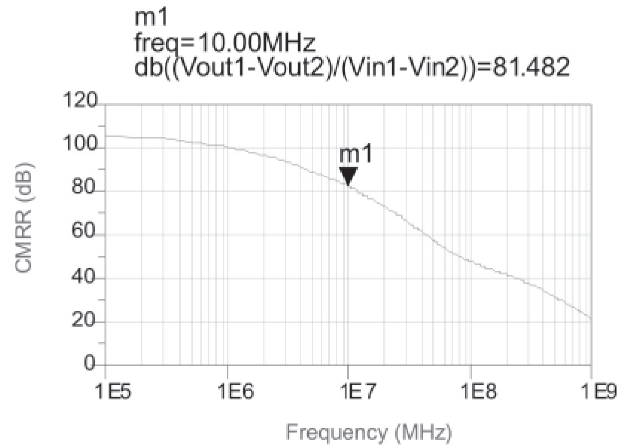

Figure 10: CMRR simulation

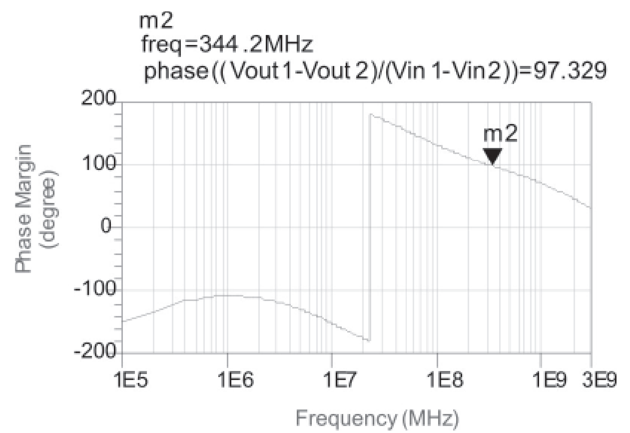

Figure 11: PM simulation

Figure 12 shows the ICP1 simulation curve. The ICP1 is equal to -15.5 dBm, so the IIP3 is around -5.5 dBm.

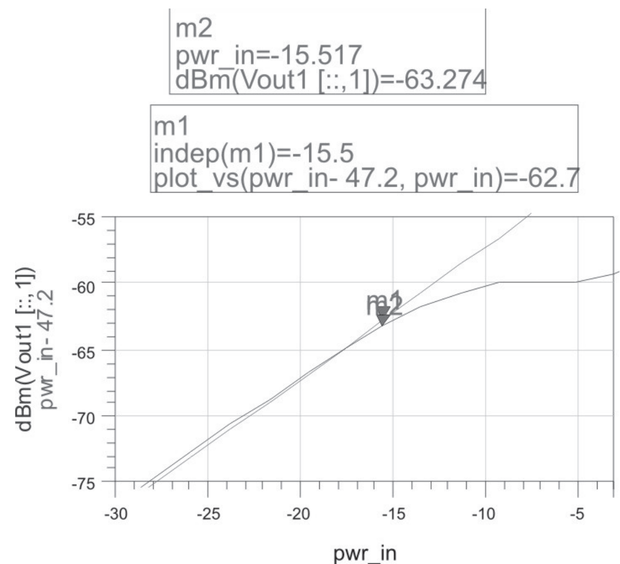

Figure 12: ICP1 simulation

Table 3: summarizes simulation results and a comparison with the standard specifications.

Table 3: Simulation results recapitulation

	Simulation Results	WiMAX Specifications
Supply Voltage	1.5 V	--
Gain range	20.35 dB@74.025 dB	21 dB@72 dB
Bandwidth (gain max)	10.40 MHz	10 MHz
Bandwidth (gain min)	13.20 MHz	10 MHz
NF (gain max)	19.383 dB	<20 dB
NF (gain min)	21.343 dB	<17 dB
IIP3	-5.5 dBm	18 dBm
Phase Margin	97 degré	>45
CMRR	81.49 dB	>100 dB--
Technology	CMOS 0.35 µm	--
Consumed Power	15 mW	--

Max gain is obtained for Rf=120 KΩ and Rs=1 KΩ, min gain is obtained while fixing Rf=30 KΩ and Rs=50 KΩ.

5 Conclusion

A variable gain amplifier designed for mobile WiMAX standard was presented. Device sizes and bias current conditions of the different blocks of the VGA are optimized for high gain, low noise and low power consumption. In order to attempt WiMAX requirements, three VGA cells were used and cascaded.The final circuit is designed in CMOS 0.35 µm AMS process technology. The simulation results showed a gain up to 74 dB,a minimum gain of 20 dB, a noise figure less than 21 dB, an input IIP3 above -3 dBm, a CMRR of 82 dB and a margin phase of 97 °. VGA circuit consumes power of 15 mW from a ±0,75 V supply voltage, however the current conveyer consumes only 1.5 mW. In future work we intend to improve VGA linearity by using a novel architecture.

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The parameter estimation of the electrothermal model of inductors

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Abstract: This paper presents the electrothermal model of inductors dedicated to the analysis of dc-dc converters in SPICE and the proposed method of determining parameters of this model. The parameter estimation algorithm of this model is described in detail. The results of verification of the correctness of the model and the estimation procedure for arbitrarily selected choking - coils are presented. Very good agreement between the calculated and measured characteristics of the considered choking-coils was obtained.

Keywords: Inductors; modelling; parameters estimation; self-heating

Ocena parametrov elektrotermičnega modela tuljav

Izvleček: Članek opisuje elektrotermični model in določevanje parametrov tuljav, ki se uporabljajo v dc-dc konverterjih v SPICE. Natančno je opisan algoritem določevanja parametrov modela. Predstavljeni so rezultati verifikacije modela in postopek ocenitve parametrov na izbranih tuljavah. Rezultati simulacij se dobro ujemajo z meritvami.

Ključne besede: Tuljava; modeliranje; ocean parametrov; samogretje

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1 Introduction

Inductors are important components of switched-mode power converters [1 - 4]. Properties of such converters depend on the properties of their structural components, i.e. the ferromagnetic core and the winding. Ferromagnetic materials used to build the core of the inductor are characterized by magnetization hysteresis characteristics. The magnetic permeability of the core, which is proportional to the inductance of inductors is a non-linear function of magnetic force and temperature [5 - 11].

In designing electronic circuits the computer programs dedicated to their analysis are used. Currently, one of most popular programs for this analysis is SPICE software [12 – 15]. The credibility of calculation results depends on the accuracy of the models of the used elements [16]. The inductor models typically use a linear model of the coil or non-linear model of the core and the linear model of the winding [2, 13, 17]. Nonlinear models of the core were presented in [3, 10, 13, 18, 19], but various modifications of the Jiles–Atherton model are the most commonly used models [6, 7, 11, 18, 19, 20]. This model does not take into account such an important phenomenon as self-heating.

In papers [3, 18] the electrothermal model of the chocking-coil for SPICE using the electrothermal core model presented in [11] is proposed. The electrothermal model of the choking–coil is devoted to calculate parameters of its model for the inductor used in the analyzed circuit. Therefore, it is important to prepare algorithm parameter estimation of such a model. This paper presents a modified form of the electrothermal model of the inductor, proposes the method for determining parameters of the model and provides an example of the results of calculations and measurements to illustrate the correctness of the elaborated method.

2 The electrothermal model of the inductor

The presented electrothermal model of the choking – coil takes into account electrical phenomena occur-

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ring in the winding, magnetic phenomena occurring in the core and thermal phenomena in the core and the winding. Due to the fact that the choking – coil core is made of soft magnetic material the hysteresis of the magnetization curve can be omitted in the model [6]. The considered electrothermal model of the choking - coil has the form of a sub-circuit of SPICE. The network representation of the elaborated model is presented in Figure 1. The model is composed of three blocks. The first block is the main circuit and it includes a series connection of controlled voltage sources E_{LS}, E_{RS}, the voltage source V_L with the zero value and the coil with inductance L equal to 2 μ H and the parallelly connected capacitor C_w modeling interturn capacitance of the winding.

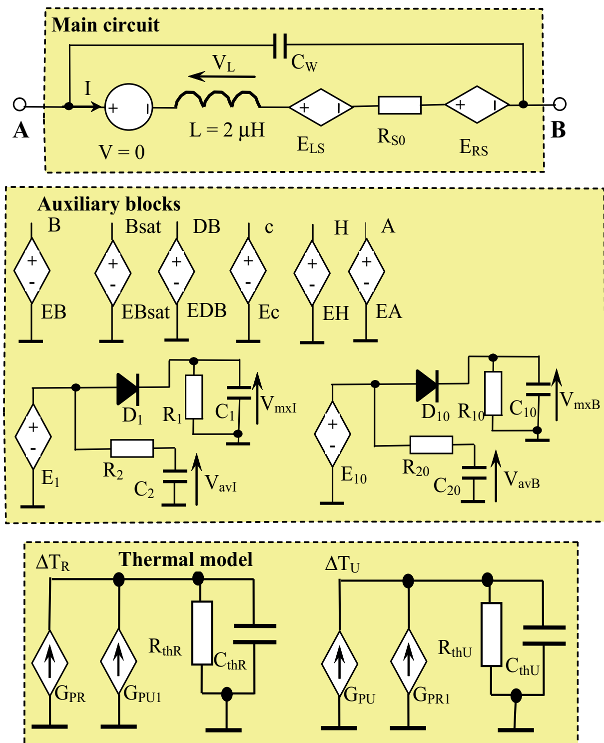


Figure 1: Network representation of the electrothermal model of the inductor

The voltage source V_L monitors the value of the current of the choking – coil. The coil L make it possible to calculate the time derivative of the current of the choking – coil. E_{LS} represents the voltage drop on non-linear inductance of the choking – coil and is described by the formula [3]

$$E_{LS} = w_S \cdot \frac{f \cdot V_L}{(f + f_b) \cdot L} \cdot L_S = w_S \cdot \frac{f \cdot V_L}{(f + f_b) \cdot L} \cdot \frac{z^2 \cdot S_{Fe} \cdot B_{sat} \cdot A}{l_{Fe} \cdot (|H| + A)^2 + A \cdot B_{sat} \cdot l_p / \mu_0} \quad (1)$$

where z denotes the number of turns in the choking–coil winding, V_L - voltage on the coil L, S_{Fe} - effective cross-section area of the core, B_{sat} – saturation magnetic flux density, H - magnetic force in the core, l_{Fe} - magnetic path in the core, A – the field parameter, l_p - air gap length in the core, μ_0 – permeability of free air, which amounts to 12.57 • 10^{-7} H/m, dB/dH – magnetic permeability of the core, f – the frequency of the inductor current, f_b - reference frequency.

The resistor R_{SO} represents series resistance of the inductor at temperature T_0. The value of this resistance is described by formula:

$$R_{SO} = \rho \cdot \frac{l_d}{S_d} \quad (2)$$

where ρ is resistivity of copper equal to 1.72 • 10^{-8} Ω•m at temperature 20° C, l_d is the length of winding, and S_d is the cross-section of the coil wire.

In turn, the controlled voltage source E_{RS} is described by:

$$E_{RS} = V_{RS} \cdot \alpha_\rho \cdot (T_U - T_0) + \frac{l}{d} \cdot \sqrt{\mu_0 \cdot \rho \cdot (1 + \alpha_\rho \cdot (T_U - T_0))} \cdot 2 \cdot (I - I_{av}) \cdot \sum_{n=1}^{4} \sqrt{n \cdot f} \cdot \left(a_n \cdot \cos\left(\frac{2 \cdot \pi \cdot f}{t}\right) + b_n \cdot \sin\left(\frac{2 \cdot \pi \cdot f}{t}\right) \right) + P_R \cdot \frac{I}{I_{sk}^2} \quad (3)$$

In the equation (3) there are three components. The first one models the dependence of series resistance on temperature. The V_{RS} is a component of the voltage across the resistor R_{SO}, α_ρ is the temperature coefficient of resistivity of copper, which amounts to 4.45 • 10^{-3} K^{-1} and T_U is temperature of the winding. The second component models the additional voltage drop at the choking–coil which is a result of the skin effect. To describe these phenomena one takes into account the fact that the current of the choking–coil operating in the dc-dc converter has a periodic triangular waveform. This waveform is modeled with a Fourier series, wherein the number of components is limited to four. The Fourier series coefficients of the model are described by:

$$a_n = \frac{2 \cdot \cos(2 \cdot n \cdot \pi \cdot (d_1 - 0{,}5) - (-1)^n)}{d_1 \cdot n^2 \cdot \pi^2 \cdot (1 - d_1)} \quad (4)$$

$$b_n = \frac{\sin(2 \cdot n \cdot \pi \cdot (d_1 - 0{,}5) - (-1)^n}{2 \cdot \pi^2 \cdot n^2 \cdot d_1 \cdot (1 - d_1)} \quad (5)$$

where I is choking–coil current, d – diameter of the coil wire, I_{av} – average value of the coil current calculated in the auxiliary block, d_1 - duty of the converter control signal, and f – frequency of this signal. The third component in the formula (3) represents the choking–coil voltage drop resulting from energy losses in the core. The P_R component describe energy losses in the core, I_{sk} is the RMS value of the choking–coil current.

In the auxiliary block the following are determined: magnetic force *H*, magnetic flux density *B*, the time derivative of the magnetic flux density *DB*, field parameter *A*, maximum and average values of the magnetic flux density and of the current, coefficient *c* defining the influence of the Curie temperature T_C on the value of the magnetic flux density. Inductance of the inductor is proportional to the magnetic permeability of the core corresponding to the characteristics *B(H)* slope [2, 6, 13]. To determine the value of the magnetic flux density the formula described in [6, 21] is used:

$$B = B_{sat} \cdot \frac{H}{|H| + A} \tag{6}$$

where B_{sat} is the saturation flux density of the core.

On the other hand, the value of the magnetic force is calculated by the formula [5]:

$$H = \frac{z \cdot I - \frac{B \cdot l_p}{\mu_0}}{l_{Fe} + l_p} \tag{7}$$

In the auxiliary block, the field parameter *A*, which makes it possible to take into account the influence of temperature on the magnetization curve and inductance of the inductor, is also determined. The dependence of the parameter *A* on temperature is described by the empirical formula:

$$A = A_0 \cdot \exp[(-T_R + T_a)/\alpha_T] \tag{8}$$

where α_T is the temperature coefficient of the parameter *A*.

It should be noted that the saturation flux density in the core also strongly depends on temperature and the inclusion of this impact has been expressed by the dependence [6, 10, 11]:

$$B_{sat} = B_{sat0} \cdot [1 + \alpha_{BS} \cdot (T_R - T_0)] \cdot c \tag{9}$$

where B_{sat0} is the saturation flux density at temperature T_0 and α_{BS} – the temperature coefficient of B_{sat}.

The *c* coefficient was defined by:

$$c = \begin{cases} 1 \quad for\ T_R < T_C \\ 1 - 0.1 \cdot (T_R - T_C) \quad for\ T_R < T_C + 10K \\ 0 \quad for\ T_R > T_C + 10K \end{cases} \tag{10}$$

where T_R denotes temperature of the core.

On the other hand, to calculate the average and peak-to-peak values of the current, and the magnetic flux density, two detectors are defined: the peak-to-peak value detector and the average value detector, consisting of the two-terminal networks R_1C_1 , R_2C_2 and $R_{11}C_{11}$, $R_{21}C_{21}$, diodes D_1 and D_{11}, the controlled voltage sources E_1 and E_{11}, respectively representing the inductor current and the magnetic flux density of the core.

The thermal model is used to determine the core temperature T_R and the winding temperature T_U of the inductor using the compact model proposed in [6, 12, 16, 22 , 23]. This model includes two controlled current sources, representing power losses in the core G_{PR} and in the winding G_{PU}, respectively. The included in this two-terminal circuits R_{thR}, C_{thR} and R_{thU}, C_{thU} represent thermal time constants of the core and the winding, so that it is possible to take into account the phenomena of self-heating. These time constants fulfill equations describing the relation between the controlled current sources and G_{PU1} used for modeling the thermal coupling between the core and winding. The currents of these sources are respectively 0.8 G_{PR} and 0.8 G_{PU}. Depending how one defines a power loss in the winding, G_{PU} includes resistive losses and the skin effect . The losses in the winding are described by the formula:

$$P_U = \rho \cdot I^2 \cdot [1 + \alpha_\rho \cdot (T_U - T_0)] + l/d \cdot \sqrt{\mu_0 \cdot \rho \cdot f \cdot (1 + \alpha_\rho \cdot (T_U - T_0))} \cdot 2 \cdot \sum_{n=1}^{4} \sqrt{n \cdot f} \cdot \left(a_n \cdot \cos\left(\frac{2 \cdot \pi \cdot f}{t}\right) + b_n \cdot \sin\left(\frac{2 \cdot \pi \cdot f}{t}\right)\right) \cdot (I_{mx} - I_{av})^2 \tag{11}$$

where I_{mx} is the maximum coil current calculated in the auxiliary block.

In turn, the core losses are described by [10]:

$$P_R = V_e \cdot \left(\frac{DB}{2}\right)^{\beta - \alpha} \cdot (1 + D \cdot (T_R - T_m))^2 \cdot \frac{P_{V0}}{T} \cdot \int_0^T \left|\frac{dB}{dt}\right|^\alpha dt \tag{12}$$

where V_e denotes the equivalent volume of the core, P_{V0} are volumial power losses in the core, *DB* is the magnitude of flux density, *D* – the square temperature coefficient of power losses P_{v0}, *T* - period of a inductor current, *α* and *β* are exponents in the dependence of core losses based on frequency and amplitude of the flux density in the choking–coil, respectively, T_m is the temperature, at which losses are minimal.

3 Parameter estimation

The presented model is described by 20 parameters that can be divided into 3 groups:

a. electrical parameters,
b. magnetic parameters,
c. thermal parameters.

The proposed estimation algorithm uses the concept of local estimation described in [22, 24]. According to this concept, the model parameters are estimated in groups on the basis of the measured characteristics of the inductor operating in specific conditions.

The magnetic parameters of the choking–coil corresponding to the ferromagnetic core reactor can be divided into three groups:

- The parameters of ferromagnetic material, of which the core is made, related to the hysteresis loop, such as the saturation flux density B_{sat0}, the Curie temperature T_C, the field parameter A, the air gap length l_p, the temperature coefficient of saturation flux density changes α_{BS}, the temperature coefficient α_T of the magnetic field parameter,
- The geometric parameters of the core, such as the magnetic path length in the core l_{Fe}, the equivalent value of the core volume V_e, the effective cross-section area of the core S_{Fe},
- The ferromagnetic material parameters corresponding to core losses such as P_{V0}, D, α, β .

Some parameters associated with the magnetic material used to construct the ferromagnetic core can be read directly from the catalog data supplied by manufacturers e.g. the saturation flux density B_{sat0} and the Curie temperature T_C [22].

In order to determine the temperature coefficient of saturation flux density changes the designer needs to:

1. Read from the catalog characteristics , eg, [25, 26], the value of the saturation flux density B_{sat0} at the reference temperature T_0 and the value of this parameter B_{sat1} at a different temperature T_1.
2. Calculate the value of the temperature coefficient of saturation flux density changes according to the formula [22] :

$$\alpha_{BS} = \frac{B_{sat1} / B_{sat0} - 1}{T_1 - T_0} \tag{13}$$

The geometric parameters of the cores should be read from the catalog data or should be determined basis of the dimensions of the core and calculated using the basic geometrical relationships. For example, to determine the geometrical parameters of the ring core one should:

1. determine the dimensions of the core (Fig. 2), i.e. the outer diameter d_z, the inner diameter d_w and height h_R (these data are usually contained in the name of the core, e.g. RTP 26,9 x14, 5x11)

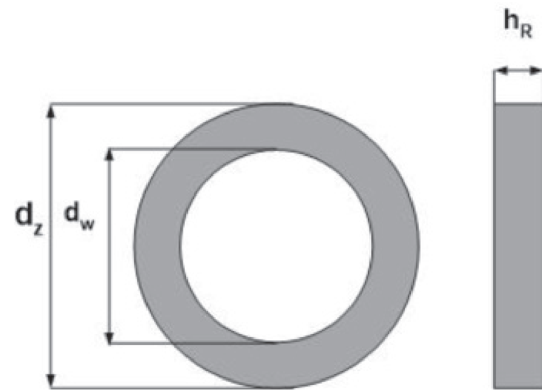


Figure 2: Dimensions of the ring core

2. calculate the magnetic path length in the core l_{Fe} using the formula

$$l_{Fe} = \pi/2 \cdot (d_z + d_w) \tag{14}$$

3. calculate the effective cross-section area of the core S_{Fe} using the formula:

$$S_{Fe} = \frac{(d_z - d_w) \cdot h_R}{2} \tag{15}$$

4. calculate the equivalent value of the core volume V_e by:

$$V_e = \frac{\pi \cdot (d_z^{\ 2} - d_w^{\ 2}) \cdot h_R}{4} \tag{16}$$

In order to determine the values of the parameters A, w_s, and l_p it is necessary to measure the dependence of inductance L on the DC current using the measurement system described in [27]. The measurement should be performed at the frequency $f << f_b$. In the measured characteristics of $L(i)$, whose typical course is shown in Figure 3 one should select 3 points: $X_1(I_1, L_1)$, $X_2(I_2, L_2)$ and $X_3(I_3, L_3)$. Then, the following system of equations must be solved for w_S, l_p and A:

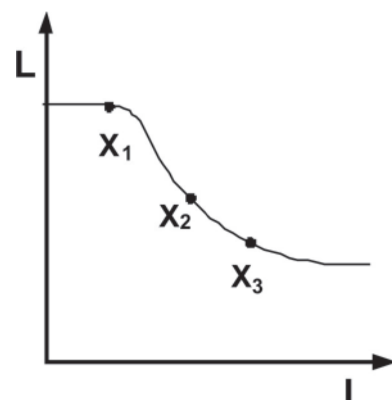


Figure 3: Typical course of the dependence of inductance of the inductor on the dc part of its current

$$\begin{cases} L_1 = \dfrac{w_S \cdot z^2 \cdot S_{Fe} \cdot B_{sat} \cdot A}{l_{Fe} \cdot \left(\dfrac{z \cdot I_1 - B_{sat} - A \cdot x + \sqrt{B_{sat}^2 + z^2 \cdot I_1^2 + A^2 \cdot x^2 + 2 \cdot A \cdot x \cdot (B_{sat} + z \cdot I_1) - 2 \cdot B_{sat} \cdot z \cdot I_1}}{2 \cdot x} + A \right)^2 + A \cdot B_{sat} \cdot l_p / \mu_0} \\ L_2 = \dfrac{w_S \cdot z^2 \cdot S_{Fe} \cdot B_{sat} \cdot A}{l_{Fe} \cdot \left(\dfrac{z \cdot I_2 - B_{sat} - A \cdot x + \sqrt{B_{sat}^2 + z^2 \cdot I_2^2 + A^2 \cdot x^2 + 2 \cdot A \cdot x \cdot (B_{sat} + z \cdot I_2) - 2 \cdot B_{sat} \cdot z \cdot I_2}}{2 \cdot x} + A \right)^2 + A \cdot B_{sat} \cdot l_p / \mu_0} \\ L_3 = \dfrac{w_S \cdot z^2 \cdot S_{Fe} \cdot B_{sat} \cdot A}{l_{Fe} \cdot \left(\dfrac{z \cdot I_3 - B_{sat} - A \cdot x + \sqrt{B_{sat}^2 + z^2 \cdot I_3^2 + A^2 \cdot x^2 + 2 \cdot A \cdot x \cdot (B_{sat} + z \cdot I_3) - 2 \cdot B_{sat} \cdot z \cdot I_3}}{2 \cdot x} + A \right)^2 + A \cdot B_{sat} \cdot l_p / \mu_0} \end{cases} \quad (17)$$

Where $x = \mu_0 \cdot l_p \cdot (l_{Fe} + l_p)$.

In order to determine the value of the temperature coefficient α_T, it is necessary to measure the dependence of $L(i)$ for the temperature $T_1 > T_0$, and then to determine the value of the parameter A_1 at temperature T_1 using the formula (17). The value of α_T is given by:

$$\alpha_T = \frac{T_0 - T_R}{\ln(A_1 / A_0)} \quad (18)$$

In order to determine the parameters describing losses in the core:

1. one should read from the catalog characteristics of the core material describing the dependence of power losses density P_v on the amplitude of the magnetic flux density (B_m) at constants frequency f, the coordinates of two points $X_4(B_{m1}, P_{V1})$ and $X_5(B_{m2}, P_{V2})$. The typical course of such characteristics is shown in Figure 4. Next, one should calculate the value of the β coefficient by the formula:

$$\beta = \frac{\log(P_{v1} / P_{v2})}{\log(B_{m1} / B_{m2})} \quad (19)$$

2. to determine the coefficient α one should read from the catalog characteristics describing the dependence of the power density of the core loss on frequency (Fig. 4b) at the known amplitude B_m in points $X_6(f_1, P_{V3})$ and $X_7(f_2, P_{V4})$ and calculate the value of the factor α from the formula:

$$\alpha = \frac{\log(P_{v3} / P_{v4})}{\log(f_1 / f_2)} \quad (20)$$

3. to determine the parameter P_{V0} it is necessary to read point e.g. $X_6(f_1, P_{V3})$ from the characteristics describing the dependence of power density losses P_V on frequency at the constant value of B_m (Fig. 4b) and next, calculate the value of P_{V0} from:

$$P_{VO} = \frac{P_{v3}}{f_1^{\alpha} \cdot B_m^{\beta} \cdot (2 \cdot \pi)^{\alpha} \cdot [0.6336 - 0.1892 \cdot \ln(\alpha)]} \quad (21)$$

4. in the catalog characteristics $P_v(T)$ at first one should read the value of temperature T_m at which the characteristics of $P_v(T)$ reaches the minimum at point $X_8(T_m, P_{V5})$ (Fig. 4c), then one should select point $X_9(T_6, P_{V6})$ of some characteristics and calculate the parameter D by the formula:

$$D = \frac{Pv_6 - Pv_5}{Pv_5 \cdot (T_6 - T_m)^2} \quad (22)$$

In turn, the value of the parameter f_b associated with the dependence defining the output voltage of the controlled voltage source E_{LS} can be determined from the dependence describing the characteristics of the magnetic permeability μ of the core of the frequency $\mu(f)$, whose typical course is shown in Figure 5.

The frequency f_b is calculated by the formula

$$f_b = \frac{f_1 \cdot \mu_1 - f_2 \cdot \mu_2}{\mu_2 - \mu_1} \quad (23)$$

where in the calculations the coordinates of two points $X_{10}(f_1, \mu_1)$ and $X_{11}(f_2, \mu_2)$ lying on the curve $\mu(f)$ were used.

To the electrical parameters appearing in the description of the electrothermal model of the inductor belong

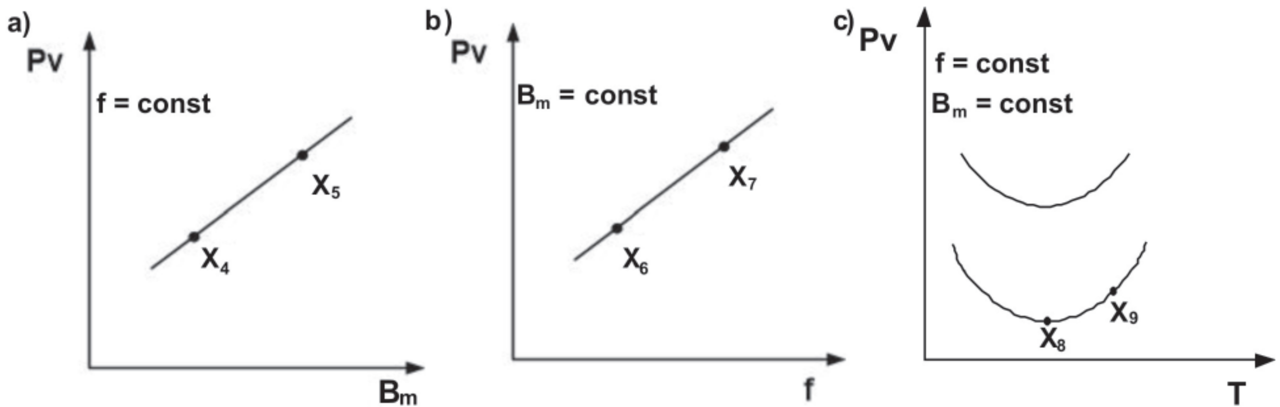


Figure 4: Dependences of power losses density on the amplitude of the flux density (a), frequency (b) and temperature (c)

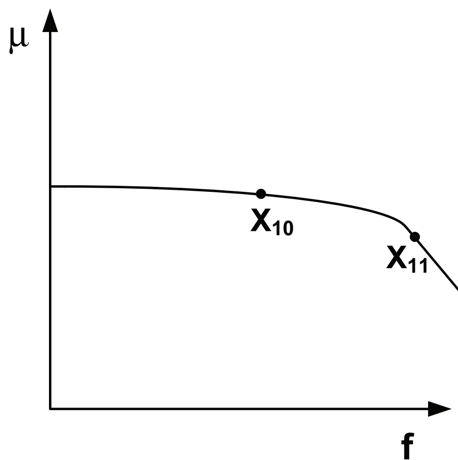


Figure 5: Typical dependence of magnetic permeability of the ferromagnetic core on frequency

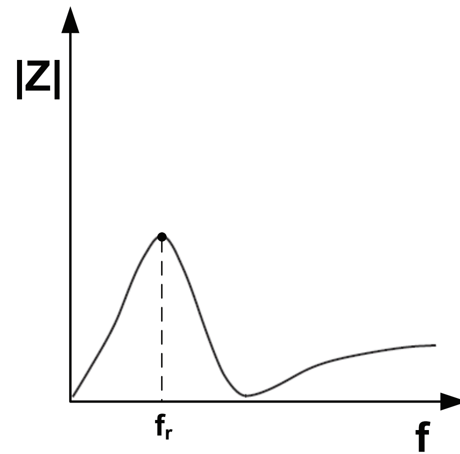


Figure 6: Typical dependence of the module of inductor impedance on frequency

also length of the winding l_d and cross-section of the coil wire S_d. These parameters are used to determine series resistance of the coil. The length of the winding for the ring core is estimated by calculating the product of the number of turns z and the girth of cross-section of the core, assuming that it is rectangular, by the formula:

$$l_d = 2 \cdot z \cdot \left(h_R + \left(\left(d_z - d_w\right)/2\right)\right) \tag{24}$$

In turn, the cross-sectional area of the wire is calculated on the basis of simple geometric formulas and the known wire diameter d_3.

The capacitor C_w is determined by the formula:

$$C_w = \left(f_r^2 \cdot 4 \cdot \pi^2 \cdot L_0\right)^{-1} \tag{25}$$

where f_r is resonant frequency of the inductor, L_0 is the inductance value for $I_{DC} = 0$. The resonant frequency of the chocking - coil can be read from the course of the dependence of the impedance module, whose typical course is shown in Figure 6, on frequency.

To determine the thermal parameters a_i, τ_{thi}, R_{thi} it is necessary to perform measurements of their own transient thermal impedance of the winding $Z_{thu}(t)$ and of the core $Z_{thr}(t)$, as well as the mutual transient thermal impedance between the core and the winding $Z_{thur}(t)$ using the method described in [28]. Based on the measured waveforms $Z_{thu}(t)$, $Z_{thr}(t)$ and $Z_{thur}(t)$ the values of capacitance and thermal resistance are calculated using the method described in [22, 23].

4 Experimental results

In order to verify the correctness of the proposed method of estimating parameters of the inductor, the values of the parameters of two arbitrarily selected inductors with ferromagnetic cores were estimated and the calculated and measured characteristics of these inductors were compared. The investigations were performed for two inductors containing ring cores of the same size (26.9 mm x 14.5 mm x 11 mm). The first one was the core RTF of ferrite material F-867 and the other

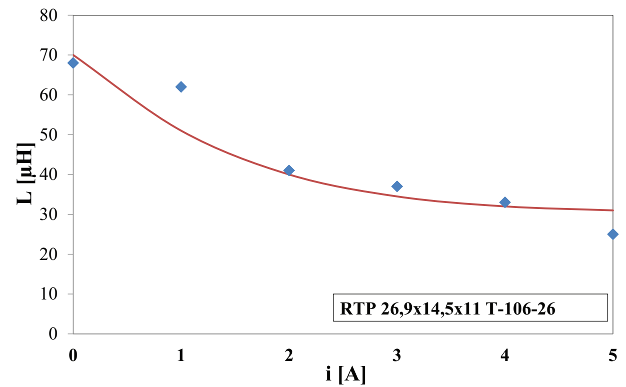
was the core RTP of powdered iron from the material T106 -26. On both the cores 20 turns of the enameled copper wire of 0.8 mm diameter were wound. Using the estimation algorithm proposed in the previous section, the values of all the model parameter values were read or calculated and collected in Table 1.

The measured and calculated characteristics of the considered inductors are shown in Figures 7 – 8. In these figures the results of measurements are denoted as points, whereas the results of electrothermal analysis are represented by lines.

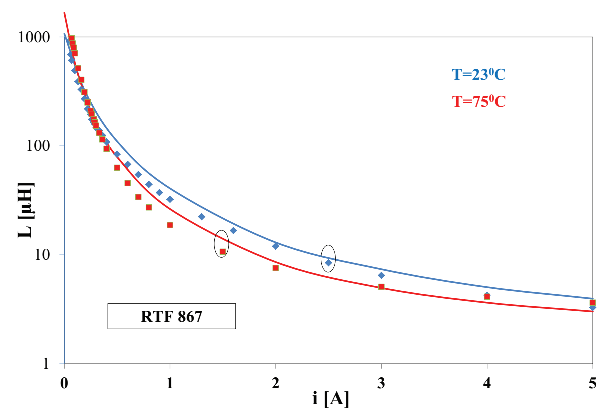
Table 1: Values of parameters of the electrothermal model of inductors with the cores RTP T106-26 and RTF F 867.

Parameter	B_{sat0} [T]	l_p [μm]	T_C [K]	A [A/m]	α_{BS} [1/K]
RTP T106-26	1.38	14	1023	4024	$2.8\cdot10^{-3}$
RTF F867	0.5	0.1	488	260	$2.8\cdot10^{-3}$
Parameter	ws	l_{Fe} [mm]	V_e [m³]	S_{Fe} [m²]	z
RTP T106-26	0.5	64.99	$4.43\cdot10^{-6}$	$68.2\cdot10^{-6}$	20
RTF F867	0.5	62.8	$3.14\cdot10^{-6}$	$50\cdot10^{-6}$	20
Parameter	S_d [m²]	l_d [m]	P_{v0} [kW/m³]	D [K⁻²]	α
RTP T106-26	$502\cdot10^{-9}$	0.6	2	0	1.59
RTF F867	$502\cdot10^{-9}$	0.6	100	$0.5\cdot10^{-6}$	1.02
Parameter	β	α_T [1/K]	T_m [K]	f_b [kHz]	d [mm]
RTP T106-26	2.15	$100\cdot10^{3}$	368	546	0.8
RTF F867	2.82	240	343	850	0.8

Figure 7 shows the dependence of inductance on the DC current of the inductor containing the powder core RTP T106 -26 (Fig. 7a) and the inductor with the ferrite core RTF F867 (Fig.7b) The tests were performed at frequency of 100 kHz for two ambient temperatures equal to 23 and 75°C. As you can see, good agreement between the results of measurements and calculations was obtained. For both the considered choking–coil the dependence *L(i)* is a decreasing function of the current, where the choking–coil with the ferrite core with the same geometrical dimensions achieved a higher value of inductance, moreover a wider range of changes in its value was observed. A decrease in inductance of the ferrite core (even two hundreds times) was much larger than for the core of the powdered iron (about 30 %). The different courses of the dependence *L(i)* for both the inductors were due to the non-linear magnetization curve of ferromagnetic cores. It is worth noticing that the course of the dependence *L(i)* for the choking–coil with the ferrite core showed the visible influence of the ambient temperature on its course, while for the inductor with the powder core such influence is not observed. In the characteristics of the choking–coil with the ferrite core an increase in temperature equal to 50 °C caused an increase in its inductance even up to 45 %.



(a)

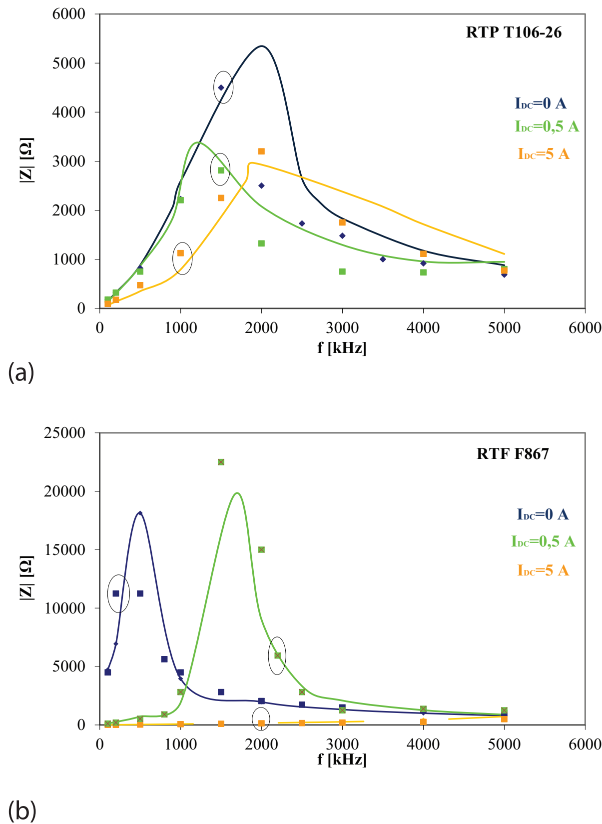


(b)

Figure 7: Measured and calculated dependence of inductance of inductors with the powder (a) and ferrite (b) cores on the current

Figure 8 shows the dependences of the module of impedance of the choking–coils with the considered cores on frequency at the constant values of the DC current. As it is visible, good agreement between the measurements and calculations results was obtained. By considering winding capacitance in the electrothermal model of the choking–coil the resonance on these characteristics was obtained, which corresponds to the obtained measurement results. The value of the resonant frequency for the ferrite core increases with an increase of the DC current, whereas for the powder core it oscillates in the range of 1.3 MHz to about 2.3 MHz.

In order to illustrate the influence of the nonlinearity of the inductor and the self-heating phenomena in this element on characteristics of dc-dc converters, the results of calculations (lines) and measurement (points) of the boost converter with the core RTP T106-26 [29] were presented in Figs. 9 and 10. In Fig.9 calculated and measured dependences of the output voltage V_{out}



(a)

(b)

Figure 8: Calculated and measured dependences of the module of impedance of inductors with the powder (a) and ferrite (b) cores on frequency

of the examined converter on the load resistance R_0 at the fixed value of the duty factor of the control signal d = 0.5 at two values of the frequency of the control signal equal in turn 50 kHz and 400 kHz, are presented. Results of calculations passed with the use of the electrothermal model of the inductor are marked with solid lines, whereas results of calculations obtained by means of the linear model of the inductor are marked with dashed lines.

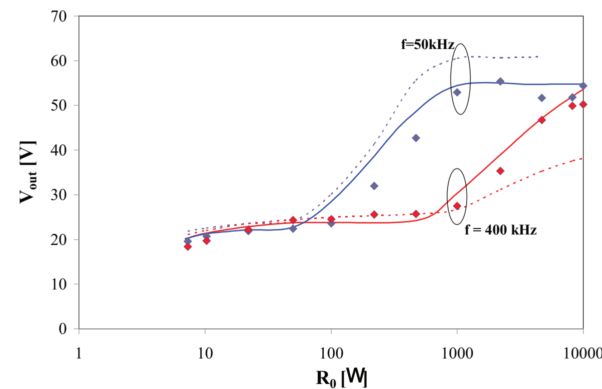


Figure 9: Calculated and measured dependences of the output voltage of the boost converter on the load resistance

As one can notice, the use of the electrothermal model of the inductor makes possible to obtain the considerably better agreement between performance of calculations and measurement than with the use of the linear model of the inductor. It is proper to notice that the regard of losses in the inductor and dependences of the inductances on frequency causes a decreasing in the output voltage of the considered converter. The use of the linear model of the inductor can cause the overestimate of results of calculations even about 50%.

In turn, Fig.10 illustrates the dependence of the core temperature T_R (solid lines) and the winding temperature T_U (dashed lines) on the load resistance corresponding to characteristics from Fig.9. As it is visible, for both considered frequencies the decreasing dependences $T_R(R_0)$ and $T_U(R_0)$ are obtained, whereas an increase in frequency causes a decrease in value of the temperature of the inductor. From the fact, that the winding temperature is lower than the core temperature results, that a main source of losses is the core of the inductor.

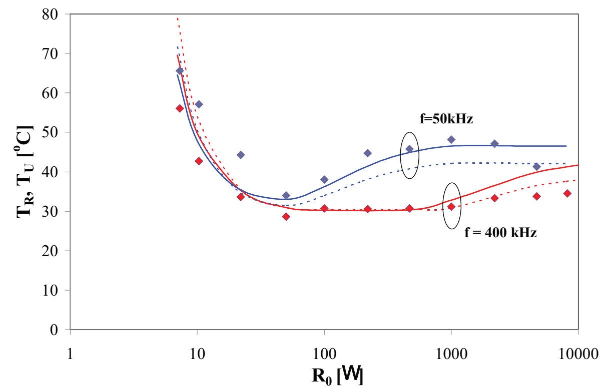


Figure 10: Calculated and measured dependences of the core and winding temperatures of the load resistance

5 Conclusions

This paper describes the electrothermal model of the choking–coil with ferromagnetic the core dedicated for SPICE software and proposes a method of estimating values of magnetic, electrical and thermal parameters of this model. The proposed algorithm is simple to implement and largely uses the data presented by manufacturers of the ferromagnetic core and winding wire in the catalog data.

The investigations were performed for two arbitrarily chosen inductors with the core made of powdered iron and ferrite material. The presented experimental results show that the proposed method of estimating the

parameters is correct, which is proved by good agreement between the measured and calculated characteristics of the considered inductors.

The electrothermal model of the inductor together with the proposed estimation method of its parameters can be useful for designers of switch-mode power supplies and in the analysis of the considered class of electronic circuits.

6 Acknowledgements

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A 5-Gbps CMOS Burst-Mode CDR Circuit With an Analog Phase Interpolator for PONs

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Abstract: This paper presents a 5-Gb/s low-power burst-mode clock and data recovery circuit based on analog phase interpolator for passive optical network applications. The proposed clock recovery unit consists of two double-edge triggered sample-and-holds (DT-SHs) and a phase interpolator. The PI instantaneously locks the recovered clock to incoming burst-mode data by coefficients generated at the DT-SHs' outputs. To reduce power dissipation in clock recovery unit, instead of two buffers, only one is utilized for the DT-SH. The proposed PI-based BM-CDR has been designed and simulated in 0.18-µm standard CMOS technology. The Results show that reduction in power dissipation of 40% for the clock recovery unit has been achieved. The proposed BM-CDR circuit retimes data at 5Gb/s for a 2^{10}-1 pseudo-random binary sequence within the first UI. The recovered data shows jitter at 14ps (pp). The circuit, including 1:2 data demux, draws 29mW power from a 1.8-V supply.

Keywords: Burst mode communications; Passive optical networks; Clock and data recovery; Phase interpolator; Sample and hold

5-Gbps CMOS vezje s hitrim dostopom zaporednih naslovov in anlognim faznim interpolatorjem za PON

Izvleček: Članek predstavlja 5Gb/s urno in podatkovno reševalno vezje s hitrim dostopom zaporednih naslovov na osnovi analognega pasivnega interpolatorja za pasivna optična omrežja. Predlagana enota za obnavljanje ure vsebuje dvorobno proženo vezje vzorčenja (DT-SHs) in fazni interpolator. PI hkratno zaklene obnovljeno uro na pridobljen podatek s koeficienti, ki jih generira izhod DT-SHs. Namesto dveh predpomnilnikov je, za zagotavljanje nižje porabe energije, uporabljen le eden. Meritve kažejo na 40 % znižanje porabe energije. Predlagano vezje je simulirano in načrtovano v 0.18 µm CMOS tehnologiji. Predlagano BM-CDR vezje obnavlja podatke s 5 Gb/s za 2^{10}-1 psevdonaključno zaporedje v prvem UI. Restavrirani podatki kažejo jitter 14ps (pp). Poraba energije pri napajalni napetosti 1.8 V je 29 mW.

Ključne besede: komunikacija s hitrim dostopom zaporednih podatkov; pasivna optična omrežja; restavriranje podatkov in ure; fazni interpolator

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1 Introduction

Optical access networks for the development of broadband services have been widely used. Fiber-to-the-home (FTTH), which is one of typical services of optical access networks, has grown rapidly [1]. Passive optical network (PON) architecture is considered to be an effective solution in such networks [2]. PON is based on point to multipoint configuration where the receiver in the optical line terminal (OLT) must deal with several packets with different amplitudes and phases, which are transmitted from optical network units (ONUs). An optical splitter, that does not need electrical power, provides splitting of bit streams to ONUs, and multiplexing of traffic flows from ONUs [1]. Downstream traffic from the OLT is transmitted to all ONUs in continuous mode (CM), and each ONU selects traffic addressed to itself. In the upstream path ONUs transmit data to the OLT using time-division multiple access (TDMA) to provide time slot assignments for each ONU [3]. Therefore, the time between packets is short, and the OLT in central office requires clock and data recovery (CDR) circuit to be capable of fast data re-generation. Fig. 1 illustrates a PON system. This communications is called burst-mode (BM) in which data transmitted to the receiver is in burst packets. In synchronous optical networks (SONET), jitter transfer function is an important parameter and

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SONET has stringent jitter specifications. However, in PON where the transfer mode is asynchronous [2], we are able to trade off the loop bandwidth with jitter thus obtaining fast locking. In burst-mode communications, BM-Rx needs to work with BM-CDR with an instantaneous locking method to be able to deal with burst data. Accordingly, several approaches have already been proposed to form BM-CDRs with short phase acquisition time. For instance, in [4] BM-CDR based on injection-locking is proposed where its potential to fail lock is unacceptable at high-speed circuits due to process, voltage, and temperature variations. BM-CDR based on gated-voltage controlled oscillator (GVCO) is presented in [5], but it suffers from mismatches between the VCOs and incoming data rate, resulting in low consecutive identical digits (CIDs) tolerance. Moreover single GVCO approach is presented in [6]. The oversampling technique is capable of fast phase locking, reported in [7,8], however its power dissipation is remarkably high. Another approach employs the use of broad-band phase-locked-loops (PLLs) requiring high bandwidth for instantaneous locking, thereby jitter reduction is not well achieved in this approach. The work in [9] addresses PLL based BM-CDR. A new approach based on phase interpolator has recently been proposed [10], which has several advantages such as fast acquisition time and low power dissipation over previous methods.

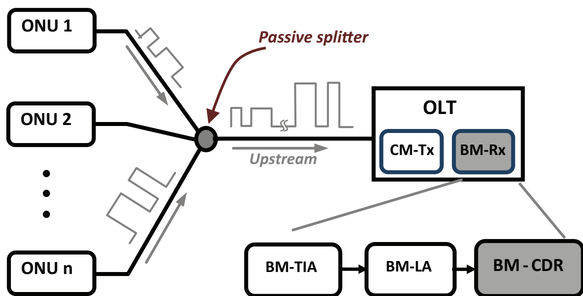

Figure 1: Application of burst-mode CDR in a passive optical network

In this paper we propose a novel phase interpolator (PI)-based BM-CDR circuit with a new structure for double-edge triggered sample-and-hold (DT-SH). The DT-SH utilizes one shared-buffer between two single-edge triggered S/H (ST-SH) to increase the speed and reduce the power. This paper is organized as follows: Section II describes the architecture of the BM-CDR and the design and analysis of each building block. Section III presents simulation results. Discussion and conclusions are given in section IV.

2 BM-CDR Architecture

Fig. 2 shows the block diagram of the proposed PI-based burst-mode CDR circuit. As seen, input data is applied to the DT-SHs to sample and hold quadrature clocks at both rising and falling edges of the data. The DT-SH consists of two ST-SHs, followed by a buffer which is shared between them. DT-SHs provide the sampled values of S_1 and S_2 for the PI in order to recover clock at the output of clock recovery unit. In this way, the rising edge of the recovered clock is placed at the midpoint of incoming burst data, so that optimum sampling can be achieved in the flip-flop. Next, the frequency divider provides 2.5GHz-clock from the recovered clock in order to generate de-multiplexed data at a rate of 2.5Gb/s. In the following section, we first analyze the principle of analog phase-interpolation technique and afterwards we present the proposed structure for the DT-SH.

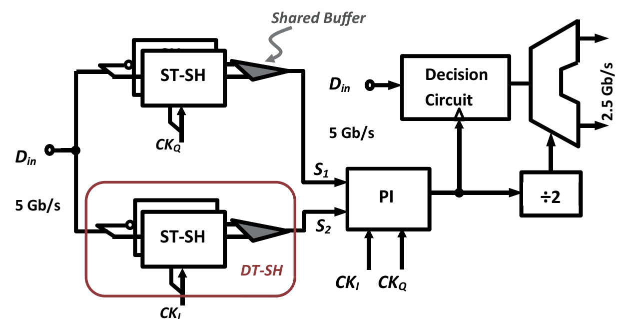

Figure 2: Block diagram of the proposed BM-CDR

2.1 Phase Interpolator

An important consideration on the subject of phase interpolators is their controller which can be either digital or analog. As explained in [11], digitally controlled PI due to low phase resolution and speed limitation, degrades jitter performance of the CDR. Hence we utilized analog PI in this work. Digitally controlled PI in continuous-mode CDR is reported in [12]. Assuming two input quadrature clock signals, CK_I and CK_Q, $sin2\pi ft$ and $-cos2\pi ft$, respectively, are applied to the phase interpolator circuit of Fig. 3. The PI circuit multiplies these two signals, producing a clock at the output with the same frequency as quadrature clocks. In fact, the summation is performed in the PI core, and the output current of differential stages are summed on the load resistor. In order to obtain a phase range between 0° to 360°, four differential stages instead of two, are used in the schematic of the PI. However, one can use both positive and negative values for weighting factors to provide a 360° phase range. But this method, due to the need for switching of input clocks, produces additional jitter. The phase and amplitude of the interpolated signal is controlled by the current sources of the PI that realize the weighting factors. It is desired to have a recovered clock whose falling edge is aligned with data transition. Consequently, in the decision circuit, input data is being sampled at its midpoint by rising edge of the recovered clock. Every single transition of data samples and holds

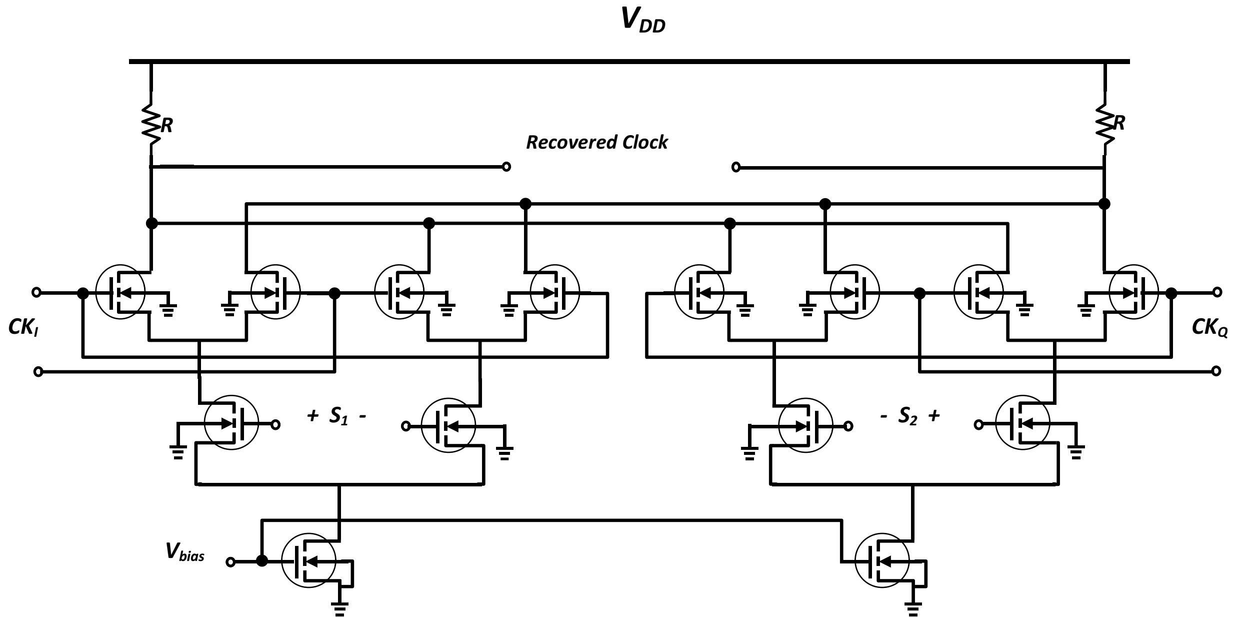

Figure 3: PI schematic

CK_I and CK_Q, and provides voltage levels for the current tails of the phase interpolator circuit. A data transition at $t=t_0$ results in the PI coefficients of S_1 and S_2.

The achieved recovered clock at the output of the PI is given in Eq. (1) where it describes a clock whose falling edge coincides with the data transition [10].

$$Recovered\ \mathrm{CK} = (\mathrm{S}_1 \cdot CK_1) + (S_2 \cdot CK_O) \quad (1)$$

$$CK_1 = \sin(2\pi\ \mathrm{ft}) \quad (1.a)$$

$$CK_Q = \cos(2\pi\ \mathrm{ft}) \quad (1.b)$$

In the presence of data transition, the sampled values of input quadrature clocks at t_0 yield the coefficients below:

$$CK_I(t = t_o) = \sin(2\pi\ \mathrm{ft}_0) = S_2 \quad (2.a)$$

$$CK_Q(t = t_o) = -\cos(2\pi\ \mathrm{ft}_0) = S_1 \quad (2.b)$$

Substituting the above coefficients in Eq. (1) yields the recovered clock below:

$$\text{Recovered } CK = -\cos(2\pi\ \mathrm{ft}_0) \cdot \sin(2\pi\ \mathrm{ft}) - \\ -\cos(2\pi\ \mathrm{ft}) \cdot \sin(2\pi\ \mathrm{ft}_0) \quad (3)$$

$$\text{Recovered } CK = -\sin\{2\pi\ \mathrm{f}(\mathrm{t} - \mathrm{t}_0)\}$$

This shows that the clock's falling edge is aligned with every data transition, where its rising edge sample the jittered data at its midpoint in the decision circuit. Ideally any change in data transition causes proportional change in DT-SHs output, and subsequently PI output phase changes. In order to have linear phases at the PI output, having sinusoidal values for control signals S_1 and S_2 are necessary, and Eq. (4) must be satisfied for any values of the coefficients [11].

$$S_1^2 + S_1^2 = const. \quad (4)$$

Equation (4) leads to a circle in Fig. 4(b). However, in practice implementing sinusoidal control signals to PI tail is not easily possible; hence, as seen in Fig. 4(b), a triangular approximation can be used. This approximation only effects on the amplitude of recovered clock. We can see that the phase of the recovered clock is the same as ideal one.

2.2 Double-edge Triggered Sample and Hold

In the PI-based BM-CDR, sample-and-hold plays a critical role in the performance of overall architecture. In the block diagram of Fig. 2, two double-edge triggered S/Hs (DT-SHs) are utilized in which input data samples and holds quadrature clocks, producing voltage levels to drive current sources of the PI. In this work we proposed a new technique for the two DT-SHs to share a single buffer in order to sum the sampled values by both rising and falling edge of data and to bring them into one common path, thereby saving power in the idle mode of each buffer is possible. In this way the power dissipation in the DT-SHs will become half of the conventional work in [10] wherein each DT-SH employs two buffers. Since the power consumption of the DT-SHs is relatively high, it considerably reduces the overall power dissipated in clock recovery unit. Fig. 5(a) shows the proposed technique where a DT-SH, with the highlighted shared buffer, is presented. The schematic diagram of the sampling switch is depicted in Fig. 5(b). The sampled values are given below, each

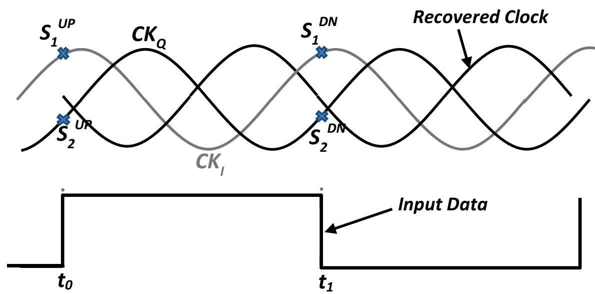

Figure 4a: The use of quadrature clocks for sampling

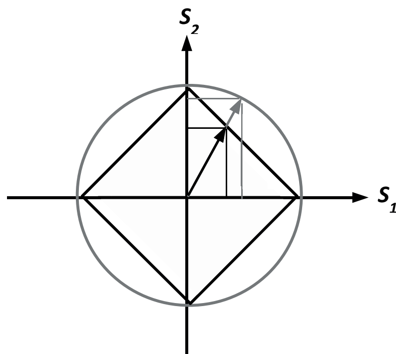

Figure 4b: Weighting factors S_1 and S_2 for an ideal PI (dashed line) and the practical one (solid line)

having differential values which are illustrated in the model of Fig. 4(a).

S_1^{UP} : CKQ Sampled at rising edge of data at t_o

S_1^{DN} : CKQ Sampled at falling edge of data at t_1

S_2^{UP} : CKI Sampled at rising edge of data at t_o

S_2^{DN} : CKI Sampled at falling edge of data at t_1

To reduce charge injection, differential structure for the ST-SHs is utilized. Besides, dummy transistor is also used to alleviate charge injection. Since the clock frequency is ideally equal to the data bit rate, the samples at rising edge and falling edge of data are the same. Thereby, as illustrated in Fig. 4(a), we have:

$$S_1^{UP} = S_1^{DN} = S_1$$

$$S_2^{UP} = S_2^{DN} = S_2$$

In order to achieve a high sampling rate and short acquisition time, an open-loop sample-and-hold configuration is of interest here. At high sampling rates, the needs for larger switch and smaller hold capacitance increase, which make charge injection worse. This phenomenon is likely to result in a large value of error

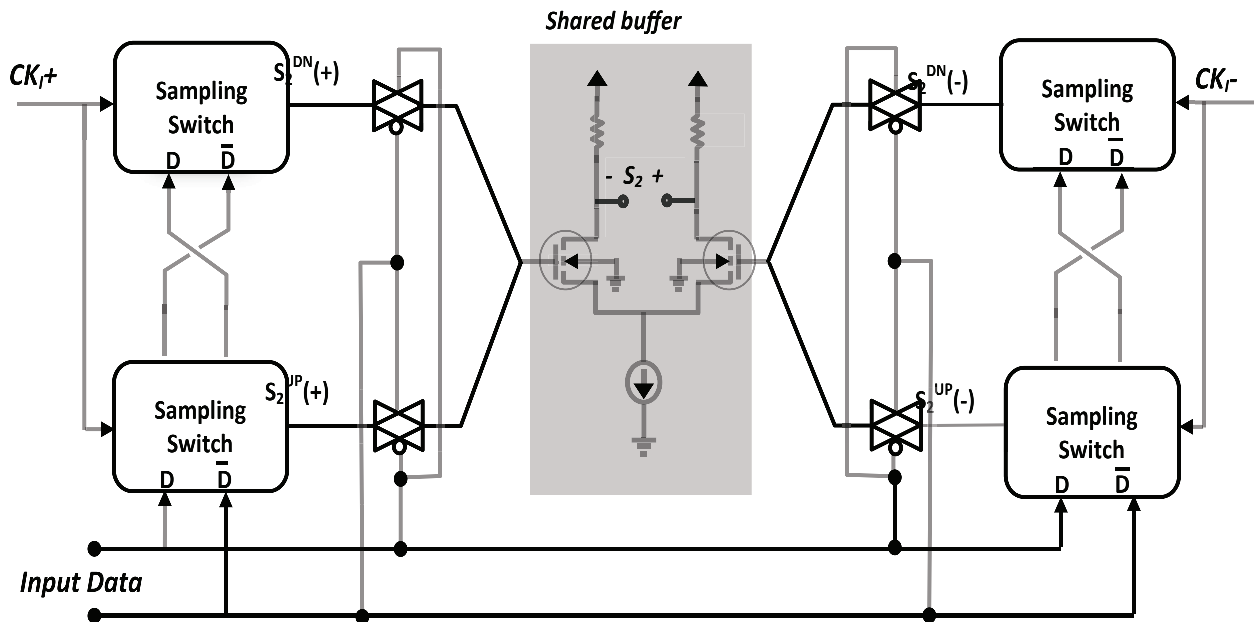

Figure 5a: Double-edge triggered S/H (DT-SH): Sampling of CK_I at both rising edge and falling edge of data

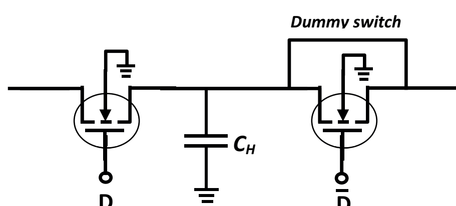

Figure 5b: Circuit implementation of the sampling switch

voltage. Both device size and hold capacitance directly effect on error voltage, creating variations in sampled values at sampling switches' output. Subsequently, tail currents in the PI vary, resulting in a poor jitter performance in the recovered clock. By choosing the size of dummy switch, half of the main switch, we can effectively remove the error voltage caused by charge injection [13]. Moreover, fully differential design makes it ro-

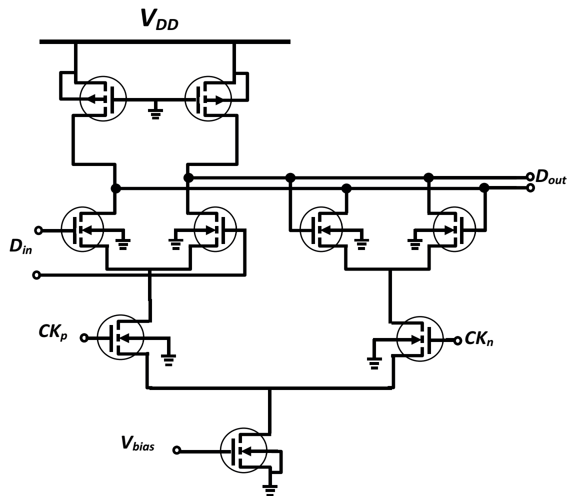

Figure 6a: CML latch

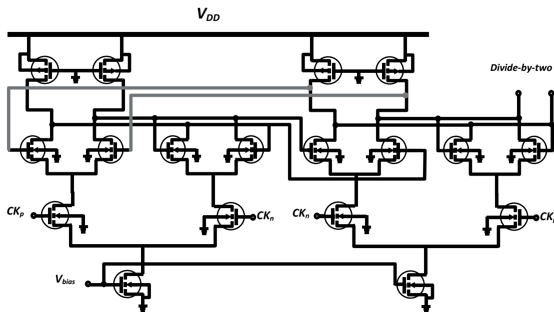

Figure 6b: Frequency divider: divide-by-two

bust against noise and other non-idealities. Therefore the shortcoming can be eliminated as well.

The time it takes when the first bit of new data packet arrives, till the recovered clock locks to this data packet, is said to be lock time. In our work, lock time is significantly affected by the buffer's load resistor and parasitic capacitances of the devices. In the previous work, because of having two buffers inside each DT-SH connected to the PI, it might increase parasitic effects and hence the time constant. It is worth mentioning that the time constant of the discussed circuit can be reduced by use of this technique, making lock time shorter. The configuration of the schematic diagram of DT-SH in Fig. 5(a) is purposefully designed in a specific way to be able to work with current-mode logic (CML) data. Thus the CML-to-CMOS data converter is not required in the primary stage of the system. To reject the track-mode and pass the hold-mode signals coming from sampling switches, transmission gates (TGs) are used. Shown in the Fig. 5(a), when the main transistor in the sampling switch block is in the sampling mode, TG which is controlled by input data goes off. Either two TGs in the left or the ones in the right of DT-SH configuration are not turned on at the same time, so that electrical short circuit at the TGs' output is not occurred. Parasitic capacitances of the transistors in sampling switches create C_H and no more capacitor is needed.

2.3 Flip-flop, Frequency Divider and De-multiplexer

The received burst data is sampled using a CML D flip-flop, consisting of master and slave latches. Fig. 6(a) shows the schematic diagram of the CML latch used in the proposed BM-CDR. The flip-flop is clocked by the recovered clock produced from the PI at the frequency of 5GHz. It is known that CML flip-flops consume more power than its CMOS counterparts. On the other hand, CML flip-flop is faster, has better performance at high speed circuits. Therefore CML flip-flop is utilized in this design. The CML latch shown in Fig. 6(a) comprises of two stages. The first stage, which is composed of differential transistors, forms a sampler and the second one, which is composed of cross-coupled pair transistors, forms a hold stage. These two different stages make different time constants. Both time constants must be carefully chosen to satisfy the setup time and hold time requirements of the D flip-flop [14].

The architecture of Fig. 2 consists of a 1-to-2 data demux which de-serializes retimed serial data into parallel. We wish to demultiplex the 5Gb/s data by means of the latches used in the flip-flop driven by a half-rate clock [15]. The divider circuit provides a 2.5GHz clock with the same phase as recovered clock. Fig. 6(b) illustrates the topology of the CML divide-by-two circuit to which the recovered clock is applied.

3 Simulation Results

The CDR/deserializer has been simulated in 0.18-μm CMOS technology with a 1.8-V supply. By applying a 5Gb/s pseudo-random binary sequence (PRBS) CML data of length 2^{10}-1 bits to the proposed PI-based BM-CDR, simulation results show the functionality of the system. Instantaneous phase locking is achieved as the recovered clock locks to the input data in the first unit interval (UI). The output of the clock recovery unit is buffered to be able to drive both the decision circuit and the frequency divider of next stage. Because of the delay in DT-SHs and PI circuitry and also delay added due to the buffers which are used after clock re-

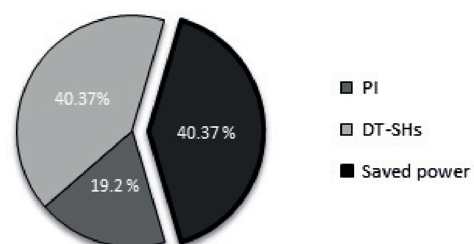

Figure 7: Power dissipation in clock recovery unit (dark area denotes saved power in this work in comparison with the work in [10])

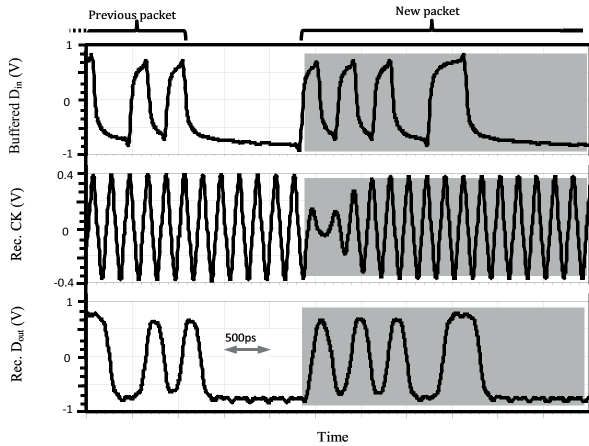

Figure 8a: Instantaneous phase locking in response to burst-mode data

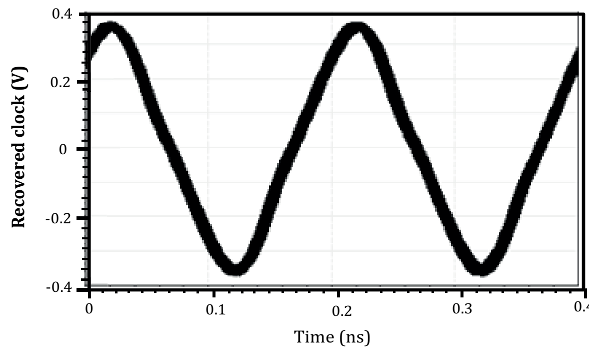

Figure 8b: Recovered clock in response to 2^{10}-1PRBS continuous-mode data

covery unit, a couple of buffer stages in the decision circuit path have been added to compensate the delay in the recovered clock path. Therefore optimum sampling has been achieved from the first bit of incoming data. Since the total power consumption in a ST-SH belongs to the power consumption in buffer, it has been approved that by sharing buffer, power dissipation in the proposed DT-SH has become half. According to the simulation results, in case of employing non-shared buffer scenario, 4.26mW power is consumed in the clock recovery unit whereas in our work it was only

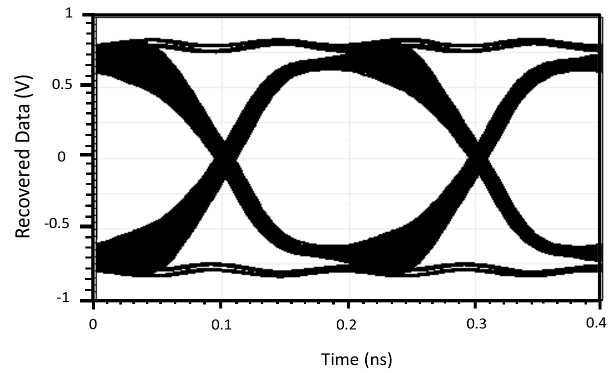

Figure 8c: Eye diagram of retimed data at 5Gb/s in response to 2^{10}-1PRBS continuous-mode data

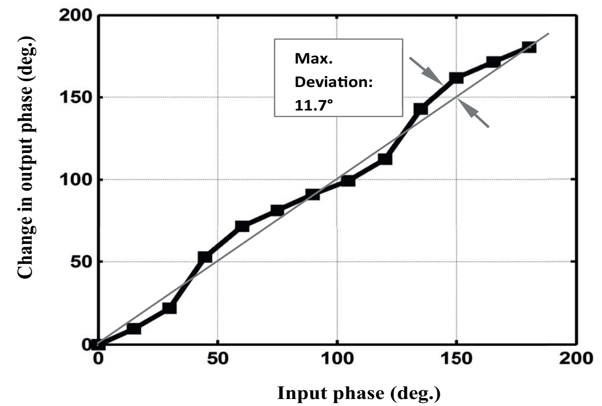

Figure 9: Simulated characteristics of the PI

2.54mW. For simplicity the power consumption of each building block in the clock recovery unit is depicted in Fig. 7. It is now observed that the power consumption of the PI is only a small part of the clock recovery unit and a great percentage of total power is dissipated in DT-SHs. Making use of the shared-buffer technique has saved more than 40% power of the clock recovery unit in comparison to utilizing two buffers for each DT-SH (non-shared buffer design used in the work in [10]). Fig. 8(a) illustrates instantaneous phase locking of recovered clock to the incoming burst-mode data. Note the phase locking in the presence of a new data packet with a different phase, which is highlighted in the dia-

Table 1: BM-CDR performance summary and comparison with other works

Parameters	[4]*	[6] *	[7] *	[10] *	This work**
Supply voltage	1.5V	3.3V/1.8V	N/A	1.2V	1.8V
Process technology	90nm	250nm	130nm	65nm	180nm
Data rate (Gb/s)	20	10.3125	10.3125	1-6	5
Method	Injection Locking	GVCO	Oversampling	PI	PI
Phase locking time	1UI	1UI	N/A	1U	1UI
Power consumption	102mW (CDR core)	856mW	5.8W (entire Rx)	22mW (CDR core + demux)	29mW (CDR core + demux)

* Fabricated ** Simulated

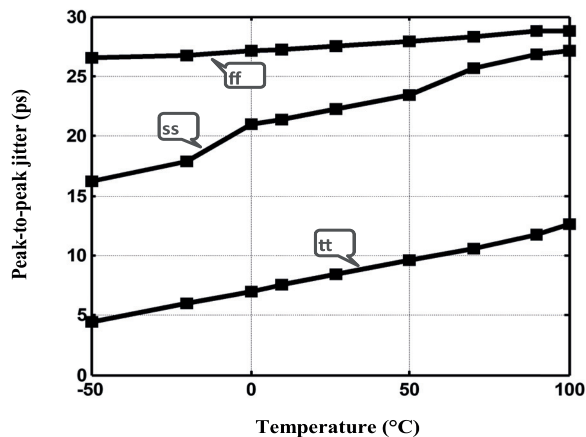

Figure 10: Peak-to-peak jitter of the recovered clock for process and temperature variations

gram. Fig. 8(b) shows the recovered clock in response to a continuous-mode PRBS data of length 2^{10}-1 bits. As shown in Fig. 8(c), recovered data with the eye opening of 1.2V is achieved. The simulated peak-to-peak jitter of recovered clock and data is 9ps and 14ps, respectively. A simulation for the PI characteristics has been performed and plotted in Fig. 9. The phase of input quadrature clocks has been shifted from 0° to 180°, and the result for recovered clock shows a maximum deviation of 11.7° from its ideal interpolation at 5GHz. Corner case simulation has also been performed and results for the recovered clock in *slow-slow* (SS) and *fast-fast* (FF) cases shows a peak-to-peak jitter of 22.5ps and 27.5ps, respectively. Fig. 10 shows the simulation results for peak-to-peak jitter of the recovered clock vs. process and temperature variations. According to simulation results, the proposed BM-

CDR circuit consumes 29mW power from a 1.8-V supply. The performance of the system and a comparison with other works is summarized in Table I. Although, the simulation results may not be comparable with the experimental results; however the concept of the proposed technique for power reduction is approved.

4 Discussion and Conclusions

The requirement for immediate-locking burst-mode CDR circuits at high data rates in passive optical networks is a challenging topic. This work presents a PI-based burst-mode clock and data recovery circuit dedicated to reduce the power consumption of clock recovery unit in high speed multi-access networks. The architecture benefits from the fact that the system is able to work with CML data, coming directly from post amplifier of the previous stage (LA); therefore designing a CML-to-CMOS data converter is not required. Moreover, since designing high-speed buffers is a challenging topic and it is power hungry, reducing the buffers used in DT-SH by a factor of 2, dramatically alleviated power consumption and speed limitations. By employing our technique in DT-SH block by sharing a buffer between two ST-SHs, we showed that approximately 40% reduction in power consumption in clock recovery unit is achieved. Results verify that the recovered clock locks to the incoming burst data within the first UI. Although by sharing the buffer, linear values at the DT-SH's output are observed, and the PI linearity is simulated with a maximum deviation of 11.7° from its ideal interpolation. The functionality of the system is verified in the presence of process and temperature variations. The proposed BM-CDR consumes 29mW power from a 1.8-V supply. The circuit retimes input jittered-data and obtains a p2p jitter of 14ps at 5Gb/s.

Acknowledgement

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Current-mode Quadrature Oscillator using CCCCTAs with Non-interactive Current Control for CO, FO and Amplitude

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Abstract: This paper presents a current-mode quadrature oscillator with amplitude controllability. The proposed circuit consists of two current controlled current conveyor transconductance amplifiers, two grounded capacitors and one grounded resistor. The condition of oscillation, frequency of oscillation and amplitude of output current can be independently controlled with electronics method via DC bias current. In addition, the proposed oscillator has high impedance of outputs ports which facilitates easy driving an external load without additional current buffers. It also uses all grounded passive elements which suitable for implementation in the integrated circuit. The theoretical results are verified by PSPICE simulation and experimental results that well conform to the theoretical anticipation.

Keywords: Current-mode; Quadrature Oscillator; Current Controlled Current Conveyor Transconductance Amplifier; Grounded Elements

Kvadraturni oscilator v tokovnem načinu z uporabo CCCCTA z neinteraktivno kontrolo toka za CO, FO in amplitudo

Izvleček: Članek opisuje tokovno krmiljen kvadraturni oscillator z nadzorom amplitude. Predlagano vezje je sestavljeno iz dveh tokovno krmiljenih transkontuktančnih ojačevalnikov, dveh ozemljenih kondenzatorjev in ozemljenega upora. Frekvenca in amplituda oscilatorja je neodvisno nastavljiva preko vhodnega DC toka. Predlagan oscilator ima visoko izhodno impedanco, ki omogoča enostavno krmiljenje zunanjih bremen brez dodatnih virov. Zaradi ozemljenih pasivnih elementov je primerno za integrirana vezja. Teoretični izračuni so preverjeni v PSPICE in eksperimentalno potrjeni.

Ključne besede: tokovni način; kvadraturni oscillator; tokovno krmiljen transkonduktančni ojačevalnik; ozemljeni elementi

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1 Introduction

An oscillator which provides two sinusoidal signals with 90° phase difference, or well known as quadrature oscillator, has been continuously proposed since it plays an important role and has been widely applied in various applications such as communication, instrumentation, measurement and signal processing, etc [1-4]. Especially in communication systems, the sinusoidal oscillator is frequently used to generate the carrier signal for modulation system [5-6] such as AM, FM, ASK etc. Normally, the oscillator would generate the signal without amplitude controllability. So in some applications which need the exact amplitude, the amplifier circuit is required, causing the complicated circuit. Recently, the portable electronics devices which run on compact batteries have been necessary to reduce voltage power supply and power consumption. These requirements call for the development of current-mode circuit designs due to their potential advantages such as inherently wide bandwidth, higher slew-rate, greater linearity, wider dynamic range, simple circuitry and low power consumption [7-8].

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Several quadrature oscillators have been proposed in the literature [9-29]. A lot of them focus on the use of electronically adjustable active building blocks (ABB), such as, current controlled current conveyor (CCCII), current conveyor transconductance amplifier (CCTA), current controlled current conveyor transconductance amplifier (CCCCTA), differential voltage current conveyor transconductance amplifier (DVCCTA), current follower transconductance amplifier (CFTA) and current controlled current follower transconductance amplifier (CCCFTA). Some parameters (such as transconductance or parasitic resistance) of these ABBs are tuned by external current or voltage which is easy to control by microcontroller or microcomputer. The review of these oscillator topologies is as follows. The oscillators in Ref. [9-29] use grounded capacitor which is attractive for integrated circuit implementation. In Ref. [9-10], the electronic tuning of frequency of oscillation (FO) by adjusted parasitic resistance R_x is achieved. However, the condition of oscillation (CO) is controlled by current gain control, which is not so common [30-31]. CCCIIs based sinusoidal oscillator was introduced in [11]. The magnitude of sinusoidal output current can be electronically adjusted as well as the frequency of oscillation, but this oscillator circuit employs three CCCIIs and the control of CO is done by adjusting the value of capacitor which is unconventional. The proposed oscillators in [12-14] exhibit advantages in electronic tuning of the FO by the transconductance g_m, but the CO is controlled by change the value of passive resistor, which cause addition complication [30-31]. Although electronic adjusting can be used by digital potentiometer, but it is difficult for implementation [31]. The FO in [12, 19-24] is electronically adjusted by the transconductance gain g_m. Some oscillators in [17, 25], the FO and CO cannot independently controlled. The circuits in [18-23, 26-27] can be electronically adjusted the CO and FO. The magnitude of sinusoidal output signal in [28] can be electronically adjusted but the FO and CO cannot be electronically adjusted. However, the amplitude of output signal in [9-10, 12-27, 29] cannot be electronically controlled. The comparison of proposed oscillator with previous work is shown in Table 1.

Table 1: The comparison of proposed oscillator with previous oscillators

Ref.	ABB	No. of ABB	No. of R+C	Electronic tune for both CO and FO	Independent tune of CO and FO	Output current with high impedance	Amplitude controllability
[9]	CG-CCCII	2	0+2	✓	✓	✓	x
[10]	CG-CCCII	2	0+2	✓	✓	x	x
[11]	CCCII	3	0+2	✓	x	✓	✓
[12]	CCTA	1	1+2	x	✓	x	x
[13]	CCTA	1	2+2	x	✓	✓	x
[14]	DVCCTA	1	2+2	x	✓	x	x
[15]	CCCCTA	1	0+2	x	✓	x	x
[16]	MO-CCCCTA	1	0+2	✓	x	✓	x
[17]	CG-CCTA	1	2+2	✓	x	x	x
[18]	CCTA	2	1+2	✓	x	✓	x
[19]	CCCCTA	2	0+2	✓	x	✓	x
[20]	CCCCTA	4	0+2	✓	✓	✓	x
[21]	MCDTA+ CFTA	2	0+2	✓	x	✓	x
[22]	CFTA	1	1+2	✓	x	✓	x
[23]	CCCFTA	2	0+2	✓	x	✓	x
[24]	ZC-CFTA	4	0+2	✓	✓	✓	x
[25]	CG-CFTA	2	0+2	✓	x	✓	x
[26]	CCCCT+ OTA	2	0+3	✓	x	✓	x
[27]	DO-CCCCTA	1	0+2	✓	x	✓	x
[28]	CDBA	2	3+2	x	x	✓	✓
[29]	DO-CCCCTA	1	2+2	✓	✓	✓	x
proposed circuit	CCCCTA	2	1+2	✓	✓	✓	✓

The purpose of this paper is to present the quadrature oscillator using CCCCTAs. The proposed circuit provides the following advantage features:

The current-output signal from high-impedance is easy to drive a load without using a buffering device [30-32]. The proposed circuit uses only grounded capacitors which are advantageous from the point of view of integrated circuit implementation [30-32].

The CO and FO can be electronically and independently controlled.

The amplitude of output current can be controlled via external bias current without effect of the CO and FO, which can provide the AM and ASK signal, widely used in communication systems [32].

Low active and passive sensitivities.

The workability of the proposed sinusoidal oscillator is confirmed via the PSPICE simulation and experiment.

2 Current Controlled Current Conveyor Transconductance Amplifier (CCCCTA)

Since the proposed circuit is based on CCCCTA [15], a brief review of CCCCTA is given in this section. It was modified from the first generation CCTA [8]. The characteristics of the ideal CCCCTA are represented by the following hybrid matrix:

$$\begin{bmatrix} I_y \\ V_x \\ I_{z,zc} \\ I_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & R_x & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_o \\ V_z \end{bmatrix} \quad (1)$$

For the CCCCTA implemented by a bipolar technology, the parasitic resistance R_x is given as

$$R_x = \frac{V_T}{2I_{B1}} \quad (2)$$

and transconductance g_m is given as

$$g_m = \frac{I_{B2}}{2V_T} \quad (3)$$

The circuit symbol and equivalent circuit of the CCCCTA are illustrated in Fig. 1(a) and (b), respectively

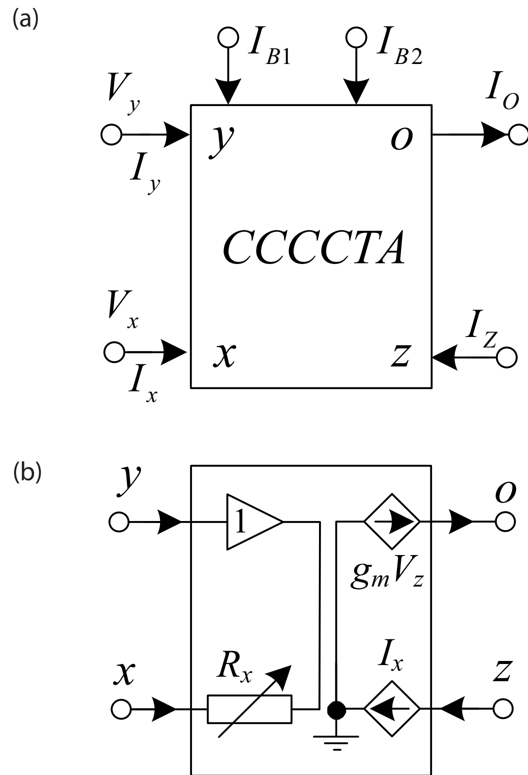


Figure 1: CCCCTA (a) schematic symbol (b) equivalent circuit

3 Proposed circuit configuration

The proposed quadrature oscillator is shown in Fig. 2. It consists of two CCCCTAs, two grounded capacitors and one grounded resistor. The quadrature output current ports are I_{O1}, I_{O2} and I_{O3} is the output current with amplitude controllability. The use of grounded passive element is advantageous from the point of view of integrated circuit implementation [30-32]. Moreover, it is found that the oscillator provides high output impedance which can directly drive a load without buffering devices [30-32]. Using (1) and doing routine circuit analysis, the system characteristic equation can be expressed as

$$s^2 + \left(\frac{1}{R_1} - \frac{1}{R_{x2}}\right)\frac{s}{C_1} + \frac{g_{m1}}{C_1C_2R_{x1}} = 0 \quad (4)$$

From (4), it can be seen that the proposed circuit can produce oscillations if the condition of oscillation is fulfilled

$$R_1 = R_{x2} \quad (5)$$

If the above condition of oscillation is satisfied, the circuit produces oscillation with frequency of

$$\omega_{osc} = \sqrt{\frac{g_{m1}}{C_1 C_2 R_{x1}}} \quad (6)$$

Substituting the parasitic resistance R_x and transconductance g_m as respectively shown in (2) and (3) into (5) and (6), the CO becomes

$$I_{B3} = \frac{V_T}{2R_1} \quad (7)$$

and the FO is obtained as

$$f_{osc} = \frac{1}{2\pi V_T}\sqrt{\frac{I_{B1} I_{B2}}{C_1 C_2}} \quad (8)$$

It is found that the CO can be electronically controlled through DC bias current I_{B3} without effect of the FO. Also, the FO can be electronically tuned through I_{B1} or I_{B2} without effect of the CO. Consequently, this circuit enables non-interactive current control for both the CO and the FO.

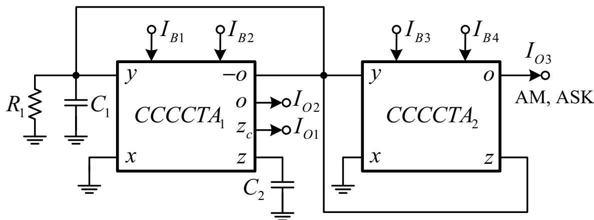


Figure 2: The proposed quadrature oscillator using CCCCTAs

The ratio between output current I_{O2} and I_{O1} is

$$\frac{I_{O2}}{I_{O1}} = \frac{g_{m1}}{C_2 s} \quad (9)$$

It is found that the phase difference of output current I_{O1} and I_{O2} is 90 °. However at oscillation state ($\omega=\omega_{osc}$), the relationship of I_{O2} and I_{O1} in (9) is changed to

$$\left.\frac{I_{O2}}{I_{O1}}\right|_{\omega=\omega_{osc}} = \sqrt{\frac{C_1 g_{m1} R_{x1}}{C_2}} \quad (10)$$

Substituting the parasitic resistance R_x and transconductance g_m as respectively shown in (2) and (3) into (10), the ratio between output current I_{O2} and I_{O1} becomes

$$\left.\frac{I_{O2}}{I_{O1}}\right|_{\omega=\omega_{osc}} = \sqrt{\frac{C_1 I_{B2}}{4C_2 I_{B1}}} \quad (11)$$

It is obvious seen from (11) that the tune of I_{B2} or I_{B1} for controlling the frequency of oscillation causes change of amplitude I_{O2} and I_{O1} during tuning process. When amplitude of I_{O2} or I_{O1} increases the voltage at notes V_{y1} and V_{z1} also increase too. This phenomenon will increase the THD if amplitude reaches high levels due to the limits of dynamical range of CCCCTA. However, this can be alleviated by simultaneously changing I_{B2} and I_{B1} ($I_{B2}=I_{B1}$).

Furthermore, the output current I_{03} can be obtained as

$$I_{O3} = g_{m2} V_{z2} \quad (12)$$

From (12), the voltage V_{z2} is the sinusoidal signal. It means that the amplitude of sinusoidal signal I_{O3} can

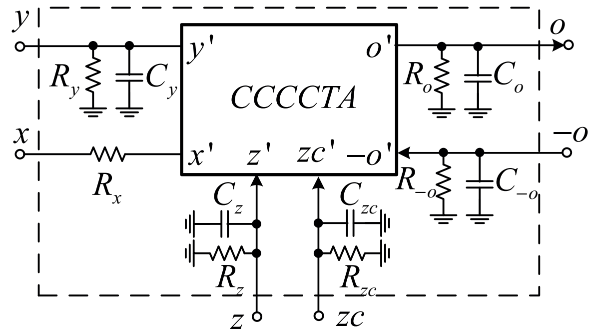


Figure 3: The non-ideal CCCCTA

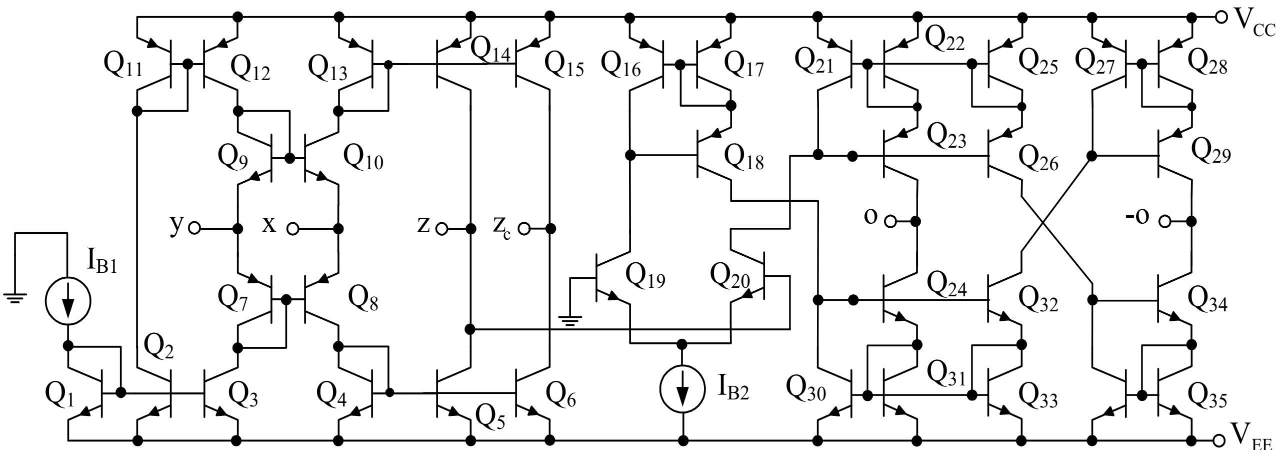


Figure 4: The internal construction of CCCCTA

be electronically controlled by I_{B4} without effect of CO and FO. Therefore, if I_{B4} is a modulating signal, AM and ASK signal can be obtained at I_{O3}. In addition, the output current I_{O3} port is high-impedance. It is easy to drive a load without using a buffering device.

The sensitivities of active and passive for frequency of oscillation are low as shown in (13)

$$S_{g_{m1}}^{\omega_{osc}} = \frac{1}{2},\ S_{C_1,C_2,R_{x1}}^{\omega_{osc}} = -\frac{1}{2} \tag{13}$$

4 Non-ideal Analysis

Considering to voltage and current tracking errors, the CCCCTA properties can be written as

$$\begin{bmatrix} I_y \\ V_x \\ I_z \\ I_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ \gamma & R_x & 0 & 0 \\ 0 & \alpha & 0 & 0 \\ 0 & 0 & 0 & \pm\beta g_m \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_o \\ V_z \end{bmatrix} \tag{14}$$

Where $\gamma = \gamma_o/(1+s/\omega_\gamma)$, $\alpha = \alpha_o/(1+s/\omega_\alpha)$ and $\beta = \beta_o/(1+s/\omega_\beta)$. They are frequency-dependence of non-ideal of voltage and current gains, respectively. ω_γ, ω_α and ω_β are dc non-ideal bandwidths with ideality equal to infinity. γ_o, α_0 and β_o are dc non-ideal gains with ideality equal to unity. Moreover, the effect of parasitic resistances and capacitances are also taken into account. The C_y, C_z and C_o are parasitic capacitors at y, z and o terminals, respectively, with ideality equal to zero. The parasitic resistors R_y, R_z, R_o at y, z and o terminals with ideality equal to infinity. These parasitic components of the CCCCTA are shown in Fig. 3.

Re-analysis the circuit in Fig. 2, the characteristic equation is modified to

$$s^2 + s\left(\frac{G_{z1}}{C_2^*} + \frac{G_1^*}{C_1^*} - \frac{G_{x2}}{C_1^*}\right) + \frac{\beta_1\gamma_1\alpha_1 G_{x1} g_{m1} + G_1^* G_{z1} - G_{x2} G_{z1}}{C_1^* C_2^*} = 0 \tag{15}$$

Then, the CO and FO of the proposed circuit become

$$\frac{G_{z1}}{C_2^*} + \frac{G_1^*}{C_1^*} - \frac{G_{x2}}{C_1^*} = 0 \tag{16}$$

And

$$\omega_{osc} = \sqrt{\frac{\beta_1\gamma_1\alpha_1 G_{x1} g_{m1} + G_1^* G_{z1} - G_{x2} G_{z1}}{C_1^* C_2^*}} \tag{17}$$

Where $C_1^* = C_1 + C_{y1} + C_{y2} + C_{-o1} + C_{z2}$, $C_2^* = C_2 + C_{z1}$
$G_1^* = G_{y1} + G_{y2} + G_{-o1} + G_{z2} + G_{R1}$, $G_1 = \frac{1}{R_1}$, $G_{x1} = \frac{1}{R_{x1}}$
$G_{x2} = \frac{1}{R_{x2}}$, $G_{y1} = \frac{1}{R_{y1}}$, $G_{y2} = \frac{1}{R_{y2}}$, $G_{-o1} = \frac{1}{R_{-o1}}$,
$G_{z1} = \frac{1}{R_{z1}}$ and $G_{z2} = \frac{1}{R_{z2}}$.

5 Simulation Results

To prove the performances of the proposed oscillator, the PSPICE simulation was performed for examination. The BJT technology was simulated by using the parameters of the PR200N and NR200N bipolar transistors of ALA400 transistor array from AT&T. Fig. 4 depicts the schematic description of the CCCCTA used in the simulations with ± 1.8 V power supplies.

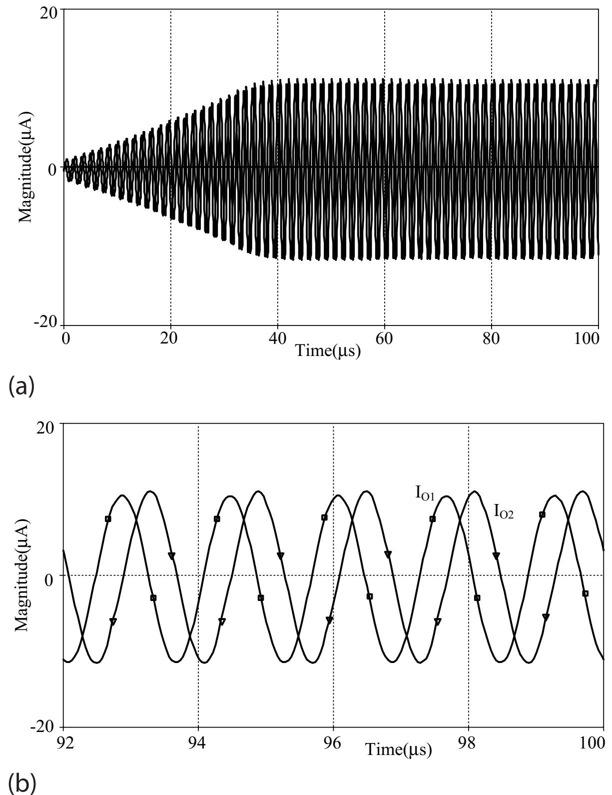


Figure 5: The waveforms of sinusoidal oscillator (a) transient state (b) steady state

The sinusoidal oscillator was designed with C_1 = 1 nF, C_2 = 0.47 nF, R_1 = 1 k Ω, I_{B1} = 58 µA, I_{B2} = 115 µA and I_{B4} = 10 µA. From (7), the bias current I_{B3} was set nearby $V_T/2R_1$ to start-up the oscillation, which is I_{B3} = 10 µA. The power dissipation of this case is about 4.26 mW. This yields oscillation frequency of 630 kHz. Fig. 5 (a)

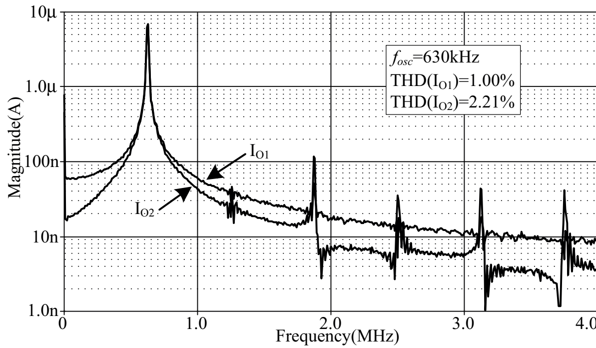


Figure 6: The frequency spectrum of signal in Fig. 5.

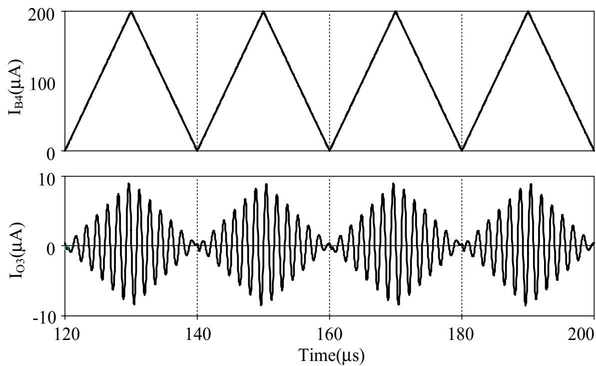


Figure 7: The results of operation of AM

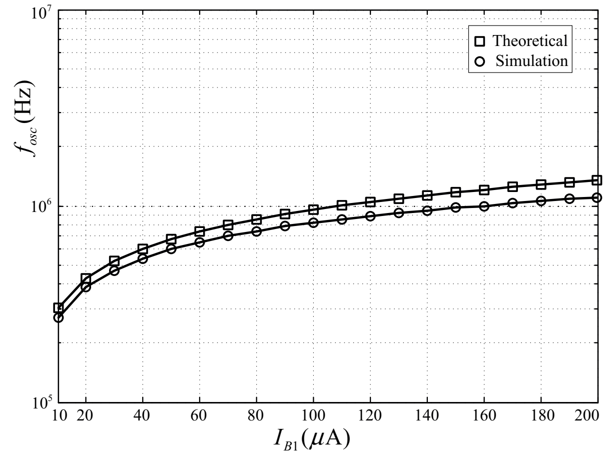
and (b) show simulated output waveforms in transient and steady state, respectively. Fig. 6 shows simulated output spectrum, where the total harmonic distortions (THD) of output current I_{O1} and I_{O2} are about 1.00 % and 2.21 %, respectively.

The simulated result of the proposed circuit serving as an AM generator at I_{O3} is shown in Fig. 7, where I_{B4} was triangular signal with a 50 kHz frequency. It is confirmed that the proposed circuit can easily generate AM signal.

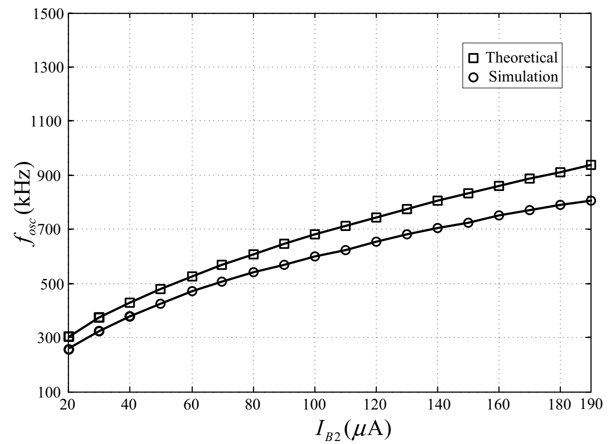
The electronically adjustment of the FO can be demonstrated in Fig. 8 (a), while keeping I_{B2} = 115 μA and tuning bias current I_{B1} from 10 μA-200 μA. Similarity, Fig. 8 (b) shows the simulation of FO, which remains I_{B1} = 58 μA and adjusts I_{B2} from 20 μA-190 μA. It is clear seen that the simulation results are in accordance with the theoretical analysis as shown in equation (8). The error of the oscillation frequency stems from the non-ideal parameters as depicted in the Section IV. The amplitude of output current I_{O1} can be exhibited in Fig. 9, when tuning bias current I_{B1} and I_{B2}.

6 Experimental Results

To prove the theoretical analysis of proposed oscillator, the experimental results are shown in this section. The



(a)



(b)

Figure 8: The frequency of oscillation against bias current (a) I_{B1} (b) I_{B2}

circuit for experiment is illustrated in Fig. 10. It was constructed by using commercial ICs, which are AD844A [33] and LM13700N [34]. The values of components in experimental circuit were chosen as C_1 = 1 nF, C_2 = 0.47 nF, R_1 = 1.1 kΩ, R_{L3} = 1 kΩ (R_{L3} was used to measure the output current by an oscilloscope). The intrinsic resistances R_{x1} and R_{x2} are realized by OTA-based grounded resistance simulator with following value

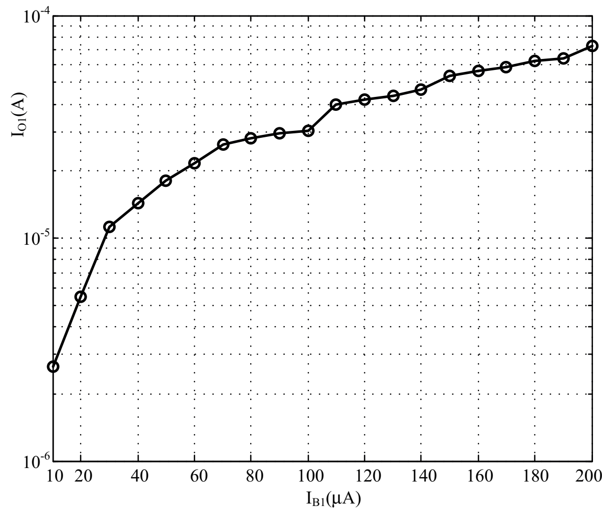
$$R_x = \frac{2V_T}{I_B} \tag{16}$$

From (16) the CO and FO can be rewritten as

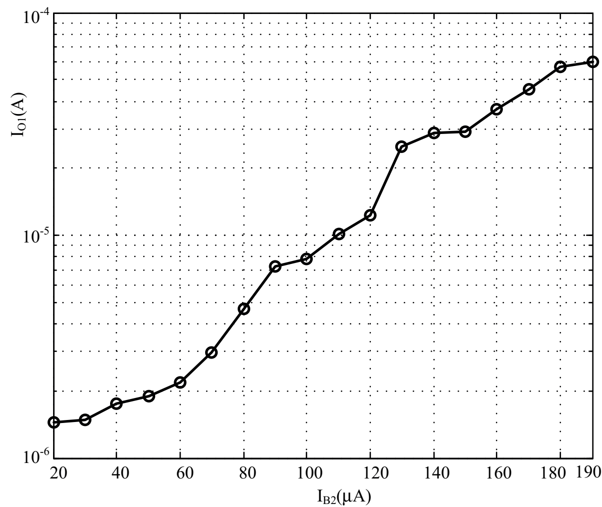
$$I_{B3} = \frac{2V_T}{R_1} \tag{17}$$

And

$$f_{osc} = \frac{1}{4\pi V_T}\sqrt{\frac{I_{B1}I_{B2}}{C_1 C_2}} \tag{18}$$



(a)



(b)

Figure 9: The amplitude of I_{O1} against bias current (a) I_{B1} (b) I_{B2}

The relationship of V_{o2} and V_{o1} is as follows:

$$V_{O2} = \frac{I_{B1} V_{O1}}{2 V_T s C_2} \tag{19}$$

Similarly, the amplitude of output voltage V_{O3} is shown in (20)

$$V_{O3} = \frac{I_{B4} R_{L3} V_{O1}}{2 V_T} \tag{20}$$

The circuit in Fig. 10 was biased with I_{B1} = 60 µA, I_{B2} = 115 µA, I_{B3} = 56 µA, I_{B4} = 60 µA and ±5 V power supplies. An oscilloscope Rigol model DS1046B [35] was used to measure the output waveforms. The waveform of output signals are shown in Fig. 11 (a) where the FO is about 321 kHz. The calculated value of FO from (18) is about 370.84 kHz. The deviation of FO is suffered from parasitic elements of the CCII, OTA and parasitic element of oscilloscope. Moreover, the parasitic influences of the CCII and OTA are shown in Table 2 and 3, respectively. Fig. 11 (b) exhibits the signals of V_{O1} and V_{O2}, which are the phase difference of 90° Furthermore, the frequency spectrum of output signals by use signal analyzer Agilent Technologies model N9000A [36] shown in Fig. 12, that is the FO is about 320.6 kHz. The parameters in Fig. 12 can be calculated the THD of V_{O1}, V_{O2} and V_{O3} are about 1.73 %, 1.53 % and 1.31 %, respectively. These THD (V_{O1}, V_{O2} and V_{O3}) are close to the simulation, which are about 1.50 %, 1. 27 % and 2.17 %, respectively.

To generate the AM signal, I_{B4} is feed as triangular waveform with 25 kHz of frequency. The voltage of current converter in Fig. 13 is used for this case. Fig. 14 shows the AM signal. It is clearly seen that this result confirms the theoretical analysis as shown in (20).

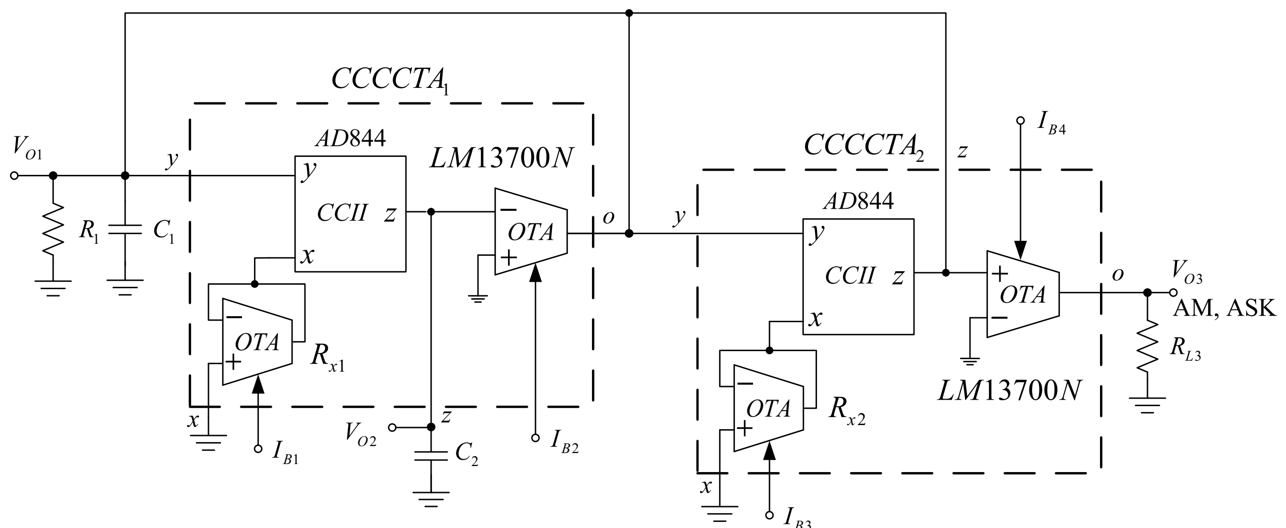


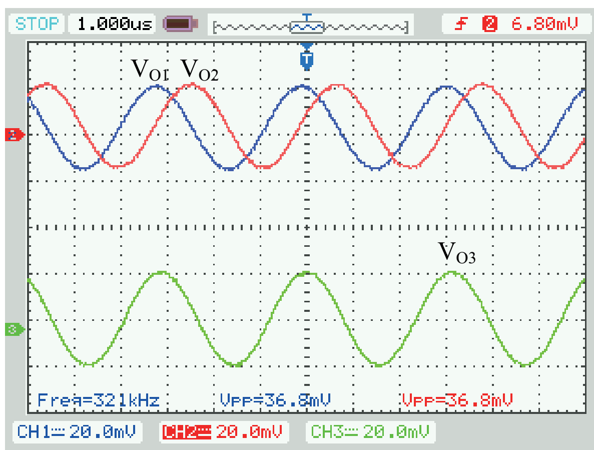
Figure 10: The oscillator circuit for experimental test

Table 2: The parasitic influences of CCII (AD844A) [33]

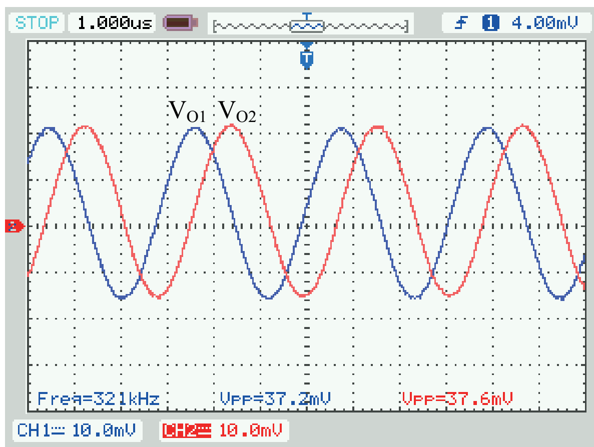
Port	Resistance	Capacitance
y	7 MΩ	2 pF
x	6 5Ω	2 pF
z	3 MΩ	4.5 pF

Table 3: The parasitic influences of OTA (LM13700N) [34]

Port	Resistance	Capacitance
Input	100 kΩ(I_B=100 μA)	5.2 pF
output	11 MΩ(I_B=100 μA)	4.6 pF



(a)



(b)

Figure 11: (a) The waveform of output signals (V_{O1}, V_{O2} and V_{O3}), (b) The waveform between V_{O1} and V_{O2}

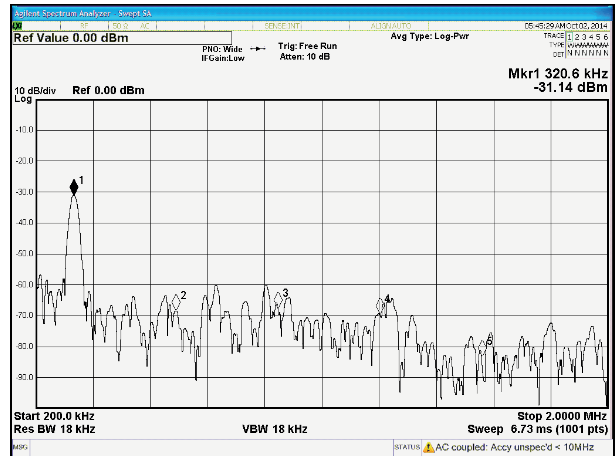


Figure 12: The spectrum of output signal

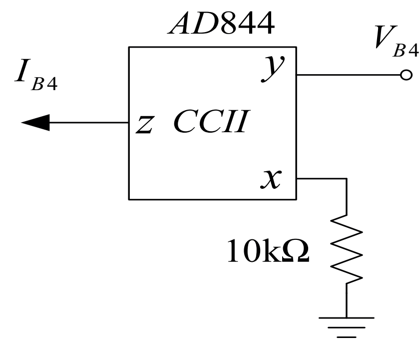


Figure 13: The V to I converter circuit

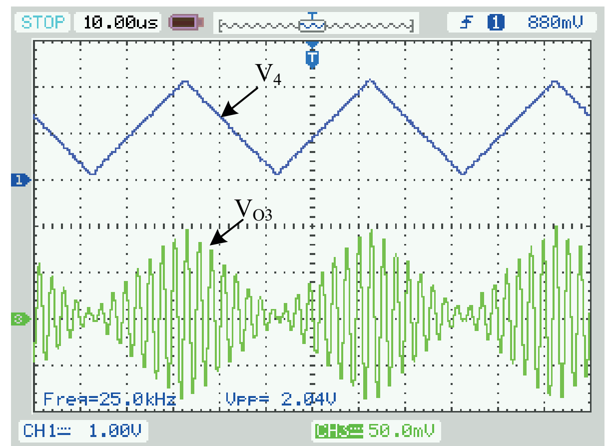


Figure 14: The waveform of AM signal

7 Conclusion

Current-mode quadrature oscillator using CCCCTAs and grounded elements has been presented. The proposed circuit consists of two CCCCTAs, two grounded capacitors and one grounded resistor. The condition and frequency of oscillation are independently adjusted by input bias current of CCCCTAs. Due to high-output impedances, it enables easy driving load without external current buffer. In addition, the amplitude of sinusoidal output signal can be electronically tuned. Moreover, it can provide the AM/ASK signals that are widely used in communication systems [32]. The PSpice simulation and experimental results well conform to the theoretical anticipation.

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Relative appraisal of Ultra-Thin Body MOSFETs: An analytical modeling including hot carrier induced degradation

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Abstract: This paper focuses on the physics and modeling of nanoscale ultra-thin body (UTB) single gate (SG) and double-gate (DG) Metal Oxide Field-Effect Transistors (MOSFETs). An analytical modeling for surface potential and threshold voltage of Fully Depleted (FD) DG-MOSFET is proposed by solving the 2-D Poisson's equation. The degradation due to the hot carrier effect, is investigated in short-channel devices. The parabolic potential approximation is utilized to solve 2D Poisson's equation in the channel region. The developed surface potential model includes the effect of both positive as well as negative interface charges. The calculated minimum surface potential is used to develop the threshold voltage model. Based on the model, the interdependence of the device parameters, such as the silicon film thickness (t_{Si}), oxide thickness (t_{ox}), channel length (L) are investigated in this paper. A conventional enhancement type n-MOSFET has been studied by developing an analytical model and checking its validity with numerical simulator Sentaurus, by Synopsis Inc.

Keywords: Ultra-Thin Body (UTB) MOSFET; Surface Potential; Threshold Voltage; Short Channel Effects (SCEs); hot carriers; trap charge

Relativna ocean ultra tankih MOSFET: Analitično modeliranje z upoštevanjem degradacije zaradi vročih nosilcev

Izvleček: Članek se osredotoča na modeliranje in delovanje ultra tankih eno- (SG) ali dvo-vratnih (DG) MOSFET tranzistorjev. Na osnovi reševanja 2D Poissonove enačbe je opravljeno analitično modeliranje površinskega potenciala in pragovne napetosti popolnoma osiromašenega DG_MOSFET tranzistorja. Vpliv degradacije zaradi vročih nosilcev je obravnavan na elementih s kratkimi kanali. Za reševanje Poissonove enačbe je uporabljena parabolična aproksimacija potenciala, ki upošteva tako pozitivne, kakor tudi negativne naboje. Minimalen površinski potencial je uporabljen za izračun pragovne napetosti. Obravnavana je povezanost parametrov, kot je debelina oksida, dolžina kanala in debelina silicijeve plasti. N-MOSFET tranzistor je bil simuliran z numeričnim simulatorjem Sentaurus

Ključne besede: ultra tanki (UTB) MOSFET; površinski potencial; pragovna napetost; vpliv kratkih kanalov; vroči nosilci; naboj pasti

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1 Introduction

CMOS devices come to nanoscale regime to acquire higher density and performance and lower power consumption. The inauspicious effects cause threshold voltage variation with higher leakage current in short devices known as short channel effects (SCEs). Due to these SCEs the conventional scaling comes to an end, but to maintain the Moore's law research going towards inventions of novel devices[1–4].

The predictions of International Technology Roadmap for Semiconductors (ITRS) are followed by the device designers to propose various novel device structures and process parameter variations [5]. Non classical silicon MOS structures, such as FinFETs, are replacing the conventional bulk MOS devices because of their capability to attain higher speeds and reduced short channel effects (SCEs) with the added advantage to design highly integrated CMOS circuits[6–9].

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For the modern short channel devices, the electric field under the gate oxide can no longer be treated in a single direction. In addition, the velocity of the carriers drifting between the channel and the drain saturates. This result in reduction in electron and hole mobility and thus an increase in effective sheet resistance [10]. The mobility enhancement can be possible through concepts like undoped channel and strained channel etc. [11], [12].

Further the generated hot carriers due to higher electric field may also be trapped in the oxide region of MOSFETs, leading to interface-trap buildup and the trapping of carriers in the oxide. Thus, trapped charges in the oxide region of MOSFETs change the potential profile of the channel and have adverse effects like shifting the threshold voltage. They may compromise operation of the device by generating charged defects in the oxide layer, and by degrading the oxide and the Si-SiO_2 interface. These effects constitute a reliability problem. Hot carriers also generate unwanted current components. Hence, analysis of hot carriers becomes one of the most crucial tasks [13],[14].

This paper presents an analytical model of surface potential, electric field and threshold voltage for short-channel Ultra-Thin Body (UTB) symmetrical Double-Gate (DG) MOSFETs including the effects of the interface charges. The parabolic potential approximation method is utilized while solving the two-dimensional (2D) Poisson's equations along with the assumption that the interface charge distribution is uniform along the channel [3], [15], [16]. The simulation results from Sentaurus are utilized to verify the obtained model.

2 Device structure

The schematic diagram of the ultra-thin body (UTB) single gate (SG) and double-gate (DG) MOSFET structures are used for modeling and simulation as shown in Fig. 1. The device has uniformly doped source–drain with doping concentration of $N_D = 1\times 10^{20}$ cm^{-3}. The channel is kept lightly doped with doping concentration of $N_A = 1\times 10^{16}$ cm^{-3}. The gate oxide thickness, buried oxide thickness and the silicon are $t_{ox} = 2$ nm $t_b = 50$ nm and $t_{Si} = 10$ nm, respectively. Damaged region due to the interface oxide traps charges (N_F) is shown in Fig. 1 with black line and labeled as distance *L*2.

The gate length (*L*=*L*1+*L*2) is divided into two parts to identify the damaged length *L*2. The work function of the gate material is: ϕ_{M1} = 4.6 eV (e.g., Mo). The simulation is carried out by the device simulator Sentaurus, a 2-D numerical simulator from Synopsis Inc. [17]. To

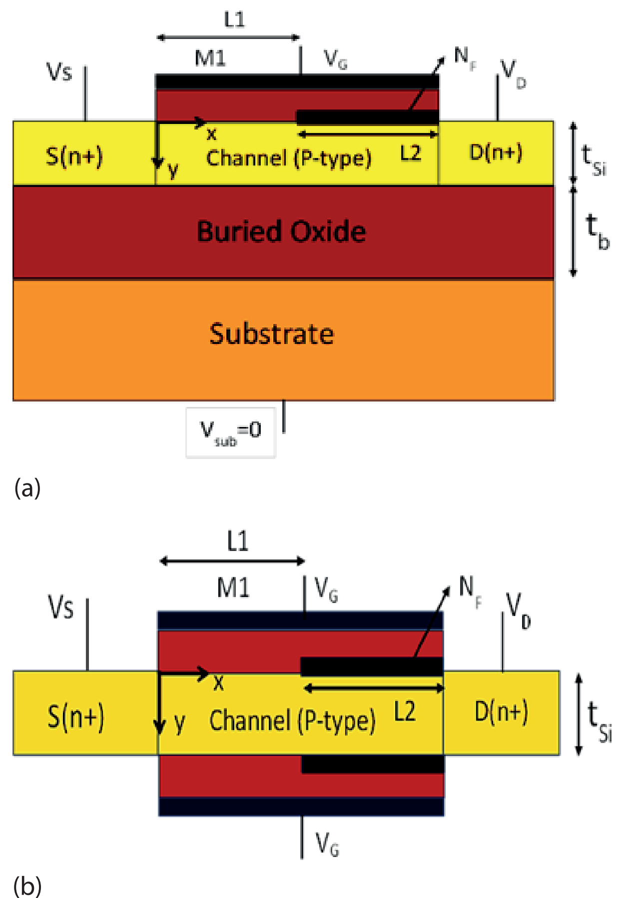


Figure 1: Schematic Structure of UTB (a) Single Gate and (b) Double Gate, Fully Depleted Silicon on Insulator MOSFET with Damaged Region

study the surface potential along the channel we have taken the cutline at the surface of the channel and across the thickness of channel of the device. To obtain accurate results for MOSFET simulation we need to account for the mobility degradation that occurs inside inversion layers. The drift-diffusion model which is the default carrier transport model in Sentaurus device is applied. The basic mobility model is used, that takes into account the effect of doping dependence, high-field saturation (velocity saturation), and transverse field dependence. The impact ionization effects are ignored. The silicon band gap narrowing model that determines the intrinsic carrier concentration is also included in simulation. The solution of the device equations are done self-consistently, on the discrete mesh, in an iterative fashion. For each iteration, an error is calculated and device attempts to converge on a solution that has an acceptably small error. The Poisson equation, continuity equations, and the different thermal and energy equations are included in simulation. [17]. All the structure junctions assumed as abrupt, and the biasing conditions considered at room temperature in the simulation.

3 Analytical Model Formulation

3.1 Surface Potential Formulation

Flat band voltage (front channel)

$$(V_{FB,f})_{si} = \phi_M - \phi_{si} \quad (1)$$

where $\phi_{f-Si} = V_T \ln(N_a/n_i)$, $\phi_{Si} = \frac{\chi_{si}}{q} + \frac{E_{g,Si}}{2q} + \phi_{f-Si}$

Back channel flat band voltage (back channel)

$$(V_{FB,b})_{si} = \phi_{sub} - \phi_{si} \quad (2)$$

where $\phi_{sub} = \frac{\chi_{si}}{q} + \frac{E_{g,Si}}{2q} + \phi_{f-sub}$, $\phi_{f-sub} = V_T \ln(N_{sub}/n_i)$

Built in voltage across source-body and drain body junction

$$V_{bi,Si} = \frac{E_{g,Si}}{2q} + \phi_{f-Si} \quad (3)$$

Considering the effect of oxide charges in the Si-SiO_2 interface, 2-D Poisson's equation for the potential distribution in the silicon regions can be written as [18]:

$$\frac{\partial^2 \phi_1(x,y)}{\partial x^2} + \frac{\partial^2 \phi_1(x,y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{si}} \text{ for } 0 \le x \le L_1, 0 \le y \le t_{Si} \quad (4)$$

$$\frac{\partial^2 \phi_2(x,y)}{\partial x^2} + \frac{\partial^2 \phi_2(x,y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{si}} \text{ for } L_1 \le x \le L, 0 \le y \le t_{Si} \quad (5)$$

The potential profile in the vertical direction can be approximated by a parabolic function

$$\varphi_1(x,y) = \phi_{s1}(x) + a_{11}(x)y + a_{12}(x)y^2 \text{ for } 0 \le x \le L_1, 0 \le y \le t_{Si} \quad (6)$$

$$\varphi_2(x,y) = \phi_{s2}(x) + a_{12}(x)y + a_{22}(x)y^2 \text{ for } L_1 \le x \le L, 0 \le y \le t_{Si} \quad (7)$$

Poisson's equation can be solved by following the boundary condition

1. Electric flux(displacement) at the gate oxide/strained Si film interface is continuous

$$\left.\frac{d\varphi_1(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s1}(x) - V'_{GS1}}{t_f} \quad (8)$$

$$\left.\frac{d\varphi_2(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s2}(x) - V'_{GS2}}{t_f} \quad (9)$$

where $V'_{GS1} = V_{GS} - (V_{FB1,f})_{si}$, $V'_{GS2} = V_{GS} - (V_{FB2,f})_{si}$

and the effect of trapped charges are to be considered as

$$(V_{FB1,f})_{si} = \phi_M - \phi_{si}, \; (V_{FB2,f})_{si} = \phi_M - \phi_{si} - \frac{qN_f}{C_{ox}}$$

2. Electric field at the interface of the buried oxide and the back channel is continuous

$$\left.\frac{d\varphi_1(x,y)}{dy}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{-\phi_B(x) + V'_{SUB}}{t_b} \quad (10)$$

$$\left.\frac{d\varphi_2(x,y)}{dy}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{-\phi_B(x) + V'_{SUB}}{t_b} \quad (11)$$

Where $V'_{SUB} = V_{SUB} - (V_{FB,b})_{si}$

3. Electric flux (displacement) and the electric potential at the trapped charged interface is continuous

$$\left.\frac{d\varphi_1(x,y)}{dx}\right|_{x=L_1} = \left.\frac{d\varphi_2(x,y)}{dx}\right|_{x=L_1} \quad (12)$$

$$\phi_1(L_1,0) = \phi_2(L_1,0) \quad (13)$$

4. The surface potential at the source end is

$$\phi_1(0,0) = \phi_{s1}(0) = V_{bi,si} \quad (14)$$

5. The surface potential at the drain end is

$$\phi_2(L,0) = \phi_{s2}(L) = V_{bi,si} + V_{DS} \quad (15)$$

Using the boundary conditions (8)-(11) we obtain coefficients and obtain the expressions for $\phi_1(x,y)$ and $\phi_2(x,y)$. Substituting $\phi_1(x,y)$ and $\phi_2(x,y)$ into (4) and (5) respectively and subsisting y=0 we obtain

$$\frac{d^2\phi_{s1}(x)}{dx^2} - \alpha\phi_{s1}(x) = \beta_1 \quad (16)$$

$$\frac{d^2\phi_{s2}(x)}{dx^2} - \alpha\phi_{s2}(x) = \beta_2 \quad (17)$$

where $\alpha = \frac{2(C_f C_{Si} + C_f C_b + C_b C_{si})}{t_{si}^2 C_{si}(2C_{si} + C_b)}$,

$$\beta_1 = \frac{qN_A}{\varepsilon_{si}} - 2V'_{GS1} \frac{C_f(C_{si} + C_b)}{t_{si}^2 C_{si}(2C_{si} + C_b)} - 2V'_{SUB} \frac{C_b}{t_{si}^2 C_{si}(2C_{si} + C_b)},$$

$$\beta_2 = \frac{qN_A}{\varepsilon_{si}} - 2V'_{GS2}\frac{C_f(C_{si}+C_b)}{t_{si}^2 C_{si}(2C_{si}+C_b)} - 2V'_{SUB}\frac{C_b}{t_{si}^2 C_{si}(2C_{si}+C_b)}$$

The solution for (16) and (17) are simple second order non-homogenous differential equation with constant coefficients which can be expressed as

$$\phi_{s1}(x) = A\exp(nx) + B\exp(-n*x) - \frac{\beta_1}{\alpha} \quad (18)$$

$$\phi_{s2}(x) = C\exp(n(x-L_1)) + D\exp(-n(x-L_1)) - \frac{\beta_2}{\alpha} \quad (19)$$

where $n = \sqrt{\alpha}$, $p_1 = \frac{\beta_1}{\alpha}$, $p_2 = \frac{\beta_2}{\alpha}$

Using the boundary condition (15)-(18) we solve for A, B, C, and D

$$A = ((V_{bi,si}(1-\exp(-nL)) + V_{DS} + (p_1 - p_2)\cosh(nL_2) + p_2 - p_1\exp(-nL))/(2\sinh(nL)) \quad (20)$$

$$B = ((V_{bi,si}(\exp(nL)-1) + p_1\exp(nL) - p_2 - V_{DS} - -(p_1 - p_2)\cosh(nL_2))/(2\sinh(nL)) \quad (21)$$

$$C = A\exp(nL_1) + \frac{p_2 - p_1}{2} \quad (22)$$

$$D = B\exp(-nL_1) + (\frac{p_2 - p_1}{2}) \quad (23)$$

3.2 Electric field formulation

Electric field horizontal component under metal gates M1/M2 can be expressed as

$$E_1(x) = An\exp(nx) - Bn\exp(-nx) \quad (24)$$

$$E_2(x) = Cn\exp(n(x-L_1)) - Dn\exp(-n(x-L_1)) \quad (25)$$

The minimum potential of front channel can be expressed as

$$x_{\min} = \frac{1}{2n}\ln(\frac{B}{A}) \quad (26)$$

$$\phi_{s,\min} = 2\sqrt{AB} - p_1 \quad (27)$$

3.3 Threshold Voltage Formulation

For strained-Si SOI MOSFET the threshold condition under the front gate is modified as

$$\phi_{s,\min} = \phi_{th} = 2\phi_{f,si} \quad (28)$$

$$V_{TH} = \frac{-\eta + \sqrt{\eta^2 - 4\sigma\xi}}{2\sigma} \quad (29)$$

Where $\gamma = \exp(-nL)$, $\sigma = \frac{1}{\gamma} + \gamma - 2 - \sinh^2(nL)$,

$$V_{bi1} = V_{bi,si}(1-\gamma) + V_{DS} - (u-v)\cosh(nL_2) - v + u\gamma$$

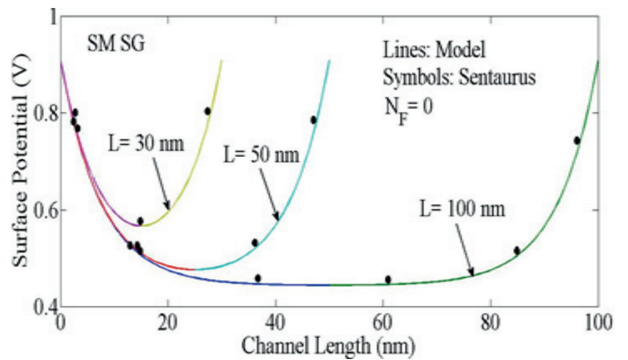
$$V_{bi1} = V_{bi,si}(1-\gamma) + V_{DS} - (u-v)\cosh(nL_2) - v + u\gamma$$

$$u = \frac{C_b}{C_f}V'_{SUB} - \frac{qN_A t_{si}}{C_f} - V_{FB1,si},\quad v = \frac{C_b}{C_f}V'_{SUB} - \frac{qN_A t_{si}}{C_f} - V_{FB2,si}$$

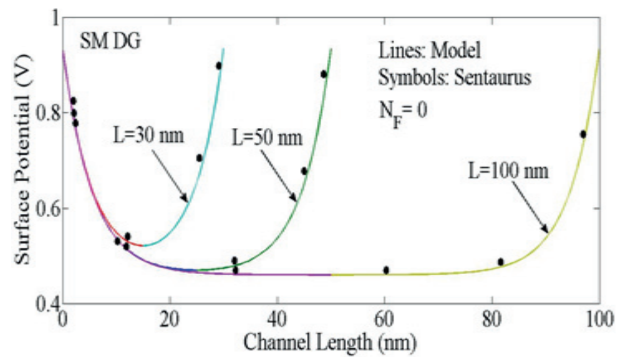
$$\xi = V_{bi1}V_{bi2} - \sinh^2(nL)(\phi_{th} - u)^2,$$

$$\eta = V_{bi1}(-\frac{1}{\gamma} + 1) + 2\sinh^2(nL)(\phi_{th} - u) - V_{bi2}(1-\gamma)$$

4 Results and Discussion



(a)



(b)

Figure 2: Variation of Surface potential for different channel length (a) Single Gate and (b) Double Gate. Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=10 nm, L=30, 50, 100 nm, t_{ox}=2 nm, V_{DS}=0 V and V_{GS}=0.1 V, N_F =0.

In this section, results obtained from theoretical models of the surface potential, electric field and threshold voltage are compared with the numerical simulation

results. A systematic comparison is made among UTB SG and DG SOI MOSFETs with considering the Si-SiO_2 interface trap charges. Fig. 2 demonstrates the surface potential curve for both SG and DG devices for different values of the channel lengths. From the figure, as channel length decreases, the height of potential barrier increases resulting undesirable short channel effects (SCEs). However, if one closely analyze the Fig. 2(a) and (b), it can be seen that the DG device is less susceptible for SCEs than SG. Fig. 3(a) shows an analogy of surface potential between SG and DG by maintaining all the parameters at constant value. Form the figure it can be clear that the DG device has more control over the channel as compare to SG device. This is because of two gates i.e. front and back gates in case of DG.

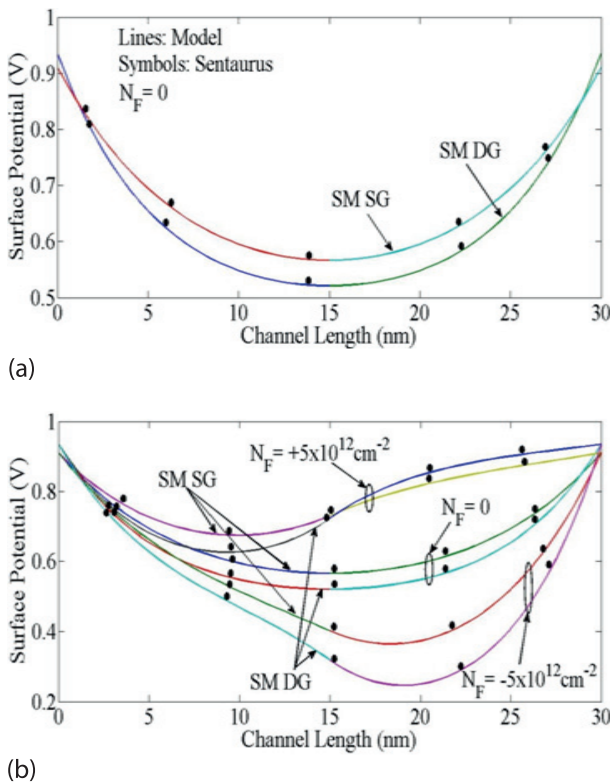


Figure 3: (a) Comparison of Variation of Surface potential for Single Gate and Double Gate, (b) Variation of Surface potential for different trapped charge for Single Gate and Double Gate. Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=10 nm, L=30 nm, t_{ox}=2 nm, V_{DS}=0 V and V_{GS}=0.1 V.

Fig. 3(b) shows the surface potential variation along the channel length for different amount and polarity of interface trapped charges in the oxide for SG and DG. From the figure, the minimum of the surface potential is at the channel center for device having N_F=0 and is moving towards the source and drain side, for positive and negative interface charge cases, respectively. Positive interface charge will cause higher SCEs on the device than its counterparts due to lower barrier height. However, device having negative interface charges will cause more drain induced barrier lowering (DIBL) as the minimum potential point shifts towards the drain side. So both positive and negative interface charges are undesirable for the device performance. It can be observed that DG device has higher barrier height with less prominent to interface trap charges.

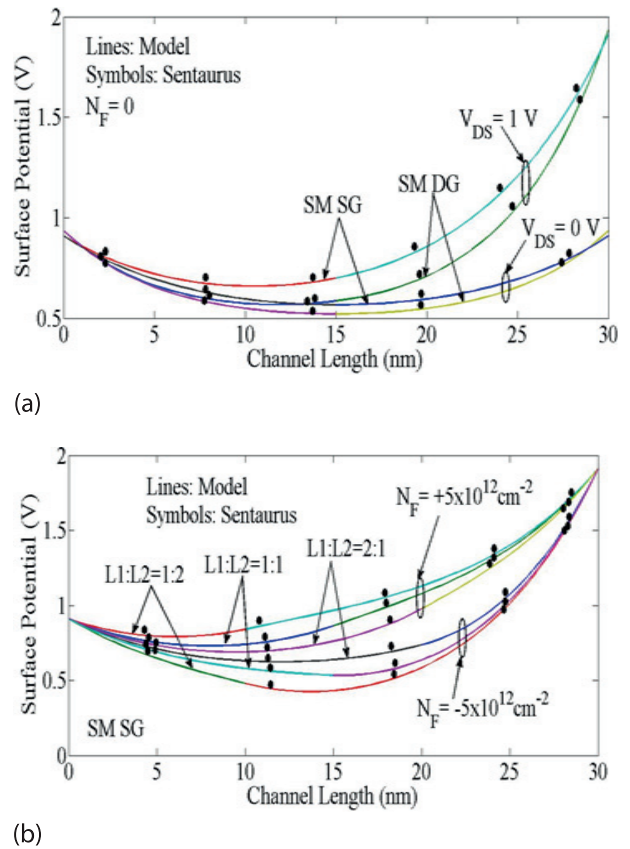


Figure 4: (a) Variation of Surface potential for different V_{DS} for both Single Gate and Double Gate. (b) Variation of Surface potential for different damaged region length ratios of Single Gate. Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=10 nm, t_{ox}=2 nm, L=30 nm and V_{GS}=0.1 V.

Fig. 4(a) demonstrates the surface potential curve along the channel length for various values of the drain voltage for both SG and DG. Because of the presence of two gates (DG), the variation of channel potential under the undamaged region with respect to drain voltage is much smaller than in SG. As a consequence, V_{DS} has only a small influence on drain current after saturation. Also due to two gates, the variation of channel potential minima with respect to drain voltage is much smaller than SG which minimizes the DIBL effect. Fig. 4(b) depicts the surface potential with the metal gate length ratio variations for different ratio of undamaged ($L1$) and damaged ($L2$) channel length distances,

considering positive and negative charges in the oxide interface for SG device. As seen from the figure in case of positive interface charges, the increase in the length of damaged region i.e. *L*2, raises the minimum surface potential and shifts it towards the source side. The position of the minimum surface potential is closer to source for a greater length of *L*2. This indicates a higher SCE in the device as the *L*2 extends more. This will further lower the source channel barrier height and hence a higher threshold voltage roll-off. However, in case of negative interface charges, the increase of the length of *L*2 region decreases the minimum surface potential. This will give a higher source-channel barrier height and hence a lower threshold voltage roll-off. The shifting of the minimum surface potentials is opposite as that of in the positive interface charge case i.e. the minimum surface potential point shifts towards drain side as *L*2 length decreases. Similar analysis can be predicted from Fig. 5(a) in case of DG.

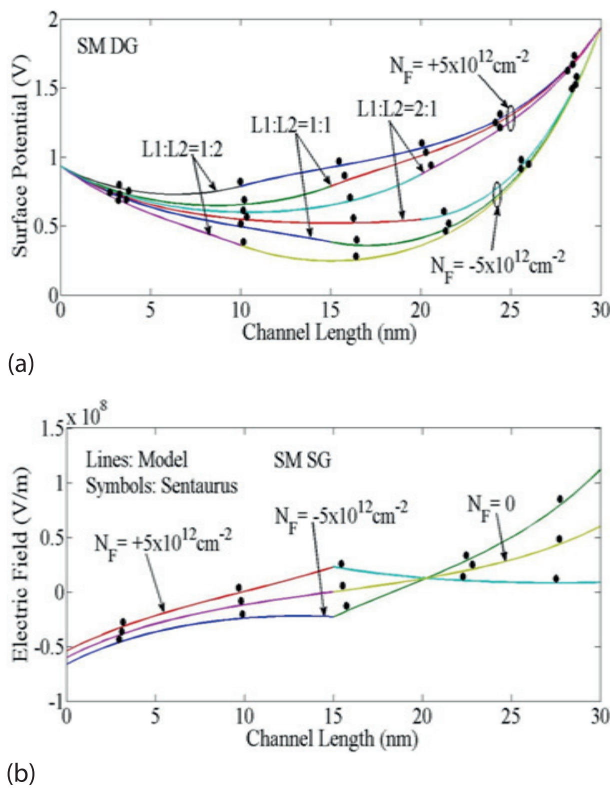


Figure 5: (a) Surface Potential variation along the channel length for interface charge variations for different damaged region length ratios (*L*1/*L*2=1:2, 1:1, 2:1) of Double Gate device. (b) Electric Field variation along the channel length for interface charge variations of Single Gate device. Parameters used are ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=10 nm, *L*=30 nm, t_{ox}=2 nm, V_{DS}=1 V and V_{GS}=0.1 V.

Fig. 5(b) shows the variation of the electric field distribution along the channel for different amounts and polarity of interface trapped charges in the oxide for SG case. From the figure, the inflection point of the electric field lies at the interface of the damaged and undamaged regions. The device having positive interface charge will give maximum electric field peak as compare to N_F=0 and N_F negative cases. So, positive interface charge case will cause higher short channel effect on the device than its negative charge counterparts due to high electric field. Similar analogy can be forecast for DG device from Fig. 6(a). However, one can observe a lower electric field in case of DG from SG by comparing the Fig. 6(b) and Fig. 6(a).

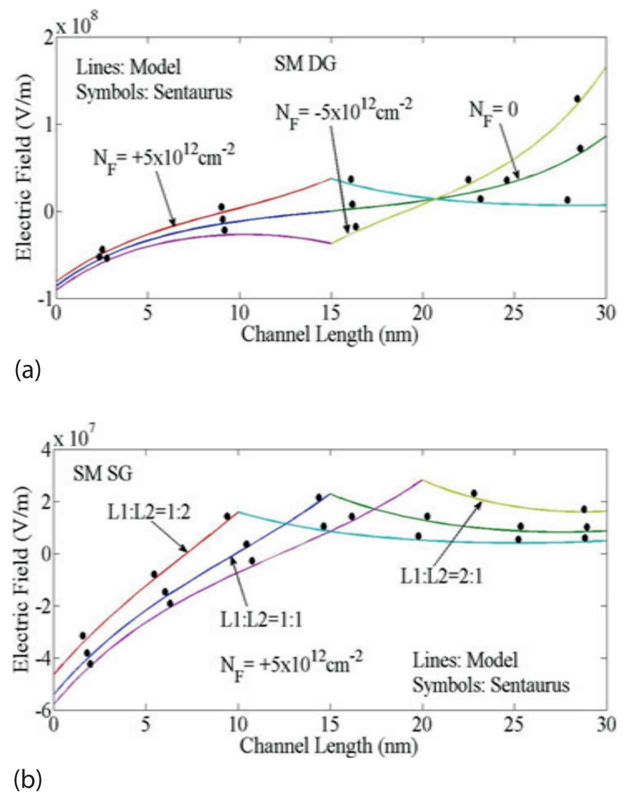
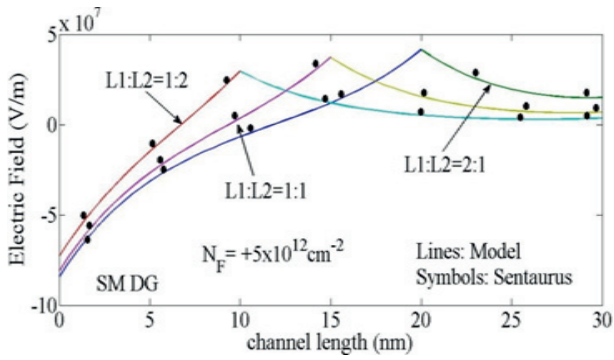


Figure 6: (a) Electric Field variation along the channel length for interface charge variations of Double Gate. (b) Electric Field variation along the channel length for different damaged region length ratios (*L*1/*L*2=1:2, 1:1, 2:1) of Single Gate. Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=10 nm, *L*=30 nm, t_{ox}=2 nm, V_{DS}=1 V and V_{GS}=0.1 V.

Fig. 6(b) shows the variation of horizontal electric field of the UTB-SG SOI MOSFET for different gate length ratios by considering positive interface charges. The point of maximum barrier lies at the intersection point of the damaged and undamaged regions. As length *L*2 decreases or the *L*1/*L*2 ratio increases, the point of peak electric field at the interface is shifted towards the drain side. This causes a higher carrier drift velocity and device speed. The carrier transport efficiency increases with decreasing *L*2, which causes a reduction in hot

carrier effect (HCE) and improvement in DIBL. In case of DG, the Fig. 7(a) can be referred for analysis purpose. Fig. 7(b) and Fig. 8(a) show the variation of the electric field distribution along the channel for different gate length ratios by considering negative interface trapped charges in the oxide for SG and DG device, respectively. From both the figures, as the length of damaged region i.e. *L*2 decreases, the peak of the electric field shifted towards the drain side. By comparing between positive and negative interface charge cases, the device having positive interface charge will give maximum electric field peak as compare to N_F=0 and N_F negative cases. So, positive interface charge case will cause higher short channel effect on the device than its negative charge counterparts due to high electric field. Fig. 8(b) shows the threshold voltage variation along the channel length for N_F=0, negative and positive in the oxide for SG device. From the figure, the threshold voltage is higher in case of negative N_F and it is lower for positive interface charge case. This is due to the lower barrier height in case of positive interface charge as discussed in Fig. 3(b). So, the device having positive interface trap charges are more susceptible to short channel effects.



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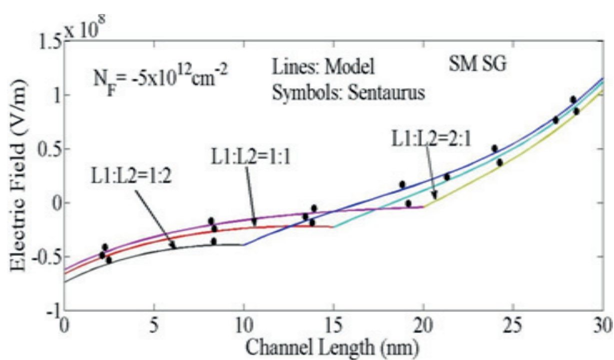
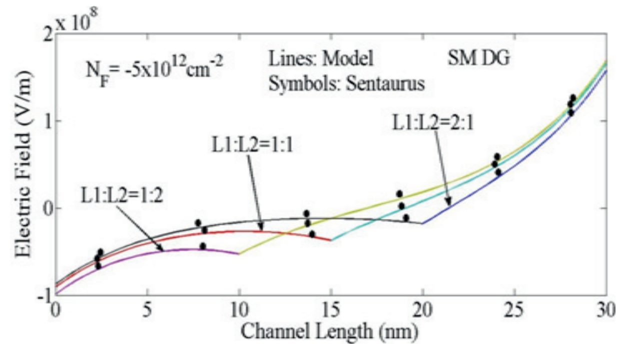
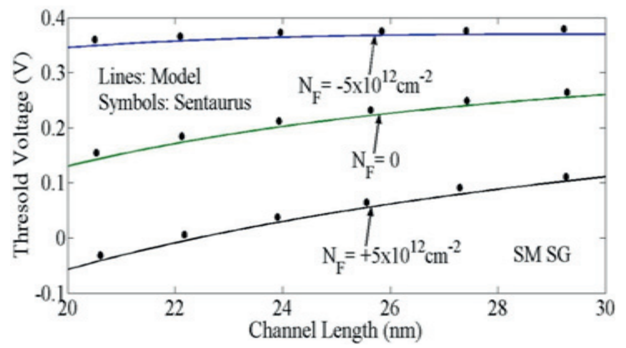


(b)

Figure 7: (a) Electric Field variation along the channel length for different gate length ratios (*L*1/*L*2=1:2, 1:1, 2:1) of Double Gate. (b) Electric Field variation along the channel length for different gate length ratios (*L*1/*L*2=1:2, 1:1, 2:1) for negative trap charge of Single Gate. Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=10 nm, *L*=30 nm, t_{ox}=2 nm, V_{DS}=1 V and V_{GS}=0.1 V.



(a)



(b)

Figure 8: (a) Electric Field variation along the channel length for different gate length ratios (*L*1/*L*2=1:2, 1:1, 2:1) for negative trap charge of Double Gate. (b) Threshold Voltage variation along the channel length for different gate trapped charges of Single Gate. Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=10 nm, *L*=30 nm, t_{ox}=2 nm, V_{DS}=1 V and V_{GS}=0.1 V.

Figure 9 (a) and (b) shows the variation of threshold voltage with the channel length for different damaged and undamaged length ratios (*L*1/*L*2= 1:2, 1:1, 2:1) for negative and positive interface trapped charge cases respectively. It is observed that SCE become serious on decreasing the channel length ratios. That means the threshold voltage is higher for the higher undamaged gate length i.e., *L*1. This is because of the higher channel barrier height for higher length ratio (*L*1/*L*2=2:1) as predicted in Fig. 4(b). Further, the roll-off in the threshold curve is higher for the device having smaller length ratio (*L*1/*L*2=1:2). This is attributed to the fact that the control gate loses its control over the channel at smaller *L*1 and higher *L*2.

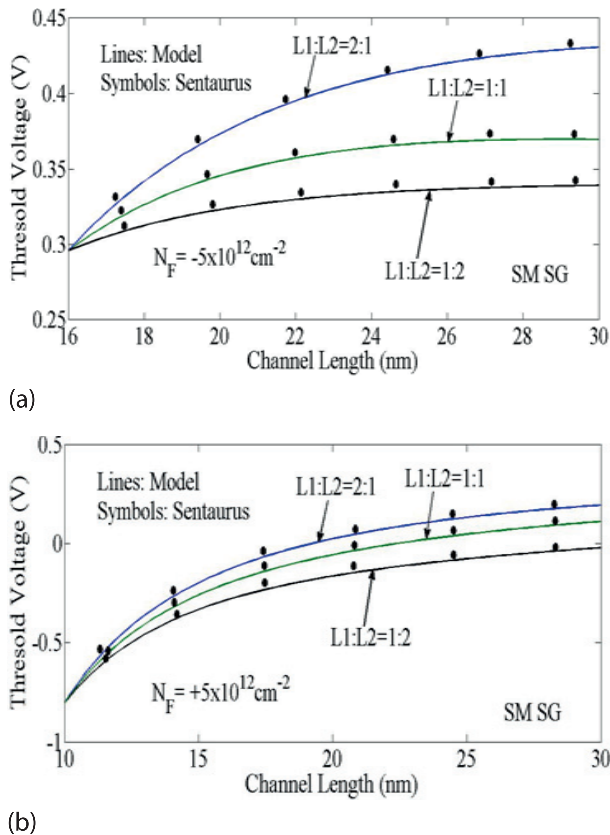


Figure 9: Threshold Voltage variation along the channel length for different gate length ratios (*L*1/*L*2=1:2, 1:1, 2:1) of Single Gate including negative trap charge. (b) Threshold Voltage variation along the channel length for different gate length ratios of Single Gate including positive trap charge Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=10 nm, *L*=30 nm, t_{ox}=2 nm, V_{DS}=0.1 V and V_{GS}=0.1 V.

5 Conclusion

The derived model for surface potential, electric field and threshold voltage has been shown the effectiveness of UTB DG SOI MOSFET to suppress the SCEs. Due to the additional gate introduction, there is more control over the channel region and that will be the important factor for suppression of hot carrier effect (HCE) and DIBL. An extensive analysis is carried out to study the effect of various parameters like drain bias, damaged and undamaged length ratio variation, and interface charge variation on surface potential, electric field, and threshold voltage. From the result, the deterioration in the threshold voltage may be improved by increasing the length of *L*1 i.e. decreasing the undamaged region. The DIBL and HCE can be controlled effectively by increasing the gate length ratio (*L*1/*L*2), which can be achieved by proper fabrication methodologies. The device performance is going to deteriorate in presence of the interface trap charges in the oxide. The derived analytical model is compared and found to be in excellent agreement with the simulation results obtained from Sentaurus™.

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Low Leakage Charge Recycling Power Gating Structure for CMOS VLSI Circuits

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Abstract: Power dissipation has become an important factor in integrated circuits fabrication due to the rapid increase of battery powered hand held devices. In particular static dissipation increases considerably as technology scales down. To extend the battery lifetime of portable devices and ensure proper operation of digital circuits, static dissipation reduction needs to be addressed. In this paper, a low leakage charge recycling technique is proposed for this concern. The simulation results reveal that this technique exhibits 74 % leakage reduction, 37 % ground bounce reduction, 58 % Power Delay Product (PDP) reduction and nearly 10-33 % improvement in noise margin compared to conventional technique.

Keywords: charge recycling; data retention; drowsy mode; leakage power; power gating; sleep mode

Vezja CMOS VLSI z nizkim uhajalnim tokom vrat

Izvleček: S porastom števila baterijsko napajalnih naprav je poraba energije postala ključen problem pri izdelavi integriranih vezij. Natančneje, z manjšanjem velikosti vezij se poraba povečuje. Za podaljšanje baterijskega delovanja in zagotavljanje zanesljivega delovanja prenosnih naprav je porabo energije potrebno posebej obravnavati. V članku je predlagana tehnika nizkega uhajalnega toka in obnovljivega naboja. Rezultati nakazujejo 74 % znižanje uhajalnega toka, 27 % znižanje vpliva ozemljila, 58 % znižanje PDP in 10 - 33 % izboljšanje meje šuma glede na klasične tehnike.

Ključne besede: obnavljanje naboja; zadržanje podatkov; uhajalni tok; stanje pripravljenosti

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1 Introduction

Power dissipation in CMOS circuits mainly has two important components namely dynamic power dissipation and static power dissipation. Total power dissipation is dominated by dynamic power or switching power component. However in deep submicron technologies, static power is increasing and it is nearing the dynamic power [1]. Hence the concept of minimizing static power gains importance, if the devices remain idle for long time as its battery power will be drained off due to leakage. Static Power in CMOS circuits results due to the leakage currents flowing through the transistor when there are no input transitions. The main sources of leakage currents in a MOS transistor [2] are shown in figure 1.

Sub-threshold Leakage: The current which flows from the drain to the source of a transistor operating in the weak inversion region.

Gate leakage: The current which flows directly from the gate through the oxide to the substrate due to gate oxide tunnelling and hot carrier injection.

Gate Induced Drain Leakage: The current which flows from the drain to the substrate induced by a high field effect in the MOSFET drain caused by a high V_{DG}.

Reverse Bias Junction Leakage: It is caused by minority carrier drift and generation of electron/hole pairs in the depletion region.

Sub threshold leakage is the most predominant component compared to other leakage sources and minimizing this will lead to substantial decrease in static power [2]. Throughout this paper leakage refers to sub threshold leakage. Several techniques have emerged to reduce leakage power. Mutoh [3] proposed a power gating technique (sleep approach) which cuts off power to the circuit blocks when they remain idle. In sleep

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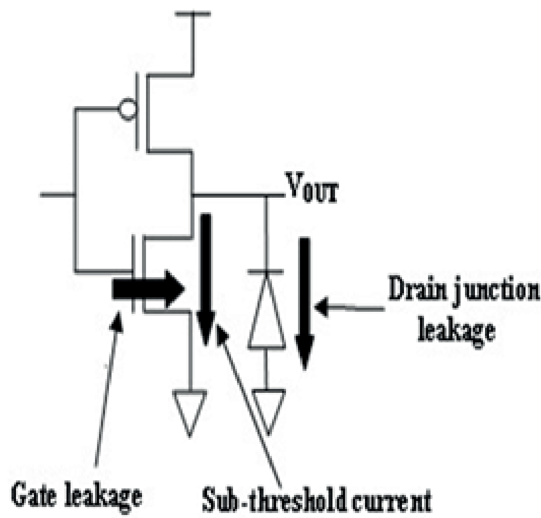

Figure 1: Leakage Currents

approach, the circuit blocks operate in active and sleep modes. High leakage reduction is obtained in sleep mode but the data in the circuit blocks are lost. Also when the circuit makes a transition between active and sleep mode, a large rush through current flows through the sleep transistor. When the circuit is in active mode, charge is stored at the gate of the sleep transistor and it is dumped to ground as the circuit moves to other state. No attempt is made to use the charge at the gate of the sleep transistor.

In this paper, we introduce low leakage charge recycling power gating structure which reuses the charge stored at the gate of sleep transistor to reduce rush through current and to provide data retention. The remainder of the paper is organized as follows: Section 2 describes about the literature survey of the leakage reduction techniques. The proposed technique and its functionality are elaborated in section 3 and the experimental results are discussed in section 4. Section 5 concludes the work.

2 Previous work

In CMOS circuits, data in the circuit blocks are lost if the circuit block is in standby mode. This becomes undesirable if the standby duration is short. To retain the data, an intermediate data preserving mode called drowsy mode is introduced by raising the virtual ground node voltage, thereby maintaining a significant voltage difference across the circuit blocks. The virtual ground voltage is raised by utilizing clamping devices like diodes, MOS transistors etc.

In [4], the authors proposed a sleep buffer approach which provides data retention without using any clamp devices. In sleep buffer technique, virtual ground voltage is raised, by recycling the charge at the gate of sleep transistor through sleep buffer and it works well when the circuit switches between active and drowsy modes frequently but the sleep mode is lost. This approach provides power gating to internal circuits and sleep buffer, but is not suitable for long idle periods due to high leakage. In [5], authors proposed a tri modal switch (TMS) which provides low leakage sleep mode and uses charge recycling for data retention. In sleep mode, leakage reduction is offered but a sneak path exists from V_{DD} to ground through sleep and drowsy transistors. TMS technique is not efficient in terms of area and leakage reduction. In paper [6], the authors propose a charge recycling technique as shown in figure 2, which reuses the charge at the gate of the sleep transistor to clamp the virtual ground level, thereby attaining data retention in intermediate mode. In this technique, a pass transistor (PT) is connected between the virtual ground rail and gate of sleep transistor for recycling the charge during mode transitions but the leakage power is soaring. In this paper, we provide an efficient power gating technique which mitigates leakage power in sleep mode and provide low energy, low ground bounce based on charge recycling concept.

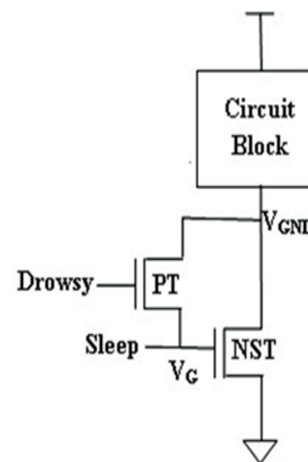

Figure 2: Charge Recycling Technique

3 Proposed technique

In this section, we present the circuit configuration and functionality of the proposed low leakage charge recycling (LLCR) technique. Figure 3 shows the circuit configuration of LLCR technique and its functionality is provided in Table 1. A PMOS transistor (PST) at the supply rail and NMOS transistor (NST) at the ground rail are used for power gating. A pass transistor (PT) is connected between V_G and V_{GND} for charge recycling and for boosting the V_{GND} level. LLCR technique enables three different circuit operation modes: active, sleep

and drowsy depending on the values of the control signals as shown in table 1.

Table 1: LLCR Technique Functionality

Sleep	Sleep bar	Drowsy	Circuit Mode
1	0	0	Active
0	1	0	Sleep
0	0	1	Drowsy

3.1 Active Mode

In active mode sleep bar, drowsy signals are low and sleep signal is high making the transistors PST and NST *on* and transistor PT *off*. As the sleep transistor is *on* the virtual ground (V_{GND}) node voltage is approximately at zero level. The voltage across the CMOS circuit block is $\approx V_{DD}$ and the circuit block resumes its normal operation. As the sleep signal is raised high, the voltage at the gate of the sleep transistor (V_G) is raised and the electric charge gets stored at V_G.

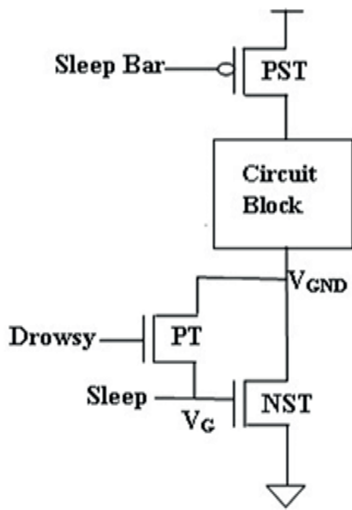

Figure 3: Low Leakage Charge Recycling Technique

3.2 Drowsy Mode

In drowsy (intermediate power saving) mode, drowsy signal is set to high while the sleep signal is set to low. The drowsy transistor is *on* and the charge stored at the gate of sleep transistor during active mode, increases the virtual ground voltage through the *on* drowsy transistor.

At the beginning of mode transition from active to drowsy, the drain current of the sleep transistor is given by

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2} \right] \quad (1)$$

The transistor PT conducts when the drowsy signal is high and the charge stored at V_G flows into V_{GND} through PT. This process continues until the charge at V_{GND} and V_G are equalized. Thus the drain and gate nodes of sleep transistor are connected through the pass transistor and its *Vgs* and *Vds* becomes equal. Now the current I_D through sleep transistor is as in equation (2).

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[\frac{V_{ds}^2}{2} - V_{th}V_{ds} \right] \quad (2)$$

The current I_D in equation (2) flows from virtual ground to ground and the V_{GND} voltage reaches equilibrium (*Vcr*) at the balance point of the leak current of the circuit block and the current through the sleep transistor. Thus the voltage level of V_{GND} node is increased to *Vcr* and the voltage across the circuit block is (V_{DD}-/*Vtp*/-*Vcr*), which is sufficient to retain the data in the block.

3.3 Sleep Mode

When the sleep, drowsy signals are low and sleep bar signal is high, transistors PST, NST and PT are *off*. The voltage across circuit block is zero and it enters into deep sleep mode. According to Table 2, gate leakage of PMOS is high, if it is in (011) state, that is when the PMOS is in direct contact with V_{DD} due to tunnelling of more electrons. In figure 2 all the PMOS transistor in the pull up network are connected to V_{DD}, which means that there are higher possibilities of electrons tunnelling from gate to source if the gate voltage of PMOS transistors are zero. In LLCR technique, only the sleep transistor (PST) is in direct contact with V_{DD} and all other PMOS transistors in the pull up network are connected through PST. In sleep mode, since PST is not in (011) state, no PMOS transistors in the circuit block are in (011) state even if their gate voltages are zero and thus the gate leakage is drastically reduced.

Table 2: Gate Leakage Currents; G=Gate, D=Drain, S=Source

Device	Bias {GDS}	90nm (nA)	65nm (nA)	45nm (nA)
PMOS	110	7.739	212.2	1240.5
PMOS	101	7.739	212.2	1240.5
PMOS	100	15.478	424.5	2480.7
PMOS	011	12.594	347.2	1991.5

Gate Leakage Current of PMOS at four significant states: [7]

Sub threshold leakage current of a MOS transistor is given by

$$I_{ds} = I_{dso}\, e^{\frac{V_{gs}-V_{to}+\eta V_{ds}-K\gamma V_{sb}}{n v_T}} \left(1 - e^{\frac{-V_{ds}}{v_T}}\right) \quad (3)$$

Where I_{dso} is the current at threshold, n is a process-dependent term affected by the depletion region characteristics, η is the DIBL coefficient, Vto is the threshold voltage when the source is at the body potential, V_T = kT/q = 26 mV, S is sub threshold slope and $k\gamma$ is the body effect coefficient. Sub threshold leakage current increases with Vds due to DIBL effect. In the proposed technique Vds of the PMOS transistors in the pull up network is very less as they are not in direct contact with V_{DD}. Hence as per equation (3) the sub threshold leakage reduction is high in LLCR technique. Therefore it is observed that the overall leakage reduction in LLCR is significantly better than charge recycling technique as the proposed LLCR technique suppresses the major constituents of leakage.

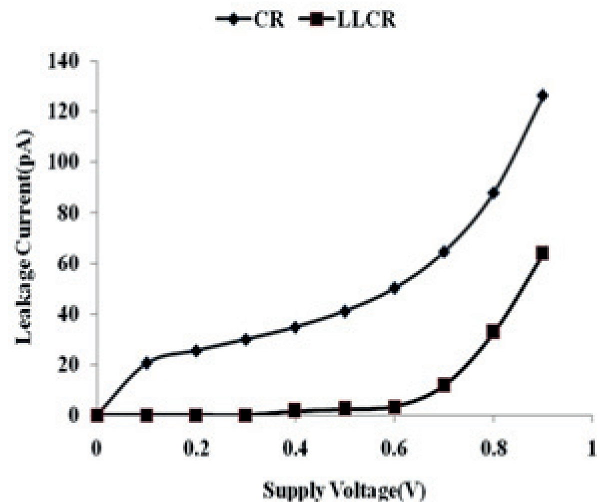

Figure 4: Leakage Current Comparison

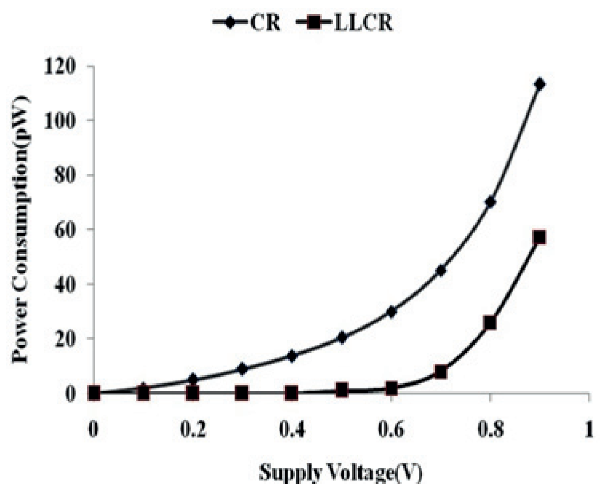

Figure 5: Static Power Comparison

4 Experimental results

We estimated leakage power, noise margin, ground bounce, delay and power delay product for conventional charge recycling and low leakage charge recycling techniques. We used Synopsys HSPICE for simulation of a two input NAND gate using 32nm PTM models [8]. Section 4 is organized as follows: Estimation of static power is characterized in section 4.1, ground bounce analysis is done in section 4.2, power delay product is discussed in 4.3. Section 4.4 deals with static noise margin analysis.

4.1 Static Power Estimation

In CMOS circuits, leakage of pull up network is determined by the parallel PMOS transistors that are in direct contact with V_{DD}. Considering figure 2, all the PMOS transistors in the pull up network are in direct contact with V_{DD} and as the circuit blocks size increases, number of PMOS parallel paths in contact with V_{DD} also increases and the leakage increases. Considering the proposed scheme, sub threshold leakage is determined by only one PMOS transistor (PST) irrespective of the circuit block size. This illustrates that the leakage in proposed LLCR technique is less compared to the leakage in the structure of figure 2. The leakage current and static power comparisons in sleep mode are shown in figure 4 and figure 5 respectively.

4.2 Ground Bounce analysis

In CMOS circuits the parasitic components of the power and ground distribution networks produce power/ground bounce. As shown in figure 6, the instantaneous discharge current through the sleep transistor gives rise to current surges during mode transitions and the bouncing noise in one power gating domain is transferred to the surrounding active circuits blocks through the shared power and ground distribution networks. The active circuit blocks thereby may errornously latch a wrong value or switch at a wrong time, if the voltage due to the ground bounce is more than the noise margin of the circuit. The ground bouncing noise has become an important reliability issue in nanometer regime with shrinking noise margins.

The parasitic resistance, inductance and capacitance used for ground bounce calculation are 217 mΩ, 8.18 nH and 5.32 pF [10]. Figure 7 shows the ground bounce due to transitions from sleep to drowsy mode. Conventional charge recycling technique switches from 16.6 mV to 36.8 mV and the proposed LLCR technique switches from 14 mV to 30.9 mV. Hence it is clear that the proposed technique perform better as compared to the

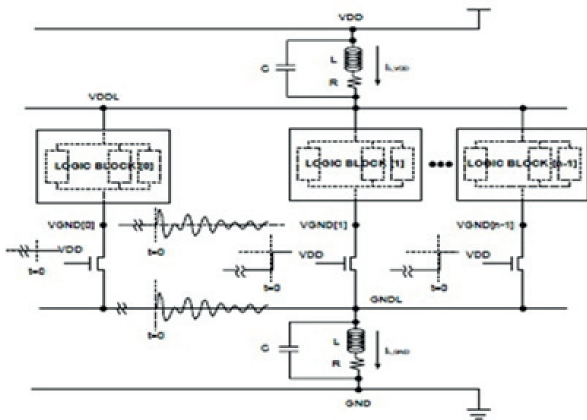

Figure 6: Ground bounce in a System-on-a-Chip employing multiple power gating structures to control leakage power [9].

conventional charge recycling technique. The average virtual ground voltage of CR and LLCR technique during mode transition is 180 mV and 114 mV respectively and it is given in table 4 which implies that the ground bounce surges are less in the proposed technique.

4.3 Power Delay Product Estimation

Power delay product (PDP) is another important factor for analysing the digital circuits, which is a product between propagation delay and power consumption. Static power delay product comparison is shown in figure 8. The delay of LLCR technique is 8.556E-12 seconds while the delay of conventional technique is 5.32E-12 seconds. Delay of LLCR technique is more due to the parasitic capacitance of the additional PMOS sleep transistor (PST). However the proposed method has a superior performance in terms of power delay product compared to the conventional charge recycling technique as the leakage power dissipation of LLCR technique is much less.

4.4 Static noise margin

In drowsy mode data stability should be high as this mode is meant for preserving the data. Noise margin defines the data stability of the circuits in data retention mode by determining the allowable noise voltage on the input so that the output will not be corrupted. Higher the noise margin better is the stability. The specification most commonly used to describe noise margin are the low noise margin NM_L, and the high noise margin NM_H. These parameters are estimated from the DC transfer characteristics of the circuits by calculating V_{IL}, V_{OL}, V_{IH} and V_{OH} values. The DC characteristics and its slope of the proposed technique for noise margin calculation are shown in figure 9.

Noise margin values depend on the effective supply voltage experienced by the circuit block. As the average virtual ground voltage value of LLCR technique is less during mode transitions, the supply voltage experienced by the circuit block is more leading to good data retention and stability as compared to conventional technique. Table 3 lists the noise margin values and it is clear that the data stability is high in LLCR

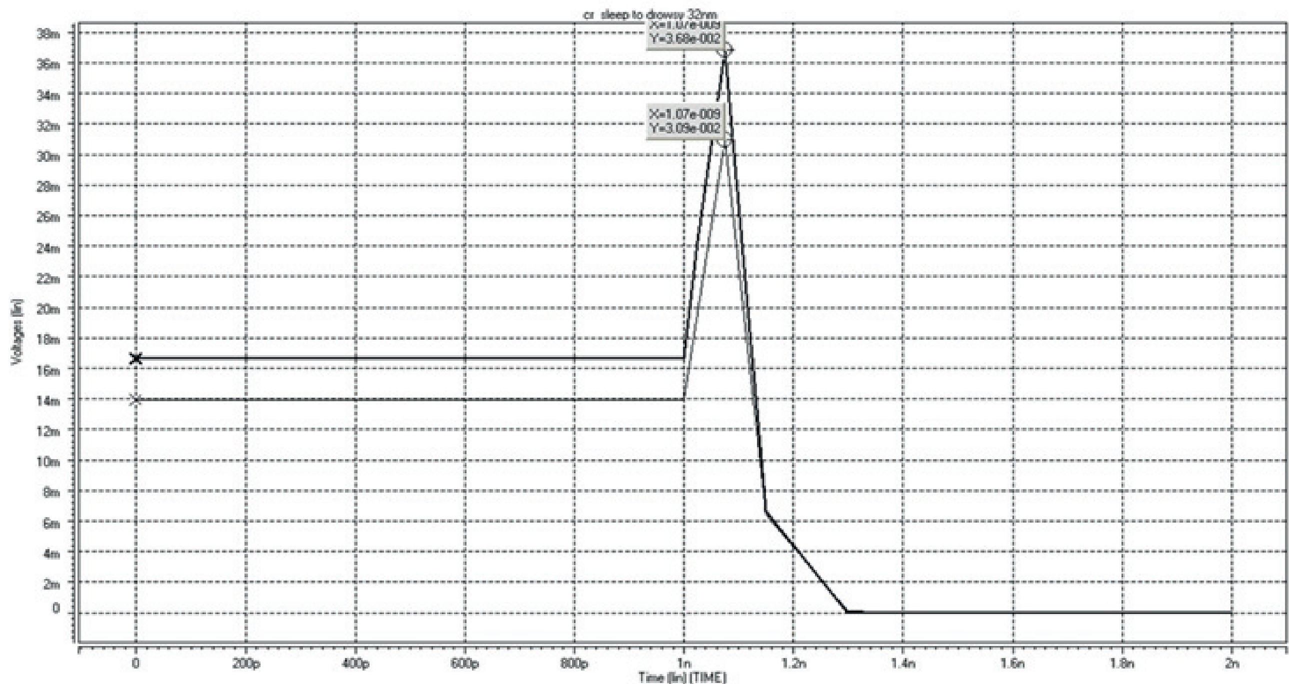

Figure 7: Ground Bounce Comparison

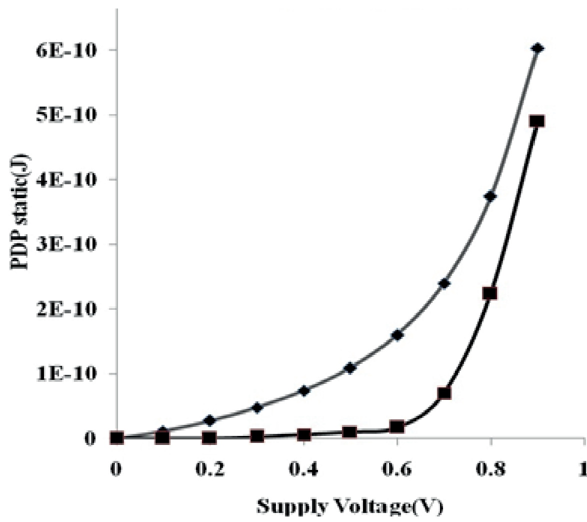

Figure 8: PDPstatic Comparison

technique by a maximum of about 32.5 % over conventional technique.

Table 3: Static Noise Margins (mV)

Technique	NML	NMH
LLCR	266	293
CR	243	221

The performance characteristics comparison shown in table 4 proves that the low leakage charge recycling technique performance is better than conventional charge recycling technique. In conventional power gating structures always there is a trade off between the leakage power and ground bounce but the proposed technique offers both leakage power and ground bounce reduction.

Table 4: Performance Characteristics

	CR	LLCR
Static Power(xE-10W)	2.2947	0.5980
Average Vgnd Voltage(xE-1V)	1.8090	1.1450
Delay(xE-12S)	5.32	8.55
PDP(xE-21J)	1.2214	0.5081

5 Conclusion

In this paper performance characteristics such as leakage power in sleep mode, data stability, ground bounce and power delay product of conventional charge recycling technique and proposed LLCR technique are scrutinized in detail. From the analysis it is apparent that the LLCR technique consumes low power in sleep mode compared to conventional charge recycling technique. Ground bounce, noise margin and power delay product estimation makes clear that this scheme is an efficient power gating technique. The proposed LLCR technique can be used in hand held devices such

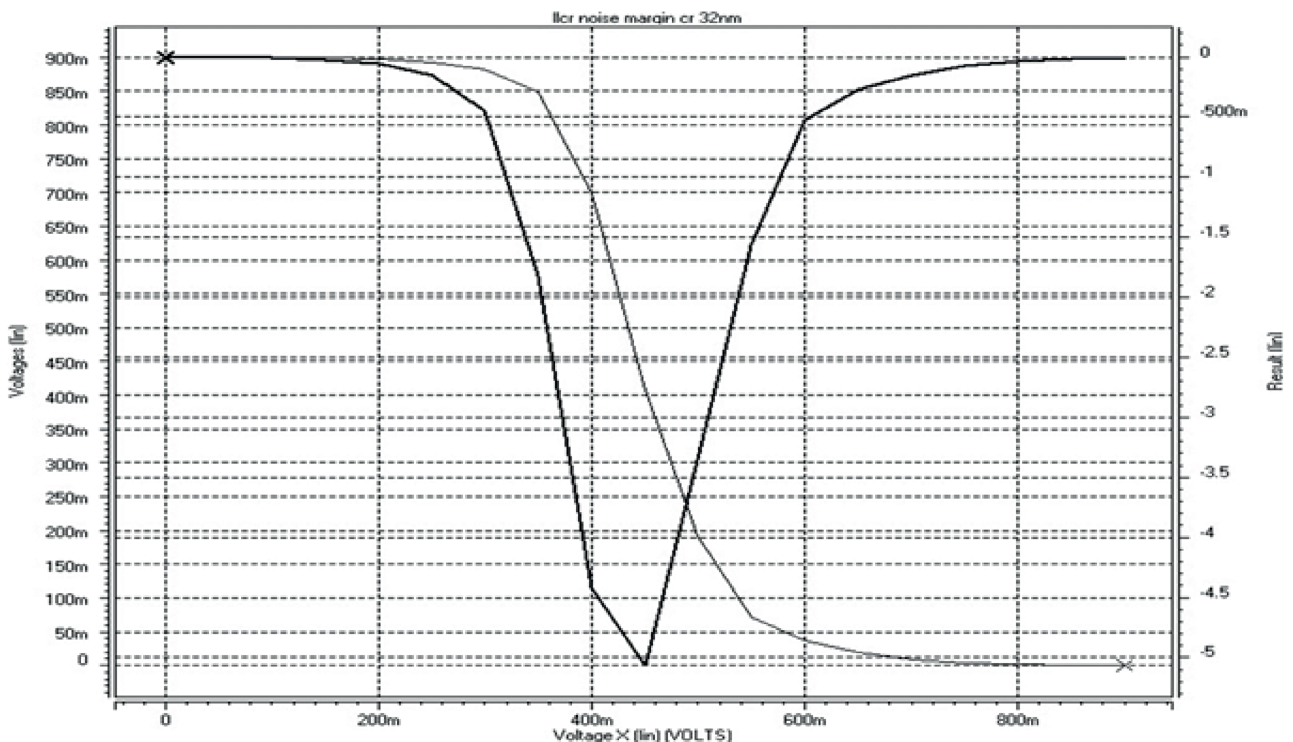

Figure 9: DC transfer Characteristics of LLCR Technique

as mobile phones and laptops for leakage reduction and data retention if the devices are idle for short duration as well as for long duration.

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Comparative Assesment of Ground Plane and Strained based FDSOI MOSFET

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Abstract: In the present work, we have investigated the performance of ground plane and strained silicon on FDSOI MOSFETs. The 2D ATLAS simulations are done and the simulation model is validated with previously published experimental results. The transfer characteristics, DIBL, Vt, Ion and Ioff of all the structures are analyzed for 25 nm and 32 nm gate length. The effect of body thickness on device performance is also evaluated. Strained device offer higher drive current, but increases the leakage current. We have applied the ground plane to reduce the leakage current. The DIBL is higher for the strained device. DIBL in GPS and GPB structures (strained and unstrained) is almost same, and is lower than conventional FDSOI structure. The FDSOI devices have the lowest threshold voltage as compared to the GP and GPB devices, with GPB offering the highest Vt. The drain current is observed to increases almost linearly with body thickness. The deployment of ground plane and strained silicon on FDSOI MOSFET shows promise to substitute conventional MOSFET for high speed and low power applications.

Keywords: FDSOI; Strained FDSOI; Ground Plane in BOX; Ground Plane in substrate; DIBL

Primerjalna ocena FDSOI MOSFET-ov z masnim slojem in na osnovi napetega silicija

Izvleček: V članku predstavljamo rezultate raziskav lastnosti masnega sloja in napetega silicija na FDSOI MOSFET. Simulacije so opravljene z 2D ATLAS simulatorjem in preverjene z rezultati prejšnjih raziskav. Analizirane so prenosne karakteristike, DIBL, Vt, Ion in Ioff za dolžine vrat 25 nm in 32 nm. Prav tako je obravnavan vpliv debeline elementa na njegove lastnosti. Elementi z napetim silicijem omogočajo višje krmilne tokove, a imajo hkrati tudi večji uhajalni tok. Za zmanjševanje uhajalnega toka je dodan masni sloj. DIBL je višji ob uporabi napetega silicija. DIBL pri GPS in GPB elementih je enaka in nižja kot pri klasičnih FDSOI strukturah. FDSOI strukture imajo najnižjo pragovno napetost v primerjavi z GP in GPB elementi. Ponorni tok se linearno povečuje z debelino substrata. Uvedba masnega sloja pri FDSOI MOSFET nakazuje možnost njihove uporabe pir hitrih aplikacijah z nizko porabo.

Ključne besede: FDSOI; napet silicij; masni sloj; DIBL

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1 Introduction

The performance of conventional MOS transistor is degraded by short channel effects in the sub-100 nm regime. In such a scenario, the Silicon-on-Insulator (SOI) technology come forward to become the next driver to continue the Moore's Law. SOI has proved capable of providing increased transistor speed, reduced power consumption and enhanced device scalability as demanded by the today's era and beyond technology generations. Today, however, the ever increasing demand for small size, high speed and low power consumption overshadows the inherent advantages of SOI. The fully depleted (FD) SOI transistor came into manufacturing mainstream by 2008 [1]. According to France-based Soitec, almost all semiconductor companies have either switched to SOI or are considering it for current and future devices. While IBM, AMD, Sony Group and Toshiba have adopted SOI for the cell processor, Philips semiconductors has been using SOI for high voltage ICs. Freescale and ST Microelectronics have also begun to use SOI wafers. Several device based on SOI varying from single gate to multiple gate

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structures have evolved and are in the stage of being researched [2].

Although SOI technology is widely used by the chip-makers, at smaller gate length (below 50 nm), its performance is degraded by short channel effects (SCE). For short gate lengths devices operates under very high traverse electric fields, which continue increases with scaling. The increase in the vertical electric field severely degrades silicon channel mobility [3]. Many device level techniques has been adopted to reduce the SCE's like- Thin body FD SOI with raised source and drain, graded Channel FDSOI, Metal gate FDSOI, Buried insulator Engineering, Ground plane FDSOI MOSFET, multiple gate FDSOI MOSFET , etc.

For the mobility enhancement, innovations in device design are required to keep up the device performance. In this regard, silicon has attractive feature, which boosts the device performance. Most of the semiconductor companies like Intel and Texas Instruments have switched to strained silicon based devices for mobility enhancement [4]. In fact, now, Silicon on Insulator (SOI) and Strained Silicon are the two key drivers of CMOS scaling.

In this paper, we have studied the effect of ground plane and strained silicon on FDSOI MOSFET. Ground plane is the highly doped P-type semiconductor in NMOS case and highly doped N-type semiconductor in PMOS. Ground plane is used for grounding the electric field lines originating from drain due to high drain bias. Ground plane act as a collector of the drain electric field lines, thereby reduces DIBL. Two types of insertion techniques viz. GPS (Ground plane in substrate) and GPB (ground plane in BOX) are possible. The GPB structure is more effective when the distance between the GP and the drain is small as compared to the channel length. In GPS structure, the BOX thickness should be kept as small as possible to reduce leakage current. To minimize the leakage current, GPB structure is preferred [5].

Strain in silicon channel can be introduced either during processing known as process-induced strain or from the bottom by growing silicon on top of a crystalline template typically silicon with 20 % or more germanium content, known as substrate-induced strain. In this work, we use the substrate-induced strain. The most effective way to introduce high tensile strain to the channel is to epitaxial grow strained silicon on a relaxed silicon germanium (Si-Ge) layer [6]. There is no doubt that Strained silicon helps in increasing the ON current, but it also significantly increases the leakage current (OFF current), which degrades the device performance. To decrease the leakage further we implied the concept of Ground plane in strained devices to optimize the device for low power and high-speed applications.

In this work, we have compared and analyzed the device performance of FDSOI, FDSOI-GP, FDSOI-GPB, Strain-FDSOI, Strain-FDSOI-GP and Strain-FDSOI-GPB MOSFETs. We have proposed new device, in which strained channel and ground plane, both device level techniques are incorporated in the same structure. This structure is the optimized structure of strained silicon and ground plane. The transfer characteristics, DIBL, V_t, I_{on} and I_{off} of all the six structures are analyzed for 25 nm and 32 nm gate length. The effect of body thickness on device performance is also evaluated. In Section 2, the device structure of all devices is discussed. In Section 3 the simulation framework and model calibration is discussed. Section 4 presents the result and discussion. Finally, section 5 concludes the paper.

2 Device Description

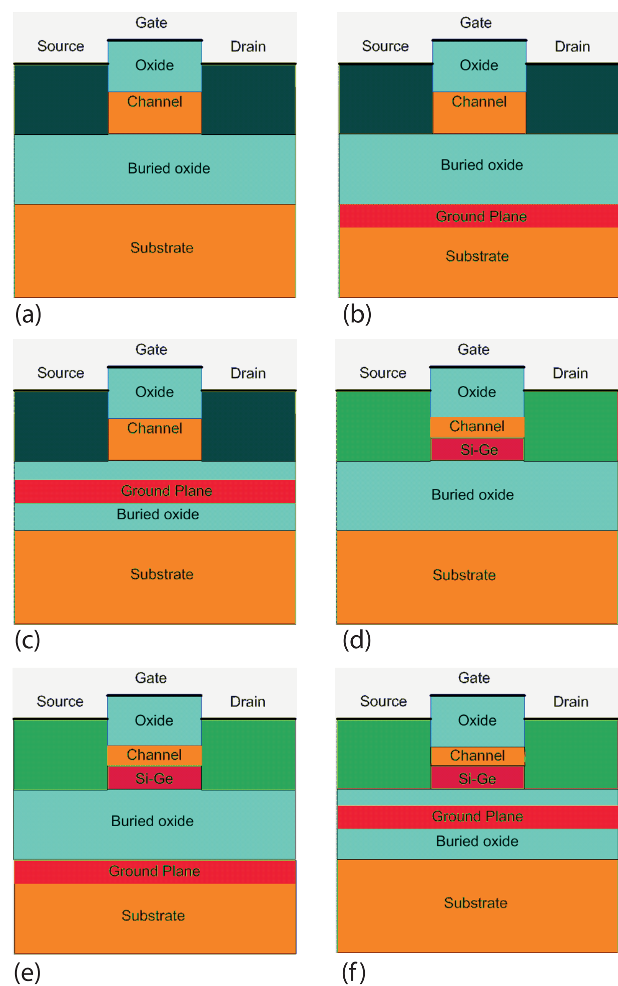


Figure 1: Physical structure of FDSOI devices (a) conventional FDSOI, (b) FDSOI-GP, (c) FDSOI- GPB, (d) Strained FDSOI, (e) Strained FDSOI-GP, (f) Strained FDSOI-GPB

Fig 1 shows the six different FDSOI device structure i.e. Conventional FDSOI (FDSOI), FDSOI with ground plane in substrate (FDSOI-GP), FDSOI with ground plane in BOX (FDSOI-GPB), strained FDSOI (Strain FDSOI), strained FDSOI with ground plane in substrate (Strain FDSOI-GP), Strained FDSOI with ground plane in BOX (Strain FDSOI-GPB). All the devices are analyzed at 25 nm and 32 nm gate length. Gate oxide thickness of 2 nm has been used. The source and drain regions are doped with the concentration of 10^{16} cm^{-3}, have an abrupt doping profile at source and drain ends. For conventional FDSOI BOX thickness of 50 nm and substrate thickness of 70 nm is used. Substrate has been taken intrinsic and channel has lightly doped with P-type semiconductor to adjust the threshold voltage. Ground plane is made by the P++ type doping in NMOS for the two structures of ground plane are discussed in this work, Ground plane thickness is taken as 5 nm in both the cases.

The strained SOI structure is designed using the substrate induced strain i.e. biaxial strain. Strain induced by placing the Silicon Germanium layer under the device silicon layer. The proportion of germanium in (Si-Ge) alloy and the thickness of the (Si-Ge) layer are the main factors that control the strain in the channel. We have used 20 % of germanium and 80 % of silicon and thickness of silicon germanium layer is 22 nm.

3 Simulation model calibration and experimental comparison

The 2D simulation were carried out by using ATLAS device simulator incorporating the concentration dependent mobility model and electric field dependent carrier mobility model with velocity saturation. Shockley–Read–Hall recombination/ generation with doping-dependent carrier lifetime, and Auger recombination were included in the simulation to account for leakage currents. For numerical iteration Gummel numerical solution procedures is used along with the Fermi Dirac carrier statistics to obtain an improved initial guess for Newton solution scheme. The Gummel iteration method is generally used for the SOI. Watt mobility model is also used with suitable modification in the saturation velocity of the electrons for considering best mobility approximation In the presence of heavy doping, greater than 10^{18} cm^{-3}, experimental work has shown that the pn product in silicon becomes doping dependent. As the doping level increases, a decrease in the bandgap separation occurs, where the conduction band is lowered by approximately the same amount as the valence band is raised. To deploy the strain in the simulation we used the strained silicon low field mobility model [7].

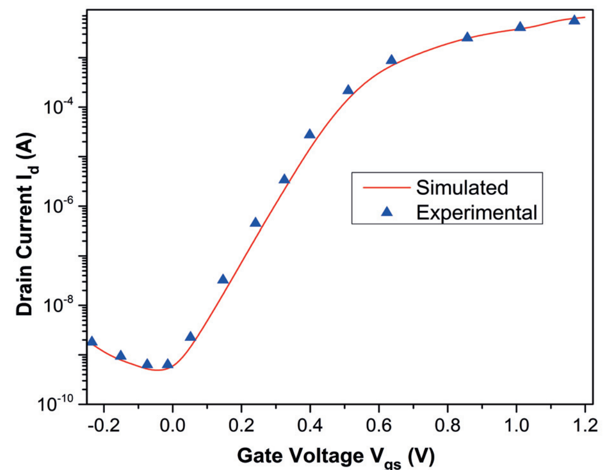


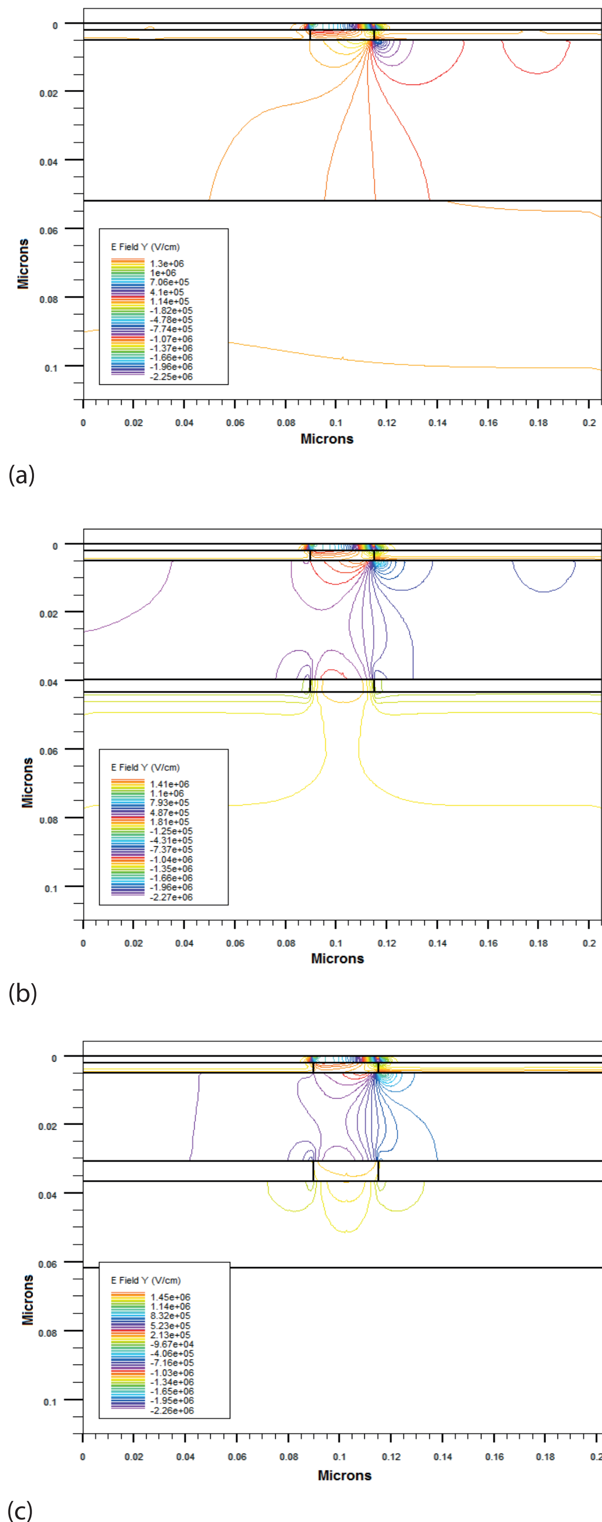
Figure 2: Experimental [8] (symbols) and simulated (solid lines) transfer characteristics for FDSOI-GP at V_{ds} = 1 V.

In this section, we have simulated the fabricated Ground Plane FDSOI structure of ref [8] and calibrated our simulation model by comparing the simulation with the experimental transfer characteristic. Fig 2 shows a very good agreement between the experimental [8] and simulated transfer characteristics of FDSOI-GP device, validating our simulation model. Post validation extensive simulation of the FDSOI, FDSOI-GP, FDSOI-GPB, Strain FDSOI, Strain FDSOI-GP, and Strain FDSOI-GPB is done to analyze the effect of gate length and body thickness on the device performance.

4 Results and Discussion

Fig. 3 shows the electric field contour of the FDSOI, FDSOI-GP, and FDSOI-GPB structures. In Fig 3(a), conventional FDSOI have large number of electric field lines passing through the channel body, hence the drain to substrate leakage is high in this structure. Whereas, in FDSOI-GP and FDSOI-GPB (fig 3(b) and 3 (c)) comparatively less electric field lines pass through the channel, thereby reducing the leakage due to the addition of ground plane in conventional FDSOI structure. The GPB structure has the lowest leakage in all the above mentioned structures due to the reduced distance between the channel and the ground plane [5].

Fig 4 shows the transfer characteristics for a 25 nm (Fig 4a) and 32 nm (Fig 4b) length device. On reducing gate length from 32 nm to 25 nm the drain current is obseved to increases for all devices. The fact that the drain current is able to sustain its increase is thanks to the increasing drain velocity at the drain side of the device. On-state current, I_{on}, defined as the current at V_{dd} = 0.8 V when the gate length is 25 nm and V_{dd} = 25 nm



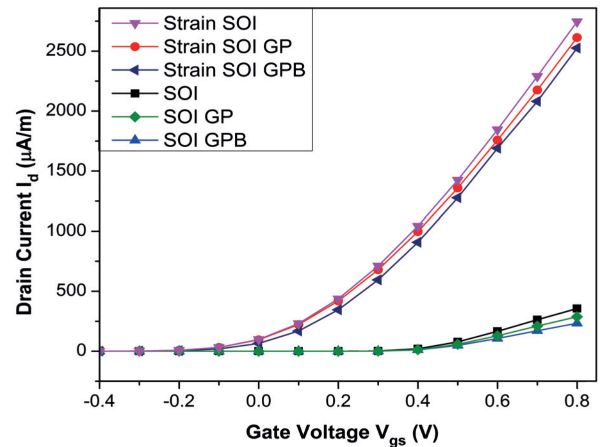
(a)

(b)

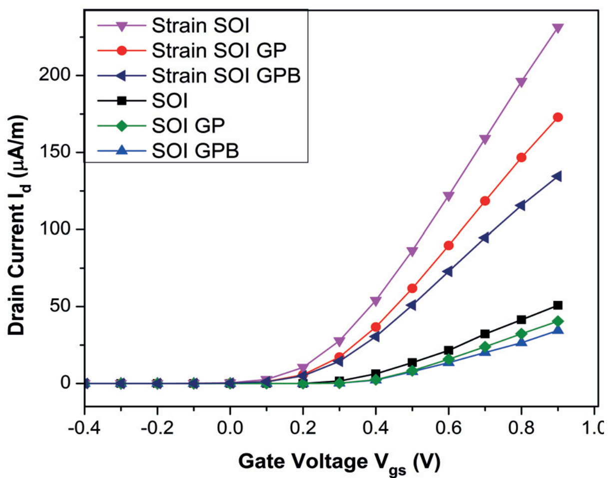
(c)

Figure 3: Electric Field Contour for FDSOI Devices extracted from ATLAS device simulator at $V_{gs} = V_{ds} = 1$ V. (a).Conventional FDSOI, (b). FDSOI-GP, (c). FDSOI-GPB

for 32 nm gate length, it is greater in strained channel devices then devices without strain in channel because application of biaxial strain to the channel increases the mobility of the charge carriers and increased mo-



(a)



(b)

Figure 4: Transfer Characteristics of the FDSOI, FDSOI-GP, FDSOI-GPB, Strain-FDSOI, Strain-FDSOI-GP and Strain-FDSOI-GPB devices. (a) For gate lengths of 25 nm, (b) For gate length 32 nm. The drain voltage $V_{ds} = 1$ V.

bility directly enhances the drive current.[9] The I_{on} is inversely proportional to gate length and it increases as gate length decreases.

The benefit of adding strain is visible at both the gate lengths. The I_{on} is highest for FDSOI devices followed by GP and GPB for both stained and unstrained devices. In GPB structures, the current drive capability of the transistor is less as the active region is much closer to the ground plane.

From figure 5, it can be seen that the off state leakage current (I_{off}) defined as the drain current at zero bias. This leakage current is less in GP structures because the highly conducting surface (ground plane) acts as a barrier for electric field and shields the fringing electric field lines from drain to channel. The leakage cur-

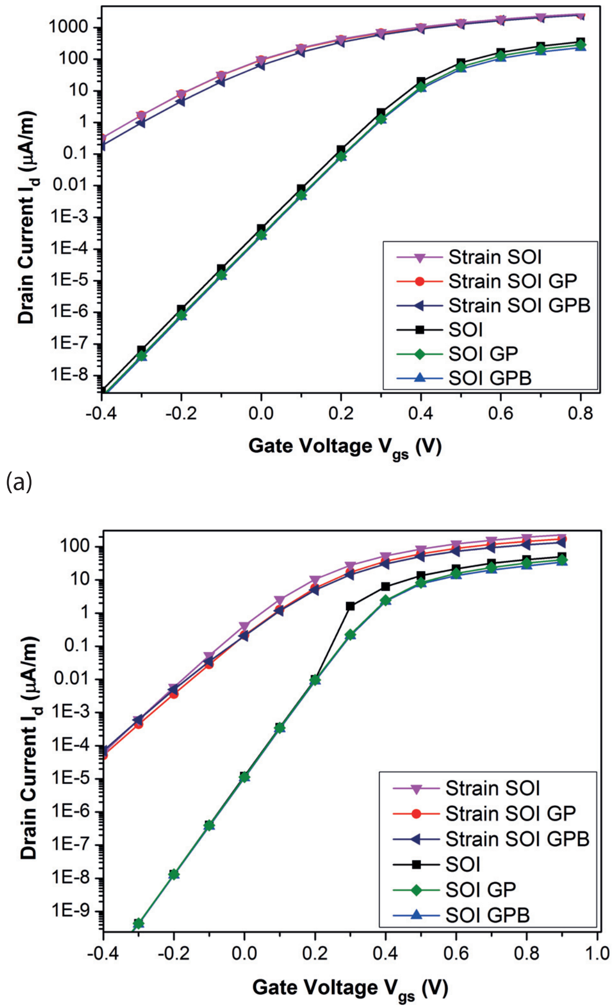


Figure 5: Subthreshold Characteristics of the FDSOI, FDSOI-GP, FDSOI-GPB, Strain-FDSOI, Strain-FDSOI-GP and Strain-FDSOI-GPB devices. (a) For gate lengths of 25 nm, (b) For gate length 32 nm. The drain voltage V_{ds} = 1 V.

rent is lowest in case of GPB structures because in this structure the active region of the device comes closer to ground plane region[5], reducing the drain induced electric field [5]. The leakage current is significantly larger for the device with channel under strain. To reduce the leakage current in strained FDSOI further we apply the ground plane, and it reduce the leakage current upto some extent.

In short gate length (L_g) devices the threshold voltage (V_t) is a function of drain to source voltage (V_{ds}) leading to Drain Induced Barrier Lowering (DIBL). As L_g reduces, the drain depletion region comes closer to the source depletion region and finally the field is penetrated. The lowered potential barrier at the source increases the injection of electrons by the source over the reduced channel barrier, due to which V_t is shifted. To find the DIBL, we have to first calculate the threshold voltage as the gate voltage at which the drain current I_d = 6 (*W/L*) nA, where width, *W* of the device is taken as 1 μm. DIBL short channel effect is calculated by the

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{ds}} = \left[\frac{(V_{th1} - V_{th2})}{(V_{ds1} - V_{ds2})} \right] \quad (1)$$

where, V_{th1} is threshold voltages extracted at drain bias of V_{ds1} = 0.1 V and V_{th2} is threshold voltages extracted at drain bias of V_{ds2}=1.0 V

Fig 6 shows the DIBL of all the devices under consideration having gate length of 25 nm and 32 nm. It is observed that DIBL increases with decreasing in L_g. The degradation in DIBL with L_g is due to the interaction of drain and source side depletion regions with each other near the channel surface to lower the source potential barrier. When a high V_{ds} is applied to a short gate length device, it lowers the barrier height, resulting in further decrease of the V_t. It is known that DIBL in ground plane devices is dependent on the distance between the channel and the ground plane [10]. If this distance is reduced DIBL will also reduce due to the effect of grounding the electric field lines originating from channel at high drain voltage. DIBL of GPS and GPB structure is almost same (Fig 6) because the distance of the ground plane from the channel is same in both the structures.

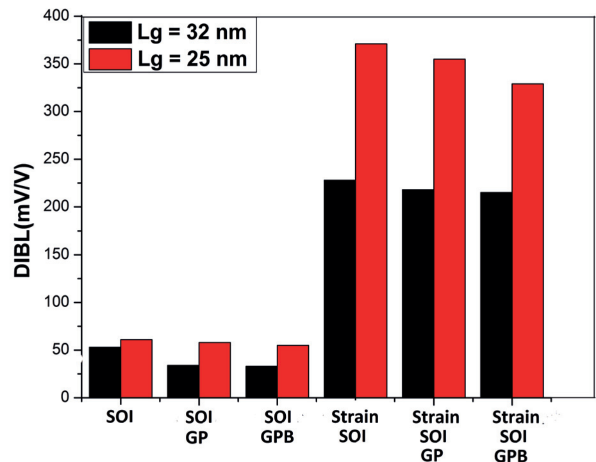


Figure 6: Comparison of DIBL for the FDSOI, FDSOI-GP, FDSOI-GPB, Strain-FDSOI, Strain-FDSOI-GP and Strain-FDSOI-GPB devices at gate lengths of 25 nm and 32 nm.

The strain causes the band gap (E_g) reduction that decreases the silicon work function (Fermi level decreases due to the increase of the intrinsic carrier concentration), which consequently affects the depletion region at the drain/channel junction, increasing the DIBL [11]. The DIBL for all the strained device is observed to be higher than unstrained devices. The DIBL for GPS and

GPB structures (stained and unstrained) is almost same, and is lower than conventional FDSOI structure.

The variation in threshold voltage for all devices for 25 nm and 32 nm gate lengths are shown in Fig 7. The V_t reduces with decrease gate length because of V_t roll-off effect. The FDSOI devices have the lowest V_t as compared to the GP and GPB devices. The V_t of GP and GPB devices is almost same, with GPB having slightly higher V_t as compared with GP device. The ground-plane keeps the electric field lines from propagating into the channel region, which helps to improve the SCE. The blocked field leads to increases in the threshold voltage. The application of strain reduces the threshold voltage [9].

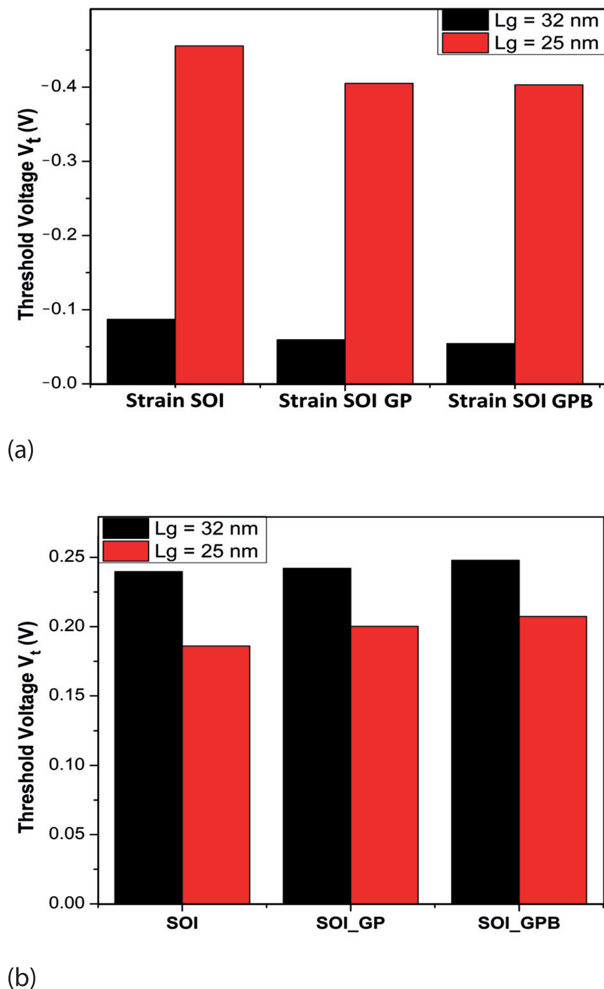


Figure 7: Comparison of Threshold Voltage for the FD-SOI devices at gate lengths of 25 nm and 32 nm. (a). Unstrained FDSOI, FDSOI-GP, FDSOI-GPB (b). Strain-FDSOI, Strain-FDSOI-GP and Strain-FDSOI-GPB

The strained Si/SiGe devices have negative threshold voltage. Negative threshold voltage is due to the lower conduction band edge in the strained Si than that in SiGe. The band gap narrowing is larger for biaxial strain as the valence band edge is shifted more. The threshold voltage decreases with increase in Ge content because of decrease in flatband voltage, decrease in source-body/drain-body build in potential [12].

The transfer characteristics of the conventional FDSOI devices as a function of body thickness are shown in Fig. 8a (for L_g=25 nm) and Fig.8b (for L_g=32 nm). It is observed that the drain current increases almost linearly with T_{si}. For body thickness less than 3nm, the quantum mechanical effect start to dominate and degrades the device performance. The threshold voltage (V_t) decreases as T_{si} increases and short channel effects comes into existence. The scaling of the T_{si} region increases the distance between conduction band (E_C) and ground state eigen energy due to which carriers goes into the higher energy subband, fermi level is also moves towards

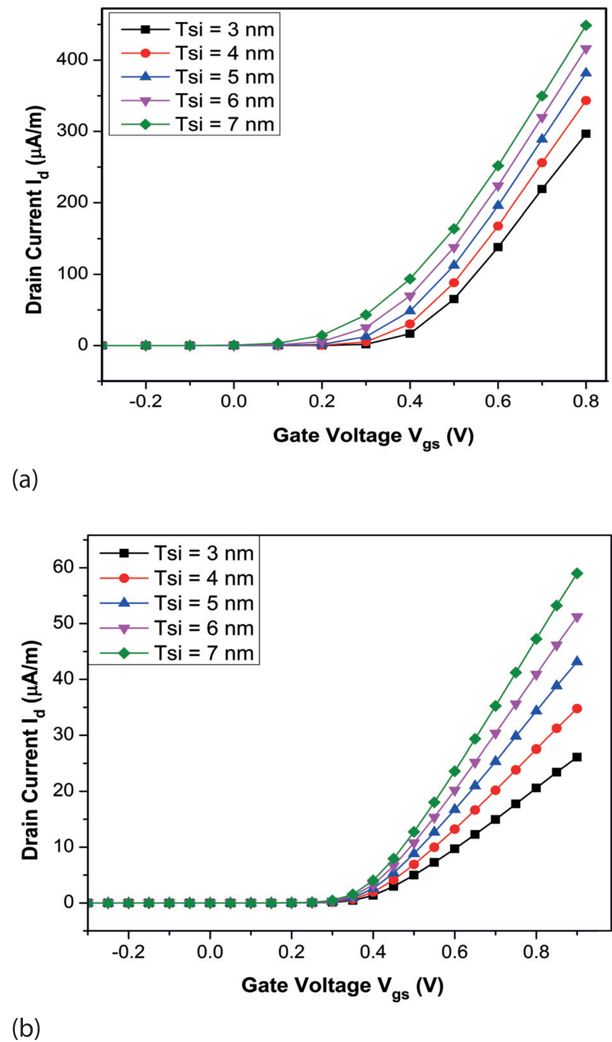


Figure 8: Transfer Characteristics of the FD SOI devices as a function of body thickness. (a) L_g = 25 nm, (b) L_g = 32 nm. The drain voltage V_{ds} = 1 V.

ground state eigen energy, due to which V_t increases. The peak values of drain current for the 25 nm device is 448 µA (Fig 8a.) and for 32 nm device is 58.9 µA (Fig 8b). These values are also shown in the table (Table 1).

Table 1: I_{on} and I_{off} of the FDSOI, FDSOI-GP, FDSOI-GPB, Strain-FDSOI, Strain-FDSOI-GP and Strain-FDSOI-GPB devices at gate lengths of 25 nm and 32 nm.

	L_g = 25 nm		L_g = 32 nm	
Device	I_{on} (µA)	I_{off} (nA)	I_{on} (µA)	I_{off} (pA)
FDSOI	356	45.2	50.7	12.1
FDSOI-GP	287	28.1	40.5	11.3
FDSOI-GPB	233	25.1	34.5	10.8
FDSOI	2750	97.9	231	0.418
FDSOI-GP	2610	94.7	172	0.216
FDSOI-GPB	2530	64.2	134	0.205

5 Conclusion

Effect of ground plane and strained silicon on FD SOI MOSFET (fully depleted Silicon on insulator MOSFET) has been studied. I_{off} reduced using FDSOI-GPS structure as compared to conventional FD SOI MOSFET and it is further reduced in case of FDSOI-GPB structure at two gate lengths 25nm and 32nm. The leakage current is less in GPB because in this structure the device region comes closer to ground plane region. Hence, the drain induced electric field reduced. In these structures, the current drive capability of the transistor also reduces. To increase the I_{on} concept of strained silicon has been deployed. The peak drain current in strained FD SOI structure is 2.750 mA as compared to 0.356 mA of conventional FD SOI MOSFET for 25 nm gate length device. To decrease leakage current, the concept of ground plane in strained SOI structure has been introduced. The simulated result shows that there is a reduction of leakage current by using strained GPS FD SOI up to some extent. The DIBL for all the strained device is observed to be higher than unstrained devices. The DIBL for GPS and GPB structures (strained and unstrained) is almost same, and is lower than conventional FDSOI structure. The FDSOI devices have the lowest V_t as compared to the GP and GPB devices, with GPB offering the highest V_t.). The drain current is observed to increases almost linearly with T_{si}.

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A Study of Analytical Solutions of Plate Equation for Pressure Microsensor Diaphragm: Limitations, Comparison and Usage

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Abstract: Analytical solutions of plate equation for square diaphragms provide quick estimation of the output characteristics of pressure sensors before finite element method (FEM) analysis. In this work, we analyze the limitations of using the model of a plate for the diaphragm of a piezoresistive pressure sensor. A comparison of various solutions of plate equations available in literature with FEM solution of plate is also carried out. Based on the above analysis, the most accurate analytical solution is determined. Using this solution, the methodology of obtaining the sensitivity and non-linearity of piezoresistive pressure sensors is delineated. This study shows the scope and limitations of using analytical solutions of plate equations for obtaining the output characteristics of a pressure sensor.

Keywords: Analytical equations; finite element method (FEM); piezoresistive pressure sensors

Študija analitčne rešitve enačbe plošče za mikrosenzorsko tlačno opno: omejitve, primerjava in uporaba

Izvleček: Analitične rešitve enačbe plošče za kvadratno opno predstavljajo hitro ocenitev izhodnih karakteristik senzorjev tlaka še pred analizo z metodo končnih elementov (FEM). V delu predstavljamo omejitve uporabljene metode na opni piezorezistivnega senzorja tlaka. Opravljena je tudi primerjava različnih objavljenih rešitev enačbe plošče s FEM rešitvijo. Na osnovi te analize je določena najboljša rešitev, ki je uporabljena za določitev občutljivosti in nelinearnosti piezorezistivnega senzorja tlaka. Študija predstavlja omejitve uporabe metode za določevanje izhodnih karakteristik senzorja.

Ključne besede: analitične enačbe; metoda končnih elementov (FEM); piezorezistivni sensor tlaka

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1 Introduction

Pressure sensors constitute a major portion of sales in the microelectromechanical systems (MEMS) mechanical sensors market [1]. Various transduction mechanisms are used in these sensors to convert the pressure input into an electrical signal. Based on these transduction mechanisms, pressure sensors can be classified as capacitive, piezoresistive, piezoelectric, optical and resonant [2, 3]. Piezoresistive pressure sensors have several advantages like small size, high linearity, high reliability and simple IC fabrication [4]. These sensors are used in applications like tire pressure monitoring system (TPMS), intracranial pressure measurement, aircraft gas turbine combustion control and chemical processing. Piezoresistive pressure sensors usually consist of four resistors (also known as piezoresistors), connected in a Wheatstone bridge arrangement, on top of a diaphragm. The diaphragm of a pressure sensor is formed by bulk micromachining of silicon using wet chemical etchants or dry etching using deep-reactive-ion-etching (DRIE). When the diaphragm of a sensor is stressed (under the influence of a pressure load), the resistance of the piezoresistors changes due to piezoresistivity. Thus, the output of the Wheatstone

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bridge gives an estimate of the pressure input. In order to estimate the output characteristics of the sensor prior to fabrication, finite element method (FEM) based tools are used. However, analytical methods help in obtaining a quick estimate of the important output parameters like sensitivity and linearity before moving on to time consuming FEM based simulations [5, 6]. The diaphragm of a pressure sensor can be assumed to be a thin plate clamped at the edges. However, the above assumption has some flaws owing to the difference in the boundary condition in a plate and in an actual pressure sensor diaphragm as shown in Fig. 1. For square diaphragm based pressure sensors, no accurate solutions are available for plate equations. Over the years various approximate solutions have been proposed in the literature for the diaphragm deflection [6-10]. The diaphragm deflection is related with the surface stresses on the diaphragm and thus is related with the output of the sensor.

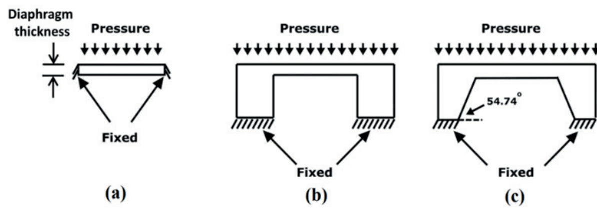


Figure 1: Cross-section and boundary conditions. (a) Plate. (b) Diaphragm etched using deep-reactive-ion-etching. (c) Diaphragm etched using wet bulk micromachining.

In this paper, we first analyze the effect of boundary conditions on deflection and stress on the diaphragm using FEM tools. Next, the accuracy of different analytical solutions of plate equations for square diaphragm available in literature is estimated by comparing them with FEM simulations of a plate. Finally, using the most accurate analytical solution, the methodology for obtaining sensitivity and linearity of the sensor is delineated.

2 Governing equations

The differential equation for a two dimensional square plate (as shown in Fig. 2) with a uniform pressure load, *P*, can be expressed as [11]:

$$D\left[\frac{\partial^4 w}{\partial x^4}+2\frac{\partial^4 w}{\partial x^2 \partial y^2}+\frac{\partial^4 w}{\partial y^4}\right]=P \quad (1)$$

where $D = Eh^3/12(1-v^2)$ is the flexural rigidity of the diaphragm, and w is the deflection of the diaphragm at (x,y). *E* is the Young's modulus of silicon, *h* is the thickness of the diaphragm, and **v** is the Poisson's ratio of silicon.

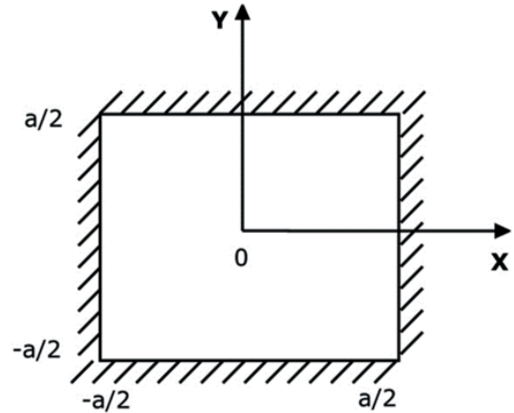


Figure 2: Schematic of a square plate.

The boundary conditions for the plate shown in Fig. 2 are as follows:

$$W\left(x=\pm\frac{a}{2};y\right)=0 \quad (2)$$

$$W\left(x;y=\pm\frac{a}{2}\right)=0 \quad (3)$$

$$\frac{\partial w}{\partial x}\left(x=\pm\frac{a}{2};y\right)=0 \quad (4)$$

$$\frac{\partial w}{\partial y}\left(x;y=\pm\frac{a}{2}\right)=0 \quad (5)$$

The solution of Eq. (1) with the above boundary conditions yields an expression for *w*(x,y). This expression can then be plugged into Eq. (6) and Eq. (7) to obtain the surface stresses of the diaphragm.

$$\sigma_x=-\frac{Eh}{2(1-v^2)}\left(\frac{\partial^2 w}{\partial x^2}+v\frac{\partial^2 w}{\partial y^2}\right) \quad (6)$$

$$\sigma_y=-\frac{Eh}{2(1-v^2)}\left(\frac{\partial^2 w}{\partial y^2}+v\frac{\partial^2 w}{\partial x^2}\right) \quad (7)$$

where $\boldsymbol{\sigma}_x$ and $\boldsymbol{\sigma}_y$ are the x- and y-directed surface stresses, respectively. In the above equations, it is assumed that the diaphragm bending is elastic and the diaphragm deflection is small compared to diaphragm thickness (less than 1/5th of the diaphragm thickness).

3 Effect of clamping conditions

The clamping conditions used in a plate rigidly clamped at all the four edges (Fig. 1 (a)) are different from those

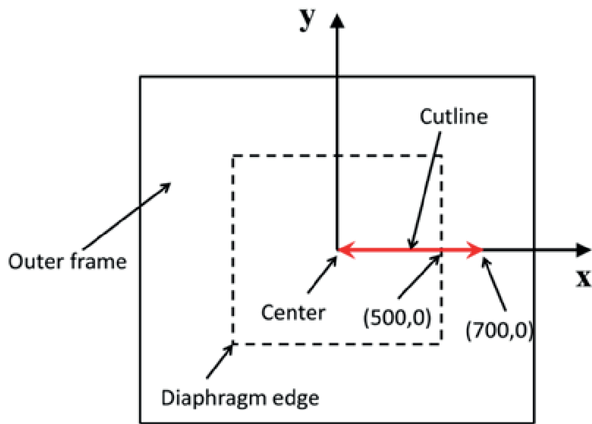
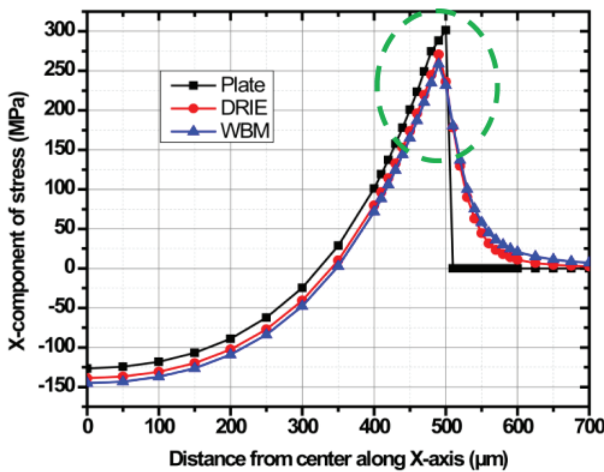
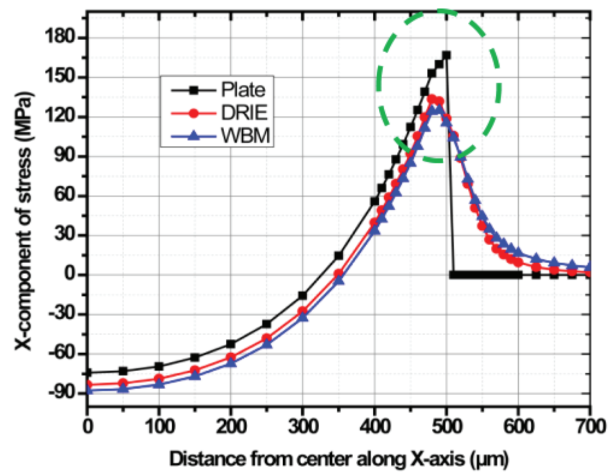
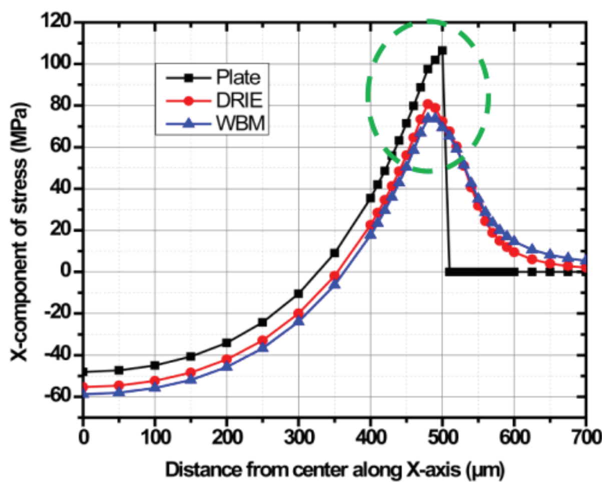


Figure 3: Top view of cutline along x-axis.

found in actual pressure sensor fabricated using DRIE and Wet bulk micromachining (WBM) as shown in Fig. 1 (b) and 1 (c), respectively. This boundary condition affects the magnitude of stress and the stress distribution on the top surface of the diaphragm where the piezoresistors are placed. In order to determine the effect of this boundary condition on the stress distribution, the x-direction stress for the three models (as shown in Fig. 1 (a)–(c)) are compared using FEM tool Coventorware. A square diaphragm of size 1000 µm x 1000 µm is used in the simulations. Simulations are performed for diaphragm thicknesses of 30 µm, 40 µm, 50 µm and 60 µm. A pressure load of 10 Bar is applied on all the diaphragms for these simulations. The x-directed stress along the cutline as shown in Fig. 3 is determined using these simulations. Fig. 4 shows the result of these simulations. It is clear from the result that the stress distribution is dependent upon the clamping conditions used for the simulations. In the DRIE and WBM model, the stress extends beyond the edge of the diaphragm (at x = 500 µm). The DRIE and WBM model show stress values close to each other in all the cases. However, it







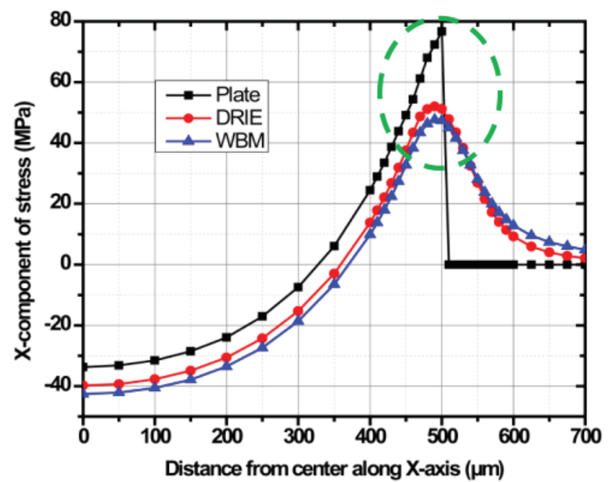


Figure 4: X-directed stress along cutline in diaphragm with different thicknesses. (a) 30 µm. (b) 40 µm. (c) 50 µm. (d) 60 µm.

can be observed that as the thickness of the diaphragm increases, the stresses near the edge of the diaphragm for the plate model is farther away from other models (as shown in the region encircled by dotted lines). This indicates that the diaphragm in a pressure sensor can be approximated by the plate model only for thin diaphragms and the plate equations can be used in such a situation. Also, the piezoresistors cannot be placed outside the diaphragm edges when plate equations are used to analyze the diaphragm as the stress fields outside the diaphragm edges cannot be evaluated. Thin diaphragms are more sensitive and less linear and the vice versa is true for thick diaphragms. For good sensitivity and linearity, diaphragm must neither be too thick nor too thin. Analytical solutions of plate equations provide sufficiently accurate solutions in this regime as they are valid in such cases.

4 Comparison of different solutions for plate equation with FEM

For the square diaphragm, many approximate solutions are available in literature. These define the deflection (*w*) of the diaphragm at a given (x,y). Some of these solutions are [6-8]:

$$w = 0.0213P\frac{a^4}{16D}\left(1-\frac{4x^2}{a^2}\right)^2\left(1-\frac{4y^2}{a^2}\right)^2 \quad (8)$$

$$w = \frac{w_0}{4}\left[1+\cos\left(\frac{2\pi\ \mathrm{x}}{\mathrm{a}}\right)\right]\left[1+\cos\left(\frac{2\pi\ \mathrm{y}}{\mathrm{a}}\right)\right] \text{where } \frac{P\left(\frac{a}{2}\right)^4}{12C_bD}, \mathrm{C_b} = 4.06 \quad (9)$$

$$w = P\frac{a^4}{16D}\left(1-\frac{4x^2}{a^2}\right)^2\left(1-\frac{4y^2}{a^2}\right)^2 \left[0.02023+0.0214\frac{x^2+y^2}{a^2}+0.1\frac{x^2y^2}{a^4}\right] \quad (10)$$

$$w = \frac{49a^4b^4p}{8D\left(7b^4+4a^2b^2+7a^4\right)}\mathrm{x} \left(\frac{1}{2}-\frac{x}{a}\right)^2\left(\frac{1}{2}-\frac{y}{b}\right)^2\left(\frac{1}{2}+\frac{x}{a}\right)^2\left(\frac{1}{2}+\frac{y}{b}\right)^2 \quad (11)$$

Sometimes, a modified differential equation as shown in (12) is used for obtaining the solution of membrane on (100) plane with edges directed along <110> direction. This equation considers the anisotropic nature of the material properties of silicon.

$$\frac{\partial^4 w}{\partial x^4}+2\alpha\frac{\partial^4 w}{\partial x^2\partial y^2}+\frac{\partial^4 w}{\partial y^4}=\frac{P}{D} \quad (12)$$

where $\alpha = \nu + \frac{2G}{E}\left(1-\nu^2\right)$ is known as the anisotropy coefficient and characterizes the anisotropy in silicon. G is the shear modulus. For a square diaphragm, some of the proposed solutions for (12) are [9-10]:

$$w = \frac{0.02126\,a^2b^2p}{16D}\left[\left(1-\left(\frac{2x}{a}\right)^2\right)\left(1-\left(\frac{2y}{b}\right)^2\right)\right]^2 \mathrm{x} \sum_{\mathrm{i=0}}^{\mathrm{n}}\sum_{\mathrm{j=0}}^{\mathrm{n}} k_{ij}\left(\frac{2x}{a}\right)^i\left(\frac{2y}{b}\right)^j \quad (13)$$

$$w = \frac{0.0224\,a^2b^2p}{16D}\sum_{\mathrm{i=0}}^{\mathrm{n}}\sum_{\mathrm{j=0}}^{\mathrm{n}} k_{ij}\cos^2\left(\frac{(2i+1)\pi\ x}{\mathrm{a}}\right)\mathrm{x} \cos^2\left(\frac{(2j+1)\pi\ y}{\mathrm{b}}\right) \quad (14)$$

where *n* is an even positive integer, *i*, *j* = 0,2,4,6,…..*n*, k_{ij} are the shape factors. The shape factors for n=4 is given in Table 1. In all the equations above, a = b, due to the diaphragm being square in shape.

Table 1: Shape factors for n = 4

	Eq. (13)	Eq. (14)
k_{00}	1	1
k_{20}	0.233	0.0284
k_{02}	0.233	0.0284
k_{22}	0.252	0.0123
k_{40}	-0.00166	0.0038
k_{04}	-0.00166	0.0038
k_{42}	0.13	0.0030
k_{24}	0.13	0.0030
k_{44}	-0.235	0.0016

The deflection of diaphragm obtained by the solutions of plate equations given by Eqs. (8), (9), (10), (11), (13), and (14) are compared with FEM solution in order to find the most accurate solution. A diaphragm size of 1000 µm × 1000 µm and diaphragm thickness of 30 µm are chosen for the comparative study. A pressure of 10 Bar is applied. Fig. 5 shows the combined plot of diaphragm deflection (along the x-axis) obtained using

different analytical equations. These solutions are compared with solution obtained using FEM. The material properties of silicon used in analytical solutions are as follows: Young's modulus (E) = 169.8 GPa and Poisson's ratio (v) = 0.066. Orthotropic properties of silicon are used in the FEM solution [12]. To find the most accurate solution, the root mean square deviation (RMSD) of each of the solution (from the FEM solution) is obtained using the following formula:

$$RMSD = \sqrt{\frac{\sum_{i=1}^{n}\left(Def_{i,Analytical} - Def_{i,FEM}\right)^2}{n}} \quad (15)$$

where n is the total number of points where the deflection is calculated on the cutline along x-axis, $Def_{i,analytical}$ is the diaphragm deflection obtained by the particular analytical solution at point *i*, $Def_{i,FEM}$ is the diaphragm deflection obtained by FEM solution at point *i*. The calculated value of RMSD is enlisted in Table 2.

Table 2: Root mean square deviation (RMSD) from FEM solution

Equation no.	RMSD
(8)	0.1994
(9)	0.2400
(10)	0.3906
(11)	0.2024
(13)	0.1414
(14)	0.1796

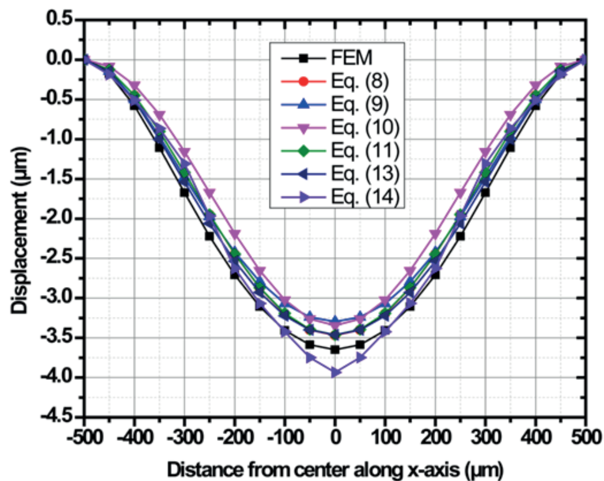


Figure 5: Comparison of diaphragm deflection obtained using different analytical solutions and FEM.

Table 2 indicates that the RMSD value obtained for Eq. (13) is the lowest. Hence, the solution given in Eq. (13) provides the most accurate picture of the diaphragm deflection for a plate and is chosen for calculating the output of the piezoresistive pressure sensor in next section.

5 Sensitivity and linearity calculations using analytical solution

Consider a pressure sensor diaphragm with four piezoresistors connected in Wheatstone bridge as shown in Fig. 6. The relative change in resistance of each resistor can be given by [13]:

$$\frac{\Delta R}{R} = \pi_l \sigma_l + \pi_t \sigma_t \quad (16)$$

where $\boldsymbol{\pi}_l$ and $\boldsymbol{\pi}_t$ are the longitudinal and transverse piezoresistive coefficients, respectively. $\boldsymbol{\sigma}_l$ and $\boldsymbol{\sigma}_t$ are the longitudinal and transverse stress, respectively.

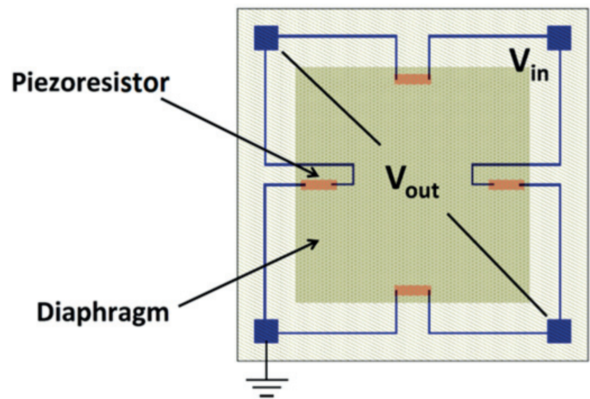


Figure 6: Top view of a piezoresistive pressure sensor diaphragm with piezoresistors.

The piezoresistors on the diaphragm have a finite size and therefore the stress on the piezoresistors must be calculated by averaging the stresses as shown in Eqs. (17) and (18).

$$\sigma_{yave} = \frac{1}{A}\int_y \int_x \sigma_y dxdy \quad (17)$$

$$\sigma_{xave} = \frac{1}{A}\int_y \int_x \sigma_x dxdy \quad (18)$$

where $\boldsymbol{\sigma}_{xave}$ and $\boldsymbol{\sigma}_{yave}$ are the average x- and y-directed stresses at the piezoresistor location, respectively. A is the area of each piezoresistor. Substituting $\boldsymbol{\sigma}_{x\,ave}$ for $\boldsymbol{\sigma}_l$ and the value of $\boldsymbol{\sigma}_{y\,ave}$ for $\boldsymbol{\sigma}_t$ in Eq. (16), we obtain:

$$\frac{\Delta R}{R} = \pi_l \sigma_{xavg} + \pi_t \sigma_{yavg} \quad (19)$$

A computer program is developed using the solution of plate equation and the change in resistance of piezoresistors on the diaphragm. The four piezoresistors are placed at the center of the edges of the diaphragm in order to experience maximum stresses. The program

calculates the stress distribution at the surface of the diaphragm using Eqs. (6) and (7) and the longitudinal and transverse stresses over the piezoresistors are averaged to find the change in resistance of each resistor. The piezoresistors are assumed to be aligned along <110> direction on (100) plane. The piezoresistors are assumed to have p-type doping, for maximum sensitivity [14]. The Wheatstone bridge is provided with an input of 5 V. The sensitivity of the pressure sensor is the relative change in the output voltage per unit change in applied pressure [6]. The pressure vs. output voltage graph is not a straight line and the nonlinearity of the sensor is calculated using an end point straight line [6]. To demonstrate the usage of analytical equations, different sensor structures with diaphragm sizes and thicknesses are chosen as shown in Table 3. A pressure of 10 Bar is applied on each of these models. Four piezoresistors are placed at the edge of the diaphragm with dimensions: 100 µm (length) × 10 µm (width). It is assumed that the contact with the resistor is made at the two ends of the resistor. Usage of analytical solutions for analyzing pressure sensor diaphragms entails that the diaphragm must neither be too thin nor too thick. The reason for the same has been explained in the earlier section. As a thumb rule, for a particular diaphragm size and thickness chosen in Table 3, the diaphragm deflection at full scale pressure is kept between $1/5^{th}$ and $1/10^{th}$ of diaphragm thickness. The sensitivity plots of the different models are shown in Fig. 7 and the non-linearity plots is shown in Fig. 8. To find the sensitivity of a particular model, the slope of the curve must be divided by the supply voltage (5 V). The non-linearity of the sensor is the maximum percentage non-linearity for the particular sensor structure. The sensitivity and non-linearity for a particular pressure range can be optimized according to requirement by varying the diaphragm size, diaphragm thickness, piezoresistor dimensions and piezoresistor placement. However, the limitations and conditions required for using analytical solutions as explained earlier must be considered during design optimization.

Table 3: Dimensions for different sensor structures (Pressure – 10 Bar)

Model no.	Diaphragm size (µm × µm)	Diaphragm thickness (µm)
1	600 × 600	15
2	800 × 800	22
3	1000 × 1000	30
4	1200 × 1200	35
5	1400 × 1400	42
6	1600 × 1600	48

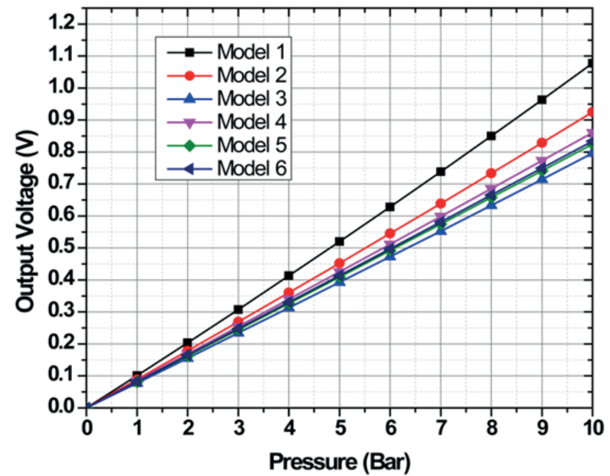


Figure 7: Sensitivity plots for different models.

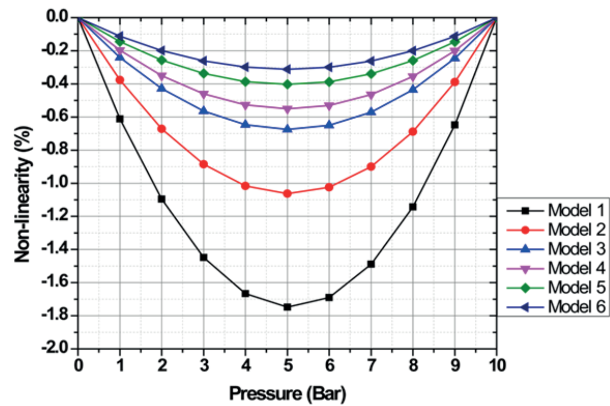


Figure 8: Non-linearity plots for different models.

6 Conclusions

This paper gives a description of the various analytical solutions of plate equation available in literature and delineates the limitation of using these solutions for modeling the diaphragm of a piezoresistive pressure sensor. However, analytical solutions of a plate can be used for obtaining the sensitivity and non-linearity of a pressure microsensor when the diaphragm is neither too thick nor too thin. The various analytical solutions are also compared with FEM solution to obtain the most accurate solution. The method for obtaining the output characteristics of the sensor using analytical equations is also explained. Using the method shown in this paper, analytical solutions can be used for the first level design and optimization of a piezoresistive pressure sensor. This may then be followed up by FEM simulations for the optimized model. Analytical methods help in saving time compared to FEM method.

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Contour Graph Approach of Micropower Clock Generator Design for Energy Harvesting Charge Pump Circuits

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Abstract: This paper presents a novel design methodology of micropower noncritical clock generator for charge pump circuits. Embedded clock generator circuit requires careful attention in terms many issues: topology choices, component sizes, power dissipation and signal voltage values. This paper also presents comparisons and performance optimization of microwatt clock generators using SPICE simulator. Additionally a contour graph approach is developed to find relevant parameters value in order to minimize the power consumption and the chip area. The circuit design was implemented on standard 0.35 µm Si CMOS process. The active area dimensions are 42 µm*25 µm. Consistent results were obtained between experimental results and transient simulations. In comparison to previous papers, under low-voltage constraints, interesting measured circuit consumption was observed: 1.15 µW from 1 V.

Keywords: Contour curve; clock generator; micropower clock; power consumption; optimization; low power; charge pump; energy harvesting

Metoda grafa obrisa za urni generator majhnih moči pri črpanju energije z okolja

Izvleček: Članek predstavlja novo metodologijo načrtovanja urnih generatorjev za črpanje energije z okolja. Vgrajeno vezje urnega generatorja zahteva posebno pozornost pri: topologiji, velikosti komponent, porabi energije in napetosti signala. Predstavljena je optimizacija in primerjava urnih generatorjev v SPICE okolju. Za zmanjšanje porabe energije je uprabljena metoda grafa obrisa. Vezje je bilo implementirano v 0.35 µm Si CMOS tehnologiji z aktivno površino 42 µm * 25 µm. V primerjavi s prejšnjimi rešitvami je bila dosežena nizka poraba energije: 1.15 µW pri napetosti 1 V.

Ključne besede: Graf obrisa; generator ure; poraba energije; energija iz okolice

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1 Introduction

Energy harvesting is becoming a practical solution to improve battery lifetime in micro-scale electronic systems for wireless sensor applications. Many research papers have been proposed to design an energy harvesting system based on a charge pump circuit [1]. Charge pumps (CPs) are circuits that generate voltages greater than the supply voltage from which they operate. Some of these circuits are based on two anti-phase pumping clocks [2]. For this charge pump circuit operation, low frequency clock generator is actually needed. Clock generator circuits are thus widely-used in CPs and are an important subpart of these systems [3,4]. In the literature, some papers have been published on their performance, where oscillators are aimed to be used as clock generators [3, 5, and 6]. In the context of energy scavenging, power consumption is a crucial issue [7]. The energetic constraint is also applied to clock generators despite the fact that it is sometimes underplayed or un-optimized. This trend is confirmed by the publications on subthreshold mode circuits [8], in which power consumption is dominated by leakage current Ioff [9, 10] and supply voltages lower than 1 V [7]. Furthermore to keep the cost low, attention should

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also be given to the chip size by introducing effective design methods.

This work compares power consumption and performance analysis of different square-wave clock generator topologies. Topologies comparison aim at selecting an appropriate low frequency clock generator topology, under low power constraint, in the energy scavenging context. This comparison is performed under some specific conditions: the energy criterion is more important than noise performance. The operating frequency is in the range of hundreds of megahertz (in accordance with charge pump circuit design concepts for energy harvesting applications [11], from 1 Hz to 100 MHz). Furthermore, the clock signal generator is designed to drive CP switches [4]. In this scheme, its output square signal amplitude should be high enough to have an appropriate voltage gate control of the CP switches. In this work, the minimum voltage level is set to V_t = 0.7 V, as the CP CMOS switches are not operating in subthreshold mode. About the supply voltage, as the clock generator will be associated with a bandgap and a charge pump circuit, the typical value that will be considered is 0.8 V. And finally in this context, the studied topologies are intended for application in highly integrated systems (consuming a reasonable silicon area), using a low-cost 0.35 µm Si CMOS process.

Many candidates are well-known in the literature: LC circuits, CMOS oscillators and crystal oscillators. Some of them are not suitable for low-cost process integration (crystal oscillators) or rather interesting for high frequency low noise applications. Some others use additional external components. Alternative topologies are interesting for the purpose of this work: the Schmitt trigger circuit, the ring oscillator and the voltage controlled ring oscillator. Some drawbacks are known, but under certain aspects of ring oscillators, they can be exploited. All, these points will be respectively presented in section 2, 3 and 4. Attention will be paid to low power consumption and frequency range in order to select one of these circuits. Section 5, will present the contour graph methodology which was used to optimize the circuit under the constraints (power, frequency, chip area). Then a power consumption comparison is performed for the different clock generator topologies at selected low frequencies. Measurement results are provided in section 6, along with the parasitics effect on power consumption offset and comparison with some publications. Section 7, finally presents the conclusions of this paper.

2 Schmitt trigger clock generator STCG

The circuit depicted in Fig. 1 is known as a multivibrator circuit, astable type. The circuit is configured around an inverting Schmitt trigger gate and a delay structure (composed of the surrounding components, R and C).

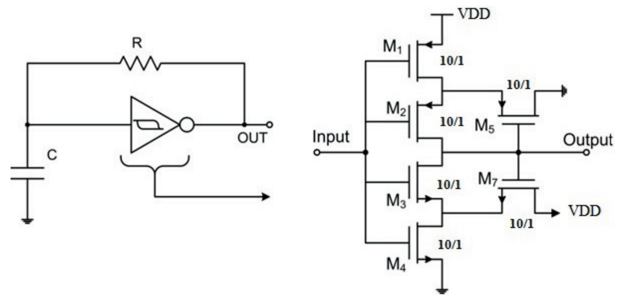

Figure 1: Schmitt Trigger Clock Generator circuit

The oscillation frequency f_o is mainly determined by the delay structure as:

$$f_o = \frac{1}{RCIn\frac{V_{high}(V_{low} - V_{DD})}{V_{low}(V_{high} - V_{DD})}} \tag{1}$$

Where, V_{DD} is the power supply voltage. Considering the upper (V_{high}) and lower (V_{low}) switching voltages (usually associated with transistors transconductance ratios), which define the hysteresis of the gate in the transfer curve: the Schmitt trigger's output is a well defined voltage, which is really suitable for noisy signal or signal cleaning functions [12].

Dynamic behavior simulations of STCG circuit have been performed using SPICE simulator and 0.35 µm Si CMOS process parameters.

The operating frequency range was simulated for different values of the delay structure (τ = R.C, Fig. 2).

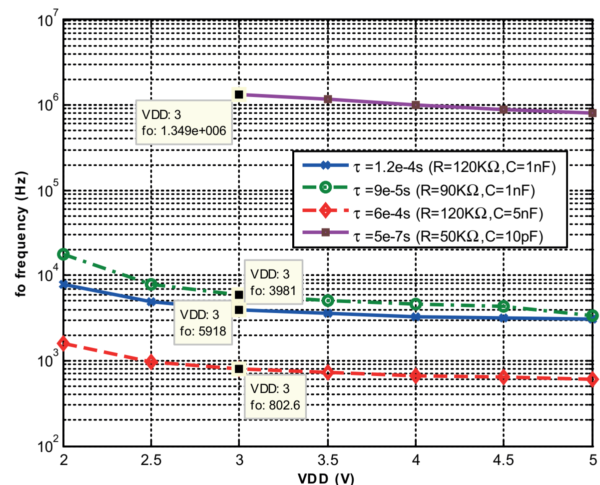

Figure 2: Simulated output frequency fo versus supply voltage (VDD) - STCG circuit

Over the frequency range of 10 Hz to hundreds of megahertz, f_o is inversely proportional to τ = R.C. The oscillation frequency range is obviously governed by the RC time-constant.

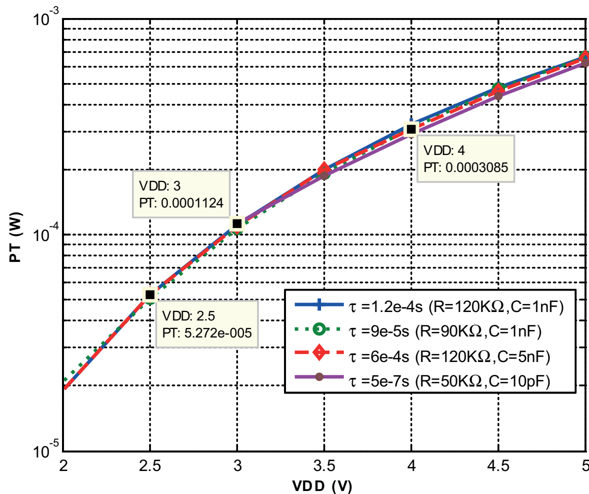

Figure 3: Spice simulated power consumption as a function of the supply voltage VDD - STCG circuit

From the power dissipation point of view, Fig. 3 displays power simulation results as a function of the supply voltage V_{DD}. From this graph, it can be seen that a fall of the supply voltage, lowers the power consumption. Also, it can be deduced that the variation of the power consumption has a small fluctuation as function of the delay structure τ.

Transient results and the theory reveal that the circuit does not work properly for a supply voltage less than 2 V. In fact, the gate hysteresis tends to disappear at this voltage level. At this lowest 2 V voltage, the total power consumption is 20 µW.

Consequently, and especially in the context of our purpose where a low power and frequency clock generator is required, this drawback (lowest supply voltage=2 V) can represent a major limitation for the use of this topology. In the next section a different topology (inverter based clock generator) is presented.

3 Ring oscillator RO

A ring oscillator (RO) (Fig. 4) consists of an odd number of inverters in a unity gain feedback loop [13]. To achieve oscillation, the circuit must satisfy the Barkhausen's criterion which means that the total phase shift and the gain of the feedback loop must be 2π and one respectively [14].

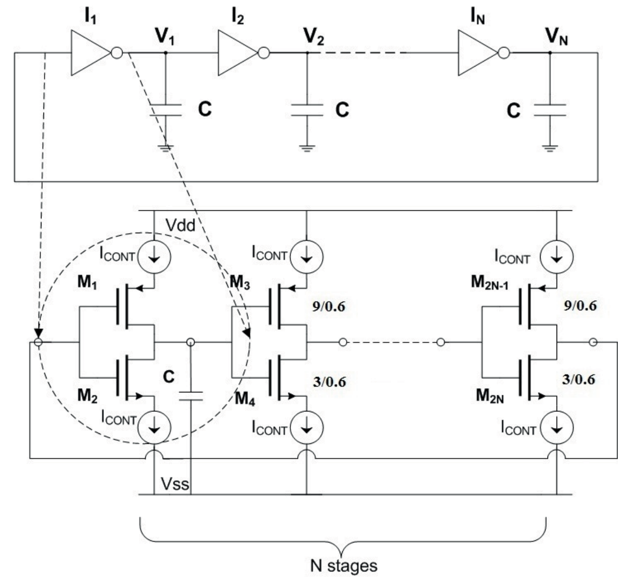

Figure 4: Ring Oscillator circuit and additional C capacitors

To design oscillators whose output frequency ranges from 1 Hz to 100 MHz, a ring structure of three stages is chosen. C capacitors have also been included to lower the output signal frequency to meet the custom specifications of charge pump circuits.
Instead of C addition, we could have chosen a greater number of stages. In terms of output frequency value and power consumption, this is not compatible with our application (supply voltage value of 0.8 V and low power circuit) as depicted in Table 1.

Table 1: RO clock generator frequency as a function of V_{DD} and the inverter stage number without capacitors

V_{DD} (V)	3 stages	5 stages	7 stages
0.8	18.45 MHz	10.54 MHz	7.65 MHz
1	115.5 MHz	63.1 MHz	44.55 MHz
1.5	257 MHz	191 MHz	114.5 MHz

Theoretically, the frequency of the oscillation can be found as:

$$f_o = \frac{1}{2N\tau_{inv}} \quad (2)$$

Where N is an odd number and τ_{inv} is the propagation delay of one inverter stage. The delay of each inverter stage will be given by:

$$\tau_{inv} = \frac{V_o C_{in}}{I_{CONT}} \; avec \; V_o = \int \frac{I_{CONT}}{C_{in}} dt \quad (3)$$

Where, V_o is the voltage signal amplitude, I_{CONT} is a DC control current source (Fig. 4) and C_{in} the equivalent input capacitor of the following inverter (intentional ad-

dition (C) and MOS transistors parasitics). The expression of the frequency becomes [15]:

$$f_o = \frac{I_{CONT}}{2NV_oC_{in}} \quad (4)$$

It is known that the delay of each stage is governed by the supply voltage V_{DD} and the capacitors value, C. This dependence can be verified by simulations of the frequency performance and power consumption (Fig. 5 and Fig. 6). These parametric simulations (sweep on C) are performed as a function of V_{DD}.

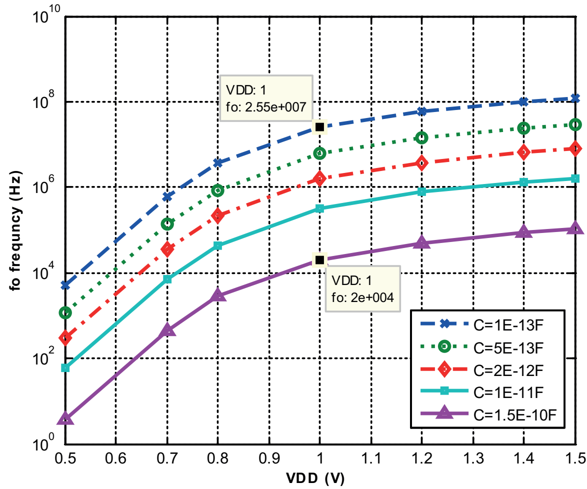

Figure 5: Simulated output signal frequency (fo) as a function of the supply voltage V_{DD} and C capacitor value, RO circuit

In Fig. 5, considering the V_{DD} range between 0.5 V and 1.5 V, the output frequency ranges from 10 Hz to 1 GHz. But referring to section 1, the lowest supply is limited to 0.7 V in order to ensure the charge pump correct operation. In the same context, considering the lowest voltage limit, the real performances range from 500 HZ to 1 GHz. Furthermore, taking into account additional circuits which should be included in the global charge pump circuit (bandgap and charge pump circuit), the supply voltage must be greater than 0.8 V and below 1.5 V. In this voltage range, referring to Fig. 5, we can see that suitable capacitor values to generate a 20 kHz signal (at 1V as supply voltage) are in the order of 1.5×10^{-10} F. This can be a drawback for the chip size.

About of power consumption, Fig. 6 reports power simulations as a function of the supply voltage V_{DD} and capacitor C. Power consumption decreases naturally with the reduction of the supply voltage. In contrast, the simulations reveal that the capacitors value C, is not explicitly related to power in this circuit. For purpose of comparison, when the supply voltage value is 1 V and for an output signal of 20 kHz, this circuit has a consumption power of 9 µW. At the end of this section, it has been remarked that to obtain the required operating frequency range, additional capacity must be included or greater number of stages must be designed. These points are disadvantages for the chip area. Therefore, the next paragraph will discuss a third topology of clock generators.

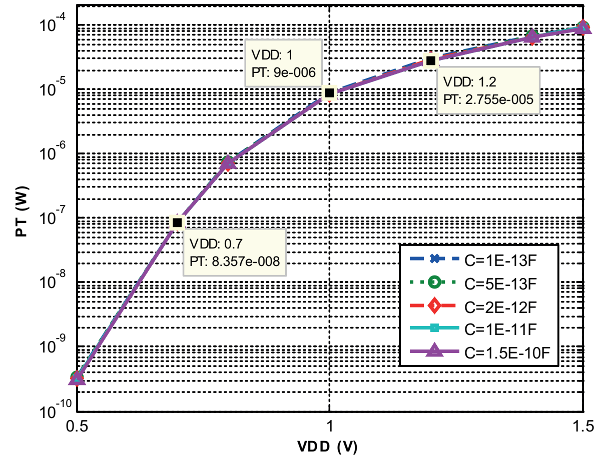

Figure 6: Simulated power-V_{DD} curves over a range of capacitor value, RO circuit

4 Voltage controlled ring oscillator VCRO

Since the limitations and drawbacks of the previous topologies the voltage-controlled ring oscillator (VCRO) will be opted to meet the custom performances (frequency, power and area) of the charge pump design. Different schemes can be used for controlling the circuit. Compared to the RO circuit, a voltage-controlled ring oscillator (VCRO) commonly uses variable voltage source to control its oscillation frequency (the possibility to adjust the clock frequency is obviously a strong point). Tunability of the VCRO is implemented via a variable resistance in the circuit. Theses resistances are designed using a transmission gate (Nmos-Pmos transistors), where the MOS transistors are controlled by their gate voltage. This topology (Fig. 7) was firstly proposed by Retdian [15] in order to improve the output voltage swing. Compared to Fig. 4, this circuit is also composed of three stages to satisfy some criteria. Among these criteria: the output frequency and the power consumption. Each stage includes one inverter (namely INV_i in Fig. 7, consisting of MP_{INVi} and MN_{INVi} transistors) and one transmission gate (namely TG_i, made up of MP_{TGi} and MN_{TGi}). The voltage V_{CONT} applied on transmission gates enables the resistance tuning. The result being as expected, a control of the output frequency, which can be given as:

$$f_o = \frac{1}{2NC_{in}\left(R_{in} + R_{TG}\right)} \quad (5)$$

Where: R_{IN} is the inverter equivalent resistance, and R_{TG}, the transmission gate equivalent resistance. C_{in} is the equivalent input capacitor of the following inverter (the sum of the MOS transistors parasitic capacitors).

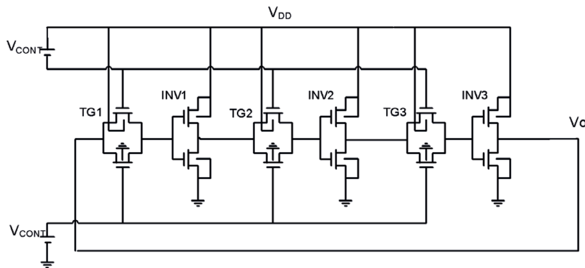

Figure 7: Voltage Controlled Ring Oscillator circuit, VCRO

5 VCRO performance optimization using contour graph approach : power, frequency and area

5.1 Contour graph approach

The contour graph approach is a good graphical tool for representing spatial relations between two variables. In addition, a contour line or isoline (often, is just called a « contour ») is a curve that joins points of equal values. Plotting these contours forms a map called a contour map.

Hence, considering the VCRO candidate, electrical and geometrical characteristics can be optimized, to find a minimum power dissipation point [16] using this contour graph approach.

In order to apply this approach and evaluate the the power dissipation and frequency behaviors, simulations are performed as a function of V_{DD}, V_{CONT} and W/L transistor ratios.

To go further, once V_{DD} and V_{CONT} have been fixed to their typical value (0.8 V),_concerning the transmission gates and the inverters of VCRO: the W/L transistor ratio (which is assumed to be identical for each electronic sub-function), have an impact on the optimal operation point. Fig. 8, 9, 10 and 11 show their influence on isopower dissipation and isofrequency graphs.

First focusing on MP_TG and MN_TG transistors, frequency performance and power dissipation are studied for a set of values of W/L ratio. Contours of Fig.8 and 9 demonstrate that frequency performance and power dissipation are mainly dependent on MP_TG transistors.

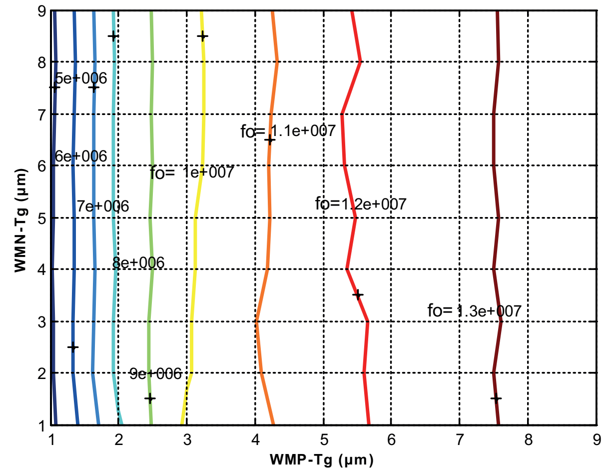

Figure 8: Isofrequency curves versus TG transistors width (MP_TG, MN_TG), VCRO circuit

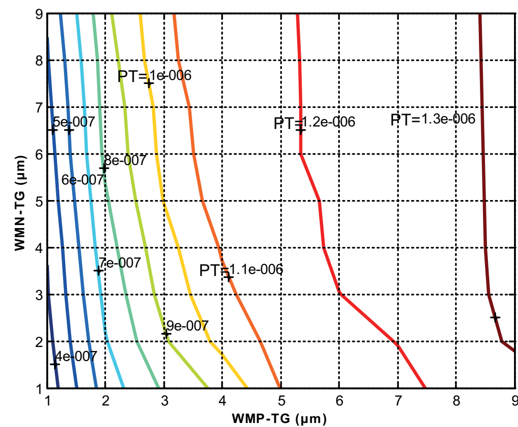

Figure 9: Isopower consumption (PT) versus TG transistors width (MP_TG,MN_TG), VCRO circuit

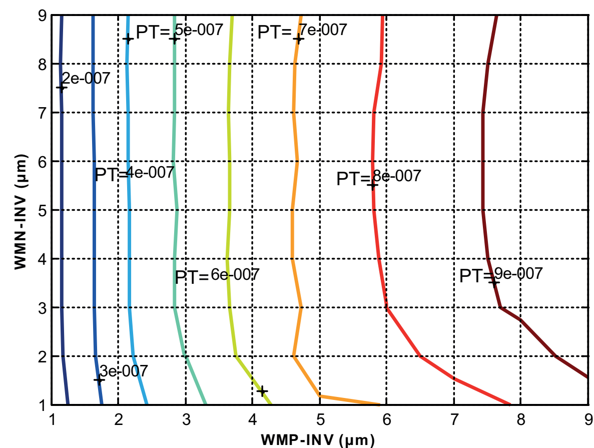

Figure 10: Isopower consumption curves versus IN transistors width (MP_INV, MN_INV) - VCRO circuit

Now, regarding the inverters and the effect of W/L transistor ratio: power dissipation and frequency performance are given respectively in Fig. 10 and Fig. 11 for MP_INV and MN_INV transistors.

It appears that the variation of power dissipation has a rather small fluctuation compared to MP_TG and MN_TG impact on the power dissipation (Fig. 10). About Fig. 11, MP_INV and MN_INV transistors have roughly the same impact on frequency performance.

Previously, we saw that C capacitors in ring oscillators didn't change power dissipation (Fig. 6). Consequently, it can suggest that inverter transistor dimensions (MP_INV, MN_INV) mainly contribute to the overall equivalent capacitance.

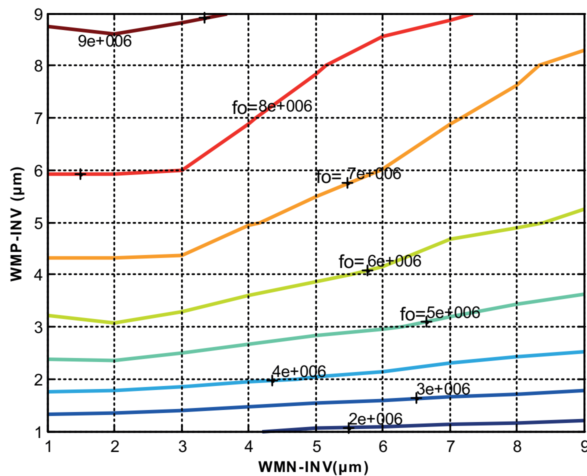

Figure 11: Frequency performance versus IN transistors width (MP_INV, MN_INV) - VCRO circuit

About the conclusions of this approach: these curves indicate that power dissipation is dominated by MP_TG transistors (as depicted by the vertical parts). A power optimization method can firstly consist of sizing of MP_TG transistors, based on energy resources. And secondly the desired frequency performance can be adjusted using the W/L ratios of MP_INV and MN_INV transistors. This methodology can save time for low power and low frequency oscillator with small size devices. In the purpose of our work, the operating frequency of the charge pump is in the range of tens of megahertz. By using this contour graph method (Fig 8, 9, 10, 11), the following sizes were selected to generate the required frequency.

Table 2: Selected CMOS transistors sizes - VCRO (V_{DD} = V_{CONT} = 0.8 V)

Transistors	W/L (µm)
MP_INV	9/0.6
MN_INV	4.5/1.2
MP_TG	3/0.6
MN_TG	1.5/1.2

For the given parameters of transistors, in order, to study the evolution of the power dissipation and frequency characteristics as a function of V_{DD}, V_{CONT} Fig. 12 and 13 show contour graphs representing lines of equal frequency and power (isofrequency and isopower graphs). In these simulations, the points that are located under the line defined by V_{DD} = V_{CONT}, should not be considered, as this means that $V_{DD} < V_{CONT}$. In this case, additional circuits are needed to generate negative voltages for the TG transistors. That's the reason why we will consider $V_{DD} > V_{CONT}$.

Concerning the frequency performance (Fig. 12), the output frequency (f_o), doesn't depend strongly on V_{DD} as denoted by the vertical parts. Reading the isolines of Fig. 13, power dissipation varies between 0.1 nW and 10 µW. For a given value of V_{DD} while V_{CONT} is increasing, we note that the power dissipation increases too.

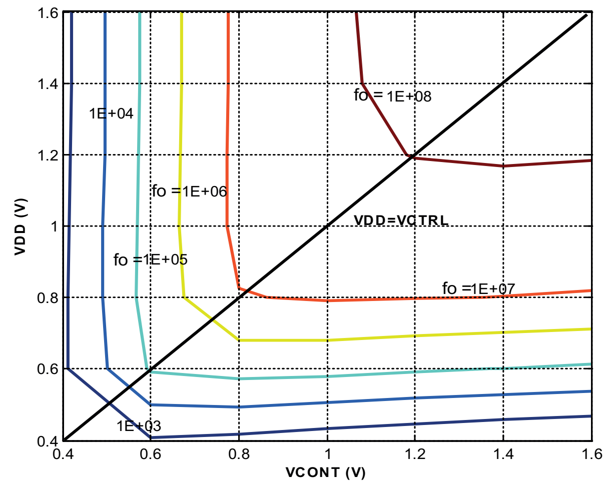

Figure 12: Simulated isofrequency contour graphs (fo) as a function of V_{DD} and V_{CONT}, VCRO circuit

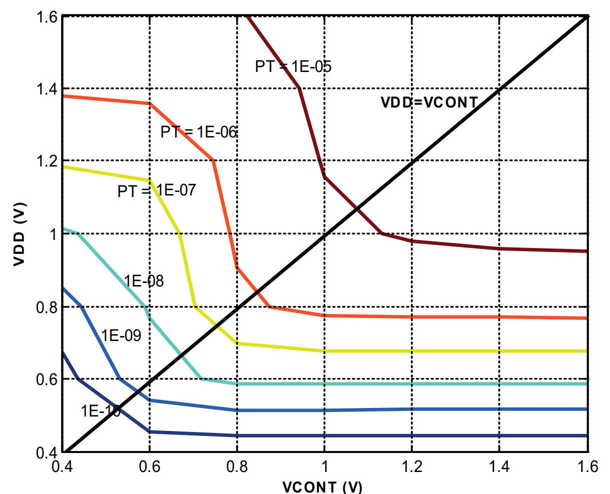

Figure 13: Constant power dissipation contour graphs simulations (PT) as a function of VDD and VCONT, VCRO circuit.

In order to operate to a specific frequency f_o (which depends on the CP topology) and at the minimum power dissipation, V_{DD} and V_{CONT} should be the lowest with respect to the application requirements. The optimal operating point can be extracted from these curves, which are useful for circuit design. The optimal operating point is the voltages (V_{DD} and V_{CONT}), which give the minimum power dissipation for a desired output frequency.

V_{DD} and V_{CONT} can be chosen independently. But Fig. 14 pictures the impact of the difference between the two voltages: power dissipation as a function of $V_{DD} - V_{CONT}$ for different output frequencies. These results clearly show that the optimal point is achieved when $V_{DD} = V_{CONT}$.

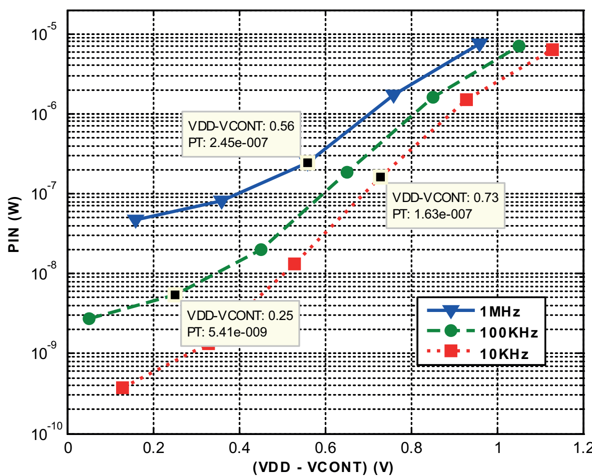

Figure 14: Power dissipation (P_T) as a function of V_{DD} - V_{CONT} for three frequencies, VCRO circuit

5.2 Validation of the approach and comparisons results

In order to evaluate the VCRO performance and the design approach, and for the purpose of comparison with previous clock generators (STCG, RO), the frequency and power performances (Fig 15 and16) have been investigated.

On Fig. 15, the output frequency is plotted as a function of V_{CONT} at a supply voltage of 1 V. For control voltage (V_{CONT}) between 0.1 V and 1 V, this topology achieves a tuning frequency range from 20 Hz to 36.6 MHz. This frequency range is reached using a reasonable silicon area as no additional capacitors are needed

Concerning the power dissipation (Fig. 16) the total power dissipation in CMOS circuits comes from two parts [17]: static and dynamic power.

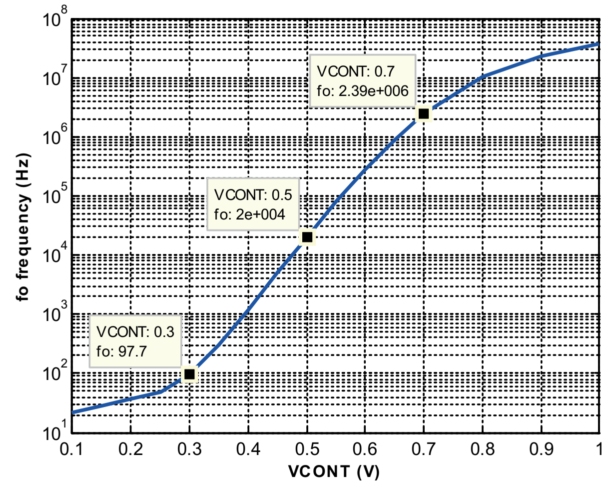

Figure 15: Output frequency simulation as a function of V_{CONT}, V_{DD} = 1 V, VCRO circuit

$$P_T = \underbrace{I_S V_{DD}}_{Statics} + \underbrace{aC_{out} V_{DD}{}^2 f_o}_{Dynamic} \tag{6}$$

Where, ***Is*** the total current leakage, ***a*** is the activity factor, $\boldsymbol{C_{out}}$ is the total output switching capacitance and $\boldsymbol{f_o}$ the clock frequency. Dynamic dissipation has theoretically been far greater than static power. This issue is also true for this circuit as proved in Fig. 16

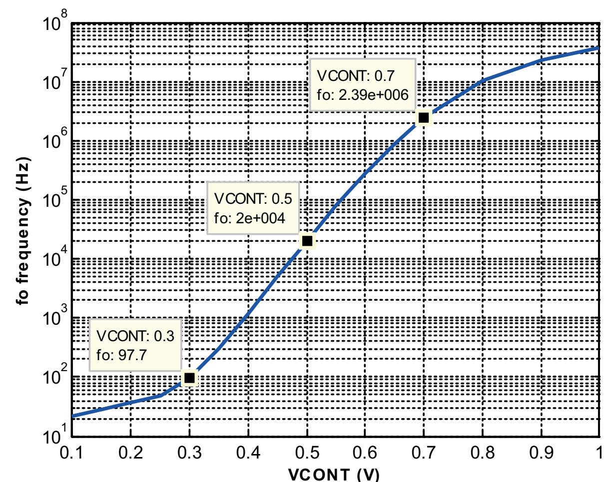

Figure 16: Simulated frequency dependence of power consumption (P_T), VCRO

In the same manner (in view of eq6), on Fig. 17, the total simulated power consumption, P_T, is reported as a function of V_{CONT} at V_{DD} = 1 V. Dynamic power dissipation increases with high V_{CONT} values. And as in some way Fig. 15 and 17 have shown that V_{CONT} and the output frequency has identical trend, it should be noticed that low V_{CONT} values cannot be used in the frequency range of interest. Thus in the useful range of V_{CONT} (V_{CONT} <0.35 V), dynamic dissipation dominates the total power consumption.

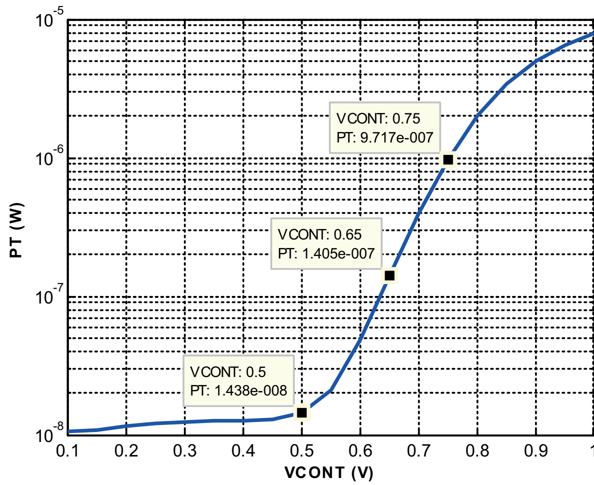

Figure 17: Simulated power dissipation (P_T) as a function of V_{CONT}, V_{DD} = 1 V, VCRO circuit

For the purpose of comparison, this circuit has a power consumption of 14.38 nW (Fig. 17) at V_{DD} = 1 V and V_{CONT} = 0.5 V. In this case the output frequency is 20 kHz.

These data (summarized in Table 3) tend to indicate that the VCRO reaches the lowest power dissipation for the operating ranges under consideration (frequencies, voltages). Indeed, the latter exhibits a typical 14.38 nW power dissipation, one decade below the others.

Table 3: Typical simulated power dissipations of the CMOS clock generators @ 20 kHz

VCRO	RO	STCG
P_T = 14.38 nW	P_T = 9 µW	P_T = 20 µW

6 Experimental results and discussions

In order to verify and validate the system operation for low frequency and low power power clock applications, a three stages voltage controlled ring oscillator was implemented using AMS 0.35 µm Si CMOS technology. Fig. 18 shows the microphotograph of the circuit. The VCRO occupies a small effective area of 1050 µm^2, where its dimensions are 42 µm x 25 µm.

This section also describes the measured results for the power dissipation and output frequency of the VCRO. Fig. 19 compares the simulated and measured power dissipation as a function of V_{CONT} at a supply voltage of 1 V. As seen the measured power dissipation increases with the voltage control as mentioned earlier. The trends are nearly the same. We note, however, an offset between the simulated and measured power consumption. Our analysis of the mismatch, of the circuit and the layout, took us to an assumption:

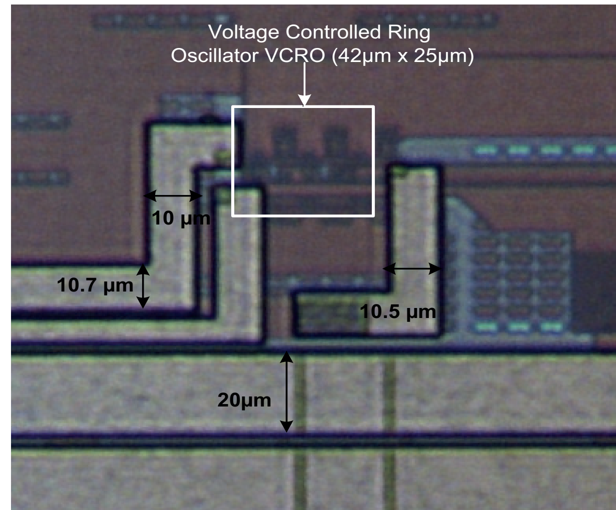

Figure 18: Die photo of the VCRO circuit using AMS 0.35 µm Si CMOS technology - active area: 42 µm x 25 µm

the effect of parasitics (resistances and capacitances) associated with metal wires, bonding pad and bonding wires. Indeed, in the context of the charge pump circuit, VCRO is not intended to be connected to any lead frame in an individual package. Among the possible parasitics, as we have two output bonding pads, we decided to include two capacitances to the circuit (Fig. 20), as it could change the output frequency and consequently the power consumption. Furthermore, about the interconnecting metal wires: their resistance can be neglected considering their short lengths and actual widths (Fig. 20).

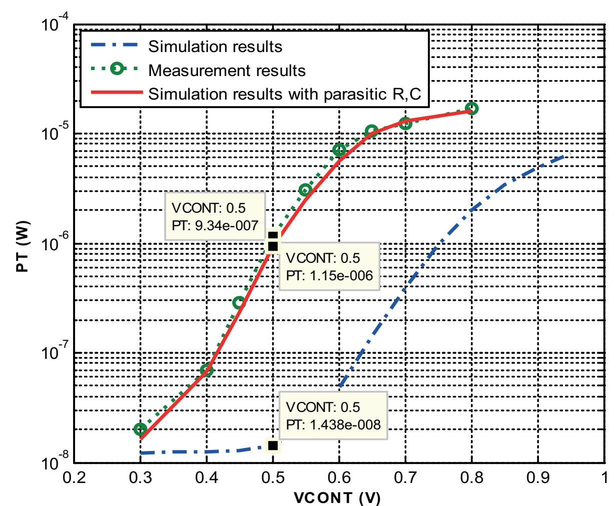

Figure 19: Measured and simulated power consumption as a function of V_{CONT} @VDD = 1 V.

Thus, new simulations were computed with the addition of C capacitors and their series resistors. As pictured in Fig. 19, a good match can be observed be-

tween the corrected measurements and prediction given in the previous section.

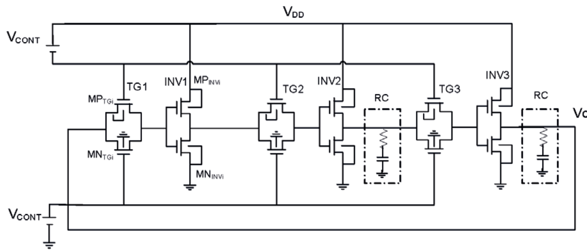

Figure 20: VCRO and the effect of selected parasitics

The second experiment (Fig. 21) aims at comparing the simulated and measured output frequency as a function of V_{CONT} and the supply voltage. These curves were obtained for V_{DD} ranging from 1 V to 2 V and V_{CONT} from 0.4 V to 0.65 V. Through these curves, we see that the frequency increases with the voltage control and also increases as the supply voltage increases too. Good agreement are observed.

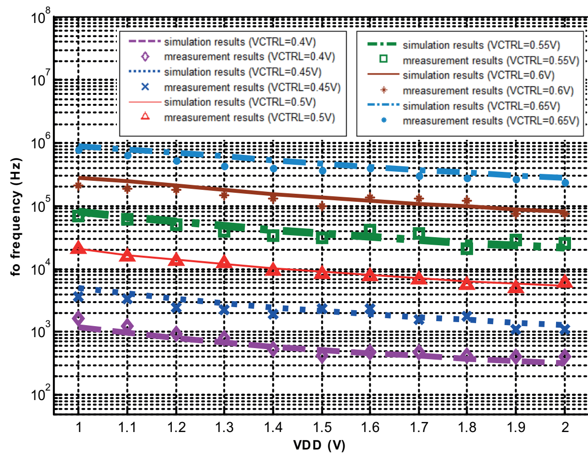

Figure 21: Measured and simulated output frequency as a function of V_{DD} and V_{CONT}

A summary of the performances of this circuit is presented in table 4.

To demonstrate the advantages of the proposed design, Table 5 reports performance comparisons between the VCRO circuit and others comparable designs which have been already reported in the literature.

Table 4: Simulated performances of the VCRO

Parameters	Values
Supply voltage	0.4 V-1.6 V
Control voltage range	0.4 V-1.6 V
Frequency range	400 Hz-190 Mhz
Power consumption range	25.23 pW-79.5 µW
Area of layout	1050 µm^2
Technology	AMS 0.35 µm CMOS

As observed the VCRO has very low power consumption with the lowest silicon area. A further advantage is that the VCRO circuit can be fully integrated, as it does not require any external components, compared to other circuits presented in Table 5.

Referring to section 5 and table 2, the frequency of oscillation of the VCRO while V_{DD} = 1 V and V_{CONT} = 0.5 V is around 20 kHz. Thus, Fig. 22 shows the transient simulation response for this frequency. In this typical condition, Fig. 23 illustrates the measurement output waveform of the VCRO oscillating at 18.62 kHz and exhibits the good agreement between simulation and experimental waveforms. Voltage level is also suitable for the charge pump CMOS switches control.

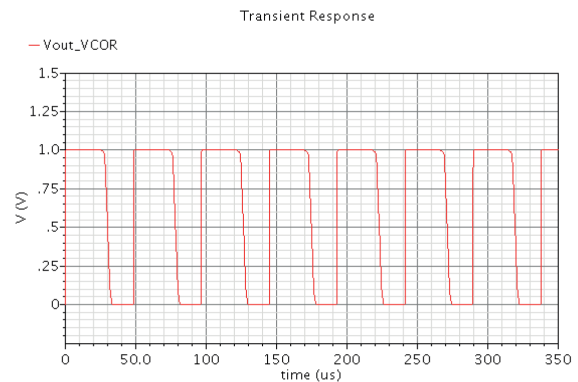

Figure 22: Simulated transient voltage of the VCRO, V_{DD} = 1 V, V_{CONT} = 0.5 V (F_{osc} = 20 kHz)

Table 5: Measured performances comparison with other designs

	[3]	[5]	[6]	[13]	[18]	This work
Supply voltage (V)	0.8	2.5	1.25	1.25	1	1
Power consumption (µW)	0.62	5.9	1120	810	52	1.15
Frequency (Hz)	50E3	34.6E3	6E6	200E3	100E3	20E3
External components	no	yes	yes	no	yes	no
Area (mm^2)	0.24	0.1	0.14	0.032	0.09	0.01050
Technology(µm, CMOS)	0.35	3	0.18	0.35	0.35	0.35

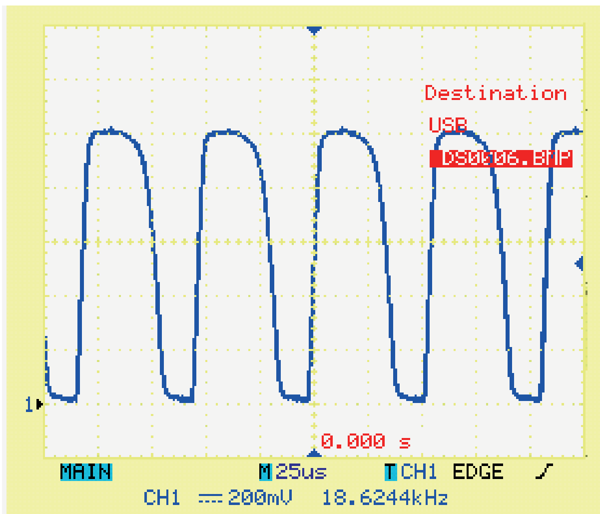

Figure 23: Measured VCRO output waveform V_{DD} = 1V, V_{CONT} = 0.5 V (18.62 kHz)

7 Conclusions

Through the preceding realizations and analysis, this work has examined power dissipation for three CMOS clock generator circuits. It has shown that the voltage controlled ring oscillator achieves the lowest power consumption for moderate frequency. Its silicon area on the chip is really interesting (1050 µm^2), which is significantly smaller than comparable clock generators. In comparison with others, another strong point was also studied: for the power consumption estimation, nanowatt values are observed. It can be less than 15 nW.

The simulation results also show that the VCRO exhibits a wide frequency tuning range, with good transient characteristics, both at high and low frequencies. This is usually difficult to obtain from the conventional generators.

Complementary simulations have shown the effect of input voltages (V_{DD}, V_{CONT}) and transistors sizes scaling (W/L ratios), on power and frequency performances. The optimal point is guaranteed when the V_{DD} = V_{CONT} relation is verified. Another important point is that, MP_TG transistors of VCRO, dominate the power dissipation and the frequency performance. From the same complementary simulations, contour graphs were drawn in order to find the optimal voltages and dimensions. These results are valuable information for the design of low power VCRO clock generator circuits.

Finally, to validate this approach, the VCRO circuit has been fabricated using AMS 0.35 µm Si CMOS technology. Output signal path parasitics has been considered for the power consumption measurements. A close agreement between simulation and experimental data is obtained, which testify the performances of the VCRO circuit for lower power systems and energy harvesting applications.

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