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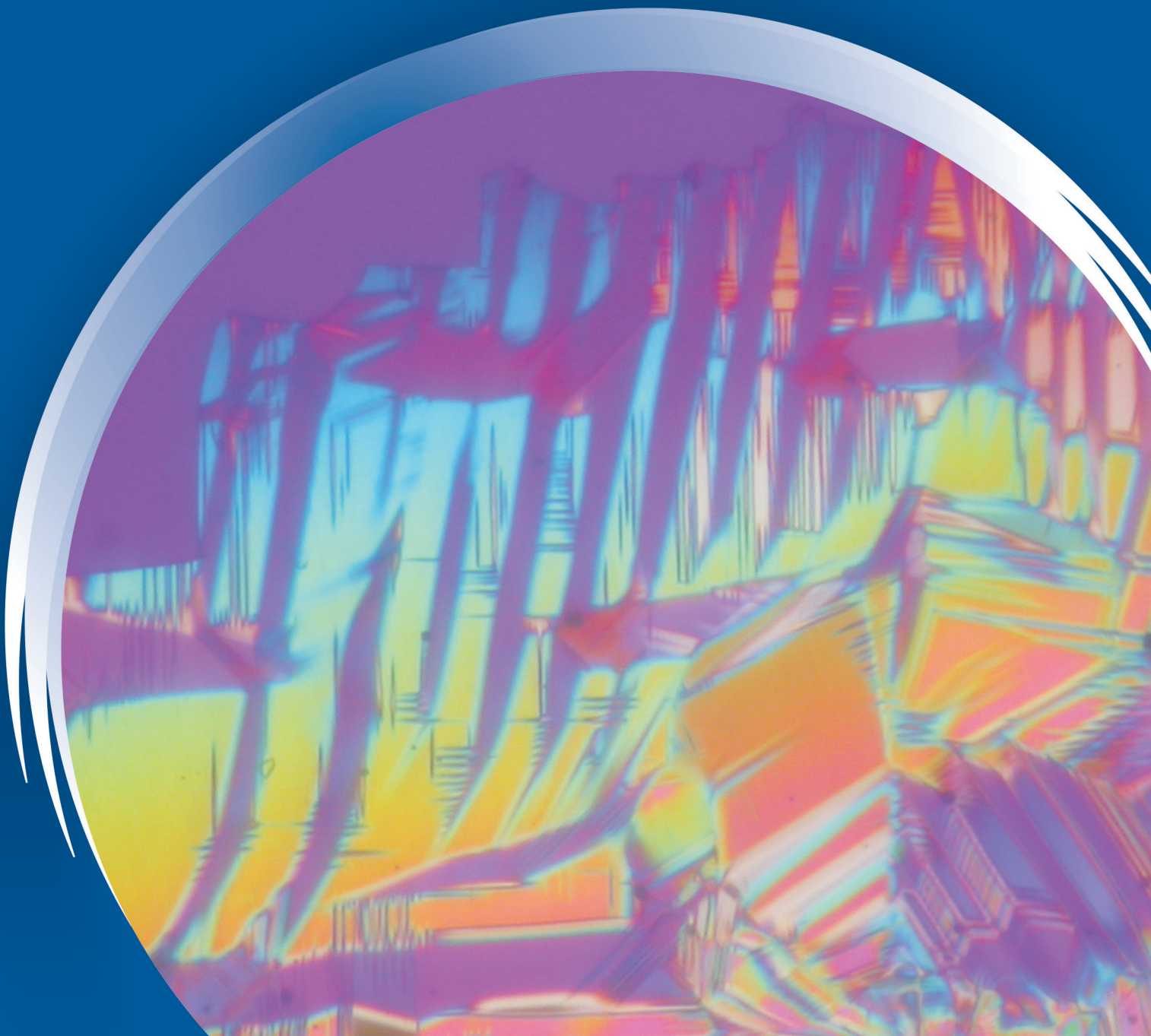

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This issue is devoted to the late Professor Marija Kosec.

Prof. Dr. Marija Kosec
(1947 – 2012)

»…Prof. Marija Kosec has been a shining star on the sky of Slovenian Science and Research…«
Prof. Marko Topič, the President of the MIDEM Society on 4th Jan 2013

Professor Marija Kosec, or Marička, as almost everyone called her, was born on the 5th September 1947 in Šinkov turn, Slovenia. She graduated in 1970 in chemical technology, received her MSc in 1975 and her PhD in chemistry in 1982 at the University of Ljubljana, Slovenia, under the supervision of Professor Drago Kolar. The topic of her Master Thesis was lead-free piezoelectric sodium potassium niobate, which, after being almost forgotten for about 25 years, became extremely popular with the revived interest in environment-friendly lead-free piezoceramics. Her doctoral thesis involved the study of phase relations in calcium uranate systems and within this period she mastered the techniques of thermal analysis.

Since 1971 she was employed at the Jožef Stefan Institute (JSI), Ljubljana, Slovenia, and in 1997–2001 she was the Head of the Ceramics Department followed by being the Head of the Electronic Ceramics Department (2002–2012). In 2007–2009 she was the President of the Scientific Council of Jožef Stefan Institute. In 1993 she was a visiting scientist at the Ceramics laboratory of Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland. In the years 2004–2009 she was also the Director of the Slovenian Centre of Excellence "Materials for electronics of next generations and other emerging technologies", and in the period 2009–2012 of the Centre of Excellence "Advanced Materials and Technologies for the Future" (NAMASTE).

Since 1999 she was Professor of Materials Science at the University of Ljubljana, with courses at graduate and post-graduate level. She was active in the Jožef Stefan International Postgraduate School since its establishment in 2004 as its Vice-President. She was a visiting professor at Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland, Shizuoka University, Japan, and for shorter periods at a number of other universities and institutes. She was Adjunct Professor at Xi'an Jiaotong University, China. She was an inspiring advisor to many PhD students at the University of Ljubljana, the Jožef Stefan International Postgraduate School and the University of Oulu, Finland.

She served as a member or chair of many scientific societies, committees or advisory bodies both in Slovenia and abroad. In the period 2005–2006 she was the President of the Slovenian Academy of Engineering. Since 1999 she was a member of the European Liaison Committee of International Microelectronics and Packaging Society (IMAPS). In 2001 she became a member of the Ferroelectrics Committee at IEEE.

Professor Kosec was a very active and strong supporter of the Society for Microelectronics, Electronic Components and Materials (MIDEM Society) and its long-term member. In the years 1996-2005 she was the President, and in the periods 1989-1996 and 2005-2011 the Vice-President.

In recognition to her achievements she was awarded the title Ambassador of Science of the Republic of Slovenia (2003), she was a recipient of the Zois Award, the highest national science award (2006), and of the Puh recognition for the implementa-

tion of research results in industry in 2009. In 2010 she received the Ferroelectrics Recognition Award from IEEE Ultrasonics, Ferroelectrics, and Frequency Control Society for her significant contributions to the processing science and technology of ferroelectric powders, bulk ceramics, thin and thick films.

The research work of Prof. Kosec was on synthesis and processing of ceramic materials for electronics, especially ferroelectrics and piezoelectrics. She established strong collaborations with researchers from complementary fields, especially from solid-state physics and electronics both in Slovenia and around the world. Her contribution was in better understanding and consequently controlling the synthesis of complex perovskite materials in solutions, colloidal systems, by mechanochemical activation or reactions in solid state.

It is worthwhile to note the highly technologically demanding processing of transparent electrooptically active lead lanthanum zirconate titanate bulk ceramics, which she undertook in the frame of a military project together with colleagues from the Condensed Matter Physics Department within JSI, in 1980s'.

In 2001 the group of Prof. Kosec took part in the first European framework project on environment-friendly lead-free piezoceramics based on alkaline niobates. Her first publication on sintering of sodium potassium niobate from 1975, which had been her Master degree topic, eventually became the seminal paper on sintering of this still not thoroughly-understood material. Together with the colleagues from the Condensed Matter Physics Department she discovered a new group of lead-free relaxors. In the frame of a European project, the group prepared for the first time single crystals of sodium potassium niobate by solid state crystal growth with piezoelectric properties exceeding those of the polycrystalline counterpart.

Research of ferroelectric thick films (thickness range of a few 10 μm) is among the notable achievements of Prof. Kosec and her group. In 1992 the German printing company MAN Roland Druckmaschinen patented the process of ferroelectric printing and in order to prove the concept, ferroelectric thick films with the thickness of a few 10 μm with almost theoretical density were needed. At that time there was almost no knowledge on ferroelectric thick films processing. Professor Kosec and her colleagues succeeded to process the films with required materials and functional properties and patented the processing of such films. Integration of ferroelectric and piezoelectric thick films on different substrates was later the topic of a number of European framework projects. The development of integrated medical ultrasound transducer in collaboration with colleagues from the University François-Rabelais, Tours, France, and pressure sensors with Slovene companies HIPOT RR in HYB should be also noted.

In the field of Chemical Solution Deposition (CSD) of ferroelectric $Pb(Zr,Ti)O_3$ thin films (i.e., with thicknesses of a few 100 nm) she addressed together with her colleagues the problem of chemical homogeneity on sub-nanometre scale. The exceptional practical outcome of this work from more than 10 years ago was in major lowering of the crystallization temperature of the perovskite phase from the usually reported 600-650 °C to as low as 400 °C, which is today still among the lowest reported crystallization temperatures. The value of this achievement lies in the easier integration of thin films into electronic components where temperature plays an important role. Due to the expertise in CSD of ferroelectric thin films the group of Professor Kosec collaborated in European framework projects on microwave phase shifters based on tunable ferroelectric thin film, thin film capacitors with exceptionally high dielectric permittivity and thin films and 2D-structures for oxide based transparent electronic components. Only a few years ago the extremely large electrocaloric temperature change in lead lanthanum zirconate titanate thin films was confirmed by direct measurements in collaboration with colleagues from the Condensed Matter Physics Department within JSI.

Professor Kosec was author or co-author of more than 300 scientific papers in international journals and of about 15 chapters in books. She gave more than 150 invited talks at international conferences and at different research institutions including Max Planck Institut, MIT, Tokyo Institute of Technology, and she was extremely proud of having the opportunity to visit and give lectures at important Japanese producers of electronic components including Murata, TDK, Panasonic and Toshiba.

She endeavored to connect the basic research with the applied research, development and industry. She was principal investigator of more than 40 contracts with industry, she lead or collaborated in more than 20 European framework programme or other international projects. Together with her colleagues she wrote more than 160 technical reports, eleven national patents, one European and one US patent. To strengthen good collaboration between academia and industry she organized or supported organization of different meetings where knowledge and skills from both parts could merge.

In September 2012 Professor Kosec was the chair of the 48th International Conference on Microelectronics, Devices and Materials with the Workshop on Ceramic Microsystems; however, due to the fast progressing of her illness she could not take active part in this very successful event. She died only a few months later, on December 23, 2012.

Her optimistic approach to life in general and to her research in particular, her sharp mind and her extensive background knowledge, her sincere interest in people and her generous heart are missed.

Prof. Barbara Malič
Electronic Ceramics Department
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Ljubljana, Slovenia.

Original scientific paper

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Characterisation of thick-film resistors as gauge sensors on different LTCC substrates

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Abstract: A thick-film resistor can sense mechanical deformations in C-MEMS structures. The relatively low elastic moduli of LTCC ceramics, compared to alumina ceramics, would suggest an increased sensitivity of the sensing elements. Selected thick-film resistors (Du Pont 2041 and ESL 3414) were evaluated as piezo-resistors for force sensors. The resistors were screen printed and fired on various LTCC tapes (Du Pont 951, ESL 41020, Heraeus HL 2000, Ferro L8 and Heraeus CT 702) as well as on alumina substrates. The LTCC tapes were analysed by scanning electron microscopy, energy-dispersive X-ray analysis and X-ray powder analysis. The crystalline phases in the LTCC materials were determined. E electrical characteristics, i.e., sheet resistivities, noise indices and gauge factors of the thick film resistors, were measured. While there were variations in the other electrical characteristics of the resistors fired on different substrates, the gauge factors were rather independent of the substrate materials

This work is dedicated to the late Professor Marija Kosec

Keywords: thick film resistors, LTCC, X-Ray diffraction, micro-structures

Karakterizacija debeloplatnih uporov kot senzorjev sile na različnih LTCC substratih

Izvleček: Debeloplastni upori lahko služijo kot senzorji sile / deformacije na ali v večplastnih MEMS strukturah. Razmeroma nizki moduli elastičnost LTCC (Low temperature co-fired ceramics – keramika z nizko temperature žganja), če jih primerjamo s keramiko na osnovi Al2O3, vodijo do večjih občutljivosti senzorjev pri istih dimenzijah. Dva debeloplastna uporovna materiala – Du Pont 2041 in Electro Science Labs 3414 – sta bila tiskana in žgana na relativno inertnih Al2O3 in različnih LTCC podlagah. Testirani LTCC materiali so bili Du Pont 951, ESL 41020, Heraeus HL 2000, Ferro L8 in Heraeus CT 702. Z izjemo Du Pontovega 951 so vsi ti materiali brez svinca, medtem ko steklena faza v 951 vsebuje okrog 2 mol.% PbO. LTCC folije so bile analizirane z elektronskim vrstičnim mikroskopom, mikro anaslizo in rentgensko analizo. Določili smo faze, ki izkristalizirajo med žganjem. Izmerili smo električne karakteristike debeloplastnih uporov na različnih podlagah. Medtem, ko so plastne upornosti, temperaturne odvisnosti upornosti in indeksi šuma odvisni od podlag, na katerih so bili žgani upori, je faktor gauge – sprememba upornosti v odvisnosti od deformacije – v glavnem neodvisna od podlag.

Ključne besede: debeloplastni upori, LTCC rentgenska praškovna analiza, mikrostrukture

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1 Introduction

Fired thick-film resistors basically consist of a conducting phase in an insulating matrix, usually a silica-rich, lead-borosilicate-based glass. The ratio between the conductive and the glass phases roughly determines the specific resistivity of the resistor. During the firing cycle the conductive phases of the resistor materials interact with the glass phase forming conductive networks through the sintered layers. In most modern thick-film resistor compositions the conductive phase is either ruthenium oxide or electrically conducting pyrochlores: mainly lead or bismuth ruthenates [1-3] with resistivities of 40 x 10^{-6}, 150 x 10^{-6} and 270 x 10^{-6} ohm.cm for RuO_2, $Bi_2Ru_2O_7$ and $Pb_2Ru_2O_{6.5}$, receptively [2-4]. During the firing cycle the conductive phases of the resistor materials interact with the glass phase. The resistors are fired for only a short time at the highest temperature, typically 10 minutes at 850°C.

Advanced microelectronic packages – ceramic modules – with a high density of interconnections and in-

tegrated electronic components are, in many cases, realised by Low Temperature Co-Fired Ceramics (LTCC) technology, which is considered as one of the more advanced technologies for the fabrication of these packages. LTCC materials are sintered at low temperatures around 850°C or 900°C. In order to sinter to a dense and non-porous structure at these, rather low, temperatures, LTCC materials contain some (or a great deal of) low-melting-point glass phase. LTCCs are mainly based on a mixture of crystallisable glass and ceramics: in most cases alumina [5-8].

Sensors for mechanical quantities are fundamental parts of MEMS, and screen printed and fired thick-film resistors can be used to sense the mechanical deformations in MEMS structures. The important characteristic of LTCC materials is a relatively low elastic modulus, which means an increased sensitivity of the sensing elements due to the larger deformation under same conditions as compared to alumina substrates. This is shown in Fig. 1. – calculated deflections of diaphragms with the same radii and thicknesses made with the alumina and the LTCC at an applied pressure of 100 kPa.

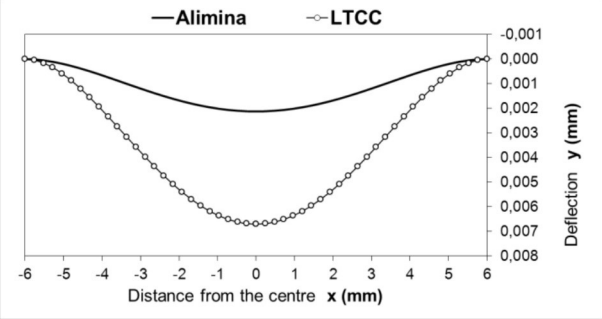


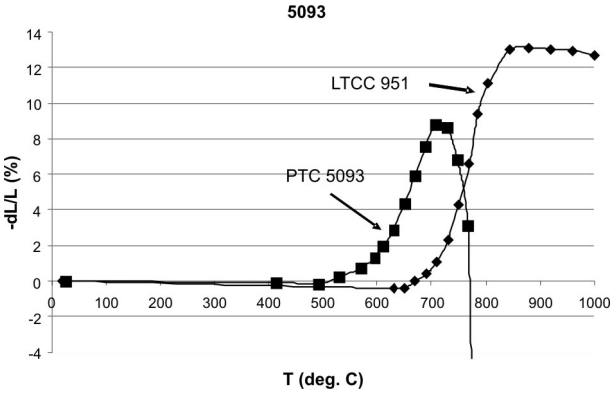
Figure 1: The deflections of diaphragms made with the alumina and the LTCC at an applied pressure of 100 kPa.

The change in the resistance of a resistor under an applied stress is partly due to deformation, i.e., the changes in the dimensions of the resistor, and partly due to an alteration in the specific resistivity as a result of changes in the microstructure of the material [9]. The gauge factor (GF) of a resistor is defined as the ratio of the relative change in the resistance (ΔR/R) and the strain (Δl/l):

$$GF = (\Delta R/R) / (\Delta l/l) \quad (1)$$

Geometrical factors alone result in gauge factors of 2–2.5. Gauge factors higher than this are due to microstructural changes, i.e., changes of the specific conductivity. The GFs of thick-film resistors are mostly between 3 and 15.

Thick-film resistors are often integrated on the top of, or within, multilayer LTCC structures. However, most thick-film resistor materials are developed for firing on relatively inert alumina substrates. Therefore, the compatibility and interactions with the rather glassy LTCC substrates, leading to changes in the electrical characteristics, need to be evaluated [10-12]. Another factor could be the difference in the shrinking rates of resistors and LTCC tapes, if they are fired together on the surface or buried within green LTCC structures. This is shown in Figs. 2.a. and 2b. – sintering curves of the "normal" Du Pont resistor 5093 and the Du Pont LTCC 951, and the microstructure of the buried resistor after firing. In Figs. 3.a and 3.b the sintering curves and the microstructure of a buried resistor Du Pont CF-041 that was developed for compatibility with LTCC materials are shown [13]. The "normal" thick-film resistors start to shrink at temperatures around 100K to 150K lower than the LTCC materials, while in the case of resistors that are compatible with LTCC, both materials start to shrink at similar temperatures, i.e., at 650°C



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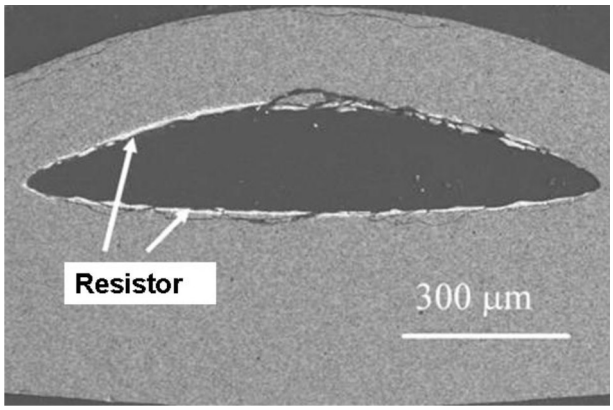
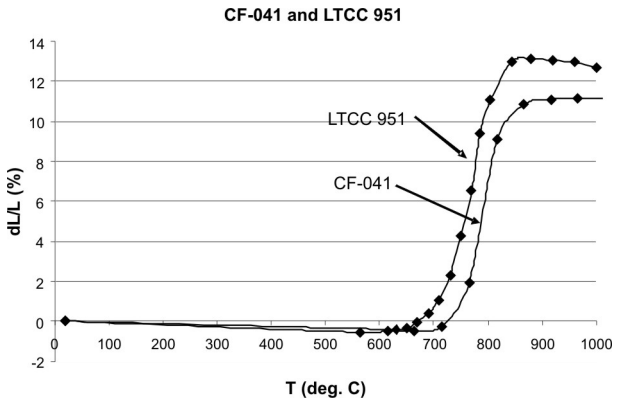


b.

Figure 2:.a. Sintering curves of Du Pont thick film resistor 9053 and Du Pont LTCC 951; b. Thick-film resistor (Du Pont 5093) buried within LTCC (Du Pont 951) structure. Different sintering rates lead to deformation.

For strain sensors, two thick-film resistors, i.e., 2041 (Du Pont, nominal resistivity 10 kohm/sq.) and 3414-B (Electro Science Labs. nominal resistivity 10 kohm/sq.)



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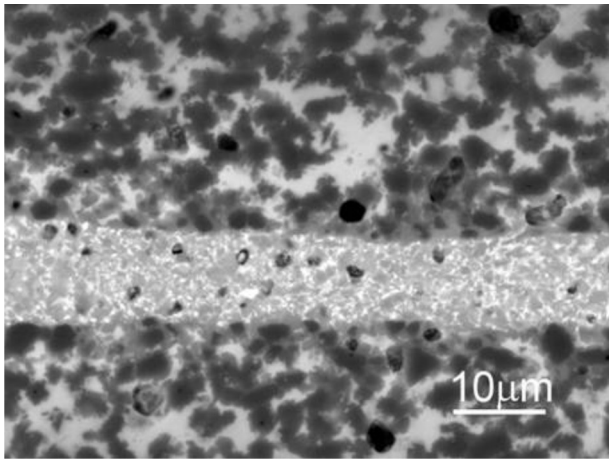


b.

Figure 3: a. Sintering curves of Du Pont thick film resistor CF-041 and Du Pont LTCC 951; b. Thick-film resistor (Du Pont CF-041) buried within LTCC (Du Pont 951) structure. Sintering rates of resistor and LTCC materials are comparable and the structure is not deformed.

were evaluated. The 2041 resistor was chosen because of its low noise [14], whereas the 3414-B was developed as a material with a high gauge factor, especially for use in strain gauges [15]. The resistors were screen printed and fired on five LTCC tapes, i.e., Du Pont 951, ESL 41020, Heraeus HL 2000, Ferro L8 and Heraeus CT 702. The resistors were also fired on rather inert alumina substrates.

As mentioned above, the electric characteristics of the resistors could deteriorate. Therefore, the main purpose of the paper will be an evaluation of the electrical characteristics of the resistors fired on alumina and different LTCC substrates. The sheet resistivities, noise indices, temperature coefficients of resistivities (TCRs) and gauge factors were measured.

LTCC DP 951, which contains between 2 and 3 mol. % of PbO is, at least from the data in the open literature, the "workhorse" in electronic packaging. The HL-2000 is a well-known "zero shrinkage" material. "Zero shrinkage" does not mean that there is no shrinkage during firing. However, while "ordinary" LTCC tapes shrink in longitudinal and vertical directions, the HL-2000 shrinks only in "z" direction, while the "x" and "y" dimensions stay more or less the same.

The important "electrical" characteristics for all the evaluated LTCC materials (taken mainly from data sheets) are rather similar as, after firing, all the LTCC materials consist of a glass phase, a ceramic filler and a phase or phases that crystallise during firing. To summarise; the dielectric constants are between 7 and 8, the insulation resistivities are between 10^{12} and 10^{13} ohm.cm and the break-down voltages are between 1000 V/25 um and 1500 V/um. These very similar reported results are reasonable, as more or less all LTCC materials are based on a mixture of glass and ceramic phase.

2 Experimental

The LTCC substrates were made by laminating three layers of LTCC tape at 70°C and a pressure of 20 MPa. The laminated green tapes were fired with the firing profiles required by the data sheets. The maximum firing temperatures were between 850°C and 900°C. The thick-film resistors printed on LTCC and alumina substrates were terminated with Pd/Ag conductors and fired at 850°C. The dimensions of the resistors for microstructural analyses and X-ray diffraction (XRD) analyses, which were printed and fired without conductor terminations, were 12.5×12.5 mm^2.

The samples – green and fired LTCC tapes – were investigated by X-ray powder diffraction analyses (XRD) with a Philips PW 1710 X-ray diffractometer using Cu Kα radiation. A JEOL JSM 5800 scanning electron microscope (SEM) equipped with an energy-dispersive X-ray analyser (EDS) was used for the overall microstructural and compositional analyses of the LTCC samples and the cross-sections of the resistors fired on different substrates. Prior to an analysis in the SEM, the samples were coated with carbon to provide electrical conductivity and to avoid any charging effects. Note that the boron oxide, which is also present in the glass phase of LTCC tapes, cannot be detected in the EDS spectra because of the low relative boron weight fraction in the glass and the strong absorption of the boron Kα line during the EDS analysis in the glass matrix.

The sheet resistivities were measured. The current noise indices were measured in dB on 100-mW loaded resistors using the Quan Tech method (Quan Tech Model 315-C). TCRs were calculated from resistivities measured between 25°C and 125°C.

The changes of resistivity as a function of substrate deformation (gauge factors) were measured with a simple device [16,17] . The ceramic substrate is supported on both sides. The load is applied to the middle of the substrate with a micrometer and this induces a tensile strain in the resistor. The magnitude of the strain is given by equation (2) [18]:

$$\varepsilon = \Delta l/l = (d * t * 6)/L^2 \quad (2)$$

d = deflection (m)
t = substrate thickness (m)
L = distance between support edges (m)

The gauge factors are calculated using equations (1) and (2) from the strain and resistivity changes. The test structures with resistors (the bending test) are shown in Fig. 4. For the measuring set-up used to obtain the results reported later, the distance between the support edges was 40 mm.

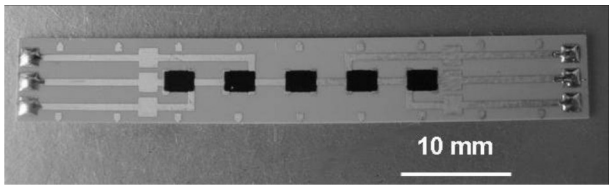


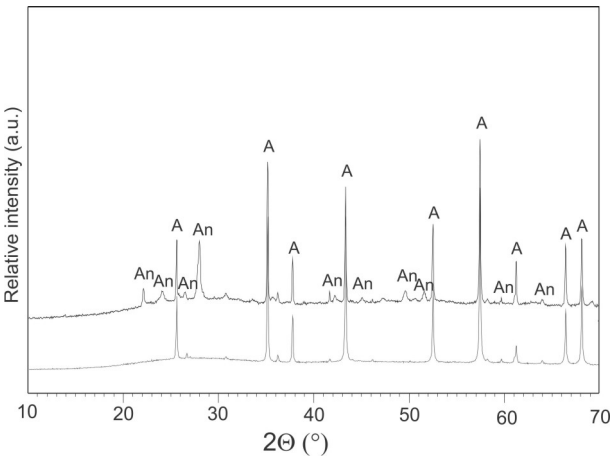
Figure 4: Test structure for resistivity vs. deformation evaluations. Five black squares are thick film resistors with dimensions 1.6x1.6 mm^2.

3 Results and discussion

3.1 LTCC materials

The X-ray spectra of the green and fired LTCC tapes Du Pont 951, ESL 41020, Heraeus HL-2000, Ferro L8 and Heraeus CT 702 are shown in Figs. 5.a, 5.b, 5.c, 5.d and 5.e, respectively. The unfired tapes are a mixture of glass and crystalline phase. In all the tapes the main crystalline phase is the alumina. The Heraeus CT 702 tape also contains a small amount of anatase, and the Ferro L8 tape small amounts of the anatase and the quartz. After the firing the peaks of other phases that crystallized from the glass phase can be observed. The main phases are the anorthite (calcium or barium alumo silicates) and the celsian (barium alumo silicate). The crystalline phases in unfired and fired LTCC tapes are summarized in Table 1.

The EDS analyses of the LTCC tapes are presented in Table 2. All the LTCC materials, with the exception of Heraeus HL-2000, also contain Co_2O_3, which is added tp produce a blue colour in the fired tapes. As the concentrations of cobalt oxide are below 0.5 mol.% they



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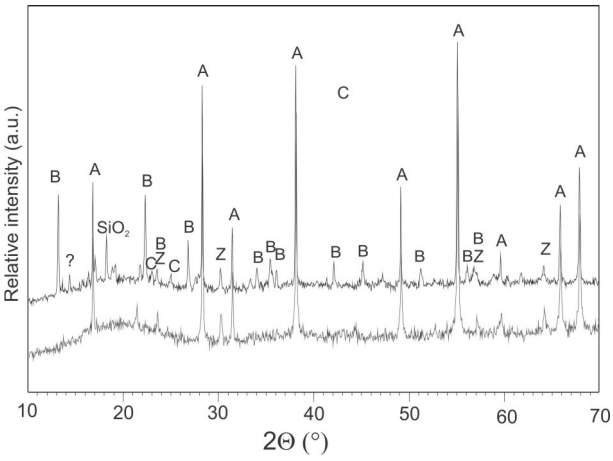

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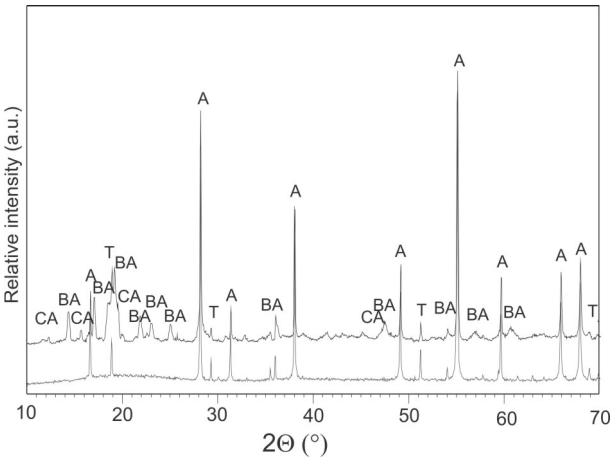
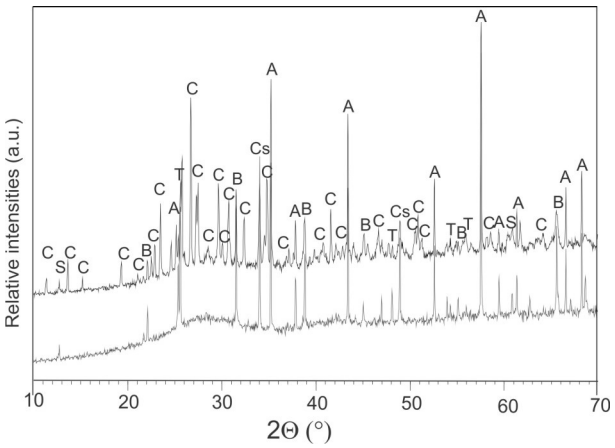


c.

Figure 5: a. X-ray spectra of Du Pont 951 LTCC before and after firing. The peaks of alumina and anorthite are denoted "A" and "An", respectively; b. - X-ray spectra of ESL 41020 LTCC before and after firing. Unidentified peak is marked by "?"; c. X-ray spectra of Heraeus HL-2000 LTCC before and after firing. Unidentified peak is marked by "?";



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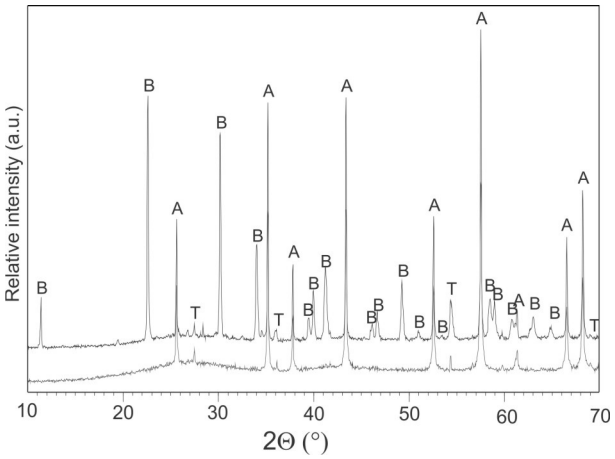


e.

Figure 5: d. X-ray spectra of Ferro L8 LTCC before and after firing. Al_2O_3 is denoted "A", TiO_2 "T", calcium alumo silicate "C", $BaTiO_3$ "B", quartz "S"and celsian (barium alumo silicate) "C"; e. X-ray spectra of Heraeus CT-702 LTCC before and after firing. Al_2O_3 is denoted "A", TiO_2 "T" and barium alumo silicate "B".

are not included in the Table. Most are lead-free, while the Du Pont 951 contains 2 mol.% (around 8 wt.%) of lead oxide. The main oxides are alumina (from 35 to 65 mol,%) and silica (from 25 to 40 mol.%). Heraeus HL-2000, Ferro L8 and Heraeus 702 also contain a small amount of titania, presumably to "assist" in the glass crystallization during firing.

Table 2: Composition of LTCC materials (mol.%)

	DP 951	ESL 41020	Her. 2000	Ferro L8	Her. 702
1/2 Na2O	2				
MgO					4
1/2 Al2O3	53	39	52	65	34
SiO2	36	39	31	26	40
1/2 K2O			3		
CaO	4	12	8	1	4
TiO2			3	1	3
ZnO		2			5
BaO		8	3	7	7
PbO	2				

3.2 Thick-film resistors

Two typical microstructures of thick-film resistors fired on LTCC substrates are shown in Figs. 6.a (2041 on ESL 41020 LTCC) and Fig. 6.b (3414 on ESL 41020 LTCC). The resistor layers are on top of the LTCC substrates. The light grains are the conductive phase and the darker matrix is a glass phase. In both cases the light phase at the resistor/LTCC interface is rich in the PbO, which diffused from the resistor layer into the LTCC substrate during firing. However, this "reacted" layer is thicker in the case of the 3414-B resistor, which means more extensive interactions and therefore a more significant influence on the resistors' characteristics.

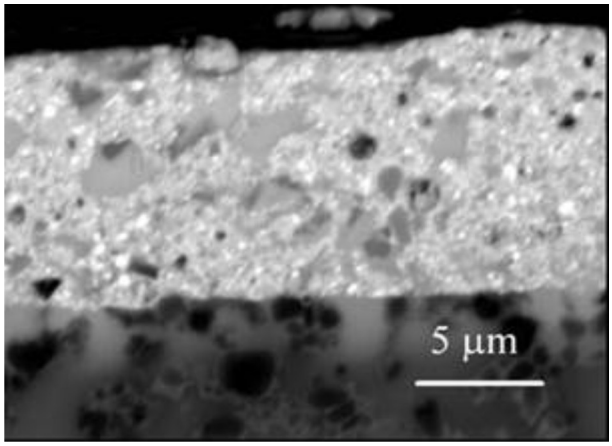
The electrical characteristics of the thick-film resistors on alumina and different LTCC substrates, i.e., sheet resistivities, TCRs, noise indices and gauge factors of 2041 and 3414 resistors are summarized in Table 3. The sheet resistivities, noise indices and gauge factors are graphically presented in Figs. 7, 8 and 9, respectively. Note that the noise indices in Table 3 are given in (dB), while in Figure 8 they are presented in (uV/V). These two units are related with a simple equation:

$$\text{noise (dB)} = 20 \log \text{noise (uV/V)} \quad (3)$$

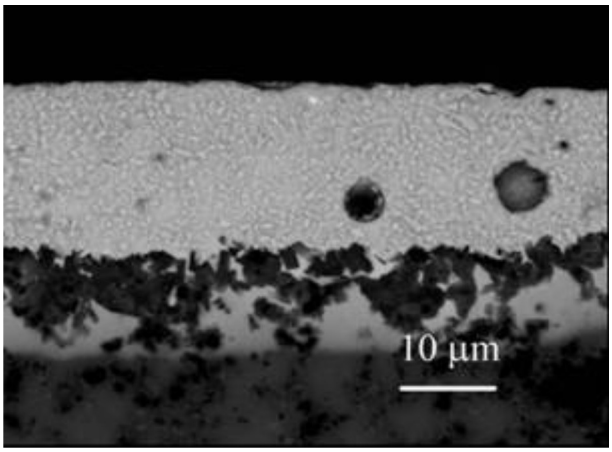
The sheet resistivities of the 3414 resistors are more "dependent" on the types of LTCC substrates than the resistivities of the 2041 resistors. I all cases sheet resistivities of resistors on LTCC substrates are higher, some-

Table 1: Evaluated LTCC materials and XRD analyses of crystalline phases in unfired and fired tapes.

	LTCC	Unfired tapes	Fired tapes
Du Pont	DP 951	Alumina	Alumina, anorthite
ESL	41020	Alumina	Alumina, celsian, gahnite
Heraeus	HL-2000	Alumina	Alumina, anorthite
Ferro	L8	Alumina, quartz, anatase	Alumina, quartz, anatase, celsian
Heraeus	702	Alumina, anatase	Alumina, anatase, anorthite



a.



b.

Figure 6: Microstructure of 2041 thick film resistor fired on ESL 41020 LTCC; b. Microstructure of 3414 thick film resistor fired on ESL 41020 LTCC

times significantly higher. The presumed reason for this is the diffusion of a glass phase from LTCC substrates into resistor films during firing resulting in a dilution of conductive phase in resistors. Also, the noise indices of the 3414 are significantly higher. However, the values of the gauge factors are for both resistors more or less independent of the substrate materials. The gauge factors of the 3414 thick-film resistors were higher (between 15 and 19) than the gauge factors of the 2041

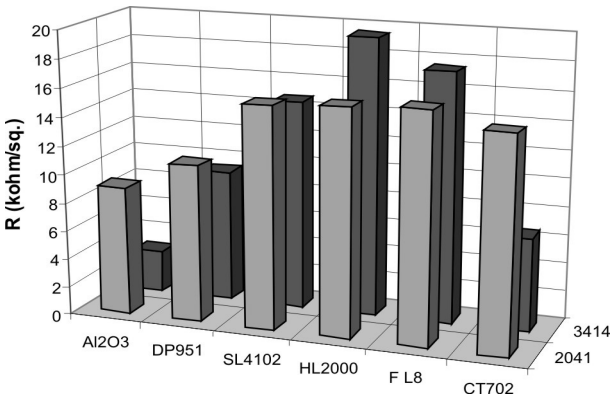


Figure 7: Sheet resistivities of 2041 and 3414 thick film resistors fired on alumina and LTCC substrates

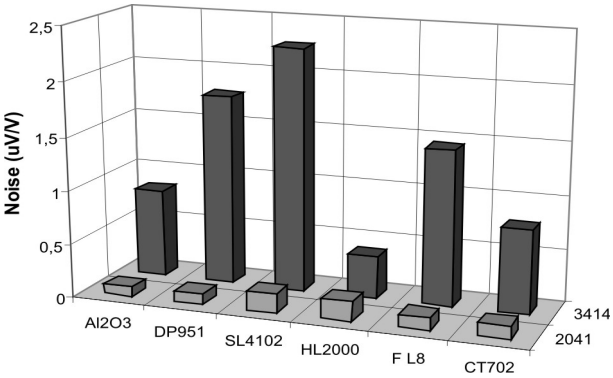


Figure 8: Noise indices of 2041 and 3414 thick film resistors fired on alumina and LTCC substrates

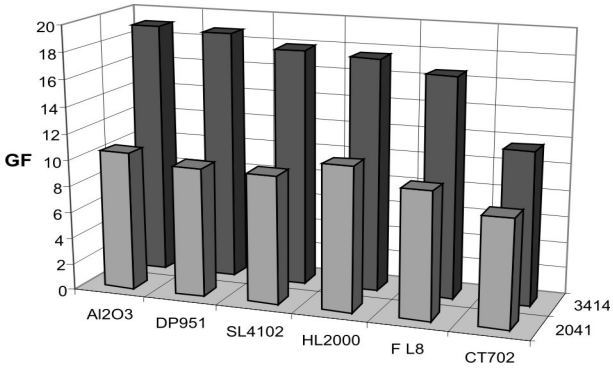


Figure 9: Gauge factors of 2041 and 3414 thick film resistors fired on alumina and LTCC substrates

Table 3: Electrical characteristics – sheet resistivities, noise indices, TCRs and gauge factors – of the 2041 and 3414 thick-film resistors fired on alumina and different LTCC substrates.

	Resistor 2041				Resistor 3414		
Substrate	R (kohm/sq.)	N.I. (dB)	TCR (x10-6/K)	GF	R (kohm/sq.)	N.I. (dB)	GF
Al2O3	9.0	-21.0	15	10.5	3.0	-4.2	19.1
DP 951	11.0	-20.0	20	9.8	9.3	5.0	18.8
ESL 41020	15.5	-15.1	55	9.7	14.7	7.1	17.9
HL 2000	15.8	-14.5	50	10.9	19.5	-7.9	17.5
Ferro L8	16.1	-18.7	-40	9.6	17.5	3.2	16.7
CT 702	14.9	-18.4	-15	8.2	6.6	-2.1	11.6

resistors (around 10). These experimental results indicate that both the evaluated thick-film resistors could be used as sensing elements in the LTCC structures if other electrical characteristics are taken into account.

4 Conclusions

Sensors for mechanical quantities are fundamental parts of MEMS, and screen-printed and fired thick-film resistors can be used to sense the mechanical deformations in MEMS structures. The important characteristic of LTCC materials is the relatively low elastic modulus, which means an increased sensitivity of the sensing elements due to the larger deformation under same conditions as compared to alumina substrates. Therefore, thick-film resistors are often integrated on the top of or within multilayer LTCC structures. However, as most of the thick-film resistor materials are developed for firing on relatively inert alumina substrates the compatibility and interactions with the rather glassy LTCC substrates, leading to changes in the electrical characteristics, need to be evaluated.

For strain sensors two thick-film resistors with nominal resistivity of 10 kohm/sq. , Du Pont 2041 and ESL 3414-B, were tested. The resistors were screen printed and fired on five LTCC tapes, i.e., Du Pont 951, ESL 41020, Heraeus HL 2000, Ferro L8 and Heraeus CT 702. The resistors were also fired on rather inert alumina substrates. The LTCC materials were evaluated with XRD and EDS analyses. Results show that the unfired LTCC tapes are based on a mixture of glass phase and ceramic filler. After firing the crystalline phases crystallize from the glass component. The EDS microanalysis indicated that most of the LTCC materials, with the exception of Du Pont 951, are lead-free.

The sheet resistivities, temperature coefficients of resistivity, noise indices and gauge factors of the resistors processed on different substrates were measured. While there are variations in the other electrical characteristics of the resistors fired on different substrates, the gauge factors for both resistors are rather independent of the substrate materials.

5 Acknowledgment

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The influence of the platinum substrate roughness on the ferroelectric properties of $0.65Pb(Mg_{1/3}Nb_{2/3})O_3–0.35PbTiO_3$ thick films

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Abstract: The $0.65Pb(Mg_{1/3}Nb_{2/3})O_3–0.35PbTiO_3$ thick films were screen-printed on conductive platinum substrates, which differed in the surface roughness for almost an order of magnitude, namely, the vertical root mean square roughness values, determined by atomic force microscopy, were 44 nm and 342 nm, respectively. The films, sintered at 950 °C, crystallized in monoclinic and tetragonal perovskite phases, however, the film on the flat Pt substrate exhibited a higher degree of the (001) orientation of the tetragonal phase, and also a higher remnant polarization than the film on the rough Pt substrate. Transmission electron microscope analysis revealed the presence of an interfacial Pb-Pt phase between the film and the substrate, which was in the form of a continuous layer on the flat substrate, while on the rough Pt-substrate, it was segregated in surface imperfections. The appearance of the intermetallic phase at the film-substrate interface was attributed to the transient reducing atmosphere generated in the thick film upon heating as a consequence of thermal decomposition of organic screen-printing additives. This work confirms the importance of the substrate roughness in regard to the functional properties of the films.

This work is dedicated to the late Professor Marija Kosec

Keywords: 0.65PMN–0.35PT, thick film, platinum substrate, roughness, ferroelectric properties

Vpliv hrapavosti platinske podlage na feroelektrične lastnosti debelih plasti $0.65Pb(Mg_{1/3}Nb_{2/3})O_3–0.35PbTiO_3$

Izvleček: Debele plasti $0.65Pb(Mg_{1/3}Nb_{2/3})O_3–0.35PbTiO_3$ so bile z metodo sitotiska nanesene na prevodne platinske podlage, ki so se razlikovale v hrapavosti površine za skoraj velikostni red, in sicer je bila vertikalna srednja vrednost hrapavosti (koren srednjih kvadratov - rms), ki smo jo določili z mikroskopom na atomsko silo, 44 nm in 342 nm. Plasti, sintrane pri 950 ° C, kristalizirajo v monoklinski in tetragonalni perovskitni fazi, vendar plasti na ravni Pt-podlagi izkazujejo višjo stopnjo (001) usmerjenosti tetragonalne faze, prav tako pa tudi višjo remanentno polarizacijo, kot plasti na hrapavi Pt-podlagi. Analiza, narejena s presevno elektronsko mikroskopijo, je razkrila prisotnost intermetalne faze Pb-Pt med debelo plastjo in platinsko podlago, ki je bila na ravni podlagi prisotna v obliki neprekinjene plasti, medtem ko je bila na podlagi z veliko hrapavostjo segregirana v otočke. Pojav intermetalne faze na meji plast-podlaga pripisujemo prehodni redukcijski atmosferi, ki nastane v debelih plasteh med segrevanjem zaradi termičnega razpada organskih dodatkov v pasti za sitotisk. V članku je prikazan velik vpliv hrapavosti podlage na funkcijske lastnosti debelih plasti.

Ključne besede: 0.65PMN–0.35PT, debela plast, platinska podlaga, hrapavost, feroelektrične lastnosti

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1 Introduction

Relaxor-ferroelectrics, including the solid solution of $Pb(Mg_{1/3}Nb_{2/3})O_3–PbTiO_3$ (PMN–PT) as the prototype material, are characterized by a high dielectric permittivity, high electrostrictive and high piezoelectric properties and may be used for applications such as sensors, actuators, ultrasonic medical diagnostics and

non-destructive testing [1–3]. Several applications require films with the thicknesses in a range of few μm to a few 10 μm, and screen-printing is a simple, convenient and low-cost method for producing them.

Recently, bending-type actuators with large-displacement, consisting of the 0.65Pb($Mg_{1/3}Nb_{2/3}$)O_3–0.35$PbTiO_3$ (0.65PMN–0.35PT) thick-film on a thin Pt support, were designed. The preparation of such thick-film actuators is not trivial. After screen printing the film on a bulk platinized alumina substrate and subsequent firing, the 0.65PMN–0.35PT/Pt structure needs to be removed from the stiff substrate. The performance of such self-standing 0.65PMN–0.35PT/Pt actuator is excellent, i.e., the displacements of nearly 100 μm have been achieved for actuators with the dimensions of 18 mm × 2.5 mm × 50μm at only 18 V, which is five times larger as compared to the displacement of similar actuators described in the literature [4]. A future trend is to pattern the thick-film by printing directly on a thin Pt foil, which acts both as the substrate and as the bottom electrode. For successful design of such actuators, the influence of the surface conditions of the Pt-support on the properties of the active thick film needs to be understood.

In this work two substrates with different surface roughnesses were used and their influence on the structure and ferroelectric properties of the 0.65PMN–0.35PT thick films was compared. The first one was an optically-polished platinum block, while the second one was prepared by screen printing the platinum paste on such block and firing at 1200 °C, resulting in a much higher surface roughness. Such screen-printed bottom electrodes are typically deposited on alumina or Low Temperature Cofired Ceramic (LTCC) substrates. By introducing a screen-printed Pt-layer on top of the Pt-block our aim has been to : i) mimic the configuration of a typical screen-printed thick film structure and thus to achieve similar film/substrate interface conditions, however, ii) by using the platinum block as the substrate to keep the same level of thermal stresses in both thick film structures. The influence of the roughness of the Pt-substrate on the structural and ferroelectric properties of 0.65PMN–0.35PT thick films is discussed.

2 Experimental

For the synthesis of 0.65Pb($Mg_{1/3}Nb_{2/3}$)O_3–0.35$PbTiO_3$ (0.65PMN–0.35PT) a mixture of PbO (99.9%, Aldrich), MgO (98%, Aldrich), TiO_2 (99.8%, Alfa Aesar) and Nb_2O_5 (99.9%, Aldrich) in the stoichiometric molar ratio with an excess of 2 mol% PbO was high-energy milled in a planetary mill (Retsch, Model PM 400). After milling, the powder was heated at 700 °C for 1 h, milled in an attritor mill in i-propanol, dried and sieved. More details about mechanochemical activation of 0.65PMN–0.35PT powder are described in [5–8].

The 2-mm-thick platinum substrates were obtained from Zlatarna Celje (Pt 999). A Pt paste (Ferro 6412) was screen-printed and fired at 1200 °C for 1 h on Pt substrate. The thickness of the printed layer was around 10 μm. In further text, the substrates are denoted as Pt-flat and Pt-rough, respectively.

The 0.65PMN–0.35PT thick-film paste was prepared from a mixture of the prereacted powder and an organic vehicle, consisting of alpha-terpineol, [2-(2-butoxy-ethoxy)-ethyl]-acetate and ethyl cellulose in the ratio 60/25/15. The paste was printed on both substrates four times with intermediate drying at 150 °C. The samples were heated at 500 °C for 1 h to decompose the organic vehicle, and sintered at 950 °C for 2 h in $PbZrO_3$ packing powder with an excess of 2 mol% PbO and then cooled to room temperature with a rate of 3 °/min. The thicknesses of the films were around 40 μm. A fourfold printing of the paste (i.e., 40 μm of final thickness) is an optimal choice to study film properties. A single printed layer is not sufficiently uniform, while in films thicker than 100 μm, cracks would appear during thermal treatment.

The sintered films were analysed by PANalytical X'Pert PRO MPD X-ray diffractometer using Cu $K_{\alpha 1}$ radiation (λ = 1.54051 Å) from 2θ = 10° to 70° using a step of 0.033° and the time per step of 100 s. The phase composition was determined by the Rietveld analysis using the Jana2006 software [9]. The starting unit-cell parameters and the atomic positions for the 0.65PMN–0.35PT were taken from a former Rietveld study by Singh et al. [10].

The cross-section samples were prepared for microstructural analysis. The samples were mounted in epoxy, ground and polished using standard metallographic techniques. The microstructures of the samples were investigated by a field emission scanning electron microscopy (FE-SEM, Supra 35 VP, Carl Zeiss) by secondary electrons. The digitalized microstructures were processed with the Image Tool software14 (UTHSCSA Image Tool Version 3.00, 2002) to obtain the areas consisting of more than 120 grains. The grain size was expressed as the Feret's diameter (d_F).

The cross-section microstructures were also analysed by analytical transmission electron microscope (TEM, JEM 2010F, JEOL) equipped with an Energy-Dispersive X-ray spectrometer (EDXS). The samples were prepared conventionally by mounting the thick-film structures

with the epoxy glue into the sandwich, which was then ground, polished, dimpled and finally Ar^+-ion milled until perforation.

The topography and the root mean square (rms) vertical roughness of both Pt substrates were analyzed by the atomic force microscope (AFM, Asylum Research, Molecular Force Probe 3D). A tetrahedral non-coated Si tip on a Si cantilever coated by Al was used for the contact-mode imaging with the typical spring constant of 2 N/m.

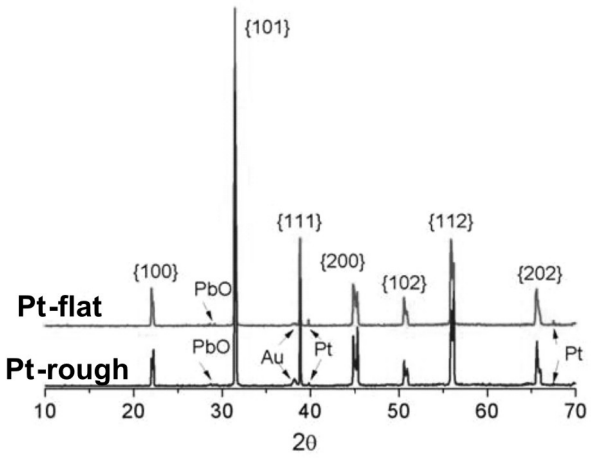
The 0.65PMN–0.35PT thick-film paste, dried at 150 °C to constant mass, was analysed by the thermogravimetric and differential thermal analysis (TG/DTA, Netzsch STA 409C). The sample with the mass of about 50 mg, deposited in an Al_2O_3 crucible, was analysed upon heating from 30 °C to 650 °C with the heating rate of 10 K min^{-1} in the flowing synthetic air (80 % N_2 – 20 % O_2) atmosphere.

For ferroelectric measurements, Au/Cr electrodes with a 1.5-mm diameter were deposited by magnetron sputtering (BAL-TEC SCD 005) on the top surface of the films. The ferroelectric hysteresis loops were measured by the Aixacct TF Analyser 2000 and the high voltage amplifier TREK 609E-6 at 50 Hz.

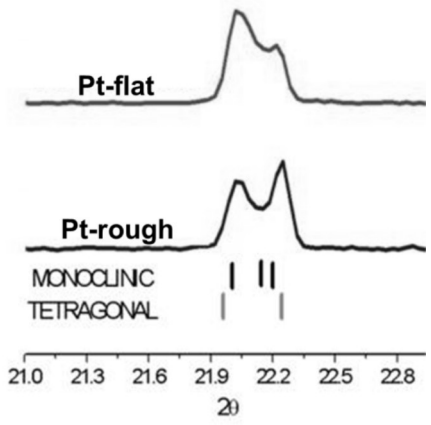
3 Results

The X-ray diffraction diagrams (XRD) for 0.65PMN–0.35PT thick films on the Pt-flat and Pt-rough substrates, prepared under the same conditions, reveal the presence of the perovskite phase, see Figure 1a. No extra reflections, which might correspond to the pyrochlore phase, were observed. Low-intensity diffraction peaks of PbO were detected in both XRD-patterns. Figure 1b shows the magnified regions of the diffraction patterns which correspond to the family of {100} Bragg peaks.

Although the 0.65PMN–0.35PT films on both substrates were prepared under the same conditions, their XRD patterns are obviously different. For description of the perovskite diffraction patterns the coexistence of monoclinic and tetragonal phases should be considered. Namely, it was shown in our previous work that the phase ratio in the 0.65PMN–0.35PT thick films on different substrates depended on the stress conditions, induced by the choice of the substrate [5]. The amounts of the monoclinic Pm and tetragonal P4mm phases in the two samples were calculated, and they are 81 % ± 1 % and 19 % ± 1 % in both cases. The same phase ratio in both samples indicates that the thermal stresses in both films are the same, in agreement



a.



b.

Figure 1: (a) The XRD diagram of 0.65PMN–0.35PT films on the Pt-flat and Pt-rough substrates. The families of Bragg peaks are written in brackets. The peaks corresponding to top Au and bottom Pt electrodes are marked by arrows; **(b)** The regions of the diffraction patterns corresponding to the family of {100} Bragg peaks. The refined peak positions of the (0 0 1), (1 0 0) tetragonal (grey, below) and the (0 0 1), (1 0 0), (0 1 0) monoclinic (black, above) phases are marked.

with [5]. When the (001) preferential orientation of the tetragonal phase was included in the Rietveld refinement, the quality of the fit was improved. The reliability factors for the monoclinic Pm (R_M) and tetragonal P4mm (R_T) phases, and the goodness of the fit (*GOF*) for the 0.65PMN–0.35PT films on Pt-flat and Pt-rough substrates were 3.68, 4.18, 1.10, and 4.05, 5.32, 1.42, respectively.

In a randomly oriented tetragonal perovskite-phase thick film, the number of the a-domains, i.e., with the a-axis in plane of the film, is twice that of the c-domains, i.e., with the polar, c-axis out of plane of the film. Consequently, the ratio of the peak intensities $I_{(001)}/(I_{(100)}+ I_{(010)}$

+ $I_{(001)}$) for the non-oriented perovskite phase is 0.33. In our study such ratio was 0.66 and 0.50 for the 0.65PMN–0.35PT films on Pt-flat and Pt-rough substrates, respectively. Thus, in both cases, the preferential c-domain orientation was evidenced, and it was more pronounced in the film on the Pt-flat substrate, reaching twice the value of the randomly oriented phase.

The SEM cross-section microstructures of the 0.65PMN–0.35PT films on both Pt substrates are shown in Figure 2. The films are quite dense. The grain size, d_F, is similar in both films, i.e., 1.1 μm ± 0.4 μm and 1.3 μm ± 0.5 μm for the films on Pt-flat and Pt-rough substrates. The comparison of the PMN–PT/Pt interfaces in Figure 2a and c reveals the flat surface of the polished Pt block in the former case, and a much rougher surface of the screen-printed platinum layer in the latter one.

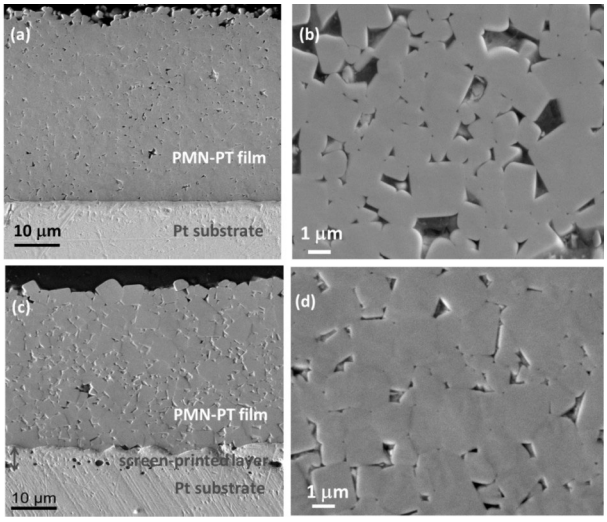


Figure 2: SEM cross-section images of 0.65PMN–0.35PT films on **(a)**, **(b)** Pt-flat and **(c)**, **(d)** Pt-rough substrates.

Moreover, the surface roughness of 0.65PMN–0.35PT films on both Pt substrates is determined primarily by the grain size, which is similar in both films. The rms roughness determined by AFM is approximately 0.5 μm.

The 0.65PMN–0.35PT thick films on both Pt substrates were further examined by the TEM-EDXS analysis. In Figure 3, the bright- and dark-field TEM micrographs of the film/Pt substrate interfaces are shown. In both specimens, an intermetallic Pb-Pt phase was detected at the film/substrate interface. The distributions of the intermetallic Pb-Pt phase at the film/Pt interface were different in the two samples and they could be related to the fractions of the (001) preferential domain orientation in the 0.65PMN–0.35PT thick films. Namely, in the film on the Pt-flat substrate, which showed a higher degree of the (001) preferential orientation, a continuous Pb-Pt layer was formed at the film-substrate interface (see Figure 3a and c), while in the film on the Pt-rough substrate with a lower degree of the (001) preferential orientation, only rare inclusions of Pb-Pt pockets were detected (Figure 3c and d).

Note that in the film on the Pt-flat substrate an additional layer could be observed between the Pb-Pt phase and 0.65PMN–0.35PT thick film, see Figure 3a. From the electron diffraction analysis we assume that this could be a pyrochlore phase, however a precise analysis of this layer could not be performed.

The intermetallic Pb-Pt phase has been often reported in the studies of lead-based perovskite thin films of various compositions, such as lead zirconate titanate (PZT) [11–17], however, in the thick-film studies it was reported only in the case when the PZT film was deposited on the platinised silicon substrate [18].

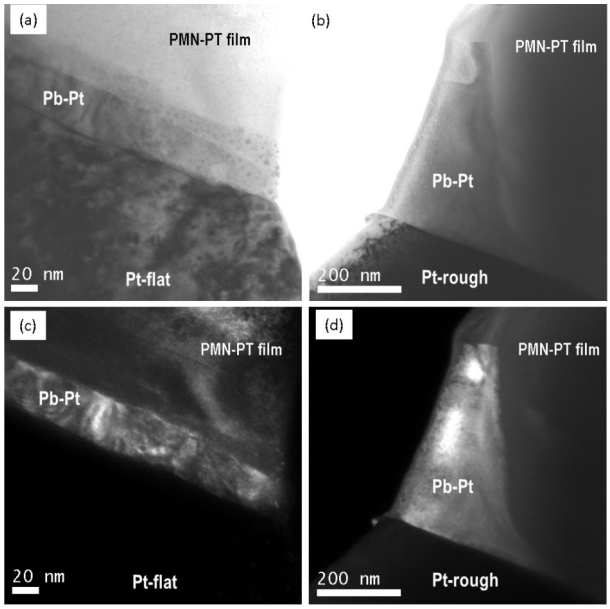


Figure 3: Bright **(a), (b)** and dark-field **(c), (d)** TEM micrographs of 0.65PMN–0.35PT films on Pt-flat and Pt-rough substrates.

Similar to PZT or PMN–PT thin-film structures [11–17], the formation of the intermetallic Pb-Pt phase in the thick 0.65PMN–0.35PT films may be attributed to the partial reduction of Pb^{2+} species to metallic lead in the process of the thermal decomposition of the organic vehicle in the 0.65PMN–0.35PT thick film during heating to 500 °C in air.

In order to verify the assumption, the thermal analysis of the 0.65PMN–0.35PT thick film paste, dried at 150 °C, was performed in air, see Figure 4. The sample lost 8.41 weight % upon heating to 450 °C. The major weight loss of 7.95 % occurred between approximately 200 and 380 °C, as evident from the thermogravimetric

(TG) and derivative thermogravimetric (DTG) curves, respectively. This weight loss was strongly exothermic, with the differential thermal analysis (DTA) peak at 308 °C. A minor weight loss of about 0.5 % occurred between 380 and 450 °C with the DTG and DTA–exo peaks at 430 °C. The two steps of weight loss are due to thermal decomposition of residual solvent alpha-terpineol, [2-(2-butoxy-ethoxy)-ethyl]-acetate and ethyl cellulose in air. It is reasonable to expect that in the bulk of the powder thermal oxidation of organic species in ambient atmosphere could result in a decreased partial pressure of O_2 to a low enough level to cause transient reduction of Pb^{2+} species to metallic lead, and, as already discussed above, in the thick film, to the formation of a Pb-Pt phase at the film/Pt-substrate interface.

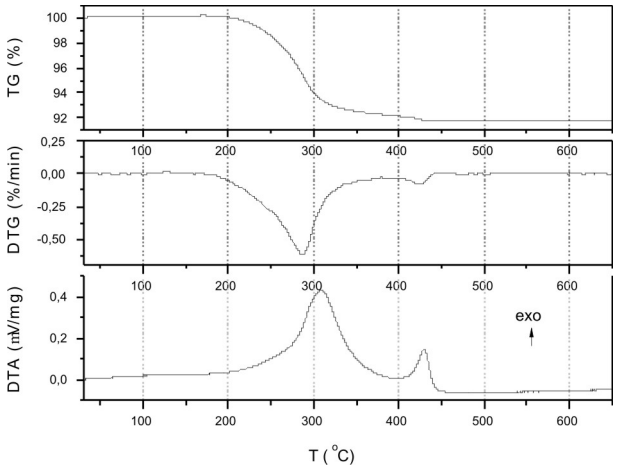


Figure 4: TG, DTG and DTA curves of the 0.65PMN–0.35PT paste, dried at 150 °C, recorded in air.

In solution-derived PZT thin films such Pb-Pt phase was stable upon heating to 350–700 °C, depending on the heating rate [12, 15, 16], and upon further heating in air the metallic lead was reoxidized to Pb^{2+} [12]. Note that the thickness of thin films was a few 100 nm. In the thick 0.65PMN–0.35PT films on Pt-substrates, which were sintered at 950 °C and cooled to room temperature, the Pb-Pt phase was still present. The exact composition of the intermetallic phase could not be determined due to the sputtering of Pt from the substrate during the TEM-specimen preparation. In the Pb-Pt phase diagram [19] three intermetallic compounds are formed, i.e., the Pb_4Pt, which is stable up to 360 °C, the PbPt, which is stable up to 795 °C, and the $PbPt_3$, which is stable up to 915 °C; and at higher temperatures the liquid phase is formed. We assume that in the case of the 0.65PMN–0.35PT thick film, the lead could not be reoxidized due to the slow diffusion of oxygen through about 40 µm of the film thickness (see Figure 2).

The cross-section microstructures of both 0.65PMN–0.35PT films on Pt-substrates reveal significant differences in the substrate roughness as evident from Figures 2a and c, respectively. The latter was evaluated on the pristine Pt-substrates by AFM imaging. The topographic AFM image of the Pt-flat substrate reveals a

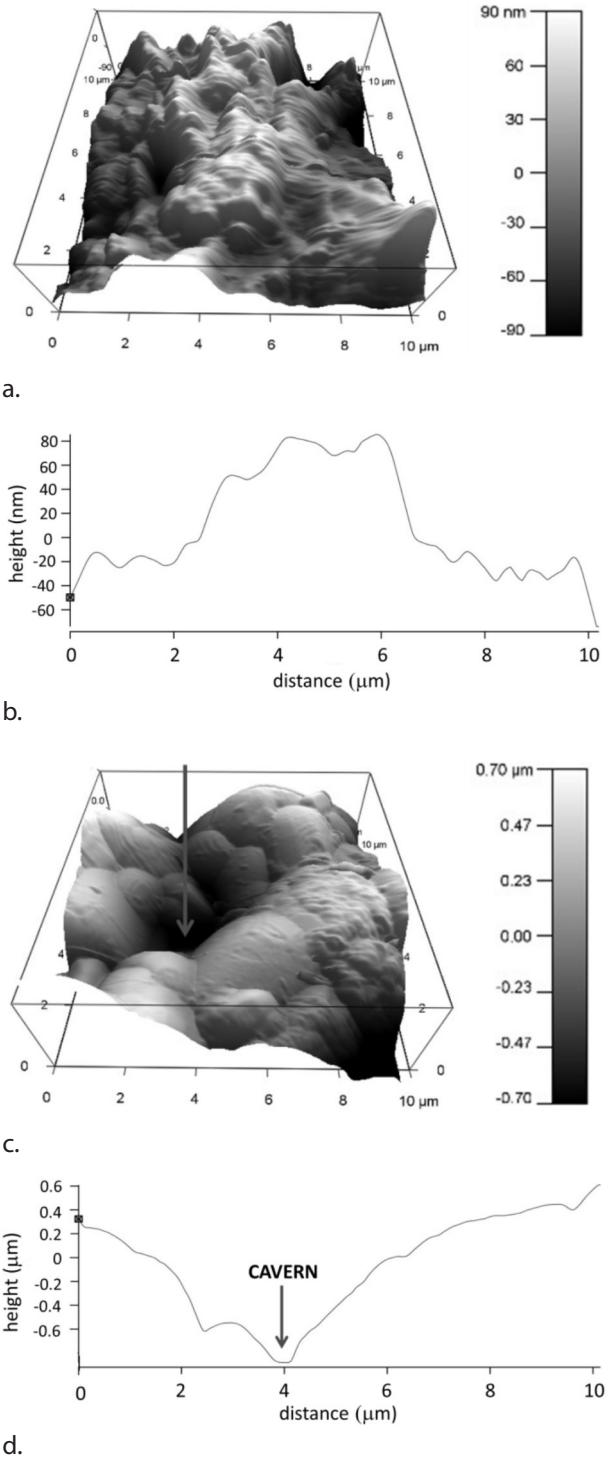


Figure 5: Topographic AFM images and scanning line profiles of the Pt-flat **(a), (b)** and Pt-rough **(c), (d)** substrates. Note the change of scale of the two pairs of images.

smooth surface with the image rms roughness of 44 nm, see Figure 5a. The profile of a selected scanning line is given in Figure 5b. In contrary, the topographic AFM image of the Pt-rough substrate reveals a much rougher surface, with the image rms roughness of 342 nm, see Figure 5c, d, which is almost an order of magnitude higher than the former value. Such pronounced substrate roughness along with the presence of caverns in the size range of 1 μm (see the arrows in Figure 5c, d) could give rise to the Pb-Pt interfacial phase segregation promoted by the action of capillary forces, c.f. Figure 3 b, d. In the case of the optically-polished Pt-flat substrate surface, the intermetallic phase is distributed evenly and forms a continuous layer at the film/substrate interface, c.f. Figure 3 a, c.

Further, we investigated the ferroelectric properties of 0.65PMN–0.35PT films on both Pt substrates. The polarisation - electric field hysteresis loops of the films are shown in Fig 6. The coercive electric field (E_c) is in both cases similar, around 15 kV/cm. However, the values of the remnant polarization (P_r) of the films on Pt-flat and Pt-rough substrates are 27 and 15 μC/cm^2, respectively. This means that the higher remnant polarization coincides with the higher degree of (001) domain orientation. Such relation was found in the study of the domain structure in tetragonal 0.62PMN–0.38PT single crystals, where the spontaneous polarization is along the (001) direction. The P_r along (001) direction was 37 μC/cm^2, while it was much lower along the non-polar (111) direction, around 20 μC/cm^2 [20].

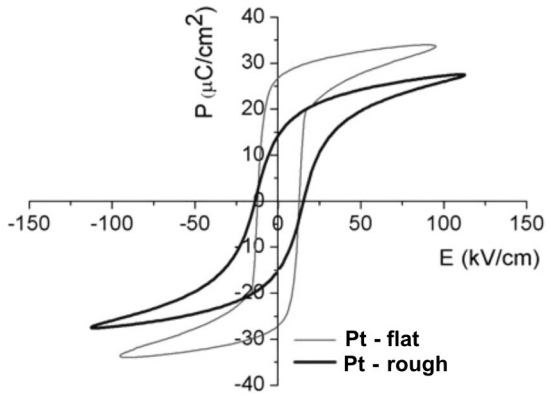


Figure 6: Polarisation – electric field hysteresis loops of the 0.65PMN–0.35PT thick films on Pt-flat and Pt-rough substrates.

4 Conclusions

In this work the influence of the roughness of the Pt-substrate on the structural and ferroelectric properties of 0.65PMN–0.35PT thick films was discussed. The thick-films were deposited on the Pt substrates with very different roughnesses. The optically-polished Pt-substrate revealed a smooth, flat surface with an rms roughness of 44 nm. In contrary; the Pt-substrate with an additional screen-printed Pt-layer had a rough surface with an rms roughness of 342 nm.

Transmission electron microscope analysis revealed the presence of a Pb-Pt layer at the film/substrate interface in both cases. This intermetallic phase was presumably formed as a consequence of a partial reduction of Pb^{2+} during the thermal decomposition of organic additives in the screen-printed film upon heating. The choice of the substrate markedly influenced the distribution of the interfacial layer: on the flat substrate, it was in a form of a continuous layer, while on the rough substrate it formed pockets.

The 0.65PMN–0.35PT film, deposited on the flat Pt substrate, revealed a larger degree of the (001) domain orientation of the tetragonal phase than the film, deposited on the rough substrate. Consequently the remnant polarization (P_r) of the former film was higher, i.e., 27 μC/cm^2, than of the latter film, i.e., 15 μC/cm^2. The work demonstrates that the surface properties of the platinum substrate and related film/substrate interface reactions may significantly influence structure and ferroelectric properties of thick films.

5 Aknowledgement

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Current transients in solution-derived amorphous Ta_2O_5-based thin-film capacitors

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Abstract: Ta_2O_5-based thin films were prepared by Chemical Solution Deposition at temperatures not exceeding 400 °C. Amorphous Ta_2O_5 and Ta_2O_5–Al_2O_3–SiO_2 (Ta:Al:Si = 8:1:1 atomic ratio) films on platinized Si-substrates were investigated. The Ta_2O_5 film heated at 400°C exhibited the highest relative dielectric permittivity, ε_r (27±3). The ε_r decreased with a lowering of the processing temperature, and showed lower values for the Ta_2O_5–Al_2O_3–SiO_2 samples. However, the mixed-composition thin films exhibited less leakage and thus had improved current-voltage characteristics, compared to those of the pure Ta_2O_5 thin films.

Current vs. time (*I–t*) measurements were performed for the investigated Ta_2O_5-based capacitors in the metal-insulator-metal geometry. The drop in the current depended on both the composition and the thermal budget of the insulator. The recorded current transients are considered to be due to the trapping of the injected carriers in the dielectric film. The charging process proved to follow an exponential law.

This work is dedicated to the late Professor Marija Kosec

Keywords: leakage current, high-*K* dielectrics, amorphous materials, sol-gel chemistry

Prehodni tok v tankoplastnih kondenzatorjih na osnovi Ta_2O_5, pripravljenih s sintezo iz raztopine

Izvleček: S sintezo iz raztopine, nanašanjem z vrtenjem in s segrevanjem pri temperaturah do 400 °C smo pripravili amorfne tanke plasti na osnovi Ta_2O_5 in Ta_2O_5 – Al_2O_3–SiO_2 (molsko razmerje Ta: Al: Si = 8:1:1) na platiniziranih silicijevih podlagah. Plasti Ta_2O_5 izkazujejo najvišjo dielektričnost ε_r (27±3) po segrevanju pri 400°C, medtem ko je dielektričnost plasti, pripravljenih pri nižjih temperaturah nižja. Dielektričnost plasti na osnovi Ta_2O_5 – Al_2O_3–SiO_2 je prav tako nižja od dielektričnosti plasti samega Ta_2O_5, vendar plasti na osnovi mešanice oksidov izkazujejo boljše tokovno-napetostne karakteristike. Izmerili smo prehodne toke *I–t* tankoplastnih kondenzatorjev s strukturo kovina-dielektrik-kovina. Upadanje toka s časom ob konstantni napetosti izkazuje nepričakovano dolge časovne konstante. Hitrost upadanja toka s časom je odvisen tako od temperature segrevanja plasti kot tudi od kemijske sestave plasti. Razloge za opisani potek *I–t* pripisujemo procesu ujetja nosilcev naboja v dielektriku. Dejstvo, da lahko časovno odvisnost tokov v plasteh dielektrikov matematično opišemo z vsoto dveh ali treh eksponentnih funkcij nakazuje na to, da je v materialu prisotnih več različnih defektov z različnimi časovnimi konstantami procesa ujetja in sprostitve naboja.

Ključne besede: uhajalni tok, dielektriki z veliko dielektričnostjo, amorfni materiali, sol-gel

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1 Introduction

Transparent electronics has attracted much interest in the past years since it is considered to have the potential to be the next generation of optoelectronic devices [1]. It aims at the realization of fully transparent, lightweight and reliable electronics for everyday applications, *e.g.,* flexible displays. Thin-film transistors (TFTs) are important electronic devices that are mainly used as *on-off* switches in the active-matrix backplanes of

flat-panel displays. A lot of effort has been put into the research and development of transparent TFTs [2]. The requirements to be fulfilled include: low-cost deposition, low-temperature processing, suitable properties of the thin films both from the performance point of view and device downscaling. The first devices were reported about a decade ago [3,4,5], and have attracted considerable attention with respect to display applications. The transition from the a-Si:H TFTs to the transparent ones was conditioned by the use of materials with a higher dielectric permittivity (ε_r or *K*) than SiO_2. Therefore, the so-called high-*K* dielectrics should have an ε_r over 10, and preferably higher than 20 [6].

Ta_2O_5 thin films have attracted a lot of attention as insulating materials for metal–oxide–semiconductor field-effect transistors (MOSFETs) and high-density memory cells [7,8] due to their high dielectric constant [6], high refractive index and their chemical and thermal stability [9]. In past years the use of Ta_2O_5 as a gate dielectric in transparent TFTs has also been proposed. Thin films deposited by rf magnetron sputtering [10], and e-beam evaporation [11] showed promising performance in the new generation of oxide TFTs. To the best of our knowledge, little work has been reported on the sol-gel processing of such thin films, although it is an economic, versatile and effective method. In this work an investigation of the conduction mechanisms and the charging effects in Ta_2O_5-rich thin films in view of their application as gate dielectrics in TFTs is presented. Thin films of both the ternary composition Ta_2O_5–Al_2O_3–SiO_2 with the Ta:Al:Si = 8:1:1 atomic ratio (further denoted as 8:1:1) and pure Ta_2O_5 (further denoted as Ta) prepared by Chemical Solution Deposition (CSD) were investigated. The samples were processed at low temperatures, *i.e.,* not exceeding 400 °C, in order to check their suitability for gate-dielectric applications, and also to ensure their amorphous structure, which is generally preferred in TFTs [10]. As a typical high-*K* material, tantalum pentoxide begins to crystallize at 600 °C and it is crystalline above 700 °C [12]. Moreover, it is expected for Al_2O_3 and SiO_2 to stabilize the amorphous phase in multicomponent dielectrics based on Ta_2O_5, hindering crystallization up to about 1000 °C [13].

2 Methods

Alkoxide-based precursor solutions were synthesized at room temperature in a nitrogen atmosphere. The sol-gel synthesis of the precursors has been described elsewhere [14].

The Ta_2O_5-rich thin films were deposited on platinized silicon ($Pt/TiO_2/SiO_2/Si$, further denoted as Pt/Si) substrates purchased from aixACCT Laboratories (Institut für Werkstoffe der Elektrotechnik, Aachen, Germany) by spin coating for 30 s at a controlled speed of 3000 rpm. After each deposition, the films were heated in air on hot plates at 150 °C for 2 minutes and at 250 °C, 300 °C, 350 °C or 400 °C for an additional 2 minutes. The process was then repeated several times in order to achieve the film thickness of 100–200 nm.

All the films were amorphous, as determined by X-ray diffraction (XRD, PANalytical X'Pert PRO diffractometer) with Cu Kα1 radiation [15].

A JEOL Ltd. JSM–7600F Field Emission Scanning Electron Microscope (FE-SEM) was used to investigate the fracture surfaces of the films on the Pt/Si and to determine the film thickness.

The electrical characterization was performed on metal-insulator-metal (MIM) capacitors fabricated by sputtering Au/Cr top electrodes with a diameter of 0.4 mm using shadow masks.

The capacitance and loss factor, tan δ, were measured at room temperature with a driving signal of 50 mV using a HP 4284A impedance analyzer. The relative permittivity values, ε_r, were determined at a frequency of 100 kHz.

The current–voltage (*J*–*V*) characteristics were measured using a Keithley 238 Source Measurement Unit with down to 10 fA of current-measurement resolution.

3 Results and Discussion

The fracture surfaces of the thin films deposited on Pt/Si were checked by FE-SEM. The analysis of the cross-section images revealed no microstructural features, in agreement with the amorphous state of the films, as determined by XRD [15]. The thickness of around 200 nm was determined for the samples heated at 250 °C, and it decreased considerably with the thermal budget. The densification was enhanced by the higher heating temperatures, leading to a thickness of about 115 nm for the samples heated at 400 °C. The results are listed in Table 1.

The dielectric properties of the films, in terms of capacitance and loss factor, were checked with little change in the frequency range from 10 kHz to 1 MHz. The ε_r values determined at 100 kHz are listed in Table 1.

For amorphous Ta_2O_5 thin films, relative dielectric permittivities in the range 20–28 are generally reported [6,16,17]. Among the samples investigated in the present study, the Ta film heated at 400 °C exhibited the

Table 1: Thickness values as determined from the FE-SEM cross-section images, and room-temperature dielectric permittivity and the loss factor of the investigated thin films, measured at 100 kHz. The values were estimated with an uncertainty of 10%.

T (°C)	Thickness (nm)		εr		tan δ	
	Ta	8:1:1	Ta	8:1:1	Ta	8:1:1
250	190 ±19	210 ±20	10 ±1	9 ±0.9	0.032	0.029
300	187 ±18	181 ±18	17 ±1.7	18 ±1.8	0.027	0.025
350	150 ±15	134 ±13	25 ±2.5	19 ±1.9	0.055	0.040
400	115±11	118 ±12	27 ±2.7	22 ±2.2	0.044	0.028

highest ε_r, a value of 27± 3. The 8:1:1 sample heated at the same temperature exhibited a lower permittivity of about 22± 2. The difference in ε_r between the two compositions also persisted for the heating temperature of 350 °C. The samples heated at 300 °C and 250 °C showed similar permittivity values for both compositions, with an important decrease for the lowest heating temperature as compared to the rest. The samples exhibited dielectric losses from 2.5% up to 5.5% at 100 kHz.

It is known that compared to Ta_2O_5, Al_2O_3 and SiO_2 have a lower ε_r, being respectively 9 and 3.9 [6]. Since the relative permittivity value roughly follows a linear rule of mixtures with composition [13], the multicomponent dielectrics containing alumina and/or silica would exhibit decreased permittivity as compared to the pure oxides. The ratio 8:1:1 was considered in order to have acceptable permittivity values. According to Robertson an ε_r value higher than 20 is expected to fulfil the requirements of further downscaling in the development of microelectronics and integrated micro-technology devices [18]; therefore, the thin films heated above 300 °C are suitable for further applications.

For good performance in passive and active electronic devices, *i.e.,* capacitors and TFTs, the dielectric layer should exhibit both high permittivity and high resistivity, and thus a low leakage current.

In our previous study, the current-voltage measurements revealed considerably improved characteristics for the 8:1:1 samples within the investigated heating temperature range, with a significant overall decrease of the leakage currents in contrast to that of the Ta_2O_5 thin films [15]. The *J–V* characteristics were also dependent on the thermal budget of the samples, *i.e.,* the leakage currents for the investigated samples increased with the processing temperature (Fig.1 a). The current-voltage characteristics were ohmic at low applied electric fields (E < 100 kV/cm) and exhibited a Poole-Frenkel-like behaviour at higher applied fields. The Ta samples heated at 350 °C and 400 °C exhibited highly nonlinear behaviour at E > 100 kV/cm [15].

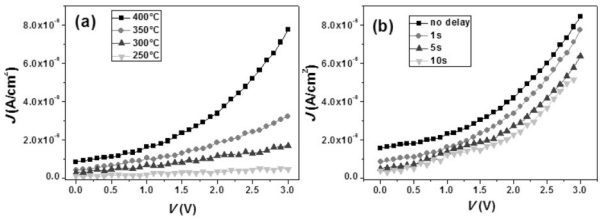

Figure 1: (a) Current density versus applied voltage characteristics of the 8:1:1 thin films recorded after a delay time of 1 s at each measurement point. (b) *J-V* characteristics recorded with different delay times for the 8:1:1 thin film processed at 400 °C.

We noticed a significant dependence of the *I–V* curves if measured at different scan times. In order to understand the charge transport in solution-derived Ta_2O_5-based thin films further investigations were performed. Fig. 1 b shows the leakage current densities of the 8:1:1 sample processed at 400 °C obtained with the fastest scan-rate or after a certain delay between the voltage set and the current measurement for each point. A decrease in the leakage current at longer step delay times was observed. Similar results were obtained for the Ta sample. The *J–V* characteristics recorded for the thin films heated at lower temperatures proved to be less influenced by the step delay time chosen for the measurements.

The time-dependent decrease of the current in the Ta_2O_5 films with the applied d.c. voltage, also known as the current transient, has been previously reported [19,20,21]. To obtain an insight into the time scale of this effect, we performed additional current *vs.* time (*I–t*) measurements at a constant applied voltage of 1 V (Fig. 2) for 1 min. The samples processed at higher temperatures showed more pronounced current drops, which is in agreement with the larger differences in the *J–V* characteristics when recorded after longer delay times. The 8:1:1 samples had a lower drop of the current as compared to the Ta ones, which is in accordance with the difference in the capacitance between the two series.

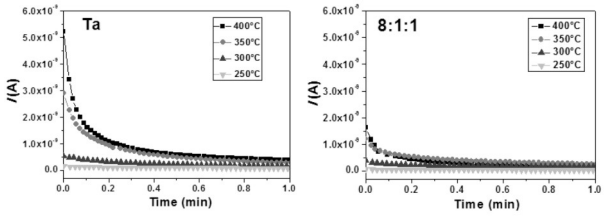

Figure 2: Room-temperature current transients measured under a constant applied voltage of 1V.

The time-dependent current variation in the Ta_2O_5 thin films was reported to occur as an initially high drop of the current followed by a gradual decrease after a certain relaxation time [20]. In this study, the Ta sample heated at 400 °C reached the steady-state after about 10 min (Fig. 3a). For the rest of the samples the measurements were performed for longer times. As the relative change of the current depends on its absolute value [20], the films having larger initial currents when the voltage was applied reached their steady-state currents much faster. Therefore, the Ta thin films heated at lower temperatures required much longer times to reach their steady-state current values. Moreover, the 8:1:1 samples reached the steady-state currents only after several hours (Fig. 3b).

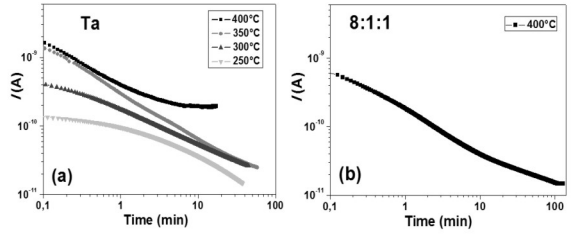

Figure 3: *I–t* characteristics of the Ta thin films series (a) and the 8:1:1 sample processed at 400 °C (b), measured under the applied voltage of 1V.

It is clear that such current transients cannot occur due to the intrinsic capacitance of the sample only, but they might originate from the dielectric absorption and mostly from an additional bulk charge-trapping mechanism since high-*K* dielectrics contain a large bulk density of defects and trapped charges [6]. Therefore, we checked to see how the conductivity is dependent on the voltage polarity. The current was recorded as the voltage was swept from the negative to the positive bias and back. Besides the initial build-up, also the current hysteresis width proved to be dependent both on the composition (Fig. 4 a) and the heating temperature of the samples (Fig. 4 b). This suggests that charge trapping occurs when the voltage is applied. The clockwise hysteresis proves that charges are trapped when going positively and released when going back. The process is more pronounced for the Ta sample or for a larger thermal budget. Charge trapping can be reduced by different heat treatments, or by changing the composition. It was reported that $HfSiO_x$ exhibits a lower hysteresis than HfO_2 [6], which is consistent with our results. The delay time played little role, as the hysteresis width was only slightly reduced for the step delay times of up to 10 s.

At first, the current transients were believed to be an intrinsic characteristic of the Ta_2O_5 and to be due to charge-trapping (or emission) in the dielectric film [19].

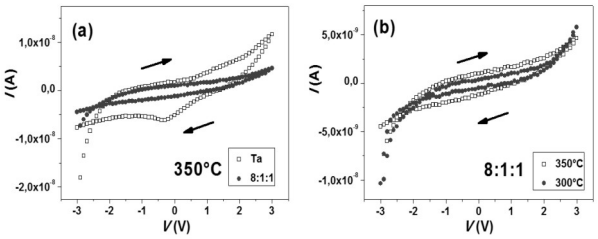

Figure 4: *I–V* curves of Ta_2O_5-based thin films measured with the minimum delay time. The voltage was swept from the negative to positive values and back as indicated by the arrows in the figures.

Later, other explanations for the current-transients in the metal-insulator-semiconductor (MIS) capacitors were given [20,21]. More recent papers of A. Persano et al. (2010) reported the room-temperature current-voltage characteristics of amorphous Ta_2O_5 thin films measured in the MIM configuration and proposed the temporal variation of the polarization to be the cause of the transient currents. Their proposed explanation is that the charge carriers injected by applying an electric field are trapped in the defects of the dielectric film, thus changing the polarization [22]. We assume a similar effect in the case of our Ta_2O_5-based thin films.

For the investigated samples, the current transients were modelled as the exponential decay given by Eq. (1) with correlation coefficients higher than 0.99.

$$I(t) = A_1 \exp\left(-\frac{t}{\tau_1}\right) + A_2 \exp\left(-\frac{t}{\tau_2}\right) + A_3 \exp\left(-\frac{t}{\tau_3}\right) + y_o \quad (1)$$

where t is time, A_1, A_2, and A_3 are process pre-factors, τ_1, τ_2, and τ_3 are process time constants, and y_0 is the steady-state current due to ohmic resistivity.

Fig. 5 shows the current transients of the thin films heated at 400 °C fitted with Eq. (1). The parameter values used for excellent agreement are listed in Table 2. The fact that the relaxation process is determined by three time constants shows that the charge-trapping occurs at different rates, indicating that different kinds of bulk defects are involved in the process. Similar results were obtained for the thin films heated at 350 °C and 300 °C. For the samples heated at 250 °C (Fig. 5b), the current transients were fitted with a second-order exponential decay, *i.e.*, A_3=0. These results are in agreement with our previous results, which proved that the 250 °C thin films exhibited only ohmic behaviour, even at an applied electric field higher than 100 kV/cm, whereas in the case of the thin films heated at higher temperatures, the Poole-Frenkel conduction mechanism was dominant.

Table 2: The steady-state current due to ohmic resistivity (y_0), the process prefactors (A), and the process time constants (τ) used for fitting the current transients depicted in Fig. 5, which were modelled as third- and second-order exponential decays for the samples heated at 400 °C and 250 °C, respectively.

T (°C)	Sample	y_0 (A)	A_1 (A)	τ_1 (s)	A_2 (A)	τ_2 (s)	A_3 (A)	τ3 (s)
400	Ta	1.92 x10-10	1.65 x10-9	0.19	3.17 x10-9	0.03	3.83 x10-10	1.49
	8:1:1	3.16 x10-11	1.52 x10-10	2.68	4.83 x10-10	0.36	1.02 x10-9	0.04
250	Ta	1.38 x10-11	5.95 x10-11	10.53	6.67 x10-11	1.19		
	8:1:1	2.00 x10-11	1.54 x10-11	1.70	2.41 x10-11	13.20		

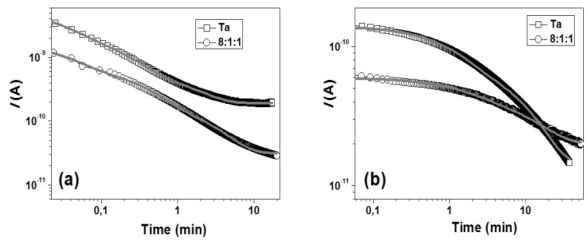

Figure 5: Current transients of the Ta and 8:1:1 thin films heated at 400 °C (a) and 250 °C (b), upon applying a constant voltage of 1 V. The solid lines are the fits to the current data with the third- (a) and the second-order (b) exponential decay, respectively.

4 Conclussions

Solution-derived Ta_2O_5 and Ta_2O_5–Al_2O_3–SiO_2 (Ta:Al:Si = 8:1:1 atomic ratio) thin films were processed in the temperature range from 250 °C to 400 °C. The amorphous thin films exhibited ε_r values up to 27± 3 for the Ta sample processed at 400 °C. The dielectric permittivity depended both on the composition and the heating temperature, showing lower values for the 8:1:1 samples and an important decrease for the sample heated at 250 °C.

The dc electrical conduction in the Ta_2O_5-based dielectric films was described in terms of bulk-limited processes, with Poole-Frenkel becoming the dominant mechanism for applied fields E > 100 kV/cm. Long-lasting current transients were recorded in the investigated samples at a constant applied electric field. The room temperature *I–t* measurements proved to be dependent on the thermal budget of the samples, rendering smoother transients and lower overall current values for the samples processed at lower temperatures. Moreover, the drop of the measured current was higher for the single-oxide samples than for the Ta_2O_5–Al_2O_3–SiO_2 films, in agreement with the dielectric permittivity results. The charging process has been investigated, finding that it follows an exponential law that can be fitted with two to three different time constants, indicating that different kinds of defects are involved in the charge-trapping process.

5 Acknowledgements

We acknowledge the financial support of the Slovenian Research Agency (Young researcher programme, contract number: 1000-10-310134; and projects: J2-4273, P2-0105), and of the EU7FP Project "ORAMA", Grant Agreement NMP3-LA-2010-246334.

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Compositional and Microstructural Study of Sol-Gel-Derived $PbZr_{0.3}Ti_{0.7}O_3/Al_2O_3/SiO_2/Si$ Thin-Film Structures

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Abstract: In this work we discuss the results of compositional and microstructural analyses of $PbZr_{0.3}Ti_{0.7}O_3/Al_2O_3/SiO_2/Si$ thin-film structures. The $PbZr_{0.3}Ti_{0.7}O_3$ (PZT) and Al_2O_3 thin films were prepared by the alkoxide-based sol–gel method. A dense, nanocrystalline, 20-nm-thick, γ-alumina layer was formed on the silicon substrate after annealing at 900°C for 1 hour. On top of this alumina layer, a PZT film with a <100> orientation of the tetragonal perovskite phase, about 300-nm-thick, was obtained after annealing at 550°C. The alumina layer did not completely prevent the diffusion of lead oxide from the PZT to the Si substrate. An additional Al-Si-Pb-O amorphous layer with a maximum thickness of 10 nm was observed between the Al_2O_3 and SiO_2 layers.

This work is dedicated to the late Professor Marija Kosec

Keywords: PZT thin films, interface reactions, SEM, TEM

Fazna in mikrostrukturna analiza tankoplastnih struktur $PbZr_{0.3}Ti_{0.7}O_3/Al_2O_3/SiO_2/Si$, pripravljenih s sol-gel sintezo

Izvleček: V delu so predstavljeni rezultati fazne in mikrostrukturne analize tankoplastnih struktur $PbZr_{0.3}Ti_{0.7}O_3/Al_2O_3/SiO_2/Si$. Z alkoksidno sol-gel sintezo smo pripravili tanke plasti s sestavo $PbZr_{0.3}Ti_{0.7}O_3$ (PZT) in Al_2O_3 na silicijevi podlagi. Po segrevanju na 900°C, 1 uro smo uspeli pripraviti gosto, 20 nm tanko plast γ-aluminijevega oksida na silicijevi podlagi. Na površino omenjenega aluminijevega oksida smo nanesli 300 nm tanko plast PZT, ki ima po segrevanju pri 550°C tetragonalno simetrijo in je orientirana v smeri <100>. Tanek sloj aluminijevega oksida ni popolnoma preprečil difuzije svinčevega oksida iz PZT v silicijevo podlago. Med Al_2O_3 in SiO_2 smo opazili dodatno, 10 nm amorfno plast Al-Si-Pb-O.

Ključne besede: Tanke plasti PZT, reakcije med plastmi, SEM, TEM

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1 Introduction

A lead-zirconate-titanate solid solution, with a composition close to the morphotropic phase boundary, is used in many multilayered structures due to its outstanding piezoelectric and ferroelectric properties. However, in order to obtain a stronger piezoelectric response, interdigitated electrodes (IDEs) have been introduced to replace the traditional parallel-plate electrode configuration, for example in energy-harvesting applications. [1,2] However, an IDE system requires a direct contact between the active film and the substrate. The direct integration of the piezoelectric $Pb(Zr,Ti)O_3$ layer on the silicon substrate leads to the formation of lead-silicate glass phases, which are not piezoelectric.[3] In order to prevent these undesired reactions, many materials were studied as barrier layers, such as Al_2O_3[4,5,6], $Ba(Mg_{1/3}Ta_{2/3})O_3$[7], $MgAl_2O_4$[8] and Ir.[9]

Alumina is a very good candidate for this barrier layer due to its chemical and thermal stability. Thin alumina layers, as a barrier layer between the $Pb(Zr_{0.52}Ti_{0.48})O_3$ and Si substrate, were prepared by a sol–gel route[4], by chemical vapor deposition (CVD)[5,6] or by a com-

bination of the two, i.e., the sol–gel and the CVD methods.[10] Depending on the method used and the heat-treatment conditions, amorphous or crystalline alumina was obtained.[4,5,6] For example, a pure crystalline alumina layer was obtained after annealing at 750°C for 30 min using the sol–gel method[4], and at 1000°C using the CVD method.[5,6] In addition, by using the CVD method, <001> or <111> oriented alumina films can also be grown on the silicon.[5]

However, despite the fact that there are a number of articles about the influence of the alumina layer on the functional properties of $Pb(Zr,Ti)O_3$ films, any detailed structural characterization of these multilayered thin-film structures is usually missing.

In this work we used the sol–gel route in order to prepare a $PbZr_{0.3}Ti_{0.7}O_3/Al_2O_3/SiO_2/Si$ thin-film structure. The aim of the work was, first, to analyze the phase composition and the microstructure of the alumina layer and, second, to evaluate the chemical compatibility between the alumina and the $PbZr_{0.3}Ti_{0.7}O_3$ film. The analyses from the micro- to the nano-level were performed by X-ray diffraction and analytical microscopy methods.

2 Experimental

An alumina precursor solution with a concentration of 0.25 M was prepared in a dry atmosphere by dissolving aluminum sec-butoxide, $(Al(O\text{-}secC_4H_9)_3$, Aldrich) in 2-methoxyethanol (CH_3-O-CH_2-CH_2-OH (2-MOE), Alfa Aesar). The solution was then intensively stirred in a dry box for 1 hour.

A precursor solution with the composition $PbZr_{0.3}Ti_{0.7}O_3$ and 10% excess of PbO was prepared in an atmosphere of dry nitrogen by mixing dehydrated lead acetate ($Pb(OAc)_2$, Alfa Aesar) titanium iso-propoxide ($Ti(O\text{-}iC_3H_7)_4$, Alfa Aesar) and zirconium iso-propoxide ($Zr(O\text{-}iC_3H_7)_4$, Alfa Aesar) in 2-MOE. After the mixing, the solution was refluxed for 2 hours and distilled to reach a concentration of ~0.5 M. After cooling to room temperature, 4 vol.% of formamide ($HCONH_2$, Alfa Aesar) was added to the solution. A detailed description of the $Pb(Zr,Ti)O_3$ solution's preparation can be found in.[11]

A thin alumina film was prepared by spin-coating (3000 rpm, 30 sec) the precursor solution on the SiO_2/Si substrate. Four layers of solution were deposited; after which each layer was dried for 5 min. at 200°C and given 5 min. of pyrolysis at 350°C. After the fourth layer, the thin-film $Al_2O_3/SiO_2/Si$ structure was annealed at 900°C for one hour with a heating rate of ~14°C/min.

Later, four layers of $PbZr_{0.3}T_{0.7}O_3$ solution were deposited on an $Al_2O_3/SiO_2/Si$ substrate (3000 rpm, 30 sec), with each deposition being followed by 2 min. of drying at 200°C and 2 min. of pyrolysis at 350°C. After the deposition of each second $PbZr_{0.3}T_{0.7}O_3$ layer (subsequently denoted as the PZT layer) the $PZT/Al_2O_3/SiO_2$/Si structure was exposed to rapid thermal annealing at 550°C for 15 min in air. The heat-treatment conditions were defined according to Malič et al.[12]

The thermal decomposition of the aluminum precursor solution, dried at 60°C, was followed by thermogravimetry and differential thermal analysis (TG/DTA, Netzsch STA 409), using a heating rate of 10°C/min. in a Pt crucible and an atmosphere of air.

The phases of the thin-film structures were determine with an X-Ray diffractometer (CuKα radiation, Philips PW 1710) in the range $2\theta=10°–65°$ using a step of 0.034° per 100 seconds.

Prior to the scanning electron microscope (SEM) and focused ion beam (FIB) microscope analyses the samples were coated with carbon in a sputter coater (SCD 050, BALTEC) to prevent charging and to provide electrical conductivity.

For the transmission electron microscopy (TEM) cross-section observations the thin-film samples were cut into pieces with a wire-saw, after which two pieces were glued together, head-to-head, with highly dispersed epoxy glue, and then glued into a copper ring. After the hardening of the glue, the thickness of the sample was mechanically reduced by grinding from 1 mm to ~100 µm. The sample was then dimpled from one side to a final thickness of ~20 µm. Finally, thin disks were exposed to an ion-milling procedure with 3.5-keV argon ions using a precision ion polishing system (PIPS, Gatan, Model 691). The areas adjacent to the specimen hole were used for the TEM observation.

The thin-film structures were characterized using a field-emission SEM (FE-SEM, Jeol JSM-7600F), a FIB microscope (FIB, Helios Nanolab 650, FEI) equipped with an INCA X-ray energy dispersive spectrometer (Oxford Instruments), a transmission analytical electron microscope (TEM, Jeol JEM-2100) and a high-resolution TEM (TEM, Jeol JEM-2010F) equipped with an Oxford LINK ISIS 300 energy-dispersive X-ray spectrometer (EDXS).

3 Results and discussion

3.1 Preparation and characterization of the alumina thin film on the SiO_2/Si substrate

In order to define the annealing conditions, a thermal analysis of the dried starting aluminum alkoxide solution was performed. The obtained TG and DTA curves are presented in Figure 1. During heating from room temperature to ~500°C the sample loses 50% of its mass, above 500°C no significant mass loss is observed. The mass loss is accompanied by an endothermic peak at ~140°C, which can be related to the evaporation of water and residual solvent, and the exothermic peak at ~310°C, which can be attributed to the decomposition of organic species.[13]

The DTA curve shows two additional exothermic peaks at ~870°C and ~1110°C.

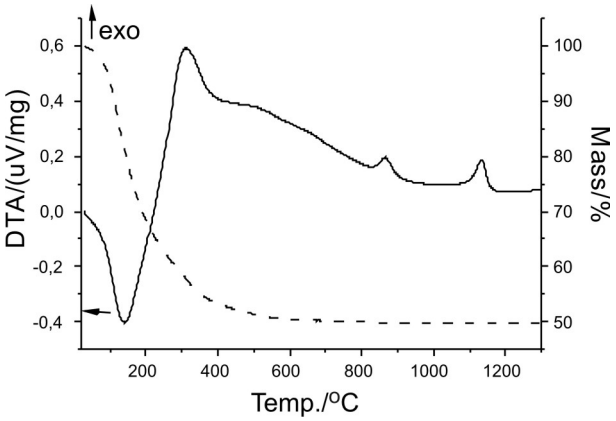
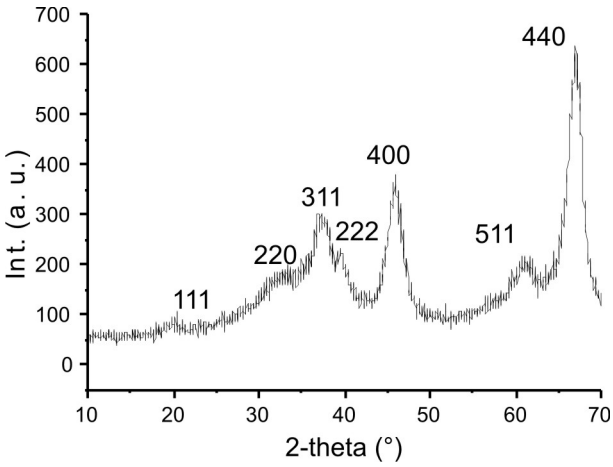


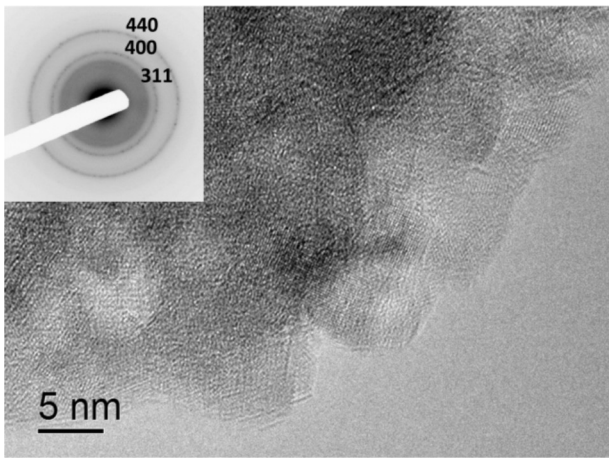
Figure 1: TG/DTA curves of aluminum alkoxide solution performed from 20°C to 1400°C.

The exothermic peak at 870°C could be related to the crystallization of the cubic γ-alumina from the amorphous gel. According to Bahlawane et al.[14] the γ-alumina crystalizes in the 850-900°C temperature range when using aluminum alkoxide as a precursor. The exothermic peak at 1100°C could be related to the growth of the γ-alumina crystals, which is an exothermic process. However, let us note that at the same temperature, above 1100°C, the alumina also transforms to the rhombohedral α-alumina. Most probably in our case these two effects overlap.

Based on the TG/DTA analysis, the dried aluminum precursor was annealed at 900°C for 1 hour, and, in order to characterize the obtained powder, XRD and TEM analyses were performed. An XRD pattern and a TEM bright-field image are shown in Figure 2. Figure 2(a) shows that all the peaks in the XRD pattern can be indexed by γ-alumina with a defect cubic spinel structure (PDF#80-1385). The peaks are very broad, indicating that the powder is poorly crystallized. The bright-field TEM image (Figure 2(b)) shows a few-nm-sized Al_2O_3 powder. According to the SAED analysis (Figure 2(b)) the Al_2O_3 nano-crystals have a cubic symmetry; this result is in agreement with the XRD data.



(a)



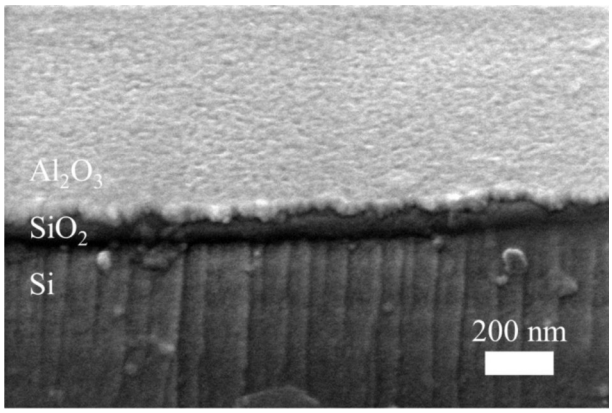
(b)

Figure 2: XRD pattern (a) and TEM image (bright field) (b) of Al_2O_3, after calcination at 900°C for 1 hour. The diffraction rings (inset of image b) were indexed with the cubic Al_2O_3 (PDF#80-1385)

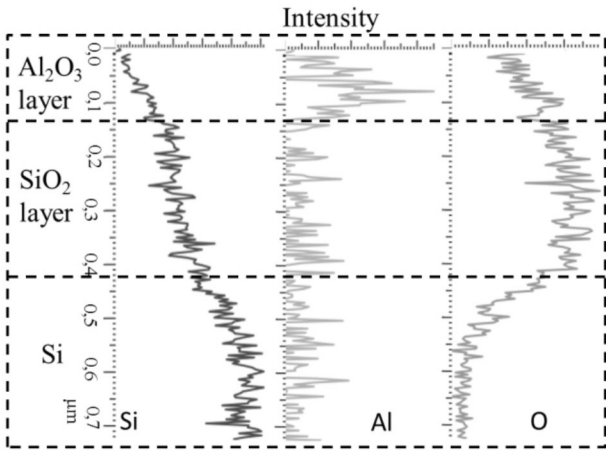
In accordance with these results, four layers of aluminum alkoxide solution were spin coated on the SiO_2/Si substrate and annealed for 1 hour at 900°C. The cross-section SEM micrograph of the prepared Al_2O_3/SiO_2/Si structure is shown in Figure 3(a). In order to determine the chemical composition a qualitative SEM-EDXS line analysis was performed across all the layers in the Al_2O_3/SiO_2/Si structure. (Figure 3(b)).

The surface of the upper layer is dense; the layer consists of a few-nm-sized grains. The SEM-EDXS analysis confirmed the presence of an upper Al_2O_3 layer on the SiO_2/Si substrate. However, the concentration profile of the Si shows that a small amount of Si was also detect-

ed within the Al_2O_3 layer, which can be related to the small spatial resolution of the EDXS analysis. Namely, when using a lower energy (below 10 keV) the information is coming from a depth of approximately 100–200 nm[15], i.e., greater than the thickness of the alumina layer, which is a few tens of nm. Therefore, besides the Al, a Si signal can also be detected. We should note that according to the SiO_2-Al_2O_3 diagram, different alumosilicates can be formed;[16] however, in the case of a thin, crystalline, alumina film on the silicon substrate, no silicon diffusion was reported in the literature. [4,5,6,10]



(a)



(b)

Figure 3: Cross-section SEM micrograph of the Al_2O_3/SiO_2/Si structure, after annealing at 900°C for 1 hour (a). The EDS line analysis across the Al_2O_3, SiO_2 and Si for Si, O and Al, performed at 5 keV (b). The cross-section and imaging were performed with the FIB microscope.

In order to analyze the Al_2O_3 film on the nanometer scale, the Al_2O_3/SiO_2/Si structure was investigated by TEM. In Figure 4, a cross-section TEM micrograph of a ~20-nm-thick Al_2O_3 film on a SiO_2/Si substrate is presented. The film consists of a few-nm-sized Al_2O_3 grains, as already observed by SEM analysis. According to the SAED analysis, the alumina grains have a cubic symmetry. The results are in accordance with the XRD analysis performed on sol-gel-derived Al_2O_3 powder (Figure 2).

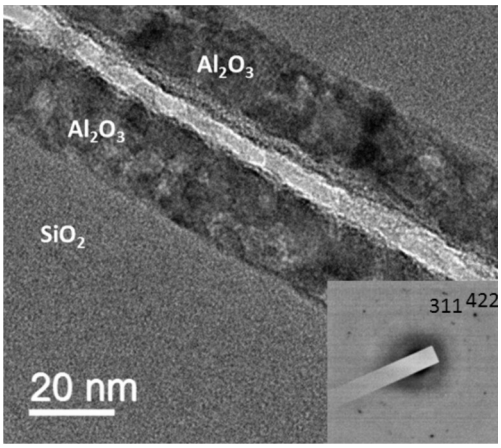


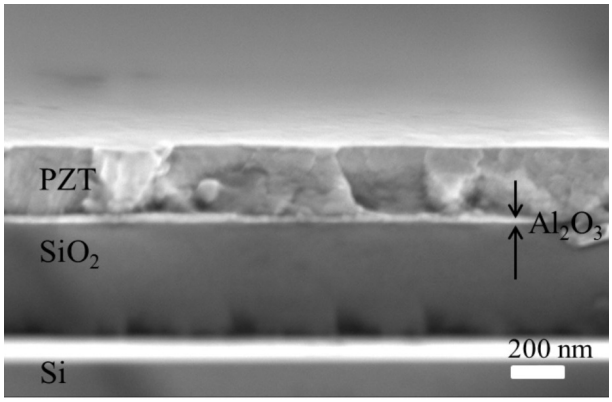
Figure 4: Cross-section TEM micrograph (bright field) of a polycrystalline Al_2O_3 thin film on a SiO_2/Si substrate, after firing at 900°C for 1 hour with the corresponding SAED patterns. The diffraction rings were indexed with the cubic Al_2O_3 (PDF#80-1385)

According to the SEM and TEM results, we can conclude that a continuous, dense, crystalline ~20-nm-thick layer of aluminum oxide on the silicon substrate was formed after annealing at 900°C.

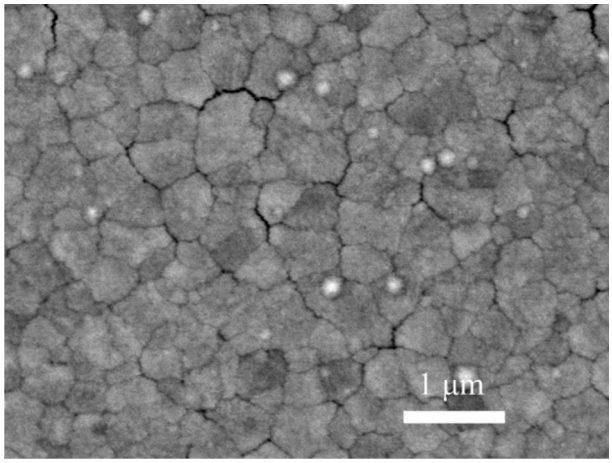
3.2 Characterization of the $PbZr_{0.3}Ti_{0.7}O_3$/Al_2O_3/SiO_2/Si structure

In the next step, the $PbZr_{0.3}Ti_{0.7}O_3$ solution was spin coated on the Al_2O_3/SiO_2/Si substrate and the film was annealed two times, i.e., after the second and the fourth depositions of the solution, at 550°C for 15 min. A cross-section SEM micrograph of the $PbZr_{0.3}Ti_{0.7}O_3$/Al_2O_3/SiO_2/Si structure is shown in Figure 5(a); the surface of the upper PZT layer is shown in Figure 5(b). The PZT film on the Al_2O_3/SiO_2/Si substrate is ~300-nm-thick and the thickness is uniform within the investigated range. It consists of a few-hundred-nm-sized, irregularly shaped grains. In the surface microstructure, the boundaries between the grains are clearly visible. Besides larger PZT grains, some small, white, round inclusions of a lead-rich secondary phase are also seen at the PZT grain boundaries. A similar microstructure for a PZT thin film on a platinized silicon substrate was observed by Kosec et al.[17] The authors explained that up to 4-μm-sized grains of PZT are formed due to the small number of nucleation sites.[17] The PbO secondary phase at the PZT surface was also observed by Bursill et al.[18]

In Figure 6, the X-ray powder-diffraction pattern of the $PbZr_{0.3}Ti_{0.7}O_3$/Al_2O_3/SiO_2/Si structure is shown. High-in-



(a)



(b)

Figure 5: SEM-BE micrographs of the $PbZr_{0.3}Ti_{0.7}O_3/Al_2O_3/SiO_2/Si$ structure (a), the surface of the PZT layer on the $Al_2O_3/SiO_2/Si$ substrate (b), after annealing at 550°C.

tensity peaks marked with hkl indices can be ascribed to the randomly oriented perovskite PZT phase with the tetragonal symmetry; however, no {00l} reflections were detected. Evidently, the PZT film is a-axis oriented, which in other words means that the c-axis of the PZT unit cell is parallel with the $Al_2O_3/SiO_2/Si$ substrate. Such an orientation of the $Pb(Zr,Ti)O_3$ film on the silicon substrate is a consequence of the tensile stresses within the multilayered structure that develop during cooling.[19,20] A low-intensity reflection at $2\Theta=29^o$, which could be ascribed to PbO, was also observed. The XRD results are in accordance with the SEM analysis, where besides the larger perovskite PZT grains, smaller round inclusions of lead oxide at the grain boundaries between the PZT grains were observed (see Figure 5).

In order to analyze the $PbZr_{0.3}Ti_{0.7}O_3/Al_2O_3/SiO_2/Si$ structure at the nano level the TEM analysis was performed (Figure 7(a)). An enlarged view of the PZT layer is shown in Figure 7(b) and the boundaries between the PZT–Al_2O_3–SiO_2 layers in Figure 7(c). A dense, ~300-nm-

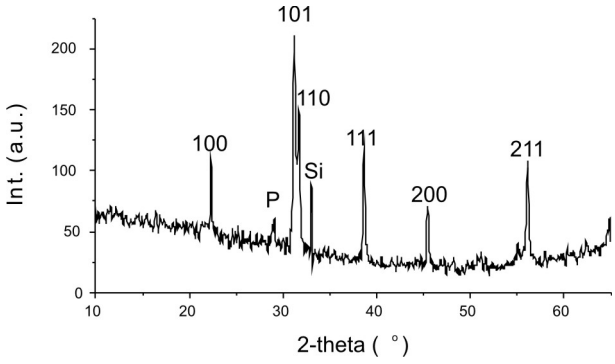


Figure 6: XRD pattern of the $PbZr_{0.3}Ti_{0.7}O_3/Al_2O_3/SiO_2/Si$ structure after annealing at 550°C. Peaks belonging to the tetragonal $PbZr_{0.3}Ti_{0.7}O_3$ perovskite phase (ICSD 90473) are marked with hkl, the peak belonging to the silicon substrate (PDF 01-072-1088) is marked with Si, the peak marked with P could be indexed with the orthorhombic PbO (PDF 01-072-0094).

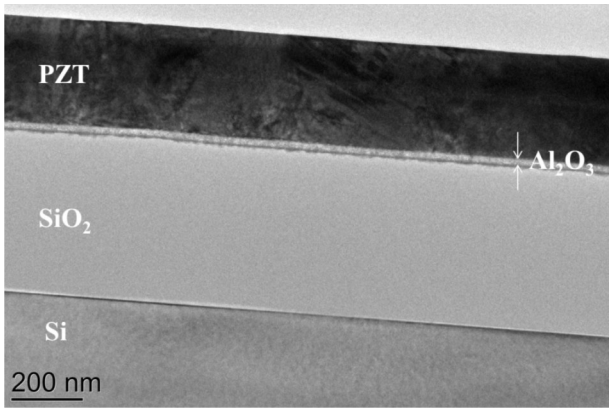
thick PZT layer is observed on the top of the thin polycrystalline alumina layer with a uniform thickness. The PZT layer consists of ~300-nm-sized grains. Small pores are visible within the PZT layer. The SAED pattern of the PZT grain, shown in Figure 7(b), was indexed with the tetragonal $PbZr_{0.3}Ti_{0.7}O_3$ unit cell (a, b=3.978 Å and c=4.148 Å, SG: P4mm, ICSD #90473). According to the diffraction pattern the PZT grain is oriented in the <001> zone axis. The c-axis of the perovskite grain is perpendicular to the observed plane, i.e., it is parallel to the $Al_2O_3/SiO_2/Si$ substrate. The result is in accordance with the XRD data, where an a-axis-oriented PZT film was observed (Figure 6).

However, a closer look at the structure (Figure 7(c)) shows that an intermediate layer of amorphous secondary phase is formed between the alumina and the SiO_2. A maximum thickness of the secondary phase is around 10 nm.

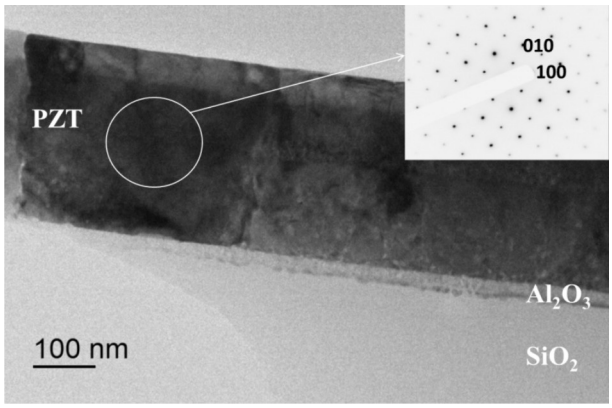
In order to determine the chemical composition of the secondary phase, a TEM-EDXS analysis was performed through all the layers, as shown in Figure 8.

According to the EDXS analysis, the intermediate layer below the Al_2O_3 contains Al, Si, O and Pb, indicating that PbO diffused through the alumina layer towards the substrate. In the PZT and alumina concentration profiles, silicon is also present, most probably due to the sputtering of silicon during the preparation of the TEM sample.

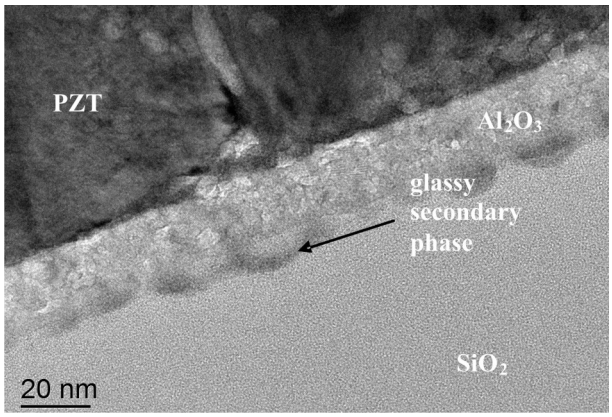
To conclude, although the nanosized Al-Si-Pb-O-containing amorphous phase was formed below the alumina layer, no lead-deficient pyrochlore phase was observed in the PZT film. Presumably, the small amount of diffusion of PbO from the PZT to the Si was compen-



(a)



(b)



(c)

Figure 7: Cross-section TEM micrographs (bright-field) of $PbZr_{0.3}Ti_{0.7}O_3/Al_2O_3/SiO_2/Si$ structure (a), enlarged view of the PZT layer with SAED of the tetragonal perovskite PZT grain in the <100> zone axis (b) and the boundaries between the SiO_2, Al_2O_3, and PZT layers (c).

sated with an excess of PbO used in the starting precursors. It seems that the alumina layer is not thick enough (~20 nm) to prevent lead oxide diffusion from the PZT towards the Si substrate completely, and thus, a thicker alumina layer would be needed.

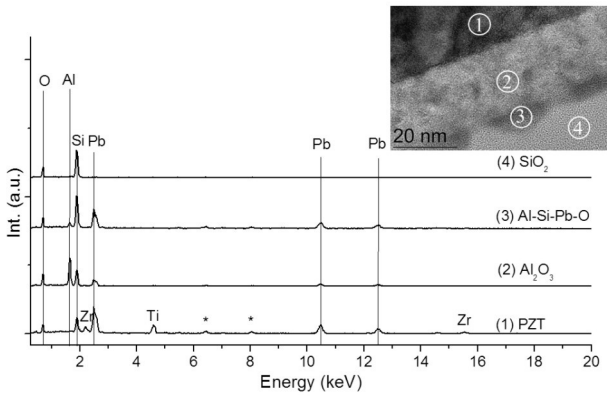


Figure 8: TEM - EDXS patterns obtained from the $PbZr_{0.3}Ti_{0.7}O_3/Al_2O_3/SiO_2/Si$ structure. Inset: On the HR-TEM image the regions where the analyses were performed are marked.

4 Conclusions

A dense, nanocrystalline layer of γ-alumina oxide was successfully synthesized on a silicon substrate using the sol-gel method. After the deposition and annealing at 900°C for 1 hour an ~20-nm-thick alumina layer was obtained, and investigated as a buffer layer between the $PbZr_{0.3}Ti_{0.7}O_3$ (PZT) layer and the silicon substrate. An a-axis-oriented tetragonal PZT film was obtained on the $Al_2O_3/SiO_2/Si$ substrate after annealing at 550°C. The PZT layer is ~300-nm-thick and consists of ~300-nm-sized grains. According to the TEM-EDXS analysis, an additional, up to 10 nm, Al-Si-Pb-O phase was observed below the alumina layer, indicating that a minor diffusion of lead oxide through the alumina layer into the silicon took place during the annealing at 550°C.

5 Acknowledgment

This work was supported by the Slovenian Research Agency PR-05024. The authors would like to thank Jena Cilenšek, Silvo Drnovšek, Brigita Kmet and Goran Drazic for support in the experimental work. Authors also acknowledge the Center of Excellence Nanoscience and Nanotechnology for access to the FIB.

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Lead zirconate titanate multi-element structure by electrophoretic deposition

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Abstract: Processing of aligned piezoelectric elements for multi-element linear-array transducers was studied. Transducers consist of six rectangular elements with a length of about 6 mm, a width of 1.1 mm and a distance between them of about 0.4 mm. Lead zirconate titanate (PZT) elements were prepared on metalized alumina substrates by electrophoretic deposition (EPD) process and sintering. PZT and PbO particles were dispersed in ethanol and deposited on the substrate at a constant current. After the sintering at 950°C, uniform elements with a thickness of around 20 µm and a density around 83 % were obtained. The space between elements, i.e., a kerf, was filled with an epoxy resin. Electrical contacts of each element were performed using wedge bonding and a six element structure was electromechanically characterized. A thickness mode coupling factor (kt) of around 17 %, a resonance frequency of around 70 MHz (in free mechanical conditions), a dielectric constant of around 370 were measured. A good reproducibility was observed. Limitations of the EPD method in terms of spatial resolutions for patterning very small piezoelectric elements are discussed and results show that EPD is a promising process for high frequency linear array applications.

This work is dedicated to the late Professor Marija Kosec

Keywords: Electrophoretic deposition, piezoelectric thick film, multi-element transducer, ultrasound applications.

Večelementna struktura svinčev cirkonat titanat z elektroforetskim nanosom

Izvleček: Študirali smo pripravo piezoelektričnih elementov za ultrazvočne pretvornike. Pretvornik je bil sestavljen iz linearnega niza šestih elementov z dolžino 6 mm in širino 1 mm, razdalja med posameznimi elementi je bila 0.5 mm. Elemente na osnovi svinčevega cirkonata titanat (PZT) smo pripravili na metalizirani korundni podlagi z metodo elektroforetskega nanosa (EPD). Delce PZT in svinčevega oksida smo dispergirali v etanolu ter jih v ustreznem stehiometričnem razmerju z EPD nanesli na podlago pri konstantnem toku. Po žganju pri 950°C so imeli elementi debelino okoli 20 µm, homogeno mikrostrukturo in gostoto okoli 83 %. Presledke med posameznimi elementi (ang. kerf) smo zapolnili z epoksidno smolo, nanesli zgornjo elektrodo ter izmerili elektromehanske lastnosti posameznih elementov. Povprečni sklopitveni faktor piezoelektričnega elementa je bil 17 %, dielektrična konstanta okoli 370 in resonančna frekvenca okoli 70 MHz. Rezultati meritev posameznih elementov so bili podobni. V prispevku poročamo tudi o možnostih oblikovanja debeloplastnih struktur z EPD ter navajamo omejitve metode predvsem s stališča ločljivosti. Rezultati raziskave so pokazali, da je opisana metoda primerna za pripravo visokofrekvenčnih pretvornikov, sestavljenih iz linearnega niza piezoelektričnih elementov.

Ključne besede: Elektroforetski nanos, piezoelektrične debele plasti, ultrazvočni pretvorniki, ultrazvok

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1 Introduction

Ultrasound techniques are widely used for non-destructive testing as well as medical investigations. For imaging small biological structures such as skin and eyes, the ultrasonic transducers have to operate at frequencies over 20 MHz to reach spatial resolutions lower than 100 micrometers [1-2].

High frequency (HF) single element transducers were extensively studied. These transducers consist of few tens of micrometers thick piezoelectric elements deposited onto a mechanical support. The piezoelectric material is the most important component of the transducer because its characteristics together with its geometry mainly define the properties of the transducer, in particular its operating frequency and sensitivity [3].

Transducers with good performance were obtained using different technologies for the piezoelectric thick film fabrication such as screen-printing [4-6], pad printing [7-9] and composite sol-gel [10-12], in a wide range of frequencies from 15 to 70 MHz. The main disadvantages of single element transducers are a fixed focal distance which leads to a limited depth of field. Moreover, to perform mode-B imaging [13], the transducer must be inserted into a probe which ensures a mechanical movement. Consequently, a limited frame rate is obtained.

Since the early 2000's, high-frequency multi-element transducers have been studied and developed.

Annular arrays [14-15] with typically 5 to 8 ring-shaped-elements are used and a variable focal distance is obtained by changing the delays applied on the electrical excitation and received signals. However, the mechanical movement is always required. Linear arrays consist of a higher number of elements, e.g., 64, 128 or 256, but scanning and focusing are completely managed by electronics. However, the technological implementation of such transducers is much more complex [16-17]. In particular, the fabrication of the multilayer structure (backing, piezoelectric layer with elements and matching layers) is a challenge mainly due to the micrometer-size of rectangular piezoelectric elements with a thickness of few tens of micrometers. As an example, for a linear array transducer operating at 50 MHz, an element width around 25 µm, a space between elements (kerf) around 10 µm and a thickness around 30 µm are needed [18]. Cannata *et al* [19] designed a kerfless linear array transducer to simplify its fabrication procedure. Their design was based on a uniform piezoelectric layer. The individual elements were obtained simply by shaping the bottom electrode or the top electrode or both. However, they reported that the crosstalk between elements was significant both electrically and mechanically, which reduces the performance of the transducer and in particular the piezoelectric element directivity [20]. Foster *et al*. [21] used laser-machining to dice and sub-dice the elements from a piezoelectric layer to fabricate a HF linear array with very low kerf value. They prepared an efficient linear array transducer with 256 elements that was operated at a resonant frequency of 40 MHz.

1-3 or 2-2 piezo-composites were also used as the piezoelectric layer for high frequency linear array fabrication [22-23]. In such structures, cross-talk is naturally reduced and kerfless structure or partial cuts between elements were used. Moreover, due to polymer content, the piezocomposite is flexible, which is often used to obtain geometric focusing along the elevation [24-26]. At frequencies above 20 MHz, the typical size of the periodic microstructure of a composite (alternatively constituted of piezoelectric rods or layers and polymer) must be very low, typically around ten micrometers. Good performance was obtained but required highly technical and costly processes.

Recently, electrophoretic deposition (EPD) was used to process piezoelectric thick films on a complex-shape substrate and thus to fabricate efficient, geometrically-focused single element transducers [27]. EPD is an adaptive and low cost method enabling the deposition of various materials on a complex-shape conductive substrate. The charged particles dispersed in a solvent can be deposited on an electrode, e.g., a metalized substrate, by applying a DC electric field between it and a counter-electrode [28-30]. To process piezoelectric thick films with desired microstructure and functional response, the properties of the suspension, the deposition process as well as the drying and sintering procedure have to be optimized [31].

The purpose of the present study was to deposit rectangular piezoelectric elements for high frequency transducers with a straightforward procedure to test the compatibility of electrophoretic deposition with the development of a high frequency linear array.

We report here the results on patterning of lead zirconate titanate thick film structures by EPD and consequent sintering. The simple prototype linear array transducer consisting of six piezoelectric elements, has been prepared. The electromechanical properties in thickness mode of each individual element were measured. Finally, the use of EPD to fabricate array elements with very small sizes originally defined in 2D thanks to conductive electrodes is evaluated and quantified.

2 Experimental procedure

2.1 Substrate preparation and thick film fabrication

Dense alumina substrates, namely Al_2O_3 (Kyocera A493) with dimensions 12 mm x 12 mm and a thickness of 640 µm were used. A gold paste (8884-G, ESL) was screen-printed onto the Al_2O_3 and fired at 900°C for 10 min to deliver six aligned rectangles with a length of 6 mm, a width of 1 mm and a space between them of 500 µm. These golded substrates are denoted Au/Al_2O_3. A photograph of the electroded substrate is presented in Figure 1. The acoustical properties of dense alumina are reported elsewhere [32]. Additional gold lines were screen-printed at the same time to simplify the electrical contact for the future transducer fabrication.

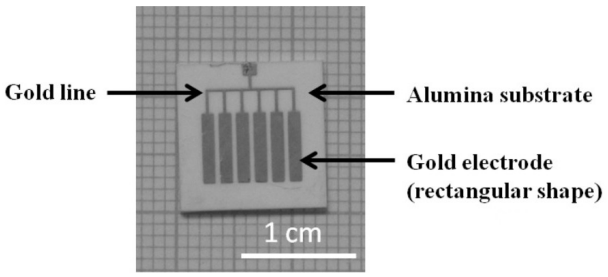

Figure 1: Representative Au/Al_2O_3 structure consisting of 6 aligned rectangular gold electrodes with a length of 6 mm, a width of 1 mm and a space between electrodes of 500 µm.

$Pb(Zr_{0.53}Ti_{0.47})O_3$ powder (PZT) was prepared by solid state synthesis from PbO (99.9+ %, Aldrich), ZrO_2 (99.9 %, Tosoh) and TiO_2 (99.9 %, Alfa Aesar). The homogeneous mixture was calcined at 950 °C. After the calcination the powder was milled for 8 h in an attritor mill. Details are given in [33].

PZT and PbO suspension with a solid load content of 1 vol. % was prepared. PZT and PbO particles were dispersed in ethanol using polyacrylic acid (PAA, Alfa Aesar, M_v 2000) and n-butylamine (BA, Alfa Aesar). The procedure is reported in [33]. The suspension for EPD was prepared by mixing PZT and PbO suspensions in stoichiometry 98 mol % PZT and 2 mol % PbO and is denoted as PZT-PbO.

The zeta-potentials of PZT and PbO particles in ethanol were measured at room temperature using a ZetaPals zeta-potential analyzer (Brookhaven Instruments). The conductivity of the suspension was measured at room temperature using a Cond 730 Inolab system.

EPD was performed at room temperature in a horizontal electrode cell with two Au/Al_2O_3 identical substrates, acting as a cathode and an anode. The distance between the electrodes was 25 mm. The area of the whole conductive surface was 42 mm^2. The deposition was performed at a constant current density of 2.38 mA/cm^2 for 40 sec using a Keithley 2400 generator (Keithley Instruments Inc., Cleveland, USA).

The as-deposited layers were sintered at 950°C for 2 hours with heating and cooling rates of 2°C/min in a lead oxide rich atmosphere provided by $PbZrO_3$/PbO packing powder.

The thickness and the surface of as-deposited dried layers were investigated by a profilometer (Viking 100 Solarius Inc.).

The microstructures of sintered thick films were characterized with a scanning electron microscope (SEM) (JEOL 5800, Japan). The microstructure was prepared by cutting samples into two pieces and mounting them in parallel in epoxy resin, grinded and polished. A small layer of carbon was deposited on the top of the microstructure in epoxy.

The density of the sintered thick film was obtained by a quantitative characterization of the ceramic microstructure. This characterization was obtained from SEM images converted to binary ones using an image analysis software (ImageTools 3.0, University of Texas Health Science Center, USA) to determine the volume fraction of pores [34]. We quantified the black and white pixels of the binary images and calculated the percentage of the porosity by dividing the number of black pixels by their total amount. An experimental error of ± 3 % is estimated.

2.2 Preparation and characterization of the prototype

After sintering, the spaces (kerfs) between piezoelectric elements were filled with epoxy resin. To perform the electromechanical characterization, a 100 nm thick top gold electrode was sputtered on the whole area of the sample. The six-element structure was poled at 150°C for 10 min in an oil bath with an electric field of 6 kV/mm.
After poling, the six elements numbered 1-6 were electrically separated and the structure was glued on a Printed Circuit Board (PCB) substrate with additional copper connection to facilitate electrical contacts. The electrical connections between copper lines and elements through gold wires were performed by wedge bonding. Finally, epoxy resin was added on the gold wires to protect these connections. A photograph of the demonstrator is shown in Figure 2.

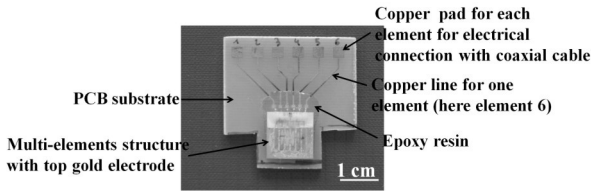

Figure 2: Photograph of the demonstrator.

The electromechanical properties of the piezoelectric thick film structures were deduced from the measurement of the complex electrical impedance around the fundamental thickness mode resonance. A HP 4395 vector analyzer and an impedance test kit were used. The theoretical behavior of the electrical impedance was computed as a function of frequency for the thickness mode using a one-dimensional model based on the KLM equivalent electrical circuit [35-36]. Then a fitting process was used to deduce the thickness mode parameters of the EPD piezoelectric thick films from the experimental data [6, 12, 37].

For one piezoelectric element, the structure along the thickness is composed of four layers, *i.e,* three passive and the active thick film. The passive layers are the alumina substrate and the two gold electrodes. The parameters of these layers are fed in the KLM model and considered as constants [9, 32]. Parameters for the flat alumina substrate are given in [27].
Finally, five thickness mode parameters of the thick film were deduced: the longitudinal wave velocity v_l, the dielectric constant at constant strain $\varepsilon_{33}^S/\varepsilon_0$, the effective thickness coupling factor k_t and the loss factors (mechanical δ_m, electrical δ_e).

For the measurement of the electroacoustic responses of the elements, a 50 Ohms coaxial cable with a length of around 30 cm, was used. Two electrical contacts were performed. One on the copper pad (see Figure 2) corresponding to the desired piezoelectric element and the other on the top gold electrode, which is common for all elements using conductive epoxy resin. Each element was characterized in pulse-echo mode on a brass target in water. An AVTEC AVG–3B –C impulse generator (Avtech Electrosystems Ltd., Ottawa, Canada) was used for the electrical excitation. Reception was performed with a home-made high frequency receiver.

3 Results and discussion

For EPD, the suspension that contains PZT and PbO particles dispersed in an ethanol was used. The zeta potential of - 50 ± 5 mV and - 40 ± 5 mV were obtained for PZT and PbO, respectively. The conductivity of PZT-PbO suspension was 18 µS/cm at 24°C. The high negative value of the zeta potential indicates that the negatively charged particles are well dispersed in a solvent. The low value of the conductivity is favorable for the deposition process [38]. During the EPD process, the piezoelectric layer is deposited onto the positively charged Au/Al_2O_3 substrate.

The uniformity of the as-deposited six elements on Au/Al_2O_3 was investigated by a profilometer. The image and the profile in A-A direction are shown in Figure 3a and b, respectively. From the profile image, it is evident that the edges of all the lines are thicker that their centers. The variations in the thickness may be related to the non-uniform electric field applied during the EPD. In between the lines we have not detected any deposit. No micro defects such as cracks were observed. The as-deposited elements had a thickness around 50 micrometers

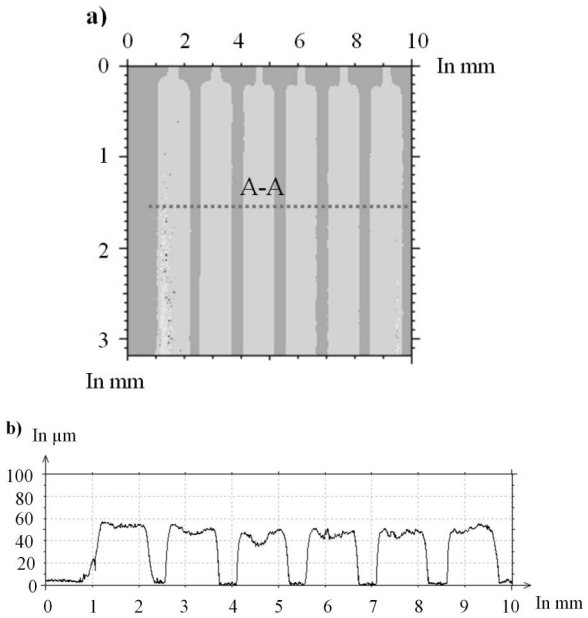

Figure 3: a) Image of the six as-deposited elements on Au/Al_2O_3. b) Profile of the six as-deposited elements on Au/Al_2O_3 measured by profilometer.

The sintered samples were analyzed by SEM in order to determine precisely the thickness of the elements, their width and the kerf. Microstructures of PZT-PbO elements in cross-sectional orientation sintered at 950°C are shown in Figure 4. Good adhesion between PZT-PbO and Au/Al_2O_3 is evident and no delamination of electrode and/or PZT-PbO from the substrate was detected.

The thickness of the film is not uniform and varies from about 18 ± 3 µm in the middle to about the 30 ± 3 µm at the edge of the elements as evident from the Figure 4. The thickness is based on the measurement of six elements and the average value is given. It is also seen

that the PZT elements were wider than the size of the gold bottom electrode of about 100 µm. Consequently, a kerf around 400 µm was measured. From Figure 4c it is evident that the PZT-PbO is homogeneous and consists of micrometer sized grains. The density of the layer calculated by stereological analysis was 6.640 g/cm^3, corresponding to 83 ± 3 % of the theoretical density.

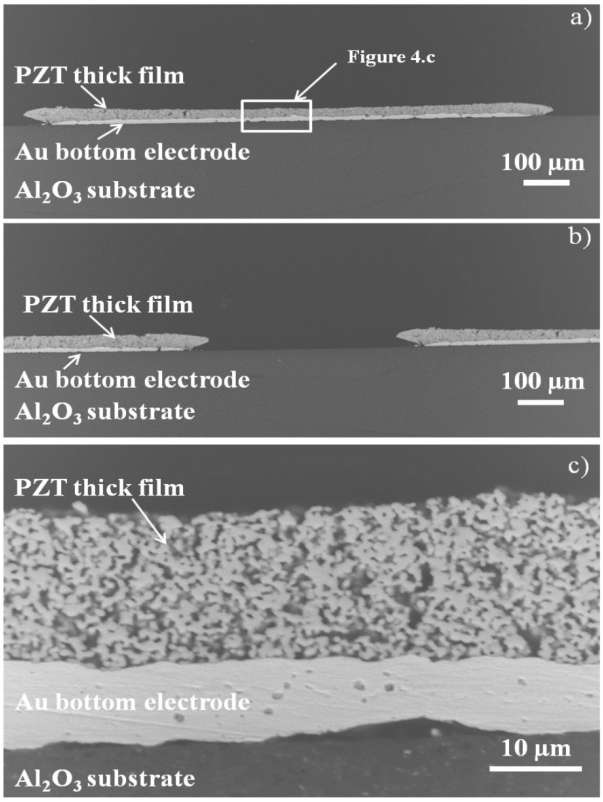

Figure 4: PZT-PbO thick films on a flat Au/Al_2O_3 substrate sintered at 950 °C for 2 h. SEM cross section image of a) one element; b) two elements and kerf in the middle. c) Inset from Figure 1a) (magnification x 2000)

3.1 Electromechanical properties of the structure

Impedance measurements were performed on the 6 elements. For the first two elements (numbered 1 and 2), electrical connections were strongly degraded and measurements were not exploitable. Consequently, experimental results from elements 3 to 6 were used. Figure 5 represents the electrical impedances (experimental and theoretical) in air of a representative element in the structure.

The extracted parameters from impedance curves of the 4 elements are summarized in Table I. For the calculation, we used the thickness measured at the center of the element (which represents the majority of the whole element area), which was about 20 µm. The results were compared to those on sample "Ref_PZT-PbO" published in a previous study [39]. The "Ref_PZT-PbO" thick film was prepared from the same suspension as the multi-element structure in this study. It was deposited at identical conditions, i.e., for 60 sec on a surface of 64 mm^2. After the sintering, the thickness of the sample was uniform, i.e., 20 µm, and a density of 83 ± 2 % was found.

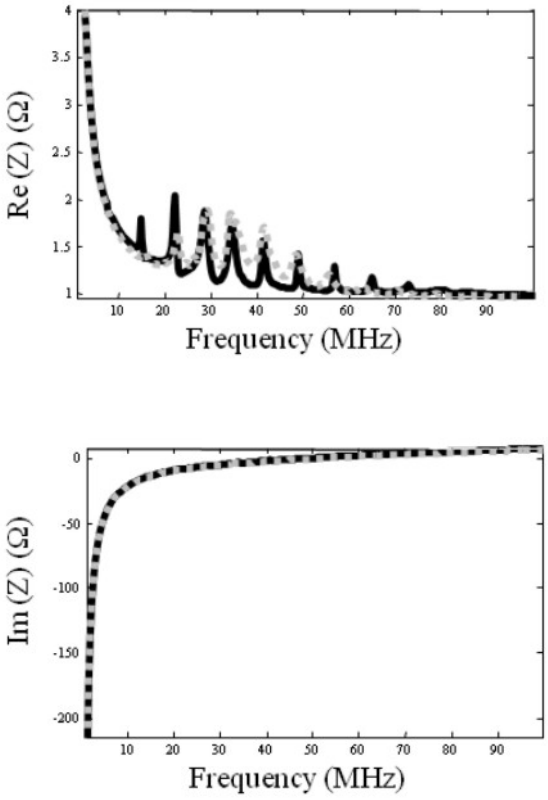

Figure 5: Complex electrical impedance of one element (number 5) in air as a function of frequency around the fundamental resonance (black solid line: theoretical, gray dashed line: experimental).

Table 1: *t*: thickness, v_l: the longitudinal wave velocity, $\varepsilon^S_{33}/\varepsilon_0$: dielectric constant at constant strain, δ_m: mechanical losses, δ_e: dielectric losses, f_0: thick film resonance frequency (in free mechanical conditions).

Sample	t (µm)	v_l (m/s)	k_t (%)	$\varepsilon^S_{33}/\varepsilon_0$	δ_m (%)	δ_e (%)	f_0 (MHz)
Element 3	20	2850	17	360	22	3	71
Element 4	19	2790	17	350	17	3	70
Element 5	20	2900	20	410	20	3	72
Element 6	20	2850	15	390	17	3	71
Ref_PZT-PbO ([39])	20	2780	48	320	6	1	69

The four elements have a higher longitudinal wave velocity and dielectric constant than the PZT-PbO thick film considered as reference [39].

A lower porosity content in the four elements can explain these differences. Mechanical losses were also significantly higher in the four elements than in the reference sample. This could be explained by the non-uniformity of the thickness of the four elements. Indeed, when using the KLM model to extract parameters, a constant thickness was assumed; consequently, mechanical losses were overestimated.

The main difference observed between the four elements and the reference sample was the thickness coupling factor which was about 17 ± 2 % for the four elements, while it was 48 % for the reference sample. The higher k_t for the reference samples may be related to the more efficient pooling that was performed at 12 kV/mm. The electric field of 6 kV/mm was evidently too low, therefore the poling procedure for the piezoelectric rectangular elements must be optimized. Finally, it is also important to notice the good reproducibility of the electromechanical properties and dimensions measured on the four elements. This reproducibility attests that linear arrays with higher number of element are feasible by such a process.

3.2 Electroacoustic response of a representative element

Figure 6 a represents the pulse-echo response of a representative element (number 5). In this configuration, only one element is excited while other elements stay with floating electric potential. The sensitivity S=20.log10 (U_e/U_r), where U_e and U_r are the excitation and reception peak voltages, was evaluated from the received voltage in pulse-echo mode. The sensitivity was -45 dB. The bandwidth at -6 dB deduced from the frequency response (Figure 6.b) has a value of 16 MHz and a center frequency of 42 MHz (which corresponds to a fractional bandwidth at -6dB of 38 %). These delivered electro-acoustic properties confirm the high potential of the EPD process. But in this configuration, the alumina substrate was not an ideal material to be used as backing for three main reasons. The attenuation in this material is low (typically 0.06 dB.mm [32]) and the thickness of the substrate in not sufficiently high to avoid back wall echoes. In fact, Figure 6 a represents only the first echo corresponding to the electro-acoustic response of the structure, but additional echoes follow due to multiple reflections in the substrate. Moreover, acoustical impedance of the alumina substrate is twice that of the piezoelectric element and this large difference limits the bandwidth of the electro-acoustic response. For medical imaging applications, a bandwidth higher than 50 % is required. In the future, a material with sufficiently high attenuation and lower acoustical impedance must replace alumina substrate. Unpoled porous PZT material is a viable option for properties and compatibility with the EPD process. This material was already used for single element transducers [6]. For this study, the objective was to demonstrate the potential of the EPD process and the alumina substrate was chosen in order to guarantee a good accuracy for the measured electromechanical properties (typically the thickness coupling factor) [12].

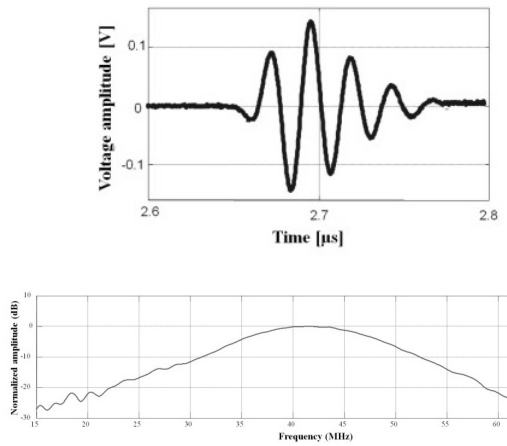

Figure 6: Experimental electro-acoustic responses for the element number 5 of the multi-element structure. (a) time response and (b) frequency response.

4 Conclusions

The electrophoretic deposition process was used for the fabrication of piezoelectric PZT-PbO thick films on flat Au/Al_2O_3 substrates for ultrasonic high frequency linear array configurations. After the sintering, the piezoelectric elements had a rectangular shape with a width of 1.1 mm and a kerf of 400 µm. The thickness of the films of around 20 µm delivered ultrasound frequencies over 30 MHz, which is well adapted to high resolution medical imaging applications.

The elements are characterized by a dielectric constant of 370, a coupling factor around 17 % and a longitudinal wave velocity around 2800 m/s. For an optimized high frequency linear array configuration, the width of elements and kerf need to be significantly reduced as mentioned in the introduction. The most critical step will be to minimize the kerf value to a few tens of micrometers while keeping the "Π shape" of the elements. For that, several routes are already planned and a modified experimental protocol for EPD will be tested. The electromechanical performance of all elements is similar but still needs to be improved by optimizing the poling conditions. Nevertheless, high reproducibility of elements in terms of shape and performance suggests that EPD can be considered as a promising process for the fabrication of high frequency linear arrays.

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Supercapacitor Energy Storage System for Improving the Power flow in Photovoltaic Plants

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Abstract: Recently new elements have been added to the distribution grids which have changed the way the grids operate; this change in performance can affect the safety and reliability of management of the distribution grids. The disadvantages due to the changes in energy production justify the search for power injection systems capable of damping these changes. It is necessary that these power injection systems change their passive performance in the grid, becoming active elements that are integrated into the management of it, obtaining not only no negative effects on the grid, but also enhancing its reliability and operating possibilities. One of the major drawbacks of renewable energy generation is the change in energy production. This justifies the search for power injection systems capable of absorbing such fluctuations. In this paper, we present an injection system capable of integrating a photovoltaic generation system as a quasi-manageable generation system, incorporating the energy storage to moderate fluctuations in the energy generated, using a set of supercapacitors. With these functions, the inverters will become active parts of the grid, developing the concept of smart grid, which is generally accepted as the evolution of the current grid towards the one that will exist in the future. The system is composed of a voltage source inverter that injects the power into the grid, while a bidirectional direct current converter regulates the charge of the supercapacitor.

Keywords: Photovoltaic Plants, Power Injection Systems, Solar Energy, Energy Storage System, Supercapacitor

Sistem hranjenja energije s super kondenzatorjem za izboljšanje pretoka energije v fotonapetostnih sistemih

Izvleček: Nedavno se je v električno omrežje dodalo nove elemente, ki vplivajo na učinkovitost varnost in zanesljivost omrežij. Ta slabost potrjuje iskanje sistemov, ki zmanjšujejo njihov vpliv na omrežja. Pomembno je, da ti pasivni sistemi postanejo aktivni in ne zmanjšujejo le negativnih vplivov temveč celo izboljšujejo omrežja. Ena izmed glavni slabosti obnovljivih virov energije je njihova spremenljivost proizvodnje. V članku je predstavljen sistem, ki je sposoben omiliti vplive fluktuacij obnovljivih virov energije s vključitvijo hranilnikov energije v obliki super kondenzatorjev.

Ključne besede: fotonapetostni sistemi, napajalni sitemi, sončna energija, hranilniki energije, super kondenzatorji

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1 Introduction

During the last few years, due to the regulatory framework for renewable energy, the number of Photovoltaic Generation Systems (PVGS) connected to the grid is experiencing a dramatic increase.

One of the main disadvantages of photovoltaic generation is that it limits the power granted to the evacuation points, due to its consideration as an unmanageable power source, which prevents ensuring the dynamic stability of the grid.

So that the PVGS do not affect the behavior of the grid, they must not only meet the supply to the grid specifications about quality and reliability, but must also ensure their successful integration, controlling the power generation curve. The generation curve is

highly dependent on climatic conditions [1] making its prediction and integration difficult in a planned system of generation [2], [3]. At present, these problems will not seriously affect the operation of the grid, but could become important in a near future with the present forecasting for integrating unmanaged renewable energy sources.

One possible solution to this problem could be that the photovoltaic generation systems acted as "quasi-manageable", generating energy at constant power during periods of time, whose value will be communicated previously to the manager responsible of the grid to which it connects. In order to function in this way, an energy storage system is needed, whose design, sizing and composition is determined in this article.

With this function, inverters will become active parts of the grid, able to assist in the management, planning and operation of these grids, achieving one of the main objectives in research and development of the European technological platform of smart grids.

PVGSs generated power fluctuations produce, in many cases, inversions of the net power flows in the head of the lines where they are connected. Fig. 1 shows the power measured in a line of the substation (Fig. 2) belonging to a rural meshed distribution grids, where there is a 1 MWp PVGS and less than 200 conventional customers (that sum up about 5 MW of contracted power capacity). Fig. 2 has been obtained using a Power Quality Meter (Topas 1000), and one can observe that there are not only rapid fluctuations of power, but also inversions of the net power flow in the line.

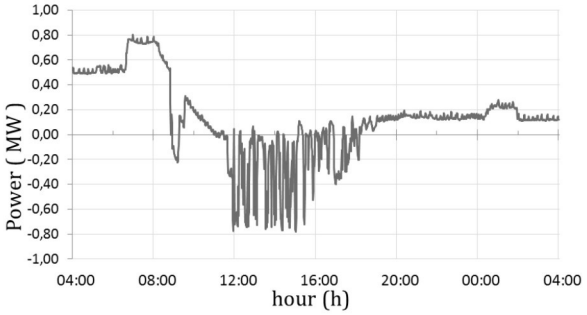


Figure 1: Power exiting the substation versus the time of the day.

Conventional power injection systems (PIS) of PVGSs are not designed to avoid these fluctuations. These systems usually consist of a DC-DC converter, which adapts the voltage of the photovoltaic system and tracks the maximum power point (MPPT), and of an inverter that converts DC-voltage into alternating voltage, controlling the current that is injected into the grid and seeking the power factor to be one [1].

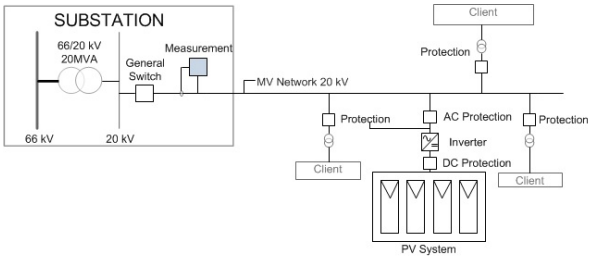


Figure 2: Installation diagram for the analyzer in the Substation.

Some effects of power fluctuation into the grid have been observed, for example, sudden drops in output power of 25 % in less than 3 minutes, especially in suburban and rural grids, and significant changes in the expected energy flow causing operational problems [3], [4].

In this paper, to give the PIS capacity to mitigate power fluctuations, it is necessary to include in its structure a storage element capable of absorbing energy.

This paper describes the principal energy storage technologies and discusses the possibility of using a supercapacitor energy storage system and shows how to integrate it. A supercapacitor energy storage system has been selected because it is easy to implement in present PIS structures and stores the energy in its original electrical form. Therefore, this technology is incipient and it is expected that it will have a great development in a near future.

2 Energy storage systems

To ensure continuity of supply in an environment in which a significant percentage of generation comes from renewable energy sources, Energy Storage Systems (ESS) are needed. This is one of the ideas behind the establishment of micro-grid concept. In addition, having an ESS could palliate the unmanageable nature of these sources of energy, allowing the set of PVGS and ESS to generate a constant power, eliminating or diminishing the fluctuations in the power generated by the PVGS.

Currently the feasibility of micro-grid is being analyzed, which could be managed as islands (or management areas that attempt to balance generation and consumption). These micro-grid would be interconnected, and would have generation systems, mainly from renewable sources (wind, photovoltaic,...) with the corresponding ESS. These ESSs could be made with different technologies, such as batteries, inertia frills, supercapacitors, or superconducting magnets [1].

In the design of future PIS for PVGS, in a context of gradual increase in the percentage of generation by these plants, the ESS will be of great importance, mainly because of the need to manage and optimize the flow of energy from such sources. Recent studies consulted use systems with batteries, supercapacitors or a hybrid of both [5].

The principal ESS and the most relevant ESS technology characteristics are summarized in Table I [6].

Table 1: Energy storage technologies

Technology	Power	Energy density	Back-up time	Response time	Efficiency	Lifetime(years)
Pumped hydro	100 MW – 2 GW	400 MWh – 20 GWh	hours	12 minutes	70 - 80 %	50
CAES	110 MW – 290 MW	1.16 GWh - 3 GWh	hours	12 minutes	90 %	< 50
BESS	100 W – 100 MW	1 kWh - 200 MWh	hours	seconds	60 - 80 %	< 10
Flywheels	5 kW – 90 MW	5 kWh – 200 kWh	minutes	12 minutes	80 - 85 %	20
SMES	170 kW – 100 MW	110 Wh – 27 kWh	seconds	milliseconds	95%	30
Supercapacitors	< 1 MW	1 Wh- 1kWh	seconds	milliseconds	> 95%	> 10

2.1 CAES (Compressed Air Energy Storage)

CAES uses the peaks of energy generated by renewable energy plants to run a compressor that compresses the air into a hermetic underground reservoir or surface vessel/piping. The compressed air is used, combined with a variety of fuels in a combustion turbine to generate electric energy when demand is high. The energy storage capacity depends on deposit volume and maximum storage pressure of the compressed air [6].

2.2 Pumped Hydroelectric

Pumped hydroelectric storage has been commonly used for 70 years. These plants are the most used for large scale applications at present [7].

2.3 Superconducting Magnets

A Superconducting Magnetic Energy Storage (SMES) system stores the energy as magnetic energy in a superconducting magnet cryogenically cooled, achieving a system with negligible losses. The AC energy is stored as DC energy and brought back from DC to AC energy from the superconducting magnet by a reversible AC/DC Power Converter Module (PCM).
The energy stored by an SMES is

$$E = \frac{1}{2} LI^2 \tag{1}$$

where L is the equivalent self-inductance of the superconductor system, and I is the DC current that flows through the winding. This current is the principal magnitude that the PCM uses for controlling the energy stored or generated by the system.

SMES efficiency is between 95 % and 98 %. It has a high availability, being able to supply high energy quantity in time intervals of milliseconds [9].

The main disadvantage of the SMES system is that the energy density is low and there is a need for a cryogenization system that could be very complex for large scale application. A possible solution is to combine them in hybrid ESS increasing their energy and power [10].

2.4 Flywheels

Due to their simplicity, flywheel energy storage systems (FESS) have been widely used in commercial small units (about 3 kWh) [10].

Energy is stored as kinetic energy using a rotor that rotates with high angular speed

$$E = \frac{1}{2} J\omega^2 \tag{2}$$

where J is the momentum of inertia and ω is the angular velocity.

The rotor is a hollow cylinder and has magnetic bearings to minimize friction. The rotor is located in a vacuum pipe to decrease its friction even more. The rotor is integrated into a motor/generator machine that allows the energy flow in both directions.

There are two topologies, slow flywheels (with angular velocity below 6,000 rpm) based on steel rotors, and fast flywheels (below 60,000 rpm) that use advanced material rotors (carbon fiber or glass fiber). FESS presents an efficiency of 80-85 %, with a useful life of 20 years.

The trend of FESS applied to the renewable energies is to combine them with other technologies, like micro CAES or thermal energy storage systems [11].

2.5 Batteries

These systems could be located in any place and be rapidly installed. Large systems (known as Battery Energy Storage System, BESS) don't have the environment impact of other ESS technologies and can be located in a building (or similar) near the point of demand

BESS uses a PCM to convert the battery DC energy into AC grid-compatible energy. These units present fast dynamics with response times near 20 milliseconds and efficiency from 60% to 80% [9].

The energy is stored as electro-chemical energy. The battery temperature change during charge and discharge cycles must be controlled because it affects its life expectancy.

Large scale BESSs that exist nowadays are the 10 MW (40 MWh) systems installed in China and California, and the 20 MW (5 MWh) system installed in Puerto Rico [9].

New battery technologies are being developed for a higher energy store capacity and at a lower cost than the Lead Acid battery. Some of these new technologies are Lithium Ion, Regenesys® Redox, Nickel Metal Hydride, Hydrogen Vanadium Redox, Nickel Cadmium and Zinc Bromide [12].

2.6 Supercapacitors (ultracapacitors)

The energy stored in supercapacitor Energy Storage System (SESS) will depend on the voltage at the ends, such as

$$E = \frac{1}{2} C V^2 \tag{3}$$

where V is the supercapacitor voltage.

The specific capacitance of such a double-layer is given by

$$C = \varepsilon_0 \varepsilon_r \frac{A}{D} \tag{4}$$

where C is the capacitance, ε_0 the dielectric constant of free space, ε_r the dielectric constant of the medium between the two layers, A the surface area, and D is the distance between the two layers (the distance from the electrode surface to the center of the ion layer). This approximation is roughly correct for concentrated electrolytic solutions.

The most relevant properties of the SC, compared to conventional capacitors, are its high capacity values (approximately thousands of Farads), greater energy density (10 Wh/kg), and power (50 kW/kg), a high efficiency (above 95 %) and low maintenance cost and longer life [13]-[19].

In this paper considers that the ESS is built from SC. The SC is an emerging technology that is beginning to be applied for the implementation of ESS for PVGS. These devices can be implanted easily in existing systems of power injection because their behavior is similar to a conventional capacitor.

SESS voltage must be limited to a maximum value, V_{max}, so also there is a limit to the maximum amount of energy, W_{max}, which can be stored in the SC.

Similarly it is desirable to limit the minimum voltage of the SESS, V_{min}, to ensure that the converter responsible for the SESS control works in a proper operating range. Defining an index of change in voltage, Δ, as the ratio between V_{min} and V_{max}, expressed as a percentage, it is possible to obtain the energy available (when the SESS is charged) as:

$$W_{SESS} = \frac{N}{2} C V_{max}^2 \left(1 - \left(\frac{\Delta}{100}\right)^2\right), \tag{5}$$

where N is the number of SC modules in series that the SESS contains. From the above equation it is possible to deduce the number of SC that are needed to build the SESS.

3 Energy storage capacity

As mentioned above, the idea is to design a system that transforms renewable energy in quasi-manageable, and for this purpose a SESS has been designed, assuming that the set PVGS-SESS behaves as a conventional power source delivering the power which is demanded.

The design of the SESS done assumes that the set PVGS-SESS must behaves as a constant power source for pre-established time intervals. For this analysis is considered a PVGS with nominal peak power equal to 100 kWp. The result can be easily extrapolated to other PVGS powers. As it is well known the power generated by a PVGS in a regular weather conditions depend on the time of day as shown in Fig 3.

When determining the interval of constant injected power into the grid, it has been considered the symmetry of the generated power for optimizing the variations of storage energy.

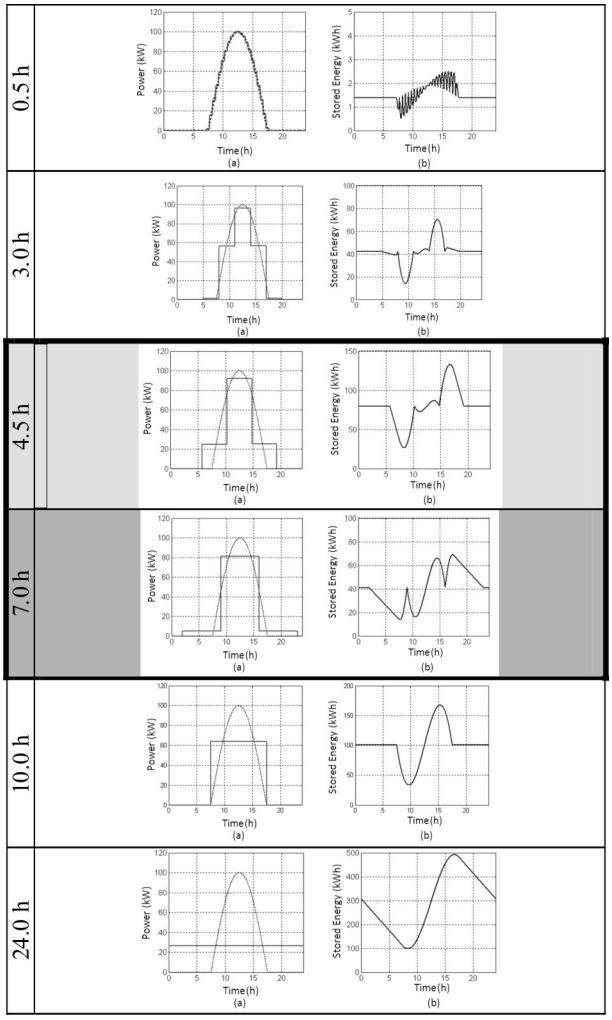


Figure 3: Power and energy for different constant injected power interval lengths: a) Generated and injected power; b) energy stored in the SESS.

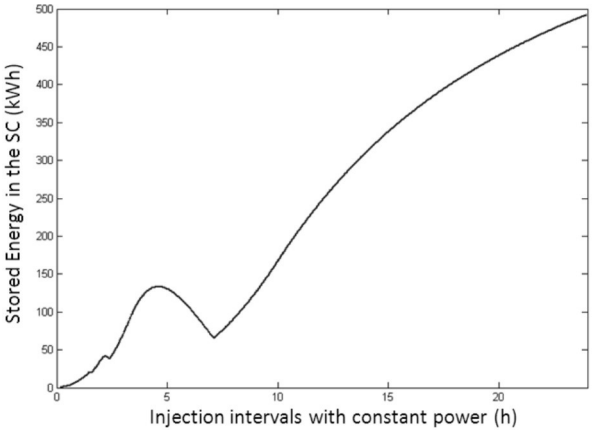


Figure 4: SESS Capacity versus the length of constant injected power intervals.

Also, it has been taken into account that the minimum storage energy must be at least 20% of the maximum energy for guarantying a minimum voltage that allows the control electronics to operate correctly, as the DC / DC converter present buck/boost margin.

The variation of the SESS storage capacity when varying the length of the constant injected power interval is shown in Fig. 4. It is highlighted that for an interval length of 3 and 7 hours is needed the same storage capacity, being better the 7 hours interval that ensures constant injected power during more time. It is also highlighted that the constant injected power interval length equal to 4,5 hours produces a relative maximum being worse that the 7 hours option.

4 Description of the proposed system

The proposed scheme for the PVGS connected to the grid, is shown in Fig. 5. The inverter used is of high switching frequency (10-20 kHz). The SESS control is performed using a bidirectional DC/DC converter.

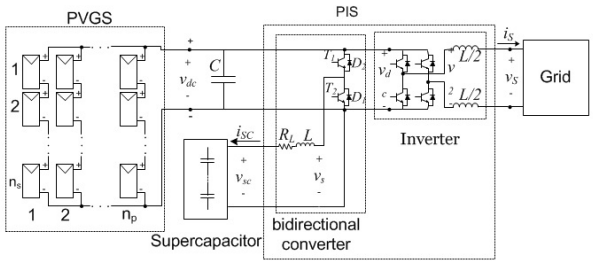


Figure 5: Proposed system scheme.

The main objective of the proposed system is to inject a constant power into the grid following a reference value, charging or discharging the SESS depending on the power generated by the PVGS being higher or lower than the reference power. The control electronic system is conformed by two converters: the inverter and a bidirectional DC-DC converter.

4.1 Inverter

The inverter's purpose is to inject the energy generated by the PVGS into the grid, producing sinusoidal currents in phase with the voltages. To control the active power that is injected, it is sufficient, if the voltage is perfectly sinusoidal, to control the fundamental component of the stress of the inverter. The MPPT routines are also developed by the inverter.

As mentioned, the inverter controls the current injected into the grid using a synchronous hysteresis band [1], [18] with a switching frequency of 20 kHz. The inverter must build the power supply with the desired quality.

4.2 BiDDC: Bidirectional DC/DC converter

To control the SESS a BiDDC has been chosen, which allows a correct operation of the system opposite the changes in SC terminals due to variations in the energy stored in them, also allowing bidirectional power flow and hence the charging and discharging of the SESS.

The converter has three operating modes: a first charging mode, in which the energy flow is from the PVGS towards the SESS (which will occur when the power generated by the PVGS is greater than the reference operation point or when the SESS voltage is less than the start-up voltage); a second mode, of discharge, where the energy will flow from the SESS to the grid (via the inverter, which will occur when the power generated by the PVGS is less than the power reference operation point); and a third mode, stand-by, where there is no flow of energy (which occurs when the power generated by the PVGS is lower than the set point and the voltage of the SESS in lower than the one of start-up).

4.2.1 Charge mode

In this mode of operation, the energy goes from the PVGS (through the DC bus) towards the SESS, making the control through the switching of T_2.

By closing the switch T_2 the current passes through the L_{SC} towards the SC (Fig. 6a). In that time interval, some energy is dissipated in R_L, some accumulates in L_{SC} (increasing the current), and the rest, the largest amount, is stored in the SESS. The free movement diode D_1 conducts when the switch T_2 is closed and the current goes out from the SC (Fig. 6c).

In the steady state, considering that there are no losses, the increase in i_L during closing of the switch must be equal to the decrease when the switch is opened. The input power must be the same as the converter output power. Because of this, we find that the work cycle of the switch T_2 satisfies the following relation:

$$D_2 = \frac{T_{on,T_2}}{T} = \frac{V_{SC}}{V_{dc}} = \frac{I_{dc}}{I_{SC}}. \tag{6}$$

This index represents the percentage of time T_2 remains closed during each switching cycle.

In this mode of operation, the converter behaves like a DC transformer (transformation ratio, a = D_2) and to make it work we must have $D_2 \geq V_{SC} / V_{dc}$.

The ripple of the SESS current is calculated from the positive slope that occurs when the switch T_2 is closed, neglecting the resistance of the coil R_L:

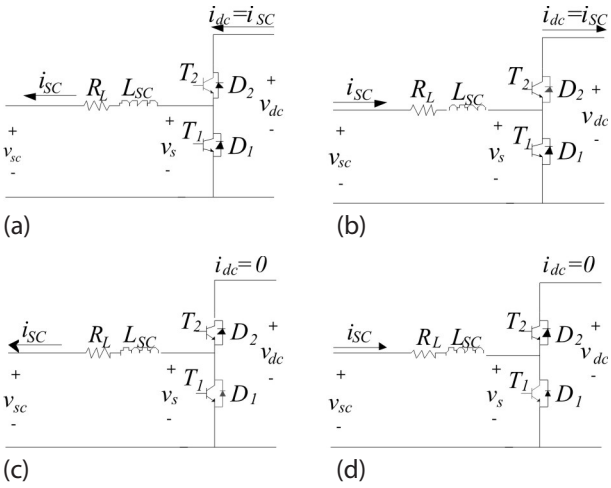


Figure 6: BiDDC Operation modes: a) Charge mode with power flow; b) Discharge mode with power flow; c) Charge mode without power flow d) Discharge mode without power flow

$$\Delta i = \frac{V_{dc}}{L_{SC} f} D_2 \left(1 - D_2\right), \tag{7}$$

where f is the switching frequency. A small ripple is desirable, and the maximum ripple occurs for $D_2 = 0.5$. and when the voltage $V_{SC} < V_{dc} / 2$. The design variables to control this ripple are the switching frequency, f, and inductance value, L_{SC}.

To control the transfer of energy, the flow of the SESS is controlled with a synchronous hysteresis band controller, which controls the voltage applied to the coil terminal.

If the applied voltage is lower than V_{SC}, there will be no current flow because it cannot pass through the diode D_1 (reverse direction), or through T_1 (switched off). If the modulated voltage is greater than V_{SC}, the current averaged over one switching period depends on the resistance R_L. The following expression sets the value

$$\overline{I_L} = \frac{V_{dc} D_2 - V_{SC}}{R_L}. \tag{8}$$

From this equation we deduce that for the existence of an energy transfer to V_{SC}, we need a modulation index D_2 greater than V_{SC} / V_{dc}.

4.2.2 Discharge mode

In this mode of operation, the energy goes from the SESS to the grid (through the DC bus and the inverter). In this mode the control is performed by the switching of T_1.

This mode of operation increases the current in the coil L_{SC} when the switch T_1 is closed (Fig. 6d). if the current goes in the opposite way (Fig. 6b) the current through L_{SC} decreases and passes through the diode D_2 towards the DC bus.

As the previous operation mode, the current flow through the SESS is controlled through the voltage applied in the coil L_{SC} terminal.

The current i_L increment when the switch is closed must be equal to its decrement when the switch is opened. And considering that there are no losses, the input power must be the same as the converter output. We reach the transformation ratio:

$$\frac{1}{1-D_1}=\frac{V_{dc}}{V_{SC}}=\frac{I_{SC}}{I_{dc}}. \tag{9}$$

Modulation index D_1 represents the percentage of time T_1 remains closed during each switching cycle.

In this mode of operation, the converter behaves like a DC transformer (with a transformation ratio of a = 1/(1-D_1)) and works as long as (1-D_1) ≥ V_{SC}/ V_{dc}.

Operating the same way as in the previous case, we can calculate the value of current in the DC bus

$$\overline{I_L}=\left(\frac{V_{SC}}{1-D_1}-V_{dc}\right)\Big/\left(\frac{R_L}{(1-D_1)^2}\right). \tag{10}$$

Actually, T_1 is triggered in a complementary way with respect to T_2, so it is possible to define one duty cycle $D=D_2=1-D_1$.

5 Control system

The control can be divided into blocks which are shown in the diagram represented in Fig. 7.

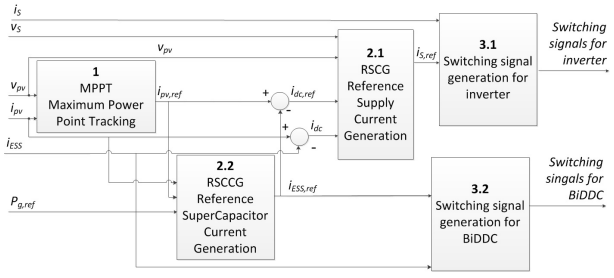


Figure 7: PVGS system control squeme.

The Maximum Power Point Tracking, Reference Supply Current Generation and Generation of switching signals to inverters blocks are implemented as described in [20].

This block generates the inverter switching signals using a synchronous hysteresis band that compares with zero, in each sampling period, the error existing between the reference supply current and the measured supply current [20].

The switching signals of the DC/DC bidirectional converter are generated by a synchronous hysteresis band that compares with zero, in each sampling period, the error existing between the reference current of the SESS and the measured current of the SESS.

The SESS reference current is obtained as the current that we would have to inject into the SESS to cancel the difference existing between the reference power that has to be injected into the grid and the actual power generated by the PVGS.

6 Simulation Results

The simulations are done in two steps. Firstly, the energy storage system based on supercapacitors is analyzed in electrical terms by maintaining a constant irradiance. Secondly, the behavior of the system is exposed when there are irradiance fluctuations.

Fig. 8 shows the scheme of the simulated system, which simulates a PIS, capable of establishing and maintaining the PVGS in its MPP and injecting the value of the power established. The PVGS model used in the simulation offers the properties exposed in [21]-[22]. The main features of PVGS and PIS are shown on Tables II and III. The power converter model was developed by using switching states. The simulated PVGS has 16 photovoltaic cells connected in series (Shell SP-150-P), which maximum power point voltage is 544 V for nominal conditions of irradiance of 1000W/m^2 and temperature of 25ºC.

Table 2: PVGS Characteristics

Parameter	Value
Number of series-parallel connected cells	16-1
Photovoltaic cell reference	SHELL SP150-P
Short-circuit current (25ºC, 1000W/m2)	4.8 A
Open-circuit voltage (25ºC, 1000W/m2)	43.4 V
MPP current (25ºC, 1000W/m2)	4.4 A
MPP voltage (25ºC, 1000W/m2)	34 V

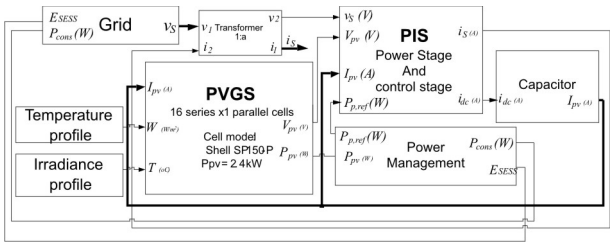


Figure 8: Simulated System scheme.

Table 3: PIS parameters for simulations

Parameter	Valor	Parameter	Valor
Inductance L	2x50 mH	Capacitor C	64.36 µF*2
Inductance L_C	100 mH	Inductor resistance R_L	0.01 Ω
Switching frequency			20 kHz

Through the analysis of power reference profile shown in Fig. 9, the evolution of the power of a stand-alone SESS is observed (Fig.º10). SESS consists of 6 modules in series with a capacity of 1.65 F, 100 times less capacity than the commercial module of reference BMOD165P048 from Maxwell Technologies, to reduce the duration of the simulations. The control of the system avoids that the SESS is completely uncharged, turning off by its-self when the SESS voltage catches a minimum value. In Fig. 10 one can check the stand-alone SESS control dynamic performance. As the power is directly proportional to the voltage and the flow, for the power to be constant, when the voltage in SESS rises, the flow has to go down and vice versa. In other words, as we can appreciate in Fig 10 and 11, when the SESS is loaded the system requires less flow to maintain the same power.

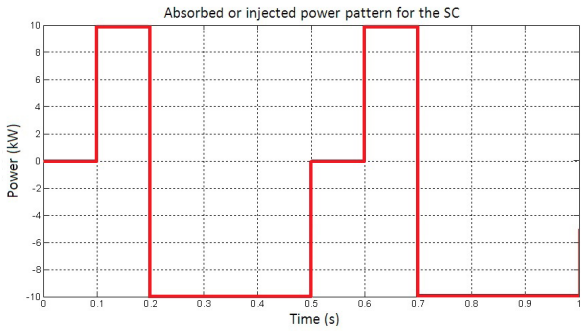


Figure 9: SESS power pattern.

Finally, a simulation of the complete system shown in Fig. 8 is carried out for the irradiance profile shown in Fig. 12. This irradiance profile has been selected to evaluate the behavior of the entire system (including the SESS) when varying conditions occur. In Fig. 13 we observe that the system fulfills the specifications of

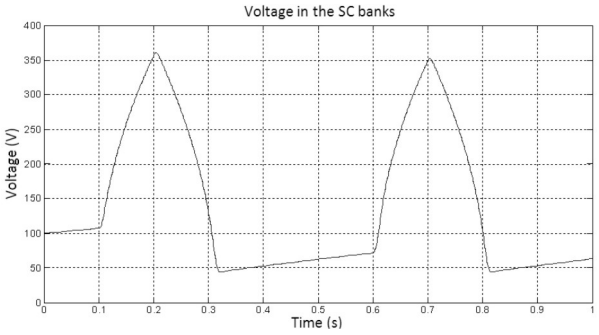


Figure 10: SESS voltage.

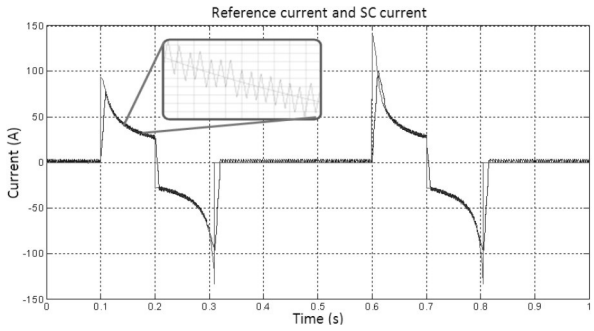


Figure 11: Reference current and SESS current.

not injecting power in the grid until the SESS obtains a minimum voltage. Once it has obtained this voltage the SESS is capable of absorbing and injecting energy and controlling the power injected in the grid. At this point, the system begins to inject the constant power (or set point) even though there are variations in the irradiance.

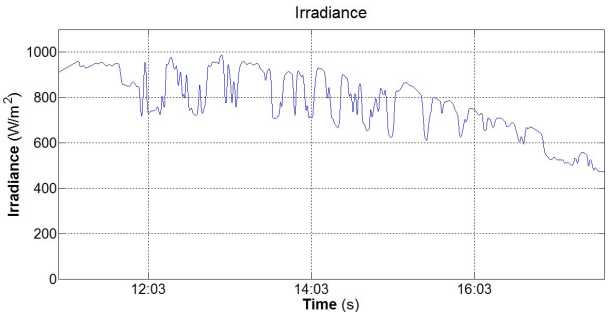


Figure 12: Irradiance profile for simulation test.

Fig. 14 and 15 show respectively the flow and the voltage of the SESS. Fig. 16 shows a detail of the flow injected in the grid by the inverter that is in phase with the voltage. As it can be seen, the system maintains the power reference despite of the irradiance changes.

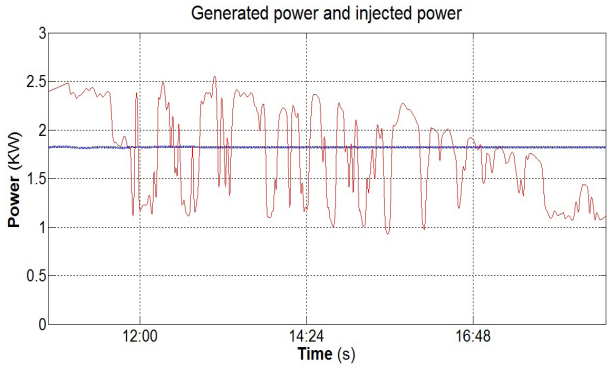


Figure 13: PVGS generated power and power injected to the grid.

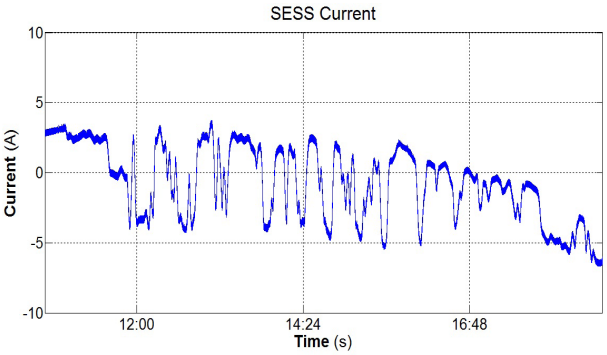


Figure 14: SESS current.

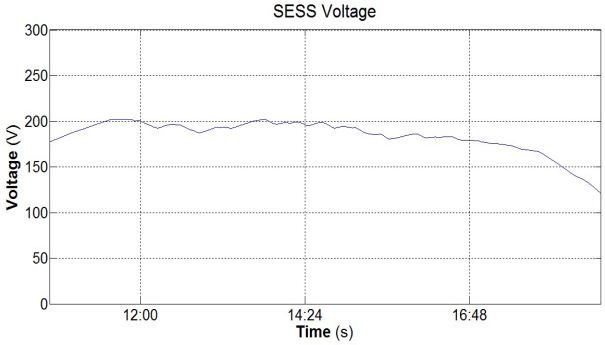


Figure 15: SESS voltage.

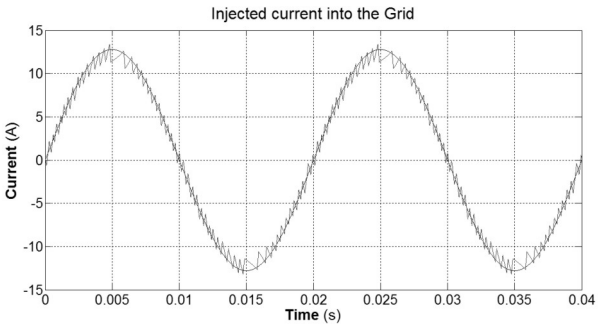


Figure 16:. Current injected to the grid.

7 Experimental results

The PVGS-SESS prototype has been tested experimentally, Fig 17, to verify its correct functioning. This prototype is composed of an electronic converter SEMITRANS Stack with four SKM50GB123D SEMIKRON branches, three for the VSI and one for the DC / DC converter, four SKHI 22 drivers and a Maxwell Technologies supercapacitor BMOD0165 P048 B01. To model the photovoltaic plant a solar array simulator HP E4351B has been used.

The control platform used is a control board NI sbRIO9632 FPGA/Processor with the Development software LabVIEW 2011 SP1. The measurements were made with Voltage transducers LV 55-P and Current transducers LA 55P/SP1.

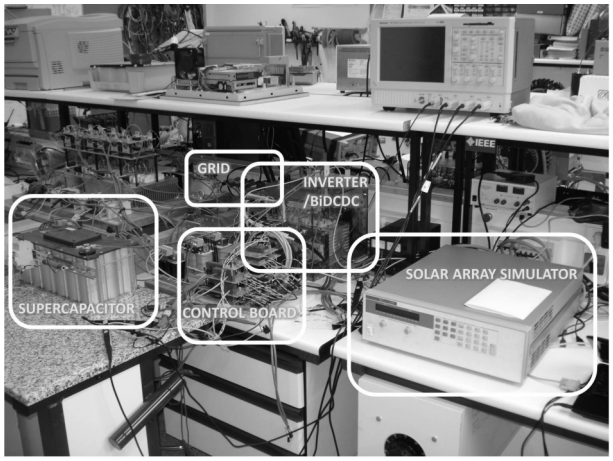


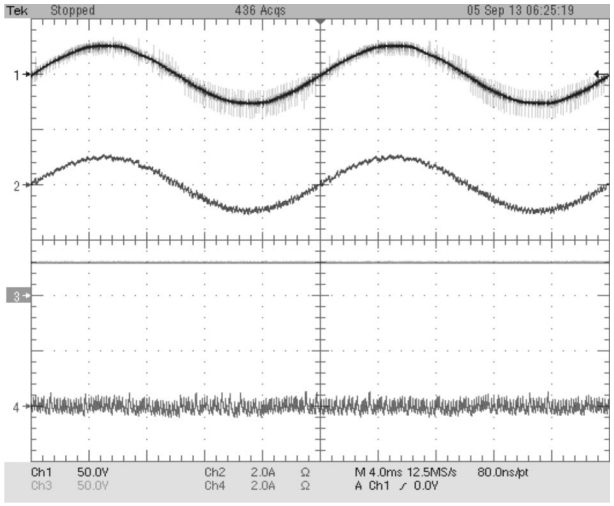
Figure 17: Experimental prototype.

is 20 kHz. The PLL is implemented here in order to maintain the synchronization with the grid despite of voltage distortions or grid events. And the PI controller is also implemented in the FPGA together with the SC and grid current references with the purpose of providing a fast response.

The processor is taken for the slower tasks, such as MPPT, and the high computational cost tasks, such as power calculations. It is synchronized with the FPGA with the Scan Engine feature at 10 ms and the sample rate of the loop is 200 ms.

Some experimental tests have been carried out to validate the control system and the prototype performance. Fig 18 shows the waveforms when the system is working in the steady state during the process of loading and unloading the SESS.

Fig 19 (a) shows the transient state of the PVGS-SESS system when it operates without the SESS. In this case



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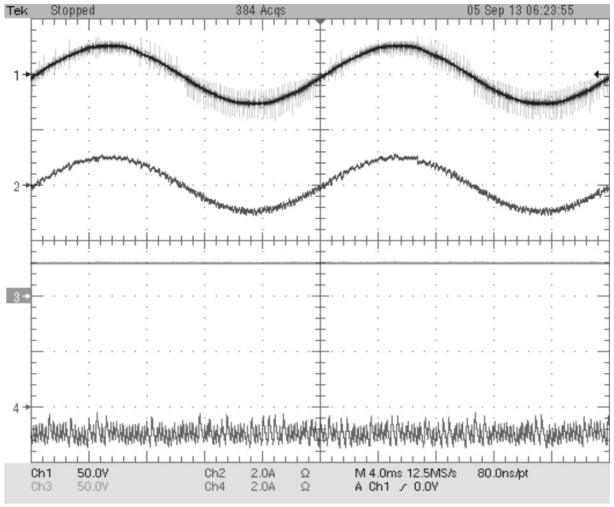

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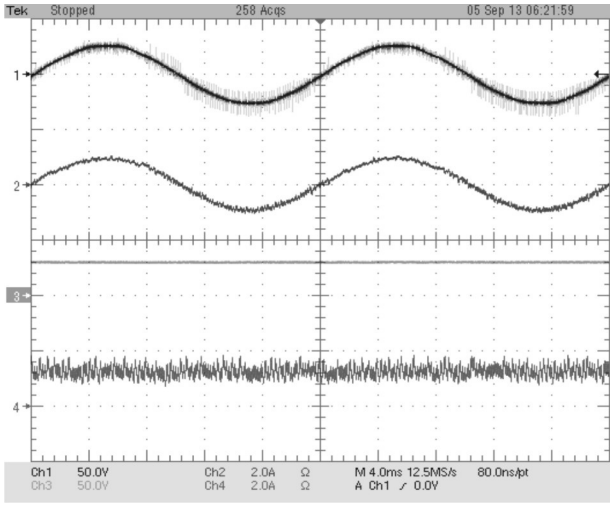
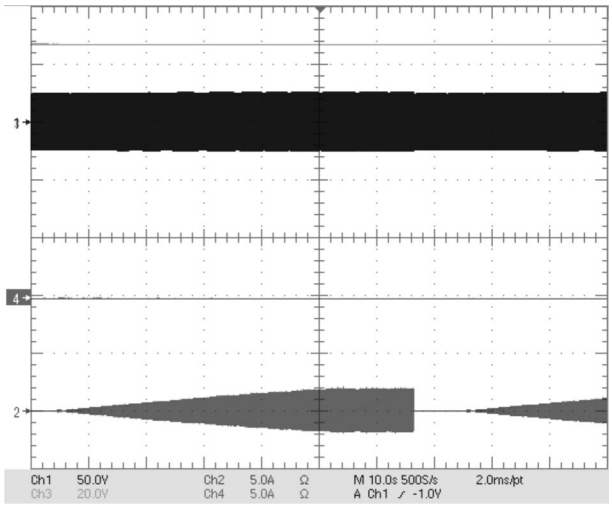


c.

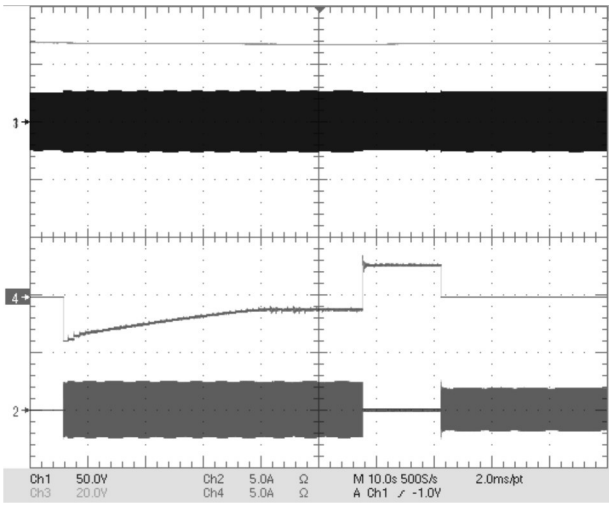
Figure 18: Steady state experimental waveforms: (a) Injecting the same power than the PV panels, (b) Injecting less power than the PV panels, and (c) Injecting more power than the PV panels energy.

the aim is to inject the maximum power available from the PV system. To obtain this, the current is injected in phase with the voltage, so that voltage and current of the same phase are synchronized. In Fig. 19 (a) one can see how the injected power reaches the MPP and stabilizes with active power control disabled. The test also adds a disconnection and the start procedure again.

However, when you activate the SESS, the active power injected is the one demanded by the grid manager. Following the same pattern, when the SESS is enabled, Fig 19(b) shows how the power injected into the grid matches the reference. This is because the DC / DC converter is the one that injects the energy required until the MPP is achieved. It is easy to see how the active power injection instantly becomes the reference thanks to the SESS, so the MPPT setup procedure does not matter.

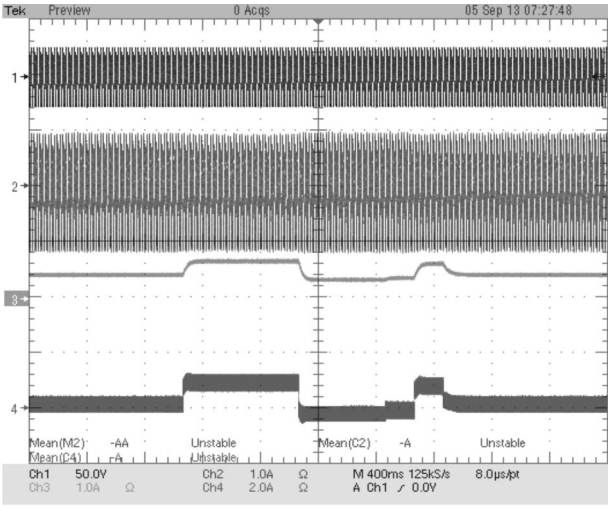


a.

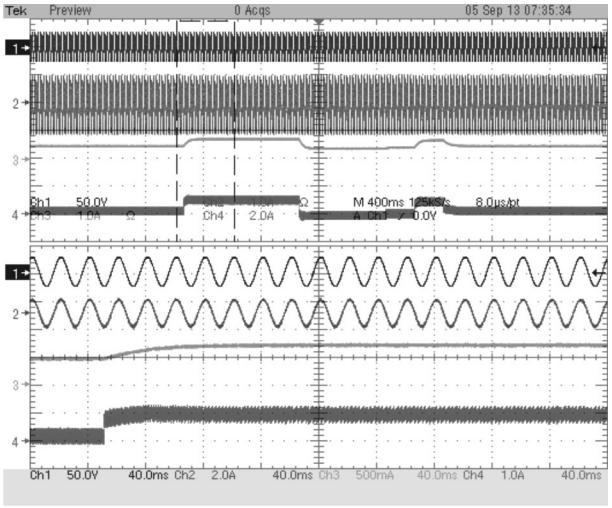


b.

Figure 19: Transient state experimental waveforms: (a) Injecting without active power control, (b) Injecting with different active power references.



a.



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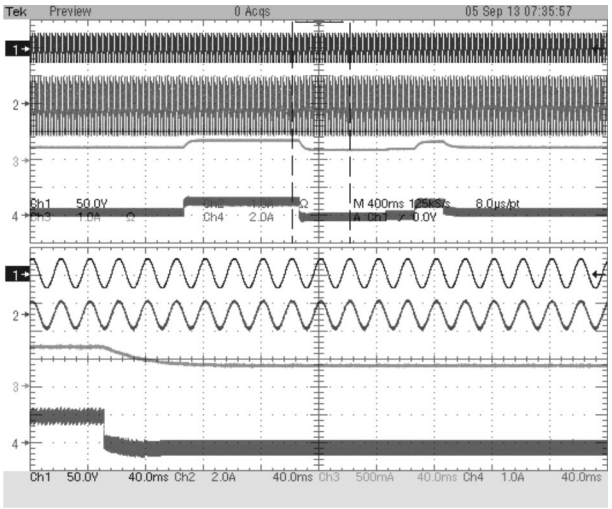

c.

Figure 20: Transient state experimental waveforms: (a) Injecting with different value of active power generation, (b) and (c) Details of the dynamics of the system.

Figure 20 shows the evolution of the PVGS-SESS system when the irradiance changes. The irradiance profiles are introduced by interfacing the solar array simulator. As it can be seen in Fig 20 (a), these changes of irradiance cause fluctuations in the power generated by the PV that also are observed in PV current, and the PVGS-SESS system reacts storing or supplying energy in the SC.

In Fig 20 (b) and Fig 20 (c) the dynamic response of the system can be seen. In this situation, the system, due to an excess or a shortage of energy generated, reacts and is able to inject the set reference power. This is because of the DC / DC converter injects the energy required until the reference power is obtained. As mentioned above, the active power injection instantly becomes the reference thanks to the SESS.

8 Conclusion

In this paper a new topology for the power injection system used in photovoltaic generation systems is presented. This topology is based on two converters, a voltage source inverter that injects the power into the grid and a bidirectional direct current converter that regulates the charge of the SC. The performance of the proposed system was tested by simulation and by a laboratory prototype. The proposed system dampens the fluctuations and maintains the reference power injected into the grid by the PVGS during the time set by the grid manager, showing the benefits of using a SESS in an injection system connected to the grid for photovoltaic generators. On the one hand, the MPPT transients do not affect to the desired injected power, and on the other hand, the irradiance changes maintain the injected power reference. Its operation is based on the traditional energy generation, making renewable energy generation "quasi-manageable".

It is easy to incorporate a SESS into the existing inverter topologies, being able to maintain constant the power injected into the grid, having a good steady and transient state performance. The time interval which ensures the power injected determines the size or capacity of the SESS. It is important to note how higher intervals need the same capacity than smaller ones, due to the symmetry over the time of the day of the generated power, but longer intervals guarantee a better integration into the distribution grid management. Finally, we showed how the PVGS can be improved, in order to ensure maximum energy extraction and guarantee that the set reference power is delivered.

9 Acknowledgement

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On Self-Avoiding Walks across n-Dimensional Dice and Combinatorial Optimization: An Introduction

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Abstract: Self-avoiding walks (SAWs) were introduced in chemistry to model the reallife behavior of chain-like entities such as solvents and polymers, whose physical volume prohibits multiple occupation of the same spatial point. In mathematics, a SAW lives in the n-dimensional lattice Z^n which consists of the points in R^n whose components are integers.

In this paper, SAWs are a metaphor for walks across faces of n-dimensional dice, or more formally, a hyperhedron family $\mathbf{H}(\Theta, b, n)$. Each face is assigned a label $\{\underline{\varsigma} : \Theta(\underline{\varsigma})\}$; $\underline{\varsigma}$ represents a unique n-dimensional coordinate string, $\Theta(\underline{\varsigma})$ is the value of the function Θ for $\underline{\varsigma}$. The walk searches $\Theta(\underline{\varsigma})$ for optima by following five simple rules: (1) select a random coordinate and mark it as the 'initial pivot'; (2) probe all unmarked adjacent coordinates, then select and mark the coordinate with the 'best value' as the new pivot; (3) continue the walk until either the 'best value' <= 'target value' or the walk is being blocked by adjacent coordinates that are already pivots; (4) if the walk is trapped, restart the walk from a randomly selected 'new initial pivot'; (5) if needed, manage the memory overflow with a streaming-like buffer of appropriate size. Hard instances from a number of problem domains, including the 2D protein folding problem, with up to $(2^{25}) * (3^{24})$ coordinates, have been solved with SAWs in less than 1,000,000 steps – while also exceeding the quality of best known solutions to date.

Keywords: combinatorial optimization, algorithms, self-avoiding walks

Kombinatorična optimizacija in sprehodi brez ciklov v n-dimenzionalni kocki

Izvleček: Sprehodi brez ciklov (Self-avoiding walks, SAWs) so bili uvedeni v kemiji kot realistični model obnašanja dolgih verig, kot so topila in polimeri. V matematiki sprehodi brez ciklov obstojajo v n-dimensionalni rešetki Z^n, ki vsebuje točke v R^n katerih elementi so cela števila.

V tem članku predstavimo sprehode brez ciklov kot metaforo za sprehode preko ploskev n-dimenzionalne kocke, formalno v hyperhedron družini $\mathbf{H}(\Theta, b, n)$. Ploskev predstavimo kot par $\{\underline{\varsigma} : \Theta(\underline{\varsigma})\}$, kjer $\underline{\varsigma}$ predstavlja unikatno n-dimenzionalno koordinato in $\Theta(\underline{\varsigma})$ predstavlja vrednost funkcije Θ za $\underline{\varsigma}$. S sprehodom iščemo optimalne vrednosti funkcije $\Theta(\underline{\varsigma})$, pri tem pa uporabimo pet enostavnih pravil: (1) izberi naključno koordinato in jo označi kot 'prvi pivot'; (2) obišči vse še ne obiskane sosedne koordinate, nato koordinata z 'najboljšo vrednostjo' postane novi pivot; (3) nadaljuj sprehod, dokler 'najboljša vrednost' ne doseže oz. preseže 'ciljne vrednosti' ali dokler sprehod ne postane blokiran od sosednjih koordinat, ki so že 'pivoti'; (4) če je sprehod blokiran, začni novi sprehod z naključno izbranim 'novim prvim pivotom'; (5) če je meja pomnilnika presežena, vključi ustrezno velik medpomnilnik podatkovnega toka.

Zahtevni problemi iz različnih področij, vključno 2D zvijanje proteinov s številom koordinat kot n.pr. $(2^{25}) * (3^{24})$, se uspešno rešujejo s sprehodi, ki se končajo z manj kot 1.000.000 koraki – dobljene rešitve pa presegajo kvaliteto do sedaj znanih najboljših rešitev.

Ključne besede: kombinatorična optimizacija, algoritmi, sprehodi brez ciklov

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1 Introduction

Instances of combinatorial problems arise in many contexts such as operations research, computer-aided design, machine learning, robotics, data mining, bio-informatics, etc. An exhaustive search for an optimum solution is not possible for most instances of practical size due to the huge number of feasible solutions. The question arises about the choice of heuristic algorithms to be deployed by the solver. To date, stochastic search methods offer the best compromise, including Metropolis-Hastings algorithm [1, 2], simulated annealing [3, 4], Gibbs sampling [5], tabu search [6, 7], and many others. New heuristics are emerging on Wikipedia and in journals under metaphors such as ant colonies, bird flocks, natural disasters, biological processes, etc.

Our approach is simple; we only take a few liberties with rigorous mathematical notation. When we refer to a *function f* (x^i_1, x^i_2, . . . x^i_n), we imply an *objective function*, which in general is a *multivalued function*, returning a *value* for a specific *coordinate* (x^i_1, x^i_2, . . . x^i_n). The *support set* of the function is defined in terms of such coordinates. A combinatorial problem is defined by its function *and* its *coordinate type*. Coordinates are represented as a set of strings, such as 01011... for a binary coordinate, 210210... for a ternary coordinate, 4, 2, 5, 3, ... for a permutation coordinate, etc. A combinatorial problem can also be stated in terms of *concatenated* coordinates of different types. For example, we define the 2D protein folding problem *on a square lattice* by computing its function values with coordinates represented as *a concatenation of binary and ternary coordinates*.

We define a *walk* as a sequence of steps that chain a set of *pivot coordinates, adjacent coordinates* as the *local neighborhood* of the pivot coordinate, and *probing* as evaluating the function for values in this neighborhood. A *feasible solution* of the combinatorial problem is a pair (*coordinatePivot:valuePivot*). Once we capture the description of the combinatorial problem in these terms, the search procedure is as simple and as generic as the five rules outlined in the abstract – for *any* combinatorial problem. For more about this notation and examples of various problem instances, see [8].

We have a number of on-going projects with the goal to prototype SAWs as a powerful generalpurpose search procedure that, unlike alternatives, does not require knobs and dials to set-up. These projects include instances of problems defined for Golomb rulers, integer partitioning, maximum independent set, minimum vertex cover and maximum clique, graph linear arrangement, job scheduling, etc. A nearly completed project demonstrates significant improvements in solutions of the notoriously hard *labs problem* [9]: here we compare, side-by-side, the performance of state-of-the-art memetic/tabu and SAW solvers. In the present paper we apply SAW to solve the 2D protein folding problem *on a square lattice* [10]. Since this implementation is based on a scripting language, it is not suitable for solving very large problems. However, the solver does achieve a number of state-of-the art solutions on a significant subset of problem instances from the literature and an asymptotic performance that may well dominate alternative solvers when fully implemented.

The paper is organized as follows. To motivate the approach taken in this paper, Section II starts with a fable about Gretel and Hansel who devise distinctive methods to search for a *pass-key*. Section III formulates the problem and concludes with pseudo code, describing global search with self-avoiding walk. Section IV summarizes a number of performance experiments in 2D protein folding problem defined *on a square lattice*. With some 1000 independent solutions for each member of 10 instance classes of increasing size (with at least 3 instances in each class), these experiments not only replicate the earlier work of others, but also reveal new and improved folding conformations. The paper concludes with directions for future work.

2 Motivation

We introduce a fable to motivate our approach. It involves Gretel and Hansel, living in two adjacent apartments, and a Joker whose omnipresence is never revealed directly. Gretel and Hansel are returning from a party. They discover not only that locks have been changed on both apartment doors with punch-key locks but also that mats that hid the keys were replaced with two urns, each containing a set 36 tickets. Each ticket has a printed label with five digits in the format xx.yy:z; only one label opens Gretel's door, and only one opens Hansel's door. The two sets are identical.

Who gets in first? Watching Gretel, she takes the ticket from the urn and if she does not succeed in opening the door, she puts the ticket into her handbag and retrieves another ticket. Hansel, who had a few drinks at the party, takes the ticket and if he does not succeed in opening the door, returns the ticket to the urn. We say that Gretel is sampling contents of the urn without replacement, while Hansel is sampling with replacement. The probability of Gretel finding the correct ticket on trial k follows uniform distribution, given n tickets: the probability is 1/n, the mean value is (n + 1)/2, and the variance is (n^2 - 1)/12. However, the probability of Hansel finding the correct ticket on trial k follows geo-

metric distribution: the probability is $(1/n)(1 - (1/n))^{k-1}$, the mean value is n, and the variance is $n^2(1 - (1/n))$. The point of the fable so far: we learn that in a search scenarios such as described here, one can improve the chance of first success by dynamically reducing the search space after each trial. In the best case for Gretel, the capacity of her handbag must match the capacity of the urn. If the capacity of the handbag is less than the capacity of the urn, and the handbag gets full before finding the key, she needs to return the unsuccessful ticket to the urn before proceeding with the next trial. In the average case, Gretel's search, even with handbag of limited capacity, always requires fewer trials than Hansel's.

Another surprise awaits after Gretel and Hansel manage to make an entry. Neither has stepped into their apartment's vestibule; instead, each is now standing on a four-sided platform (in their own apartment) and can see, besides the platform on which they are standing, only the surfaces of the four adjacent platforms sloping downwards. Each of them believes that she/he is standing on a face of a huge platonic solid, such as the polyhedron with 36 faces and 72 edges between the faces shown in in Figure 1. Neither realizes that they stepped into a virtual world where not everything is as it seems. The face on which they are standing belongs to a virtual combinatorial object *hyperhedron*, also with 36 faces, but as they will walk from face to face, they will discover that some faces have five adjacent faces, some have even six.

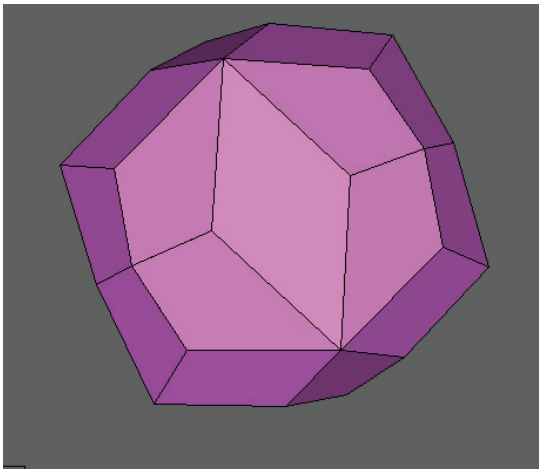
Joker has replaced the two urns with two hyperhedrons and pasted the tickets from each urn into the center of the face in each the hyperhedron, with labels showing. He also hid Gretel's pass-key under one ticket, and Hansel's key under another ticket.

Only Joker has the global view of the hyperhedron. He interprets it as follows. He moves *inside* the hyperhedron, finds the center of the face, and attaches one end of a string to the center and attaches the other string to the center of the adjacent face. He repeats the process for all faces and thus creates a graph; a graph with 36 face-centered vertices and 84 edges. To represent this graph in the plane, he defines *a distance between the coordinates* assigned to each label and makes a projection of the graph as a layered graph shown in the bottom of Figure 1. This graph is not visible to Gretel and Hansel, however, the graph enables Joker to trace each step they would make during their search. Joker also assigned function values to each coordinate: his choice of values is expected to confound Gretel and Hansel in their search. He gives both one, *and only one*, hint about the pass-key: the ticket most likely hiding the pass-key is the one where *value* on the label is 1 or less than 1. If Gretel find Hansel's key first, the key would not fit and she needs to continue the search – and vice versa for Hansel.

Who will find the pass-key to the apartment first? Each is standing on the face with the label 00.00:2 (at the bottom of Figure 1). From this face, Gretel and Hansel can see only the four adjacent faces: 00.10:9, 01.00:6, 10.00:5, 00.01:2. Their task is to *walk* from face to face until they find the *pass-key* to their old apartment.

Gretel is a computer science major and remembers a lecture about Hamiltonian walks in graphs. She knows that she is standing on one of 36 faces and that if she associates each face with a vertex in a graph and the edges between adjacent faces with edges in this graph, she can *compute and remember* the path that visits each face only once. In the worst case, she will take 35 steps to find the key. The procedure she uses to compute the coordinates for each step in the Hamiltonian walk is not as simple to explain as the procedure used by Hansel and explained next. Suffice it to say that function values associated with each coordinate have no role in determining the Hamiltonian path in the graph.An example of Gretel's walk, as traced by Joker, is shown in 2-a. She takes 5 steps to find Hansel's key and needs to continue for a total of 23 steps before finding her key. The first step, from 00.00:2 to 00.00:6, is a deliberate step in this Hamiltonian walk – a step that Hansel would never have taken from this starting position, for reasons we explain next.

Hansel's major is land surveying and he takes the hint about function values associated with each coordinate very seriously. He devises a few rules before starting the walk: (1) mark the face from where the walk starts with an easy-to-spot token; later on in the paper, we call this face the initial pivot. (2) probe each adjacent face that has not yet been marked and write its value on a list. (3) select the adjacent face with the smallest value, step on this face, call it a current pivot, and mark it with a new token. If there are several faces with the same value, make a random selection. (4) repeat step (2) from the current pivot until reaching the target value. The process of marking the pivots during the walk with tokens makes this walk self-avoiding. Hansel can run into a problem with these rules in two cases: (1) he runs out of tokens and can no longer mark the walk; (2) he steps onto a face where all adjacent faces have been marked already, i.e. the walk is trapped. In either of these cases, Hansel has to collect all tokens and restart the walk from a new face, now selected by a random jump. An example of Hansel's walk, as traced by Joker, is shown in Figure 2-b. While Hansel can find the ticket that hides his pass-key in 3 steps or less from many initial positions, it takes 10 steps to find his key if he starts



http://dmccooey.com/polyhedra/JoinedTruncatedOctahedron.html

Joined Truncated Octahedron	
Vertices:	38 (24[3] + 6[4] + 8[6])
Faces:	36 (24 kites + 12 rhombi)
Edges:	72 (24 short + 48 long)
Symmetry:	Full Octahedral (Oh)

The item on the left is a polyhedron with 36 faces and 72 edges [11]. Each face has 4 adjoining faces. This polyhedron is an approximation of the a virtual combinatorial object, a hyperhedron introduced next. By assigning to each face a unique coordinate as a concatenation of a binary strings ofl ength 2 and a ternary string ofl ength 2, we create a hyperhedron with $2^2 \times 3^2 = 36$ faces, the same as polyhedron. However, this hyperhedron has 84 edges compared to 72 in the polyhedron. We count the edges by creating a Hasse graph [8]: each face is assigned a vertex with a unique label and the edges between vertices represent adjacencies between faces. We find that the number of edges between vertices varies from 4 to 6.

The label always contains a unique coordinate string, and in most cases, the label is extended with a value returned by the function evaluated with the coordinate. The Hasse graph is drawn as an undirectedlayered graph on a grid such as the one below: it has 36 vertices and 84 edges with labels such as 00:00:2, 00.10:9, and 01:21:9; the string following ':' represents the value. We say that vertices 00.00:2 and 00.10:9 are adjacent since the distance between coordinates is 1, while coordinates 00.10:9 and 01:21:9 are not adjacent since the distance is 3.

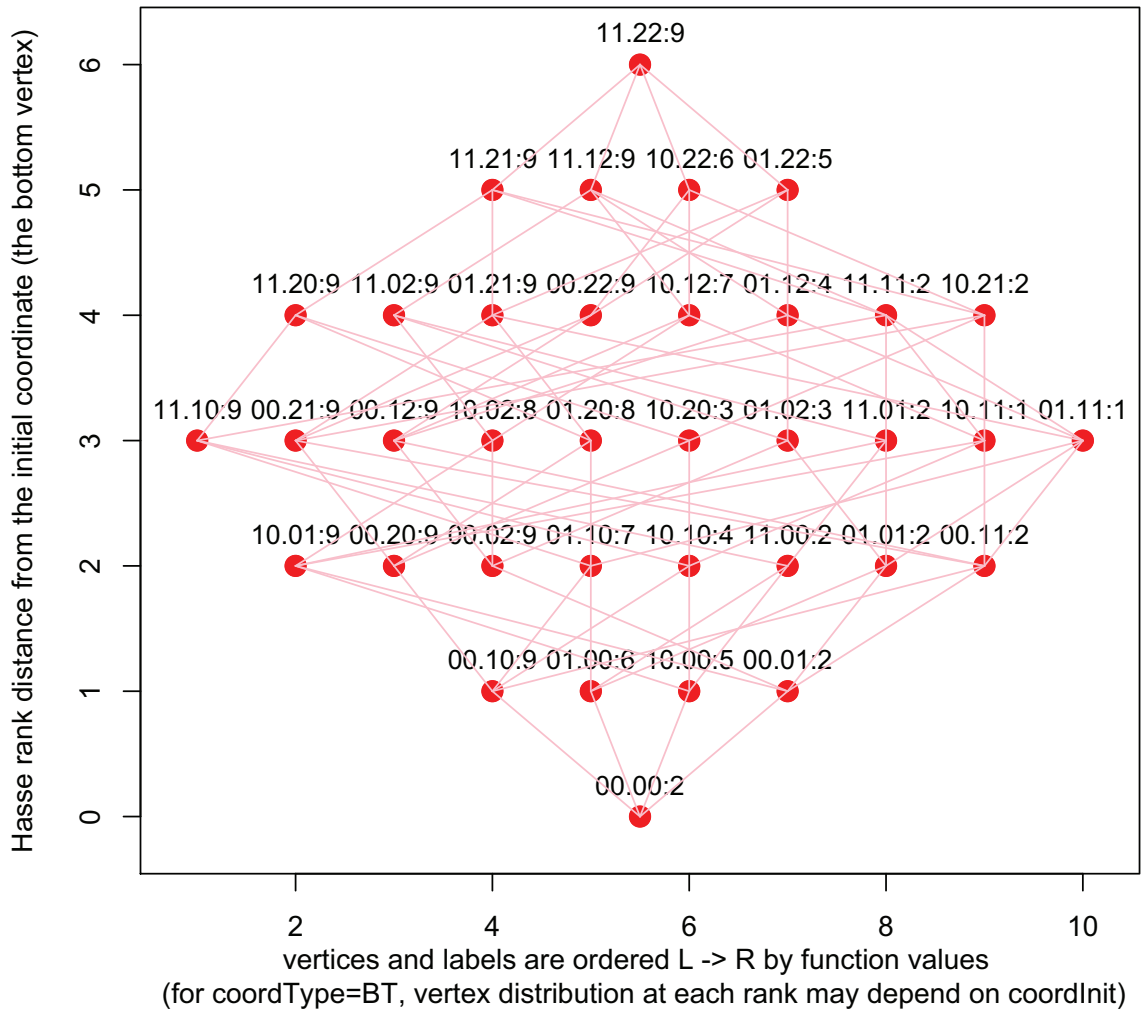


Figure 1: A polyhedron solid and a hyperhedron projection: each has 36 faces, but face-to-face adjacencies are different.

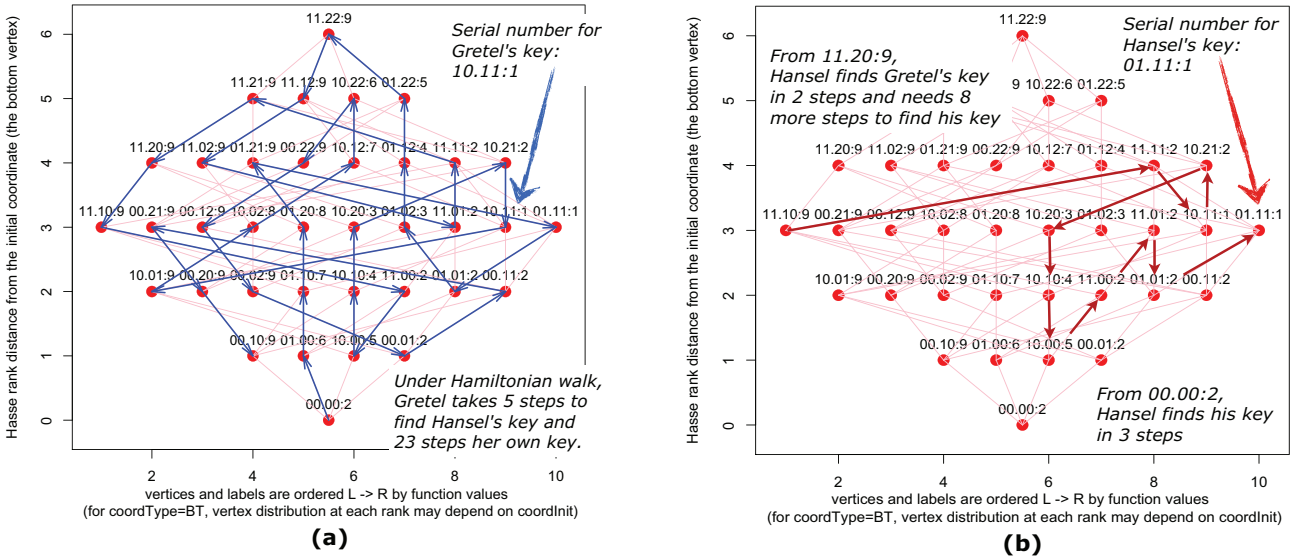


Figure 2: A Hamiltonian walk in the Hasse graph taken by Gretel and a self-avoiding walk taken Hansel. Vertices traversed during the walk are in two categories: (1) only binary coordinate is changing, ternary coordinate is fixed; (2) binary coordinate is fixed, only ternary coordinate is changing. At each pivot, before Hansel decides on the next step, he probes the function values at all adjacent coordinates (that are not yet pivots in the walk) and chooses the coordinate with 'valueBest'. If there are multiple adjacent coordinates with the same 'valueBest', the choice is random. Gretel's walk, self-avoiding by definition, continues until 'valueBest = valueTarget = 1' and the key found fits her lock, Hansel's walk terminates when the key found fits his lock.

from 10.10:9 and takes the third step to 10.21:2 instead of 00.11:2 (both of these choice are equally likely).

What have we learned from the second part of the fable is this: (1) A Hamiltonian walk, while self-avoiding by definition, should not be the first choice under the search scenarios described in this paper. Moreover, the approach would not scale to large problem instances. (2) On the other hand, rules devised by Hansel seem to be highly effective. The good news is that these rules are now enabling effective combinatorial searches not only in the cases of protein folding investigated in this paper but also on hard combinatorial problems in other domains, notably the low autocorrelation binary sequence problem, where the self-avoiding walks solve large problems that could not be solved with state-of-the art memetic/tabu search methods [9]. Moreover, problem of self-avoiding walks getting trapped has not presented itself neither in the case of protein folding nor the case of the labs problem [9].

We used to call these walks Hansel's walks until we learned about polymer and protein chain folding and self-avoiding walks [12]. In our context, the self-avoiding walks are walks in hyperhedra, a virtual world, not in a space of real-world constraints imposed by various lattice formulations in two or three dimensions [13]. In our formulation we deal with real-world folding constraints by way of computing the function values in terms of our coordinate system which foremost defines positions and distances between face-centered vertices in hyperhedra. For problems such as protein folding, some coordinates may induce a penalty value when a conflict is detected during folding; the penalty value assigned may depend on the perceived level of conflict. Hansel's strategy, of always selecting the best available value in the local neighborhood for the next step, keeps the walk going, across faces of a specific hyperhedron, for as long as required.

3 Notation and Definitions

Self-avoiding walks (SAWs) were first introduced by the chemist Paul Flory in order to model the real-life behavior of chain-like entities such as solvents and polymers, whose physical volume prohibits multiple occupation of the same spatial point [12]. In mathematics, a SAW lives in the n-dimensional lattice $\mathbf{Z}^n$ which consists of the points in $\mathbf{R}^n$ whose components are all integers [14].

In Section II, we illustrated a grid of a *finite dimension* that was created by projecting face-centered vertices in a hyperhedron, onto a plane as a Hasse graph. This section illustrates: (1) projections of vertices in Hasse graphs that have 1-to-1 relationship to lattices defined by *unit cells*; (2) example of a SAW-in-a-hyperhedron search for best folding of a protein chain of size *n* on a specific 2D lattice ; (3) formalized definitions of walks

and a generic SAW pseudo-code as a principal component of a global stochastic search solver.

Lattices, unit cells, and graphs. A lattice is a periodic array of points on a grid in space. A unit cell is a subset of |V| points on a grid in a lattice [15]. A self-avoiding walk in a unit cell and a Hamiltonian walk in a Hasse graph with |V| vertices [8] can be considered as two faces of the same coin[1]. We illustrate this premise with the three examples in Figure 3. In Figure 3-a on the left, the primitive cell is a square, forming a unit cell of 9 squares with 16 grid points. On the right, we have a Hasse graph with 16 vertices with binary coordinate labels; this graph is regular since the degree of each vertex is 4 – i.e. each vertex has 4 immediate neighbors. Given the starting point in the unit cell, we can express the walk in terms of directional encoding (North, South, East, West): for the first six steps we would write NWSSSE. Given the starting point in the graph, we express the walk as a sequence of its pivot coordinates (2): 0110, 0111, 0101, 0100, ... etc. However, there is a significant difference in the two data structures: in the unit cell, neighborhood size, depending on the location in the grid, varies from 2, 3, to 4, whereas in the graph, each vertex has 4 neighbors.

The crux in drawing the Hasse graph into its distinct layers is the notion of Hasse rank distance between the vertices with respect to the reference vertex (or the origin vertex) placed at the very bottom of the graph [8]. When coordinates are binary strings, the rank distance is the familiar Hamming distance, for coordinate that represent permutations, the rank distance is the permutation inversion distance, the rank distance between the ternary and quaternary coordinates in Figure 3 is defined as an arithmetic addition of modulo-3 or modulo-4 distances between coordinate components. For example, the distance between 2101 and 0201 is 2+1+0+0=3, the distance between 3210 and 0123 is 3+1+1+3=8, etc. The distance between two coordinates that have been concatenated, shown in the Hasse graph in Figure 1, is an arithmetic addition of distances between the corresponding concatenated segments, for example the distance between 00.10 and 01.21 is (0+1)+(1+1)=3.

Function values assigned to coordinates in Figure 3 are shown for completeness. They represent a special case of index function related to each coordinate. Typically, they exhibit 1, 2, or 4 minima and have been designed for performance testing of combinatorial algorithms [8]. However, these values have no particular significance in Figure 3 .

In Figure 3-b on the left, the primitive cell is a cube, forming a unit cell as a stack of 3 cubes with 16 grid points. On the right, we have a Hasse graph with 16 vertices with quarternary coordinate labels; this graph is not regular since the degree of each vertex varies from 2, 3, to 4. In Figure 3-c on the left, the primitive cell is a cube, forming a unit cell as a large cube that contains 8 primitive cubes with 27 grid points. On the right, we have a Hasse graph with 27 vertices with ternary coordinate labels; this graph is not regular since the degree of each vertex varies from 3, 4, 5, to 6.

In the context of this paper, it is important to also study advances in self-avoiding walks being made in physics and elsewhere, for example on the progression of improvements in the walk lengths of self-avoiding walks on 2-, 3-, and 4-dimensional lattices [16].

Protein folding examples. There are numerous articles that cover many more details about protein folding than we can present here, from very technical [10] to tutorial [17]. Our presentation attempts to be generic and aims to make the problem accessible as a complex puzzle.

Let us take n beads in k colors, arrange them into a linear chain of length n and register the position and the color of each bead, then allow the chain to fold onto a predefined grid in a space of 2 or 3 dimensions. The most popular model is the 2-color HP (hydrophobic and polar, black and white, '1' and '0') model, where any pair of H-type beads that are adjacent on the grid after folding forms a bond. We measure the quality of the folding by counting the number of such bonds in a given arrangement, called a conformation. Once we subtract this number from 0, we call the value energy of the folding and the objective of any folding optimization algorithm is to minimize the value of this energy. In Figure 4 we display a number of chains, each of length 10, where the number of black beads varies from 2 to 10 and the energy from -1 to -4 (the maximum possible). An additional characteristic of the chain is denoted as weight: it is simply the number of black beads in the chain.

On a 2-dimensional square lattice, each step of a SAW has a choice of at most 3 adjacent points of the grid: left, right, and forward, encoded as 0, 1, and 2. With the binary encoding of the colors and the ternary encoding of the self-avoiding walk to control the folding, we encode the coordinate for the folding problem for a chain of black and white beads of length *n* as a concatenation of *n* binary and *n - 1* ternary coordinates, defining a hy-

[1] We are making this point metaphorically: a unit cell is a specific subset of grid points in a lattice [15] and details about crystal structure arrangements and unit cells are a far beyond the scope of this paper.

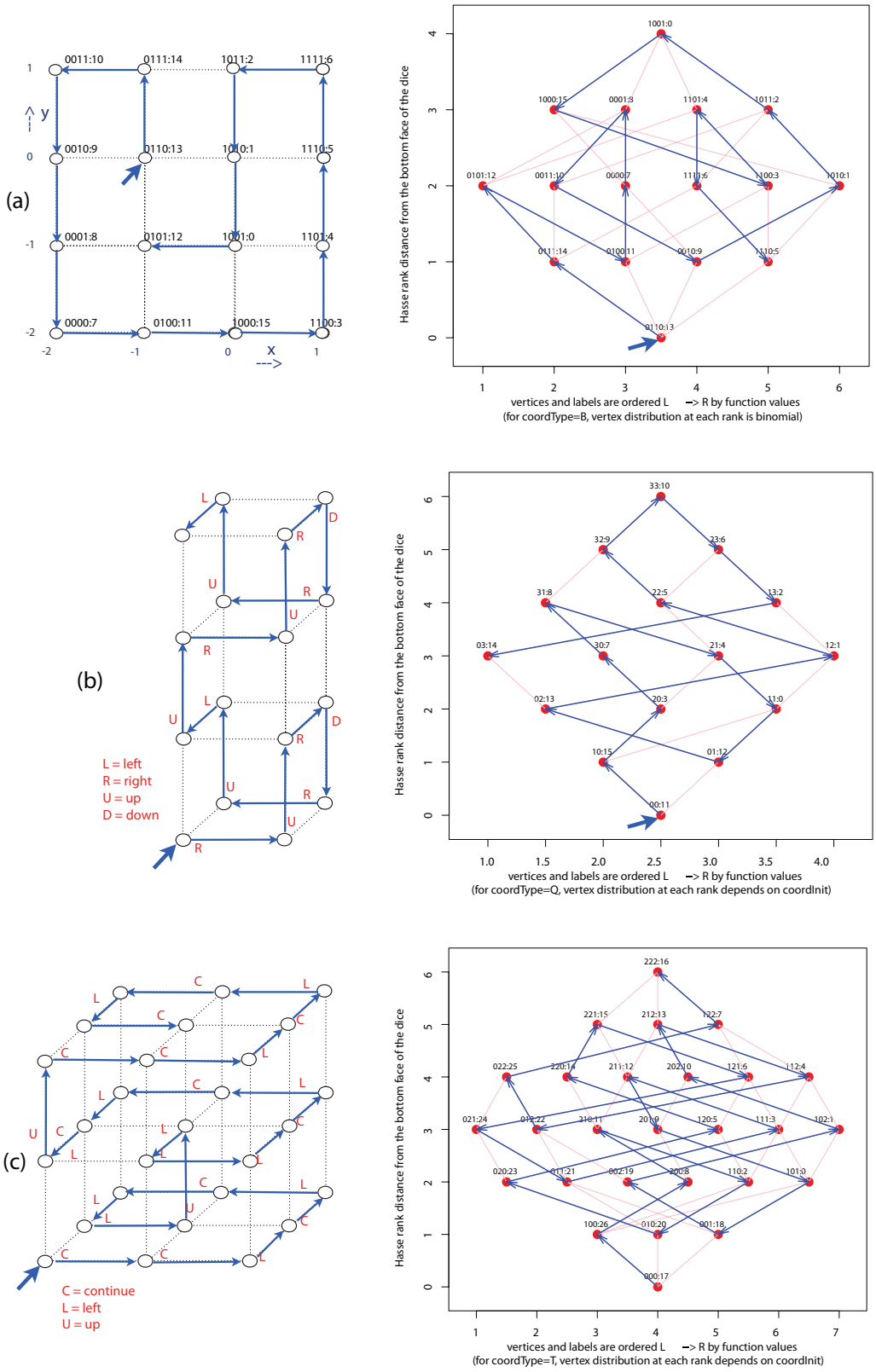


Figure 3: Two sides of the same coin: instances of three self-avoiding walks of lengths $2^4 - 1$, $4^2 - 1$, and $3^3 - 1$ in 2-D and 3-D in **unit cells**, subsets of points on a grid in a lattice [15], versus instances of three Hamiltonian walks of the same length in **Hasse graphs** [8] defined by dimensions 4 (wrt to base 2), 2 (wrt to base 4), and 3 (wrt to base 3). The walks in unit cells are contiguous only with respect to coordinates defined in lattices. Similarly, the walks in Hasse graphs are contiguous only with respect to coordinates defined in Hasse graphs.

perhedron with a total of (2^n) x (3^{n-1}) face-centered vertices. As an alternative, we may also choose a more efficient hexagonal lattice which, when the chain is folded, will produce more bonds (the bees have done it!). In this case, there are 5 adjacent points on the grid; now the string of length *n* is represented as a concatenation of *n* binary and *n - 1* quinary coordinates, defining a hyperhedron with a total of (2^n) x (5^{n-1}) face-centered vertices.

In this paper, we experiment with foldings on a 2-dimensional square lattice. We have grouped our experiments under three plans:

Plan A Stretch a chain of length *n* with weight ω and assign the *k* black beads into fixed positions. Represent this chain as a binary coordinate of length *n* and weight *k*. Search for folding of this chain on a square lattice in 2D that will minimize its energy. Represent the solution as a ternary coordinate of length *n - 1*.

Plan B Fold a chain of length *n* with weight *k* = *n* into a preferred conformation. Typically, the preferred conformation is the one where the energy, with all beads being black, is the global minimum. Two such conformations, with all beads being black and the energy of -4, are shown in Figure 4. Now, represent this conformation as ternary coordinate of length n. Search for a binary coordinate of weight *k* < *n* that either retains the minimum energy under all beads being black or is as close as possible to this value.

Plan C Select the length of the chain *n*, its weight *k*<= *n*, and the target energy value that can be satisfied with at least one feasible folding conformation. Assign a random binary string of length n and weight *k* as the initial binary coordinate. Assign a random ternary ternary string of length *n - 1* as the initial ternary coordinate. Chances are that some initial ternary coordinates do not represent a feasible folding – this is not an issue since in our formulation, the search escapes the unfeasible regions effectively. The search now proceeds by probing simultaneously segments of each concatenated coordinate: the binary segment and the ternary segment before returning a feasible solution with the given weight and the energy target value.

Plan A represents the traditional formulation of the folding problem and many experimental results are reported under this plan. Plan B is also known as the inverse folding problem formulation and experimental results are also reported under this plan. A number of experiments that rely on exhaustive enumeration have similarities with Plan C. However, we are not aware of any publication of experimental results as described under Plan C in this paper; if brought to our attention, we shall report on them in our future publication.

The summary of statistical experiments in Figure 4 reveals a number of interesting properties. All have been performed under Plan C, with 1000 randomly selected initial configurations for each of the six weight and energy input pairs:

- As the tabulated binary weight increases and the energy target value decreases, the number of unique solution decrease from 813 (out of 1000 trials) to 2 (for weight = 4 and energy = -4), but then increase to 197 (for weight = 10 and energy = 4). The walkLength statistics varies significantly for each case – as does the distribution, which is bimodal, heavy-tailed, and clearly geometric for the case of only 2 unique solutions with weight = 4 and energy = -4.
- The beneficial side-effect our testing strategy is revealed for the case of weight = 4 and energy target = -3. Out of 1000 trials, there are 95 conformations with energy = -4, i.e. the returned solution is better than the target solution of -3. These solutions are in the class of 'rare solutions' where only two unique solutions have been reported after 1000 trials for weight = 4 and energy = -4. We shall take advantage of this strategy also when performing experiments on longer chains which are summarized in Section IV.

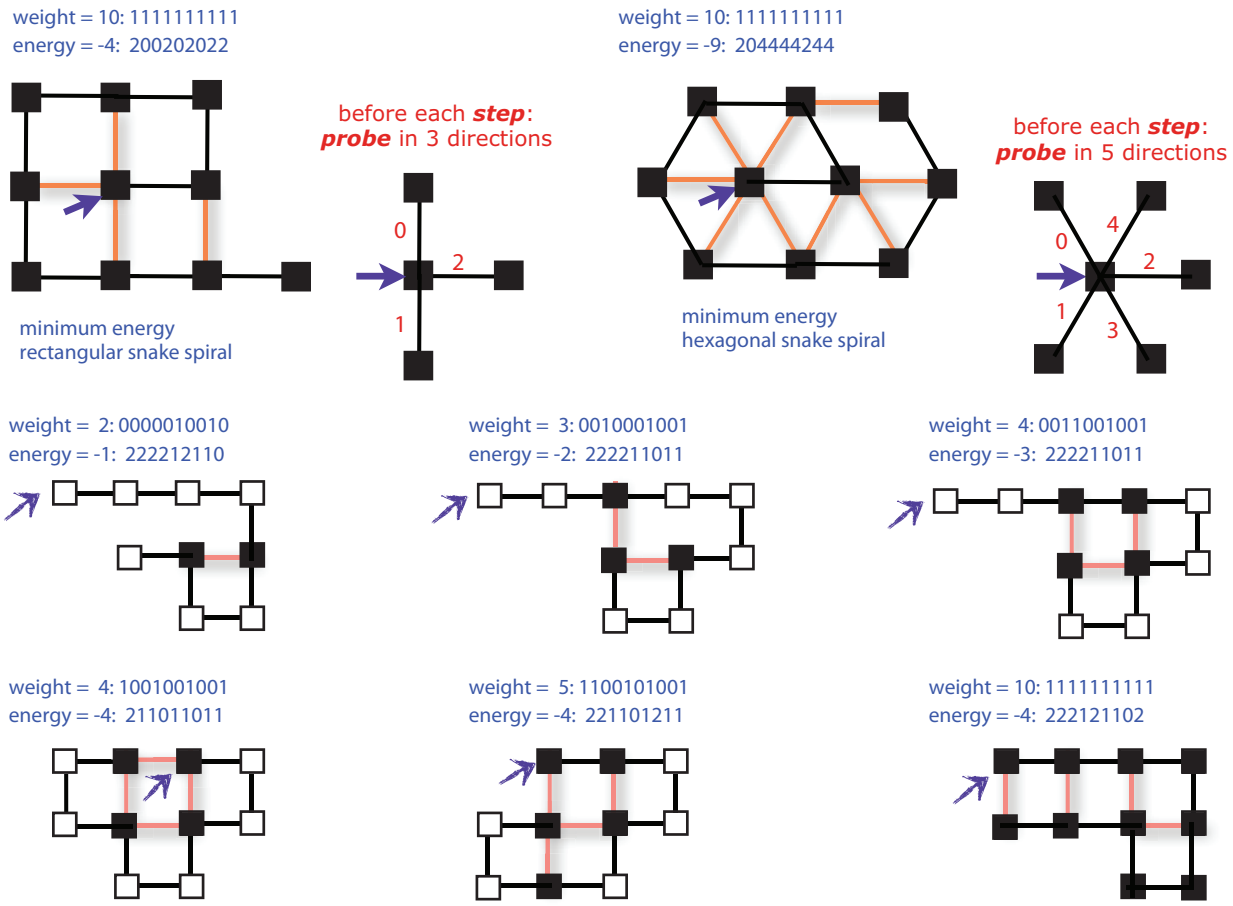
We complete this subsection with the summary of results under Plan A, Plan B, and Plan C, shown in Table 1. Notably, the search with SAW under the plan B (the inverse folding formulation) is significantly easier than the search under Plan A (the traditional folding formulation). However, the search with SAW under Plan C requires significantly more steps than the Plan A and Plan B combined. The experiment under Plan C in Table 1 is a replication, under a different initial seed, of the experiment in Figure 4 in the row weight = 4, energy = -4.

Global stochastic search under SAW. We now briefly formalize coordinate neighborhoods, walks, and self-avoiding walks, concluding with a concise pseudo code that is the basis for our prototype solver on stochastic search under SAW.

Coordinate neighborhood. Formally, a neighborhood of a coordinate $\underline{\varsigma}_j$ is a set of coordinates

$$N(\underline{\varsigma}_j) = \left\{ \underline{\varsigma}_j^i \mid d\left(\underline{\varsigma}_j, \underline{\varsigma}_j^i\right) = 1, \quad i = 1,2,...,L_j \right\} \quad (1)$$

where $d(\underline{\varsigma}_j, \underline{\varsigma}_j^i)$ is the rank distance between coordinates. The coordinate $\underline{\varsigma}_j$ is also called a pivot coordinate, has L_j neighbors, each a distance of 1 from the



Six folding experiments under the weight and energy target shown, with 1000 seeds each

binary weight	energy target	beyond target	unique solutions	walkLength median	walkLength mean	walkLength stdev	walkLength max	probesPerStep median	probesPerStep mean	probesPerStep stdev
2	-1	0	813	1000	843.6	695.5	2336	10.8	11.3	2.12
3	-2	0	511	39	338.0	580.7	2353	13	13.1	1.61
4	-3	95	204	26	104.1	290.7	2017	14.6	14.7	1.47
4	-4	0	2	797.5	1074.3	965.7	7433	13.9	14.0	0.82
5	-4	0	51	37.5	73.1	131.0	1755	15.8	16.0	1.27
10	-4	0	197	2	4.3	24.6	689	22	21.2	4.47

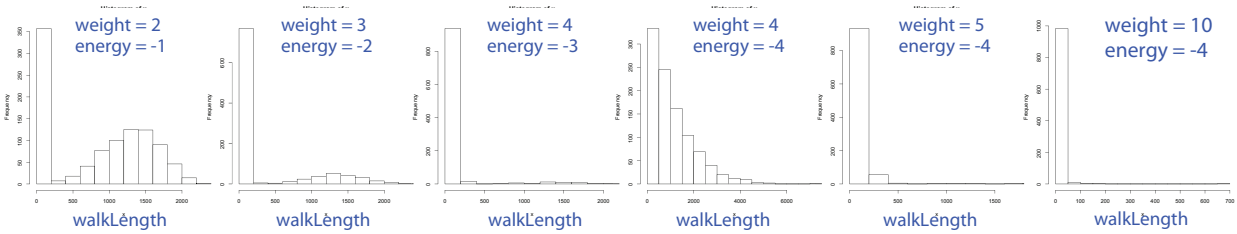


Figure 4: Empirical observations about the HP model of protein foldings in 2D with a chain of size 10 and SAWs: (1) lower bound on energy in rectangular grid is -4 (probes are made in 3 directions); (2) lower bound on energy in hexagonal grid is -9 (probes are made in 5 directions); (3) instances of 6 folding conformations in rectangular grid, each for a distinct pair of weight and energy target, define 6 classes of solutions; (4) walk length statistics and distributions, with a sample size of 1000 for each experiment. In order to find the postulated energy targets, an exhaustive enumeration or a Hamiltonian walk would visit, on the average, a total of $0.5 * (2^{10} * 3^9 - 1) = 10,077,696$ coordinates under the rectangular grid formulation (compare with the maximum of 7433 in the table) and a total of $0.5 * (2^{10} * 5^9 - 1) = 999,999,999$ coordinates under the hexagonal grid formulation. Our hypothesis: compared to the results shown here, the hexagonal grid may exhibit an energy landscape where SAWs will find energy minima in less steps on the average.

pivot coordinate. In Figure 5-a we illustrate a Hasse graph that highlights three neighborhoods. Coordinates in this graph are a concatenation of binary coordinates of length 2 and ternary coordinates of length 2. Each binary coordinate always has a neighborhood of 2 (dotted edges) while the neighborhood of ternary coordinate can vary from 2 to 4 (solid edges). For example, the coordinate 00.00 has 2 binary and two ternary neighbors; the coordinate 10.11 has 2 binary and 4 ternary neighbors.

In Figure 5-b we illustrate the dynamics of neighborhood evaluations for an instance shown in Figure 4. We could not possibly have drawn a Hasse graph for this instance, however the principle of binary and ternary neighborhoods illustrated in Figure 5-a are the same.

What we can show is the trace of the entire neighborhood evaluation that takes place: starting with the pivot coordinate 1100101001.21101111, the best coordinate of the next pivot in this neighborhood is 1100101001.21101211 since it has the best energy conformation of -4. The trace also shows values of the objective function for various conformations – all values that are > 0 represent conformations that would lead to a conflict during folding; penalties values are assigned at different levels: +8 (initial pivot), +9, +8, +4, etc. Not all binary coordinates have been evaluated due to an input requirement that weight <= 5. The situation where a pivot would get trapped by adjacent pivots and the neighborhood would become empty did not yet arise.

Contiguous walks and SAWs. Let the coordinate $\underline{\varsigma}_o$ be the initial coordinate from which the walk takes the first step. Then the sequence

$$\{\underline{\varsigma}_0, \underline{\varsigma}_1, \underline{\varsigma}_2, ..., \underline{\varsigma}_j, ..., \underline{\varsigma}_\omega\} \quad (2)$$

is called a walk list or a walk of length ω, the coordinates $\underline{\varsigma}_j$ are denoted as pivot coordinates and $\Theta(\underline{\varsigma}_j)$ are denoted as pivot values. Given an instance of size L and

Table 1: Statistical experiments with SAWs to solve, under Plan A, Plan B and Plan C, the HP model of protein folding in 2D on a square lattice. The input parameters for each plan are: Chain size = 10; Energy target = -4; either fixed binary coordinate coordB of weight 4 (plan A); or fixed ternary coordinate coordT (plan B); or both initialized randomly (plan C). Experiments are performed with 1000 initial coordinates for each plan, and both the energy target of -4 and the binary weight target of 4 are reached under each plan, always returning only one binary solutions and two ternary solutions. Walk lengths under each plan differ significantly, with plan C representing the hardest instance of the folding protein problem. This is also the problem where SAW is the most effective compared to the (hypothetical) hamiltonian walk.

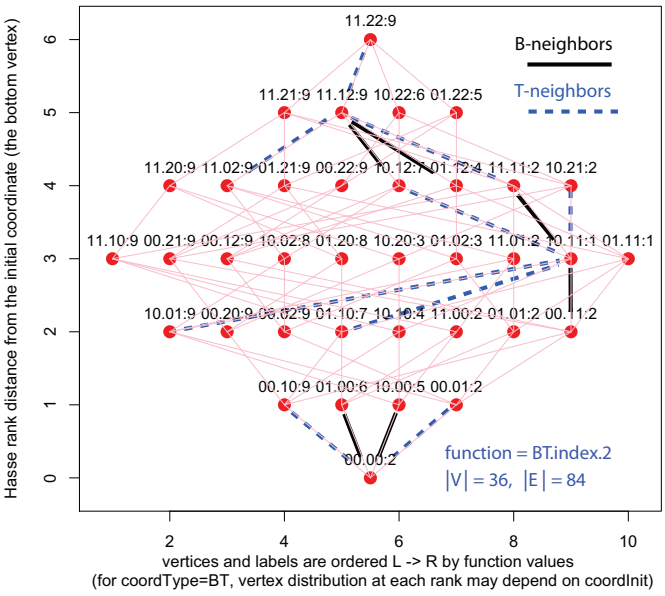
Plan A		median	mean	stdev	min	max
Given coordB	cntProbe	244	330.6	302.4	10	1994
with weight = 4,	walkLength	25	33.7	31.4	1	205
FIND coordT	probesPerStep	10	10.4	1.2	7.9	16
coordB = 1001001001						
coordT = 200100100	The average walkLength to reach one of the two coordT					
coordT = 211011011	under Hamiltonian walk = $0.25(3^9 - 1) = 4921$					

Plan B		median	mean	stdev	min	max
Given coordT,	cntProbe	26	34.0	15.6	1	127
FIND coordB	walkLength	4	5.2	2.4	0	20
with weight = 4	probesPerStep	6.5	6.5	0.49	1	8.5
coordT = 211011011	The average walkLength to reach the single coordB					
coordB = 1001001001	under Hamiltonian walk = $0.5(2^{10} - 1) = 511$					

Plan C		median	mean	stdev	min	max
FIND coordB,	cntProbe	10564.5	14187.8	12787.2	35	81156
with weight = 4	walkLength	752.5	1027.1	936.3	2	5936
& FIND coordT	probesPerStep	13.9	14.0	0.7	12.0	19.6
coordB = 1001001001						
coordT = 200100100	The average walkLength to reach one of the two coordT					
coordT = 211011011	under Hamiltonian walk = $0.25 * (2^{10} * 39 - 1) = 5038848$					

its best upper bound Θ_L^{ub}, we say that the walk reaches its target value (and stops) when $\Theta(\underline{\varsigma}_\omega) = \Theta_L^{ub}$.

We say that the walk is contiguous if the rank distance between adjacent pivots is 1; i.e. we find



Introduced in Figure 1, labels in this graph are a a concatenation of binary coordinates and ternary coordinates. Each binary coordinate always has a neighborhood of 2 (dotted edges) while the neighborhood of ternary coordinate can vary from 2 to 4 (solid edges). For example, the coordinate 00.00 has 2 binary and two ternary neighbors; the coordinate 10.11 has 2 binary and 4 ternary neighbors.

$$d(\underline{\varsigma}_j, \underline{\varsigma}_{j-1}) = 1, \quad j = 1,2,\ldots,\omega$$

We say that the walk is self-avoiding if all pivots in (2) are unique. We say that the walk is composed of two

```
% func.BT.neighb.saw foldHP2 1100101001.21101111

iB iT    coordB.coordT yBest n   p   coordT  y
NA NA     1100101001  . 21101111  +8  0  1          21101111   +8
 4 NA 1100       001001. 21101111  +8  1  2          21101111   +8
 9 NA 110010100       0. 21101111  +8  2  3          21101111   +8
 0 NA      0100101001.  21101111  +8  3  4          21101111   +8
 1 NA 1    00101001.    21101111  +8  4  5          21101111   +8
 6 NA 110010      0001. 21101111  +8  5  6          21101111   +8
NA  4     1100101001  . 21101111  +8  6  7 2110        2111 +9
NA  4     1100101001  . 21101111  +8  7  8 2110        0111 +9
NA  6     1100101001  . 21101111  +8  8  9 211011       21 +8
NA  6     1100101001  . 21101111  -2  9 10 211011       01 -2
NA  0     1100101001  . 21101111  -2 10 11          11101111 +4
NA  2     1100101001  . 21101111  -2 11 12 21        201111 +8
NA  2     1100101001  . 21101111  -2 12 13 21        001111 +8
NA  3     1100101001  . 21101111  -2 13 14 211        11111 +5
NA  5     1100101001  . 21101111  -4 14 15 21101       211   -4*
NA  5     1100101001  . 21101111  -4 15 16 21101       011 -2
NA  7     1100101001  . 21101111  -4 16 17 2110111       2 +8
NA  7     1100101001  . 21101111  -4 17 18 2110111       0 +8
NA  1     1100101001  . 21101111  -4 18 19 2       2101111 +8
NA  1     1100101001  . 21101111  -4 19 20 2       0101111 +8

1100101001.21101211 -4          <-- the next step to take
%
```

Indices iB and iT that address values in binary and ternary coordinates are always randomly permuted in order to prevent biasing the order of choices for best function value yBest. Function values y > 0 represent not only unfeasible conformations but also the relative level of unfeasibility. The counters n and p report the size of the neighborhood and the number probes to find each value of y.

Figure 5: An example of neighborhood calculation from an initial pivot coordinate (1100101001.21101111) that leads, in a single step, to an optimal conformation depicted in Figure 4.

Table 2: Statistical summary of experiments, a companion to Figure 8. Experiments under 'Referenced solutions' are under Plan A as defined in the paper. Experiments under 'Equivalent SAW solutions' and 'Better SAW solutions' are under Plan C. All experiments, except for the one flagged in the footnote, are based on a sample size of 1000. As an additional bonus, we also found another improved solution while running the case of L = 24, weight = 10, energy = 10. The energy improved from -10 to -11 and it is this conformation which shown in Figure 8.

	Reference solutions				Equivalent SAW solutions				Better SAW solutions			
	energy target	walkLength			energy target	walkLength			energy target	walkLength		
instance		median	mean	stdev		median	mean	stdev		median	mean	stdev
length = 20												
weight = 10	-9	2079	3097	2890.8	-9	315	812	1183.0	-10	9742	15088	16364
unique sols	4				928				109			
length = 24												
weight = 10	-9	957	1575	1765	-9	649	4104	54529	-10	9059	19391	26142
unique sols	35				975				875			
length = 25												
weight = 9	-8	13099	21557	27639	-8	959.5	9679	95154	-10	933928	1243210	1087628
unique sols	32				990				11*			

(*) Statistics for the pair (weight = 9, energy target = -10) are based on the sample size of 62 (rather than 1000) as is the case with other entries in this table.

```
1: s ← 1901                                   ▷ initial seed
2: ξ_0 ← coordInit(s)                         ▷ initial coordinate
3: Θ(ξ_0) ← ξ_0                               ▷ initial value
4: ξ* ← ξ_0                                   ▷ initial best coordinate
5: Θ(ξ*) ← ξ*                                 ▷ initial best value
6: ω ← 0                                      ▷ initial walk length
7: Θ_L^ub ← 0                                 ▷ initial upper bound
8: τ ← 1                                      ▷ initial cntProbe
9: τ_lmt ← 2^24                               ▷ cntProbe limit value
10: isCens ← 0                                ▷ initialize as uncensored
11: if Θ(ξ*) ≤ Θ_L^ub then
12:     Table ← (s, ξ*, Θ(ξ*), τ, ω, isCens) ; return
13: end if
14: while Θ(ξ*) > Θ_L^ub do
15:     if τ == τ_lmt then
16:         isCens ← 1 ; break
17:     else
18:         ω = ω + 1                         ▷ a new step!
19:         temp ← coordUpdate(ξ_{ω−1}, τ)
20:         ξ_ω : Θ(ξ_ω) : τ ← temp
21:         if Θ(ξ_ω) ≤ Θ(ξ*) then
22:             ξ* ← ξ_ω
23:             Θ(ξ*) ← ξ*
24:         end if
25:     end if
26: end while
27: if isCens == 1 then
28:     Table ← (s, ξ*, Θ(ξ*), τ, ω, isCens)
29: else
30:     if Θ(ξ*) == Θ_L^ub then
31:         Table ← (s, ξ*, Θ(ξ*), τ, ω, isCens)
32:     else
33:         Θ_L^ub ← Θ(ξ*) ▷ Better upper bound!
34:         Table ← (s, ξ*, Θ(ξ*), τ, ω, isCens)
35:     end if
36: end if
```

The procedure `coordUpdate.saw` takes the pivot coordinate, the probe counter and the walk list. In Step 6, it computes, in random order, the neighborhood $\mathcal{N}(\underline{\varsigma}_{\omega-1})$ of all adjacent coordinates. The order randomization ensures that all coordinates get an equal chance of selection; without it, some paths in the Hasse graph may never be taken, thereby inducing a bias in the average walk length. The Step 7 eliminates all adjacent coordinates that may have been used as pivots already and returns a neighborhood subset $\mathcal{N}_r(\underline{\varsigma}_{\omega-1})$. If the neighborhood subset is not empty, the procedure `bestNeighbor` in Step 9 probes all coordinates in the subset and returns the new pivot as the coordinate:value pair with the *'best value'*, along with the incremented value of τ, updates the walk list to $Walk_\omega$ in Step 10, and exits on Step 18. An empty neighborhood implies that the SAW is *trapped*, i.e. the selection of the pivot for the next step is blocked by adjacent coordinates that are already pivots. Subsequently, a new walk segment is initialized with a random coordinate in Step 15. The procedure exits with the expected parameter values on Step 16.

```
1: ω ← ω + 1
2: Walk_{ω−1} ← {ς_0, ς_1, ς_2, ..., ς_{ω−1}}
3: procedure COORDUPDATE.SAW(ς_{ω−1}, τ, Walk_{ω−1})
4:     ℤ ← i = 1, 2, ..., L
5:     ℤ_p ← permute(ℤ)
6:     𝒩(ς_{ω−1}) ← {ς^i_{ω−1} | d(ς_{ω−1}, ς^i_{ω−1}) = 1, i ∈ ℤ_p}
7:     𝒩_r(ς_{ω−1}) ← {𝒩(ς_{ω−1}) | ς^i_{ω−1} ∉ Walk_{ω−1}}
8:     if 𝒩_r ≠ ∅ then
9:         ς_ω:Θ(ς_ω):τ ← bestNeighbor(𝒩_r, ς_{ω−1}, τ_{ω−1})
10:        Walk_ω ← {ς_0, ς_1, ς_2, ..., ς_{ω−1}, ς_ω}
11:    else                                   ▷ trapped pivot, restart
12:        s ← randomSeed()
13:        ς_0 ← coordInit(s)                 ▷ new initial coord.
14:        Θ(ς_0) ← ς_0                       ▷ new initial value
15:        Walk_0 ← {ς_0}                     ▷ new walk segm.
16:        return ς_0:Θ(ς_0):τ:Walk_0
17:    end if
18:    return ς_ω:Θ(ς_ω):τ:Walk_ω
19: end procedure
```

Figure 6: The walk as a part of the **global stochastic search** process: the walk stops (1) upon reaching the best upper bound, returning a new or already known solution coordinate, or (2) upon finding a new best upper bound, returning a new best solution coordinate, or (3) upon exceeding the allocated time of counter limit, returning a new or already known censored solution coordinate and a value above the upper bound. The procedure that controls the performance of the walk, here a self-avoiding walk, is named coordUpdate.

or more walk segments if the initial pivot of each walk segment has been induced by a well-defined heuristic such as random restarts. Walk segments can be of different lengths and if viewed independently of other walks, may be self-avoiding or not. A walk composed of two or more self-avoiding walk segments may no longer be a self-avoiding walk, since some of the pivots may overlap and also form cycles.

Global stochastic search under SAW. The pseudo-code in Figure 6 formalizes the global search algorithm that relies on SAW as its search engine. The code forms the basis for the prototype solver not only for the porting folding instances experiments in this paper but also for a number of other problem instance as outlined in Section I.

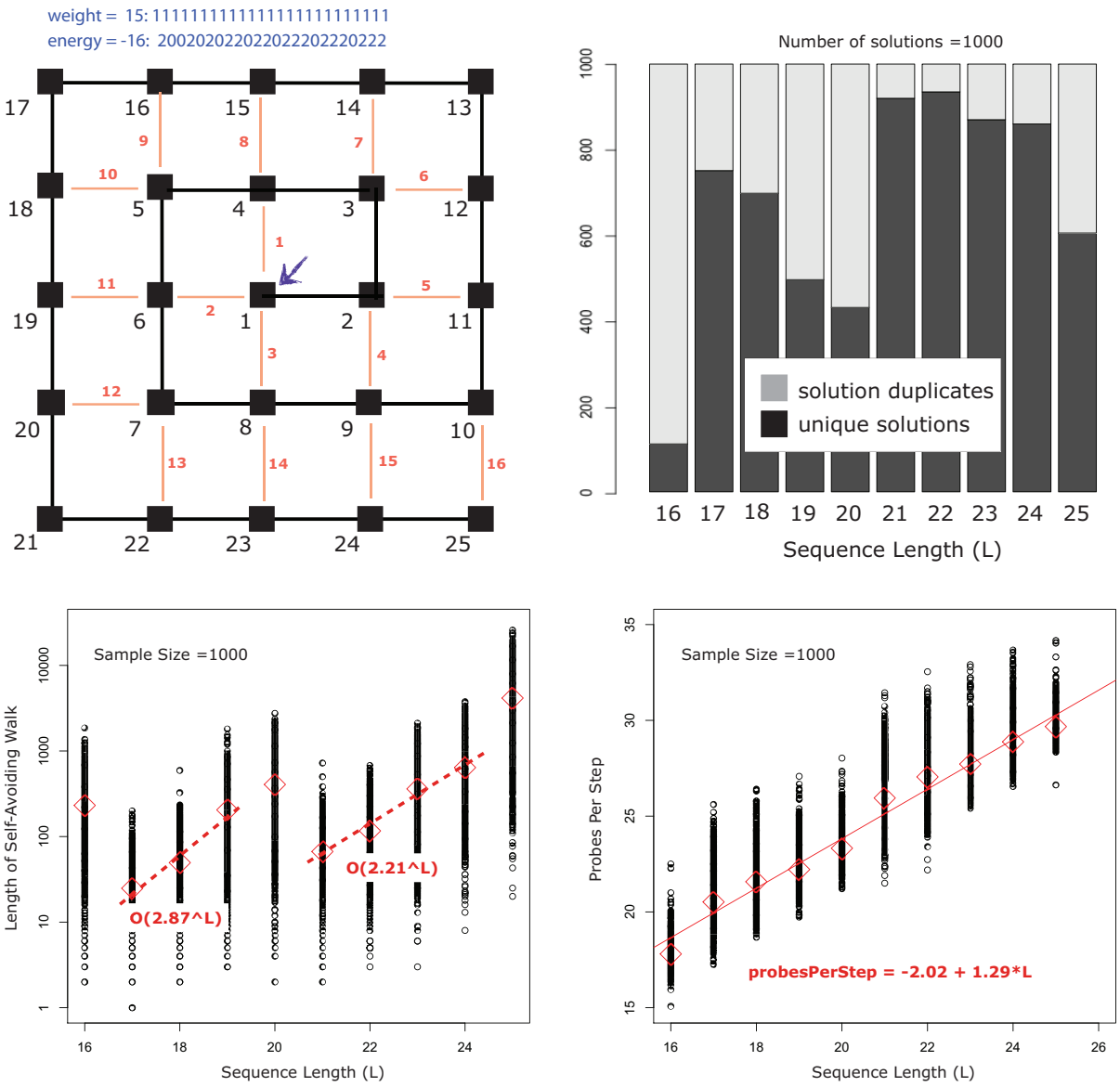


Figure 7: The spiral chain can be considered as a simpler case of the perfect HP problem posited for a 3-D cube in [18]. In our context, we ask: how many conformations can be found with the same energy and how hard is it to find them? Some of the answers can be gleaned from the asymptotic performance of the SAW solver in terms of the required walkLength to reach the minimum energy targets of (-9, -10, ..., -16) for chain lengths for L = (15, 17, ..., 25). It appears that there are clear different walkLength performance regimes when solving with L = (16, 20, 25) when compared to solving with other values of L.

4. Summary of Experiments

Experimental results, summarized in Figure 7, Figure 8, and Table 2, can only be descried briefly.

The motivation for the experiment in Figure 7 came from [18]:

Instance: An integer n and a finite sequence of S over the alphabet {H, P} which contains n^3 H's.

Question: Is there a fold of S in $\mathbf{Z}^3$ for which H's are perfectly packed into an n x n x n cube?

This problem has been proven to be NP-hard and the more general problem as NP-complete.

The spiral chain in Figure 7 can be considered as a simpler case of the perfect HP problem posited for a 3-D cube in [18]. In our context, we ask: how many conformations can be found with the same energy and how hard is it to find them? The answers that we display in

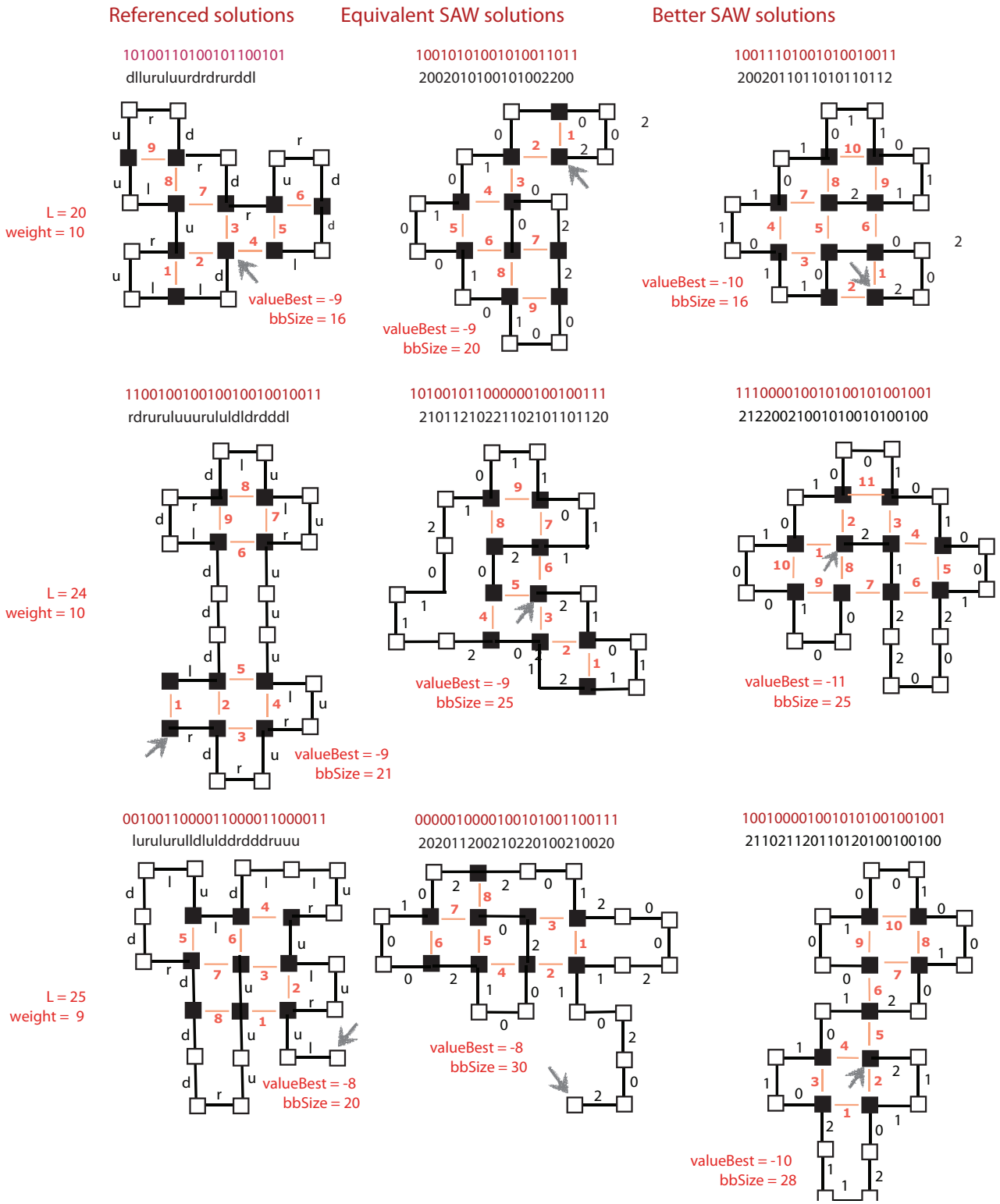


Figure 8: Comparisons of protein folding conformations for chain lengths of 20, 24, and 25. instance conformation in the column 'Referenced solutions' are from from [19] and [20] and have been reported under what we call Plan A in this paper. Instances under the column 'Equivalent SAW solutions' are alternative foldings obtained by our SAW solver under Plan C and the same energy targets as shown for 'Referenced solutions'. Instances under the column 'Better SAW solutions' are alternative foldings obtained by our SAW solver under Plan C and better energy targets: -10 vs -9 for L=20; -11 vs -9 for L=24, and -10 vs -8 for L=25.

Figure 7 are somewhat surprising and will be analyzed in more depth later.

Experiments performed on well-known instance classes under Plan A and Plan C are summarized in Figure 8 and Table 2. The main objectives are:

1. Under Plan A: replicate experiments to achieve the same or better target energy values published for standard instances with chains of length of 20, 24, and 25, given a fixed binary coordinate [19], [20]. Return solutions as ternary coordinates.
2. Under the first Plan C: find simultaneously, the pair of binary and ternary coordinates that maintain the weight of binary coordinates under Plan A – at the same or better target energy values.
3. Under the second Plan C: find simultaneously, the pair of binary and ternary coordinates that maintain the weight of binary coordinates under Plan A and exceed the energy target value found under the first experiments of Plan C.

Our findings so far:

- Under Plan A, our experiments replicate but not improve published energy target values.
- Under the first Plan C, our experiments generate up to 990 (out of 1000 initiated) new and unique solutions. In most cases, energy values remain the same as for Plan A. However, there also are improvements that lead to experiments under the second Plan C.
- Under the second Plan C, experiments with improved energy targets generate from 11 to 875 unique solutions with the assigned energy target value, except for the chain of length 24, where again, an improved energy target value is observed for two instances.

5 Conclusions and Future Work

Our experiments with the SAW solver raise the expectation that the solution of the protein folding problem, where the chain configuration and its confirmation are optimized simultaneously, may be feasible at an acceptable cost. One of the best way to accelerate improvements is cooperate with other researchers so that solver implementations can be compared side-by-side for their strengths and weaknesses, following the example in [9].

Experiments are being planned also for triangular and hexagonal grids in 2- and 3-dimensions.

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Delaying analogue quadrature signals in Sin/Cos encoders

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Abstract: Various measurement and control systems use magnetic or optical encoders that transform linear displacement and other physical quantities to an analogue quadrature signal. In this paper, we study the problem of, how to accurately delay the analogue quadrature signals in the Sin/Cos encoders within the range of ±10° with the circuit that is potentially integrable on a single chip. Such precision is needed for the efficient phase shift compensation. The typical analogue delay circuit comprises a summing amplifier and a digitally controlled variable resistor that is used to set a delay. We propose a new circuit based on the voltage divider with better linearity and a completely symmetrical range. The design procedure for the delay circuit is also presented.

Keywords: quadrature encoder signals, phase delay, error analysis, delay circuit, analogue quadrature signals.

Zakasnjevanje analognih kvadraturnih signalov v Sin/Cos enkoderjih

Izvleček: Razni krmilni in merilni sistemi uporabljajo optične in magnetne enkoderje, ki pretvarjajo linearni pomik in tudi druge fizične veličine v analogni kvadraturni signal. V tem prispevku objavljamo rezultate raziskave, v kateri smo proučevali problem natančnega zakasnjevanja enega izmed kvadraturnih signalov, ki jih generirajo Sin/Cos enkoderji. Natančnost zakasnitve je pomembna za učinkovito korekcijo faze. Rešitev za zakasnjevanje v območju ±10° smo iskali v obliki vezja, ki je integrabilno. Tipično analogno vezje, ki se uporablja za zakasnjevanje, temelji na seštevalniku, ki vsebuje digitalno krmiljen potenciometer. Z novo strukturo zakasnilnega vezja, ki temelji na napetostnem delilniku, smo dosegli boljšo linearnost in popolnoma simetrično območje. Prikazan je tudi načrtovalski postopek.

Ključne besede: kvadraturni signali, fazna zakasnitev, analiza pogreška, zakasnilno vezje, enkoder.

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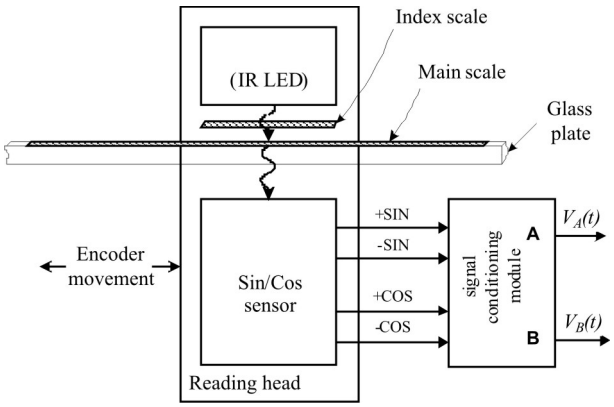
1 Introduction

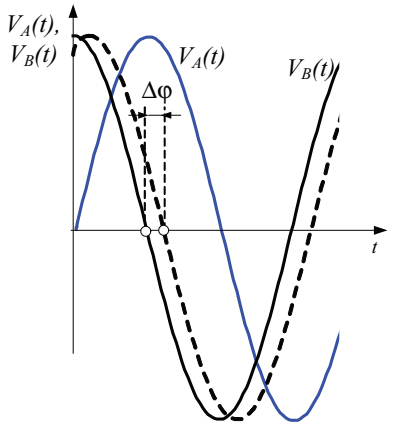
Various measurement and control systems use magnetic or optical encoders that transform linear displacement, the angular position, velocity, and other physical quantities to an analogue quadrature signal. The precision of the system is further improved with the interpolator. The ideal quadrature signals consist of two periodic signals with equal amplitudes and a relative phase shift of 90°. The signals are usually denoted as signal A and signal B or SIN and COS signal (Fig. 1).

Imperfections of encoders and quadrature signals are the major cause of the interpolation error. A method for estimating the accuracy of quadrature output sensors is proposed in [1-2]. The reduction of the imperfections can be performed either in software or implemented with the conditional circuit which is inserted between the output sensors and the interpolator [3]. Authors [4-8] proposed various interpolation algorithms that reduce the imperfections of the signals. These approaches generally require high-precision ADCs and a high-speed DSP to compute the angle to the required resolution. A harmonic distortion reduction achieved by adequate design of a reading-plate is also reported in [9].

All proposed methods are aimed toward the compensation of the imperfections. In this paper, we focus on the problem of how to precisely set the small delay $\Delta\varphi$ of the analogue quadrature signal within the interval (-10°, 10°). Such precision is needed for the efficient phase shift compensation. The most straightforward way to delay an analogue harmonic signal is to use a circuit with at least one reactance as in the analogue



a.



b.

Figure 1: a. Sin/Cos sensor and **b.** the quadrature signals

phase shifter. Yet these solutions are frequency dependent. The second method is based on a trigonometric identity: adding a fraction of signal A to signal B delays a cosine signal. The typical analog delay circuit, based on this idea, comprises a controlled resistor and a summing amplifier [3, 9, 10] In this paper we propose a new circuit that has better linearity and is based on the voltage divider.

This paper is organized as follows. In Section 2, we briefly describe the theoretical aspect of the delaying an analogue orthogonal signal and the structure of the proposed circuit. Example of the design procedure is in Section 3. The experimental version of the proposed circuit was built and the measurements were carried out (Section 4). Finally, the results are summarized in the Conclusion section.

2 Delaying the orthogonal signals

The ideal quadrature signals consist of two periodic signals with equal amplitudes and with a relative phase shift of 90°. The actual signals are harmonically distorted, have unequal amplitudes ($Vs \neq Vc$), have DC offset (V_0) and a phase shift offset ($\Delta\varphi_0$). If the harmonic distortion is neglected then signals can be expressed as

$$V_A(t) = V_s \sin(\omega t) + V_{os} \quad \text{and}$$
$$V_B(t) = V_c \cos(\omega t + \Delta\varphi_0) + V_{oc} \tag{1}$$

It will be assumed that signal B has to be delayed, and the total shift is smaller than 10°

$$|\Delta\varphi_0 + \Delta\varphi| \le \Delta\varphi_{\max}, \quad \Delta\varphi_{\max} = 10^\circ \tag{2}$$

Given is the required phase shift step k_φ and delay interval ($\pm\Delta\varphi_{max}$). Let b denote the control signal. Then the characteristic of an ideal delay circuit is specified by

$$\Delta\varphi(b) = \pm k_\varphi b, \; b = 0, 1, 2 \ldots b_{max} \tag{3}$$

The most straightforward way to delay an analogue harmonic signal is to use a circuit with at least one reactance as in the analogue phase shifter. Yet these solutions are frequency dependent. The second method is based on a trigonometric identity: adding a fraction of signal A to signal B (see Fig. 2) delays a cosine signal.

$$V_{c\_out} \cos(\omega t + \Delta\varphi) = V_c \cos(\omega t) + kV_s \sin(\omega t) \tag{4}$$

where $-1 < k < 1$. Let k_A denote the amplitude imbalance of the signals A and B

$$k_A = \frac{V_s}{V_c} \tag{5}$$

Note that value of the actual amplitude imbalance k_A is not known precisely and may vary within known ranges.

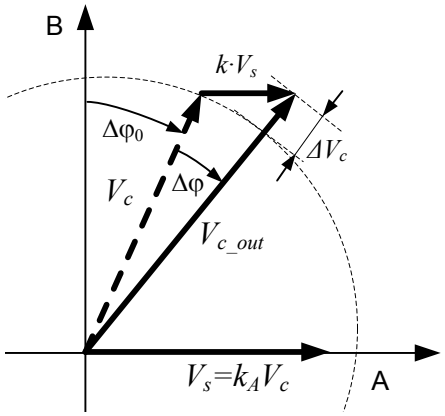


Figure 2: Positive Δφ increases the amplitude of signal B. Note, that amplitudes of real signals are not equal

By applying the trigonometric formulas and considering (5), the resulting delay is given by

$$\Delta\varphi(k,\Delta\varphi_0)=45^\circ-\frac{\Delta\varphi_0}{2}+arctg\left(\frac{(k_Ak-1)}{(k_Ak+1)}\cdot\frac{\cos\Delta\varphi_0}{1+\sin\Delta\varphi_0}\right) \quad (6)$$

Note, that delay does not depend solely on *k*, but also on the phase shift offset $\Delta\varphi_0$ and amplitude imbalance k_A as well. Furthermore, adding the signal B also increases/decreases the amplitude of signal A for ΔV_c (see Fig. 2)

$$V_{c\_out}=\sqrt{(kV_s)^2+(V_c)^2-2kV_sV_c\sin\Delta\varphi_0}=V_c+\Delta V_c \quad (7)$$

If there is no initial phase shift offset ($\Delta\varphi_0$=0°) the equations (7) reduces to

$$V_{c\_out}=V_c/\cos\Delta\varphi;\ \Delta\varphi>0 \quad (8)$$

$$V_{c\_out}=V_c\cos\Delta\varphi;\ \Delta\varphi<0$$

To set a required delay digitally, *k* in (6) has to be controlled by the digital signal *b*. If $\Delta\varphi_0$ = 0°, the equation (6) simplifies to

$$\Delta\varphi(b)=arctg(k_Ak(b)),\ \ b=0,1,2\ldots b_{max} \quad (9)$$

The relation (9) is approximately linear[1], if *k* is small

$$\Delta\varphi(k)\approx\frac{180}{\pi}k_Ak \quad (10)$$

The required range of *k* is

$$k\approx\pm\frac{\Delta\varphi_{\max}\pi}{180} \quad (11)$$

If $\Delta\varphi_{max}=\pm10°$ is chosen, then the required range of *k* is ±0.1745. The biggest change of the amplitude within this range is ±1.5 %.

Fig. 3 (a) shows typical implementations of the equation (4) [3, 9, 10]. A small amount of signal A is added to signal B using a summing amplifier. A desired fraction of signal A is set by the value of R_d, whereas R_{bs} is needed for setting the step of the delay. The influence of the wiper's resistance[2] R_w (see Fig. 4) and the week linearity are the main disadvantages of this variant. We propose a new circuit based on the voltage divider with better linearity and a completely symmetrical range (Fig. 3(b)). For these reasons we decided to study variant based on the voltage divider.

2.1 Delay circuit

A scheme of the implemented circuit shown in Fig. 3(b) is presented in Fig. 5. A delay is set by digital potentiometer RD. The unity gain amplifier A_5 eliminates the

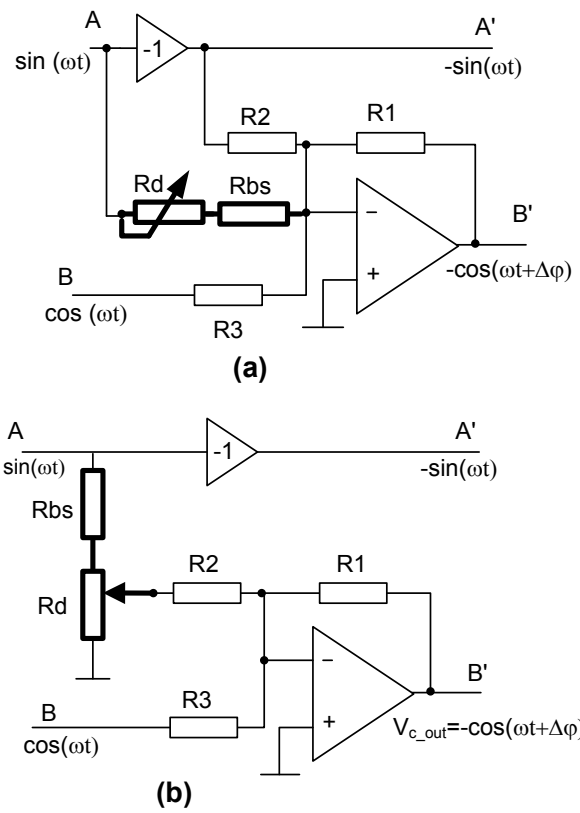


Figure 3: Two possible configurations of the delay circuits

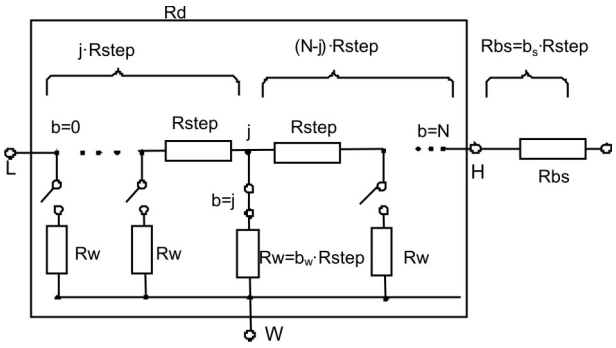


Figure 4: Simplified model of a digital potentiometer R_d with N segments and the additional resistor R_{bs}. R_w is a resistance of the CMOS switch.

influence of the wiper's resistance R_w. All control signals for the digital potentiometers are generated with FPGA module. The fraction of the signal A is added to a signal B by a specially designed summing amplifier A_2. Unity gain amplifiers (A_7, A_6) may be neglected if the output resistance of the sensors is low. Out of the many imperfections only the amplitude imbalance k_A will be considered in the analysis that follows. Since DC offset affects phase shift, all opams should have low offset voltage.

1 $arctg(x)=\left(x-x^3/3+x^5/5-\ldots\right)$

2 *For the 128-tap, 100kW digital potentiometer MAX5439 is Rw = 0.9 ... 2kW*

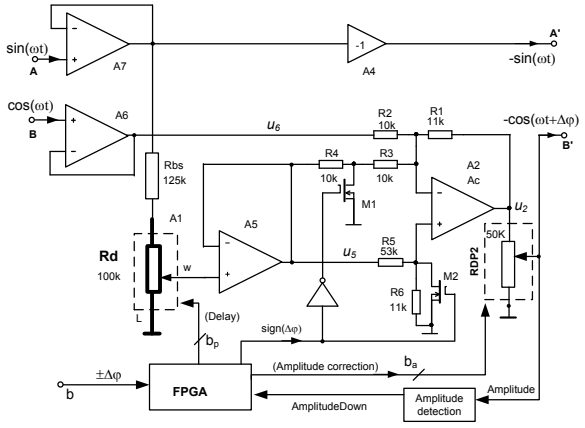


Figure 5: An implemented delay circuit with simple amplitude correction circuit

First, we rewrite the equation (9) into the form

$$\Delta\varphi(b) = arctg\left(k_A A_1(b) A_2\right) \tag{12}$$

where A_2 is a gain of the summing amplifier and $A_1(b)$ is the attenuation of the voltage divider. By applying a model of N-bit digital potentiometer (see Fig. 4), we obtain

$$A_1(b) = \frac{b}{N + b_s} \tag{13}$$

Note that b is in the numerator, which means that A_1 is linearly dependent on b. Let Ac denote the gain u_2/u_6 and A_2 the gain u_2/u_5

$$A_c = u_2 / u_6 = -R1 / R2 \tag{14}$$

The analysis of the circuit gives

$$\begin{aligned} u_2 &= A_c V_c \cos\omega t + A_c k_A A_1(b) V_c \sin\omega t = \\ &= A_c V_c \left(\cos\omega t + k_A A_1(b) \sin\omega t\right) \end{aligned} \tag{15}$$

This proves the correct implementation of the theoretical model (4). Note, that A_c does not affect the phase shift but the amplitude of the delayed signal.

The sign of the delay is controlled by MOS switches M1 and M2. For $\Delta\varphi<0$ is M1 OFF and M2 is ON. If the change of amplitude (8) cannot be tolerated, then the amplitude correction is needed. If the amplification of cos signal, that is defined by ratio R1/R2, is greater that one, then oversized output amplitude can be adjusted with a divider RDP2 that is controlled by the amplitude detection circuit. By choosing R2=R3=R4, we obtain

$$A_2 = \frac{u_2}{u_5} = -\left(\frac{R1}{R3 + R4}\right) = -\frac{A_c}{2} \tag{16}$$

To achieve positive delay the summing amplifier is transformed by the switches M1=ON, M2=OFF to the non-inverting type with the same inverted gain.

$$A_2 = \frac{u_2}{u_5} = +\left(\frac{R6}{R5 + R6}\right)\left(1 + \frac{R1(R2 + R3)}{R2R3}\right) = +\frac{A_c}{2} \tag{17}$$

The equal gain (11) is obtained by the appropriate ratio R6/R5:

$$\frac{R5}{R6} = \frac{2}{A_c} + 3 \tag{18}$$

Note that gains A_1, A_2 and Ac are well defined since they depend on the ratio of resistors. A_c has to be greater than one to ensure that the amplitude of u_2 will always be greater than Vc. This oversized output amplitude of cos signal is reduced to Vc with a divider RDP2 that is controlled by the amplitude detection circuit.

The equation (12) can be rewritten now

$$\Delta\varphi(b) = arctg\left(\frac{k_A}{2}\frac{b}{(N + b_s)}\right) \tag{19}$$

If the amplitude imbalance k_A is unknown then k_A has to be considered as a random variable. In order to reduce the phase error, amplitudes has to be equalized by a special circuit. For small delays is (19) approximately linear

$$\Delta\varphi(b) \approx \frac{180}{\pi}\frac{k_A}{2} \cdot \frac{b}{(N + b_s)} = \Delta\varphi_{step} b \tag{20}$$

By rearranging (18) and setting $\Delta\varphi_{step} \approx k_\varphi$ we can derive a designing rule for R_{bs}

$$R_{bs} = b_s R_{step} = \left(\frac{90 k_A}{\pi k_\varphi} - N\right) R_{step} \tag{21}$$

2.2 Reducing the systematic error due to the nonlinearity

Let $\Delta\varphi_{err\_s}$ denote the systematic error, which is the difference between a measured $\Delta\varphi(b)$ and the target value

$$\Delta\varphi_{err\_s}(b) = \Delta\varphi(b) - k_\varphi b \tag{22}$$

One reason for the $\Delta\varphi_{err\_s}$ is a nonlinear function arctg in (12). If the argument of the arctg follows tg function, then the nonlinearity is eliminated:

$$\begin{aligned} \Delta\varphi(b) &= arctg\left(k_A A_1(b) A_2\right) = \\ &= arctg\left(tg\left(k_A A_1(b) A_2\right)\right) = k_A A_1(b) A_2 \end{aligned} \tag{23}$$

The simplest way to implement this idea is to adequately change the value of the signal b. Let b_p denote modified control signal

$$b_p = b + \Delta b \tag{24}$$

From (23) we can derive a modification rule $b \rightarrow b_p$:

$$b_p = floor\left(0.5 + \frac{2(N+b_s)}{k_A} tg\left(\frac{k_A}{2}\frac{b}{(N+b_s)}\right)\right) \tag{25}$$

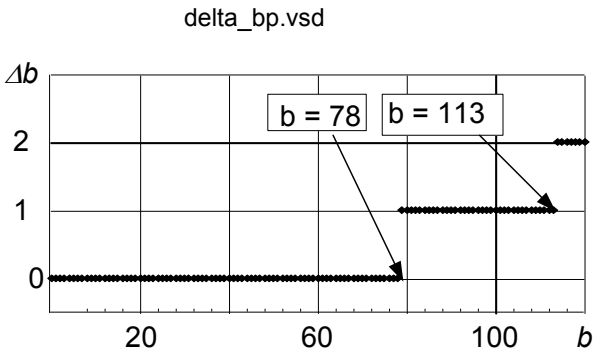


Figure 6: The solution of (25) and (24)

From the solution of (24) and (25) a simple modification rule can be constructed (see Fig. 6). If the range of the control signal is b=1…127, then the rule is

if (b≤78) then $b_p = b$
if (78<b<113) then $b_p = b+1$
if (b≥113) then $b_p = b+2$

Note that the modification rule reduces the range

$$b_{\max} = N - \Delta b_{\max} \tag{26}$$

For example, If $k_\varphi = 0.1°$ and $N = 127$, then the biggest error is $\Delta\varphi_{err\_s} = -0.15°$ (Fig. 7(b)). By using the correction of the signal b, the error is not completely eliminated yet substantially reduced: $-0.06° < \Delta\varphi_{err\_s} < +0.06°$ (see (Fig. 7(a))).

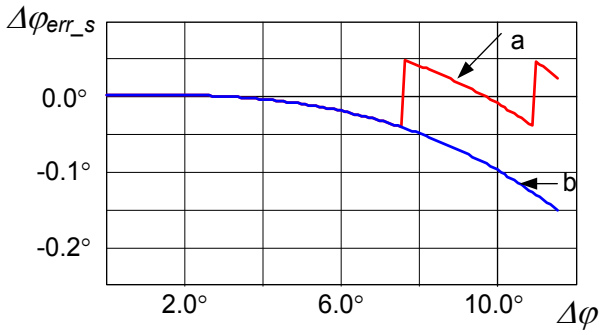


Figure 7: Systematic (linearity) error $\Delta\varphi_{err\_s}$ (Eq. 11, 23 and 25) for $k_\varphi = 0.1°$ and $N = 127$. Amplitudes are equal ($k_A \approx 1$). **a** with linearity correction, **b** without correction

3 Example of the design procedure

Given are: $k_\varphi = 0.1°$, $\Delta\varphi_{max} \leq 10°$, $\Delta\varphi_{min} \geq -10°$, $k_A \approx 1$

128-tap, 100kΩ digital potentiometer MAX5439 was selected for a prototype with discrete components. This means: R_d = 100 kΩ, N=127 and R_{step}=787Ω. If the integrated version were planned then N would be 101. Equation (21) gives b_s = 159 and R_{bs}=125kΩ. A_c was chosen 11/10 and R2=R3=R4=10kΩ. Equations (14) and (18) determine the value of R1=11kΩ and R5/R6=53kΩ/11kΩ. The resulting theoretical characteristics (19) of the delay circuit are:

$$\Delta\varphi(b) = -arctg\left(\frac{b}{572}\right);\ b = 0, 1, 2, \ldots 125$$

$\Delta\varphi_{max}$ = 12.52° , $\Delta\varphi_{min}$ = -12.52° , $|\Delta\varphi_{err\_s}| < 0.06°$, $|\Delta\varphi_{step}| = 0.10°$

4 Measurement results

To estimate a worst-case a SPICE simulator was applied. OPA27 amplifiers and two digital potentiometers (128-Tap MAX5437 and MAX5439) were used in the prototype circuit. The magnetic encoder sensor was replaced by the signal generator that generates almost perfect signals. Each delay was measured 100 times with digital oscilloscope LeCroy LT344. Data for the positive delay[3] are shown in Fig. 8. The signal generator had an offset delay ($\Delta\varphi_{err}(b = 0)$) which was removed in the analysis. The biggest total error $\Delta\varphi_{err}$ = 0.39° was at 10°. Best results were in the range from 0° to 5° where total error was below 0.2°.

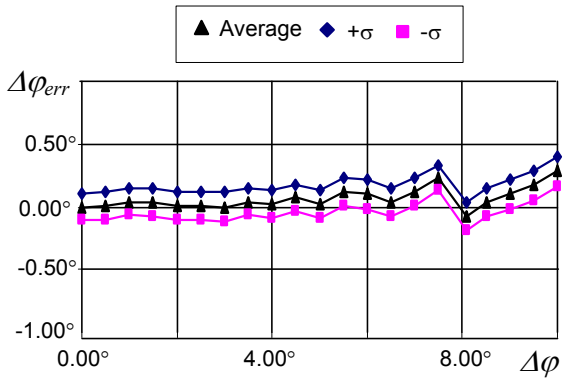


Figure 8: Simulation and actual measurement results (f = 1 kHz)

3 *The negative delay had even better results*

5 Conclusions

In order to achieve a precise delay, low-offset voltage opamps are required and the circuit has to be designed in such a way, that the delay depends only on the ratio of the resistors. The design procedure for the delay circuit was developed: two out of four parameters (N, A_c, k_φ, $\Delta\varphi_{max}$) can be chosen, the other two are calculated. If the signals are perfect and frequency is low, then the precision of the delay is limited only by the systematic error $\Delta\varphi_{err-s}$ and the resistors ratio. In the ideal case the phase step defined by $\Delta\varphi_{step} = \Delta\varphi_{max}/N = 10°/128 = 0.08°$. The actual usable $\Delta\varphi_{step}$ depends on the quality of the signal and on the tolerances as well. To verify the theoretical results the SPICE simulation was applied and a discrete prototype of the delay circuit was built. The prototype shows that with the discrete elements it is possible to obtain the total error below 0.2° in the range from 0° to 5°, if signals are of good quality. To obtain more reliable yield estimation the additional tolerance analysis is needed.

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A Novel Topology of Variable Gain Distributed Amplifier in 0.13 μm CMOS Technology for UWB Applications

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Abstract: We present a new design of CMOS variable gain distributed amplifier (VGDA) by using a new topology of gain cell and a preamplifier circuit. In order to improve the gain, the proposed gain cell has modified cascade structure with optimized bulk source bias. Variable gain is made in the Preamplifier circuit. This section also increases the gain. Another significant advantage is that the noise level of VGDA has reduced. For this architecture, number of stages calculated in optimum mode and achieved third stages. The main advantage of this circuit is gain control with high range, and best input/output impedance matching in all of range and throughout the entire bandwidth. High flatness gain (in optimum mode) and low noise with best reverse isolation over the entire bandwidth up to 10 GHz are the other features of the proposed VGDA, which makes the VGDA to be more stable. The complete designed circuit was simulated in Taiwan Semiconductor Manufactory Company (TSMC) O.13 μm CMOS technology. The simulated provide a gain control range of 39 dB, from -10 dB to +29 dB, 29.4 dB as flat gain in optimum mode, 2.93 dB as the noise figure average across the bandwidth. Reverse isolation is better than –45.8 dB across the bandwidth, the input/output return loss is better than -10 dB and 61 mW total dc power consumption.

Keywords: CMOS distributed amplifier, variable gain, ultra wide band (UWB), high gain, low noise

Nova topologija porazdeljenega ojačevalnika s spremenljivim ojačenjem v 0.13 μm CMOS tehnologiji za UWB naprave

Izvleček: Predstavljamo nov obliko CMOS porazdeljenega ojačevalnika s spremenljivim ojačenjem (VGDA) z uporabo nove topologije ojačevalne celice in predojačevalnega vezja. Za doseganje višjega ojačenja ima predlagana ojačevalna celica modificirano kaskadno strukturo z optimizirano prednapetostjo substrata. Spremenljivo ojačenje je izvedeno v predojačevalnem vezju. Drugo pomembna novost je znižanje nivoja šuma. Glavna prednost vezja je kontrola ojačenja v visokem obsegu, najboljše ujemanje vhodne in izhodne impedance v celotnem območju in pasovni širini. Celotna struktura je bila simulirana v Taiwan Semiconductor Manufactory Company (TSMC) v 0.13 μm CMOS tehnologiji. Simulacije so pokazale kontrolo ojačenja od -10 dB do +29 dB z 29.4 dB ravnim ojačenjem pri optimalnem delovanju. Šum čez celotno pasovno širino znaša 2.93 dB. Reverzna izolativnost je boljša od -45.8 dB čez celotno pasovno širino; vhodno izhodne povratne izgube boljše od -10 dB in skupna dc moč 61 mW.

Ključne besede: CMOS porazdeljen ojačevalnik, spremenljivo ojačenje, UWB območje, visoko ojačenje, nizek šum

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1. Introduction

Recently, CMOS distributed amplifiers (DAs) have become increasingly popular for ultra-wideband (UWB) systems with 3.1 to 10.6 GHZ bandwidth, because of its wide input-impedance-matching bandwidth, wide gain bandwidth, and excellent linearity, UWB circuits find applications in various fields, such as high-speed

links, high resolution radars, imaging systems, wideband military systems, electronic warfare and broadband commercial radio systems. Among all kinds of high-speed circuits, the wideband amplifier is a key building block at both the transmitting and receiving ends. So far, however, to design the high speed analog systems some contradictory characteristic must be comprehended such as gain, operating frequency, impedance matching, power and noise. Accordingly the design of ultra wide band amplifier is one of the most significant issues in wireless networks. Design of high speed analog circuits requires adapting to contradictory characteristics, including gain, operating frequency, impedance matching, power, and noise, thus the design of ultra wide band amplifier is one of the most important issues in wireless networks. The distributed configuration is used frequently due to its wide bandwidth and high tolerance of process variation. As the semiconductors technology advances, the distributed amplifier (DA) becomes increasingly popular. Although a conventional distributed amplifier (CDA) can achieve a broad bandwidth, due to additive gain mechanism, obtaining a high gain is impracticable [1]. For wideband applications, approximately, the gain of CMOS CDA is restricted to 10dB, even though various circuit techniques have been reported such as the capacitive division technique [2], m - derived technique, loss-compensation technique with negative resistor [1,3] also negative capacitance [4] and nonuniform design approach [5]. Recent developments in the field of CDA, have led to acquiring high gain. These developments include cascaded multi-stage distributed amplifier (CMSDA) [6,7], matrix DA [8], cascaded single-stage distributed amplifiers (CSSDAs) [9], combination of the conventional DA and the cascaded single stage DA [10], and DA with internal feedback [11]. Recently, the DAs with gain control feature are used in various applications. The researches to date, have tend to focus on different methods which have been used for constructing this circuit. Programmable gain distributed amplifier (PGDA) [12] and variable gain distributed amplifier (VGDA) [13-16] are two major topology design methods of this circuit. Input and output impedance matching and stability throughout range, play a key role in designing these circuits and must be investigated attentively. However, a major problem with designing a faultless VGDA, is that there is almost no topology which possesses all the ideal characteristics such as high gain, broad bandwidth, low noise figure (NF), good impedance matching and low dc power consumption. This paper will focus on a new topology for designing VGDA, which relieves more appropriate range control. It has also devalued noise level while higher gain has obtained. Reverse isolation and input and output impedance matching are the other apparent characteristics of this new topology. This paper critically discusses this issue. It has been organized in 5 sections as below: In section 2, theories of distributed circuit and variable gain distributed amplifier have given. In section 3, the proposed VGDA topology has presented. Circuit design and simulation are discussed in section 4 and eventually section 5 presents conclusions.

2 Theory of DA and VGDA

In this section, brief description of distributed circuit has given; then DA has investigated.

2.1 Distributed circuit

A compact circuit is a kind of circuit which dimensions are small compared to the wave length of desired signal. At high frequencies, the device dimension is comparable to the wavelength of the signal and hence could not be called circuit as compression that circuit assumed to distribute. In general, the distributed term can be considered as any system that uses parallel signals from multiple directions [3]. Implementation of this circuit in CMOS technology is more interesting due to low cost and good performance. Distributed circuits in the microwave range are very common and utilizable. Amplifiers, oscillators and mixers are Instances of these circuits. In continue a new topology of DA which obtains high efficiency and low noise are presented.

2.2 Distributed amplifier

The concept of distributed amplification has been around for over Seventy years. Although the term distributed amplifier was coined in a paper by Ginzton et al. in 1948 which used vacuum tubes, the underlying concept can be traced to the patent specification entitled "Improvements in and relating to thermionic valve circuits" filed by Percival in 1935. Traditionally, DA design architectures have been realized using III-V semiconductor technologies, such as GaAs [17] and InP [18], it because of the extraordinary performance of technologies, this performance generate from higher band gaps (higher electron mobility), higher saturated electron velocity, higher breakdown voltages and higher resistivity substrates. The latter contributes to the availability of higher quality-factor (Q-factor or simply Q) integrated passive devices in the III-V semiconductor technologies. Even so, in order to meet the marketplace demands on cost, size, and power consumption of monolithic microwave integrated circuits (MMICs), ongoing research continues in the development of mainstream digital bulk-CMOS processes for such purposes. In 1997, the first implementation of distributed amplifier CMOS technology (0.8 μm) was performed.

Allstot group in Washington University had presented the general solution for DA with CMOS technology in 2000 and 2002 [19,20]. DA had overcome balance between gain and bandwidth.

A schematic of the CMOS conventional distributed amplifier is shown in Figure 1. As it can be seen, CDA consists of two main parts: gain cell, gate and drain transmission lines. These two lines implemented either by artificial transmission lines (in compare with cascade of LC filter sections to form a ladder type structure) or by uniform transmission lines. The internal capacitors of transistor can provide essential capacity. The operation of a DA is based on the fact that the signal from the input travels forward along the gate line and gets amplified by each transistor. The drain line carries these amplified signals both in the forward and reverse direction. The forward traveling waves on the drain line are in phase synchronization with the forward traveling wave of the gate line and with each other, implying that each device adds power in phase to the output signal at each tap point on the drain line. The forward traveling wave on the gate line and the reverse traveling wave on the drain line are absorbed by terminations which are generally matched to the loaded gate and drain lines.

Assuming the transmission lines to be lossless, the propagation constant and characteristic impedance of the transmission lines is given by:

$$\gamma_g = \alpha_g + j\beta_g \approx j\omega\sqrt{L_g\left[C_g + \frac{G_{gs}}{l_g}\right]} \tag{1}$$

$$Z_g = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{L_g}{C_g + \frac{C_{gs}}{l_g}}} \tag{2}$$

For the gate line and:

$$\gamma_d = \alpha_d + j\beta_d \approx j\omega\sqrt{L_d\left[C_d + \frac{G_{ds}}{l_d}\right]} \tag{3}$$

$$Z_d = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{L_d}{C_d + \frac{C_{ds}}{l_d}}} \tag{4}$$

Where α is the attenuation constant and $\beta = \frac{2\pi}{\lambda}$ is the wave number, Under perfect matching conditions both the lines are terminated by their characteristic impedances (Z_g, Z_d are gate and drain line characteristic impedances, respectively) [21].

2.2.1 Gain of distributed amplifier

Assuming phase synchronization on each of the lines we have:

$$\beta_g l_g = \beta_d l_d = \beta\, l = \Theta \tag{5}$$

And l_g, l_d are gate and drain line length, respectively. The voltage gain is given by:

$$A_v = -\frac{NgmZ_d}{2} e - jN\Theta \tag{6}$$

Where N is the number of stages or sections in the amplifier. With the increase in the number of sections in a DA the gain increases linearly but so long the conditions of uniform loading are valid. The power gain of the distributed amplifier (assuming lossless transmission lines) can be written as:

$$G = \frac{gm^2 Z_d Z_g N^2}{4} \tag{7}$$

Where Z_g, Z_d are gate and drain line characteristic impedances, respectively. In practical implementation the transmission lines cannot be devoid of losses. Actually, the loaded gate and drain transmission lines will have α_g and α_d as the real part of their propagation constants respectively. Although imaginary components do appear in the propagation constants, their contribution is negligible in the useful frequency range. Under phase synchronization condition of (5), the power gain of the amplifier is [22]:

$$G \approx \frac{gm^2 Z_d Z_g}{4}\left|\frac{e^{-N\gamma_g 1g_{-e}N\gamma_d 1_d}}{\alpha_g l_g - \alpha_d l_d}\right|^2 \tag{8}$$

Thus the gain does not increase monotonically with N and at a particular frequency. The optimum value of N is given by [22]:

$$N_{opt} = \frac{\ln\left(\frac{\alpha_d}{\alpha_g}\right)}{\alpha_d - \alpha_g} \tag{9}$$

Where α_g and α_d are the attenuation constants of gate and drain transmission lines respectively.

2.2.2 Noise in CMOS distributed amplifier

Thermal noise can be considered as induced gate noise and noise from the source/drain termination resistances. If flicker-noise and the noise from the parasitic resistances of the inductors are added to these sources, an expression for the noise figure is [23]:

$$F = 1 + \left(\frac{\sin n\beta}{n \sin \beta}\right)^2 + \frac{4}{n^2 g_m{}^2 R_{og} R_{od}} + \frac{R_{og} w^2 C_{gs}{}^2 \delta \sum_{r=1}^{n} f(r,\beta)}{n^2 g_m} + \\ + \frac{4\rho}{n g_m R_{og}} + \frac{KI_{ds}{}^a}{KT_o n C_{ox} R_{og} L_{eff}{}^2 \left(\frac{w}{2\pi}\right)^{ef} g_m{}^2} + \frac{R_{ig} \sum_{r+1}^{n+1} f(r,\beta)}{n^2 R_{og}} + \\ + \frac{4 r_{id}}{n g_m{}^2 R_{og} R_{od}{}^2} \qquad (10)$$

Where:

$$f(r,\beta) = (n - r + 1)^2 + \left(\frac{\sin(r-1)\beta}{\sin \beta}\right)^2 + \\ + \left(\frac{(2(n-r+1)\sin(r-1)\beta \cos \beta)}{\sin \beta}\right) \qquad (11)$$

$$R_{og} = \sqrt{\frac{L_g}{C_g}} \ , \ R_{od} = \sqrt{\frac{L_d}{C_d}} \qquad (12)$$

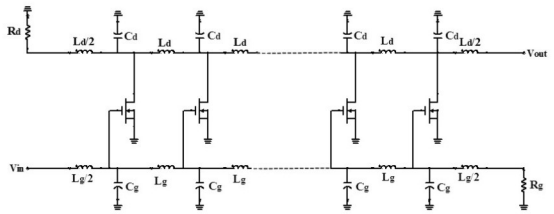

Figure 1: Conventional Distributed Amplifier structure

R_{ig} is the series resistance of the gate line inductors and R_{id} that of drain line inductors, T_o is the standard noise temperature for noise figure calculations (T_o = 290 K). K, a and e are parameters that characterize the flicker-noise, ρ and δ are parameters that characterize the thermal channel noise and the gate-induced noise respectively, and β is the progation constant of the artificial lines.

2.3 Variable gain distributed amplifier

Variable gain is a useful feature for the distributed amplifier, because it can be used along with baseband circuitry in an automatic gain control (AGC) loop. The AGC prevents large input signals from saturating the receiver front-end and amplifies small signals to above the detectable level. One of the important property of DA is possessing high gain and broadband matching simultaneously. A CDA with adjustable termination resistors [14] is the first reported VGDA in CMOS technology; however, the gain is less than 10 dB with a power consumption of 9 mW. a cascaded multi-stage distributed amplifier with variable-resistance metaloxide semiconductor field effect transistors (MOSFETs) [15] in 0.35 µm SiGeBiCMOS has been proposed to take the advantage of the multiplicative gain mechanism in order to reach high gain performance, but the variable gain structure is composed of the variable resistance NMOS using control voltage; hence it is not practical for low voltage and low power systems, to deal with this limitation, the PMOS variable resistor has been used in [16]. In the next section, a new topology of VGDA will be presented which has various advantages.

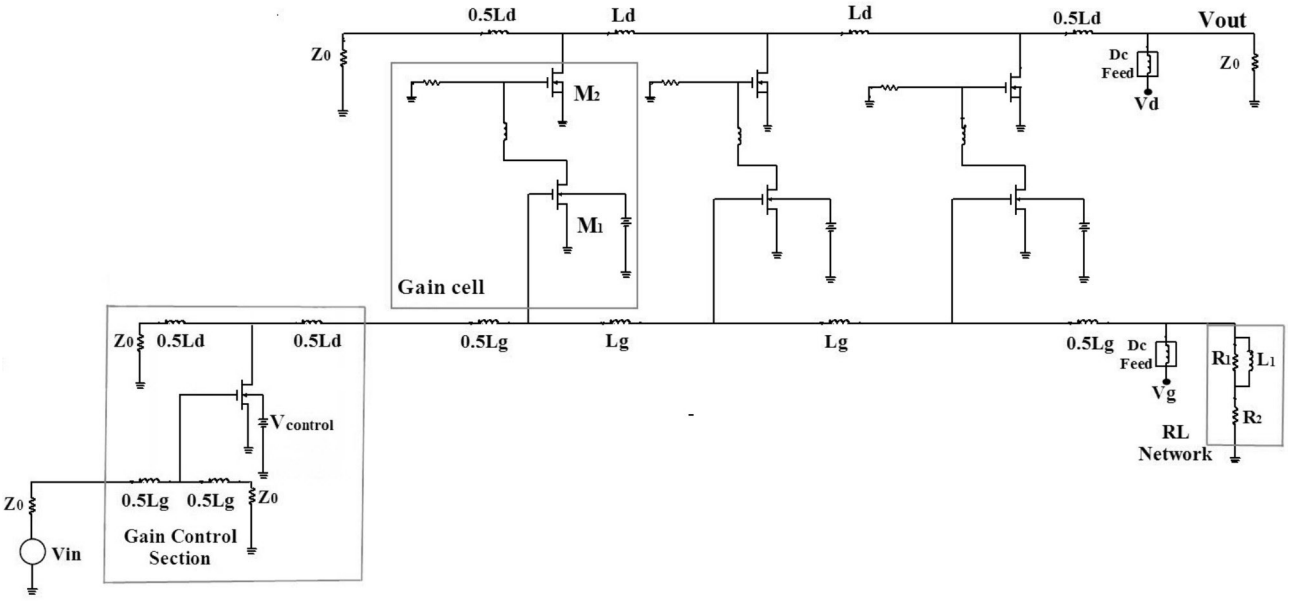

Figure 2: Schematic of proposed 3-stage variable gain distributed amplifier with new topology

3 Proposed variable gain distributed amplifier architecture

Figure 2 illustrates the proposed topology of variable gain distributed amplifier. First, the gain cells with new design will be discussed; then, one of the most effective parts of proposed VGDA circuit will be explained. This section is preamplifier, which is responsible for controlling the gain.

3.1 Gain cell architecture of proposed VGDA

Figure 3 shows the gain cell which is proposed in this paper. As mentioned in the previous sections, one of the influencing parameters on the gain is transconductance (gm). If it increases, the gain also increases. First, the study has focused on reason of optimizing bulk transistor (m_1) and then discusses about using inductor between two transistors in cascade structure, that result is transconductance increases and thereby, increase gain.

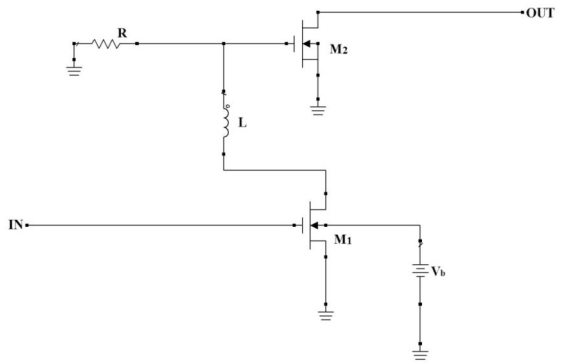

Figure 3: Proposed gain cell

The relation between bulk-source voltage, V_{BS}, and V_T is given as:

$$V_T = V_{To} + \gamma\sqrt{2\left|\varphi_f\right| + \left|V_{BS}\right|} - \gamma\sqrt{2\left|\varphi_f\right|} \tag{13}$$

Where: V_{BS}, V_{To}, γ and φ_f refer to: bulk source voltage, zero bias threshold voltage, bulk threshold parameter strong inversion surface potential, respectively. Equation (13) shows that the value of the threshold conductance voltage of the CMOS depends on the V_{BS} voltage. Figure 4 illustrates the small signal model of the CMOS transistor regarding the bulk effect.

m_1 transistor has two dependent current source. These source are "$g_m V_{gs}$" and "$g_{mb} V_{bs}$". They cause a relevant current with V_{gs} and V_{sb} voltages in drain terminal. In some circuits the source terminal is connected to the bulk in order to reject the effect of $g_{mb} V_{bs}$. The inducted current value toward the drain terminal by CMOS transistor given by:

$$g_m v_{gs} + g_{mb} v_{bs} \tag{14}$$

Where the v_{gs} and v_{bs} are input voltage of the gate source and bulk source capacitor, respectively. The transconductance relation of CMOS transistor given by:

$$g_m = \frac{\delta\, l_d}{\delta\, V_{GS}} = \psi\, v_{DS} \tag{15}$$

$$g_{mb} = \frac{\delta\, l_d}{\delta\, V_{BS}} = \frac{\psi\gamma v_{DS}}{2\left(2\left|\varphi\, f\right| + V_{BS}\right)^2} \tag{16}$$

Where:

$$\psi = \frac{(\mu_0\, c_{OX})W}{L} \tag{17}$$

equation (16) shows the dependency of g_{mb} value on bulk source voltage (V_{BS}) that the result is change in total g_m and thus changed gain by changing the bulk source voltage, this property has been used in this paper with optimal bias point on the bulk for maximum efficiency.

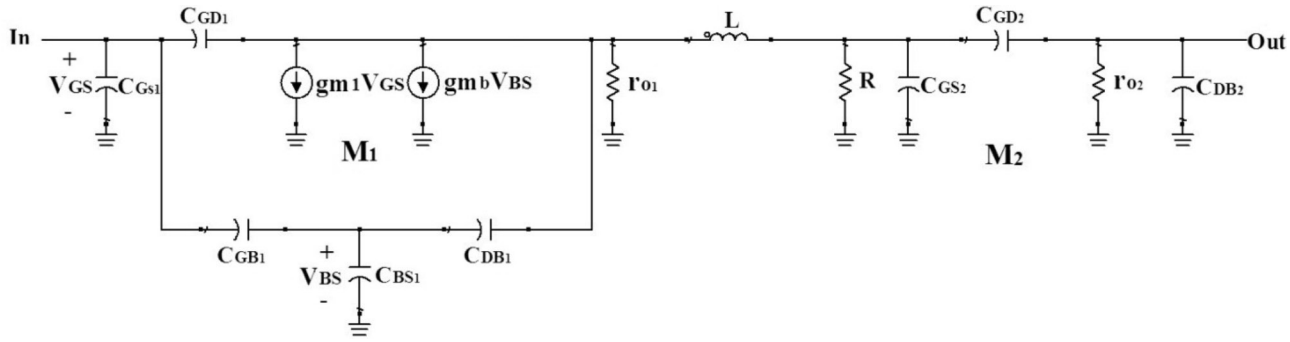

Figure 4: Small-signal equivalent circuit of the proposed VGDA gain cell

As can be seen in Figure 4, in the proposed design, an inductor is utilized between two transistors of cascade structure. According to the small signal equivalent circuit of gain cell (shown in Figure 5), C_{GS}, C_{DB} and C_{GD} are the respective gate to source, drain to bulk, and gate to drain capacitances of transistors, $r_{o(1,2)}$ are the output resistances of the transistors. Typically, $r_{o(1,2)}$ are relatively large and, therefore, can be neglected. Neglecting $r_{o(1,2)}$ and combining C_{GD1} with $C_{GB1,}$ C_{GS1} and C_{GD2} with C_{GB2}, C_{GS2} and also C_{DB1}, C_{DB2} with C_{BS1}, C_{BS2} formed C'_{GS1}, C'_{GS2}, C'_{DB1} and C'_{DB2}, respectively. We can derive the total transconductance of gain cell as:

$$G_m = \frac{\delta I_{out}}{\delta V_{in}} = g_{m1total} g_{m2} \frac{R \,\|\, \frac{1}{sC'_{GS2}} \frac{1}{SC'_{DB1}}}{\frac{1}{sC'_{DB1}} + sL + R \,\|\, \frac{1}{SC'_{GS2}}} =$$

$$= g_{m1total} g_{m2} \frac{R}{LC'_{DB1}C'_{GS2}Rs^3 + LC'_{DB1}s^2 + RC'_{DB1}s + RC'_{GS2}s + 1} \quad (18)$$

The concept of $g_{m1total}$ is related to g_m and g_{mb} of m_1. Usually, $C'_{GS2} >> C'_{DB1}$ and, thus, the total transconductance expression can be further simplified as:

$$G_m \approx g_{m1total} g_{m2} \frac{R}{LC'_{DB1}C'_{GS2}Rs^3 + LC'_{DB1}s^2 + RC'_{GS2}s + 1} =$$

$$= g_{m1total} g_{m2} \frac{R}{(LC'_{DB1}s^2 + 1)(RC'_{GS2}s + 1)} \quad (19)$$

From (19), three poles can be observed. One pole is formed by the input capacitor of the upper transistor. This pole normally dominates the low-frequency response due to the fact that the value of the gate-to-source capacitance of a transistor is usually large. The other two complex conjugate poles are created by the inductance and output capacitance of m_1. In practice, these two poles are located on the left s plane instead of exactly on the complex axis because of the loss incurred in real circuits. The presence of these two poles will boost up the transconductance of this gain cell at (20), which can also be considered as the cutoff frequency of the proposed gain cell transconductance.

$$f_c = \frac{1}{\sqrt{LC'_{DB1}}} \quad (20)$$

Where L and C'_{DB1} are the inductance used in gain cell and the new capacity of drain bulk which is obtained, respectively. In order to use the proposed distributed amplifier in reality, all losses were considered. The proposed gain cell has significantly higher transconductance, which provides a higher gain, as mentioned. Also, given that the gain cell has cascade structure, has better isolation. Another advantage is the input and output impedance matching well preserved, which helped to improve the stability of proposed DA.

3.2 Gain control section

In this VGDA, a preamplifier circuit is used. The main application of this section related to gain controlling. As can be seen in Figure 2, gain controlling is performed by changing bulk source voltage of preamplifier transistor. As discussed in the previous section, by changing the bulk source voltage of transistor, transconductance of transistor will change, that gain will be changed. This circuit has other effects on improving the performance of DAs. The first advantage occurs because signal is amplified before to injecting to the gate line which result in stronger signal arrives to the gain cell across the line, so the gain of DA has sharply increased. Another important advantage of this section is the significant reduction of noise.

Preamplifier is an amplifier which contains a transistor with low noise common source structure, the other section of the circuit is a distributed amplifier.

Therefore, the proposed topology can be assumed as a combined Amplifier as shown in Figure 5, which the first and second blocks are corresponds to the preamplifier and gain cell, respectively.

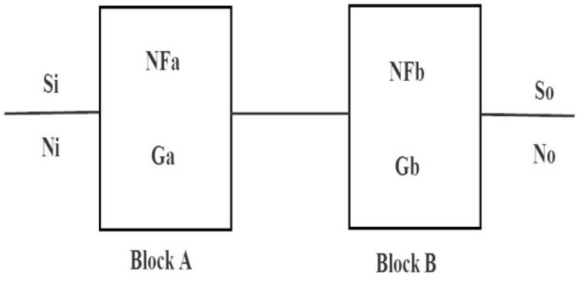

Figure 5: Block of composite amplifier

In this circuit, noise figure is equal to Equation 21:

$$NF = NF_a + \frac{NF_b - 1}{G_a} \quad (21)$$

Where NF_a and NF_b are the noise figure, G_a and G_b and are the gain of block a, and block b, S_i and S_o input and output signal, N_i and N_o input and output noise, respectively.

According to equation, (21) it can be concluded that if block a, which is part of the preamplifier, has high gain

and low noise, it makes total noise of the circuit to reduce. In addition, to further reduce noise, we used the proposed technique in [24], that instead of using single resistor, resistor and other circuit, consisting of resistor and inductor with parallel structure (RL network), have been used in the end of the gate line.

4 Simulation results

The characteristic impedance (Z_o) of both gate and drain lines is set 50Ω. Supply voltage of drain-source and gate-source of each cell is provided by voltage sources at gate and drain transmission lines, respectively. These voltages are considered less than 2V, Which makes the circuit to have low and good power consumption, The power consumption is only 61 mW.

In Figure 6, the flat gain response (S_{2_1}) of approximately 29.4 dB and cut-off frequency of 11.8 GHz in optimum control voltage, is shown. Figure 7 shows the gain control range of 39 dB, from -10 to +29 dB. As it can be seen in Figure 8 and 9, the input return loss (S_{1_1}) and the output return loss (S_{2_2}), respectively, both are better than 10 dB from 3.1 to 10.6 GHz in all of range, Figure 9 shows the reverse isolation (S_{1_2}) which is less than -45.8 dB across the bandwidth. The simulated noise figure (NF) of the variable gain distributed amplifier is shown in Figure 11. The average noise figure for optimum gain (29.4 dB) is around 2.93 dB within the band of interest. The simulations are carried out using "Advanced design system" (ADS) software [25].

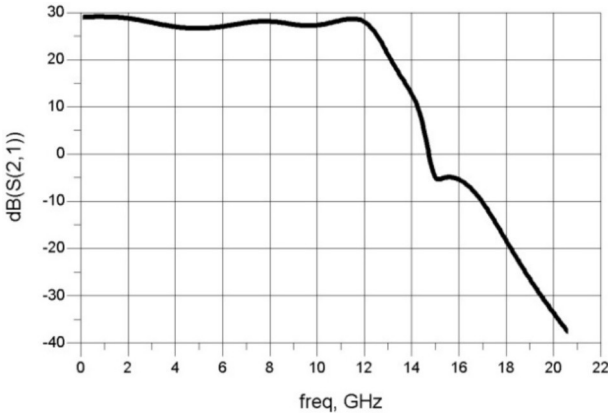

Figure6: Gain (S_{2_1}) of proposed VGDA

As yet, various DA and VGDA design methods are presented. Each of them improves one of the DA or VGDA design parameters. In result, a figure of merit (FOM) is defined to evaluate the power consumption together with the gain and bandwidth [23]:

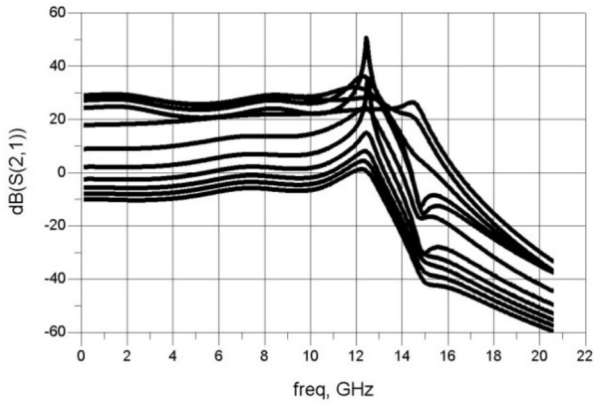

Figure 7: variable gain of proposed VGDA

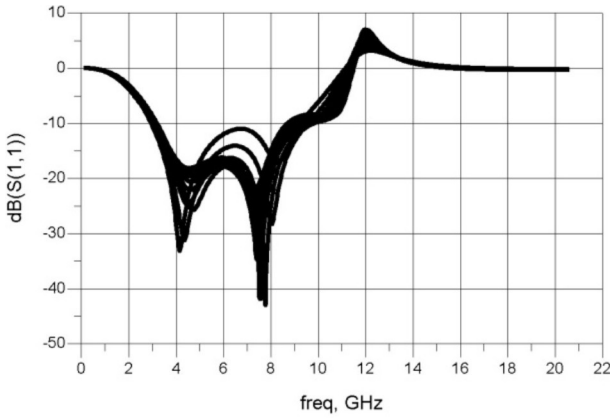

Figure 8: The input return loss

Figure 9: The output return loss

$$FOM\left[\frac{GHz}{mW}\right]=\frac{S_{2_1}[1]BW[GHz]}{(NF-1)[1]P_{DC}[mW]} \quad (22)$$

Where S_{2_2} [1] represents the average power gain in magnitude, BW[GHz] represents the -3dB bandwidth in GHz, (NF-1)[1] Represents the excess noise figure in magnitude, and P_{DC}[mW] represents power dissipation in milliwatts. This FOM includes the most relevant

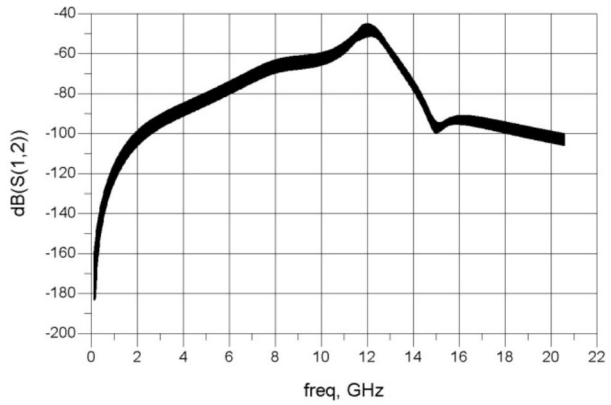

Figure 10: reverse isolation of proposed VGDA

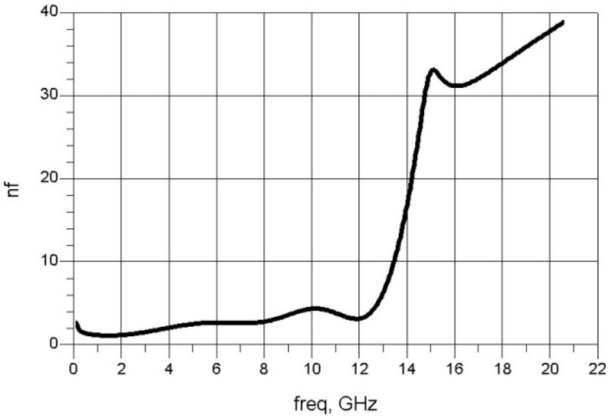

Figure 11: Noise figure for 29 dB gain of proposed VGDA

parameters for evaluating Das or VGDAs, for high gain, low-noise, low-power, and wideband applications.

Table I lists the performance figures of merit of recently published CMOS VGDAs along with those of this work, including bandwidth, gain in optimum mode, gain control range, noise figure, power consumption, and FOM. As shown, the proposed topology of VGDA exhibits the highest reported gain and FOM for CMOS VGDAs with high range of gain control in the UWB frequency.

5 Conclusions

In this paper, a novel topology which combines the preamplifier and new gain cell design with promoted cascade architecture has been proposed. Using this VGDA structure, all of the advantages of Architectures used in the new topology can be maintained. This topology can give considerations to high range gain control in ultra wide bandwidth, good impedance matching, low noise, and with reasonable dc power consumption. To authors' knowledge, this VGDA has the highest gain and FOM in 0.13 μm CMOS, and it has a comparable performance with other VGDAs in advanced processes. Moreover, this paper shows that the preamplifier circuit with new design of gain cell with optimum bias in bulk source can deliver higher gain, lower noise, and better power performance. The concept of proposed topology is demonstrated by VGDA with 3 stage (optimum stage) in a standard 0.13 μm CMOS process, and the simulated results agree with the circuit analysis well.

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Table 1: Performance summary and comparison with the published CMOS VGDA's

FOM	P_{dc} (mW)	AVG NF (dB)	GCR (dB)	Gain (dB)	Bandwidth (GHz)	topology	technology	Reference/ year
0.045	40	8.5	2.5 (0~2.5)	2.5	8.20 (0.8~9)	PGDA	CMOS 0.13 μm	[12] 2011
1.56	25	5.25	38 (-20~18)	18.1	11.4 (2.2~13.6)	VGDA	CMOS 0.18 μm	[16] 2011
2.34	7	5.95		12.5				
0.78	40	6.25	38 (-18~20)	20	10.5 (1.6~12.1)	VGDA	SiGe BiCMOS 0.35 μm	[15] 2006
2.028	6.4			12				
0.90	9	5.2	18 (-10~8)	8.6	6.97 (0.03~7)	VGDA	CMOS 0.18 μm	[13] 2006
3.78	61	2.93	39 (-10~29)	29.4	7.5 (3.1v10.5)	VGDA	CMOS 0.13 μm	This work

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