ASPECTS OF SUBMICRON BiCMOS TECHNOLOGY INTEGRATION

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Abstract: Despite tendencies that deep submicron CMOS technologies are replacing device solutions formerly realized in BiCMOS processes several applications for mixed signal digital analogue applications still require the performance of integrated BiCMOS processes. The issues of advanced process module integration (buried layers, trench isolation, self-aligned BJT and SiGe HBTs) into submicron BiCMOS processes will be covered with additional emphasis put on aspects arising from ASIC manufacturing.

Pogled na integracijo podmikronskih BiCMOS tehnologij

Ključne besede: polprevodniki, CMOS tehnologije, tehnologije submikronske, IC vezja integrirana, BICMOS tehnologije, MS signali mešani, moduli bipolarni osnovni, odnosi cenovni, trendi tehnologije, Si-Ge HBT transistorji bipolarni heterospojni, ASIC BiCMOS procesi, BJT transistorji s spojem bipolarnim, arhitekture transistorjev

Povzetek: Kljub željam, da bi podmikronske CMOS tehnologije nadomestile nekatere elektronske rešitve do pred kratkim izvedljive le v BiCMOS procesih, nekatere mešane, analogno-digitalne uporabe še vedno zahtevajo električne lastnosti, ki jih ponujajo samo integrirani BiCMOS procesi. V prispevku je obdelana integracija naprednih procesnih modulov, kot so pokopane plasti, izolacija s kanali, samonastavljivi BJT in SiGe HBT bipolarni tranzistorji, v podmikronske BiCMOS procese s stališča proizvodnje ASIC integriranih vezij.

1. Introduction

Although a bipolar transistor was the first semiconductor device demonstrated in 1947 by J. Bardeen, W. Shockley and W. Brattain, it was more or less the first realization of MOS technology in 1962, which lead the way to a worldwide growth of a semiconductor industry in the 1970s and 1980s. Due to the tremendous industrial impacts of silicon based semiconductor technology some people already address our current century as the „silicon age". The continuing advances in silicon integrated circuit technology have lead to today's VLSI and ULSI (very and ultra large scale integrated) circuits with up to several million transistors per single chip. The advantages of high density and low power consumption have made CMOS processes to the leading silicon fabrication technology. Although the implementation of both CMOS and bipolar structures on the same chip has already been demonstrated in the late 1960s /1/, the importance of BiCMOS processes emerged only in the late 1980s. The unavoidable drawbacks of the implementation like technology complexity and additional costs delayed its availability as a widely offered technology.

Two major facts have given rise to the BiCMOS technology in the last decade: growing demand for higher speed and better performance for analogue and mixed signal circuits and the reduction of some drawbacks related to BiCMOS processing, since the CMOS complexity has increased and many CMOS and bipolar process steps have converged.

The usage of BiCMOS process technology nowadays allows realization of mixed signal circuit applications 1-2 generations ahead of CMOS, unless high density digital functions set the requirements for dense chip layouts.

This article will give an overview of the basic bipolar modules used in submicron BiCMOS processes, their complexity and cost relations and an outlook to the next technology generations incorporating SiGe HBTs.

2. BiCMOS Technology for ASIC applications

Offering BiCMOS technology for mixed signal ASIC applications has to focus on the balancing between device performance and cost/complexity in manufacturing and design, as a broad range of applications for different customers has to be supported with design kits and simulation models. As BiCMOS gate array concepts can not really fulfill all requirements with respect to custom-specific mixes of bipolar and CMOS compo-

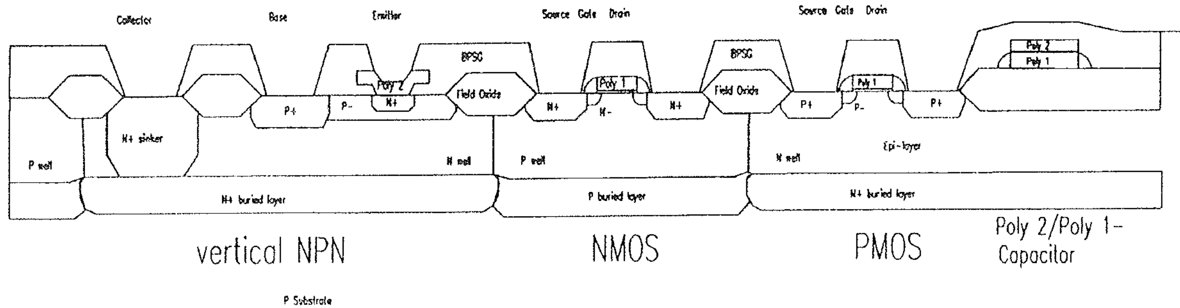

Fig. 1: Schematic cross-section of basic device elements implemented in a single poly BJT BiCMOS process /2/

nents together with resistors and capacitors the focus is put here on custom specific layout processing.

For an ASIC manufacturer not only the additional costs of highly integrated processes are of major interest, but also the associated increase of manufacturing times can be crucial with respect to fast turnaround cycles. Modular concepts for the introduction of additional process modules are envisaged to help decrease process complexity. It is even beneficial to try to reuse modules in different process technologies to keep a low number of complex process modules to be maintained. An optimum ASIC BiCMOS process will therefore try to fulfill most of the feasible applications, be as far as possible identical with the base CMOS processes and offer optional modules for special high performance functions.

2.1 Transistor architectures

2.1.1 Single poly BJT

Submicron BiCMOS processes typically incorporate buried layer architecture with a subsequent epitaxial Si-layer for formation of the twin well structure. This buried collector is contacted by a highly doped sinker to reduce the collector resistance required for high current drive applications. The BJT (bipolar junction transistor) of figure 1 is constructed by a single poly-Si layer used as emitter. In submicron processes the poly emitter module has emerged as the state of the art technology. Here the formation of the n^+ emitter contact is done by out-diffusion of Arsenic dopants from a poly-Si layer deposited in the emitter window over the base, thus allowing the formation of a very shallow emitter junction. Although there exist already sophisticated models for the poly emitter, which allow to predict the device characteristic and its various influences very well, the exact current gain mechanism is still not explained in every detail /3/.

In figure 1 the external base contacts are formed by P+ implants, usually done simultaneously with the P+ source/drain implant. The implementation of this type of bipolar transistor is commonly realized in BiCMOS processes from 1.2μm down to 0.6/0.5μm by the addition of only 3 - 4 extra masks to a double poly CMOS process (see also table 1). The performance of this architecture is limited to maximum transit frequencies F_T of 14 - 20 GHz.

For analogue applications f_{max} the maximum oscillation frequency is together with F_T an important figure of merit showing the transition performance. f_{max} is given by the simplified expression:

$$f_{max} = \sqrt{\frac{F_T}{8\pi R_B C_{JC}}} \quad (1)$$

Consequently, to improve process performance we need a high F_T value, a low base resistance R_b and a low base-collector capacitance C_{jc}.

Especially for analogue applications the limitations are often set by R_b and the parasitic C_{jc}. The base resistance is made up by the contributions from the extrinsic P+ contact, the intrinsic part between P+ and the emitter region and the pinched base resistance under the emitter. Closer spacing of P+ to emitter is usually limited by lithographic variations, while the bipolar base doping is limited by the device operational characteristic. The base doping and width has to be optimized for the bipolar parameters current gain β, electrical breakdown voltages and leakage currents and base resistance. As the extrinsic P+ is the main contribution for the parasitic base collector capacitance C_{jc}, double base contacts to each side of the emitter for lower R_b consequently increase the required area and the parasitic capacitance C_{jc}. Thus layout optimization is essential to achieve the optimum bipolar transistor performance.

An additional enhancement, which is widely incorporated, is the salicidation of the base areas and the emitter poly /4/. It reduces the sheet resistances to a few Ohm/□ and allows also denser designs e.g. by strapping the emitter contact outside the active area.

2.1.2 Double poly self-aligned BJT

The limitations of the single poly BJT with respect to the parasitic components can be improved by the implementation of a double poly self-aligned BJT (figure 3). The base area is here formed by P+ poly in direct contact with the substrate, while the poly emitter is self-aligned in between /4/. Further improvements of the high frequency performance can be achieved with optimization of the collector and buried layer doping /5/.

The advantages of the self-aligned architecture are clearly depicted by the small P+ areas thus achieving

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a reduction of the active area required for emitter and base of typically more than 50% for a double base contact bipolar transistor. Consequently the base collector capacitance C_{jc} is reduced together with the base resistance, as the P+ poly can be placed much closer to the emitter due to its self-aligned character. However, the critical part of this transistor architecture is the formation of the spacers and the integrity of the emitter area. This can lead to the use of three different composite layers (e.g. oxide, nitride, poly) for the spacer, if integration as a submicron BiCMOS process is envisaged.

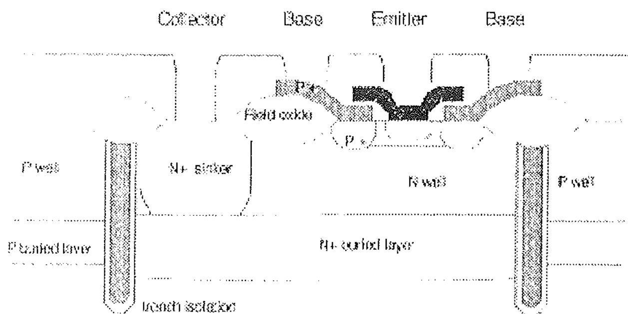

Fig. 2: Schematic cross-section of a double-poly self-aligned NPN BJT with additional poly/oxide filled trench isolation

Due to this complexity this process type is not widely offered in ASIC BiCMOS processes with geometries down to 0.6μm. However, for further scaling and the demand for higher performance this structure is mandatory in the submicron regime beyond.

Further improvements for the Si BJT focus on the base thickness and doping. Implanted and diffused base regions are limited in their width and achievable doping level due to defect enhanced Boron diffusion. Small base width and high doping must be balanced with the limitations often set by the electrical punchthrough characteristics and emitter/base leakage currents.

Further investigations have concentrated on epitaxial Si base deposition allowing a better boundary definition and higher base doping, but this approach limits the subsequent thermal budget for further process integration /6/. Although the implementation of epitaxial base structures has already demonstrated F_{TS} higher than 70 GHz, the complexity of such a module is a systematic drawback as SiGe heterojunction bipolar transistors (HBTs) can offer much higher performance with moderately additional process efforts.

2.1.3 Trench isolation

The collector to substrate capacitance C_{js} consists of the components N+ buried layer area to the low doped substrate and the much larger contribution from N+/P buried layer sidewall capacitance (see figure 2). The perimeter part is becoming more important with shrinking device geometries as the ratio of perimeter/area is increasing. Therefore trench isolation is of growing importance in high performance processes. A 0.8μm oxide/poly filled trench can decrease the perimeter capacitance down to 20 - 25 % compared to a non-trenched version. In addition the spacing of bipolar transistors can be shrinked more aggressively.

Although the trench isolation module involves from a designers point-of-view only the drawing of one more mask layer, in wafer manufacturing it stands for much more complexity. The trench formation requires a hard mask oxide, the trench mask, the etching of the oxide hard mask and the trench grooves, removal of the oxide, oxide or oxide/poly filling and planarization by plasma etching or CMP. Looking at this list of process steps it is obvious, why this module is often offered only as an optional module for BiCMOS process generations down to 0.8 - 0.5 μm.

Further reduction of Cjs can be achieved by the use of SOI, but this combination will in the next years still stay a niche market for certain applications unless the price of SOI base material will drop much more in the future /4/.

2.2 Si/SiGe HBTs

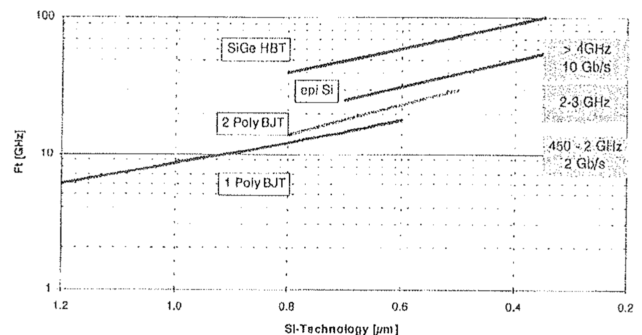

Fig. 3: Comparison of peak Ft performance of Si and SiGe bipolar transistor integrated in BiCMOS processes and their application ranges

As discussed above the restrictions of vertical scaling of emitter and base restrict Si BJTs in their practical cost-effective integration. Upper limits for Ft of 25 - 35 GHz are achieved, if processes which are available for a broader range of ASIC applications are considered.

Heterojunction bipolar transistors HBTs in silicon technology using SiGe base have emerged as a promising technology in the last decade investigated by several groups worldwide /6-10/. In contrary to a conventional silicon BJT, the epitaxial SiGe base HBT offers the possibility of decoupling current gain and low base resistance by independent adjustment of emitter and base doping. Although already very good frequency performances with F_T and f_{max} above 100 GHz have been achieved, the disadvantages of the HBT structure have so far delayed the integration in commercial HBT-BiCMOS processes. These limitations are caused by the mechanical stress in the pseudomorphic SiGe base

Table 1: Process flow examples of a BiCMOS and a post-CMOS HBT integration into a CMOS process

CMOS (1 P/2 M base process)	**BiCMOS**	**HBT-CMOS**	**optional modules**
	N+/P+ buried layer Epi Si deposition		
			Trench isolation
Twin well formation Active area definition LOCOS isolation MOS transistor implants Gate oxide / poly / etch N- /P- LDD Spacer formation	Twin well formation Active area definition LOCOS isolation Collector contact implant MOS transistor implants Gate oxide / poly / etch N- /P- LDD Spacer formation Bipolar base implant	Twin well formation Active area definition LOCOS isolation MOS transistor implants Gate oxide / poly / etch N- /P- LDD Spacer formation	
			Poly/poly capacitor
	Emitter opening Poly 2 deposition		
			High resistive implant
N+/P+ source/drain ILD deposition Contact maxk/etch TiN / W-plugs Metal 1 definition IMD 1/Planarization Via 1 mask/etch TiN / W plugs Metal 2 definition	Poly 2 mask/etch N+/P+ source/drain ILD deposition Contact mask/etch TiN / W-plugs Metal 1 definition IMD 1/Planarization Via 1 mask/etch TiN / W plugs Metal 2 definition	N+/P+ source/drain CMOS protection HBT area opening Collector implant / anneal Si/SiGe- epi deposition Emitter opening Emitter poly2 / etch P+ Base implant Mesa mask/etch Collector contact implant Spacer formation Salucidation ILD deposition Contact mask/etch TiN / W-plugs Metal 1 definition IMD 1/Planarization Via 1 mask/etch TiN / W plugs Metal 2 definition	
			IMD 2/ Planarization Via 2 mask/etch TiN / W plugs Metal 3definition
Passivation Pad mask/etch	Passivation Pad mask/etch	Passivation Pad mask/etch	

increasing with Ge content and SiGe layer thickness. This restricts the vertical Ge profile and the thermal budget must be kept low to avoid the relaxation and the Boron out-diffusion of the SiGe base. Despite the development work already performed and the fact that the epitaxial SiGe formation is already showing production worth repeatability /11/ is the availability as a commercial offered technology (e.g. for ASIC applications) still at its beginning. A practical hindrance with respect to industrial production seems also to be the additional effort for control of layer doping and gradient, as SIMS and X-ray analysis methods are not installed as frequent measurement tools in semiconductor production fabs today. However, with the repeated demonstration of better maturity of the deposition processes the control measurements could be reduced to reasonable efforts.

2.2.1 Epitaxial SiGe fabrication methods

From an industrial point-of-view out of the various methods applied to form the epitaxial SiGe (MBE, UHV-CVD and LPCVD) only the later two offer reasonable cost and throughput figures for implementation in a semiconductor fab. The type of epitaxial deposition (blanket, differ-

ential, selective) are more or less determining the yield and control issues associated with the procedure of integration into a CMOS process.

As the epitaxial SiGe base layer is grown on the collector tub in the silicon substrate any defect generated by the CMOS processing steps can potentially limit the yield by emitter pipe formation. This would suggest to implement the HBT part as early as possible into the CMOS process. However, as any out-diffusion of Boron or relaxation would deteriorate the HBT performance the subsequent processing steps are limited by a relatively low thermal budget /12/.

Another approach is a post CMOS implementation starting with the HBT part after the CMOS device formation. Such an approach will however only be successful, if the MOS LDD structures are capable of facing additional RTP-like steps. Practical employment seems therefore today limited to processes which are on one hand already based on RTP activation (typically in the submicron regime) and are not too sensitive to additional thermal treatment as observed beyond 0.5μm. Table 1 shows such an example of HBT integration into a CMOS process.

2.2.2 SiGe HBT performance considerations

The vertical doping profile of the bipolar transistor is dominating the high frequency performance both for a SiGe HBT as it is for a Si BJT. Purely by the incorporation of Ge into the base improvements in Ft from 30 to 49 GHz of bipolar transistors have been demonstrated /7/.

Major key figures of merit for the analogue and low power transistor performance can be improved in the SiGe HBT. The increased base doping allows a lower base resistance R_b to be obtained in SiGe than in Si for the same current gain β. Si/SiGe HBTs exhibit transition frequencies f_T and maximum oscillation frequencies f_{max} which are bout twice as large as in Si BJTs in combination with Early Voltages 5-6 times larger.

Device performance has been evaluated by a comparative simulation of representative BiCMOS applications in a 12 GHz 0.8μm BiCMOS process /2/ and a 45 GHz HBT process as available from IHP, Frankfurt/Oder /11/.

A VCO (voltage controlled oscillator) device for high output frequencies at low currents can typically realize up to 2.5 - 3.0 GHz at a current consumption of 5- 8 mA in the Si BJT process. If in this circuit HBTs replace the Si BJTs the device can either achieve frequencies up to 7.5 GHz for the same current levels or the current consumption can be reduced by 70 to 80% at 2.5 GHz.

On the other hand for applications like LNA (low noise amplifier) or mixers the parasitic transistor elements like base resistance and junction capacitances play a dominant role. In these cases the investigated SiGe HBT technology could not demonstrate dramatic performance improvement for the given set of SPICE parameters /13/. However, there are more technological opportunities to increase the base doping and therefore to reduce the base resistance in a SiGe HBT technology compared with Si BJT processes.

2.2.3 SiGe HBT integration

In a co-operation work with the Institute for Semiconductor Physics IHP Frankfurt/Oder and Austria Mikro Systeme International AG a SiGe HBT process has been demonstrated the first time to be capable of fabricating high performance SiGe HBTs after the completion of standard CMOS devices /11/.

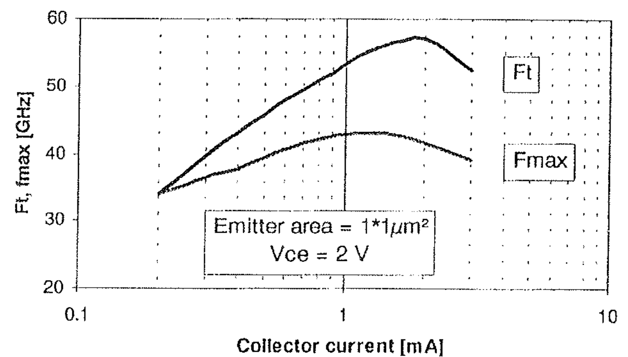

Fig. 4: HBT cut-off frequency ft and maximum oscillation frequency fmax vs. collector current

These post-CMOS integrated HBTs with 0.8μm design rules achieved f_T(f_{max}) values of up to 57(43) GHz (figure 4) without deteriorating the CMOS device parameters. Based on a 0.8μm ASIC-CMOS platform the MOSFET fabrication has been completed up to source and drain formation, and the wafers have been sealed with LTO-LPCVD oxide (table 1). The gate stack layers present on the areas reserved for the HBTs have been removed and a retrograde Phosphorus collector has been prepared in the normal CMOS well by implantation and appropriate annealing. A highly Boron doped SiGe base and a lightly doped Si emitter is then deposited by a single epitaxial RT-LPCVD step. The HBT base-collector mesa formation is continued by structuring, implantation and anneal for poly emitter and extrinsic base contact implants. Appropriate design of the base Ge profile and doping, and control of transient enhanced Boron diffusion due to the extrinsic base contact implant are of special importance to achieve the desired parameters /14/.

The emitter-pipe yield has been determined by leakage measurements of large emitter size macro HBTs with an emitter area of 10^4 μm^2 and has achieved average yields of greater than 80%.

This post-CMOS approach promises an relatively easy to implement HBT structure realizing performance figures typically achieved by special bipolar or BiCMOS processes with much more aggressive design rules.

2.3 Wafer processing costs

When balancing all technical advantages of new BiCMOS developments and their wafer processing complexity, the cost of additional manufacturing steps can also be an essential limitation, whether certain process versions can find their successful market seg-

ment. In the following a short investigation of costs correlated with process modules is given. However, it must be noted, that these calculations take only into account pure wafer processing costs consisting of operator costs, equipment costs determined by throughput and depreciation, facility utilization and material consumption. They do not contain yield issues, especially where new and advanced modules are investigated and yield models are not yet available due to lack of production data. Despite these restrictions, the figures for new process modules have been based on equivalent steps already available and thus represent realistic data gathered in an ASIC-manufacturing environment. Additionally it should be noted, that this data does not include electrical wafer test costs, as in advanced RF-analogue/digital wafer testing the testing costs can vary widely depending on the different application areas.

Table 2: Comparison of wafer processing costs for a 0.6μm CMOS process and implementation of bipolar process modules

0.6 μm CMOS 1P/2M	wafer processing cost
CMOS front end	52%
CMOS back end	48%
3. metal layer	+24%
18-20 GHz 2M BiCMOS (salicided)	+35%
add trench isolation to 2M BiCMOS	+17%
add 45 GHz HBT to 2M CMOS	+50%

Table 2 compares the costs related with the implementation of additional bipolar process modules into a 0.6μm CMOS process. Despite the use of advanced Al metal interconnect together with W-plugs and TiN layers, the basic CMOS front end costs account for 52% of the total wafer cost in manufacturing. Frontend of the process contains here all processing steps before the first inter level dielectric layer (e.g. BPSG). It is also interesting to see, that the cost for a trench isolation module is nearly in the range of an additional metal layer.

Due to a good merging of BiCMOS processing steps with the basic CMOS process the costs of a 18-20 GHz Si-BJT with salicided base and emitter and additional double poly capacitors (C= 1.8 fF/μm^2) can be kept at a level of +35%. Such a process allows applications of up to 2.5-3 GHz at a reasonable wafer price. However, the design margin might be narrow with respect to current consumption for certain low power applications in this frequency range (e.g. mobile telecom).

If the post-CMOS implementation of a HBT-module is considered (see table 1), the costs summarize up to additional +50% to the basic CMOS process. For the epitaxial SiGe step in this case the usage of a RT-LPCVD step has been assumed with a cost factor of 2.5x compared with standard Si-epi on a similar tool. For comparison, UHV-CVD tools promise already processing costs in the range of standard Si-epi-deposition.

Additionally it should be taken into account that the HBT integration realized here does not yet benefit from potential merging of deposition, etching or implant steps. We therefore strongly believe, that in the next future further optimization work can bring the additional cost for a HBT integration closer to the level of advanced Si BJTs, but will offer interesting opportunities for more advanced applications.

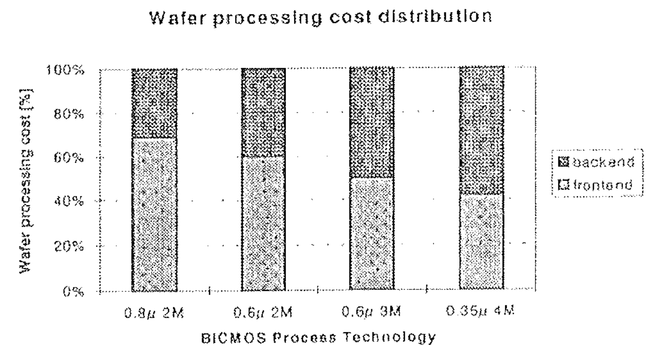

Fig. 5: Comparison of wafer cost distribution for front-end and backend processing of Si BJT BiCMOS processes for different technology generations

Figure 5 is comparing the partition of frontend and backend wafer processing costs. It is very obvious, that with the increasing complexity of the interconnect metal layers (e.g. TiN ARC layer, W-plugs, planarization) the cost of the backend in submicron processes is becoming the dominating factor. The data also indicates, that much higher complexity in the frontend process can be justified for future BiCMOS process generations without increasing the overall wafer cost uneconomically.

3. Conclusions

An overview of the common bipolar transistor architectures applied in submicron BiCMOS processes has been given with emphasis put on the correlated complexity of process integration for ASIC manufacturing.

A cost breakdown for BiCMOS modules has been presented and it has been illustrated that the additional costs incorporated with the integration of advanced frontend modules will become less important in future process technologies with smaller geometries due to the increasing costs associated with the growing number of interconnect layers.

The continuing research on Si and SiGe device and material physics and the availability of more advanced fabrication equipment have pushed the application of Si/SiGe based technology far in the regions, which were before considered of being only domains of III-V semi-

conductors. The superior device advantages of SiGe HBTs and the improvements in epitaxial processing towards production orientation will make the availability of HBT-CMOS more feasible in the near future.

Acknowledgments

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