ISSN 0352-9045

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials **Vol. 54, No. 1(2024), March 2024**

Revija za mikroelektroniko, elektronske sestavne dele in materiale **Ietnik 54, številka 1(2024), Marec 2024**



Informacije MIDEM 4-2023 Journal of Microelectronics, Electronic Components and Materials

VOLUME 54, NO. 1(189), LJUBLJANA, MARCH 2024 | LETNIK 54, NO. 1(189), LJUBLJANA, MAREC 2024

Published quarterly (March, June, September, December) by Society for Microelectronics, Electronic Components and Materials - MIDEM. Copyright © 2024. All rights reserved. | Revija izhaja trimesečno (marec, junij, september, december). Izdaja Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale – Društvo MIDEM. Copyright © 2024. Vse pravice pridržane.

Editor in Chief | Glavni in odgovorni urednik

Marko Topič, University of Ljubljana (UL), Faculty of Electrical Engineering, Slovenia

Editor of Electronic Edition | Urednik elektronske izdaje

Kristijan Brecl, UL, Faculty of Electrical Engineering, Slovenia

Associate Editors | Odgovorni področni uredniki

Vanja Ambrožič, UL, Faculty of Electrical Engineering, Slovenia Arpad Bürmen, UL, Faculty of Electrical Engineering, Slovenia Danjela Kuščer Hrovatín, Jožef Stefan Institute, Slovenia Matija Pirc, UL, Faculty of Electrical Engineering, Slovenia Franc Smole, UL, Faculty of Electrical Engineering, Slovenia Matjaž Vidmar, UL, Faculty of Electrical Engineering, Slovenia

Editorial Board | Uredniški odbor

Mohamed Akil, ESIEE PARIS, France Giuseppe Buja, University of Padova, Italy Gian-Franco Dalla Betta, University of Trento, Italy Martyn Fice, University College London, United Kingdom Ciprian Iliescu, Institute of Bioengineering and Nanotechnology, A*STAR, Singapore Marc Lethiecq, University of Tours, France Teresa Orlowska-Kowalska, Wroclaw University of Technology, Poland Luca Palmieri, University of Padova, Italy Goran Stojanović, University of Novi Sad, Serbia

International Advisory Board | Časopisni svet

Janez Trontelj, UL, Faculty of Electrical Engineering, Slovenia - Chairman Cor Claeys, IMEC, Leuven, Belgium Denis Đonlagić, University of Maribor, Faculty of Elec. Eng. and Computer Science, Slovenia Zvonko Fazarinc, CIS, Stanford University, Stanford, USA Leszek J. Golonka, Technical University Wroclaw, Wroclaw, Poland Jean-Marie Haussonne, EIC-LUSAC, Octeville, France Barbara Malič, Jožef Stefan Institute, Slovenia Miran Mozetič, Jožef Stefan Institute, Slovenia Stane Pejovnik, UL, Faculty of Chemistry and Chemical Technology, Slovenia Giorgio Pignatel, University of Perugia, Italy Giovanni Soncini, University of Trento, Trento, Italy Iztok Šorli, MIKROIKS d.o.o., Ljubljana, Slovenia Hong Wang, Xi´an Jiaotong University, China

Headquarters | Naslov uredništva

Uredništvo Informacije MIDEM MIDEM pri MIKROIKS Stegne 11, 1521 Ljubljana, Slovenia T. +386 (0)1 513 37 68 F. + 386 (0)1 513 37 71 E. info@midem-drustvo.si www.midem-drustvo.si

Annual subscription rate is 160 EUR, separate issue is 40 EUR. MIDEM members and Society sponsors receive current issues for free. Scientific Council for Technical Sciences of Slovenian Research Agency has recognized Informacije MIDEM as scientific Journal for microelectronics, electronic components and materials. Publishing of the Journal is cofinanced by Slovenian Research Agency and by Society sponsors. Scientific and professional papers published in the journal are indexed and abstracted in COBISS and INSPEC databases. The Journal is indexed by ISI® for Sci Search®, Research Alert® and Material Science Citation Index™. |

Letna naročnina je 160 EUR, cena posamezne številke pa 40 EUR. Člani in sponzorji MIDEM prejemajo posamezne številke brezplačno. Znanstveni svet za tehnične vede je podal pozitivno mnenje o reviji kot znanstveno-strokovni reviji za mikroelektroniko, elektronske sestavne dele in materiale. Izdajo revije sofinancirajo ARRS in sponzorji društva. Znanstveno-strokovne prispevke objavljene v Informacijah MIDEM zajemamo v podatkovne baze COBISS in INSPEC. Prispevke iz revije zajema ISI® v naslednje svoje produkte: Sci Search®, Research Alert® in Materials Science Citation Index™.

Design | Oblikovanje: Snežana Madić Lešnik; Printed by | tisk: Biro M, Ljubljana; Circulation | Naklada: 1000 issues | izvodov; Slovenia Taxe Percue | Poštnina plačana pri pošti 1102 Ljubljana

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials vol. 54, No. 1 (2024)

Content | Vsebina

Original scientific papers		Izvirni znanstveni članki
S. P. Philip, S. Palaniswami, E. Sekar, S. Ali K: Delay Efficient Cosine Modulated Reconfigurable Filter Bank for Digital Hearing Aids Targeting Noise Induced Hearing Loss	3	S. P. Philip, S. Palaniswami, E. Sekar, S. Ali K: Zakasnilno učinkovita arhitektura nastavljive filtrirne banke s kosinusno modulacijo za digitalne slušne pripomočke ob izgubi sluha zaradi hrupa
B. Repič, D. Belavič, D. Kuscer: The Effect of Firing Conditions on the Characteristics of Thick-film Resistors for Temperature Sensors	17	B. Repič, D. Belavič, D. Kuscer: Vpliv pogojev žganja na lastnosti debeloplastnih uporov za temperaturne
R. K. Tan, O. Mert, R. Mutlu: Examination of Resistive Switching Energy of Some Nonlinear Dopant Drift Memristor Models	25	R. K. Tan, O. Mert, R. Mutlu: Preučevanje upornostne preklopne energije nekaterih modelov memristorjev z nelinearnim odstopanjem dopanta
M. D. J. Dev, D. Judson: Hexagonal Convolutional Neural Network for Noma Rician Channel Estimator using Hexagonal Quadrature Amplitude Modulation	39	M. D. J. Dev, D. Judson: Šestkotno konvolucijsko nevronsko omrežje za ocenjevanje kanala Noma Rician z uporabo šestkotne kvadraturne amplitudne modulacije
K. Rangasamy: Fault Diagnosis of Asymmetric Cascaded Multilevel Inverter using Ensemble Machine Learning	51	K. Rangasamy: Diagnostika napak asimetričnega kaskadnega večnivojskega pretvornika z uporabo skupinskega strojnega učenja
H. Huo, W. Lü, X. Zheng, Y. Wang, S. Zhao: Analysis and Mitigation of Negative Differential Resistance Effects with Hetero-gate Dielectric Layer in Negative-capacitance Field-effect Transistors	65	H. Huo, W. Lü, X. Zheng, Y. Wang, S. Zhao: Analiza in ublažitev učinkov negativne diferencialne upornosti s hetero-vratno dielektrično plastjo v poljskih tranzistorjih z negativno kapacitivnostjo
Front page: Test samples of resistors and temperature sensors on alumina substrates processed by thick film technology (B. Repič et al.)		Naslovnica: Testni vzorci uporov in temperaturnih senzorjev na podlagi iz aluminijevega oksida, pripravljeni z debeloplastno tehnologijo (B. Repič et al.)

Editorial / Uvodnik

Dear reader,

Isn't it amazing how time flies? In the last year, our journal operations and processes ran smoothly and I am grateful to EB members, reviewers and technical support team for their valuable contribution to the success. All papers published are open-access and accessible in WoS, Scopus, DOAJ or on the journal web pages by a single mouse click. Do open-access papers help us in wider dissemination and larger readership? We are tracking the numbers and the trends look promising.

In 2023 we received more than 230 manuscripts, out of which only 20 have been accepted for publication so far, while 35 were out of scope and 94 manuscripts were rejected. The success rate remains low (below 20% in 2023) primarily because we receive many manuscripts that do not meet the quality and scientific originality that we aim at. Citation metrics for 2022 (published in June 2023) improved significantly – JCR IF-2022= 1.20, SNIP-2022=0.418 and CiteScore-2022=1.70. In 2023 we published 1 review scientific papers (on accurate positioning in wireless cellular networks) and 19 original scientific papers.

We commit ourselves to continue serving you as a part of your success in science and engineering and look forward to receiving your future manuscript(s) on our submission page (http://ojs.midem-drustvo.si/).

Be productive and efficient! Take care and stay healthy!

Prof. Marko Topič Editor-in-Chief

15 March 2024

https://doi.org/10.33180/InfMIDEM2024.101



Journal of Microelectronics, Electronic Components and Materials Vol. 54, No. 1(2024), 3 – 16

Delay Efficient Cosine Modulated Reconfigurable Filter Bank for Digital Hearing Aids Targeting Noise Induced Hearing Loss

Sajan P Philip¹, Sampath Palaniswami², Elango Sekar¹, Shoukath Ali K³

¹Department of Electronics and Communication Engineering, Bannari Amman Institute of Technology, Erode, Tamil Nadu, India

²Department of Electronics and Communication Engineering, Dr. N. G. P Institute of Technology, Coimbatore, India

³Department of Electronics and Communication Engineering, Presidency University, Bangalore, India

Abstract: In this paper, an efficient architecture for cosine modulated reconfigurable filter bank with sectional reconfigurability is proposed for Digital Hearing Aids targeting Noise Induced Hearing Loss. Polyphase implementation of the prototype filter with shared modulation coefficients reduces the computational complexity and increases the tuning flexibility. The proposed architecture can be used for frequency compensation of different classes of audiograms while keeping the group delay minimum. The proposed filter bank can provide 1296 various frequency band distribution schemes based on external control signals according to the nature of the audiogram. The architecture is based on a 16-band cosine modulated filter bank with dynamic merging of bands based on the audiogram. The flexibility of the filter bank allows matching most of the audiograms, including low or moderately-sloping SNHL and NIHL, with a notch at the center of the frequency range. For all the standard audiograms considered for evaluation, the proposed design has acceptable matching errors. The group delay is much less compared to existing reconfigurable filter banks, which provide room for accommodating other DSP algorithms in sophisticated Digital Hearing Aids. The hardware resources required for implementation are comparable with other reconfigurable filter banks designed for the same application.

Keywords: Filter bank, Cosine Modulated Filter Bank, Digital Hearing Aid, Delay Efficient Architecture

Zakasnilno učinkovita arhitektura nastavljive filtrirne banke s kosinusno modulacijo za digitalne slušne pripomočke ob izgubi sluha zaradi hrupa

Izvleček: V tem dokumentu je predlagana učinkovita arhitektura za nastavljivo filtrirno banko s kosinusno modulacijo z možnostjo sekcijske rekonfiguracije za digitalne slušne pripomočke ob izgubi sluha zaradi hrupa. Več fazno izvajanje prototipnega filtra s skupnimi modulacijskimi koeficienti zmanjšuje računsko zapletenost in povečuje prilagodljivost nastavljanja. Predlagano arhitekturo je mogoče uporabiti za frekvenčno kompenzacijo različnih razredov avdiogramov, pri čemer je skupinska zakasnitev minimalna. Predlagana banka filtrov lahko zagotovi 1296 različnih shem porazdelitev frekvenčnih pasov na podlagi zunanjih kontrolnih signalov glede na naravo avdiograma. Arhitektura temelji na 16-pasovnem kosinusno moduliranem filtru z dinamičnim združevanjem pasov na podlagi avdiograma. Prožnost banke filtrov omogoča prilagajanje večini avdiogramov, vključno z nizko ali zmerno nagnjenimi SNHL in NIHL, z zarezo na sredini frekvenčnega območja. Pri vseh standardnih avdiogramih, ki so bili upoštevani pri ocenjevanju, ima predlagana zasnova sprejemljive napake ujemanja. Skupinska zakasnitev je v primerjavi z obstoječimi nastavljivimi filtrirnimi bankami veliko manjša, kar zagotavlja prostor za namestitev drugih algoritmov DSP v zahtevnih digitalnih slušnih aparatih. Strojna sredstva, potrebna za izvedbo, so primerjiva z drugimi nastavljivimi filtrirnimi bankami, zasnovanimi za isto uporabo.

Ključne besede: filtrirna banka, kosinusna modulacija, digitalen slušni aparat, zakasnilno učinkovita arhitektura

 $* Corresponding \ Author's \ e-mail: \ sajanpphilip@gmail.com, \ sajanpphilip@bits \ athy.ac. in$

How to cite:

S. P Philip et al., "Delay Efficient Cosine Modulated Reconfigurable Filter Bank for Digital Hearing Aids targeting Noise Induced Hearing Loss", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 54, No. 1(2024), pp. 3–16

1 Introduction

According to recent research by the World Health Organization (WHO) [1], hearing-related health concerns are rising globally, including among younger generations. Digital Hearing Aids (DHA) are one of the prominent treatment options for Hearing Impairment (HI). Despite this, the usage of hearing aids is only at 17% globally, with low-income countries having limited access to DHAs. As a result, enhancing the effectiveness of DHAs is a crucial area of investigation that could improve their accessibility and value. Research towards incorporating sophisticated DSP algorithms in DHA for noise reduction, compression and intelligibility faces various challenges like increased chip area, delay, design complexity, and power consumption [2]. Similarly, the findings from audiology pose strict design constraints for DHAs [3].

Audiograms are graphs that show an individual's hearing threshold at different frequencies, measured in decibels (dB). Audiograms are used to determine the type of Hearing Impairment (HI) of a person. The audiologist measures a Patient's hearing thresholds against the frequencies between 250 Hz and 8000 Hz and marks it on a logarithmic graph, as seen in Figure 1. Hearing Impairment is broadly classified as Age-Related Hearing Impairment (ARHI), also known as presbycusis, and Noise-Induced Hearing Loss (NIHL) [4]. ARHI is considered the most common hearing disorder [5], leading to chronic disability in older age and is also referred to as Sensory Neural Hearing Loss (SNHL). On the other hand, NIHL primarily affects the working class, usually in factories with considerable noise and the young generation who habitually listen to music at high volume [6,7]. Low or moderate slopes in the lowfrequency regions of the audiogram characterize SNHL [8]. However, NIHL is characterized by frequency notching in the mid-frequency regions of the audiogram [9]. Two sample audiograms [10] demonstrating SNHL and NIHL are given in Figure 1.

The critical component in a DHA is the Filter Bank, which separates the individual frequency bands in the hearing spectrum for frequency compensation based on Hearing Loss. Hence, it is a straightforward approach to explore the possibilities of designing efficient filter banks to accommodate other DSP circuits in sophisticated DHAs. The DHA amplification characteristics are programmed by the hearing aid technician based on the audiogram measurements through a wired or wireless interface between the Computer and DHA. This process is known as audiogram matching. When the slope of the audiogram is more at a particular frequency region, a large number of narrow bands are required for error-free audiogram matching and frequency compensation. However, this may increase the computational complexity and group delay of the filter bank.

Traditional approaches like Frequency Response Masking (FRM) [11] focus on the design of a computationally efficient filter bank. However, it suffers from delay problems restricting its usage in advanced DHAs. In earlier works on Digital Audiology Technology [12], it is shown that compromise in the Linear Phase of the filter bank, up to a certain extent, is not sensible to the human ear. Based on this finding, various approaches to designing filter banks using modulation techniques have been explored. One of the popular methods is called the Cosine Modulated Filter Bank (CMFB) [13]. Over the years, the CMFB technique evolved as an attractive solution for filter banks in DHAs because of its real-valued coefficients, polyphase implementation possibilities, ease of design and less delay.



Figure 1: (a) SNHL Audiogram (b) NIHL Audiogram

Various works have been proposed in the literature to address low or moderately-sloping hearing Loss (Figure 1(a)) [3,11]. However, only a few works are available that address the notching NIHL audiograms (Figure 1(b)). There are two types of filter banks, namely fixed and reconfigurable filter banks. In the case of reconfigurable filter banks, the number of bands and band allocation frequencies can be flexibly adjusted based on the patient's audiogram. Fixed audiograms are generally used to correct hearing loss at low-frequency regions by allocating a greater number of bands. As NIHL is characterized by notches at center frequencies, flexible band allocation is essential. Thus, reconfigurable filter banks, which can correct the notched audiograms of NIHL by allocating a greater number of bands at center frequencies, are an important area of research.

Various studies show that [14] the Maximum Matching Error (MME) permissible for audiogram design is ±3dB, and it is required to allocate bands such that the MME is always within limits for the targeted audiograms. Otherwise, the user may feel uncomfortable at certain frequencies while using the DHAs due to unwanted amplification. An ideal filter bank must be able to provide tolerable MME while keeping the delay minimum [15]. The effectiveness and usability of DHAs also depend on the group delay of the device. The acceptable group delay for Closed Hearing Aid Fitting (CHAF) is up to 30 ms [16], and the same for Open Hearing Aid Fitting (OHAF) is 5 - 10 ms [17]. A higher Delay in OHAF devices results in a 'comb filtering effect,' and a higher delay in CHAF devices results in an 'occlusion effect.' The comb filtering effect is due to the superimposition of the actual and delayed sounds. Similarly, the occlusion effect is a perceived echo-like sound generated from one's voice. Even though studies claim that hearing-impaired people have higher group delay tolerance than ordinary people, a delay of more than 30 ms affects the audio-visual integration and results in 'lip reading.' Considering various studies [18], 10 ms group delay remains an unofficial standard among audiologists and hearing aid engineers [19].

This paper presents a reconfigurable CMFB architecture that provides a good trade-off between filtering complexity, implementational efficiency, design complexity, reconfigurability and group delay for DHAs targeting NIHL. The rest of the paper is organized as follows. Section 2 describes the conceptual and mathematical background of Cosine Modulated Filter Bank. Section 3 explores various articles from the literature addressing design approaches in reconfigurable filter banks for DHAs. The design and architecture of the proposed filter bank are detailed in Section 4. Results are presented in Section 5, followed by a thorough discussion in Section 6. Finally, a conclusion is drawn in Section 7.

2 Background

2.1 Choice of Cosine Modulated Filter Bank (CMFB)

CMFB falls under Modulated Filter Banks (MFB), which have many real-time applications in audio, video, transmultiplexers for communication, and biomedical signal processing [20]. MFBs are broadly classified as DFT filter banks and CMFBs. Modulating sequences are complex exponentials for the DFT filter bank and co-sinusoids for CMFB. The main attraction of CMFB compared to other filter bank approaches is that the signals can be decomposed into different bands using a single linear phase low pass Prototype filter. CMFB implementation is further classified as uniform filter banks (UFBs) and non-uniform filter banks (NUFBs) based on applications.

From a design perspective, CMFB can be classified as Perfect Reconstruction (PR) CMFB and Nearly Perfect Reconstruction (NPR) CMFB. NPR nature of the CMFB is due to its nonlinear phase property of sub-bands after modulation of the Prototype filters. Research findings show that PR is a desirable but not necessary condition for audio applications [21]. Hence, the NPR filter bank eases the complexity of implementation and provides more economical solutions for the implementation. Generally, the CMFB designs are based on FIR filters due to their guaranteed stability and reduced design complexity.

In most of the applications, uniform CMFB designs dominate. However, for applications like DHAs, it is required to use non-uniformly allocated reconfigurable band spacings. Non-uniform reconfigurable band allocation is preferable when the signal energy exhibits bandwidth-dependent distribution among frequency bands. Thus, it is important to explore the possibilities of designing non-uniform reconfigurable filter banks for DHAs using CMFB techniques. Only a few works [21-24] appear in this direction, especially as architectures for implementation in DHAs. For reconfigurable CMFB design, various approaches, namely, interpolation methods, merging bands methods, and transition band methods, can be adopted. This paper proposes the design of a non-uniform reconfigurable filter bank architecture using a merging method.

2.2 Mathematical background of CMFB

In a Modulated Filter Bank, let us assume that the filter coefficients $h_k(n)$ of k^{th} filter in the filter bank are generated through exponential modulation. ie,

$$h_{k}(n) = h_{0}(n)e^{j2\pi k/M}$$
(1)

where $h_0(n)$ is the filter coefficient of the Prototype filter. Now, it is required to design a new class of filter banks with real coefficients using the Cosine Modulation technique. This can be achieved by generating 2*M* complex filters using exponential modulation and linking the appropriate pairs of filter bands to create the sub-bands. Therefore, the prototype filter $P_0(z)$ is a lowpass filter with a cut-off frequency $\pi/2M$ as, shown in Figure 2.



Figure 2: Prototype Filter in MFB

Now, the polyphase components of $P_0(z)$ are $P_k(z)$, $0 \le k \le 2M - 1$. Thus, equation (2) gives the frequency responses of the polyphase components.

$$P_{k}(e^{j\omega}) = P_{0}\left(e^{j(\omega-\frac{k\pi}{M})}\right)$$
(2)

Where $P_k(e^{j\omega})$ are $k\pi / M$ shifted versions of the Prototype filter response as shown in Figure 3.



Figure 3: Magnitude Response of the Polyphase components in MFB

From Figure 3, it is evident that $P_k(e^{j\omega})$ and $P_{2Mk}(e^{j\omega})$ are images with respect to the zero frequency, so they can be combined to create the prototype filter with only real coefficients. When the images are combined using the method mentioned above, the pass band width of the combined filters will be $2\pi / M$, which is twice that of the Prototype Filter $P_0(z)$. Now, to make the filter bank suitable for amplitude compensation in DHAs, the initial prototype filter needs to be shifted by an amount of $2\pi / M$. Let us call the shifted version of the filters $Q_k(z)$. This is achieved by replacing z with $zW^{1/2}$ in the actual prototype filter $P_0(z)$ as given in Figure 4 and as per equation (3).

$$Q_k(z) = P_0(zW^{k+0.5}); 0 \le k \le 2M - 1$$
(3)

In the case of a uniform Cosine Modulated filter bank, the bandwidth of all the M filters is equal to π / M . An

equation that can be derived to compute the filter coefficients $h_k(n)$ of the Prototype filter $H_k(z)$ as given in equation (4).

$$h_{k}(n) = 2p_{0}(n)\cos\left[\frac{\pi / M(k+0.5)}{[n-N/2] + \theta_{k}}\right]$$
(4)

Where, $\theta_k = (-1)^k \frac{\pi}{4}, 0 \le k \le M - 1$ and N is the order of the Prototype filter. Figure 4 shows the magnitude response of an M channel non-uniform cosine modulated filter bank.



Figure 4: Magnitude Response of an M Channel Uniform CMFB

To match the logarithmic nature of the human auditory system, it is required to convert the above uniform CMFB filter bank to a Non-uniform CMFB filter bank for the actual implementation. The non-uniform filter bands are generated by merging the adjacent bands based on the narrow band and wide band requirements at different regions of the spectrum. Now, the transfer function of the resulting non-uniform CMFB filter is given by equation (5).

$$\tilde{H}_{i}(z) = \sum_{k=n_{i}}^{n_{i}+l_{i}-1} H_{k}(z)$$
(5)

Where, $i = 0, 1, 2, ..., \tilde{M} - 1$ and \tilde{M} is the number of bands in the non-uniform CMFB filter bank. In equation 5, I_i is the number of adjacent bands to be merged and n_i is the corresponding upper band edge frequency of the i^{th} band. The magnitude response of an \tilde{M} band nonuniform Cosine Modulated Filter Bank is given in Figure 5.



Figure 5: Magnitude Response of M Channel Non-uniform CMFB

3 Literature review

The Cosine Modulated Filter bank was originally derived from the Quadrature Mirror Filter Bank (QMF). The concept of QMF was later extended to create M Channel Filter Banks [25]. However, the exponential modulation in M Channel Filter banks results in complex filter coefficients. The CMFB is proposed to eliminate the complex filter coefficients [26]. Efficient polyphase implementation of uniform CMFB [27] using linear phase structure of the prototype filter has shown that the hardware savings are significant in such implementations when the ratio of the length of the filter to the number of filter bands is large. In Nearly Perfect Reconstruction (NPR) CMFB, the reconstruction criteria are relaxed to obtain efficient and faster polyphase implementations. The main objective of work related to NPR CMFB [28] is to design NPR CMFB exploiting the symmetry of the Linear Phase Prototype filter to reduce the number of multiplications in Polyphase implementation.

The design of non-uniform CMFB [10] from uniform filter banks by merging method gained the attention of researchers working in audio-related technology. It is shown [29,30] that such a strategy using interpolation techniques offers simpler designs and high stopband attenuation. Comparatively, a different approach [31] for designing non-uniform CMFB using a transition filter shows that non-uniform filter banks are designed from uniform filter banks by incorporating a transition filter to satisfy the aliasing cancellation conditions. However, individual filters need to be implemented for the non-uniform bands in this approach, which increases the computational complexity.

The first work reported [32] on the use of a CMFB filter bank for DHAs uses a uniform CMFB. In that work, it is shown how the typical design constraints for DHAs are achieved using appropriate filter bank types and efficient prototype filter design. Another important work [21] explaining the design of a non-uniform CMFB for DHA uses NPR non-uniform CMFB with a merging approach and transition filter approach. In this work, different FBs are designed for different audiograms and audiogram matching is performed. However, the architecture of the filter bank is not included in the work, and the design is non-reconfigurable for different audiograms. Hence, an efficient implementation strategy needs to be further explored for non-uniform Reconfigurable filter banks.

A reconfigurable filter bank design [22] based on CMFB published recently adopts a different approach compared to the above works. In this work, the prototype filter is Cosine Modulated, and then the sub-bands

are generated by the nonlinear transformation of the uniform sub-bands. However, the reconfigurability is limited as only four different frequency band decomposition schemes are available. The number of multipliers required is higher than the other methods, and linear phase characteristics are affected due to the introduction of nonlinear transformation of the uniform sub-bands. The literature review of the various articles shows a gap in efficient implementation strategies for non-uniform reconfigurable NPR CMFBs. Also, the value of the filter bank increases if the non-uniform filter bank design strategies can be extended to a reconfigurable filter bank, which may be programmed externally by the audiologist for different audiograms.

4 Proposed non-uniform reconfigurable CMFB

4.1 Architecture of the proposed reconfigurable nonuniform filter bank

Figure 6 shows the architecture of the proposed Reconfigurable filter bank. The main objective of the proposed reconfigurable filter bank is to provide narrow bands and wide bands at different frequency regions of the audiogram. The slope of the audiogram primarily determines the band-splitting scheme at a particular region. The passband width is narrow in regions with steep slopes and wider in areas with low slopes in audiograms. In the proposed architecture, the coefficients of narrower bands are merged to make wider bands, reducing the total multiplications required to implement the filter bank. Figure 7 shows the band allocation in the proposed filter bank. Since the sampling frequency considered for the design of DHAs is 16kHz, in Figure 7 corresponds to 8kHz and $\pi/4$ corresponds to 2kHz. The Proposed filter bank is a sectional reconfigurable filter bank. Here, the entire frequency range, or 8000 Hz, of the audiogram is divided into four equal sections. The width of each section is equal to $\pi/4$ or 2000 Hz in Figure 7. The sectional reconfigurability provides six different band-splitting schemes for each section, which the audiologist can select based on control signals, as given in Table 1. In the figure, the default 500Hz bands are named as C bands, 1000 Hz as B bands and 2000 Hz as A Bands. The D bands are 1000 Hz bands generated by merging the second and third bands at each section.

Band Split- ting Scheme	Select Line Logic $P_{3k-3}, P_{3k-2}, P_{3k-1}$	Sub band Distribu- tion	Switches to be turned ON
1	000	$\frac{\pi}{16}, \frac{\pi}{16}, \frac{\pi}{16}, \frac{\pi}{16}, \frac{\pi}{16}$	$S_{12k-11}, S_{12k-10}, S_{12k-9}, S_{12k-8}$
2	001	$\frac{\pi}{8}, \frac{\pi}{8}$	$S_{12k-7}, S_{12k-6}, S_{12k-3}, S_{12k-2}$
3	010	$\frac{\pi}{4}$	$S_{12k-7}, S_{12k-6}, S_{12k-3}, \ S_{12k-2}, S_{12k-1}, S_{12k}$
4	011	$\frac{\pi}{16}, \frac{\pi}{8}, \frac{\pi}{16}$	$S_{12k-11}, S_{12k-5}, S_{12k-4}, S_{12k-3}$
5	100	$\frac{\pi}{8}, \frac{\pi}{16}, \frac{\pi}{16}$	$S_{12k-7}, S_{12k-6}, S_{12k-9}, S_{12k-8}$
6	101	$\frac{\pi}{16}, \frac{\pi}{16}, \frac{\pi}{8}$	$S_{12k-11}, S_{12k-10}, S_{12k-3}, S_{12k-2}$

Table 1: Band Splitting Scheme and Select line logic fora Section

The fundamental idea of the proposed filter bank architecture is that it uses a parallel structure of a differently modulated FIR filter. The major components of the filter bank are the polyphase substructures of the Prototype filter marked as $A_0 - A_{16}$, the modulator blocks marked as $M_0 - M_{16}$ and the adder network. Initially, the real-valued modulation coefficients of the filter bank are stored in memory. The prototype filter coefficients and the modulation coefficients are given to the Modulator circuit as per the control signals to generate the required bands for a section.

Each modulator consists of 16 multipliers, as shown in Figure 6. The output from the modulator blocks is added inside the adder network to generate the required nonuniform bands. The adder networks 1 to 16 correspond to the 16 bands present in the filter bank. The routing of the adder network ensures that the modulated prototype filter coefficients are correctly rearranged to generate the required bands for a section. Finally, the gain



Figure 6: Architecture of the Proposed Non-Uniform Reconfigurable CMFB

of each band is varied according to the audiogram. The overall response of the filter bank is obtained by adding all the gain-adjusted sub-bands of all the sections.

The prototype filter of order 64 was first designed using the Blackman window method and implemented in a polyphase structure. This implementation requires only 32 multipliers because of the symmetry property of a Linear phase FIR filter. The choice of order 64 for the prototype filter is a trade-off between matching error and symmetry of the modulation coefficients. From the careful analysis carried out during the design phase, it is observed that maximum multiplier sharing is possible for the modulation coefficients when the order is 64, and the matching error for the targeted Audiograms is within the acceptable limits at order 64. Increasing the order does not significantly improve the matching error but increases the number of multipliers required for modulation coefficients. Decreasing the order of the filter affects the symmetry of the modulation coefficients and thus increases the number of multipliers and deteriorates the audiogram matching performance. The multipliers in the Modulator blocks may be dynamically turned ON or OFF based on the patient's Audiogram, which can reduce the power consumption of the Filter Bank. For example, if the patient has a relatively low slope audiogram, only a few multipliers will be activated in the modulator block, saving much power. Theoretically, the extreme and simplest band distribution consists of four bands and one band in each section, corresponding to 256 and 64 total multipliers for modulation. However, practical audiogram matching requires at least four bands in one or two sections, which requires almost 50% of the maximum multipliers to be turned ON. Through coefficient sharing and modulation coefficient symmetry, the total number of multipliers needed for the implementation of the proposed filter bank is 251.

The four sections in the proposed filter bank are reconfigured using three control signals each. Thus, the



Figure 7: Different Sections and corresponding band Schemes in the Proposed Reconfigurable Filter Bank

entire filter bank can be reconfigured according to the characteristics of the audiogram using only 12 external control signals. Let $P_{3k-3'}P_{3k-2'}P_{3k-1}$ be the selection lines of the k^{th} section. The combination of these select lines, according to the logic given in Table 2, is used to generate the activation signals $F_{12k-11} - F_{12k}$ for the switches $S_{12k-11} - S_{12k}$ that activate or deactivate the adders available in the Merging Circuit. Based on the switching control signals, the modulation coefficients of the proposed filter banks will be merged in the merging circuit to generate the bands for each section as per the schemes given in Table 1.

Table 2: Switch activation Logic for a Section in theProposed Reconfigurable Filter Bank

Switch Activation Signal	Logic for the 3-bit Select Lines of the <i>k</i> th section
F _{12k-11}	$\overline{P}_{3k-3}(P_{3k-2} \odot P_{3k-1}) + P_{3k-3}\overline{P}_{3k-2}P_{3k-1}$
F _{12k-10}	$\overline{P}_{3k-3}(P_{3k-2} \odot P_{3k-1})$
F _{12k-9}	$\overline{P}_{_{3k-2}}\overline{P}_{_{3k-1}}$
F _{12k-8}	$\overline{P}_{3k-3}P_{3k-2}P_{3k-1}+\overline{P}_{3k-2}\overline{P}_{3k-1}$
F _{12k-7}	$\overline{P}_{3k-3}(P_{3k-2}\oplus P_{3k-1})+P_{3k-3}\overline{P}_{3k-2}\overline{P}_{3k-1}$
F _{12k-6}	$\overline{P}_{3k-3}(P_{3k-2}\oplus P_{3k-1})+P_{3k-3}\overline{P}_{3k-2}\overline{P}_{3k-1}$
F _{12k-5}	$\overline{P}_{_{3k-3}}P_{_{3k-2}}P_{_{3k-1}}$
F _{12k-4}	$\overline{P}_{_{3k-3}}P_{_{3k-2}}P_{_{3k-1}}$
F _{12k-3}	$P_{3k-3}\overline{P}_{3k-2}P_{3k-1}+\overline{P}_{3k-3}P_{3k-2}$
F _{12k-2}	$P_{3k-3}\overline{P}_{3k-2}P_{3k-1} + \overline{P}_{3k-3}P_{3k-2}$
F _{12k-1}	$\overline{P}_{3k-3}P_{3k-2}\overline{P}_{3k-1}$
F _{12k}	$\overline{P}_{3k-3}P_{3k-2}\overline{P}_{3k-1}$

4.2 Design of the proposed non-uniform reconfigurable CMFB

Consider an M band uniform Cosine modulated Filter bank derived from a Prototype filter. The impulse response of k^{th} sub-band of the M band uniform Cosine Modulated Filter Bank is given by the following equation.

$$h_k(n) = 2p_0(n)\cos\left(\frac{\pi}{M}\left(n - \frac{N}{2}\right)(k - 0.5)\right)$$
(6)
$$; 1 \le k \le M$$

Where $p_0(n)$ is the impulse response of the prototype filter of order *N*. To design the uniform CMFB, the cut-

off frequency of the prototype filter must be equal to $\pi/2M$. From the above equation, the impulse response of k^{th} band of the band uniform CMFB can be written as follows.

$$h_k(n) = 2p_0(n)\cos\left(\frac{\pi}{16}\left(n - \frac{N}{2}\right)(k - 0.5)\right)$$
 (7)

In CMFB design, sub-bands of the filter bank are generated by modulating the Prototype filter coefficients with appropriate modulation coefficients. For example, in the above equation, the modulation coefficients of the 16-band uniform CMFB can be computed using the equation (8).

$$m(k,n) = 2\cos\left(\frac{\pi}{16}\left(n - \frac{N}{2}\right)(k - 0.5)\right) \tag{8}$$

These modulation coefficients are used to obtain the uniform bands of bandwidth 500Hz.

If the bands are implemented as direct filters modulated with the modulation coefficients, the computational resources required for the filter bank implementation will be enormous. Hence, in the proposed non-uniform reconfigurable filter bank, the prototype filter is implemented as the polyphase structure to exploit the redundancy in the modulation coefficients. From the modulation coefficient values for an even-order Prototype filter, the following patterns are observed for M =16, and this redundancy helps to implement the filter bank with optimum computational resources.

In the proposed design, the modulation coefficients for a 16-band uniform filter bank are symmetric with respect to $n = \frac{N}{2}$, $n = \frac{N}{4}$ and $n = \frac{3N}{4}$. This symmetry can be mathematically represented as given in equations (9) and (10).

$$m(k,n) = m(k,N-n); 1 \le k \le M, \ 0 \le n \le N$$
(9)

$$m(k,n) = \begin{cases} \left(-1\right)^{k} m\left(k,\frac{N}{2}-n\right), \ 0 \le n < \frac{N}{2} \\ \left(-1\right)^{k} m\left(k,\frac{3N}{2}-n\right), \ \frac{N}{2} < n \le N \end{cases}$$
(10)

This pattern observed in the modulation coefficients of the filter bank helps us to reduce the multiplier count by implementing the sub-filters as polyphase structures as per equation (11).

$$A_{g} = \begin{cases} E_{g}\left(z^{\frac{N}{2}}\right) + z^{N}p_{0}(N) & ;g = 0\\ E_{g}\left(z^{\frac{N}{2}}\right) + z^{-\left(\frac{N}{2} - 2g\right)}E_{\frac{N}{2} - g}\left(z^{\frac{N}{2}}\right) & ;1 \le g < N / 4 \\ E_{g}\left(z^{\frac{N}{2}}\right) & ;g = N / 4 \end{cases}$$
(11)

In equation (11), $E_g\left(z^{\frac{N}{2}}\right)$ represents the gth polyphase component of the prototype filter with $\frac{N}{2}$ stages.

Similarly, equations (12) and (13) give the polyphase components of the prototype filter.

$$E_{g}\left(z^{\frac{N}{2}}\right) = P_{0}\left(g\right) + z^{\frac{N}{2}}P_{0}\left(g + \frac{N}{2}\right)$$
(12)

$$E_{\frac{N}{2}-g}\left(z^{\frac{N}{2}}\right) = P_0\left(\frac{N}{2}-g\right) + z^{-\frac{N}{2}}P_0\left(N-g\right)$$
(13)

Thus, the polyphase components for the actual implementation can be denoted using equation (14).

$$A_{g} = P_{0}(g) + z^{-\frac{N}{2}} P_{0}\left(g + \frac{N}{2}\right) + z^{-\frac{(N-2)}{2}}\left(P_{0}\left(\frac{N}{2} - g\right) + z^{-\frac{N}{2}} P_{0}(N - g)\right)$$
(14)

where $P_o(g)$ is the g^{th} coefficient of the prototype filter.

Since FIR filter with even order and symmetric impulse response is used for implementation, the above equation can be modified as given in equation (15).



Figure 8: Implementation of the Sub filter component A_a

$$A_{g} = P_{0}(g) \left(1 + z^{-(N-2g)} \right)$$

+ $z^{-\left(\frac{N}{2} - 2g\right)} P_{0}\left(\frac{N}{2} - g\right) \left(1 + z^{-2g} \right)$ (15)

The architectural implementation of the polyphase component of the sub-filter A_a is illustrated in Figure 8.

Similarly, a pattern as given in equation (16) is observed for the modulation coefficients corresponding to 16 bands in the proposed filter bank when arranged into columns with the same indices.

$$\left|m(k,r)\right| = \left|m(k,17-r)\right| \tag{16}$$

This pattern also helps in reducing the number of multipliers required for the filter bank implementation by adopting the multiplier-sharing scheme between the sub-bands. The number of multipliers inside each block depends on the number of unique modulator coefficients required to create different bands for that polyphase component A_a of the Prototype filter.

Considering all the factors mentioned above, the number of multipliers required to implement modulator coefficients of a 16-band uniform filter bank is 219. Because of the symmetry in the filter coefficients, the number of multipliers needed to implement the prototype filter is 32. In total, 251 multipliers are required to implement the proposed non-uniform reconfigurable filter bank.

4.3 Delay analysis of the proposed non-uniform reconfigurable CMFB

The group delay of the proposed non-uniform Cosine Modulated Filter Bank is given by Equation (17).

$$t = \left\lfloor \frac{N-1}{2} \right\rfloor \frac{1}{f_s} = \left\lfloor \frac{65-1}{2} \right\rfloor \frac{1}{16 \times 10^{-3}} = 2ms \quad (17)$$

Where N is the length of the Prototype filter and f_s is the sampling frequency. The delay of the CMFB filter bank is much less compared to other types of filter banks. This is because the entire filter bank can be implemented using a single Prototype filter and efficiently implemented using the Polyphase structure by exploiting the redundancy in the modulation coefficients to shift the bands.

5 Experimental Results

The simulation results for the proposed Reconfigurable CMFB are shown in Figure 9. Unlike fixed filter banks, Reconfigurable CMFB must provide bands with different resolutions and band combinations for a particular region of the audiogram. That means sub-bands with



Figure 9: (a) C (b) B (c) A (d) D bands of the proposed non-uniform reconfigurable CMFB

different bandwidths are available throughout the frequency region for frequency compensation, and the audiologist may be able to merge or unmerge bands based on the characteristics of the audiogram. Figure 9 shows the different band resolutions available at different regions of the audiogram. Suppose an audiologist needs a narrow band in the middle region alone to compensate for the frequency notch; they can provide narrow bands in that region using external control signals for Section 2 or Section 3. Similarly, a steep slope can be compensated at high or low-frequency regions using narrow bands in Sections 1 and 4. A bands are enough for frequency compensation when the audiogram is almost linear with a lesser slope at all the frequency regions. Only six bands are required for frequency compensation of low or moderately-sloping audiograms, which reduces the computational resources used in the filter bank for a particular audiogram. The audiogram matching curve and audiogram matching error depicted in Figure 10 show that the proposed Reconfigurable filter bank can accommodate all kinds of audiograms, including low or moderately-sloping SNHL audiograms and NIHL audiograms. The audiogram matching performance of the proposed reconfigurable filter bank for Standard IEC 60118-15(IEC2012) audiograms and the FPGA synthesis results are given in Table 3 and Table 4, respectively. The Proposed architecture is synthesized using Zynq FPGA kits to evaluate parameters like computational resource utilization in terms of LUTs and delay in terms of logic delay. The proposed design is first converted to synthesizable Verilog code using the MATLAB HDL coder and synthesized using FPGA. The results of the proposed Reconfigurable CMFB are compared with a fixed non-uniform CMFB targeting NIHL. The results show that incorporating reconfigurability improves audiogram matching flexibility but comes with increases in computational overhead and logic delay compared to fixed CMFB.

6 Performance comparison and discussion

A detailed comparison of the Proposed Non-uniform Reconfigurable CMFB with other state-of-the-art filter banks for DHA is given in Table 5. The comparison is made with FRM [8,33-35], Farrow [36,37] and CMFBbased filter banks [21,22]. From the comparison results, it is observable that the matching performance of the Proposed filter banks is satisfactory for different kinds of real and standard audiograms. The proposed reconfigurable CMFB can flexibly match both SNHL and NIHL audiogram within the tolerable limits. The delay of the proposed filter banks is much less, making them suitable candidates for sophisticated DHAs, which provides



Figure 10: Matching performance of non-uniform and reconfigurable CMFB (a) & (b) Type 1 SNHL, (c) & (d) Type 2 SNHL, (e) & (f) Type 1 NIHL, (g) & (h) Type 2 NIHL

room for incorporating other complex DSP algorithms. The Computational resources required to implement the proposed filter banks are slightly higher than FRM methods and comparable with CMFB and Farrow methods. When architectural advantages and matching performance of the proposed filter bank are considered, it is arguable that the slight increase in the computational resources is reasonable for practical implementation. The existing fixed CMFB design [21] presents the merging method and transition filter methods. This work does not discuss the actual implementation of the filter bank, and it proposes the design of the filter bank by direct modulation of the individual bands. Also, this approach does not provide a common filter bank structure for different kinds of audiograms; instead, the design of a filter bank with different number of bands is proposed for different audiograms. This is not a practical approach, as different filter banks cannot be realized for different classes of audiograms. The matching performance of the existing work is presented with an arbitrary number of bands for different audiograms. However, the proposed filter banks offer a practically feasible implementation approach.

Table 3: Audiogram Matching performance of the proposed reconfigurable CMFB for standard IEC 60118-15(IEC2012) audiograms

Class of the	Name of the	Maximum Matching Error (MME) in dB				
Audiogram	Standard Audiogram	Fixed Non- Uniform CMFB	Recon- figurable CMFB			
	Very Mild	0.45	0.49			
Flat or Moderately Sloping Standard	Mild	0.62	0.67			
	Moderate	0.59	0.64			
	Moderate/ Severe	0.94	0.71			
Addiograms	Severe 1	2.31	0.93			
	Severe 2	2.23	0.97			
	Profound	2.67	1.28			
	Very Mild	3.21	2.38			
Steep Sloping	Mild	3.94	2.85			
Audiogram	Moderate/ Severe	4.23	2.73			

Table 4: FPGA Synthesis results of the proposed CMFB

 filter banks

Architoc	Zynq Evaluation and Development (ZED) FPGA (XC7Z020CLG484-1)								
ture	LUTs	IOBs	Total Delay (ns)	Logic Delay (ns)	Net Delay (ns)				
Non- uniform CMFB for NIHL	21756	208	279	262	17				
Proposed Recon- figurable CMFB	36987	282	454	420	34				

The existing reconfigurable CMFB approach [22] uses an indirect design approach. The Prototype filter is cosine modulated to generate uniform sub-bands, and these sub-bands undergo non-linear transformation to produce the required bands. Only four different band allocation schemes are available in the filter bank, which makes bands narrower in some regions and wider in other regions at the same time; hence, there is a dependency between different bands. The MME is beyond the tolerable limit for notched NIHL audiograms. Compared to this method, the proposed reconfigurable CMFB provides sectional independent reconfigurability in which the bands at one region do not affect the other region. For example, a narrow band can be simultaneously allocated for low and high-frequency regions, which is not available in the existing work. Also, the proposed Reconfigurable CMFB outperforms the existing Reconfigurable filter bank in matching performance.

When the matching performance of the proposed filter banks is compared with non-CMFB approaches like FRM and Farrow, the matching performance is comparable and within the tolerable limit. However, the delay performance of the proposed filter bank is the best among these methods. The delay of the existing CMFB reconfigurable filter bank [22] is higher than that of the proposed method as it uses the non-linear transformation architecture in the final stage of the filter bank. The only disadvantage of the proposed method compared to both the fixed and reconfigurable FRM approach is the slight increase in the computational resources. However, the delay performance, reconfigurability through external control signals and tolerable MME for all classes of audiograms, make it an attractive candidate for real-time implementation in modern DHAs.

The efficiency of the Proposed filter banks lies in the following aspects. Polyphase implementation of the reconfigurable CMFB keeps the computational resources within acceptable limits. Design of the entire filter bank using a Single Prototype filter reduces the design complexity. The efficient architecture of the modulator structure by exploiting the coefficient redundancy makes the filter bank realizable for practical DHA applications. The dynamic activation and deactivation of the modulator multipliers in the reconfigurable filter bank based on audiograms reduces the power consumption of the filter bank. Sectional reconfigurability provided to the reconfigurable filter bank enables tuning of the DHAs through the control signals independent of the frequency region. Merging the adjacent bands to generate wider bands reduces computational complexity.

7 Conclusions

This paper presents the architecture and design of a 16 bands sectional non-uniform reconfigurable filter bank based on the Cosine Modulation technique. The proposed reconfigurable CMFB is obtained by merging the modulation coefficients of 16 band uniform CMFB. Polyphase implementation of the Prototype filter and grouping of modulation coefficients reduced the computational resources required for the real-time implementation. The group delay of the filter bank is only 2ms, which enables it to be used in DHAs, which requires delay relaxation for the implementation of other advanced DSP algorithms. About 1296 different schemes may be obtained using this structure, making it an attractive solution for matching all classes of audiograms. It uses the merging method to generate reconfigurable sub-bands. Initially, the modulation coefficients are stored in a memory. The merging of modulation coefficients is carried out based on the external select line and is fed to multiplier blocks to generate the required bands. This helps the audiologist select wider or narrower bands for each region of the audiogram to reduce the matching error while performing frequency compensation. The unwanted multipliers may be disconnected in the modulator block to save power.

A maximum resolution of 500Hz can be obtained using this method. The number of multipliers required to implement this filter bank is 251, which is 34% higher than the existing reconfigurable CMFB approach. However, this method provides better matching performance for all classes of audiograms and has a very low group delay of 2 ms.

8 Conflict of Interest

The authors declare no conflicts of interest.

9 References

- 1. World Health Organization, World report on hearing, Geneva:2021, Licence: CC BY-NC-SA 3.0 IGOW.
- 2. Kim, Sang-Won & Kim, Minjoon & Kim, Jae-Seok. (2019). High-Performance DSP Platform for Digital Hearing Aid SoC with Flexible Noise Estimation. IET Circuits, Devices & Systems. 13. https://doi.org/10.1049/iet-cds.2018.5374
- Sajan P Philip, Sampath Palaniswami & Harikirub-3. ha Sivakumar 2020, 'A Computationally Efficient 11 Band Non-Uniform Filter Bank for Hearing Aids Targeting Moderately Sloping Sensorineural Hearing Loss', Informacije MIDEM - Journal of Microelectronics, Electronic Components and Materials, vol. 50, no. 3, pp. 153-167.
 - https://doi.org/10.33180/infmidem2020.301
- 4. Jos J. Eggermont, Chapter 2 - Epidemiology, Etiology and Genetics of Hearing Problems, Noise and the Brain, Academic Press, 2014, Pages 24-48. https://doi.org/10.1016/B978-0-12-415994-5.00002-6
- Panza F, Solfrizzi V, Seripa D, Imbimbo BP, Capozzo 5. R, Quaranta N, Pilotto A and Logroscino G, Age-

Table 5: Audiogram Matching Result Comparison of Various Filter Bank Techniques with Proposed NUCMFB and Reconfigurable CMFB

		Maximum Matching Error (MME) for Different Audiograms (in dB)							Compu- tational Re- source		Delay (ms)	
Filter bank Design Method	CMFB B	Type 1	Type 2	Type 3	Type 4	Type 5	Type 6	Type 7	Type 8	#Multipliers	#Adders	fs=16kHz
FRM 8 band (Optimized) [8]	Ν	0.83	2.11	14.13	9.64					18	36	12.8
Reconfigurable FRM 2 [33]	Ν	-	-	-	-	5.63	1.84	-	-	76	170	12.1
Reconfigurable FRM 4 [34]	Ν	1.49	2.54	2.72	-	-	-	1.49	-	84	196	18.75
Reconfigurable Farrow 1 [36]	Ν	2.45	1.67	-	-	-	2.11	-	-	216	432	1.1
Reconfigurable Farrow 2 [37]	Ν	2.60	1.51	2.96	-	2.0	1.61	-	-	138	276	1.3
FRM 16 band [35]	Ν	0.42	0.27	4.33	1.63	2.5	0.59	0.49	1.17	33	64	6
Fixed Non-Uniform CMFB (Merging) [21]	Υ	2.49	2.19	-	-	-	-	-	-	192	384	2
Fixed Non-Uniform CMFB (Transition) [21]	Υ	1.9	2.12	-	2.23	2.3	-	2.7	2.4	147	142	2
Reconfigurable CMFB [22]	Υ	-	1.65	-	-	3.75	1.35	-	-	187	156	7.77
Reconfigurable CMFB (Proposed)	Υ	1.95	0.69	3.18	2.85	2.57	1.95	2.28	1.88	251	274	2

related hearing impairment and frailty in Alzheimer's disease: interconnected associations and mechanisms. Front. Aging Neurosci. 2015 7:113. https://doi.org/10.3389/fnagi.2015.00113

- Mohammadizadeh M, Ahmadi SH, Sekhavati E, Ahani-Jegar K. Noise pollution effect in flour factory on workers' hearing in Lamerd City. J Med Life. 2015;8 (Spec Iss 3):208-211.
- 7. Dehankar SS, Gaurkar SS. Impact on Hearing Due to Prolonged Use of Audio Devices: A Literature Review. Cureus. 2022 Nov 12;14(11):e31425. https://doi.org/10.7759/cureus_
- Salmon MK, Brant J, Hohman MH, et al. Audiogram Interpretation. [Updated 2023 Mar [1]. In: StatPearls [Internet]. Treasure Island (FL): Stat-Pearls Publishing; 2023 Jan-. Available from: https://www.ncbi.nlm.nih.gov/books/NBK578179/
- 9. Agarwal G, Nagpure PS, Pal KS, Kaushal AK, Kumar M. Audiometric notching at 4 kHz: Good screening test for assessment of early onset of occupational hearing loss. Indian J Otol 2015;21:270-3
- 10. Earinfo 1996, Commonly used Auiograms. Earinfo.Com. http://www.earinfo.com/how-to-read-ahearing-aid-test/common-audiograms
- 11. Yong Lian & Ying Wei 2005, 'A computationally efficient nonuniform FIR digital filter bank for hearing aids', IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 52, no. 12, pp. 2754-2762. https://doi.org/10.1109/TCSI.2005.857871
- 12. Agnew J. The causes and effects of distortion and internal noise in hearing AIDS. Trends Amplif. 1998 Sep;3(3):82-118.
- https://doi.org/10.1177/108471389800300302
 13. Lee, Jeongjin & Lee, Byeong. (1995). A design of nonuniform cosine modulated filter banks. Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on. 42. 732 - 737. https://doi.org/10.1109/82.475253
- Woods, WS, Van Tasell, DJ, Rickert, ME & Trine, TD 2006, SII and fit-to-target analysis of compression system performance as a function of number of compression channels, International Journal of Audiology, vol. 45, no. 11, pp. 630-644. https://doi.org/10.1080/14992020600937188
- J. Agnew and J. M. Thornton, "Just Noticeable and Objectionable Group Delays in Digital Hearing Aids," Journal of the American Academy of Audiology, vol. 11, no. 06. Georg Thieme Verlag KG, pp. 330–336, Jun-2000.

https://doi.org/10.1055/s-0042-1748062

 Stone MA, Moore BC. Tolerable hearing-aid delays: IV. effects on subjective disturbance during speech production by hearing-impaired subjects. Ear Hear. 2005 Apr;26(2):225-35. https://doi.org/10.1097/00003446-200504000-00009. 17. Stone, Michael A., et al. "Tolerable Hearing Aid Delays.V. Estimation of Limits for Open Canal Fittings." Ear and Hearing, vol. 29, no. 4, 2008, pp. 601–617.

https://doi.org/10.1097/AUD.0b013e3181734ef2

 McGrath M and Summerfield Q. Intermodal timing relations and audiovisual speech recognition by normal-hearing adults. J Acoust Soc Amer 1985;77:678–85.

```
https://doi.org/10.1121/1.392336
```

- 19. Joshua Alexander, "Hearing Aid Delay and Current Drain in Modern Digital Devices", Canadian Audiologist, Vol. 6 , Issue 6, 2019. http://canadianaudiologist.ca/hearing-aid-delay-feature/
- 20. Yuan-Pei Lin and P. P. Vaidyanathan, "Application of DFT filter banks and cosine modulated filter banks in filtering," *Proceedings of APCCAS'94 - 1994 Asia Pacific Conference on Circuits and Systems*, Taipei, Taiwan, 1994, pp. 254-259 https://doi.org/10.1109/APCCAS.1994.514559
- Kalathil, S & Elias, E 2015, 'Efficient design of nonuniform cosine modulated filter banks for digital hearing aids', AEU - International Journal of Electronics and Communications, vol. 69, no. 9, pp. 1314-1320.

https://doi.org/10.1016/j.aeue.2015.05.015

- Huang, S, Tian, L, Ma, X & Wei, Y 2016, A Reconfigurable Sound Wave Decomposition Filterbank for Hearing Aids Based on Nonlinear Transformation, IEEE Transactions on Biomedical Circuits and Systems, vol. 10, no. 2, pp. 487-496. https://doi.org/10.1109/TBCAS.2015.2436916
- 23. Kumar, A, Sunkaria, RK & Dev Sharma, L 2018, Design of Cosine Modulated Non-uniform filter bank using Particle Swarm Optimization, 2018 5th International Conference on Signal Processing and Integrated Networks (SPIN), pp. 614-618. <u>https://doi.org/10.1109/SPIN.2018.8474056</u>
- 24. Vellaisamy, S & Elias, E 2018, Design of hardwareefficient digital hearing aids using non-uniform MDFvaT filter banks, Signal, Image and Video Processing, vol. 12, no. 8, pp. 1429-1436. https://doi.org/10.1007/s11760-017-1225-1
- 25. Vaidyanathan, P 1987, Quadrature mirror filter banks, M-band extensions and perfect-reconstruction techniques, IEEE ASSP Magazine, vol. 4, no. 3, pp. 4-20.

https://doi.org/10.1109/MASSP.1987.1165589

- 26. Koilpillai, RD & Vaidyanathan, PP 1992, Cosinemodulated FIR filter banks satisfying perfect reconstruction, IEEE Transactions on Signal Processing, vol. 40, no.4, pp. 770-783. https://doi.org/10.1109/78.127951
- 27. Xiqi Gao, Zhenya He & Xiang-Gen Xin 1999, Efficient implementation of arbitrary-length cosinemodulated filter bank, IEEE Transactions on Signal

Processing, vol. 47, no. 4, pp. 1188-1192. https://doi.org/10.1109/78.752623

- Bregovic, R, Yu, YJ, Viholainen, A & Lim, YC 2010, Implementation of Linear-Phase FIR Nearly Perfect Reconstruction Cosine-Modulated Filterbanks Utilizing the Coefficient Symmetry, IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 1, pp. 139-151. <u>https://doi.org/10.1109/TCSI.2009.2015599</u>
- 29. Ogale, J & Ashok, S 2011, Cosine Modulated Non-Uniform Filter Banks', Journal of Signal and Information Processing, vol. 02, no.03, pp. 10-19. https://doi.org/10.4236/jsip.2011.23024.
- Zijing, Z & Yun, Y 2007, A simple design method for nonuniform cosine modulated filter banks, IEEE 2007 International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications, MAPE, pp. 1052-1055.

https://doi.org/10.1109/MAPE.2007.4393448

- 31. Princen, J 1995, The design of nonuniform modulated filterbanks, IEEE Transactions on Signal Processing, vol. 43, no. 11, pp. 2550-2560. https://doi.org/10.1109/TFSA.1994.467351
- Lee, SJ, Kim, S & Yoo, HJ 2007, A Low Power Digital Signal Processor with Adaptive Band Activation for Digital Hearing Aid Chip, 2007 IEEE International Symposium on Circuits and Systems, pp. 2730-2733.

https://doi.org/10.1109/ISCAS.2007.378526

 Wei, Y & Wang, Y 2015, Design of Low Complexity Adjustable Filter Bank for Personalized Hearing Aid Solutions, IEEE/ACM Transactions on Audio, Speech, and Language Processing, vol. 23, no. 5, pp. 923-931.

https://doi.org/10.1109/TASLP.2015.2409774

- 34. Amir, A, TS, B & Elias, E 2018, Design and implementation of reconfigurable filter bank structure for low complexity hearing aids using 2-level sound wave decomposition, Biomedical Signal Processing and Control, vol. 43, no. 12, pp. 96-109. https://doi.org/10.1016/j.bspc.2018.02.020
- 35. Wei, Y, Ma, T, Ho, B K & Lian, Y 2019, The Design of Low-Power 16-Band Nonuniform Filter Bank for Hearing Aids, IEEE Transactions on Biomedical Circuits and Systems, vol. 13, no. 1, pp.112-123. https://doi.org/10.1109/TBCAS.2018.2888860
- Haridas, N & Elias, E 2016a, Efficient variable bandwidth filters for digital hearing aid using Farrow structure, Journal of Advanced Research, vol. 7, no. 2, pp 255-262. <u>https://doi.org/10.1016/j. jare.2015.06.002</u>

 Haridas, N & Elias, E 2016b, Design of reconfigurable low-complexity digital hearing aid using Farrow structure based variable bandwidth filters, Journal of Applied Research and Technology, vol. 14, no. 2, pp. 154-165.

https://doi.org/10.1016/j.jart.2016.03.005



Copyright © 2024 by the Authors. This is an open access article distributed under the Creative Com-

mons Attribution (CC BY) License (https://creativecommons.org/licenses/by/4.0/), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Arrived: 19. 09. 2023 Accepted: 21. 02. 2024 https://doi.org/10.33180/InfMIDEM2024.102



Journal of Microelectronics, Electronic Components and Materials Vol. 54, No. 1(2024), 17 – 24

The Effect of Firing Conditions on the Characteristics of Thick-film Resistors for Temperature Sensors

Barbara Repič^{1,2}, Darko Belavič¹, Danjela Kuscer^{1,2}

¹Electronic Ceramics Department, Jožef Stefan Institute, Ljubljana, Slovenia ²Jožef Stefan International Postgraduate School, Ljubljana, Slovenia

Abstract: An integrated miniature electrochemical sensor (ES) that offers rapid, sensitive, and selective detection of chemical and biological contaminants in a variety of samples requires temperature control to work accurately. To address this, one approach is to locate temperature sensor (TS) next to the ES components. However, this integration poses a challenge as different firing processes are required for the sensor components and the TS. Commercially available thick-film materials for the realisation of TS are designed for screen printing on alumina and firing in air at 850 °C for 10 minutes. However, a key component of an ES, a carbon-based working electrode, must be fired in an oxygen-lean atmosphere. In this study, we investigated the influence of the firing atmosphere, i.e., air and argon, on the characteristics of thick-film resistors, including thickness, roughness, phase composition, resistivity, and temperature dependence. For the study, we used two commercially available thick-film pastes, NTC2114 and NTC2113, as TS with nominal sheet resistivities of 10 k Ω /sq and 1 k Ω /sq at 25 °C, respectively. Using X-ray powder diffraction analyses, we detected RuO₂ and spinel phases in the samples heated at 850 °C in air. However, when the samples were fired in argon, we detect metallic ruthenium and alloys. As a result of these changes, the resistivity of the NTC2114 and NTC2113 increased significantly. However, despite these changes, the relative resistance and the coefficient of temperature sensitivity did not vary significantly, indicating the suitability of these materials as TS. These findings have important implications for the future integration of TS into various screen-printed ES systems, fostering the design and development of systems with enhanced accuracy and reliability in temperature measurements.

Keywords: NTC, thick film, screen printing, temperature sensors, phase composition

Vpliv pogojev žganja na lastnosti debeloplastnih uporov za temperaturne

Izvleček: Miniaturni integrirani elektrokemijski senzorji omogočajo hitro, občutljivo in selektivno zaznavanje kemijskih in bioloških onesnaževalcev v različnih vzorcih. Za pridobivanje zanesljivih in natančnih meritev pa je potrebno meriti in/ali kontrolirati temperaturo vzorca na samem mestu meritve. Najbolj primerna rešitev je integracija debeloplastnega senzorja temperature v elektrokemijski senzorski sistem. Integracija predstavlja izziv, saj so materiali za izdelavo senzorskih komponent in temperaturnega senzorja drugačni in zato zahtevajo različne postopke žganja. Komercialni debeloplastni materiali za izdelavo temperaturnega senzorja so razviti za sitotisk na inertno podlago iz aluminijevega oksida in za žganje pri temperaturi 850 °C na zraku. Ključna komponenta elektrokemijskega senzorja je delovna elektroda na osnovi ogljikovih materialov, ki zahteva žganje pri povišani temperaturi v atmosferi z nizko vsebnostjo kisika. V tej študiji smo proučevali vpliv atmosfere žganja debeloplastnih materialov, zrak in argon, na debelino, hrapavost, fazno sestavo, upornost in temperaturno odvisnost upornosti. Za študijo smo uporabili paste primerne za sitotisk NTC2114 z nazivno plastno upornostjo 10 k Ω /sq in NTC2113 z nazivno plastno upornostjo 1 k Ω /sq. Rezultati so pokazali, da je po žganju na zraku v plasteh prisoten RuO, in spinelna faza. V plasteh, žganih pri 850 °C v argonu, teh faz nismo zasledili, pač pa smo detektirali kovinski Ru in zlitine. Posledično se je upornost plasti NTC2114 in NTC2113 močno povečala: za faktor 5 pri NTC2114 in za faktor 19 pri NTC2113. Kljub tem spremembam pa se relativna upornost in koeficient temperaturne občutljivosti (β) vzorcev nista bistveno premenila, kar kaže na primernost teh materialov za izdelavo temperaturnih senzorjev. Te ugotovitve imajo pomembno vlogo za načrtovanje in razvoj integracije temperaturnih senzorjev v druge tipe elektrokemičnih sistemov. Prispevale bodo k razvoju takih sistemov, ki omogočajo bolj natančne in zanesljive meritve temperature.

Ključne besede: NTC, debele plasti, sitotisk, temperaturni senzor, fazna sestava

* Corresponding Author's e-mail: danjela.kuscer@ijs.si

How to cite:

B. Repič et al., "The Effect of Firing Conditions on the Characteristics of Thick-film Resistors for Temperature Sensors", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 54, No. 1(2024), pp. 17–24

1 Introduction

Electrochemical sensors are a powerful tool for the rapid, sensitive, and selective detection of different types of substances in a variety of samples. They are capable of detecting chemicals such as heavy metals, pesticides, antibiotics, and food additives as well as biological contaminants such as bacteria, viruses, fungi, and associated toxins in food, air, water, and soil. As a result, these sensors are used in various areas, e.g., for food quality control, monitoring environmental conditions, and promoting industrial safety [1,2].

The electrochemical detection methods involve the interaction between the target compound, i.e., the analyte, and the sensor surface, which leads to a redox reaction. This reaction produces a detectable signal, such as a change in current, potential or impedance, which is then measured and related to the qualitative and quantitative amount of the analyte. Temperature has a major influence on electrochemical measurements. It is therefore important to measure and control the temperature when carrying out electrochemical measurements [3]. The conventional measurement is performed in an electrochemical cell consisting of a working electrode (WE), a counter electrode (CE), and a reference electrode (RE) immersed in an analyte and connected to a potentiostat that controls the electrochemical potential and measures the resulting signals. However, due to technological advances these three electrodes can be integrated onto one substrate, which has led to the development of miniaturised, low-cost and portable electrochemical sensors (ES). They offer a practical solution for the detection of different classes of compounds, especially for non-professional users in remote locations, and are suitable for real-time sensing applications. One of the most commonly used integrated ES is the planar configuration, also known as screen-printed electrode (SPE). The name is derived from its manufacturing process in which thick-film materials, i.e., pastes, are deposited onto a ceramic substrate through screen-printing technology. This approach enables the production of functional, efficient and cost-effective ES with good performance characteristics [4,5].

In conventional thick-film technology, thick-film materials are applied to alumina in paste form using the screen-printing process. These deposited thick films are dried separately at a temperature of 150 °C and then fired at a peak temperature of between 800 °C and 900 °C in an air atmosphere. For the integrated ES, the processing must be adapted to the materials used for the electrodes. The RE and CE are usually made of metals such as platinum and silver, which can withstand these processing conditions. However, the WE is often made of carbon-based materials that require a different treatment. Carbon-based materials in particular need to be fired in an inert atmosphere. This requires the investigation of technological processes and the verification of technical properties to ensure a compatible process [6].

Since the electrochemical measurements, and thus the accuracy and reliability of ES, are strongly dependent on the temperature, it is of utmost importance to measure the temperature in the immediate vicinity of the WE where the redox reactions take place. This can be achieved by integrating an additional electronic component, i.e., a temperature sensor (TS), on the alumina substrate next to the electrodes. It is most appropriate if the TS is processed with a similar technology as the other sensor components, namely by screen printing and subsequent firing. The operating principle of the TS is based on the temperature-dependent resistivity of the thick-film material, which can have a negative temperature coefficient (NTC) or positive temperature coefficient (PTC) of the resistivity [7–11].

The resistance (R) of thick-film resistors are defined by their sheet resistance (R_{SH}), their length (I) and their width (w), whereby the R_{SH} depends on the resistivity (ρ) and the thickness (t) of the screen-printed and fired layer. All these relationships are shown in the Eq. (1).

$$R = \rho \times \frac{l}{t \times w}$$
 $R_{SH} = \frac{\rho}{t}$ $R = R_{SH} \times \frac{l}{w}$ (1)

Commercially available thick-film resistors usually consist of ruthenium oxide and/or bismuth ruthenate, and have a R_{SH} in decade values from 1 Ω /sq to 10 M Ω /sq. Therefore, by using materials with different R_{SH} and a different geometry of thick-film resistors, all desired different resistances can be achieved. The temperature coefficient of resistance (TCR) is described by Eq. (2), where R₁ is the resistance at temperature T₁ (usually T₁ is equal to 25 °C), and R₂ at T₂. The TCR values are below 100×10⁻⁶ K⁻¹ for most resistors [7].

$$R_2 = R_1 \Big[1 + TCR \big(T_2 - T_1 \big) \Big]$$
⁽²⁾

Specially designed thick-film resistor materials can be used as TS. These materials are designed with a high-temperature dependence of resistivity. There are several commercially available thick-film resistor materials with high PTC or NTC of the resistivity [12,13]. Most PTC resistors have a linear characteristic of resistivity as a function of temperature (Eq. (2)), while most NTC resistors have an exponential characteristic of resistance as a function of temperature (Eq. (3)), where β is the coefficient of temperature sensitivity.

$$R_{2} = R_{1}e^{\beta\left(\frac{1}{T_{1}} - \frac{1}{T_{2}}\right)}$$
(3)

Commercially available PTC thick-film resistors have a $R_{s_{H}}$ between 10 Ω /sq and 1000 Ω /sq, and values of TCR between 1000×10⁻⁶ K⁻¹ and 3000×10⁻⁶ K⁻¹. Commercially available NTC thick-film resistors have a R_{su} between 1 k Ω /sq and 100 k Ω /sq, and values of β between -2000 K and -4000 K. Therefore, NTC sensors are more sensitive, especially at low temperatures [8]. Since in our work we investigate a relatively low and narrow temperature range up to 100 °C and a target resistance between 1 k Ω and 10 k Ω , we decided to use NTC thickfilm resistors for the fabrication of TS. The NTC materials are based on the Mn-Ni-Co-O spinel phase with the addition of RuO₂ [10]. NTC pastes have been used for the realisation of temperature sensors on alumina and low temperature co-fired ceramic (LTCC) [14,15] and in microfluidic bioreactors made by multilayer LTCC technology [16].

NTC resistor has to be processed by similar technology as other sensor's components. NTC screen-printed pastes are commercially available and involve firing at a temperature of 850 °C in air atmosphere. However, the ES component, i.e., the carbon-based working electrode, requires firing in an oxygen-lean atmosphere. From our knowledge, no data is available on the processing of NTC's screen-printing pastes in such atmospheres. For compatibility purposes, the processing of NTC thick-film resistors in an oxygen-lean atmosphere needs to be studied.

In this work, we designed and processed an integrated TS using two commercially available NTC materials. The NTC pastes were screen-printed onto alumina substrate and fired at 850 °C at different conditions, namely in air for 10 min and 30 min, and in argon for 30 min. The study relates the firing conditions, thickness and phase composition of the thick-film structures to the performances of integrated sensors on an alumina substrate. The paper presents fabrication and characterization of the temperature sensors, highlighting their suitability for integration with screen-printed electrodes for electrochemical characterisation.

2 Materials and methods

2.1 Preparation of thick-film samples

Two thick-film thermistor pastes NTC2114 and NTC2113 (Ferro, King of Prussia, PA, USA) with a nominal R_{SH} of 10 k Ω /sq and 1 k Ω /sq, respectively, were used for processing temperature sensors. Thick-film resistor mate-

rial (2041, DuPont Wilmington, DE, USA) with a R_{SH} of 10 k Ω /sq was used as the reference thick-film component. It was selected because it is considered to be relatively insensitive to fluctuations in the production process and enables the production of a stable and high-quality thick-film resistor [7]. The electrical interconnections and contact pads were made from a silver-based thick-film conductor (9912MM, ESL, King of Prussia, PA, USA).

The materials were screen printed on an alumina substrate (Rubalit 708S, 96% Al_2O_3 , CeramTec, Plochingen, Germany) with the dimensions 24.0 mm \times 10.0 mm \times 0.5 mm using a screen printer (C1010, Aurel, Modigliana, Italy).

The thick-film resistors were deposited on an alumina substrate in the form of a square with dimensions of 8.0 mm x 8.0 mm for the structural investigation and of 1.1 mm x 1.1 mm with corresponding electrical interconnections for the electrical characterisations. Figure 1 shows the image of test samples, while the layout of the latter sample is shown elsewhere [17]. The screenprinted layers were dried in a dryer at 120 °C for 15 minutes and then fired under three different conditions:

- i) 850 °C for 10 minutes in air with a heating and cooling rate of 33 °C/min in a chamber furnace (PEO603, ATV Technologie, Vaterstetten, Germany). The thick-film samples from pastes 2113, 2114 and 2041 processed with this profile, are referred to as 2113-10/air, 2114-10/air and 2041-10/air, respectively.
- ii) 850 °C for 30 minutes in a flow of synthetic air. The samples were heated in a tube furnace at 450 °C for 1 hour at a heating rate of 2 °C/min and then heated at 850 °C for 30 minutes at a heating rate



Figure 1: The photo of the test samples with dimensions 8.0 mm x 8.0 mm (above) and 1.1. mm x 1.1 mm (below), where R stands for resistor, EI for electrical interconnection, CP for contact pad, and AO for alumina substrate.

of 5 °C/min. The samples were cooled to room temperature at a cooling rate of 5 °C/min. The thick-film samples from pastes 2113, 2114 and 2041 processed according to this profile, are denoted 2113-30/air, 2114-30/air and 2041-30/air.

iii) 850 °C for 30 minutes in a flow of argon. The samples were heated in a tube furnace at 450 °C for 1 hour at a heating rate of 2 °C/min and then heated at 850 °C for 30 minutes at a heating rate of 5 °C/min. The samples were cooled to room temperature at a cooling rate of 5 °C/min. The thick-film samples from pastes 2113, 2114 and 2041 that were processed with this profile, are designated 2113-30/Ar, 2114-30/Ar and 2041-30/Ar.

2.2 Characterisation

Test samples with dimensions 8.0 mm x 8.0 mm, fired for 30 min in air and Ar, were analysed in terms of thickness and phase composition. The thickness of the samples was measured by a contact stylus profilometer (Bruker DektakXT Advanced System, Karlsruhe, Germany). The X-ray powder diffraction (XRD) patterns of the samples were collected with a benchtop Powder X-Ray Diffractometer (MiniFlex 600-C, Rigaku). Diffraction patterns were collected at room temperature in the 20 range from 20° to 70° with a step of 0.02° and 0.24 s/step. The phases were identified using X'Pert HighScore Plus 2.1 (PANalytical) and the PDF-4 database (release 2019).

The NTC thick films and resistors with dimensions 1.1 mm x 1.1 mm, fired in air for 10 min and 30 min, and in Ar for 30 min, were characterized in an environmental chamber (VCL 7006, Voetsch Industrietechnik, Balingen-Frommern, Germany) at a constant relative humidity of about 40 % in the temperature range from -25 °C to 125 °C. The resistance of sensors and resistors was measured by a multimeter with multiplexed channels (2700, Keithley Instruments, Cleveland, Ohio, USA). The testing and measuring system was computer controlled including the acquisition of data. Resistances at 25 °C and calculated β , as key characteristics of temperature sensors, were evaluated for all samples.

3 Results and discussion

All thick-film samples fired in air and Ar for 30 min, measuring 8.0 mm x 8.0 mm, were about 30 μ m thick and had a surface roughness R_q of 1 μ m, regardless of the type of material and firing conditions.

XRD analysis of these samples (revealed that the samples have a high background characterised by an amorphous (glassy) phase. The amount of the glassy phase is highest in the thick film processed from 2114 paste, and lowest in 2041, regardless of the firing atmosphere. The background of the samples fired in air and argon is similar, indicating that the amount of amorphous phase for the selected sample does not vary significantly with the firing atmosphere (Figure 2, Figure 3 and Figure 4).



Figure 2: XRD patterns of a) 2113-30/air, and b) 2113-30/Ar. \blacklozenge : Ni-Mn-Co-O, \blacktriangle : alloys, \bigstar : RuO₂, +: Ru, **O**: Al₂O₃, **\square**: cubic SiO₂ and **\square**: orthorhombic SiO₂.



Figure 3: XRD patterns of a) 2114-30/air, and b) 2114-30/Ar. \blacklozenge : Ni-Mn-Co-O, \blacktriangle : alloys, \bigstar : RuO₂, +: Ru, **O**: Al₂O₃, **\square**: cubic SiO₂ and **\square**: orthorhombic SiO₂.

The phase composition of the 2113-30/air and 2114-30/ air is similar. In all the patterns we identify Ni-Mn-Co-O spinel phase (PDF 01-084-8364), RuO_2 (PDF 01-075-4303), alumina (PDF 01-075-6775) and cubic SiO₂ (PDF 01-080-4050). An additional peak at ~34 degrees is observed in 2114-30/air, characterised by orthorhombic SiO₂ (PDF 04-012-8095). The phase composition of the 2041-30/air is different than those of 2113-30/air and 2114-30/air. In the pattern we identify RuO₂ (PDF 01-075-4303), Bi₂Ru₂O₇ (PDF 04-013-7147), alumina (PDF 01-74-6775), hexagonal SiO₂ (PDF 01-078-1257) and PbO₂ (PDF 04-020-6664). The phase composition of the air-fired samples corresponds well to the composition, reported for NTC materials and resistors [7,13].



Figure 4: XRD patterns of a) 2041-30/air, and b) 2041-30/Ar. #: Bi₂Ru₂O₇, *****: Bi₂O₃, *****: RuO₂, **+**: Ru, **•**: PbO₂, *****: Pb₂O, **•**: Al₂O₃, **•**: cubic SiO₂ and **×**: hexagonal SiO₂.

The samples fired in argon atmosphere have very different phase composition compared to air-fired samples. In the pattern of 2113-30/Ar and 2114-30/Ar we have not identified any spinel phase, but metallic Ru (PDF 01-071-3766), and a phase that could correspond to alloys, such as Mn-Ni (PDF 04-003-2244) and Ni-Ru (PDF 03-065-4309), Co-Mn-O rock-salt structure (PDF 04-021-8068), alumina (PDF 01-75-6775), orthorhombic SiO₂ (PDF 04-012-8095), Mn₂SiO₄ (PDF 00-009-0485) and Ni,SiO, (PDF 04-014-7800). Although partial decomposition of Mn-Ni-O spinel upon heating at elevated temperature in air has been reported [19], our results showed that the spinel phase decomposed completely when the sample was heated to 850 °C in an argon atmosphere. The shift of diffraction peaks for rock-salt structure observed in 2113-30/Ar and 2114-30/Ar indicates, that its chemical composition in the two samples is different. In the 2041-30/Ar reference sample, we identify the characteristic peaks for Ru (PDF 01-071-3766), Pb₂O (PDF 00-002-0790), PbO₂ (PDF 04-020-6664), Bi₂O₂ (PDF 01-079-6675), as well as alumina (PDF 01-075-6775) and cubic SiO, (PDF 01-080-4050). These results clearly indicate that the spinel phase and RuO₂ decompose to metals and/or alloys when the thick-film resistors are fired in an argon at 850 °C. We expect that the resistivity of the argon-fired thick films will be very much different compared to air-fired samples, since the amount of RuO_2 and spinel phase dictate the resistivity of the NTC resistors [13,15–17].

Figure 5, Figure 6 and Figure 7 show the temperature dependences of the resistances and relative resistances for NTC2113, NTC2114 and 2041 after firing at 850 °C at



Figure 5: Resistances (a) and relative resistances (b) as a function of temperature for 2113-10/air (\times), 2113-30/ air (\bigcirc), 2113-30/Ar (\triangle).



Figure 6: Resistances (a) and relative resistances (b) as a function of temperature for 2114-10/air (\times), 2114-30/ air (\bigcirc), 2114-30/Ar (\triangle).

different conditions. The firing of the samples in air for 10 min and 30 min resulted in similar resistances while firing in an argon significantly increases the resistance of all the samples. The R_{SH} of NTC2114 and NTC2113 increased by a factor of 5 and 19, respectively, while for the resistor 2041 it increased by a factor of 3. These changes in R_{SH} can be attributed to the absence of RuO_2 and spinel phase. However, despite these changes, the relative resistance and the coefficient of temperature sensitivity (β) did not vary significantly. The temperature range of the electrochemical sensor operation lies between 10 °C and 70 °C. In this temperature range, the maximum resistance value is around 100 k Ω for the NTC2114 and around 60 k Ω for the NTC2113.



Figure 7: Resistances (a) and relative resistances (b) as a function of temperature for 2041-10/air (\times), 2041-30/ air (\bigcirc), 2041-30/Ar (\triangle).

Table 1 shows R_{SH} values measured at 25 °C, and β values calculated in the temperature range between 0 °C and 75 °C of the NTC2113, NTC2114 and 2041 resistors fired at different firing conditions.

The longer firing time in air has no significant influence on the R_{SH}. For samples fired for 10 and 30 minutes in air it varied for approximately +18 %, -17 % and -2 % for NTC2113, NTC2114 and 2041, respectively. On the other hand, firing in argon has a significant effect on R_{SH}. Compared to conventional firing in air for 10 minutes, the R_{SH} increased by factors of 19, 5 and 3 for NTC2113, NTC2114 and 2041, respectively.

The temperature dependence of the thick-film materials, expressed by the β , is relatively insensitive to the firing conditions. Compared to conventional firing conditions, 850 °C for 10 min in air, firing NTC2114 for 30

Table 1: Sheet resistivity (R_{SH}) at 25 °C and coefficients of temperature sensitivity (β) in the temperature range between 0 °C and 75 °C of NTC2113, NTC2114 and 2041 fired at different firing conditions.

Sample	R _{sH} at 25 °C [Ω/sq]	β calculated at 0/75 °C [K]
2113-10/air	2130	-1840
2113-30/air	2522	-2019
2113-30/Ar	40937	-2250
2114-10/air	13008	-2317
2114-30/air	10822	-2441
2114-30/Ar	64507	-2480
2041-10/air	10269	1
2041-30/air	10014	16
2041-30/Ar	34394	-7

minutes increases the β by about 5 % in air and about 7 % in argon. The longer firing time of the NTC2113 increases the β by about 10 % and about 22 % when fired in air and argon, respectively. The thick-film resistor material 2041, which is used as a reference material, show a resistivity-independent temperature dependence.

The air and Ar-fired NTC thick films have similar values of relative resistance and β , which makes them suitable for use as temperature sensors. However, when considering temperature-dependent resistivity and R_{SH}, the NTC2113 is a more appropriate material for processing temperature sensor, particularly due to easier signal conditioning.

4 Conclusions

A miniature electrochemical sensor (EC) needs temperature control for accurate operation, and one possible approach is to position temperature sensors near the EC. The EC component, the C-based working electrode, requires firing in an oxygen-lean environment, while temperature sensors are fired in air. In this study, we explored the processing of commercially available thickfilm resistors, NTC2113, NTC2114, and resistor 2041, deposited on alumina substrates using screen-printing method and firing at 850 °C in air for 10 and 30 min and argon for 30 min. Obtained thick films were 30 µm thick with 1 µm surface roughness, regardless of the firing conditions, confirmed by profilometry. X-ray powder diffraction analysis showed that the films contained an amorphous phase, and its quantity did not vary significantly in air and argon for the selected samples. NTC thick films fired in air contained RuO₂, Ni-Mn-Co-O spinel phase, and minor phases, alumina, and SiO₂. The reference resistor contained RuO, and bismuth ruthenate as major phases, together with lead oxide, alumina, and SiO₂. We found out that argon-fired samples did not exhibit RuO₂, spinel phase, or bismuth ruthenate, but rather metallic ruthenium and alloys. Consequently, the resistivity of the argon-fired samples was significantly higher compared to the air-fired samples. For materials fired in argon, the R_{SH} increased by a factor of 19 and 5 for NTC2113 and NTC2114, respectively. Additionally, the R_{SH} of the reference resistor increased by a factor of 3. The relative resistances and β for NTC materials were relatively unaffected by the firing atmosphere. Therefore, NTC materials show potential for use as temperature sensors. Among them, NTC2113, with its lower R_{SH} is a more suitable material due to easier signal conditioning.

5 Acknowledgement

This work was supported by the Slovenian Research and Innovation Agency, grant numbers P2-0105, J2-3049 and PR-11483.

We thank Ivana Goričan for recording X-ray powder diffraction patterns and Mitja Jerlah for screen-printing of selected test samples.

6 References

- T. N. Diep Trinh, K. T. L. Trinh, and N. Y. Lee, 'Microfluidic advances in food safety control', *Food Research International*, vol. 176, p. 113799, Jan. 2024, <u>https://doi.org/10.1016/j.foodres.2023.113799</u>.
- A. Smart, A. Crew, R. Pemberton, G. Hughes, O. Doran, and J. P. Hart, 'Screen-printed carbon based biosensors and their applications in agrifood safety', *TrAC Trends in Analytical Chemistry*, vol. 127, p. 115898, Jun. 2020, <u>https://doi.org/10.1016/j.trac.2020.115898</u>.
- 3. R. G. Compton and C. E. Banks, *Understanding Voltammetry (Third Edition)*. World Scientific, 2018.
- M. Li, Y.-T. Li, D.-W. Li, and Y.-T. Long, 'Recent developments and applications of screen-printed electrodes in environmental assays—A review,' *Analytica Chimica Acta*, vol. 734, pp. 31–44, Jul. 2012, <u>https://doi.org/10.1016/j.aca.2012.05.018</u>.
- G. Liang *et al.*, 'Development of the screen-printed electrodes: A mini review on the application for pesticide detection', *Environmental Technology* & *Innovation*, vol. 28, p. 102922, Nov. 2022, https://doi.org/10.1016/j.eti.2022.102922.
- M. Prudenziati, 'Thick-film technology', Sensors and Actuators A: Physical, vol. 25, no. 1, pp. 227– 234, Oct. 1990, https://doi.org/10.1016/0924-4247(90)87036-I.

- M. Hrovat, Z. Samardzija, J. Holc, and D. Belavic, 'Microstructural, XRD and electrical characterization of some thick film resistors', *Journal of Materials Science: Materials in Electronics*, vol. 11, no. 3, pp. 199–208, Apr. 2000, https://doi.org/10.1023/A:1008988614598.
- M. Hrovat, D. Belavič, J. Kita, J. Cilenšek, L. Golonka, and A. Dziedzic, 'Thick-film temperature sensors on alumina and LTCC substrates', *Journal of the European Ceramic Society*, vol. 25, no. 15, pp. 3443–3450, Oct. 2005,

https://doi.org/10.1016/j.jeurceramsoc.2004.09.027.

9. A. Dziedzic, L. J. Golonka, J. Kozlowski, B. W. Licznerski, and K. Nitsch, 'Thick-film resistive temperature sensors', *Meas. Sci. Technol.*, vol. 8, no. 1, p. 78, Jan. 1997,

https://doi.org/10.1088/0957-0233/8/1/011.

- S. Jagtap, S. Rane, U. Mulik, and D. Amalnerkar, 'Thick film NTC thermistor for wide range of temperature sensing', *Microelectronics International*, vol. 24, no. 2, pp. 7–13, Jan. 2007, <u>https://doi.org/10.1108/13565360710745539</u>.

https://doi.org/10.2298/FUEE1703267A.

- L. M. Sola-Laguna, P. J. Moffett, J. R. Larry, and J. Hormadaly, 'Thick film NTC thermistor series for sensor and temperature compensation application: Proceedings of the 1998 International Symposium on Microelectronics', *Proceedings of SPIE* - *The International Society for Optical Engineering*, vol. 3582, pp. 993–996, Dec. 1998.
- A. H. Feingold, R. L. Wahlers, P. Amstutz, C. Huang, S. J. Stein, and J. Mazzochette, 'New Microwave Applications for Thick-film Thermistors', *Microwave Journal*, vol. 43, no. 1, pp. 90–98, 2000.
- 14. A. Dziedzic and E. Prociow, *Some remarks about planar thermistors*. Prague (Czech Republic): Proc. 25th Int. Spring Seminar on Electronics Technology, 2002.
- 15. N. Gutzeit, J. Müller, C. Reinlein, and S. Gebhardt, 'Manufacturing and Characterization of a Deformable Membrane with Integrated Temperature Sensors and Heating Structures in Low Temperature Co-fired Ceramics', *International Journal of Applied Ceramic Technology*, vol. 10, no. 3, pp. 435–442, 2013,

https://doi.org/10.1111/ijac.12037.

 H. Bartsch, F. Weise, H. Cobas, and M. R. Gongora-Rubio, 'Cost-Effective Sensor for Flow Monitoring in Biologic Microreactors', *IEEE Sensors Journal*, vol. PP, pp. 1–1, Aug. 2021, https://doi.org/10.1109/JSEN.2021.3102262.

- D. Kuscer *et al.*, 'An advanced miniature fluidic system in multilayer ceramic technology with precise temperature and flow control for in situ pollution monitoring', *Sensors and Actuators A: Physical*, vol. 366, p. 114946, Feb. 2024, https://doi.org/10.1016/j.sna.2023.114946.
- M. Hrovat, D. Belavič, J. Kita, J. Holc, J. Cilenšek, and S. Drnovšek, 'Thick-film NTC thermistors and LTCC materials: The dependence of the electrical and microstructural characteristics on the firing temperature', *Journal of the European Ceramic Society*, vol. 29, no. 15, pp. 3265–3271, Dec. 2009, https://doi.org/10.1016/i.jeurceramsoc.2009.05.019.
- G. D. C. Csete de Györgyfalva and I. M. Reaney, 'Decomposition of NiMn2O4 spinel: an NTC thermistor material', *Journal of the European Ceramic Society*, vol. 21, no. 10, pp. 2145–2148, Jan. 2001, <u>https://doi.org/10.1016/S0955-2219(01)00190-X</u>.
- M. Hrovat, Z. Samardžija, J. Holc, and D. Belavič, 'The development of microstructural and electri- cal characteristics in some thick-film resistors dur- ing firing', *Journal of Materials Science*, vol. 37, no. 11, pp. 2331–2339, Jun. 2002, Liter (10.1022) (10.1022)
 - https://doi.org/10.1023/A:1015385704068.
- M. Hrovat, A. Benčan, D. Belavič, J. Holc, and G. Dražič, 'The influence of firing temperature on the electrical and microstructural characteristics of thick-film resistors for strain gauge applications', *Sensors and Actuators A: Physical*, vol. 103, no. 3, pp. 341–352, Feb. 2003,

https://doi.org/10.1016/S0924-4247(02)00402-8.

 M. Hrovat, D. Belavič, J. Holc, J. Bernard, A. Bencan, and J. Cilenšek, 'The interacions of conductive and glass phase in thick-film resistors during firing', *Informacije MIDEM*, vol. 34, pp. 7–10, Mar. 2004.



Copyright © 2024 by the Authors. This is an open access article distributed under the Creative Com-

mons Attribution (CC BY) License (https://creativecommons.org/licenses/by/4.0/), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Arrived: 26. 01. 2024 Accepted: 26. 02. 2024 https://doi.org/10.33180/InfMIDEM2024.103



Journal of Microelectronics, Electronic Components and Materials Vol. 54, No. 1(2024), 25 – 38

Examination of Resistive Switching Energy of Some Nonlinear Dopant Drift Memristor Models

Rabia Korkmaz Tan¹, Oya Mert², Resat Mutlu³

¹Department of Computer Engineering, Çorlu Faculty of Engineering, Tekirdağ Namık Kemal University, Çorlu, Tekirdağ, Turkey

²Department of Mathematics, Faculty of Arts and Sciences, Tekirdağ Namık Kemal University, Tekirdağ, Turkey

³Department of Electronics and Communication Engineering, Çorlu Faculty of Engineering, Tekirdağ Namık Kemal University, Çorlu, Tekirdağ, Turkey

Abstract: In the literature, there are memristor models based on nonlinear drift mechanisms and window functions. Memristors can be employed to model resistive memories. When the resistance of a memristor undergoes a transition from its lowest value to its highest value, or vice versa, this phenomenon is referred to as resistive or memristive switching. The energy required for this transition holds particular importance, especially in the context of resistive computer memory and digital logic applications. Experimental measurements can be used to determine the resistive switching energy, and it should also be possible to calculate it theoretically based on the parameters of the memristor model utilized. Recently, the resistive switching times of some of the nonlinear dopant drift memristor models have been examined analytically considering especially their memory and digital circuit applications. In the literature, to the best of our knowledge, the resistive switching energy of some of the well-known memristor models using a window function is calculated and found to be infinite. This is not feasible according to the experiments in which a finite resistive switching energy is consumed. The criterion that a memristor must have a finite resistive energy is also presented in this study. The results and the criterion for the resistive switching energy presented in this paper can be utilized to build more realistic memristor models in the future.

Keywords: Memristor, memristor models, resistive memories, window function, memristive switching, resistive switching

Preučevanje upornostne preklopne energije nekaterih modelov memristorjev z nelinearnim odstopanjem dopanta

Izvleček: V literaturi obstajajo modeli memristorjev, ki temeljijo na nelinearnih mehanizmih odstopanj in okenskih funkcijah. Memristorji se lahko uporabijo za modeliranje uporovnih pomnilnikov. Ko upornost memristorja preide iz najnižje vrednosti v najvišjo ali obratno, se ta pojav imenuje uporovno ali memristivno preklapljanje. Energija, ki je potrebna za ta prehod, je še posebej pomembna, zlasti v kontekstu uporovnega računalniškega pomnilnika in digitalne logike. Za določitev energije uporovnega preklopa se lahko uporabijo eksperimentalne meritve, prav tako pa jo je mogoče teoretično izračunati na podlagi parametrov uporabljenega modela memristorja. Nedavno so bili analitično preučeni uporovni preklopni časi nekaterih nelinearnih modelov memristorjev z odstopanjem dopanta, pri čemer so bile upoštevane zlasti njihove aplikacije za pomnilnike in digitalna vezja. V literaturi, kolikor nam je znano, uporovna preklopna energija memristorskih modelov z nelinearnim odstopanjem dopanta ni bila izračunana in podrobno preučena. V tej študiji je izračunana energija memristivnega preklopa nekaterih znanih modelov memristorjev z uporabo okenske funkcije in ugotovljeno je, da je neskončna. Glede na poskuse, pri katerih se porabi končna uporovno preklopna energija, to ni izvedljivo. V tej študiji je predstavljeno tudi merilo, da mora imeti memristor končno uporovno energijo. Rezultati in merilo za uporovno preklopno energijo, predstavljeni v tem članku, se lahko v prihodnosti uporabijo za izdelavo bolj realističnih modelov memristorjev.

Ključne besede: memristor, modeli memristorjev, uporovni pomnilniki, funkcija okna, memristivno preklapljanje, uporovno preklapljanje

* Corresponding Author's e-mail: rmutlu@nku.edu.tr

How to cite:

R. K. Tan et al., "Examination of Resistive Switching Energy of Some Nonlinear Dopant Drift Memristor Models", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 54, No. 1(2024), pp. 25–38

1 Introduction

In his influential article published in 1971, Dr. Chua introduced the memristor as the novel and fourth passive circuit element, joining the ranks of the resistor, inductor, and capacitor [1]. A perfect memristor is a passive circuit element that possesses two terminals and exhibits a nonlinear correlation between magnetic flux and electrical charge. The memristor has a resistance that varies by its charge, known also as memristance, and it also consumes power [1]. In 1976, a class of systems known as memristive systems, possessing properties akin to memristors, was introduced [2]. After nearly four decades after Dr. Chua's initial proposition, a nano-sized TiO2 thin film memristive system developed in Hewlett-Packard (HP) laboratory was demonstrated to possess memristor-like traits similar to those anticipated for its operation [3]. Hence, in 2008, the revelation of a novel nonlinear electronic circuit element, demonstrating memristor-like characteristics within certain operation ranges, captured global attention, leading to a surge in research and exploration of memristors and memristive systems [4-9]. Memristors have been explored for their non-volatile memory capabilities and dynamic load applications, as discussed in [4]. Memory phenomena are frequently observed in nanoscale devices, and certain effects can be effectively modeled using memristors [5]. The resistive memories, which are popular study areas nowadays, also behave as memristors and are regarded as memristors by Chua [6]. Domaradzki et al. provide a review of the applications of memristors in circuit design and computer technology [7]. The usage of memristors in various applications, such as memory, analog, logic, and neuromorphic circuits, is investigated in [8]. Memristor-based circuit applications encompass a variety of electronic circuits, including amplifiers [9, 10], oscillators [11], filters [11, 12], computer memories [6] and artificial neural network circuits [13]. A significant portion of memristor research has been devoted to modeling this novel circuit element. The pioneering and most basic physical model of a memristor was initially introduced in [3]. Williams and colleagues proposed the HP memristor model, assuming that the ion drift speed inside the memristor is directly proportional to the memristor current and remains uniform throughout the memristor. While the model is straightforward to comprehend, it incorporates a linear dopant drift and is considered obsolete now. Due to the discrepancy with the actual heterogeneous dispersion of ions, researchers have developed memristor models with nonlinear ion drift speeds, utilizing window functions to address this issue [3, 14-18]. The models presented in [14-16] face challenges related to boundary lock issues. To address this problem, researchers have developed polaritydependent window functions, as described in [15-17].

Chua has classified resistive memories as memristive systems [6]. Even after a memristor is turned off, it retains its last resistance value, and upon repowering, it resumes operation from that resistance value [1, 3, 6]. A memristor does not consume power when its current is zero [6]. This unique characteristic makes Non-Volatile Random-Access Memory (NVRAM) one of the most significant applications of memristive systems [4-8]. ReRAM application of the TiO2-based memristors is reviewed in [19]. Moreover, there is potential to develop high-density memristor-based Static Random-Access Memories (SRAMs) that consume low-power [20]. The initial discovery of the ReRAM structure involved nickel oxide (NiO) in 1964 [21]. Since then, various materials have been identified as suitable candidates for creating resistive memories [5, 7, 22-25]. The following examples are only a few of these materials. Silicon oxide has been utilized in the fabrication of resistive memories [22]. Moreover, the examination of conducting nanofilaments within a Pt/TiO2/Pt system during resistive switching has been investigated in [23]. [24] explores the memristive switching mechanism in metal/oxide/ metal nanodevices. Furthermore, [25] presents a comprehensive examination of both bipolar and unipolar operations in Resistive Random Access Memory (Re-RAM). Waser et al. suggest a broad classification into thermal, electrical, or ion-migration-induced switching mechanisms [26]. Choi et al. conducted atomic force microscopy studies using different vacuum conditions, showing a strong correlation between resistance switching and the creation and elimination of conducting spots [27]. The experimental findings presented in [28] demonstrate that the introduction of Si or Al implantation into HfO2 films leads to lower electroforming voltages and enhances the reproducibility of resistive switching. Sivkov et al. investigated the impact of thickness variation and electrode size on the resistive switching properties of ZrO2 [29]. Linn et al. investigated the resistive switching properties of the complementary resistive switches (CRS) and explored their potential utilization in passive nano crossbar memories to achieve power consumption reduction [30]. Rosezin et al. showcased the vertical integration of Complementary resistive switch cells utilizing Cu/ SiO2/Pt bipolar resistive switches [31]. By employing CRS-based memristors, 3D stacking crossbar memories experience reduced leakage current [32]. However, it is important to note that such CRS-based memories may require reconstructive circuits to rewrite the deleted information during reading [33].

Memristive materials find application in digital circuitry as well. The literature also explores various memristorbased digital circuits, including reconfigurable logic circuits, flip-flops, latches, and more [34-40]. Memristorbased programmable logic circuits can be developed [34]. The memristor-based flip-flop circuits possess nonvolatile characteristics and operate with low power consumption [35-37]. Memristors make the production of reconfigurable logic gates and devices possible [38, 39]. However, it is important to consider that implementing memristor-based logic and memory circuits might necessitate the use of adaptive writing circuits [33-40]. Vourkas et al. provide an overview of the design of memristor-based logic circuits [40].

The phenomenon in which a memristor's resistance transitions from R_{on} to R_{off} or from R_{off} to R_{on} when subjected to an applied voltage is referred to as 'memristive switching' or 'resistive switching' [41]. The duration needed for this process is referred to as the "memristive switching time" or "resistive switching time". The writing or erasing of memristor-based memories, as well as other memristor-based digital applications mentioned earlier, rely on the occurrence of memristive switching. This emphasizes the significance of the memristive or resistive switching time as a vital parameter in evaluating the effectiveness of memristor-based computer memories and memristor-based digital circuits [6, 8, 18, 30, 33, 41, 42]. Wang et al. have explored the conceptual and experimental aspects of memristive switching time, employing a piecewise linear charge-flux characteristic [41]. This time value may vary depending on the direction of the memristor current [15, 17, 18]. In [43], researchers have analyzed and conducted experimental investigations to explore the consequences of delayed memristive switching in memristor-based artificial neural networks. The research presented in [44, 45] involves the calculation of the memristive switching time using the HP memristor model. [46] proposes that memristive switching can be utilized for calculating the memristance function. In [18], the resistive switching times of the memristor models presented in [3, 14-17] are calculated using their respective window functions for both polarities, the computation of complex integrals for determining the resistive switching times is performed using the Wolfram Alpha program, and it is observed that the integrals diverge except the HP memristor model. The solutions of these integrals are analyzed and interpreted, leading to a diagnosis of the boundary unreachability problem in these models with an infinite switching time and the proposal of a new memristor model that provides a finite switching time [18].

In literature, different types of memories are compared for their power consumption [20, 30-32, 39, 47-49]. However, there are only a few papers regarding memristor power consumption [50-53]. In [50], an AC power formula for memristors under small signal excitation is given. In [51], the power consumption of memristor-based relaxation oscillators is examined with the instantaneous memristor power formula. In [39], it is shown that the tolerances of the memristors result in a different switching time for each memristor and, therefore, a different energy loss for writing and deleting a memristor. The resistive switching energy besides resistive switching time is an important parameter in memristor-based memory and digital applications such as flip-flops, logic gates, etc. The required resistive switching energy should be calculatable with the parameters of the memristor model used to model the device. The paper aims to examine the resistive switching energy of some of the well-known memristor models. In this paper, first, the resistive or memristive switching energy formula for the nonlinear drift speed memristor models is derived, and, then, the memristive switching energy of the memristor models given in [3, 14-18] is tried to be calculated with their window functions considering both polarities. The WolframAlpha program is used to solve the definite integrals of the resistive switching energy. Some of the definite integrals are shown to diverge. The interpretation of the results is done.

This paper is structured as follows. In the second section, the nonlinear dopant drift memristor model and the window functions used in this study are summarized. In the third section, the derivation of the integral formula to calculate the memristive switching energy considering the memristor polarity is made. Analytical solutions of the switching times of the nonlinear dopant drift memristor models are sought in the fourth section. The paper is finished with the conclusion section.

2 Memristor models and their window functions

This section provides a brief explanation of the memristor models employed in this study. A memristor, which is also a memristive system [2], is described as an (ideal) device where the charge of the memristor serves as the system's state variable. Nevertheless, the present-day terminology refers to thin-film systems, which fall under the category of memristive systems, as memristors [54]. One particular memristor model, characterized by nonlinear dopant drift, is represented by the following equations:

$$v(t) = R(x)i(t). \tag{1}$$

$$dx / dt = \mu_{v} \frac{R_{on}}{D^{2}} .i(t) f(x, i).$$
⁽²⁾

where i(t), v(t), R(x), R_{ort} , x(t) and f(x, i) are the current, voltage, resistance, minimum resistance, state variable,

and polarity-dependent window function of the memristor, respectively, *D* is the total length of the TiOx region, and μ_{a} is the dopant mobility of the TiO2 region.

The state variable of the memristor, which represents its normalized oxidized length, can be mathematically expressed as

$$x = w/D \tag{3}$$

where denotes its current oxidized length.

To determine the rate of drift speed in this memristor model, a window function is introduced, which involves multiplying the memristor current according to equation (2) [3, 14-18]. The memristor memristance or resistance is expressed as

$$R(x) = R_{on} x + R_{off} (1-x) = R_{off} - (R_{off} - R_{on}) x$$
(4)

Based on the model presented in [3] a memristor's resistance varies within the range of its minimum value, $R_{on'}$ to its maximum value, $R_{off'}$ Consequently, the following statement always holds for the resistance of a memristor:

$$R_{off} \ge R(x) \ge R_{on} \tag{5}$$

This research utilizes memristor models proposed by Strukov [3] Joglekar [14], Biolek [15] Prodromakis [16] Zha [17], Mutlu-Kumru [18]. A comprehensive overview of the memristor models employed in this study is available in [55]. These models are characterized by window functions, which act as indicators of the degree to which a memristor emulates an ideal memristor [15]. The corresponding window functions are detailed in Table 1.

While the literature represents polarity-dependent window functions as f(x), in this study, they are represented as f(x, i) to include the polarity variable.

The resistance value or memristive state variable of these memristors begins to change only when both their window function and current are not equal to zero. The window functions described in [14, 16], which exhibit zero dopant speeds at the boundaries of the memristive layer, face an issue known as the boundary lock problem: at x = 0 and x = 1, their resistance value, memristive state-variable, or window function f(x) remains unchanged regardless of the value of current flowing. The models presented in [15, 17-18] do not experience these problems. All the window functions listed in Table 1 are phenomenal functions.

The experimental data might lead to the development of more realistic window functions with improved accuracy in the future. The window function of the HP model is regarded as being equal to one [3]. The "stp()" function in Table 1 represents the unit step function and is defined as follows.

$$stp(i) = \begin{cases} 1 & , i \ge 0 \\ 0 & , i < 0 \end{cases}$$
(6)

Comparisons of the mentioned window functions, whose resistive switching time is examined in [18] are given in Table 2.

The Strukov model is characterized by a non-scalable quadratic window function and suffers from a boundary lock issue. This means that once the boundary is reached, the regions become fixed at the boundaries, causing the model to function like a resistor. Even changing the polarity cannot resolve the problem because f(0) = f(1) = 0. The window function of the Joglekar model incorporates a shaping parameter (*p*), which allows for modifications to its shape. However, it also exhibits a boundary lock issue. On the other hand, the Biolek model features a current polarity-dependent window function.

When the current of the Biolek memristor model is positive and its window function at x = 1 is 0, this causes the memristor to act as a linear time-invariant (LTI) resistor. However, when the current of the Biolek memristor model is negative and its window function at x = 1is 1, this results in a change in the memristor's resistance. On the other hand, when the current of the Biolek memristor model is negative and its window function at x = 0 is 0, the memristor behaves as a resistor. But, when the current of the Biolek memristor model is positive and its window function at x = 0 is 1, this leads to a variation in the memristor's resistance. Altering the current polarity in the model leads to a change in its resistance, thereby eliminating any boundary lock issues. Nevertheless, it is important to note that the model lacks scalability.

The Prodromakis model exhibits a boundary lock problem, but its window function can be scaled using the parameter j. Moreover, the Zha model integrates the polarity dependency of Biolek's window function with the scalability of Prodromakis' window function.

The model	Its window function $(f(x) \text{ or } f(x, i))$
HP	f(x) = 1
Strukov	$f(x) = x - x^2$
Joglekar	$f(x) = 1 - (2x - 1)^{2p}$
Biolek	$f(x,i) = 1 - \left(x - stp(-i(t))\right)^{2p}$
Prodromakis	$f(x) = j \left(1 - \left(\left(x - 0.5 \right)^2 + 0.75 \right)^p \right)$
Zha	$f(x,i) = j \left(1 - \left(0.25 \left(x - stp(-i) \right)^2 + 0.75 \right)^p \right)$
Mutlu-Kumru	$f(x,i)m_1\sqrt[n]{1-x}.stp(i)+m_2\sqrt[n]{x}.stp(-i)$

Table 1: The memristor window functions used in this study

Table 2: Comparison of the memristor window functions used in this study

Window functions	Strukov	Joglekar	Biolek	Prodromakis	Zha	Mutlu-Kumru
Variables of the window function	х	х	x, i	х	x, i	x, i
Formability	No	Yes	Yes	Yes	Yes	Yes
Formability parameter	-	р	р	р	р	n
Scalability	No	No	No	Yes	Yes	Yes
Scalability parameter	-	-	-	j	j	m ₁ , m ₂
Problem of boundary lock	Yes	Yes	No	Yes	No	No
Boundary unreachability	No	No	Yes	No	Yes	No

The resistive switching times of the memristor models given in Table 3 are calculated for each polarity in [18]. Only, the HP and Mutlu-Kumru Models have given finite resistive switching times values.

3 Derivation of resistive switching energy formula of nonlinear dopant drift memristive models

The circuits, which are shown in Fig. 1, can be used to make the memristive switching occur. The memristor in the circuit in Fig. 1a is forward-biased and a positive DC voltage is applied to it, and the switch is turned on at a time equal to zero. If the memristor resistance is equal to R_{off} at t = 0, the memristor resistance falls down from R_{off} to R_{on} in this case. The memristor in the circuit in Fig. 1b is reverse-biased and a negative DC voltage is applied to it, and the switch is turned on at a time equal to zero. If the memristor in the circuit in Fig. 1b is reverse-biased and a negative DC voltage is applied to it, and the switch is turned on at a time equal to zero. If the memristor resistance is equal to R_{on} at t = 0, the memristor memristance goes from R_{on} to R_{off} in that case. For polarity dependent memristor models, the memristive or resistive switching Energy must be found for each polarity.



Figure 1: The memristor supplied by a) a positive DC voltage source for the forward resistive switching (*x* goes up from 0 to 1) and b) a negative DC voltage source for the reverse resistive switching (*x* goes down from 1 to 0)

The model	Its resistive switching time in the forward direction	Its resistive switching time in the reverse direction				
НР	$\frac{D^2\left(R_{on}+R_{off}\right)}{2\mu_V R_{on} V_{dc}}$	$\frac{D^2 \left(R_{on} + R_{off}\right)}{2 \mu_V R_{on} V_{dc}}$				
Strukov	∞	∞				
Joglekar	∞	∞				
Biolek	∞	∞				
Prodromakis	∞	∞				
Zha	∞	∞				
Mutlu-Kumru	$\left(\frac{R_{on}-R_{off}}{V_{dc}Km_{1}}\right)\left(\frac{n}{2n-1}\right)+\frac{R_{off}}{V_{dc}Km_{1}}\left(\frac{n}{n-1}\right)$	$\frac{1}{V_{dc}K}\left(\frac{R_{on}-R_{off}}{m_2}\left(\frac{n}{2n-1}\right)+\frac{R_{off}}{m_2}\left(\frac{n}{n-1}\right)\right)$				

Table 3: The resistive switching times of the memristor models

Considering the nonlinear memristor models explained before, the memristive switching energy can be calculated as follows. The current of a forward-biased memristor supplied with the constant voltage V_{dc} is

$$i(t) = \frac{v(t)}{R(x)} = \frac{V_{dc}}{R(x)}.$$
(7)

The power of the memristor is

$$p(t) = v(t)i(t) = v(t)\frac{v(t)}{R(x)} = \frac{\left(V_{dc}\right)^2}{R(x)}.$$
(8)

For a forward-biased memristor, the energy consumption of the memristor, in which x(t) rises from 0 to 1, is calculated as

$$E_{SWP} = \int_{0}^{\tau_{SWP}} p(t) dt = \int_{0}^{\tau_{SWP}} \frac{(V_{dc})^{2}}{R(x)} dt$$
(9)

The derivative of the state variable of the memristive models can be written as

$$\frac{dx}{dt} = \frac{\mu_V R_{on}}{D^2} i(t) f(x) = \frac{\mu_V R_{on} V_{dc} f(x)}{D^2 R(x)}$$
(10)

By rearranging (10),

$$dt = \frac{D^2 R(x) dx}{\mu_V R_{on} V_{dc} f(x)}$$
(11)

During the forward resistive switching: at t = $\tau_{_{SWP}}$, $x(\tau_{_{SWP}}) = 1$ and, at t = 0, x(0) = 0. Submitting Eq. (11) into Eq. (9):

$$E_{SWP} = \int_{0}^{1} \frac{(V_{dc})^{2}}{R(x)} \frac{D^{2}R(x)dx}{\mu_{V}R_{on}V_{dc}f(x)} = \frac{V_{dc}D^{2}}{\mu_{V}R_{on}} \int_{0}^{1} \frac{dx}{f(x)}.$$

$$= \frac{V_{dc}D^{2}}{\mu_{V}R_{on}} \int_{0}^{1} \frac{dx}{f(x)}.$$
(12)

The energy or the integral in Eq. (12) depends on the window function of the forward-biased memristor. Assuming that, after the forward resistive switching occurs, for a short time, the device continuous on drawing current since the applied pulse width is wider than its forward switching time ($\tau_{SWP} \leq T_p$), an additional conduction loss occurs. It can be calculated as:

$$E_{CP} = \int_{\tau_{SWP}}^{T_{P}} p(t) dt = \int_{\tau_{SWP}}^{T_{P}} \frac{(V_{dc})^{2}}{R_{on}} dt = \frac{(V_{dc})^{2}}{R_{on}} (T_{P} - \tau_{SWP})$$
(13)

Then, the total loss in this case can be found as:

$$E_P = E_{SWP} + E_{CP} \tag{14}$$

For a reverse-biased memristor, the switching voltage is negative and equal to $-V_{dc}$, the energy consumption of the memristor, in which x(t) falls down from 1 to 0, is calculated as

$$E_{SWN} = \int_{0}^{\tau_{SWN}} p(t) dt = \int_{0}^{\tau_{SWN}} \frac{(V_{dc})^{2}}{R(x)} dt$$
(15)

The energy or the integral in Eq. (12) depends on the window function of the forward-biased memristor.

During the reverse resistive switching: at $t = \tau_{SWN'} x(\tau_{SWN}) = 0$ and, at t = 0, x(0) = 1. Submitting Eq. (11) into Eq. (15):

$$E_{SWN} = \int_{1}^{0} \frac{(V_{dc})^{2}}{R(x)} \frac{D^{2}R(x)dx}{\mu_{V}R_{on}(-V_{dc})f(x)} = = -\frac{V_{dc}D^{2}}{\mu_{V}R_{on}} \int_{1}^{0} \frac{dx}{f(x)} = \frac{V_{dc}D^{2}}{\mu_{V}R_{on}} \int_{0}^{1} \frac{dx}{f(x)}.$$
(16)

Eq. (16) is the same as Eq. (13) but the window function for the correct polarity should be utilized to calculate the switching energy.

The energy or the integral in Eq. (16) depends on the window function of the reverse-biased memristor. Assuming that, after the reverse resistive switching occurs, for a short time the device continuous on drawing current since the applied pulse width is wider than its reverse switching time ($\tau_{SWN} \leq T_p$), an additional conduction loss occurs. It can be calculated as:

$$E_{CN} = \int_{\tau_{SWN}}^{T_{P}} p(t) dt = \int_{\tau_{SWN}}^{T_{P}} \frac{(-V_{dc})^{2}}{R_{off}} dt = \frac{(V_{dc})^{2}}{R_{off}} (T_{P} - \tau_{SWN}) (17)$$

Then, the total loss can be found as:

$$E_N = E_{SWN} + E_{CN} \tag{18}$$

Considering Eq.s (12) and (16), for a nonlinear dopant drift memristor model, the resistive switching energy is proportional to the DC voltage applied, and the memristor parameters, D, μ_v , and R_{on} , the switching voltage V_{dc} define the resistive switching energy, the lower the minimum resistance of the memristor, the higher the resistive switching energy. However, the conduction loss of the memristor depends on only R_{on} for the forward-biased memristor and R_{off} for the reverse-biased memristor. If a memristor model's window function is not dependent on polarity, the resistive switching energy for each polarity is the same:

(19)

$$E_{SWP} = E_{SWN}$$

In this section, the switching energy of the examined memristor models can be found using the derived equations.

4.1 Resistive switching energy of the HP memristor model

The HP memristor model is the first memristor model given in the literature [3]. It is the simpler than the other memristor models examined in this study [18]. In this model, it is assumed that the linear dopant drift exists in the memristive element [3]. The window function of the HP memristor model is equal to one, i.e., f(x) = 1. The resistive switching energy of an HP memristor is calculated as

$$E_{SWP} = \frac{V_{dc}D^2}{\mu_V R_{on}} \int_0^1 \frac{dx}{f(x)} .$$

$$E_{SWP} = \frac{V_{dc}D^2}{\mu_V R_{on}} \int_0^1 \frac{dx}{1}$$

$$= \frac{V_{dc}D^2}{\mu_V R_{on}} \int_0^1 dx$$

$$= \frac{V_{dc}D^2}{\mu_V R_{on}} [x]_0^1 = \frac{V_{dc}D^2}{\mu_V R_{on}}$$
(20)

In [18] it is shown that the resistive switching time of an HP memristor for each polarity is the same. The resistive switching energy of an HP memristor for each polarity is also the same.

4.2 Resistive switching energy of the memristor model with Strukov window function

The Strukov window function does not depend on the polarity of the memristor. It is expressed as

$$f\left(x\right) = x - x^2 \tag{21}$$

Therefore, its resistive switching energy is the same for each polarity. Its resistive switching energy is found as

$$E_{SWP} = E_{SWN} = \frac{V_{dc}D^2}{\mu_V R_{on}} \int_0^1 \frac{dx}{f(x)}$$

= $\frac{V_{dc}D^2}{\mu_V R_{on}} \int_0^1 \frac{dx}{x - x^2}$ (22)
= $\frac{V_{dc}D^2}{\mu_V R_{on}} (\ln|x| - \ln|1 - x|)_0^1 = \infty$

The resistive switching energy of the memristor model is infinite or its integral diverges. This is expected since the model has a boundary lock problem. In [18], its resistive switching time is also found to be infinite. The resistive switching energy is the same for both directions since the Strukov window function is the same for each polarity.

4.3 Resistive switching energy of the memristor model with Joglekar window function

Joglekar window function does not depend on the polarity of the memristor either. It is expressed as

$$f(x) = 1 - (2x - 1)^{2p}$$
⁽²³⁾

where *p* is a positive integer used to shape the window function.

That is why its resistive switching energy is the same for each polarity of the memristor. Using Wolfram Alpha for the evaluation of the integral, its resistive switching energy is found as

$$E_{SWP} = \frac{V_{dc}D^2}{\mu_V R_{on}} \int_0^1 \frac{dx}{f(x)} .$$

$$= \frac{V_{dc}D^2}{\mu_V R_{on}} \int_0^1 \frac{dx}{1 - (2x - 1)^{2p}}$$

$$= \frac{V_{dc}D^2}{\mu_V R_{on}} \left(\frac{1}{2} (2x - 1)_2 F_1 \left(1, \frac{1}{2p}; 1 + \frac{1}{2p}; (2x - 1)^{2p} \right) \right)_0^1$$

$$= \left(\frac{1}{2} (1)_2 F_1 \left(1, \frac{1}{2p}; 1 + \frac{1}{2p}; 1 \right) - \frac{1}{2} 0_2 F_1 \left(1, \frac{1}{2p}; 1 + \frac{1}{2p}; 0 \right) \right) = \infty$$
where $_2F_1 \left(1, \frac{1}{2p}; 1 + \frac{1}{2p}; (x)^{2p} \right)$ is the hypergeometric

function whose value becomes infinite for x = 1.

The resistive switching energy of the Joglekar memristor model is infinite or its integral diverges. This is expected since the model has a boundary lock problem. The resistive switching energy is the same for both directions since the Joglekar window function is the same for each polarity. The memristive switching time of the memristor model has also been found to be infinite in [18].

v

4.4 Resistive switching energy of the memristor model with Biolek window function

The Biolek window function depends on the current polarity of the memristor. It can be given as

$$f(x) = 1 - \left(x - stp\left(-i(t)\right)\right)^{2p}$$
(25)

That is why its resistive switching energy should be calculated for both polarities. For the reverse-biased memristor, i.e., for $i \le 0$, using WolframAlpha integral calculator, its resistive switching energy is found as

$$E_{SWN} = \frac{V_{dc}D^2}{\mu_V R_{on}} \int_0^1 \frac{dx}{1 - (x - 1)^{2p}} .$$

$$= \frac{V_{dc}D^2}{\mu_V R_{on}} \left((x - 1)_2 F_1 \left(1, \frac{1}{2p}; 1 + \frac{1}{2p}; (x - 1)^{2p} \right)_0^1 \right) = \infty$$
(26)

For the forward-biased memristor, i.e., for i > 0, using Wolfram Alpha integral calculator, its resistive switching energy is found as

$$E_{SWP} = \frac{V_{dc}D^2}{\mu_V R_{on}} \int_0^1 \frac{dx}{f(x)} .$$

$$E_{SWP} = \frac{V_{dc}D^2}{\mu_V R_{on}} \int_0^1 \frac{dx}{1 - (x)^{2p}} .$$

$$E_{SWP} = \frac{V_{dc}D^2}{\mu_V R_{on}} \left(x_2 F_1 \left(1, \frac{1}{2p}; 1 + \frac{1}{2p}; (x)^{2p} \right)_0^1 \right) = \infty (28)$$

The resistive switching energy of the Biolek memristor model is infinite for each polarity. The resistive switching time of the Biolek memristor model has also been found to be infinite in [18] due to having the boundary unreachability problem.

4.5 Resistive switching energy of the memristor model with Prodromakis window function

The Prodramakis window function does not depend on the memristor polarity either. It is expressed as

$$f(x) = j\left(1 - \left(\left(x - 0, 5\right)^2 + 0, 75\right)^p\right)$$
(29)

Therefore, its resistive switching energy is same for both polarities. Using WolframAlpha integral calculator, it is calculated as

$$E_{SWP} = \frac{V_{dc}D^2}{j\mu_V R_{on}} \int_0^1 \frac{dx}{\left(1 - \left(\left(x - 0, 5\right)^2 + 0, 75\right)^p\right)} = \infty$$
(30)

The resistive switching energy of the Prodramakis memristor model is found to be infinite or its integral diverges. This is expected since the model has a boundary lock problem. The resistive switching energy is the same for both directions since the Prodramakis window function is the same for each polarity. The memristive switching time of the memristor model has also been found to be infinite in [18].

4.6 Resistive switching energy of the memristor model with Zha window function

The Zha window function depends on the memristor polarity and is expressed as

$$f(x) = j \left(1 - \left(0.25 \left(x - stp(-i) \right)^2 + 0.75 \right)^p \right) (31)$$

For the forward-biased memristor, i.e., for i > 0, using Wolfram Alpha integral calculator, its resistive switching energy is found as

$$E_{SWP} = \frac{V_{dc}D^2}{j\mu_V R_{on}} \int_0^1 \frac{dx}{\left(1 - \left(0.25x^2 + 0.75\right)^p\right)} = \infty$$
(32)

The resistive switching energy of the Zha memristor model is infinite for each polarity. The resistive switching time of the Zha memristor model has also been found to be infinite in [18] due to having the boundary unreachability problem.

4.7 Calculation of resistive switching energy of the memristor model with Mutlu-Kumru window function

In [18], a new memristor model without boundary lock and boundary unreachability problems have been proposed. It was the only model besides the HP memristor model whose switching times have been able to be calculated. The Mutlu-Kumru window function also depends on the polarity and is given as

$$f(x,i) = m_1 \sqrt[n]{1-x} . stp(i) + m_2 \sqrt[n]{x} . stp(-i)$$
(33)

The function f(x, i) considering the memristor polarity can be expressed as the following piece-wise function:

$$f(x,i) = \begin{cases} m_1 \sqrt[n]{1-x}, & i \ge 0\\ m_2 \sqrt[n]{x}, & i < 0 \end{cases}$$
(34)

where *n* is the shaping constant, which is a positive number, m_1 is the forward-polarity scaling constant, m_2 is the reverse-polarity scaling constant direction, *i* is the memristor current.

The Mutlu-Kumru window function for each polarity is shown in Figure 2. The resistive switching energy of the model should be calculated for both polarities. For the forward-biased memristor, i.e., for $i(t) \ge 0$, using Wolfram Alpha integral calculator, its resistive switching energy is found as

$$E_{SWP} = \frac{V_{dc}D^2}{\mu_V R_{on}} \int_0^1 \frac{dx}{m_1 \sqrt[n]{1-x}} = \frac{V_{dc}D^2}{\mu_V R_{on} m_1} \int_0^1 \frac{dx}{\sqrt[n]{1-x}}$$

$$= \frac{V_{dc}D^2}{\mu_V R_{on} m_1} \left(\frac{(1-x)^{1-\frac{1}{n}}}{1-\frac{1}{n}}\right)^1 = \frac{V_{dc}D^2}{\mu_V R_{on} m_1} \left(\frac{n}{n-1}\right)$$
(35)

For the reverse-biased memristor, i.e., for $i \le 0$, using Wolfram Alpha integral calculator, its resistive switching energy is found as

$$E_{SWN} = \frac{V_{dc}D^2}{\mu_V R_{on}} \int_0^1 \frac{dx}{m_2 \sqrt[n]{x}} = \frac{V_{dc}D^2}{\mu_V R_{on} m_2} \int_0^1 \frac{dx}{\sqrt[n]{x}}$$

$$= \frac{V_{dc}D^2}{\mu_V R_{on} m_2} \left(\frac{n}{n-1}\right)$$
(36)



Figure 2: The Mutlu-Kumru window function for a) the reverse biased memristor (i(t) < 0), various *n* values, and $m_2 = 1$, and b) for the forward biased memristor (i(t) > 0), various *n* values, and $m_1 = 1$.

From Eq.s (35) and (36), it can be seen that the resistive switching energy converges except for n = 1. If n < 1, the resistive switching energy of the Mutlu-Kumru memristor model is negative, i.e., the Mutlu-Kumru cannot be used to model a memristor for n < 1. If $m_2 = m_{11}$, the resistive switching energy of the model for each polarity is the same:

$$E_{SWP} = E_{SWN} \tag{37}$$

Also, for the Mutlu-Kumru model, the following relationship can be written as

$$E_{SWN}m_2 = E_{SWP}m_1 \tag{38}$$

In this section, it is also examined how the resistive switching energy varies with respect to *n*, the memristor power exponent, which is used to shape its window function. The reverse resistive switching energy normalized with respect to $\frac{V_{dc}D^2}{\mu_V R_{on}m_2}$ and the forward resistive switching energy normalized with respect to $\frac{V_{dc}D^2}{\mu_V R_{on}m_1}$ as a function of the parameter *n* is shown in Figure 3. The resistive switching energy asymptotically approaches infinity when n approaches 1. For high values of *n*, Eq.s (35) and (36),

$$E_{SWP} \approx \frac{V_{dc} D^2}{\mu_V R_{on} m_1}$$
(39)

and

$$E_{SWN} \approx \frac{V_{dc} D^2}{\mu_V R_{on} m_2} \tag{40}$$

For high values of *n*, Eq.s (40) and (41) become equal to Eq. (11), i.e., the Mutlu-Kumru model turns into the HP memristor model.

In [18], for the reverse-biased memristor, the resistive switching time is given as

$$\tau_{SWN} = \frac{1}{V_{dc}K} \left(\frac{R_{on} - R_{off}}{m_2} \left(\frac{n}{2n - 1} \right) + \frac{R_{off}}{m_2} \left(\frac{n}{n - 1} \right) \right) (41)$$

In [18], for the forward-biased memristor, the resistive switching time is given as

$$\tau_{SWP} = \left(\frac{R_{on} - R_{off}}{V_{dc}Km_1}\right) \left(\frac{n}{2n - 1}\right) + \frac{R_{off}}{V_{dc}Km_1} \left(\frac{n}{n - 1}\right)$$
(42)

From Eq.s (42) and (43), it can be seen that the switching time converges except for $n = \frac{1}{2}$ and n = 1. These two cases have not been reported in [18]:

- If $m_2 = m_1$, the resistive switching times of the Mutlu-Kumru model for each polarity is found as the same.
- If *n* < 1, the resistive switching times of the Mutlu-Kumru is negative, i.e., the Mutlu-Kumru is invalid for *n* < 1.

Also, for the Mutlu-Kumru model, the following relationship can be written as

$$\tau_{SWN}m_2 = \tau_{SWP}m_1 \tag{43}$$

Considering Eq.s (38) and (43),

$$\frac{E_{SWN}}{\tau_{SWN}} = \frac{E_{SWP}}{\tau_{SWP}}$$
(44)



Figure 3: The normalized resistive switching energy of the Mutlu-Kumru memristor model with respect to the parameter n for a) the reverse biased memristor (i(t) < 0) and b) the forward biased memristor (i(t) > 0).

For i(t) > 0, the resistive switching time of the Mutlu-Kumru model can also be written as

$$\tau_{SWP} = \left(\frac{R_{on} - R_{off}}{V_{dc}Km_1} \left(\frac{1}{2 - \frac{1}{n}}\right) + \frac{R_{off}}{V_{dc}Km_1} \left(\frac{1}{1 - \frac{1}{n}}\right)\right)$$
(45)

For i(t) > 0, using the resistive switching energy, the shaping factor of the Mutlu-Kumru model can be found as

$$n = \frac{E_{SWP}\mu_{V}R_{on}m_{1}}{E_{SWP}\mu_{V}R_{on}m_{1} - V_{dc}D^{2}}$$
(46)

By summitting (46) into Eq. (45), the relationship between the resistive switching energy and the resistive switching time for the forward-biased memristor is found as

$$\tau_{SWP} = \frac{R_{on} - R_{off}}{V_{dc} K m_1} \left(\frac{1}{2 - \frac{E_{SWP} \mu_V R_{on} m_1 - V_{dc} D^2}{E_{SWP} \mu_V R_{on} m_1}} \right) + \frac{R_{off}}{V_{dc} K m_1} \left(\frac{1}{1 - \frac{E_{SWP} \mu_V R_{on} m_1 - V_{dc} D^2}{E_{SWP} \mu_V R_{on} m_1}} \right)$$
(47)

For $i(t) \le 0$, the resistive switching time of the Mutlu-Kumru model can also be written as

$$\tau_{SWN} = \frac{1}{V_{dc}K} \left(\frac{R_{on} - R_{off}}{m_2} \left(\frac{1}{2 - \frac{1}{n}} \right) + \frac{R_{off}}{m_2} \left(\frac{1}{1 - \frac{1}{n}} \right) \right) (48)$$

For $i(t) \le 0$, using the resistive switching energy, the shaping factor of the Mutlu-Kumru model can be found as

$$n = \frac{E_{SWN} \mu_V R_{on} m_2}{E_{SWN} \mu_V R_{on} m_2 - V_{dc} D^2}$$
(49)

By summitting (49) into Eq. (48), the relationship between the resistive switching energy and the resistive switching time for the reverse-biased memristor,

$$\tau_{SWN} = \frac{R_{on} - R_{off}}{V_{dc} K m_2} \left(\frac{1}{2 - \frac{E_{SWN} \mu_V R_{on} m_2 - V_{dc} D^2 1}{E_{SWN} \mu_V R_{on} m_2}} \right) + \frac{R_{off}}{V_{dc} K m_2} \left(\frac{1}{1 - \frac{E_{SWN} \mu_V R_{on} m_2 - V_{dc} D^2 1}{E_{SWN} \mu_V R_{on} m_2}} \right)$$
(50)

5 Conclusion

The switching energy of memristors or resistive memories is an important physical quantity, that needs to be calculated accurately for digital applications. In this study, first, the resistive switching energy formula for the memristor models is derived. Then, the solutions of the definite integrals of the resistive switching energy of the several well-known memristor models with nonlinear dopant drift speed are given using the Wolf-
ram-Alpha integral calculator. In [18], it was shown that some of the memristor models examined could not do memristive switching in a finite time due to the boundary lock and boundary unreachability problems, i.e., the switching times of these models are found to be infinite except the HP model and the proposed (Mutlu-Kumru) memristor model. In this study, it has been shown that the memristor models with the boundary lock and boundary unreachability problems examined in [18] also require infinite energy for the resistive switching to occur. This is not feasible since an infinite amount of energy cannot be supplied with a physical power source and the calculated switching energy also does not match the experimental results in the literature in which the resistive switching occurs with a finite energy [30, 51, 58]. Amongst the examined models, only the HP memristor and the Mutlu-Kumru model need a finite switching energy. The reason for the infinite energy requirement of the memristor models with boundary unreachability problem has been found as the drift velocity of the doped region inside the memristor decreases to very low values as it approaches the boundaries in these models and, therefore, the resistive switching or the total drifting time takes infinite time, which is regarded as a modern Zeno's paradox in [56]. While the extending doped region approaches any of the boundaries under constant voltage, the doped region slows down so much that the switching time becomes infinite, and this results in an infinite energy consumption. It has also been shown that the models which have an infinite switching time [18] also have an infinite switching energy.

The memristor models well-known and commonly used in the literature are not able to do the resistive switching for whatever the switching voltage is. Any memristor model with this problem is not physically correct. Because, according to experimental studies, the ionic memristors can switch in both directions under a constant voltage and their switching energy increases with increasing voltage. If these memristor models' switching is examined with programs such as Spice, LTspice, and Simulink [15-33] it looks like these memristor models can do resistive switching in a finite time and with finite switching energy according to the simulation results. This is because the numerical methods utilized in the simulation of the resistive switching results in an error. Upon analyzing the switching behavior of these memristors using numerical methods, it appears that the doped region within the memristor can reach either of the boundaries, assuming it moves at the average speed calculated in the previous time. However, [18] demonstrates that this is not valid. The discrete nature of numerical methods like Euler or Range-Kutta makes it impossible to accurately calculate the deceleration of the doped region when it approaches any of the memristor boundaries when a memristor model with boundary unreachability problem is used.

In this study, the effect of memristor polarity on the resistive switching energy was also examined, and it has been demonstrated that the switching energy integral diverges for both polarities in the memristor models examined except the HP and the Mutlu-Kumru memristor models. The results show that the memristor models that require infinite switching energy are not physical models despite being numerically simulatable, and, therefore, better memristor models, whose not only resistive switching time but also resistive switching energy integrals converge, are needed. In [18] to solve this problem, a new memristor model with a finite switching time has been proposed. In this study, it is also demonstrated that the Mutlu-Kumru memristor model does the resistive switching with a finite amount of energy under a DC voltage for each polarity.

The Mutlu-Kumru memristor model's switching energy is also examined parametrically. It has been shown that for high n values, the switching energy of the Mutlu-Kumru model asymptotically approaches that of the HP memristor. For the Mutlu-Kumru memristor model, it has been shown that its switching time energy is a nonlinear function of its resistive switching energy.

A memristor model must have the three fingerprints of a memristor as explained in [57]. Experimental results such as the ones given in [30, 51, 58] show that a memristor must switch in a finite time but the models examined in [18] and this study except the HP and the Mutlu-Kumru models analytically cannot do resistive switching with a finite energy in a finite time. Therefore, in [18], it is suggested that if a new memristor model is proposed in the literature, its switching time must be a finite value and the convergence of the memristor switching time integral should also be satisfied as an additional criterion besides having the three fingerprints of the memristor. In our opinion, also, the resistive switching energy of a memristor must also be finite or its switching energy integral should also converge to a finite value. Only the memristor models satisfying with the criterion given here and in [18] can be used to build memristor-based digital circuits and memories more accurately in the future.

6 Acknowledgments

The authors would like to thank the editors and the anonymous reviewers whose insightful comments have helped to improve the quality of this paper considerably.

7 References

- L. O. Chua, "Memristor-The missing circuit element," IEEE Transactions on Circuit Theory, vol. 18, pp. 507-519, September 1971. https://doi.org/10.1109/TCT.1971.1083337.
- L. O. Chua and S. M. Kang, "Memristive devices and systems," Proceedings of the IEEE, vol. 64, pp. 209-223, February1976. https://doi.org/10.1109/PROC.1976.10092.
- D. B Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The Missing Memristor Found," Nature, vol. 453, pp. 80-83, May 2008. https://doi.org/10.1038/nature06932.
- T. Prodromakis and C. Toumazou, "A review on memristive devices and applications," in 17th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Athens, Greece, 2010, pp. 934 – 937.
- https://doi.org/10.1109/ICECS.2010.5724666
 Y. V. Pershin, M. Di Ventra, "Memory effects in complex materials and nanoscale systems," Advances in Physics, vol. 60, pp. 145-227, 2011.

https://doi.org/10.1080/00018732.2010.544961.

6. L. Chua, "Resistance switching memories are memristors," Applied Physics A, vol. 102, pp. 765-783, 2011.

https://doi.org/10.1007/s00339-011-6264-9.

- J. Domaradzki, D. Wojcieszak, T. Kotwica, and E. Mankowska, "Memristors: a short review on fundamentals, structures, materials and applications," International Journal of Electronics and Telecommunications, vol. 66, pp 373-381, 2020. <u>https://doi.org/10.24425/ijet.2020.131888.</u>
- S. G. Hu, S. Y. Wu, W. W. Jia et al., "Review of nanostructured resistive switching memristor and its applications," Nanoscience and Nanotechnology Letters, vol. 6, pp. 729-757, 2014. https://doi.org/10.1166/nnl.2014.1888.
- 9. S. Shin, K. Kim, and S. M. Kang, "Memristor applications for programmable analog ICs," IEEE Transactions on Nanotechnology vol. 10, pp. 266-274, 2011.

```
https://doi.org/10.1109/TNANO.2009.2038610.
```

- 10. T. A. Wey, W. D. Jemison, "Variable gain amplifier circuit using titanium dioxide memristors," IET Circuits, Devices & Systems, vol. 5, pp. 59-65, 2011. https://doi.org/10.1049/iet-cds.2010.0210.
- 11. Y. V. Pershin, M. Di Ventra, "Practical approach to programmable analog circuits with memristors," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, pp. 1857-1864, 2010. https://doi.org/10.1109/TCSI.2009.2038539.
- 12. S. C. Yener, R. Mutlu, and H. H. Kuntman, "A new memristor-based high-pass filter/amplifier: Its analytical and dynamical models," in 24th Inter-

national Conference Radioelektronika, Bratislava, Slovakia, 2014, pp. 1-4.

https://doi.org/10.1109/Radioelek.2014.6828420

- A. Thomas, "Memristor-based neural networks," Journal of Physics D: Applied Physics, vol. 46, 093001, 2013. <u>https://doi.org/10.1088/0022-3727/46/9/093001.</u>
- Y. N. Joglekar, S. J. Wolf, "The elusive memristor: properties of basic electrical circuits," European Journal of Physics, vol. 30, no. 4, 661, 2009. https://doi.org/10.1088/0143-0807/30/4/001.
- 15. Z. Biolek, D. Biolek, and V. Biolkova, "SPICE model of memristor with nonlinear dopant drift," Radioengineering, vol. 18, pp. 210-214, 2009.
- 16. T. Prodromakis, B. P. Peh, C. Papavassiliou, and C. Toumazou, "A versatile memristor model with nonlinear dopant kinetics," IEEE Transactions on Electron Devices, vol. 58, pp. 3099-3105, 2011. https://doi.org/10.1109/TED.2011.2158004.
- 17. J. Zha, H. Huang, and Y. Liu, "A novel window function for memristor model with application in programming analog circuits," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 63, pp.423-427, 2016.

https://doi.org/10.1109/TCSII.2015.2505959.

- R. Mutlu, T. D. Kumru, "A Zeno paradox: some wellknown nonlinear dopant drift memristor models have infinite resistive switching time," Radioengineering, vol. 32, pp. 312-324, 2023. <u>https://doi.org/10.13164/re.2023.0312.</u>
- 19. E. Gale, "TiO2-based memristors and ReRAM: materials, mechanisms and models (a review)," Semiconductor Science and Technology, vol. 29, 104004, 2014.

https://doi.org/10.1088/0268-1242/29/10/104004.

- V. S. Baghel and S. Akashe, Low power memristor based 7T SRAM using MTCMOS technique," in 2015 Fifth International Conference on Advanced Computing & Communication Technologies, Haryana, India, 2015, pp. 222-226. https://doi.org/10.1109/ACCT.2015.58
- 21. J. Mohr, T. Hennen, D. Bedau et al., "Fabrication of highly resistive NiO thin films for nanoelectronic applications," Advanced Physics Research, vol. 1, 2200008, 2022.

https://doi.org/10.1002/apxr.202200008

 J. Yao, Z. Sun, L. Zhong, D. Natelson, and J. Tour, "Resistive switches and memories from Silicon Oxide," Nano Letters, vol. 10, no. 10, pp. 4105-4110, 2010. https://doi.org/10.1021/nl102255r.

```
    D. H. Kwon, K. M. Kim, J. H. Jang et al., "Atomic
structure of conducting nanofilaments in TiO2 re-
sistive switching memory," Nature Nanotechnol-
ogy, vol. 5, pp. 148-153, 2010.
```

https://doi.org/10.1038/nnano.2009.456.

24. J. J. Yang, M. D. Pickett, X. Li et al., "Memristive switching mechanism for metal/oxide/metal nanodevices," Nature nanotechnology, vol. 3, pp. 429-433, 2008.

https://doi.org/10.1038/nnano.2008.160.

- 25. H. Akinaga, H. Shima, "Resistive random access memory (ReRAM) based on metal oxidess," Proceedings of the IEEE, vol. 98, pp. 2237-2251, 2010. https://doi.org/10.1109/JPROC.2010.2070830.
- R. Waser, M. Aono, "Nanoionics-based resistive switching memories," Nature materials, pp. 833– 840, 2007.

https://doi.org/10.1038/nmat2023

- 27. B. J. Choi, D.S. Jeong, S. K. Kim et al., "Resistive switching mechanism of TiO2 thin films grown by atomic-layer deposition," Journal of Applied Physics, vol. 98, 033715, 2005. https://doi.org/10.1063/1.2001146.
- H. Xie, M. Wang, P. Kurunczi; Y. Erokhin, Q. Liu, et al., "Resistive switching properties of HfO2-based ReRAM with implanted Si/Al ions," AIP Conference Proceedings, American Institute of Physics, vol. 1496, pp. 26-29, 2012.

https://doi.org/10.1063/1.4766481.

- 29. A. A. Sivkov, Y. Xing, Z. Minden et al., "Resistive switching properties of ZrO2 film by plasma-enhanced atomic layer deposition for non-volatile memory applications," Journal of Electronic Materials, vol. 50, pp. 5396-5401, September 2021. https://doi.org/10.1007/s11664-021-09065-6.
- 30. E. Linn, R. Rosezin, C. Kügeler, and R. Waser, "Complementary resistive switches for passive nanocrossbar memories," Nature materials, vol. 9, pp. 403-6, 2010.

https://doi.org/10.1038/nmat2748.

R. Rosezin, E. Linn, L. Nielen, C. Kügeler, R. Bruchhaus, and R. Waser, "Integrated complementary resistive switches for passive high-density nano-crossbar arrays," IEEE Electron Device Letters, vol. 32, pp. 191-193, 2011.

https://doi.org/10.1109/LED.2010.2090127.

- 32. E. Karakulak, R. Mutlu, and E. Ucar, "Sneak path current equivalent circuits and reading margin analysis of complementary resistive switches based 3D stacking crossbar memories," Informacije MIDEM, vol. 44, pp. 235-241, 2014.
- E. Karakulak, R. Mutlu, and E. Ucar, "Reconstructive sensing circuit for complementary resistive switches-based crossbar memories," Turkish Journal of Electrical Engineering & Computer Sciences, vol. 24, pp. 1371-1383, 2016.

https://doi.org/10.3906/elk-1309-71.

34. L. Gao, F. Alibart, and D. B. Strukov, "Programmable CMOS/memristor threshold logic," IEEE Transactions on Nanotechnology, vol. 12, pp. 115-119, 2013. https://doi.org/10.1109/TNANO.2013.2241075.

- 35. C. M. Jung, K. H. Jo, E. S. Lee et al., "Zero-sleepleakage flip-flop circuit with conditional-storing memristor retention latch," IEEE Transactions on Nanotechnology, vol. 11, pp. 360-366, 2012. https://doi.org/10.1109/TNANO.2011.2175943.
- W. Robinett, M. Pickett, J. Borghetti et al., "A memristor-based nonvolatile latch circuit," Nanotechnology, vol. 21, 235203 2010. https://doi.org/10.1088/0957-4484/21/23/235203.
- A. Vishwakarma, K. O. Ampadu, M. Huebner et al., "Memristor-based CMOS hybrid circuit design and analysis," Procedia Computer Science, vol. 218, pp. 563-573, 2023.

https://doi.org/10.1016/j.procs.2023.01.038.

 A. H. Edwards, H. J. Barnaby, K. A. Campbell et al., "Reconfigurable memristive device technologies," Proceedings of the IEEE, vol. 103, pp.1004-1033, 2015.

https://doi.org/10.1109/JPROC.2015.2441752.

- K. H. Jo, C. M. Jung, K.S. Min, and S. M. Kang, "Selfadaptive write circuit for low-power and variation tolerant memristors," IEEE Transactions on Nanotechnology, vol. 9, pp. 675-678, 2010. <u>https://doi.org/10.1109/TNANO.2010.2052108.</u>
- 40. I. Vourkas and G.Ch.Sirakoulis, "Emerging memristor-Based logic circuit design approaches: a review," IEEE Circuits and Systems Magazine, vol. 16, pp. 15-30, 2016. https://doi.org/10.1109/MCAS.2016.2583673.
- 41. F. Z. Wang, N. Helian, S. Wu et al., "Delayed switching in memristors and memristive systems," IEEE Electron Device Letters, vol. 31, pp. 755-757, 2010. https://doi.org/10.1109/LED.2010.2049560.
- 42. Y. Xie, "Modeling, architecture, and applications for emerging memory technologies," IEEE Design & Test of Computers, vol. 28, pp. 44-51, 2011. https://doi.org/10.1109/MDT.2011.20.
- 43. F. Z. Wang, N. Helian, S. Wu et al., "Delayed switching applied to memristor neural networks," Journal of Applied Physics, vol. 111, 07E317, 2012. https://doi.org/10.1063/1.3672409.
- 44. A. Özgüvenç, R. Mutlu, and E. Karakulak, "Sawtooth signal generator with a memristor," in 1st International Conference on Engineering Technology and Applied Sciences, Afyon, Türkiye, 2016, pp. 1-6. https://www.researchgate.net/ publication/305683933_Sawtooth_signal_generator_with_a_memristor
- S. C. Yener, R. Mutlu, T. Yener, and H. H. Kuntman, "Memristor-based timing circuit," in 2017 Electric Electronics, Computer Science, Biomedical Engineerings' Meeting (EBBT), İstanbul, Türkiye, 2017, pp. 1–3.

https://doi.org/10.1109/EBBT.2017.7956776

46. R. Mutlu and E. Karakulak, "A methodology for memristance calculation," Turkish Journal of Elec-

trical Engineering & Computer Sciences, vol. 22, pp. 121-131, 2014.

https://doi.org/10.3906/elk-1205-16.

47. K. M. Kim, J. Zhang, C. Graves et al., "Low-power, self-rectifying, and forming-free memristor with an asymmetric programing voltage for a high-density crossbar application," Nano Letters, vol. 16, pp. 6724–6732, 2016.

https://doi.org/10.1021/acs.nanolett.6b01781.

48. D. Niu, Y. Chen, and Y. Xie, "Low-power dual element memristor based memory design," in Proceedings of the 16th ACM/IEEE international symposium on Low power electronics and design, Austin, Texas, USA, 2010, pp. 25-30.

https://doi.org/10.1145/1840845.1840851.

 X. Guo, E. Ipek, and T. Soyata, "Resistive computation: Avoiding the power wall with low-leakage, STT-MRAM based computing," ACM SIGARCH computer architecture news, vol.38, pp. 371-382, 2010.

https://doi.org/10.1145/1816038.1816012.

- R. Mutlu, "AC power formula for unsaturated TiO2 memristors with linear dopant drift, small signal AC power formula for all memristors, and some applications for these formulas," European J. Eng. App. Sci. (EJEAS), vol. 1, pp. 51 - 58, 2018.
- M. E. Fouda, A. G. Radwan, "Power dissipation of memristor-based relaxation oscillators," Radioengineering, vol. 24, pp. 968-973, 2015. <u>https://doi.org/10.13164/re.2015.0968.</u>
- S. Gazabare, R J. Pieper, W. Wondmagegn, and N. Satyala, "Observations on model based predictions for memristor power dissipation," in 2011 Proceedings of IEEE Southeastcon, pp. 450-454, 2011.

https://doi.org/10.1109/SECON.2011.5752984.

- Y. Ho, G. M. Huang, and P. Li, "Dynamical properties and design analysis for nonvolatile memristor memories," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 58, pp.724-736, 2011. <u>https://doi.org/10.1109/TCSI.2010.2078710.</u>
- 54. S. Vongehr, X. Meng, "The missing memristor has not been found," Scientific Reports, vol. 5, 11657, 2015.

https://doi.org/10.1038/srep11657.

- K. Soni, S. Sahoo, "A review on different memristor modeling and applications," in 2022 International Mobile and Embedded Technology Conference (MECON), Noida, India, 2022, pp. 688-695. https://doi.org/10.1109/MECON53876.2022.9752214.
- 56. Zeno's paradoxes, https://en.wikipedia.org/wiki/ Zeno%27s_paradoxes [accessed on February 17, 2023].
- 57. S.P. Adhikari, M. P. Sah, H. Kim, and L. O. Chua, "Three fingerprints of memristor," IEEE Transac-

tions on Circuits and Systems I: Regular Papers, vol. 60, pp. 3008-3021, 2013.

https://doi.org/10.1109/TCSI.2013.2256171.

 J. Mustafa, R. Waser, "A novel reference scheme for reading passive resistive crossbar memories," IEEE Transactions on Nanotechnology, vol. 5, pp. 687-691, 2006.

https://doi.org/10.1109/TNANO.2006.885016.



Copyright © 2024 by the Authors. This is an open access article distributed under the Creative Com-

mons Attribution (CC BY) License (https://creativecommons.org/licenses/by/4.0/), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Arrived: 05. 12. 2023 Accepted: 29. 02. 2024 https://doi.org/10.33180/InfMIDEM2024.104

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials Vol. 54, No. 1(2024), 39 – 49

Hexagonal Convolutional Neural Network for Noma Rician Channel Estimator using Hexagonal Quadrature Amplitude Modulation

Mohan Dhas Jenish Dev¹, David Judson²

¹Assistant professor, department of Electronics and Communication Engineering, Cape Institute of technology, Rajakrishnapuram, Tamil Nadu, India ²Associate professor, Department of Electronics and Communication Engineering, St. xaviers catholic college of Engineering, Chunkankadai, Nagercoil, Tamil Nadu, India

Abstract: NOMA techniques have attracted much attention due to their ability to support massive connectivity, heterogeneous data traffic, and ultra-low latency requirements, making them ideal for next-generation wireless communication networks. In this paper proposed a novel Hexa CNN for NOMA Rician channel estimator using Hexagonal Quadrature Amplitude Modulation for signal detection and channel estimation (Hexa-QAM). Conventional OFDM-NOMA with HQAM is utilized at the transmitter (tx) side as pilot symbols which inserted to OFDM-NOMA signals to employs the channel estimation (CE) and signal detection advantages of OFDM. Three pilot insertion types Comp, Block, and Hexa were used in the proposed model. The proposed Hexa-QAM can detect the symbols for all users without additional operations based on pilot responses and data signals. However, Hexa CNN is used at the receiver to accomplish a joint flexible signal detection. The Hexagonal Quadrature Amplitude Modulation (Hexa CNN) achieves much better error performance than similar detectors. The Energy Efficiency of the proposed Hexa-QAM technique is 17%, 18%, 23.2%, 23% and 28% better than existing techniques. The accuracy of the proposed technique can be as high as 99.95%, while that of traditional models like the OMA-NOMA, MRC, PD-NOMA and UR-NOMA is 84.9%, 87.58%, and 93.91%, respectively.

Keywords: Orthogonal Frequency Division Multiplexing; Convolutional neural network; Hexagonal Quadrature Amplitude Modulation; Non-Orthogonal Multiple Access

Šestkotno konvolucijsko nevronsko omrežje za ocenjevanje kanala Noma Rician z uporabo šestkotne kvadraturne amplitudne modulacije

Izvleček: Tehnike NOMA so pritegnile veliko pozornosti zaradi svoje zmožnosti podpiranja množične povezljivosti, heterogenega podatkovnega prometa in zahtev po izjemno nizki zakasnitvi, zaradi česar so idealne za brezžična komunikacijska omrežja naslednje generacije. V tem članku je predlagana nova Hexa CNN za ocenjevanje kanala NOMA Rician z uporabo heksagonalne kvadraturne amplitudne modulacije za zaznavanje signalov in ocenjevanje kanala (Hexa-QAM). Konvencionalni OFDM-NOMA s HQAM se uporablja na strani oddajnika (tx) kot pilotni simboli, ki se vstavijo v signale OFDM-NOMA, da se uporabijo prednosti OFDM za ocenjevanje kanala (CE) in zaznavanje signalov. V predlaganem modelu so bili uporabljeni trije tipi vstavljanja pilotnih simbolov: Comp, Block in Hexa. Predlagani Hexa-QAM lahko zazna simbole za vse uporabnike brez dodatnih operacij na podlagi pilotnih odzivov in podatkovnih signalov. Vendar se Hexa CNN uporablja pri sprejemniku, da se doseže skupno prožno zaznavanje signalov. Šestkotna kvadraturna amplitudna modulacija (Hexa CNN) dosega veliko boljšo učinkovitost napak kot podobni detektorji. Energetska učinkovitost predlagane tehnike Hexa-QAM je za 17%, 18%, 23,2%, 23% in 28% boljša od obstoječih tehnik. Natančnost predlagane tehnike je lahko kar 99,95%, medtem ko je natančnost tradicionalnih modelov, kot so OMA-NOMA, MRC, PD-NOMA in UR-NOMA, 84,9%, 87,58% oziroma 93,91%.

Ključne besede: multipleksiranje ortogonalnih frekvenc; konvolucijska nevronska mreža; šestkotna kvadraturna modulacija amplitude; neortogonalen dostop

* Corresponding Author's e-mail: jenishdev56@outlook.com

How to cite:

M. D. J. Dev et al., "Hexagonal Convolutional Neural Network for Noma Rician Channel Estimator using Hexagonal Quadrature Amplitude Modulation", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 54, No. 1 (2024), pp. 39–49

1 Introduction

OFDM (Orthogonal Frequency Division Multiplexing) is a wireless communication modulation technology used to transmit multiple messages over the same band [1]. Multiple orthogonal subcarrier signals with overlapping spectra are delivered in close proximity, with each carrier modulated with bits from the incoming stream to allow multiple bits to be transmitted in parallel [2]. Signal is modulated at a low symbol rate utilizing a standard modulation approach. This retains total data rates comparable to standard single-carrier modulation approaches in the same bandwidth [3].

A multiple access technique called NOMA enables several users to share the same time-frequency resources without interfering with one another's broadcasts [4]. This enables more users to be served with the same amount of bandwidth, making it a viable solution for future wireless communication systems [5]. The ability of NOMA to serve a high number of users while sharing the same time and frequency resources is the primary reason for its implementation in 5G [6]. It provides excellent device performance, efficiency, expanded coverage, low latency, and massive networking [7,8].

CE techniques for OFDM frames based on pilot action plans are under investigation [9,10]. The pilot insertion action plan affects the CE, which is considered in several calculations for both channel evaluation at pilot frequency and channel insertion [11,12]. At the pilot frequency, the channel is estimated using LS and LMS, and the channel is inserted using direct interleaving, which includes a second request, low-pass representation, cubic spline interleaving, and additional spatial timing. [13,14]. Proposed a novel Hexa CNN for NOMA Rician channel estimator using Hexagonal Quadrature Amplitude Modulation for signal detection and CE. The major contribution of the work has been followed by:

- Conventional OFDM-NOMA with HQAM is used on the tx side as pilot symbols that are incorporated into OFDM-NOMA signals to take use of OFDM's CE and signal detection capabilities.
- Three pilot insertion types Comp, Block, and Hexa were used in the proposed model. The proposed Hexa-QAM can detect the symbols for all users without additional operations based on pilot responses and data signals.
- However, Hexa CNN is used at the receiver to accomplish a joint flexible signal detection. The Hexagonal Quadrature Amplitude Modulation (Hexa CNN) achieves much better error performance than similar detectors.

The remaining portion of the work has been followed by Section 2 denotes the literature survey Section 3 denotes the proposed Hexa-QAM methodology 4 denotes the Result and Discussion and the closing remarks are illustrated in section 5

2 Literature review

Recently, a lot of research has been done to address CE in OFDM-NOMA. This section explains the most recent techniques used in this domain.

In 2021 Hadi, M. and Ghazizadeh, R., [15] Created an OMA-NOMA-based approach where the whole bandwidth is split between OMA- and NOMA-based subcarriers to minimize cross-level interference. Simulation results show that in terms of global information throughput performance, the suggested version outperforms the other strategies indexed. In order to optimize the overall cost of an OMA-NOMA-based system, a non-convex optimization problem is developed in which the channel state information (CSI) is not fully understood.

In 2021 Rahdari, F., et al., [16] presented a method that is both easy to use and almost ideal for classifying users in an OFDM-NOMA system. Simulated data indicates that when the variance rises, energy consumption increases more when the distance varies than when the power demand does. One of the most important aspects of such integration, particularly for multimedia communications, is ensuring quality of experience for all connected users.

In 2021 Belmekki, B.E.Y., et al., [17] suggested a maximum ratio combining (MRC) in cooperative VCs transmission systems at road crossings with NOMA. Based on our findings, we determined that using MRC and NOMA is always helpful, even if it means adding complexity to the implementation. Furthermore, 50 percent of all collisions occur at road intersections, making them essential places.

In 2021 Anh, L.T. and Kong, H.Y., et al., [18] developed a power-area (PD-NOMA) system for several users via Nakagami-m fading channels in a multiple energy harvesting (EH) relay networks with hazardous backhaul lines. According to these results, the suggested PD-NOMA machine performs better in terms of customer fairness than the standard orthogonal more than oneget right of entry (OMA) machine. Current concerns include the need for enhanced a high data rate, low latency, network capacity, coverage, and QoS services, which have not been adequately handled.

In 2021 Cogen, F. and Aydin, E., et al., [19] created HQAMQSM, an HQAM assisted QSM approach. In com-

parison to QSM using the QAM scheme, the suggested HQAM-QSM system utilizes less transmission power while offering equal error performance at high SNR. Based on what computer models have shown. Regrettably, battery technology has not advanced as quickly as modern communication technologies. With respect to next-generation communication systems, energy efficiency has become a critical consideration for the reasons mentioned above.

In 2021 Tian, Y., et al., [20] developed for cooperative uplink networks, the opportunistic NOMA (UR-ONO-MA) method based on user relay (AF) amplification and propagation aims to appropriately increase the coverage of high-quality services. Numerical results demonstrate that when remote users have weak channels, the developed UR-ONOMA cooperation outperforms NOMA in terms of error probability and throughput when user relays are not used. Peripheral users located distant from the receiver may encounter peripheral interference and may not be supplied if the transmission channels are really weak, which is one of the drawbacks of ordinary NOMA in the electrical domain.

In 2021 Kazemian, M., et al., [21] proposed an E-NOMA to improve the performance of standard FFT-NOMA in 5G networks. According to simulation findings, the proposed E-NOMA approaches outperform FFT-NOMA in terms of PAPR and BER by around 4.3 dB and 9.5 dB. Furthermore, computational complexity is reduced by at least 56% as compared to a NOMA technique based on SLM NOMA has been identified as a promising method for meeting the rising traffic needs of heterogeneous wireless networks.

In 2021 Ghous, M., et al., [22] Created a MIMO-NOMA cooperative transmission strategy with SWIPT support, which included beam-forming and self-interference. Since data rate fairness and outage performance of cell-edge users are critical challenges in MIMO-NOMA systems, we focus on how to resolve these difficulties. To ensure the correctness of our study, we evaluate the analytical expressions using simulations. We demonstrate how employing antenna diversity at the MIMO-NOMA model near and far end terminals improve the outage performance of cell-edge users.

In 2023 Wang, Z., et al., [23] provide an OFDM system built using carrier frequency offset (CFO) models based on DL. Peer evaluations show that DL-based models can work well for large classes of channels without further training if they are trained with the worst (heaviest) multi-pass channel model. However, the carrier frequency offset between the transmitter and the receiver must be correctly estimated due to the OFDM system's sensitivity to carrier frequency offset. In 2020 Lemayian, J. P., & Hamamreh, J. M et al., [24] suggested an advanced revolutionary small-scale NOMA communication strategy based on physical layer security (PLS) to improve security and reliability for two users. The results show that the proposed model offers less complicated, secure, and efficient communication, making it ideal for applications with low power consumption and restricted computation. Furthermore, according to, the NOMA Energy Domain is no longer a development item in the 3rd Generation Partnership Project (3GPP) and has been deleted from Release 17 due to certain performance degradation problems.

However various literature surveys had been proposed, yet they face challenges like high bit error rate, low energy efficiency, and spectrum efficiency in the system. To overcome these challenges, proposed a novel HEXA-QAM for NOMA Rician channel estimator using Hexagonal Quadrature Amplitude Modulation for signal detection and CE.

3 Proposed RICH-NOMA methodology

In this paper proposed a novel Hexa CNN for NOMA Rician channel estimator using Hexagonal Quadrature Amplitude Modulation for signal detection and channel estimation (Hexa-QAM). OFDM-NOMA signals with inserted pilot symbols are sent to all users via the Rician fading channel. In this research, we employed combtype, block-type, and Hexa-type pilot insertions1, which are three of the most used forms of pilot designs for CE. Based on pilot answers and data signals, the proposed Hexa-QAM can recognize symbols for all users with no further processes. The Hexagonal Quadrature Amplitude Modulation (Hexa CNN) achieves much better error performance than similar detectors.

3.1 Conventional OFDM-NOMA

Traditional OFDM model use an inverse discrete Fourier transform (IDFT) to transform SC symbols independently of pilot insertion after they are serialized and parallelized. Therefore, the symbols for OFDM-NOMA are provided as follows:

$$a(m) = IDFT\{a^{(P)}\} = \sum_{P=1}^{M_c} a^{(P)w^{i(2\pi Pm/M_c)}}$$

M=1,2..., M_c (1)

Here, the SC symbol stream a(m) is before the IDFT. Ns is the frequency domain subcarrier number. In other words, it is the symbol a(p) of the k-th OFDM subcar-

rier. To prevent intercarrier interference (ICI) between OFDM subcarriers, According to CP, an OFDM symbol is represented as:

$$a_{CP}(m) = \begin{cases} a(M_s + m), m = -M_{cp}, -M_{cp} + 1, \dots, -1 \\ a(m), m = 1, \dots, M_c, \end{cases}$$
(2)

Here, the length of CP is represented by M_{cp} . The CP-added OFDM signal is serialized and transmitted on a Rician fading channel. As a result, the user received the following signal:

$$b_{CP_j}(m) = \sqrt{TA_{CP}(m) \otimes g_j(m) + v_j(m)}$$

$$j = 1, 2, \dots M,$$
(3)

Initially, the received signal is transformed from serial to parallel at the receiver in eqn (3), and CP is eliminated.

$$b_i(m) = b_{CPi}(m + M_{CP}), \quad m = 1, 2, \dots, M_c$$
 (4)

After removing the CP, the received signal undergoes a discrete Fourier transform (DFT), followed by (4) to convert the signal to serial format.

$$A_{j}(P) = DFT\{B_{j}(m)\} = \frac{1}{M_{c}} \sum_{m=1}^{M_{c}} B(m) w^{i(2\pi Pm/M_{c})},$$

P=1, 2,..., M_{c} (5)

The signals in (5) are equalized according to the CSIR (eg, complete channel estimate and/or estimated channel).

$$A_{j}(P) = \frac{B_{j}(P)}{G_{j}(P)}, P = 1, 2, \dots, M_{c}$$
 (6)

In which G_j represents G_j s DFT. The UEN sign makes use of a most probability detector, or MLD, to expect its very own alerts due to the fact it's miles given extra power. Prior to predicting their very own alerts, different UEs execute iterative SIC(s). All UEs' detection estimates and diagnosed symbols are indexed as [5].

$$\hat{A}_{j} = \underset{l}{\operatorname{argmin}} \left| A_{j}^{(M-j+1)} - \sqrt{T\alpha_{j}g_{j}A_{j}} \right|^{2}$$

$$I=1,2,\ldots,N,$$
(7)

$$\hat{A}_{j} = \underset{l}{\operatorname{argmin}} \left| A_{j}^{(M-i+1)} - \sqrt{T\alpha_{j}g_{j}A_{j}}, l \right|^{2}$$

$$I=1,2,\ldots,N, \qquad (8)$$

where $A_{j,p}$ illustrates estimated symbol of UEi and \hat{A}_{j} is illustrated in the constellation map. Proposed Hexa-QAM shown in Figure 1.



Figure 1: Proposed Hexa-QAM

3.2 Hexa transmitter & receiver

The cyclic prefix (CP) is eliminated from the received signal at the receiver following its conversion to parallel form. DFT is used to restructure the residual signal, which is subsequently transferred to serial format. Consequently, in order to retrieve two successive OFDM signals plus a data symbol (User(i,D)) at the receiver, a buffer must be utilized. Consequently, a comb interpolation approach may be employed to get a priori knowledge of the channel response of the subcarriers carrying the data symbols, allowing for the acquisition of the whole channel frequency response at each subcarrier location. One interpolation block (INTP) shapes Users(i,P). The rebuilt users (i, P) and users (i, D) are fed into his Hexa-CNN network after the INTP block.

3.2.1 Rician fading channel

Another statistical version that makes the idea that the sign includes components a robust LOS element and a random element is the Rician fading version. The linear course with regular amplitude and segment that runs from the Tx to the Rx is called the LOS element.

$$P = \frac{u^2}{2\sigma^2} \tag{9}$$

 $P = \frac{u^2}{2\sigma^2}$ described as the scale parameter and Ratio of power contributions from line-of-sight paths to other multipaths. The second one, which serves as a scaling factor for the distribution, Ω is the total power from both paths:

$$\Omega = u^2 + 2\sigma^2 \tag{10}$$

 $\Omega = u^2 + 2\sigma^2$ described as the total power obtained across all routes. The function of probability density is

$$u^2 = \frac{P}{1+P}\Omega\tag{11}$$

$$\sigma^2 = \frac{\Omega}{2(1+P)} \tag{12}$$

$$f(a \mid u, \sigma) = \frac{a}{\sigma^2} exp\left(\frac{-(a^2 + u^2)}{2\sigma^2}\right) I_0\left(\frac{au}{\sigma^2}\right)$$
(13)

This leads to the following probability density function:

$$f(a) = \frac{2(P+1)a}{\Omega} \exp\left(-P - \frac{(P+1)a^2}{\Omega}\right) I_0\left(2\sqrt{\frac{P(P+1)}{\Omega}a}\right)$$
(14)

In this case, I_0 is the first-kind modified Bessel function of order zero at 0th order.

3.3 Hexa pilot insertion

The pilot pattern is the location where the pilot is inserted in the OFDM symbol's frequency and time domains. A suitable pilot pattern can improve communication quality and significantly lower CE error. Figure 2 depicts the pilot insertion signals, with occupied circles representing pilot signals and empty circles representing data symbols. Figure 2 (a) represents the Block type, Figure 2 (b) represents the Comb type, Figure 2 (c) represents the Hexa type.

3.3.1 Block type

According to the first model, pilots are placed into each subcarrier of a single OFDM symbol within a specific time frame. Block-type channels can be used when they fade slowly; that is, when the channel remains stationary for a predetermined amount of OFDM symbols. In case the channel noise W is uncorrelated and the time domain channel vector is Gaussian, the frequency domain MMSE estimate may be obtained as follows:

$$H_{MMSE} = HG_{rX}R_{XX}^{-1}X \tag{14}$$

Where $G_{_{PX}}$ and $R_{_{XX}}^{-1}$ are the cross-covariance matrix between r and X and the auto-covariance matrix of X

respectively. R_{XX}^{-1} is the auto-covariance matrix of hand σ^2 represents the noise variance E{|W(k)|2}. The LS estimate, which minimizes $(X - YHr)^H (X - YHr)$ is represented by:

$$H_{LS} = Y^{-1}X \tag{15}$$

When the channel is slowly fading, the channel estimation inside the block can be updated using the decision feedback equalizer at each sub-carrier.

3.3.2 Comb type

In the hybrid-type MIMO-OFDM driver model, the drivers are fed into a set of subcarriers in OFDM notation, with interpolation determining the remaining subcarrier channels. When the channel is fast falling, this form



Figure 2: Hexa Pilot Insertion

of pilot placement is beneficial. In comb pilot channel estimation, the pilot signals Np are uniformly injected into Y(k) using the following equation:

$$Y(k) = Y(mL - l) \tag{16}$$

Where L= number of subcarriers N_p and m is the pilot carrier value. The estimate of the channel at pilot subcarriers based on LS estimation is given by:

$$R_e = \frac{X_p}{Y_p}$$
, k=0, 1, ... N_p-1 (17)

Where $X_p(k)$ and $Y_p(k)$ are the output and input at the kth pilot sub-carrier respectively.

3.3.3 Hexagonal quadrature amplitude modulation type (Hexa)

Existing deep learning frameworks, such as TensorFlow, PyTorch, and Caffe, are efficient and are often updated by open-source developers to improve efficiency. Rather than developing Hexa CNN from the ground up, we built it using the Tensor Flow framework, using its core libraries and external Eigen library to preserve Hexa CNN's broad applicability. In this sense, constructing Hexa CNN models of various neural network architectures on Hexa CNN is analogous to implementing rectangle CNN models of various structures on Tensor-Flow. As a result, Hexa CNN serves as a foundation for developing Hexa CNN models, which are CNN models that accept hexagonal inputs directly. The tensor in TensorFlow is rectangle-shaped, hence all tensor-related procedures must be recast for hexagonal processing. TensorFlow's input is rectangular. In compared to other hexagon-imitation models, Hexa CNN saves storage space for input and filters.

Figure 3 displays the illustration of hexagonal constellations for various values of N = 8, 16, 32, 64, 128 and 256. This image illustrates how HQAM constellations might reduce transmitted power when symbol separation is present and perhaps address the energy-efficiency issue.

Typically, two integers, i and j, are used to parameterize hexagonal constellation points.

$$(x_{p}y_{p}) = \sqrt{\rho} \left((x_{0}, y_{0}) + j_{p}(1, 0) + i_{p}\left(\frac{1}{2}, \frac{\sqrt{3}}{2}\right) \right)$$
 (18)

In this case, $(d_{min} = \sqrt{\rho})$, the smallest distance between neighboring constellation points, can be used to denote $\sqrt{\rho}$. The phrase (x_0, y_0) is chosen with the goal of reducing the highest energy. Note that there is no change at all in the properties of hexagonal coordinates when they are rotated orthogonally. Additionally, the maximum energy E_{max} and the average energy E_{avg} according to the aforementioned formulas can be obtained as follows.

$$E_{avg} \triangleq \frac{\rho}{N} \sum_{p=1}^{N} \left(\left(x_0 + j_p + \frac{i_p}{2} \right) \left(y_0 + i_p \frac{\sqrt{3}}{2} \right) \right)^2$$
(19)

$$E_{max} \triangleq \rho \max_{p} \left(\left(x_0 + j_p + \frac{i_p}{2} \right), \left(y_0 + i_p \frac{\sqrt{3}}{2} \right) \right)^2 \quad (20)$$

Where p=1,2,...,N, Additionally, by utilizing these expressions, a comparison between different HQAM constellation approach and traditional QAM constellations will provide a clearer understanding of the energy-efficiency of HQAM. As is commonly understood from communication theory, this point's power is expressed

as $|X_p|^2 = x^2 + y^2$. Given the assumption of equal probability for each symbol in the constellation.

$$T_{avg} = \frac{1}{N} \sum_{p=1}^{N} |X_T|^2$$
(21)

CFM is a metric for evaluating constellation quality. Each constellation that performs better than the other constellations is the one with the larger CFM formula is:

$$\xi = \frac{d_{min}^2}{T_{avg}} \tag{22}$$



Figure 3: Hexa constellations for M = 8, 16, 64 128 and 256

3.4 Deep learning based Hexa CNN

The Hexa CNN approach improves outcomes while maintaining the same power assumption. Hexa CNN is a sort of regularized feed-forward neural network that learns feature engineering by improving filters. The adoption of regularized weights across fewer connections eliminates vanishing and expanding gradients found in previous neural networks during back propagation.



Figure 4: Architecture of Hexa CNN

As represent in Fig 4, the convolutional layer (CL) of the Hexa CNN. The data components in CV reflect channel communication, which is a two-dimensional array whereas the kernel filter. As seen in (23), the convolution filter in our proposed CNN model is effectively a 1-D mean filter:

$$\overline{a} = \frac{1}{m} \sum_{x=1}^{m} a_x \tag{23}$$

where xi represents the ith time sample and n is the total number of samples used to determine the mean.

$$N \times \left\{ \frac{\left(M - W_s\right)}{stp} + 1 \right\}$$
(24)

The window size (WS) is expressed (in samples). WS is set to 128 samples in this article. One second is the equivalent of this window with a sampling rate of 128.

5trails × 14 channels × 129 averaged time samples (25)

The RMS value of each row's elements is extracted by the second layer, Pooling layer_1, inside a window size of WP = 64, as per equation (26):

$$A_{RMS} = \sqrt{\frac{1}{m} \sum_{x=1}^{m} a_{sx}^2}$$
(26)

where n represent the chosen window size, which is 64, and xci is the ith element in the convolution layer's output. Sample sizes are shrunk by a factor of 64, and the

Pooling layer's output size may be expressed as follows:

$$N \times \left(M_2 - W_q\right) + 1 \tag{27}$$

where Wp is the pooling layer window size and N2 is the convolutional layer's column size. Each class's final feature matrix is 5 by 14 and is translated into a 1-D vector with 70 samples.

4 Result and discussion

In this result section evaluates and compares the performance of the proposed Hexa-QAM. The proposed HEXA-QAM was evaluated with different performance measures based on CE. For implementation, the Network Simulator (NS2) was used, which had 4-GB RAM and an Intel Core processor. Regarding, Accuracy, Recall, sensitivity, Precision and Specificity.

Table 1; Simulation parameters

Parameters	Specifications
Carrier Frequency	4 GHz
Number of active carriers	256
Pilot Ratio	64 pilots or 8 pilots
Number of subcarriers	64
Guard type	Cyclic extension
Bandwidth	17.5 kHz
Signal constellation	16QAM, BPSK
Channel Model	Rician Fading Channel
power allocation factor (PAF)	PAF are chosen as β 1=0.15=15% for the user of a strong channel.
Number of subcarriers	50
cp length	16,8
learning rate	0.01
Training sample	320000

We simulate the performance of the new strategy and compare it to traditional schemes. The OFDM system parameters employed in our simulation are listed in Table 1.

4.1 Performance Metrics

The following statistical characteristics are used to analyze the classification strategy's effectiveness: accuracy, precision, specificity, sensitivity, and recall.

Figure 5 demonstrates the performance of the proposed model better than the other methods. The accuracy of the proposed technique can be as high as 99.95%, while that of traditional models like the OMA-

NOMA, MRC, PD-NOMA and UR-NOMA is 85.32, 84.9%, 87.58%, and 93.91%, respectively. The accuracy of the proposed approach improved by 14.63, 16.09%, 13.8%, and 3.75% when compared to the existing methods, respectively.



Figure 5: Performance metrics via Existing

4.2 Computational time

Table 2 compares the computation time recommended with the currently used conventional approach.

Table 2: Comparison of Computational Time

Methods	Computational Time (CT)
ANN	0.952
RNN	0.84
DNN	0.621
Proposed HEXA-QAM	0.38

The time required by the suggested approach is 0.38 seconds, whereas the computational complexity reached by the current methods is 0.952 seconds, 0.84 seconds, 0.621 seconds for ANN, RNN, and DNN, respectively. The computational time comparison reveals that the suggested Hexa CNN has less complexity than the current approaches.



Figure 6: Channel Frequency Response

Figure 6 depicts the channel frequency response of subcarriers in an OFDM symbol at multipath numbers 2 and 6, respectively, at cellular speeds of 0 and 350 km/h. The graphic shows how multipath can produce fading in the frequency domain. Fading grows as the number of multipath pathways increases.



Figure 7: Sub carrier in an OFDM symbol

The suggested HEXA-QAM regression is depicted in Figure 7. Pilots are inserted in the frequency and temporal domains with insertion intervals f=2, t=2, SNR=10 dB, multipath number L=5, and travel speed v=350 km/h in this simulation experiment.



Figure 8: Rician Fading Distribution Outage Probability

The suggested HEXA-QAM can forecast the channel frequency response accurately, and its robustness is proved by its ability to overlook outliers, i.e., pilot samples with high noise. The solid line represents the suggested RICH-NOMA method interpolation, the dotted line represents the entire estimation result unaffected by simulation noise, and the asterisk represents the projected channel response at the pilot point using the LS approach.

The outage probability variation over the Rician fading distribution is seen in Fig. 8. For HEXA-QAM, the outage probability is computed based on the quantity of interfering signals. One may compute the outage prob-

ability by ranging between 1 and 10. In this case, the likelihood of an outage decreases for both users as it increases.



Figure 9: (a) Transmitter Signal(b) Received Signal

The two-frequency signal used to deliver the Rician Fading signal is seen in Figures 9 (a) and (b). An investigation of a simulation model for the Rician Fading channel is performed. In this scenario, the multipath signal comes at a distinct time and frequency.



Figure 10: Block Type

This causes Rician Fading on the output side of the envelope detector. The BER performances of four-consumer HEXA-QAM with excellent pilot insertion methods are shown in Fig. 9 to underline the importance of the pilot insertion strategies. In terms of BER performance, Fig. 10 shows that the RICH-NOMA with block type insertion outperforms the existing.



Figure 11: Comb Type



Figure 12: Hexa Type

Although it is a mixed CE and detection strategy that may outperforms the existing, the encouraged RICH-NOMA with comb-like pilot insertion outperforms it significantly Figure 11 and 12.



Figure 13: Sum data rate vs. number of users.

Figure 13 illustrates the potential aggregate data rate for different network systems vs the total number of users at each base station. More users at each base station result in increased intra-cell interference because of the channel's considerable route loss. However, in terms of OMA-NOMA, MRC, PD-NOMA, and UR-NOMA, the suggested RICH-NOMA outperforms existing systems.



Figure 14: Energy Efficiency

As can be seen in Fig. 14, all approaches exhibit an increase in energy efficiency as SNR increases. The proposed Hexa-QAM scheme outperformed the existing OMA-NOMA, MRC, PD-NOMA, and UR-NOMA, approach in terms of EE. The EE of the proposed Hexa-QAM method is17%, 18%, 23.2%,23% and 28 % better than existing techniques.

5 Conclusions

In this paper proposed a novel Hexa CNN for NOMA Rician channel estimator using Hexagonal Quadrature Amplitude Modulation for signal detection and channel estimation (Hexa-QAM). In this proposed model contains three pilot insertion types Comp, Block, and Hexa were used in the proposed model. The proposed Hexa-QAM can detect the symbols for all users without additional operations based on pilot responses and data signals. However, Hexa CNN is used at the receiver to accomplish a joint flexible signal detection. The Hexagonal Quadrature Amplitude Modulation (Hexa CNN) achieves much better error performance than similar detectors. The proposed Hexa-QAM scheme outperformed the existing OMA-NOMA, MRC, PD-NOMA, and UR-NOMA, approach in terms of energy efficiency. The EE of the proposed Hexa-QAM technique is 17%, 18%, 23.2%, 23% and 28% better than existing techniques. The accuracy of the proposed technique can be as high as 99.95%, while that of traditional models like the OMA-NOMA, MRC, PD-NOMA and UR-NOMA is 85.32%, 84.9%, 87.58%, and 93.91%, respectively. The accuracy of the proposed approach improved by 14.63%, 16.09%, 13.8%, and 3.75% when compared to the existing methods, respectively. The proposed Hexa-QAM model has a shortcoming in that it does not account for multi-ownership. This constraint will be regarded as a future task to expand our proposed system. The limitation of the proposed Hexa-QAM model does not handle the multi-owner nature. This limitation will be considered as a future work for extending our proposed system. In the future, we will consider employing artificial intelligence approaches to optimize each user's power allotment and improve the performance of the NOMA method.

6 Acknowledgments

The authors would like to thank the reviewers for all of their careful, constructive and insightful comments in relation to this work.

7 Conflict of Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

8 References

- 1. S. Alimi, O.D. Alao and Q.A. Mumuni, An overview of orthogonal frequency division multiplexing principles, architecture, and its application. *Global Journal of Engineering and Technology Advances*, vol. *12*, no. 1, pp. 120-130 2022.
- 2. G.A. Abed, A New Approach to Improve Transmitting and Receiving Timing in Orthogonal Frequency Division Multiplexing (OFDM) Systems. *Iraqi Journal For Computer Science and Mathematics*, vol. 4, no. 2, pp. 83-96, 2023.
- A.A. Patil, C.M. Jadhao, S.S. Mhaske and R.R. Karhe, Performance Analysis of Adaptive Modulation and Coding Over AWGN Channel in an OFDM System. *International Journal of Research in Engineering, Science and Management*, vol. 6, no.5, pp. 72-78, 2023.
- R. Kanthavel, R. Dhaya, and A. Ahilan, Al-Based Efficient WUGS Network Channel Modeling and Clustered Cooperative Communication. ACM Transactions on Sensor Networks, vol. 18, no. 3, 2022.
- Krishna Bikram Shah, S. Visalakshi and Ranjit Panigrahi, Seven class solid waste management-hybrid features based deep neural network, International Journal of System Design and Computing, vol. 01, no.01, pp. 1-10, 2023.
- M. Prabhu, B. Muthu Kumar, and A. Ahilan, Slime Mould Algorithm based Fuzzy Linear CFO Estimation in Wireless Sensor Networks. IETE Journal of Research, 1-11, 2023.

- M. Amanullakhan, M. Usha and S. Ramesh, Intrusion Detection Architecture (IDA) In IOT Based Security System, International Journal of Computer and Engineering Optimization, Vol. 01, no. 01, pp. 33-42, 2023.
- A. Sayed, M. Khatun, T. Ahmed, A.A. Piya, P. Chakraborty and T. Choudhury, Performance analysis of OFDM system on multipath fading and inter symbol interference (ISI) using AWGN. In *Computational Intelligence in Pattern Recognition: Proceedings of CIPR 2021* Springer Singapore. pp. 25-36, 2022.
- 9. M.J.M. Ameen and S.S. Hreshee, Securing Physical Layer of 5G Wireless Network System over GFDM Using Linear Precoding Algorithm for Massive MIMO and Hyperchaotic QRDecomposition. *International Journal of Intelligent Engineering & Systems*, vol. 15, no. 5, 2022.
- 10. K.S. Ali, E. Hossain and M.J. Hossain, Partial nonorthogonal multiple access (NOMA) in downlink poisson networks. *IEEE Transactions on Wireless Communications*, vol. *19*, no. 11, pp. 7637-7652, 2020.
- M. F. Zia, and J. M. Hamamreh, An Advanced Non-Orthogonal Multiple Access Security Technique for Future Wireless Communication Networks. RS Open Journal on Innovative Communication Technologies, vol. 1, no. 2, 2020.
- M. Abewa, and J. M. Hamamreh, Multi-User Auxiliary Signal Superposition Transmission (MU-AS-ST) for Secure and Low-Complexity Multiple Access Communications. RS Open Journal on Innovative Communication Technologies, vol. 2, no. 4, 2021.
- M. F. Zia, H. M. Furqan, and J. M. Hamamreh, Multicell, Multi-user, and Multi-carrier Secure Communication Using Non-Orthogonal Signals' Superposition with Dual-Transmission for IoT in 6G and Beyond. RS Open Journal on Innovative Communication Technologies, vol. 2, no. 3, 2021.
- J. M. Hamamreh, M. Abewa, and J. P. Lemayian, New Non-Orthogonal Transmission Schemes for Achieving Highly Efficient, Reliable, and Secure Multi-User Communications. RS Open Journal on Innovative Communication Technologies, vol. 1, no. 2, 2020.
- M. Hadi and R. Ghazizadeh, Joint sub-carrier allocation and 3D beamforming design in OMA-NOMA based mmWave heterogeneous networks under channel uncertainties. *AEU-International Journal of Electronics and Communications*, vol. 137, pp. 153809, 2021.
- F. Rahdari, N. Movahhedinia, M.R. Khayyambashi and S. Valaee, QoE-aware power control and user grouping in Cognitive Radio OFDM–NOMA systems. *Computer Networks*, vol. 189, pp. 107906, 2021.

- 17. B.E.Y. Belmekki, A. Hamza and B. Escrig, On the performance of cooperative NOMA Using MRC at road intersections in the presence of interference. *Physical Communication*, vol. 46 pp. 101321, 2021.
- 18. L.T. Anh and H.Y. Kong, Multi-User PD-NOMA with unreliable backhaul links in a multiple EH relay network over Nakagami-m fading channels. *Physical Communication*, vol. 47, pp. 101351, 2021.
- 19. F. Cogen and E. Aydin. Performance analysis of Hexagonal QAM constellations on quadrature spatial modulation with perfect and imperfect channel estimation. *Physical Communication*, vol. 47, pp. 10137, 2021.
- 20. Y. Tian, B. Xiao, X. Wang, Y.H. Kho and C. Tian, Performance analysis of opportunistic NOMA strategy in uplink coordinated multi-points systems. *Computer Communications*, vol. 177 pp. 207-212, 2021.
- 21. M. Kazemian, J. Abouei and A. Anpalagan, A low complexity enhanced-NOMA scheme to reduce inter-user interference, BER and PAPR in 5G wire-less systems. *Physical Communication*, vol. 48, pp. 101412, 2021.
- 22. M. Ghous, A.K. Hassan, Z.H. Abbas and G. Abbas, Modeling and analysis of self-interference impaired two-user cooperative MIMO-NOMA system. *Physical Communication*, vol. 48, pp. 101441, 2021.
- 23. Z. Wang, S. Wei, L. Zou, F. Liao, W. Lang and Y. Li, Deep-Learning-Based Carrier Frequency Offset Estimation and Its Cross-Evaluation in Multiple-Channel Models. *Information*, vol. 14, no. 2, pp. 98, 2023.
- 24. J. P. Lemayian, and J. M. Hamamreh, A Novel Small-Scale Nonorthogonal Communication Technique Using Auxiliary Signal Superposition with Enhanced Security for Future Wireless Networks. RS Open Journal on Innovative Communication Technologies, vol. 1, no. 2, 2020.

 $(\mathbf{\hat{I}})$ (cc) BY

Copyright © 2024 by the Authors. This is an open access article distributed under the Creative Com-

mons Attribution (CC BY) License (https://creativecommons.org/licenses/by/4.0/), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Arrived: 22. 11. 2023 Accepted: 03. 03. 2024

https://doi.org/10.33180/InfMIDEM2024.105

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials Vol. 54, No. 1(2024), 51 – 63

Fault Diagnosis of Asymmetric Cascaded Multilevel Inverter using Ensemble Machine Learning

Kavitha Rangasamy

Department of Electrical and Electronics Engineering, Kumaraguru College of Technology, Coimbatore, Tamilnadu, India

Abstract: Cascaded Multi-Level Inverters (CMLI) are used in a wide range of high-power industrial drives and for integrating solar PV system. Asymmetric Cascaded Multilevel Inverter (ACMLI) produces an output voltage with reduced Total Harmonic Distortion (THD) when compared to Symmetric Cascaded Multilevel Inverter (SCMLI). ACMLI comprises of more semiconductor devices and thus reliability is a major concern. Efficient, high speed and precise fault detection is required for ACMLI to reduce failure rates and avoid unplanned shutdown. RMS voltage, mean voltage and THD under various single and double switch fault conditions are used as features for fault diagnosis. Fault diagnosis method for ACMLI based on probabilistic principal component analysis (PPCA) and Ensemble Machine Learning (EML) is presented. PPCA is used to optimize data and reduce the size of fault features. Finally, an EML classifier combining Support Vector Machine (SVM), K-Nearest Neighborhood (KNN) and Decision Tree (DT) is employed to diagnose the various open circuit faults. The proposed fault diagnosis method is validated using an experimental setup. The simulation and experimental result shows that EML technique diagnosis the fault with 99.32% accuracy.

Keywords: Multilevel Inverter; fault; Principal Component Analysis (PCA); SVM; Ensemble Machine Learning

Diagnostika napak asimetričnega kaskadnega večnivojskega pretvornika z uporabo skupinskega strojnega učenja

Izvleček: Kaskadni večnivojski pretvorniki (CMLI) se uporabljajo v številnih visokozmogljivih industrijskih pogonih in za integracijo fotonapetostnega sistema. Asimetrični kaskadni večnivojski pretvornik (ACMLI) proizvaja izhodno napetost z manjšim skupnim harmonskim popačenjem (THD) v primerjavi s simetričnim kaskadnim večnivojskim pretvornikom (SCMLI). ACMLI vsebuje več polprevodniških naprav. Za ACMLI je potrebno učinkovito, hitro in natančno odkrivanje napak, da se zmanjša število okvar in prepreči nenačrtovana zaustavitev. Napetost RMS, srednja napetost in THD pri različnih okvarah z enim in dvema stikaloma se uporabljajo kot značilnosti za diagnosticiranje okvar. Predstavljena je metoda diagnosticiranja napak za ACMLI, ki temelji na verjetnostni analizi glavnih komponent (PPCA) in skupinskem strojnem učenju (EML). PPCA se uporablja za optimizacijo podatkov in zmanjšanje velikosti značilnosti napak. Za diagnosticiranje različnih napak odprtega tokokroga je uporabljen klasifikator EML, ki združuje podporni vektorski stroj (SVM), K-najbližje sosedstvo (KNN) in odločitveno drevo (DT). Predlagana metoda za diagnosticiranje napak je potrjena z eksperimentalno postavitvijo. Simulacija in eksperimentalni rezultati kažejo, da tehnika EML diagnosticira okvare z 99,32-odstotno natančnostjo.

Ključne besede: večnivojski pretvornik; napaka; analiza glavnih komponent (PCA); SVM; skupinsko strojno učenje

* Corresponding Author's e-mail: kavithain2@gmail.com

How to cite:

K. Rangasamy, "Fault Diagnosis of Asymmetric Cascaded Multilevel Inverter using Ensemble Machine Learning", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 54, No. 1(2024), pp. 51–63

1 Introduction

CMLI is one of the most prominent converter topologies for renewable energy-based distribution system and high-power industrial drive applications because of its excellent scalability, low harmonic distortions, modular topology, and high efficiency [1]. As the number of voltage steps at output terminals increases, harmonic distortion reduces. However, this inherently leads to an increase in the number of power semiconductor devices [2]. ACMLI topology in natural sequence ratio (1:2:3) provides a higher number of voltage levels with the symmetrical arrangement of power semiconductor switching devices. Reduced number of dc sources, high-speed capabilities, minimal switching loss, and high conversion efficiency are the prominent advantages of the ACMLI topology. The circuit topology becomes more complicated when the number of Hbridge cells grows exponentially, and thus the possibility of a power semiconductor device failure increases, resulting in abnormal working circumstances [3].

Short Circuit Fault (SCF) and Open Circuit Fault (OCF) in semiconductor devices are the general types of faults in power devices and account for 38% of errors. Short circuit faults happen in short duration and are extremely destructive, which causes serious impacts. SCF's are transformed into OCF by a fast-acting fuse. OCF degrades inverter performance, distorts the output currents, and causes considerable risk of secondary faults in the load, grid, and converter systems. While applying CMLI to PV systems, if CMLI faults remain unidentified on time, it adversely impacts reliability, and even triggers fires. Hence, it becomes essential to design and develop intelligent fault diagnosis system to provide reliable operation of ACMLI systems [4-8].

Fault diagnostic approaches are based on current and voltage-based methods. Current based method detects OC faults through the phase current, and current residual [9]. The voltage-based fault diagnosis approach locates the fault by combining the output voltage and the diagnosis model. Line voltage error-based method is proposed for open circuit faults; however, it requires higher sampling time. The open switch faults are detected using a Fourier series and a histogram of the trajectory of voltage [10].

The data-driven fault detection method extracts voltage signals and applies signal processing methods and classification algorithms. This method provides attractive solutions due to the progress in Machine Learning (ML) algorithms and computation capability [11-12]. Fast Fourier Transform (FFT) with a hidden Markov model provides slower response in defect detection due to the sophisticated matrix operations [13]. The defect diagnostic approach for a three-level inverter utilizing a Back Propagation Neural network (BPN) and genetic algorithm is presented [14]. FFT analysis is employed to extract fault information, relative PCA and support vector machine (SVM) are employed to diagnose OCFs for SCMLI [15]. PCA and Multiclass-Relevance Vector Machine (MRVM) are applied to lower the facet of the OCF in symmetric CMLI [16].

The approach incorporates the grey wolf algorithm linked with enhanced SVM technology. The methodology uses the grey wolf algorithm to optimize the SVM parameters [17]. SVM and KNN with PPCA are used to detect the OCF under different fault circumstances in a CMLI. The SVM based fault analysis technique is effective and presents 97.6% accuracy with 70% training dataset [18].

Sparse representation with deep convolutional neural networks (DCNNs) is applied to provide an intelligent fault detection method for CMLI. By harnessing the beneficial characteristics of both approaches, the technique aims to improve defect identification efficiency and accuracy [19].

Different ML techniques, like KNN, SVM and Naive Bayesian classifier are applied. THD, RMS and mean voltage, and harmonics up-to 12th order are considered as characteristic features. The classification accuracy achieved using CMLI is 95.56%, and that of Packed Ucell (PUC) inverters is 94.28% [20]. Affine-Invariant Riemannian Metric Autoencoder Random Forest (AIRMAR) is proposed to recognize OCF in MLI [21].

To enhance the features for classification, this model employs a short-time Fourier transform (STFT), that generates a time-frequency image. Multiscale Kernel Convolution Neural Network (MKCNN) is employed that utilizes the benefits of 2D images to capture the spatial relations among diverse features. MKCNN is compared with the Back Propagation Neural Network (BPN) and CNN [22].

The shift in pole voltage when a fault occurs is investigated and Rolling average of pole voltage is extracted. Pole voltage categories and reference voltage are the input characteristics for a decision tree classifier to identify single and double switch OCF [23].

An Adaptive Hilbert-Huang filter using Scale-Invariant Feature Transform (SIFT) with a Convolution Neural Network (CNN) classifier is employed [24]. Artificial neural network (ANN) is used to detect and diagnose faults in both binary and trinary configurations in an ACMLI [25]. Most of the literature has addressed fault diagnosis in SCMLI topology, and only very few have focused on fault diagnosis in ACMLI topology. The following are the primary contributions of the paper: (i) Developing an ML based fault diagnosis technique with greater classification accuracy that detects both single and double switch fault scenarios (ii). The proposed technique can be extended for fault diagnosis of any CMLI configuration (iii) Simulation of the ACMLI has been performed in both normal and faulty conditions. (iv) Experimental implementation of the proposed technique is validated for single and double switch fault classification in ACMLI.



2 Fault diagnosis system

Figure 1: Structure of fault diagnosis system

Fig. 1 depicts the structure of a fault diagnosis system. The following four major states build up the system: 1) Feature extraction and dimension reduction; 2) Neural Network based fault classification; 3) Fault diagnosis; 4) Switching pattern reconfiguration. The voltage input signal transformation is performed to extract essential characteristics, and the output is directed to neural network classification. The network is trained with normal scenario and fault scenario, and each matching output is assigned a binary label.

FFT is a digital signal processing microchip implementation approach. FFT approach has a strong identity feature that allows it to distinguish between normal and irregular fault signals. The precisely assembled information in fig. 2. lays the foundation for developing a reliable fault identification and diagnosis system. The features used for fault classification are: FFT, RMS voltage (Vrms), mean voltage (Vmean), THD and harmonics (up-to 19th order). These values are obtained under normal, single switch fault, double switch fault conditions. Mean voltage indicates a shift and change in symmetrical pattern during faulty condition. RMS voltage provides information on the reduction in peak value due to fault. THD and lower order dominant harmonics (up-to 19th) are considered as they reveal the distortion in waveform shape.



Figure 2: Flow chart of fault diagnosis system

3 ACMLI

The single-phase thirteen-level ACMLI is shown in Fig. 3. The ACMLI has three H-Bridge modules and 12 power switching semiconductors, and three dc voltage sources supplied with values of Vdc: 2Vdc: 3Vdc. Vdc of 50V,

100V, and 150V are provided to produce a peak voltage of 300V. Each MOSFET switch is identified based on the bridge location (A, B, or C), as SA1, SA2, SB1, SB2, and so on. In natural sequence ACMLI, N-1 number of MOS-FET's are required for an L-level, and thus thirteen-level inverter requires 12 MOSFETs. The output voltage progresses in the levels of 1Vdc, 2Vdc, 3Vdc, 4Vdc... 13 Vdc. The switching sequence of ACMLI is presented in Table I. ACMLI is more susceptible to switch malfunctions as it has more semiconductor switches.



Figure 3: Circuit diagram of ACMLI

Table 1: Switching sequence of ACMLI.

	0	Vdc						-Vdc					
	0	1	2	3	4	5	6	1	2	3	4	5	6
SA1	1	1	1	1	1	1	1	0	0	0	0	0	0
SA2	0	1	0	1	0	1	1	0	1	1	0	1	0
SA3	1	0	1	0	1	0	0	1	0	0	1	0	1
SA4	0	0	0	0	0	0	0	1	1	1	1	1	1
SB1	1	1	1	1	1	1	1	0	0	0	0	0	0
SB2	0	0	1	0	0	1	1	1	0	1	1	0	0
SB3	1	1	0	1	1	0	0	0	1	0	0	1	1
SB4	0	0	0	0	0	0	0	1	1	1	1	1	1
SC1	1	1	1	1	1	1	1	0	0	0	0	0	0
SC2	0	0	0	1	1	1	1	1	1	0	0	0	0
SC3	1	1	1	0	0	0	0	0	0	1	1	1	1
SC4	0	0	0	0	0	0	0	1	1	1	1	1	1



Figure 4: Output and individual H-Bridge voltage waveform during fault conditions in ACMLI: (a) Normal condition (b) Single switch fault (c) Two switch fault in same H-Bridge cell (d) Two switch fault in different H-Bridge cell

4 Fault in ACMLI

Simple fault in ACMLI is single MOSFET malfunctioning at an instant of time, and intricate fault is two or more MOSFET malfunctioning concurrently. This paper deals with simple as well as intricate fault diagnosis. The most difficult aspect of fault detection is obtaining additional information to distinguish between comparable defects in distinct switches.

Twelve single switch faults, sixty-three double switch faults, and three input source faults are examined for validating the proposed method as shown in Table 2.

Fig .4(a) illustrates the output waveform of the ACMLI without any flaws, and distinct waveforms obtained in each H-Bridge cell. In the positive cycle, conduction takes place through switches Sn1 and Sn2 whereas in negative cycle, conduction takes place through Sn3 and Sn4 with n generalized as n=a, b, c.

Case (i) Single switch fault: The fault is located in switch SC2, thus voltage in the positive cycle of H-Bridge cell 3 is zero as shown in fig.4(b). This fault does not permit the source Vdc3 to pervade through it. Hence in H-bridge cell 3, level 3Vdc is lost which causes variation of voltage profile in positive cycle whereas the negative cycle remains unaffected.

Case (ii) Two switch faults in same H-Bridge cell: The fault is located in switches SB2 and SB3 in the same H-Bridge cell 2, thus it affects the flow of current in both positive and negative cycle. As observed in fig. 4(c), this scenario does not allow both half cycles and yields symmetrical variation of output voltage profile in both the cycles.

Case (iii) Two switch faults in different H-Bridge cells: The fault is located in switches of different H-Bridge cells, namely switches SA3 and SB2. This event triggers an asymmetrical variation in output voltage profile as shown in fig. 4(d). The condition (SA3 fault) does not permit voltage Vdc1 to pass through in negative cycle and voltage (SB2 fault) does not permit Vdc2 in positive half cycle.

Table 2	: Switching	sequence	of	ACMLI
---------	-------------	----------	----	-------

Type of faults	Labels
Healthy	1
single switch fault	2 to 13
Double switch fault	14 to 76
Input source fault	77 to 79
Total Number of samples	1183



Figure 5: RMS voltage and THD for various Fault switch condition (FSC): (a) RMS voltage (b) THD (%) (c) mean voltage.

The fault case scenarios are labelled as follows: Healthy (1), single switch fault (2 to 13), and double switch fault (14 to 76), and input source fault (77 to 79) as shown in Table 2. The values are decoded into binary form and provided as the label for fault classification. Thus, a total of 1183 samples are provided with 948 for training and 235 for testing data set.

RMS voltage, mean voltage, lower order harmonics and THD are recorded which serve as data set for various single and double OCF fault conditions. From fig.5(a) and fig.5(b) it is observed that certain faults result in similar values of RMS voltage and THD. Thus, it is nec-









q) input source fault2

Figure 6: Simulation results of output voltage under various fault switch condition

essary to consider the mean voltage shown in fig.5(c), which shows variation in polarity and amplitude under fault conditions. The mean voltage serves as a rich indicator of type and location of faults.

Simulation results of output voltage waveform for various types of single OCF are presented in fig.6(a) to (f), double switch OCF is given in fig.6(g) to (o), and input source fault is shown in fig. 6(p) to (r). Both even and odd harmonics are considered as the waveform is asymmetrical in most fault cases.

As observed in fig 6(c) and 6(d), the voltage waveforms during SB3 switch fault and SB2 switch fault are complement to each other with similar value of RMS voltage and THD. SB2 switch failure shown in fig. 6(c) causes a faulty voltage waveform with reduction in peak voltage in the positive cycle, with a negative mean voltage of 25.48V. SB3 switch fault causes a similar effect with reduction in voltage in the negative cycle as shown in fig. 6(d) and results in positive mean voltage (+25.48 V.) Hence, the polarity of mean voltage alone varies for SB2 and SB3 fault.

Single switch fault (SA1, SA4), (SA2, SA3), (SB1, SB4), (SB2, SB3), (SC1, SC4), (SC2, SC3) result in similar RMS voltage and THD as shown in fig.5 (a) and (b) with variation in mean voltage as shown in Fig.5(c).

As indicated in fig.5(c) double switch faults in certain scenario causes variation of mean voltage alone. For instance, the double switch (SC1 and SC3), (SC2 and SC4) results in similar value of RMS voltage and THD. However, the mean voltage varies in polarity as (-7.62, +7.62) respectively.

Thus, in some fault scenarios, though Vrms and THD are similar, the mean voltage exhibits a change in voltage polarity or magnitude, which serves as an essential feature for fault identification.

The system identifies the label or switches in which fault had happened. Only from the labels, label 1 is classified as no fault, label 2-13 is classified as single switch fault and labels 14 to 76 is classified as double switch fault. Fault classes 77 to 79 are identified as input source faults.

5 Data Preprocessing

FFT profile (up to 19th harmonics) are taken and PPCA is applied to extract essential information and reduce the dimensionality of data. The PPCA method is used to transform a group of correlated data into a lower-dimensional set. PPCA iteratively refines the model pa-

rameters to maximize the likelihood of the actual data. By mapping data onto a lower-dimensional substructure, it retains most of the original data's variation. The aim of PCA is to find a set of principal components that captures the most variance information.

The flow chart of fault diagnosis is represented in fig. 2. The PPCA relates the actual variable with reduced dimension latent variable which induces a corresponding distribution in the data space and given by Eq. (1)

$$h = U_{LM}H + \mu + \varepsilon \tag{1}$$

H is the latent variable principal score of reduced dimension harmonics and ϵ is multivariate Gaussian error rate, μ the mean vector, ULM is the linear transformation matrix determined by maximum likelihood techniques.

The procedure is described as follows:

- i) Input harmonics h_{d*q} and error(ϵ) where P and R are orthogonal matrices.
- ii) Determine the empirical mean of harmonics using Eq. (2) and co-variance using Eq. (3)

$$h_m = \frac{1}{q} \sum_{i=1}^{q} h_i \tag{2}$$

$$A = \frac{1}{\sqrt{q}} \left[\left(h_1 - h_m \right), \left(h_2 - h_m \right), \dots, \left(h_q - h_m \right) \right] \quad (3)$$

- iii) Decompose A as $A = PDR^{T}$ where D is the Diagonal matrix
- iv) Find Eigen values $\lambda_1, \lambda_2 \dots \lambda_r$ using a diagonal matrix D = diag (d₁, d₂, ... d_r) r = min (d, b) with d1 ≥ d2 ... ≥ dr
- v) Arrange eigen values in descending order; $\lambda \ j \geq \lambda \ j+1$

where $(1 \le 1 \dots \le d - 1)$, $\lambda_i^2 = d_i^2 (1 \le i \dots \le \min(d, q))$ for j=1 to d-1 do Pj = Rj,1

vi) Calculate Reconstruction error based on Eq. (4)

$$Q = \frac{1}{q} \sum_{i=1}^{q} ||h_i - P_j P_i^T (h_i - h_m) - h_m ||^2 \quad (4)$$

If $Q < \varepsilon$ then b=j; j=d-1

vii) Find variance and orthogonal matrix of maximum likelihood by Eq. (5) and (6) respectively

$$\sigma_{ML}^2 = \frac{1}{d-q} \sum_{i=q+1}^d \lambda_i \tag{5}$$

$$P_{ML} = P_q \sqrt{\left(\Lambda_q - \sigma^2 P I_q\right)} \tag{6}$$

The reduced dimensional output matrix of the PPCA is the first five eigen values represented by $H = [\lambda_1, \lambda_2]$ $\lambda_{s}],$ ULM is the linear transformation matrix decided by maximum likelihood techniques, μ the mean vector.

6 Machine learning algorithms

6.1 Support vector machine (SVM)

Support Vector Machine (SVM) is primarily employed for regression and classification problems. It functions exceptionally well in circumstances where exacerbated boundaries for decision-making are to be established. The goal of SVM is to split the data points into separate fault categories and optimize the distance between fault classes.

The reduced dimension matrix x_i is $x_i = [Vmean, Vrms, THD, H]$ where $H = [\lambda_1, \lambda_2...\lambda_5]$ is obtained by PPCA and yi is the output fault classification [1, 2,.....79] associated with each xi. x_i represents data point variables necessary for fault classification of Fi. Arbitrary hyperplane is characterized as a series of points meeting hyperplane as given in Eq. (7)

$$W^{\circ}x_{i} - b = 0 \tag{7}$$

where $^{\circ}$ is scalar product; W is weight/normal vector perpendicular to plane; b is the bias.

W= (w1, w2 ... wp) and $x_i = (xi1, xi2 ..., xip)$, the scalar product is represented in Eq. (8)

$$w_{\circ}xi = \sum_{i=1}^{P} w_{j}x_{ij}$$
(8)

The most important part of SVM method is to obtain weight vector (w) and bias value b such that hyperplane equation specified by Eq. (1) maximizes the margin between fault classes. The offset of maximum-margin hyperplane is b / ||W|| and ||W|| denotes the length of vector W. The goal is to find the hyperplane that separates fault classes with minimum error. For a maximum margin hyperplane to compute the support vector on either side the optimization problem is formulated as Eq. (9)

$$\min \frac{1}{2} \|\mathbf{W}\|^{2} + C \sum_{i=1}^{p} \xi_{i} y_{i} (w.\Phi(x_{i}) + b \ge 1 - \xi_{i} \quad (9)$$

$$\xi_{i} \ge 0$$

C is the regularization parameter to avoid overfitting and ξ is the slack variable which measures error made at point (xi, yi,)), ϕ is the function that transforms x_i from p to q dimensions. The harmonic measurement is too close, so Kernel function K is used to denote the proximity between samples xi and xj. The Lagrange multiplier is used to determine the weight vector w and bias b from the solution ai as shown in Eq. (10)

$$max \sum_{i=1}^{N} \alpha_i - \frac{1}{2} \sum_{i,j=1}^{N} y_i y_j \alpha_i \alpha_j K(x_i, x_j)$$
(10)

RBF kernel (where $\sigma > 0$ is a user defined parameter) is given by Eq. (11)

$$K(x_i, x_j) = \exp \frac{||x_i - x_j||^2}{2\sigma^2}$$
 (11)

6.2 KNN (K nearest neighborhood)

KNN is an instance-based technique that classifies new data points through groups based on the group which has the greatest number of members among its nearest neighborhoods. KNN establishes prediction based on correlations with adjacent points instead of specifically learning a model. The KNN is based on the Euclidean distance between xi and yi. SVM performance is vulnerable to the regularization parameter (C) and kernel parameters whereas KNN effectiveness depends on the selection of K and the distance metric. The Euclidean distance with n number of training samples is computed by Eq. (12)

$$\sum_{i=1}^{N} |x_i - y_i|^2$$
 (12)

The KNN algorithm is implemented as follows:

- Calculate the distance between x_new and x using the distance metric. Store the distances and their corresponding indices.
- Choose K Neighborhoods based on the calculated distances. Count the occurrences of each class among the K neighbors. Determine the fault class with the highest occurrence rate as the predicted fault class for X_new.

6.3 Decision tree (DT)

Decision Tree continuously splits the feature set into sections to generate a hierarchical tree-like decisionmaking framework. Every internal node point in a decision tree is based on the characteristics [Vmean, Vrms, THD, H]. To reduce the variance, the most effective characteristic is selected, which divides the data at every node. The process persists until a stopping criterion, namely tree depth is met. The designing parameters of DT are entropy and Gini Index (GI), samples in the leaf (minimum), depth of the tree, and the splitter. Entropy and GI are more responsive to node probability changes.

For each feature:

(i) Calculate the impurity of the current node using an entropy using Eq. (13)

$$Entrophy(S) = \sum_{i=1}^{n} P_i log_2 P_i$$
(13)

where Pi is the probability of fault classes, S is the case set and n is the number of fault classes.

(ii) Calculate information gain that indicates the reduction in impurity using Eq. (14)

Gain = Impurity Before Split - Weighted Average Impurity after Split

$$Gain = Entrophy(S) - \sum_{i=1}^{n} \frac{S_i}{S} Entrophy(S_i)$$
(14)

S-Sample of entire fault input Si-Sample input of ith fault class

- (iii) Select the feature with the highest information gain as the splitting attribute.
- (iv) Create a root node with the selected feature. For each possible value of the selected feature: Create a child node. Recursively apply the algorithm to the subset of training data corresponding to that value and the remaining features. Attach the child node to the root node. Return to the constructed Decision Tree.
- (v) Compute information gain for each feature and choose the feature with the highest gain.

DT follows numerous paths if their input information is slightly modified. Reliability and stability are essential in fault identification. During the validation of the proposed fault analysis technique, single and double switch OCF classes are exactly diagnosed, and the faulty MOSFETs are located with an accuracy of 99.32 %.

6.4 Extreme machine learning

To improve the performance of fault diagnosis, a bagged ensemble learning algorithm is employed. Bagging refers to an ensemble technique that generates multiple base models by training each on a bootstrapped sample of the data (randomly selected dataset with replacement). Ensemble Learning with three predictive algorithms namely SVM, KNN and decision tree are employed in this paper. The prediction from each base model is then selected by majority voting techniques, where classification is done based on the fault class with maximum number of votes as shown in fig.7.



Figure 7: Flow chart of Ensemble Learning

7 Experimental results

The experimental platform of a thirteen-level inverter shown in fig.8. is established with MOSFET. In addition, the FFT spectrum of the output voltage of the ACMLI was computed by DSP TMS320F28034 controller. An open-circuit fault was created by removing the gate signal, and the voltage under faulty condition is measured.



Figure 8: Experimental Model

The voltage signals are then processed using DSP, harmonics and THD are computed by employing FFT. The mean average voltage of ac waveform is computed by sampling the ac voltage over a period and computing the mean value digitally.

The experimental data set is obtained for 1183 data samples, of which 948 are used as training data, and the remaining 235 are taken as testing data.

From Fig. 9(a) –(d), it is evident that noise impact in experimental data is high when fault condition is performed in real-time hardware. Ensemble learning is suitable for this category as it lowers the variance within a noisy dataset and yields higher accuracy, when compared to other ML techniques. In the experimental setup, healthy, OCF, input source faults are examined. The OCF is established by removing the gate signal from the related switch. Many samples of the output voltage are taken for the same fault condition to provide complete insight into the fault classes.

Fig. 9(a) indicates the output voltage waveform for the healthy class without fault. Fig. 9(b) and 9(c) indicate single and double switch faulty instance taken from the experiment. During fault in switches SC3 and SC2 in different legs of the H-Bridge the levels vary multiple times in the same instance as shown in fig 9(b) which is similar to the simulation result shown in fig. 6(i). During simultaneous failure of switches SC1 and SC4 in the same leg, one or more voltage levels are missed as shown in fig.9(c). Fault in the input source of H-bridge 2 results in three-level waveform as shown in fig. 9(d) which is in correlation with the simulation result shown in fig. 6(q).

To eliminate randomness, each method was repeated ten times, and the averaged results are obtained. The parameters given in Eq. (15) - (18) are computed for all the proposed methods. Accuracy provides the correctness of predictions. Precision reveals the accuracy of positive predictions, and recall implies the capability of the model to correctly identify all positive instances. The F1 score is the harmonic mean of precision and recall. Specificity provides models with the ability to correctly identify negative instances.

Accuracy
$$\frac{TP + TN}{TP + TN + FP + FN}$$
 (15)

$$Precision = \frac{TP}{TP + FP}$$
(16)

$$Recall = \frac{TP}{TP + FN}$$
(17)

$$F1 = \frac{2^* Precision^* Recall}{Precision + Recall}$$
(18)

It is observed from Table 3 that SVM is superior in performance. KNN suffers from the issue of overfitting and thus classifies the fault with a relatively low accuracy of 95.54%. Decision trees when used alone, have the lowest accuracy as it is not benefited by ensemble techniques that use numerous decision trees or ML algorithms to boost accuracy.

Thus, bagging technique EML is applied, and accuracy rate of fault diagnosis is 99.32% with the training set and test set in the ratio of 80%: 20%. The results reveal the fact that EML classifier using PPCA dimensionality reduction achieve fault classification with strong characteristic information and high classification accuracy. In order to validate EML the results are compared with existing literature which is presented in Table 4.

Further online fault detection requires high-performance computation with rapid decision making. Fast diagnosis of faults requires Raspberry Pi with a dualcore Arm Cortex-M0+ processor for training of machine learning algorithms. In real time if any of the H-bridges in the system fail, the faulty H-bridge is bypassed and switching pattern reconfiguration is performed to operate the system with reduced THD and balanced voltage in positive and negative half cycle. Additional Hbridge cells with relay circuits are employed as auxiliary sources to clear the fault in real time. Auxiliary H-bridge cells and chopper circuit that generate dc voltage in a 1:2:3 ratio is employed as redundant circuits. In case of fault, the H-bridge can be disconnected, and auxiliary H-bridge cells and voltage of the chopper can be connected through a relay circuit.

SVM KNN DT ELM 97.9 95.54 91.77 **Training Accuracy** 99.32 Testing Accuracy 96.58 94.44 88.91 98.74 Precision 97.40 93.02 90.51 99.20 Recall 95.74 95.54 89.78 98.41 F1 Score 96.57 94.26 89.82 98.80 97.44 93.44 90.37 Specificity 99.12

Table 3: Parameters obtained in ML Techniques

8 Conclusion

This article presents ELM machine learning for single and double switch open circuit fault diagnosis in AC-MLI. Simulation and experimental data sets of many samples are taken, which enhance fault features and

ANN Techniques	Тороlоду	Techniques	Number of levels	Accuracy
PCA-BP [22]	Symmetric CMLI	FFT-	5-level	88.7%
RPCA-SVM [15]	Symmetric CMLI	FFT	5-level	92.5%
PPCA-SVM [18]	Symmetric CMLI	FFT	5-level	97.6%
DCNN [19]	Symmetric CMLI	Image processing	5-level	98.16%
Combined Optimizer Fault Classifier [20]	Symmetric CMLI	FFT	5-level	95.56%
AIRMAR [21]	Symmetric (Nested Neutral Point Piloted) MLI	Image processing	5-level	99.33%
Multiscale Kernel CNN [22]	Symmetric CMLI	Short-time Fouri-er transform (STFT)	15-level	98.3%
Mean Voltage Decision trees [23]	Neutral Point Clamped MLI	Pole voltage sign	11-level	98.14%
CSA optimized CNN [24]	Symmetric CMLI	Mean and RMS voltage, THD	9-level	99.84%
BPN [25]	Asymmetric CMLI	Mean and RMS volt- age, THD	7-level and 9-level	99.771%
Proposed Method	Asymmetric CMLI	Mean and RMS volt- age, THD	13-level	98.74%

Table 4: Comparison with Existing literatures

improve the accuracy of fault diagnosis. This paper identifies that faults in different switches in certain scenarios yield identical Vrms and THD values. Thus, it is necessary to take into consideration the mean voltage and FFT harmonic spectrum from (2nd to 19th). Dimensionality technique PPCA is applied to reduce the dimension of harmonics and trace the most significant features in the dataset.

Machine Learning algorithms namely SVM, KNN and DT are applied individually for fault diagnosis in ACMLI, and their performance is analyzed. ML algorithms SVM,



Figure 9: Experimental Results: (a) Normal condition (b) Fault in switch SC3 and SC2 (c) Fault in switch SC1 and SC4 (d) Fault in input source2

KNN and DT are then linked together by a bagging ML approach with maximum voting technique termed as Ensemble Machine Learning (EML). Simulation and experimental investigations are carried out to validate the performance of EML in ACMLI. The experimental results show an accurate categorization rate of 99.32%. ELM provides lower variance within a noisy dataset and thus yields higher accuracy when compared to SVM, KNN and DT algorithms. The study demonstrates that EML classifier with PPCA dimensionality reduction technique achieves the highest classification accuracy in fault diagnosis of ACMLI. The potential limitation of the study is input source fault, and double switch fault in the same leg results in similar kind of fault. To overcome this limitation, additional voltage sensors can be provided to individual input sources to detect source fault. Further research may also be carried out on fault diagnosis based on image processing of the output voltage waveform.

9 References

- Leon, Jose I., Sergio Vazquez, and Leopoldo G. Franquelo. "Multilevel converters: Control and modulation techniques for their operation and industrial applications." Proceedings of the IEEE 105, no. 11 (2017): 2066-2081. https://doi.org/10.1109/JPROC.2017.2726583
- B. N. Rao, Y. Suresh, A. K. Panda, B. S. Naik and V. Jammala, "Development of cascaded multilevel inverter based active power filter with reduced transformers," in CPSS Transactions on Power Electronics and Applications, vol. 5, no. 2, pp. 147-157, June 2020,

https://doi.org/10.24295/CPSSTPEA.2020.00013

- Babaei, E., Kangarlu, M. F., & Mazgar, F. N. (2012). Symmetric and asymmetric multilevel inverter topologies with reduced switching devices. Electric Power Systems Research, 86, 122-130. <u>https://doi.org/10.1016/j.epsr.2011.12.013</u>
- A. A. Stonier and B. Lehman, "An Intelligent-Based Fault-Tolerant System for Solar-Fed Cascaded Multilevel Inverters," in *IEEE Transactions on Energy Conversion*, vol. 33, no. 3, pp. 1047-1057, Sept. 2018, doi: 10.1109/TEC.2017.2786299. https://doi.org/10.1109/TEC.2017.2786299
- Choi, U. M., Blaabjerg, F., & Lee, K. B. (2014). Study and handling methods of power IGBT module failures in power electronic converter systems. IEEE Transactions on Power Electronics, 30(5), 2517-2533.

https://doi.org/10.1109/TPEL.2014.2373390

 S. Khomfoi, L. Tolbert, Fault diagnosis system for a multilevel inverter using a neural network, IEEE Trans. Power Electron. 22 (2007) 1062–1069, https://doi.org/10.1109/TPEL.2007.897128

- Jung, S. M., Park, J. S., Kim, H. W., Cho, K. Y., & Youn, M. J. (2012). An MRAS-based diagnosis of opencircuit fault in PWM voltage-source inverters for PM synchronous motor drive systems. IEEE Transactions on Power Electronics, 28(5), 2514-2526. <u>https://doi.org/10.1109/TPEL.2012.2212916</u>
- Mellit, Adel, Giuseppe Marco Tina, and Soteris A. Kalogirou. "Fault detection and diagnosis methods for photovoltaic systems: A review." Renewable and Sustainable Energy Reviews 91 (2018): 1-17.

https://doi.org/10.1016/j.rser.2018.03.062

 Reyes-Malanche, J. A., Villalobos-Pina, F. J., Cabal -Yepez, E., Alvarez-Salas, R., & Rodriguez-Donate, C. (2021). Open-Circuit Fault Diagnosis in Power Inverters Through Currents Analysis in Time Domain. IEEE Transactions on Instrumentation and Measurement, 70, 1-12.

https://doi.org/10.1109/TIM.2021.3082325

- Zhang, Weiwei, and Yigang He. "A hypothesis method for T-type three-level inverters opencircuit fault diagnosis based on output phase voltage model." IEEE Transactions on Power Electronics (2022). Power Electron., vol. 30, no. 12, pp. 7006–7018, Dec. 2015 https://doi.org/10.1109/TPEL.2022.3151731
- 11. B. Cai, Y. Zhao, H. Liu, and M. Xie, "A data-driven fault diagnosis methodology in three-phase inverters for PMSM drive systems," IEEE Trans. Power Electron., vol. 32, no. 7, pp. 5590–5600, Jul. 2017. https://doi.org/10.1109/TPEL.2016.2608842
- 12. Xia, Y., & Xu, Y. (2021). A transferrable data-driven method for IGBT open-circuit fault diagnosis in three-phase inverters. IEEE Transactions on Power Electronics, 36(12), 13478-13488. <u>https://doi.org/10.1109/TPEL.2021.3088889</u>
- 13. Zheng, H., Wang, R., Wang, Y., & Zhu, W. (2017, July). Fault diagnosis of photovoltaic inverters using hidden Markov model. In 2017 36th Chinese Control Conference (CCC) (pp. 7290-7295). IEEE. https://doi.org/10.23919/ChiCC.2017.8028508
- 14. Wu, Xun, Chun-Yang Chen, Te-Fang Chen, Shu Cheng, Zhi-Hong Mao, Tian-Jian Yu, and Kaidi Li. "A fast and robust diagnostic method for multiple open-circuit faults of voltage-source inverters through line voltage magnitudes analysis." IEEE Transactions on Power Electronics 35, no. 5 (2019): 5205-5220.

https://doi.org/10.1109/TPEL.2019.2941480

 T.Z. Wang, J. Qi, H. Xu, Y.D. Wang, L. Liu, D.J. Gao, Fault diagnosis method based on FFT-RPCA-SVM for Cascaded-Multilevel Inverter, ISA Trans. 60 (2016) 156–163, <u>https://doi.org/10.1016/j.isatra.2015.11.018</u> Wang, Tianzhen, Hao Xu, Jingang Han, Elhoussin Elbouchikhi, and Mohamed El Hachemi Benbouzid. "Cascaded H-bridge multilevel inverter system fault diagnosis using a PCA and multiclass relevance vector machine approach." IEEE Transactions on Power Electronics 30, no. 12 (2015): 7006-7018.

https://doi.org/10.1109/TPEL.2015.2393373

- Yuan, Q., Tu, Q., Yan, L., & Xia, K. (2023). Fault diagnosis of H-bridge cascaded five-level inverter based on improved support vector machine with gray wolf algorithm. Energy Reports, 9, 485-495. <u>https://doi.org/10.1016/j.egyr.2023.03.017</u>
- Ali, Murad, Zakiud Din, Evgeny Solomin, Khalid Mehmood Cheema, Ahmad H. Milyani, and Zhiyuan Che. "Open switch fault diagnosis of cascade H-bridge multi-level inverter in distributed power generators by machine learning algorithms." Energy Reports 7 (2021): 8929-8942. https://doi.org/10.1016/j.egyr.2021.11.058
- Du, B., He, Y., & Zhang, C. (2021). Intelligent diagnosis of cascaded H-bridge multilevel inverter combining sparse representation and deep convolutional neural networks. IET Power Electronics, 14(6), 1121-1137. https://doi.org/10.1049/pel2.12094
- Sudha, V., K. Vijayarekha, Rakesh Kumar Sidharthan, and Natarajan Prabaharan. "Combined Optimizer for Automatic Design of Machine Learning-Based Fault Classifier for Multilevel Inverters." IEEE Access 10 (2022): 121096-121108. https://doi.org/10.1109/ACCESS.2022.3193784
- Ye, S., Zhang, F., Gao, F., Zhou, Z., & Yang, Y. (2022). Fault diagnosis for multilevel converters based on an affine-invariant riemannian metric autoencoder. IEEE Transactions on Industrial Informatics, 19(3), 2619-2628.

https://doi.org/10.1109/TII.2022.3186992

- A. Sivapriya, N. Kalaiarasi, R. Verma, B. Chokkalingam and J. L. Munda, "Fault Diagnosis of Cascaded Multilevel Inverter Using Multiscale Kernel Convolutional Neural Network," in IEEE Access, vol. 11, pp. 79513-79530, 2023, doi: 10.1109/AC-CESS.2023.3299852. https://doi.org/10.1109/ACCESS.2023.3299852
- Rinsha, V., & Jagadanand, G. (2023). Rolling Average-Decision Tree-Based Fault Detection of Neutral Point Clamped Inverters. IEEE Journal of Emerging and Selected Topics in Industrial Electronics, vol. 4, no. 3, pp. 744-755. <u>https://doi.org/10.1109/JESTIE.2023.3236587</u>
- 24. Sivapriya, A., & Kalaiarasi, N. (2023). A Novel Enhanced Deep Learning-Based Fault Diagnosis Approach for Cascaded Multilevel Inverter. e-Prime-

Advances in Electrical Engineering, Electronics and Energy, 100253.

https://doi.org/10.1016/j.prime.2023.100253

 Raj, N., Jagadanand, G., & George, S. (2018). Fault detection and diagnosis in asymmetric multilevel inverter using artificial neural network. International Journal of Electronics, 105(4), 559-571. <u>https://doi.org/10.1080/00207217.2017.1378382</u>



Copyright © 2024 by the Authors. This is an open access article distributed under the Creative Com-

mons Attribution (CC BY) License (https://creativecommons.org/licenses/by/4.0/), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Arrived: 12. 10. 2023 Accepted: 10. 03. 2024

https://doi.org/10.33180/InfMIDEM2024.106

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials Vol. 54, No. 1(2024), 65 – 73

Analysis and Mitigation of Negative Differential Resistance Effects with Hetero-gate Dielectric Layer in Negative-capacitance Field-effect Transistors

Honglei Huo¹, Weifeng Lü¹, Xinfeng Zheng¹, Yubin Wang¹, Shuaiwei Zhao¹

¹School of Microelectronics, Hangzhou Dianzi University, Hangzhou, Zhejiang, China

Abstract: Negative-capacitance field-effect transistors (NCFETs) show promise as low-power devices for the next-generation. However, the negative differential resistance (NDR) effects are inherent in NCFET and adversely affect the design of integrated devices and circuits. In this study, a hetero-gate dielectric NCFET (HGD-NCFET) is proposed and investigated. The HGD-NCFET is formed by partially replacing the ferroelectric layer of NCFET with a high-dielectric constant (high- κ) material on the drain side to inhibit its NDR effects. The Sentaurus technology computer-aided design simulations demonstrate that the out conductance (G_{DS}), which is used to quantify the NDR effects, increases monotonically as a function of the length of high- κ material (L_{HK}), and G_{DS} eventually tends to zero in HGD-NCFET. In addition, the other electrical parameters of the HGD-NCFET remained almost unchanged compared to those of the original NCFET.

Keywords: negative differential resistance; negative-capacitance field-effect transistor; high-dielectric constant; hetero-gate dielectric

Analiza in ublažitev učinkov negativne diferencialne upornosti s hetero-vratno dielektrično plastjo v poljskih tranzistorjih z negativno kapacitivnostjo

Izvleček: Tranzistorji z negativno kapacitivnostjo (NCFET) so obetavni kot naprave z nizko porabo energije za naslednjo generacijo. Vendar so učinki negativne diferencialne upornosti (NDR) značilni za NCFET in negativno vplivajo na načrtovanje integriranih naprav in vezij. V tej študiji je predlagan in raziskan dielektrični hetero-vratni NCFET (HGD-NCFET). HGD-NCFET je oblikovan z delno zamenjavo feroelektrične plasti NCFET z materialom z visoko dielektrično konstanto (high-κ) na ponorni strani, da se zavirajo učinki NDR. Simulacije računalniško podprtega načrtovanja s tehnologijo Sentaurus kažejo, da se izhodna prevodnost (G_{DS}), ki se uporablja za količinsko opredelitev učinkov NDR, monotono povečuje v odvisnosti od dolžine materiala z visokim κ (L_{HK}), G_{DS} pa se v HGD-NCFET sčasoma približuje ničli. Poleg tega so ostali električni parametri HGD-NCFET skoraj nespremenjeni v primerjavi s prvotnim NCFET.

Ključne besede: negativna diferencialna upornost; poljski tranzistor z negativno kapacitivnostjo; visoka dielektrična konstanta; heterovratni dielektrik

* Corresponding Author's e-mail: lvwf@hdu.edu.cn

How to cite:

H. Huo et al, "Analysis and Mitigation of Negative Differential Resistance Effects with Hetero-gate Dielectric Layer in Negative-capacitance Field-effect Transistors", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 54, No. 1(2024), pp. 65–73

1 Introduction

Reducing the power consumption density has become one of the main research hotspots following the continuous miniaturization of silicon-based integrated circuits. However, the subthreshold swing (SS) of traditional metal-oxide-semiconductor field-effect transistors (MOSFETs) is difficult to break through 60 mV/decade at room temperature owing to basic thermodynamic limitations; thus, the scaling of the power supply voltage is limited [1,2]. Owing to the negative capacitance effects of the ferroelectric materials, negative-capacitance field-effect transistors (NCFETs) can amplify the internal gate voltage (V_{iN}) . This successfully overcomes Boltzmann's SS limitation at 60 mV/ decade, thus resulting in reduced power consumption [3-7]. Therefore, NCFETs are regarded as promising candidates for next-generation low-power devices due to their exceptional performance, including steep SS, high-switching current ratio (I_{ON}/I_{OFF}) , and compatibility with standard the complementary metal-oxide-semiconductor (CMOS) manufacturing processes. Nevertheless, NCFETs exhibit negative differential resistance (NDR) effects at lower gate voltages.

The NDR effects in NCFET originate from the coupling of the drain voltage ($V_{\rm DS}$) to $V_{\rm IN}$ via the gate–drain capacitance (C_{GD}) , which results in current loss [8,9]. Although the NDR effects are advantageous in oscillator circuits [10,11], their presence may result hysteresis in the voltage transfer characteristics of logical gates, thus leading to larger noise margins [12,13]. This is due to the fact that the transfer characteristic curves of NMOS and PMOS intersect three times resulting in two steady states of the inverters at the same input voltage, with one value for each of the forward and reverse voltage sweeps, leading to hysteresis. Meanwhile, due to the unstable saturation current of the analogue amplifier[14], the application of NCFET to an analogue circuit may result in a change in the circuit's operating point. This alteration may lead to changes in the amplification characteristics, frequency response, and linear range of the circuit, resulting in non-linear distortion. This distortion may cause additional energy conversion between different components in the circuits, leading to increased power consumption. Therefore, suppression of the NDR effects is a necessary and urgent task. Several methods have been proposed to address this issue, such as the use of oxide-layer-trapped charge through electron injection [15], adjustment of the coupling capacitance between the gate and drain [16], and the use of local Gaussian heavy doping on the drain side [17]. However, these solutions require hot-carrier injection or complex manufacturing processes.

In this study, we propose an approach to suppress the

NDR effects by partly replacing the ferroelectric layer of the traditional NCFET with a high-dielectric constant (high- κ) material (HfO₂) on the drain side. It is shown that with an increase in the HfO₂ length (L_{HK}), the electrostatic potential of the channel increased at low-gate voltages, and the NDR effects are obviously reduced.

2 Structure and modeling of heterogate dielectric NCFET (HGD-NCFET)

In this study, the NCFET used fully depleted silicon-oninsulator (FDSOI) technology. The process parameters for the device are listed in Table 1. The ferroelectric layer of the NCFET was replaced with a high-k material (HfO₂) on the drain side, forming the HGD-NCFET. The structure of a typical HGD-NCFET device is shown in Fig. 1(a). Fig. 1(b) depicts the calibrated transfer characteristic curve $(I_{DS}-V_{GS})$ for the baseline FDSOI device with the experimental data at the 14 nm node [18]. The fabrication process flow of the HGD-NCFET is shown in Fig. 2. The manufacturing process for HGD-NCFET is essentially the same as that for conventional NCFET with few additional process step or cost. To demonstrate the physical characteristics of NCFET more accurately, the high-field saturation, Fermi, Shockley Read Hall model, Slotboom model of band gap narrowing, eQuantum Potential, doping dependence, and Landau-Khalatnikov model were included in the Sentautus technology computer-aided design (TCAD) simulations [19]. Although TCAD models aim to accurately represent physical processes, they are still based on approximations and simplifications. This can result in discrepancies between simulated and actual device behavior, particularly under extreme conditions or for new materials and structures. Ferroelectric materials have a non-centrosymmetric crystal structure in which spontaneous displacement of atoms leads to non-zero spontaneous polarisation. The relationship between electric field and polarisation (P) in ferroelectrics can be expressed as $E_{FF} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho (dP/dt)$, where α , β , and y are parameters of the ferroelectric material. Then we can establish the correlation between the voltage $V_{\rm FF}$ at the ferroelectric terminals and the thickness of the attached point as $V_{FE} = T_{FE} \times (2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho(dP/dP^3))$ dt)). Then $Q=P+\varepsilon E\approx P$, and the ferroelectric capacitance (C_{EF}) can be expressed as follows [20]:

$$C_{\rm FE} = \frac{dQ}{dV_{\rm FE}} \approx \frac{1}{2\alpha \times T_{\rm FE}} = \frac{2}{3\sqrt{3}} \times \frac{P_{\rm r}}{E_{\rm C} T_{\rm FE}}$$
(1)

where P_r and E_c are the remanent polarization and coercive fields of the ferroelectric materials, respectively. Since α is negative, the $C_{\rm FE}$ is negative. Fig. 1(c) displays the equivalent capacitance circuit of the NCFET. Herein, $C_{\rm FE}$ and $C_{\rm MOS}$ represent the capacitances of the ferroelectric layer and the underlying FD-SOI, respectively. $C_{\rm MOS}$ is equivalent to the source capacitance ($C_{\rm S}$), drain capacitance ($C_{\rm D}$), oxide capacitance ($C_{\rm OX}$), and hafnium dioxide capacitance ($C_{\rm HFO2}$). Similar to the gate voltage, the drain voltage is coupled to the internal node through the gate-drain capacitance ($C_{\rm GD}$). Equivalent circuits controlled by the gate and drain are shown in Fig. 1(d). The NDR effects in the NCFET are closely related to the capacitance matching between $C_{\rm FE}$ and $C_{\rm MOS}$, as well as $C_{\rm GD}$. The differential gain ($A_{\rm V}$) and drain coupling factor ($\xi_{\rm D}$) of the NCFET are given as follows [10]

$$A_{\rm V} = \frac{dV_{\rm IN}}{dV_{\rm GS}} = \frac{C_{\rm FE}}{C_{\rm FE} + C_{\rm GS} + C_{\rm GD}} = \frac{C_{\rm FE}}{C_{\rm FE} + C_{\rm MOS}}$$
(2)

$$\xi_{\rm D} = \frac{dV_{\rm IN}}{dV_{\rm DS}} = \frac{C_{\rm GD}}{C_{\rm FE} + C_{\rm GS} + C_{\rm GD}} = \frac{C_{\rm GD}}{C_{\rm FE} + C_{\rm MOS}}$$
(3)

To ensure the stable operation of NCFET without hysteresis, the absolute value of C_{FE} must be greater than $C_{\text{MOS}'}$ that is, $C_{\text{FE}} + C_{\text{MOS}} < 0$ [21,22]. As NCFET stabilizes in the negative capacitance region ($C_{\text{FE}} < 0$), this results in $A_{\text{V}} \ge 1$ and $\xi_{\text{D}} < 0$.

Table 1: Structural parameter of the NCFET device.

Baseline structure	Value
Burrier oxide thickness	10 nm
(T _{BOX})	
Gate length (L _G)	12 nm
Insulator thickness (T _{ox})	Oxide/HfO2 0.5 /1.2 nm
Channel thickness (T _{CH})	5 nm
Source/Drain doping	$2 \times 10^{20} \text{ cm}^{-3}$
Channel doping	$1 \times 10^{15} \text{cm}^{-3}$
Coercive field (E _c)	1×10^{6} V/cm
Remanent polarization (P _r)	$5 \times 10^{-6} \text{C/cm}^2$



Figure 2: Fabrication process flow of hetero-gate dielectric negative-capacitance field-effect transistors.

3 Results and analysis

3.1 Analysis of NDR effects

The NDR effects occurred in the saturated region, and the drain current (I_{DS}) decreased when V_{DS} increased. This resulted in a negative output conductance (G_{DS}) in the NCFET. By taking the derivative of the output current $I_{DS} = f(V_{IN}, V_{DS})$ using the chain derivative rules, the G_{DS} of the NCFET can be obtained as follows [10],

$$\frac{dI_{\rm DS}}{dV_{\rm DS}} = \frac{\partial I_{\rm DS}}{\partial V_{\rm IN}} \frac{dV_{\rm IN}}{dV_{\rm DS}} + \frac{\partial I_{\rm DS}}{\partial V_{\rm DS}}$$
(3)

$$G_{\rm DS} = g_{\rm m,i} \xi_{\rm D} + G_{\rm DS,i} \tag{4}$$

where $g_{m,i}$ and $G_{DS,i}$ respectively denote the transconductance and output conductance of the underlying FDSOI. In Equation (5), $g_{m,i}$ and $G_{DS,i}$ are positive; therefore, ζ_D is the only factor that causes the G_D to be negative. In Equation (3), ζ_D is determined by the coupling capacitance C_{GD} and by the capacitance matching between C_{FE} and C_{MOS} . Thus, it is possible to increase ζ_D by increasing $|C_{FE}|$ or decreasing C_{GD} so that G_{DS} tends to zero and the NDR effects are suppressed. As shown in Fig. 3(a), the NDR effects become more pronounced



Figure 1: (a) Structure of the hetero-gate dielectric negative-capacitance field-effect transistor device. (b) $I_{DS} - V_{GS}$ calibration plot of 14 nm FDSOI comparisons between technology computer-aided design (TCAD) simulation results (solid line)and experimental data (circles)[18]. (c) Equivalent capacitance circuit for negative-capacitance field-effect transistor. (d) Gate and drain control circuits.

as the ferroelectric thickness ($T_{\rm FE}$) increases. This is because $|C_{\rm FE}|$ decreases as $T_{\rm FE}$ increases. Equation (3) verifies that the decreases of $|C_{\rm FE}|$ will lead to the decrease of $\zeta_{\rm D}$; thus, the NDR effects will become more obvious.

As $V_{\rm DS}$ increases in the linear region, two competing effects occur. The first is the reduction in $V_{\rm IN'}$ which reduces $I_{\rm DS}$ according to Equation (3). The other is the increase in the lateral electric field, which increases $I_{\rm DS}$. As shown in Fig. 3(a), the second effect dominates and $I_{\rm DS}$ increases as a function of $V_{\rm DS}$ in the linear region. However, after the output characteristic enters the saturated region, $G_{\rm DS,i}$ becomes very small. Therefore, a small $|\xi_{\rm D}|$ will also lead to a negative $G_{\rm DS}$. Fig. 3(b) shows that the $G_{\rm DS}$ is less than zero, and the NDR effects become more obvious as $T_{\rm FE}$ increases.



Figure 3: (a) Output characteristic curves $(I_{DS} - V_{DS})$ at different T_{FE} values. (b) Output conductance plots as a function of V_{DS} at different T_{FE} values.

After the addition of a ferroelectric layer to the dielectric layer of a traditional MOSFET, the amplification of $V_{\rm IN}$ can be demonstrated using Equation (2). Furthermore, $V_{\rm IN}$ increased as a function of $T_{\rm FE}$ in the NCFET. As shown in Fig. 4(a), at $V_{\rm G} = 0.3$ V, the channel electrostatic



Figure 4: (a) Electrostatic potentials of different T_{FE} values at $V_{GS} = 0.3$ V. (b) Electrostatic potentials of different T_{FE} values at $V_{GS} = 0.7$ V.

potential decreases as $T_{\rm FE}$ increases. This is because the amplification of $V_{\rm IN}$ is small when $V_{\rm G}$ is exceptionally low. Moreover, Equation (3) shows that when $T_{\rm FE}$ increases, $\xi_{\rm D}$ decreases, and the channel's electrostatic potential decreases. Conversely, as shown in Fig. 4(b), at $V_{\rm G}$ = 0.7 V, the channel's electrostatic potential increases as $T_{\rm FE}$ increases. This is because the addition of a ferroelectric layer can enhance the electrostatic potential of the channel. As a result, the NDR effects occur at a low $V_{\rm GS}$.

3.2 Inhibition of NDR effects in HDG-NCFET

The NDR effects were suppressed in the HGD-NCFET. As shown in Fig. 5(a), the suppression of the NDR effects became more pronounced as $L_{\rm HK}$ increased. Moreover, Fig. 5(b) shows that when $L_{\rm HK}$ increases to almost half of the gate length (5 nm), the $G_{\rm DS}$ value tends to zero, indicating the disappearance of the NDR effects. An increase in $L_{\rm HK}$ was accompanied by a decrease in the length of the ferroelectric layer, which led to a decrease in $C_{\rm FF}$. Fig. 5(c)



Figure 5: (a) Output characteristic curves as a function of the drain voltage at different L_{HK} values. (b) Output conductance curves as a function of the drain voltage at different L_{HK} values. (c) gate-drain capacitance (C_{GD}) curves as a function of the gate voltage at different L_{HK} values. (d) Electrostatic potentials of different L_{HK} at $V_{GS} = 0.3$ V.



Figure 6: (a) Subthreshold swing (SS) and V_{TH} of HGD-NCFET at different L_{HK} settings. (b) Drain-induced barrier lowering (DIBL) effect of HGD-NCFET at different T_{FE} settings. (c) I_{ON} and I_{OFF} responses of HGD-NCFET at different L_{HK} settings. (d) $I_{\text{ON}}/I_{\text{OFF}}$ responses of HGD-NCFET at different L_{HK} settings.

illustrates that $C_{\rm GD}$ decreases as $L_{\rm HK}$ increases. Equation (3) indicates that reducing $C_{\rm FE}$ and $C_{\rm GD}$ will increase $\xi_{\rm D}$. This results in a larger $V_{\rm IN}$ as $L_{\rm HK}$ increases at the same $V_{\rm DS}$. Therefore, as shown in Fig. 5(d), the NDR effects are sup-

pressed because the channel electrostatic potential increases with increasing $L_{\rm HK}$. It was proposed in paper [11] that the NDR effect could be suppressed by increasing the extension length of the drain region, but the NDR effect did not completely disappear with the extension of the drain. And from the transfer characteristic curve, it can be seen that the drain current is decreasing with the increase of the drain length. In the scheme proposed in this paper, the NDR effect is basically completely reduced and the drain current is increased.

To comprehensively compare the performance of the HDG-NCFET with that of the conventional NCFET, the drain-induced barrier lowering (DIBL), SS, threshold voltage (V_{TH}), on-state current (I_{ON}), off-state current (I_{OFF}), and I_{ON}/I_{OFF} were examined. As shown in Fig. 6(a), as T_{FE} increases, SS gradually decreases. When L_{HK} equals to 3 nm, 4 nm, and 5 nm, the SS is lower than that of the NCFET. This is because an increase in T_{FE} leads to a decrease in $|C_{FE}|$, thus resulting in better capacitance matching between C_{FE} and C_{MOS} . Similarly, in Fig. 6(a), the V_{TH} values of NCFET and HGD-NCFET are almost the same. As shown in Fig. 6(b), compared to the conven-

tional NCFET without $L_{\rm HK}$, the DIBL effect of the HGD-NCFET is slightly worse. This is because the DIBL effect yields larger $I_{\rm DS}$ outcomes as $V_{\rm DS}$ increases. However, the NDR effects cause I_{DS} to decrease when V_{DS} increases. Therefore, the DIBL effect is apparent when the NDR effects are inhibited. However, the DIBL effect can be mitigated by increasing $T_{\rm FF}$. This is because the increase in $T_{\rm FE}$ causes the channel barrier becoming higher. As illustrated in Fig. 6(c), when $T_{FF} = 2$ nm, the I_{OFF} results of the HGD-NCFET are larger than that of the NCFET. This is because the electrostatic potential of the NCFET being lower than those of the HGD-NCFET at a low V_{cs} . Meanwhile, I_{OFF} decreases as T_{FE} increases. Furthermore, I_{ON} increases as a function of T_{FE} . This is because the SS decreases rapidly as $T_{\rm FE}$ increases. As shown in Fig. 6(d), when $T_{\rm FF}$ is equal to 2 nm and 2.5 nm, the $I_{\rm ON}/I_{\rm OFF}$ values are close to those of NCFET at different L_{HK} settings. However, at $T_{\text{FF}} = 3 \text{ nm}$ and $L_{\text{HK}} = 5 \text{ nm}$, the $I_{\text{ON}}/I_{\text{OFF}}$ values of the HGD-NCFET are larger than those of the NCFET.

The analogue/RF characteristics of the HGD-NCFET were analyzed by studying its small signal. Fig. 7(a) illustrates the total capacitance (C_{GG}) of HGD-NCFET



Figure 7: (a) total capacitance (C_{GG}) curves as a function of the gate voltage at different L_{HK} values. (b) transconductance (g_m) curves as a function of the gate voltage at different L_{HK} values. (c) g_m curves as a function of the gate voltage at different T_{FE} values. (d) C_{GG} curves as a function of the frequency at different T_{FE} values.


Figure 8: (a) implementation of CMOS inverter employing HGD-NCFET. (b) voltage transfer characteristic curves of inverter composed of NCFET and HGD-NCFET. (c) voltage transfer characteristic curves of inverter composed of HGD-NCFET at different $T_{\rm FF}$ values. (d) input-output waveform of inverter composed of NCFET and HGD-NCFET.

under different L_{HK} values at $T_{FF} = 2$ nm. It can be seen that C_{GG} decreases with the increase of L_{HK} . This is because replacing ferroelectricity on the drain side with a high- κ material leads to a reduction in $C_{GD'}$ as shown in Fig. 5(c). Therefore, as the L_{HK} increases, the C_{GG} will decrease. Enhancing the transconductance (g_m) of transistors can significantly impact analogue circuitry. This improves amplifier performance, enhances linearity, reduces distortion, increases interference immunity, and lowers power consumption. Therefore, studying the g_m of HGD-NCFET is necessary. Fig 7.(b) shows the $g_{\rm m}$ of HGD-NCFET under different $L_{\rm HK}$ values at $T_{\rm FE}=2$ nm. The results indicate that g_m slightly increases with an increase in $L_{\mu\kappa}$ and surpasses that of NCFET. Meanwhile, as shown in Fig 7.(c), increasing $T_{\rm FE}$ significantly enhances the value of g_m . This is because an increase in $T_{\rm FF}$ results in a higher effective gate electric field of the

HGD-NCFET. Fig 7.(d) shows the curve of C_{GG} as a function of frequency. It is evident that C_{GG} remains stable within the range of 10Hz to 100GHz, indicating the device's stable operation in the low, high, and ultra-high frequency.

To expand the study of HGD-NCFET to circuits, we designed a CMOS inverter comprising of n-type and ptype HGD-NCFET, as shown in Fig. 8(a). The simulation results of the voltage transfer characteristics of the inverter are shown in Fig. 8(b). It is evident that the voltage transfer curves of the NCFET and HGD-NCFET are similar in steepness. Furthermore, Fig. 8(c) illustrates that the voltage transfer curve of the HGD-NCFET becomes steeper as the $T_{\rm FE}$ value increases at $L_{\rm HK} = 5$ nm. This is because the inner gate voltage of the HGD-NCFET is amplified more strongly as $T_{\rm FF}$ increases. Fig. 8(d) shows the variation in transient response of the inverter, where $t_{\rm PHL}$ and $t_{\rm PLH}$ represent the transition delay from high to low and from low to high voltage, respectively. The $t_{\rm PHL}$ of the HGD-NCFET is slightly smaller than that of the NCFET, while the $t_{\rm PLH}$ remains almost constant for both. This indicates that the transfer speed of the HGD-NCFET is faster compared to the NCFET.

4 Conclusion

In this study, an HGD-NCFET was proposed to suppress the NDR effects in NCFET by partly replacing the ferroelectric layer with a high-k material on the drain side. The results showed that this structural device can improve the coupling factor between the gate and the drain to increase the electrostatic potential of the channel. The suppression of the NDR effects became more prominent when the length of high-k material increased. In addition, compared with the traditional NCFET, HGD-NCFET had a steeper subthreshold swing when the length of the high-k material was almost half of the channel length. Simultaneously, the DIBL effect was mitigated with an increase in the ferroelectric thickness. Finally, the switching current ratio of the HGD-NCFET was essentially the same or even higher than that of the traditional NCFET. Therefore, compared with traditional NCFET, HGD-NCFET not only has similar electrical performances but also suppresses the NDR effects. HGD-NCFET has a higher transconductance than NCFET. Additionally, the inverter composed of HGD-NCFET exhibits a shorter transmission delay. In future investigations, we will examine the DIBL effect of HGD-NCFET as its suppression deteriorates with the increase of $L_{\rm HK}$. The preliminary idea is to better suppress the DIBL in HGD-NCFET by modifying the parameters of the spacer. In addition, we will look for effective ways to further reduce the transmission delay of the HGD-NCFET.

5 Acknowledgments

This work was supported by National Natural Science Foundation of China gant 62071160, Zhejiang Provincial Natural Science Foundation of China grant LY22F040001, and Hangzhou Dianzi University gratuate research innovation fundation grant CXJJ2023054.

6 References

1. G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior," *IEEE Transactions on Electron* *Devices*, vol. 65, no. 11, pp. 5130-5136, Nov. 2018, https://doi.org/10.1109/TED.2018.2870519

- G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Above-Threshold Behavior," *IEEE Transactions on Electron Devices*, vol. 66, no. 3, pp. 1591-1598, March 2019, <u>https://doi.org/10.1109/TED.2019.2892186</u>
- J. Jo and C. Shin, "Negative Capacitance Field Effect Transistor With Hysteresis-Free Sub-60-mV/ Decade Switching," *IEEE Electron Device Letters*, vol. 37, no. 3, pp. 245-248, March 2016, <u>https://doi.org/10.1109/LED.2016.2523681</u>
- D. Kwon, K. Chatterjee, A. J. Tan, and A. K. Yadav, "Improved Subthreshold Swing and Short Channel Effect in FDSOI n-Channel Negative Capacitance Field Effect Transistors," *IEEE Electron Device Letters*, vol. 39, no. 2, pp. 300-303, Feb. 2018, <u>https://doi.org/10.1109/LED.2017.2787063</u>
- M. Hoffmann, S. Slesazeck, and T. Mikolajick, "Progress and future prospects of negative capacitance electronics: A materials perspective," APL Materials, vol. 9, no. 2, pp. 020902.1-020902.12,Feb. 2021,

https://doi.org/10.1063/5.0032954

- J. Zhou, G. Han, and J. Li, "Negative Differential Resistance in Negative Capacitance FETs," *IEEE Electron Device Letters*, vol. 39, no. 4, pp. 622-625, April 2018, <u>https://doi.org/10.1109/LED.2018.2810071</u>
- F. I. Sakib, M. A. Hasan, and M. Hossain, "Exploration of Negative Capacitance in Gate-All-Around Si Nanosheet Transistors," *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 5236-5242, Nov. 2020, <u>https://doi.org/10.1109/TED.2020.3025524</u>
- D. Kwon, S. Cheema, N. Shanker, and K. Chatterjee, "Negative Capacitance FET With 1.8-nm-Thick Zr-Doped HfO2 Oxide," *IEEE Electron Device Letters*, vol. 40, no. 6, pp. 993-996, June 2019, <u>https://doi.org/10.1109/LED.2019.2912413</u>
- G. Pahwa, T. Dutta, and A. Agarwal, "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance—Part II: Model Validation," *IEEE Transactions on Electron Devices*, vol. 63, no. 12, pp. 4986-4992, Dec. 2016, <u>https://doi.org/10.1109/TED.2016.2614436</u>
- H. Agarwal, P. Kushwaha, J. P. Duarte, and Y. Lin, "Engineering Negative Differential Resistance in NCFETs for Analog Applications," *IEEE Transactions on Electron Devices*, vol. 65, no. 5, pp. 2033-2039, May 2018, <u>https://doi.org/10.1109/TED.2018.2817238</u>
- 11. K. Vanlalawmpuia and A. S. Medury, "Engineering negative differential resistance in negative capacitance Quad-FinFET," *Materials Science and Engineering*, vol.297, pp. 116725.1-116725.9, Nov 2023, <u>https://doi.org/10.1016/j.mseb.2023.116725</u>

- S. Gupta, M. Steiner, A. Aziz, V. Narayanan, S. Datta, and S. K. Gupta, "Device-Circuit Analysis of Ferroelectric FETs for Low-Power Logic," *IEEE Transactions on Electron Devices*, vol. 64, no. 8, pp. 3092-3100, Aug. 2017, https://doi.org/10.1109/TED.2017.2717929
- T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance Evaluation of 7-nm Node Negative Capacitance FinFET-Based SRAM," *IEEE Electron Device Letters*, vol. 38, no. 8, pp. 1161-1164, Aug. 2017, https://doi.org/10.1109/LED.2017.2712365
- H. Zhou, "Negative Capacitance, n-Channel, Si Fin-FETs: Bi-directional Sub-60 mV/dec, Negative DIBL, Negative Differential Resistance and Improved Short Channel Effect," 2018 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 2018, pp. 53-54, https://doi.org/10.1109/VLSIT.2018.8510691
- 15. K. Lee, S. Kim, and J. H. Lee, "Suppression of reverse drain induced barrier lowering in negative capacitance FDSOI field effect transistor using oxide charge trapping layer," *Semiconductor Science and Technology*, vol. 35, no. 12, p. 125003, Oct. 2020, https://sci-hub.se/10.1088/1361-6641/abb5e4
- B. Awadhiya, P. N. Kondekar, and A. D.Meshram, "Understanding negative differential resistance and region of operation in undoped HfO2-based negative capacitance field effect transistor," *Applied Physics A*, vol. 125, no. 427, pp. 1-7, Jun. 2019, <u>https://doi.org/10.1007/S00339-019-2718-2</u>
- Z. Xie,W. Lü, M. Guo, and M. Zhao, "LoGHeD: an effective approach for negative differential resistance effect suppression in negative-capacitance transistors," *Semiconductor Science and Technology*, vol. 37, no. 3, pp. 035001.1-035001.7, Oct. 2022, <u>https://doi.org/10.1088/1361-6641/ac4819</u>
- Q. Liu, "High performance UTBB FDSOI devices featuring 20nm gate length for 14nm node and beyond," 2013 IEEE International Electron Devices Meeting, Washington, DC, USA, 2013, pp. 9.2.1-9.2.4, https://doi.org/10.1109/IEDM.2013.6724592
- 19. Sentaurus Device User Guide 2018 Version O-2018.06, synopys(Mountain View, CA).
- C. -I. Lin, A. I. Khan, S. Salahuddin, and C. Hu, "Effects of the Variation of Ferroelectric Properties on Negative Capacitance FET Characteristics," *IEEE Transactions on Electron Devices*, vol. 63, no. 5, pp. 2197-2199, May 2016, https://doi.org/10.1100/TED.2016.2514782

https://doi.org/10.1109/TED.2016.2514783

 D. Kwon, S. Cheema, Y. K. Lin, and Y. H. Liao, "Near Threshold Capacitance Matching in a Negative Capacitance FET With 1 nm Effective Oxide Thickness Gate Stack," *IEEE Electron Device Letters*, vol. 41, no. 1, pp. 179-182, Jan. 2020, <u>https://doi.org/10.1109/LED.2019.2951705</u>

- 22. A. K. Saha and S. K. Gupta, "Negative capacitance effects in ferroelectric heterostructures: A theoretical perspective," *Journal of Applied Physics*, vol. 129, no. 8, pp. 080901.1-080901.9,Feb. 2021, https://doi.org/10.1063/5.0038971
- C. -I. Lin, A. I. Khan, S. Salahuddin, and C. Hu, "Effects of the Variation of Ferroelectric Properties on Negative Capacitance FET Characteristics," *IEEE Transactions on Electron Devices*, vol. 63, no. 5, pp. 2197-2199, May 2016, https://doi.org/10.1100/TED.2016.25117202

https://doi.org/10.1109/TED.2016.2514783



Copyright © 2024 by the Authors. This is an open access article distributed under the Creative Com-

mons Attribution (CC BY) License (https://creativecommons.org/licenses/by/4.0/), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Arrived: 21.01.2024 Accepted: 15.03.2024

Boards of MIDEM Society | Organi društva MIDEM

MIDEM Executive Board | Izvršilni odbor MIDEM

President of the MIDEM Society | Predsednik društva MIDEM

Prof. Dr. Barbara Malič, Jožef Stefan Institute, Ljubljana, Slovenia

Honorary president: Prof. Dr. Marko Topič, UL, Faculty of Electrical Engineering, Slovenia

Vice-presidents | Podpredsednika

Prof. Dr. Janez Krč, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia Dr. Iztok Šorli, Mikroiks d.o.o., Ljubljana, Slovenia

Secretary | Tajnik

Olga Zakrajšek, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia

MIDEM Executive Board Members | Člani izvršilnega odbora MIDEM

Prof. Dr. Slavko Bernik, Jožef Stefan Institute, Slovenia Assoc. Prof. Dr. Miha Čekada, Jožef Stefan Institute, Ljubljana, Slovenia Prof. DDr. Denis Đonlagić, UM, Faculty of Electrical Engineering and Computer Science, Maribor, Slovenia Prof. Dr. Vera Gradišnik, Tehnički fakultet Sveučilišta u Rijeci, Rijeka, Croatia Mag. Leopold Knez, Iskra TELA, d.d., Ljubljana, Slovenia Mag. Mitja Koprivšek, ETI Elektroelementi, Izlake, Slovenia Asst. Prof. Dr. Gregor Primc, Jožef Stefan Institute, Ljubljana, Slovenia Prof. Dr. Janez Trontelj, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia Dr. Danilo Vrtačnik, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia

Supervisory Board | Nadzorni odbor

Dr. Drago Resnik, retired, Slovenia Prof. Dr. Franc Smole, retired, Slovenia Prof. Dr. Drago Strle, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia

Court of honour | Častno razsodišče

Darko Belavič, retired, Slovenia Prof. Dr. Danjela Kuščer Hrovatin, Jožef Stefan Institute, Ljubljana Dr. Hana Uršič Nemevšek, Jožef Stefan Institute, Ljubljana, Slovenia

Informacije MIDEM Journal of Microelectronics, Electronic Components and Materials ISSN 0352-9045

Publisher / Založnik: MIDEM Society / Društvo MIDEM Society for Microelectronics, Electronic Components and Materials, Ljubljana, Slovenia Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale, Ljubljana, Slovenija

www.midem-drustvo.si