

10 Gb/s $2^{15}-1$ pseudo-random binary sequence generator

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Abstract: A 10 Gb/s pseudo-random binary sequence generator with a pattern length of $2^{15} - 1$ is presented. It is using a novel generation method, practically implemented as a single-stage linear-feedback shift register. The new method is suitable for the highest data rates (several tens of Gb/s), since it allows operation at clock frequencies higher than the traditionally-designed multiple-stage chain, made of the same type of D-flip-flops. Most of the required delays in the PRBS generator are derived from microwave transmission lines instead from active logic devices, thus much simplifying the circuit design. The generator produces the maximum-length bit sequence defined by the $1 + x^{14} + x^{15}$ polynomial and is implemented by a discrete design at 10 Gb/s data rate using commercially-available high-speed logic.

Key words: pseudo-random binary sequence, high-speed logic, linear-feedback shift register, maximum-length sequences.

Pseudonaključni podatkovni izvor z bitno hitrostjo 10 Gbit/s in dolžino zaporedja $2^{15} - 1$

Povzetek: V prispevku je predstavljen izvor psevdonaključnih podatkov z bitno hitrostjo 10 Gbit/s in dolžino zaporedja $2^{15} - 1$. Izvor izkorišča novo metodo za generiranje psevdonaključnega zaporedja, ki temelji na pomikalnem registru z linearno povratno vezavo, sestavljenem iz ene same (aktivne) stopnje. Nova metoda je primerna za najvišje bitne hitrosti (od nekaj deset Gbit/s naprej), saj omogoča delovanje pomikalnega registra pri višjih taktnih frekvencah, kot običajno izvedeni pomikalni registri (sestavljani iz verige enakih D flip flopov). Večina potrebnih zakasnitev v izvoru je izvedena s pomočjo mikrovalovnih prenosnih linij (namesto z aktivnimi stopnjami), kar znatno poenostavi načrtovanje vezja izvora. Izvor generira zaporedje maksimalne dolžine, določene s polinomom $1 + x^{14} + x^{15}$, in je sestavljen iz razpoložljivih posamičnih logičnih vezij ter obratuje pri taktni frekvenci 10 GHz.

Ključne besede: psevdonaključni podatkovni izvor, hitra logična vezja, pomikalni register z linearno povratno vezavo, zaporedja maksimalne dolžine

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1. Introduction

Pseudo-random binary sequences, usually maximum-length sequences (m-sequences), are widely used in communications systems. For example, they are used as spreading sequences in direct-sequence spread-spectrum systems (CDMA, GPS, etc.), as white noise, as scrambling and synchronization codes, they are found in many cryptosystems and radar applications, and last but not least they are employed as test-data patterns in Bit-Error-Rate (BER) optical and radio communication-link measurements and high-speed component and devices testing (i.e. digital devices, photodiodes, amplifiers, etc.). They are deterministic, simple to generate, verify and synchronize on, while their mathematical properties resemble random data.

The maximum-length sequences are generated by modulo-2 polynomial division with irreducible polynomials. The latter is practically implemented in the form of linear-feedback shift registers [1], where the linearity of the feedback is achieved by modulo-2 addition with EX-OR logic gates, as shown in Fig. 1 for the $1 + x^{n-1} + x^n$ trinomial. Maximum-length sequences of the length $2^n - 1$ (where n is the number of shift-register stages) have several interesting mathematical properties, like the precisely-defined pseudo-random distribution of logical ones and zeros, a two-level autocorrelation function (ideal for the radar application) and a frequency spectrum including equally-spaced, equal-amplitude spectral lines (ideal for the white noise). The maximum-length sequences have 2^{n-2} logic-level transitions, enabling a simple pattern-length synchronization by a

ripple counter [2, 3]. For example, the sequence defined by the $1 + x^{14} + x^{15}$ polynomial has exactly 8192 logic-level transitions.

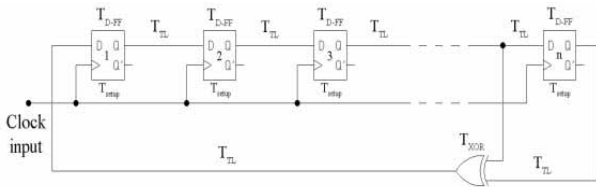


Figure 1: Typical PRBS generator implementation for the $1 + x^{n-1} + x^n$ trinomial.

The maximum operating clock frequency of the traditionally-implemented PRBS generator, as illustrated in Fig. 1, is limited by the sum of several delays in the circuit section comprising the XOR gate, since the latter has the highest delay of all. The clock period T is defined in Eq. 1 as

$$T_{D-FF} + T_{XOR} + T_{TL} + T_{setup} \leq T, \tag{1}$$

where T_{D-FF} and T_{XOR} denote propagation delays of the flip-flop and XOR gate, respectively, T_{TL} is the sum of all delays of the connecting transmission lines in this circuit section and T_{setup} is the flip-flop's setup time (valid data before the clock transition). For the integrated PRBS generators with the highest clock frequencies beyond 100 GHz, the propagation delays in the logic devices present the main delay contribution and therefore the maximum-clock-frequency limitation [3, 4].

2. Single-stage PRBS generation method

The single-stage linear-feedback shift register uses a single D-flip-flop and several transmission lines (for example microstrip, coaxial, stripline, etc.) to generate the delay required by the register length [5]. The D-flip-flop is required for the signal regeneration (retiming and reshaping). Fig. 2 illustrates the new PRBS generator, including only a single D-flip-flop, an EX-OR gate and the required transmission (delay) lines.

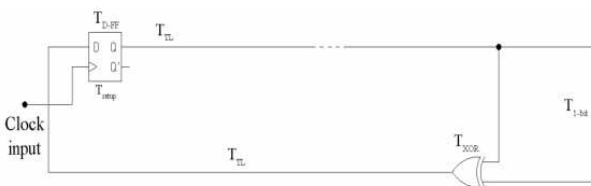


Figure 2: Single-stage PRBS generator implementation for the $1 + x^{n-1} + x^n$ trinomial.

The total loop delay must be equal to the polynomial order times the clock period T , therefore the delays shown in Fig. 2 can be written in Eq. 2 as

$$T_{D-FF} + T_{XOR} + T_{TL} + T_{setup} \leq (n - 1) * T, \tag{2}$$

where T_{D-FF} and T_{XOR} denote propagation delays of the flip-flop and XOR gate, respectively, T_{TL} is the sum of all transmission-lines delays (without the T_{1-bit}), T_{setup} is the flip-flop's setup time (valid data before the clock transition) and n is the polynomial order. In an extreme case, the maximum clock-frequency increase of the single-stage over the conventional design is $n - 1$. This applies for the trinomial shown and the fact that the T_{TL} remains the same in both designs, while T_{D-FF} being much higher in the single-stage design. In practice such an increase can hardly be accomplished, since the propagation delay of flip-flops is getting smaller with the increased toggle-rate capability (i.e. a flip-flop with high propagation delay and high toggle rate does not exist).

When compared to the conventional LFSR circuit, shown in Fig. 1, the new PRBS circuit has many advantages: simplicity, less logic devices and lower power consumption. A single-D-flip-flop design also eliminates the complex clock-distribution circuits required for several D-flip-flops in conventional high-speed LFSR designs. Finally, the clock frequency can be increased to the upper D-flip-flop toggle limit and the latter is usually much higher than the clock-frequency limit imposed by propagation delays in a traditional multi-stage designs, especially in the case of discrete-packaged devices. The discrete-packaged logic has a significant propagation delay contribution from the package itself, which severely limits the performance, particularly at and above 10 GHz toggle frequencies. The new PRBS generation method is not limited by the flip-flop's propagation delay T_{D-FF} , since the latter can be compensated by a shorter transmission-line delay T_{TL} (Eq. 2).

The single-stage method's drawbacks include: the PRBS polynomial depends on the sum of the delays of the active logic and the transmission lines, respectively, and the PRBS pattern length is limited by the insertion loss, dispersion of the transmission lines used and the input sensitivity of the regeneration stage. The design works only at a single clock frequency (with the typical range of a few percent around the central frequency). If the design is manufactured with fixed transmission lines (i.e. on a printed-circuit board), the polynomial can not be changed easily, except if broadband switches are used for the selected transmission-line lengths. However, almost all high-data-rate PRBS generators (employing the traditional generation method) with the output data rates in excess of several tens of Gb/s

and beyond, are also optimized for a single polynomial operation [3, 4].

3. 10 Gb/s $2^{15}-1$ PRBS generator

The generator is a standalone unit and comprises several modules as shown on the block diagram in Fig. 3: PRBS core, pattern-length synchronization divider, clock divider, reference oscillator and multipliers, power supply, maximum-length sequence detector and auto start, phase shifter with amplifier and finally the D-type flip-flop.

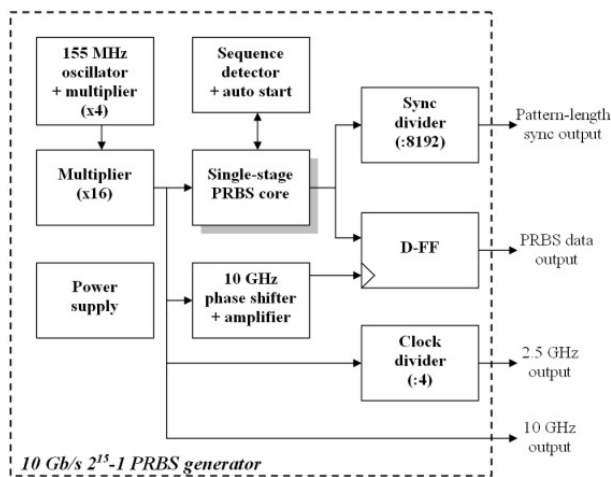


Figure 3: Block diagram of the 10 Gb/s $2^{15}-1$ PRBS generator.

The most challenging part was the single-stage PRBS core, operating at 9.95 Gb/s as a standard OC-192 (STM-64) bitrate generator. The core consists of a single (retiming) stage (D-type flip-flop), first 2:1 multiplexer used as a modulo-2 adder (XOR gate) and second one used as a logic-one insertion stage for the auto-start functionality, two buffers used as reshaping and fanout stages and finally transmission lines for the remaining delay of the linear-feedback shift register. The PRBS core is shown in Fig. 4.

The PRBS-core PCB holds also the pattern-length synchronization dividers (three :16 and one :2 divider) and also the D-type flip-flop used as the final regeneration stage for the output PRBS data. The latter is a low-jitter (3 ps_{pp} deterministic and 0.3 ps_{rms} random) high-speed device (rise/fall times typically 16 ps) for the best possible PRBS-data quality. The eye diagram of the output PRBS data, measured by a sampling oscilloscope with a 40 GHz bandwidth, is shown in Fig. 5. The PRBS core is a fully differential design using differential current-mode logic (CML) devices and interconnected by differential microstrip transmission lines. The used 4-layer FR-4

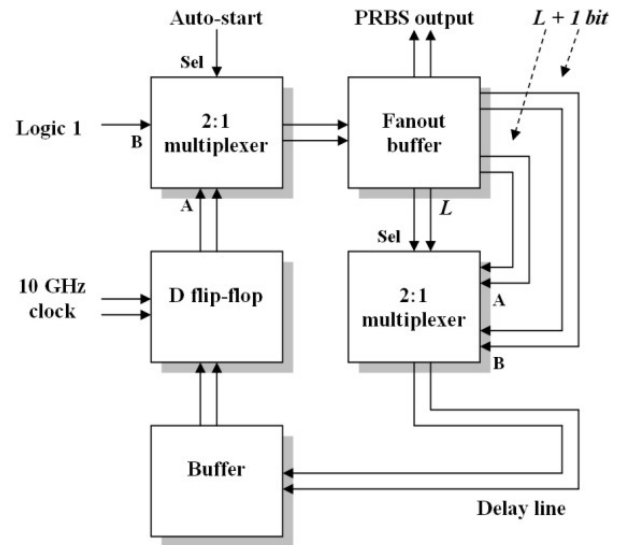


Figure 4: Simplified diagram of the differential PRBS core.

laminar is not an optimal choice due to the noticeable loss and dispersion throughout the whole frequency range (DC to more than 10 GHz), but we found it as satisfactory, since its limitations do not impair the differential signalling as much as it would be the case for the single-ended signalling. All microstrip transmission-line interconnections between the logic devices are point-to-point to keep and preserve the signal integrity as high as possible. The PRBS differential output has the CML levels and is DC coupled, while the synchronization differential output has the emitter-coupled logic (ECL) levels and is AC coupled. Describing the PRBS core in more detail (i.e. on the schematic level) is beyond the scope of this article, so it is excluded from the further discussion.

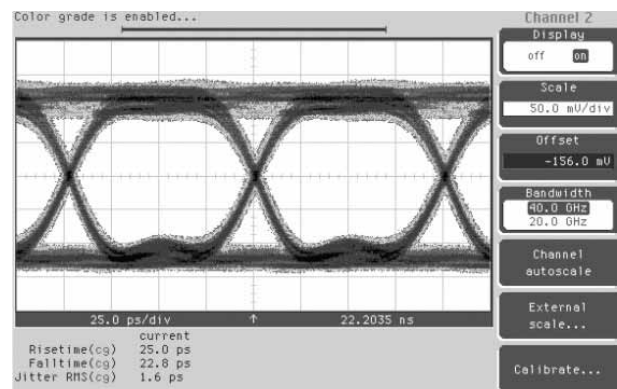


Figure 5: Eye diagram of the output PRBS data.

The calculation of the maximum operating clock frequencies for both methods reveals a big favor to the new single-stage method. If we take into account the real delay values of the traditional linear-feedback shift-register implementation ($T_{D-FF}=215 \text{ ps}$, $T_{XOR}=135 \text{ ps}$,

$T_{\text{setup}} = 10$ ps), using Eq. 1 we obtain the maximum clock frequency of 2.2 GHz for 0 ps delay of the interconnecting transmission lines. Realistically, the interconnection delay would be at least 200 ps, which further limits the maximal operating frequency of the traditional design to 1.8 GHz. The single-stage design can operate at maximum toggle limit, which is more than 12 GHz for the used logic devices in the described generator and that is an increase of more than 6 times.

The 10 GHz clock for the generator is derived from a crystal oscillator running at 155 MHz for an ultra-stable frequency and low phase noise. Several multiplier stages (including filtering, amplifying and multiplying) are used for the frequency multiplication, mostly in steps of doubling the frequency. The filtering from 155 MHz up to 620 MHz is done by lumped components, whereas from 1240 MHz and up to 10 GHz by distributed microstrip filters. Two double-layer FR-4 PCBs are used for the multiplier stages and the multiplier from 620 MHz to 10 GHz is enclosed by a brass housing to minimize the electro-magnetic interference with other circuits within the generator box. Two 10 GHz outputs are single-ended with +4 dBm power level and are AC coupled.

A clock frequency divided by 4 (therefore operating at 2.5 GHz) was added to the system to enable compatibility and to extend flexibility when using older equipment (i.e. sampling oscilloscopes or digital communication analyzers). The divider is composed of a 10 GHz buffer and two :2 divider stages. Its differential output has the CML levels and is DC coupled.

All PRBS generators include a stall-protection mechanism in case of the all-zero state in the linear-feedback shift register. In that case, the generator must automatically recover into the normal state. The described generator includes the maximum-length sequence detection and corresponding automatic recovery in the form of insertion a series of logic ones (high level) into the shift register. When it detects a normal operation, i.e. senses the maximum-length sequence, it disengages the insertion of logic ones into the register. The detection of the maximum-length sequences is done by analog processing (filtering of the first spectral line) of the synchronization output. When the detector senses a spectral line at $10 \text{ GHz} / 2^{15}-1 = 300 \text{ kHz}$ it automatically stops inserting a logic one into the register.

For the final-regeneration D-flip-flop an optimal clock phase was needed to minimize the deterministic and random timing jitter in the output PRBS data. Therefore a phase shifter operating at 10 GHz with more than 360 degrees phase-tuning range was developed with the accompanying 10 GHz amplifier. The amplifier com-

prises a single high electron mobility transistor (HEMT) on a teflon laminate. The phase shifter is composed of two serially-connected tunable band-pass filters with an intermediate amplifier stage. Each filter is a four-finger interdigital microstrip type with varactor diodes as a tunable elements in each finger. The phase shifter is also built on a 0.5 mm-thick teflon laminate for minimal loss and reliable performance. The final regeneration flip-flop's clock phase is manually adjusted to an optimal position using a resistive trimmer setting the varactor diodes' bias points. The 10 Gb/s PRBS generator prototype is shown in Fig. 6.

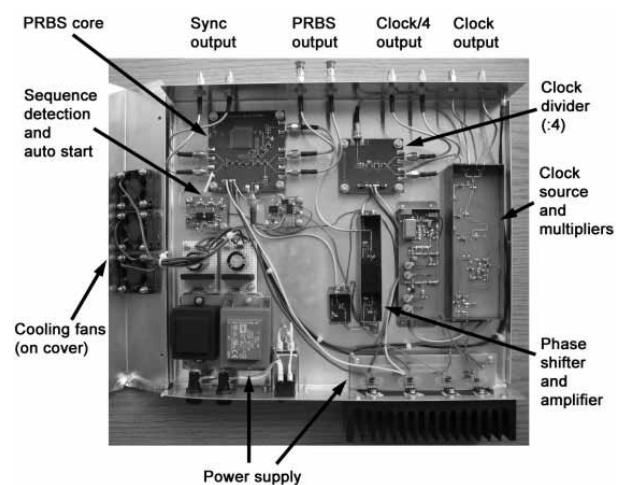


Figure 6: Photograph of the 10 Gb/s $2^{15}-1$ PRBS generator.

One of the most simple verifications for the correct operation of the PRBS generators is to check the frequency spacings between the spectral lines of the output PRBS data. The latter must be in precise agreement with the clock frequency divided by the pattern length. In this case the spacing must be $9.95 \text{ GHz} / 2^{15}-1 = 304 \text{ kHz}$. If the spacing is wider, then the sequence does not

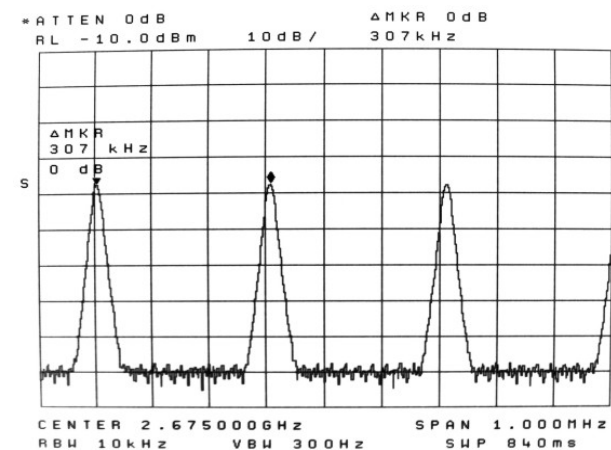


Figure 7: Frequency spacing between the spectral lines of the PRBS data.

have the maximum length and the operation is erroneous. The spacings between the spectral lines of the output PRBS data are shown in Fig. 7 and prove that the sequence has the maximum length (the marker measurement on the used spectrum analyzer has limited resolution and does not show exact spectral-line spacing).

4. Conclusion

The method and design of a PRBS generator operating at 10 Gb/s bitrate was presented. The single-stage implementation of the linear-feedback shift register uses a single retiming stage (D-type flip-flop). If the same logic devices (as built in the generator) would be used in a traditional implementation (the multi-stage chain), the maximum clock frequency would be approximately 6 times lower than the clock frequency of the single-stage implementation. The latter is actually equal to the maximum toggle limit of the devices. The single-stage method applies also for the polynomial divider in a PRBS receiver (i.e. bit-error-rate receiver). The 10 Gb/s PRBS generator, producing a pseudo-random pattern length of $2^{15}-1$, provides a good data quality with the timing jitter of only $1.6 \text{ ps}_{\text{rms}}$ at the middle of the eye crossing. Although the PRBS-core circuit was made on the cheap FR-4 laminate, a good performance was achieved due to the fully-differential design. The generator includes also a high-stability clock source and features the pattern-length synchronization. The single-stage-method principles shown in this article are fully scalable to higher clock frequencies. This applies especially for the case of integrated monolithic implementations suitable for and required by the next-generation communication-link bitrates of 80 and 160 Gb/s.

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